Service Repair Documentation
Level 3 –S88

Release	Date	Department	Notes to change
R 1.0		BenQ S CC CES	New document

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1 Introduction

1.1 Purpose

This Service Repair Documentation is intended to carry out repairs on BenQ repair level 3.

1.2 Scope

This document is the reference document for all BenQ authorised Service Partners which are released to repair BenQ Mobile phones up to level 3.

1.3 Terms and Abbreviations

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2 List of available level 3 parts

Product	Order Number	Description CM
S88	L50634-Z97-C553	CONN DC PWR PA05302-QNJ BQ2B.13120.021
S88	L50634-Z97-C633	CONN AXK7L20227 BQ2K.L1096.020
S88	L50634-Z97-C634	CONN AXK7L30227 BQ2K.L1096.030
S88	L50634-Z97-C635	CONN AXK734245 BQ2K.L1165.034
S88	L50634-Z97-C636	CONN BF1-0115 BQ2K.L1235.010
S88	L50634-Z97-C554	CONN ANT RF05301-PG BQ2K.M0001.001
S88	L50634-Z97-C556	CONN BAT3PD2.5AB303Y-C0G1 BQ2K.N0080.001
S88	L50634-Z97-C558	CONN I/O 10P P0.5 BQ2K.N0081.001
S88	L50634-Z97-C637	CONN SIM BM05306-D18 BQ2K.N5030.011
S88	L50634-Z97-C638	CONN MEMORY 11TFC-001 BQ2K.N5035.001
S88	L50615-Z77-C287	SWI RF ANTENNA MS-147 BQ6J.50017.001
S88	L50615-Z77-C262	SWI 12V50MA EVQPUM02K BQ6B.40043.031
S88	L50615-Z77-C285	SWI EVQQ7GA50 BQ6B.40043.081
S88	L50615-Z77-C286	SWI SLIDE SSSS811101 BQ6B.40081.001
S88	L50640-D5121-D670	DISDIODE ARR DAN222 BQ8C.00222.0A0
S88	L50640-D124-D670	DISDIODE VAR HVD358BKRF-E BQ8C.00358.090
S88	L50640-D5110-D670	DISDIODE RB520S-30 BQ8C.00520.080
S88	L50640-D123-D670	DISDIODE UCLAMP 0505A BQ8C.0505A.010
S88	L50640-D5122-D670	DISDIODE NSR0320MW2T1G BQ8C.1R002.081
S88	L50640-D5123-D670	DISDIODE RB161M-20 BQ8C.1R002.08Q
S88	L50640-D5124-D670	DISDIODE PMEG2020EJ BQ8C.2R002.A8F
S88	L50640-D3142-D670	DISDIODE ZEN 6.06-6.33V BQ8C.6R205.03F
S88	L50640-D5125-D670	DISDIODE 1PS79SB30 BQ8C.R2004.A84
S88	L50640-D5126-D670	DISDIODE PMEG2005EB BQ8C.R5002.A80
S88	L50664-F6101-J	CAP ARRAY 100P 50V COG BQ7G.61012.0C2
S88	L50664-F6220-K	CAP ARRAY 22P 50V J0805S BQ7G.62203.0C1
S88	L50645-G200-Y28	OSC 48MHZ 30PF 50PPM BQ8B.24800.301
S88	L50645-F102-Y48	OSCCRYST 26MHZ U-860-1-1 BQ8B.30026.D02
S88	L50645-F102-Y63	OSCCRYST 26MHZ NX2520SA BQ8B.32600.F02
S88	L50645-F102-Y64	OSCCRYST 30MHZ 30MHZ 8PF BQ8B.33000.B02
S88	L50645-F102-Y49	OSCCRYST 32.768 DST520 BQ8B.33276.705
S88	L50640-C4083-D670	DIS TRANS ARRAY PUMH10 BQ8D.00010.A1F
S88	L50640-C2143-D670	DISTRANS BC807-40W PNP BQ8D.00807.A1K
S88	L50630-C1198-D670	DISTRANS FDG6303N BQ8D.06303.03K
S88	L50630-C1199-D670	DISTRANS FDG6304P BQ8D.06304.03K
S88	L50630-C1187-D670	DISTRANS FET FDC6506P BQ8D.06506.030

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S88	L50622-f4103-k	NTC 10K 0402 NTH5G BQ6J.60009.001
S88	L50640-D118-D670	DISDIODE TVS TVM0A080MI BQ6J.80009.001
S88	L50640-D110-D670	DISDIODE TVM0A090MIRY BQ6J.80009.011
S88	L50640-D109-D670	DISDIODE TVM1A090KAR BQ6J.80011.011
S88	L50640-D119-D670	DISDIODE TVS SFI0508-050R BQ6J.80022.011
S88	L50645-K280-Y420	FILSAW 1842.5MHZ SAFEH1G BQ6J.10151.001
S88	L50645-K280-Y421	FILSAW 942.5MHZ SAFEH942M BQ6J.10152.001
S88	L50645-K280-Y437	FILSAW 1960MH SAFEH1G96FB BQ6J.10154.001
S88	L50645-K280-Y425	FIL 2.45GHZ LFB212G45B BQ6J.10168.011
S88	L50645-K280-Y453	FIL LFA24-2A1A144MT BQ6J.10189.001
S88	L50645-K280-Y454	FIL NFM18PS474R0J BQ6J.10194.031
S88	L50610-U6243-D670	IC INTF TWL3025BZGMR BQ7A.03025.B0U
S88	L50610-G6315-D670	IC MCU SH7315 BQ7A.07315.B0U
S88	L50610-U6268-D670	IC BC313141A07-IXF-E4 BQ7A.31314.A0U
S88	L50645-J4683-Y34	IC ASIC D751992AZHHR BQ7A.75199.A0U
S88	L50610-C6385-D670	IC ANA TLV3701CDBVR BQ7C.03701.09J
S88	L50610-B6237-D670	IC LOGI MC74VHC1G08DFT1G BC7C.74108.0ZH
S88	L50610-B6217-D670	IC LOGI MC74VHC1G32DFT1 BQ7C.74132.0ZH
S88	L50610-B6238-D670	IC LOGI SN74LVC1T45DCKR BC7C.74145.0HH
S88	L50610-B6239-D670	IC LOGI SN74AVC24T245ZRGR BC7C.74242.09U
S88	L50610-C6386-D670	IC ANA R1114Q281D-TR-FA BQ7D.01114.A3Y
S88	L50610-C6387-D670	IC ANA R1131N121D-TR-F BQ7D.01131.03B
S88	L50610-C6388-D670	IC ANA CXG1180EQ BQ7D.01180.095
S88	L50610-C6389-D670	IC ANA LT1931AES5 BQ7D.01931.A4B
S88	L50610-C6390-D670	IC ANA TPA2010D1YZFR BQ7D.02010.0K0
S88	L50610-C6391-D670	IC ANA MIC2211-SMYML BQ7D.02211.C3F
S88	L50610-C6392-D670	IC ANA NUF2221W1T2G BQ7D.02221.07Y
S88	L50610-C6393-D670	IC ANA MIC2291-34YML BQ7D.02291.03F
S88	L50610-C6287-D670	IC ANASW NC7SB3157L6X BQ7D.03157.090
S88	L50610-U6247-D670	IC PWR AMP RF3166-E6 BQ7D.03166.0K0
S88	L50610-C6290-D670	IC ANA VR MIC5213-2.8YC5 BQ7D.05213.E3Y
S88	L50610-C6394-D670	IC ANA BH6053GU BQ7D.06053.04U
S88	L50610-C6395-D670	IC ANA ISL6292CCR3Z BQ7D.06292.070
S88	L50610-C6396-D670	IC ANA WM8753LGEFL BQ7D.08753.075
S88	L50610-C6289-D670	IC ANA VR MAS9124A2GC06 BQ7D.09124.03B
S88	L50610-C6397-D670	IC ANA MAX9890AEBL+T BQ7D.09890.070
S88	L50610-U6244-D670	IC IR XCVR HD155165BPEB BQ7D.15516.0FU

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3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Power Supply
- Board Adapter S88
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- Power Supply Cables
- BGA Soldering equipment

Reference: Equipment recommendation V1.6
(downloadable from the technical support page)

4 Required Software for Level 3

- Windows XP
- BenQ Troubleshooting Software XCST Level3

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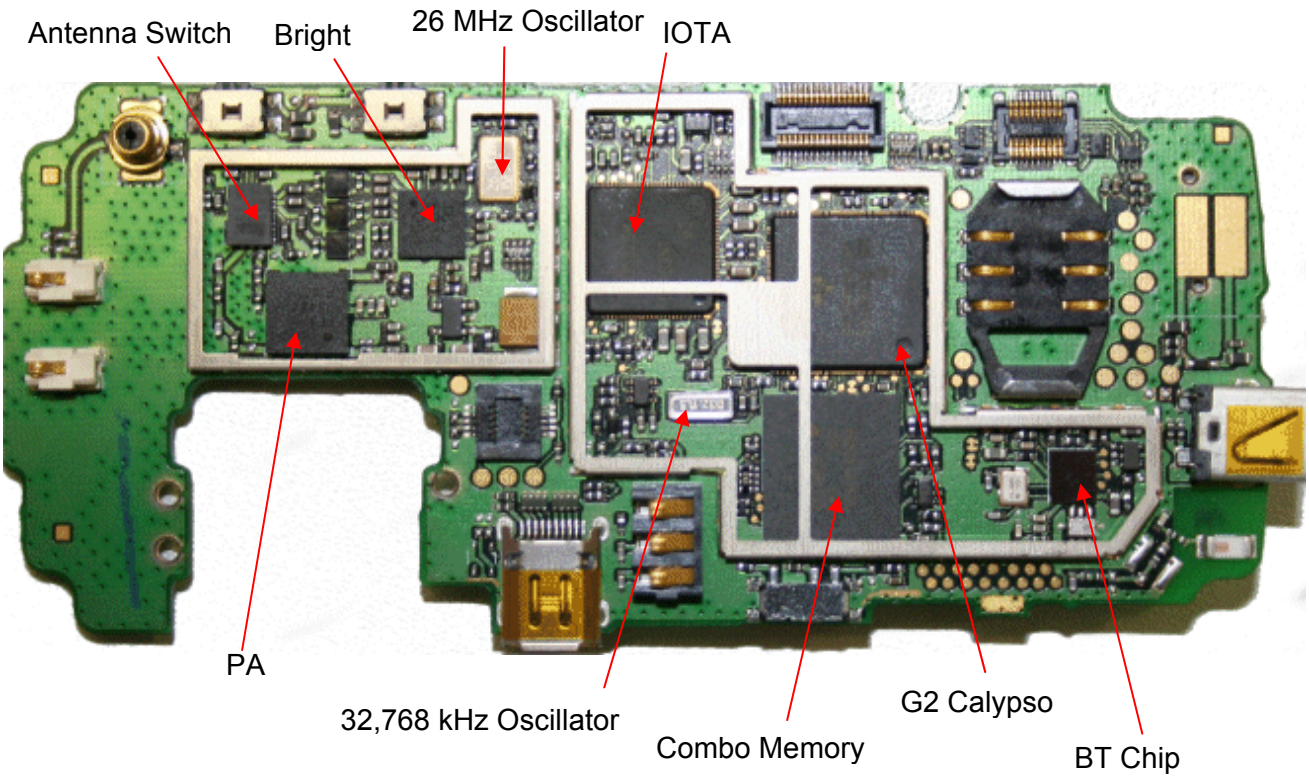
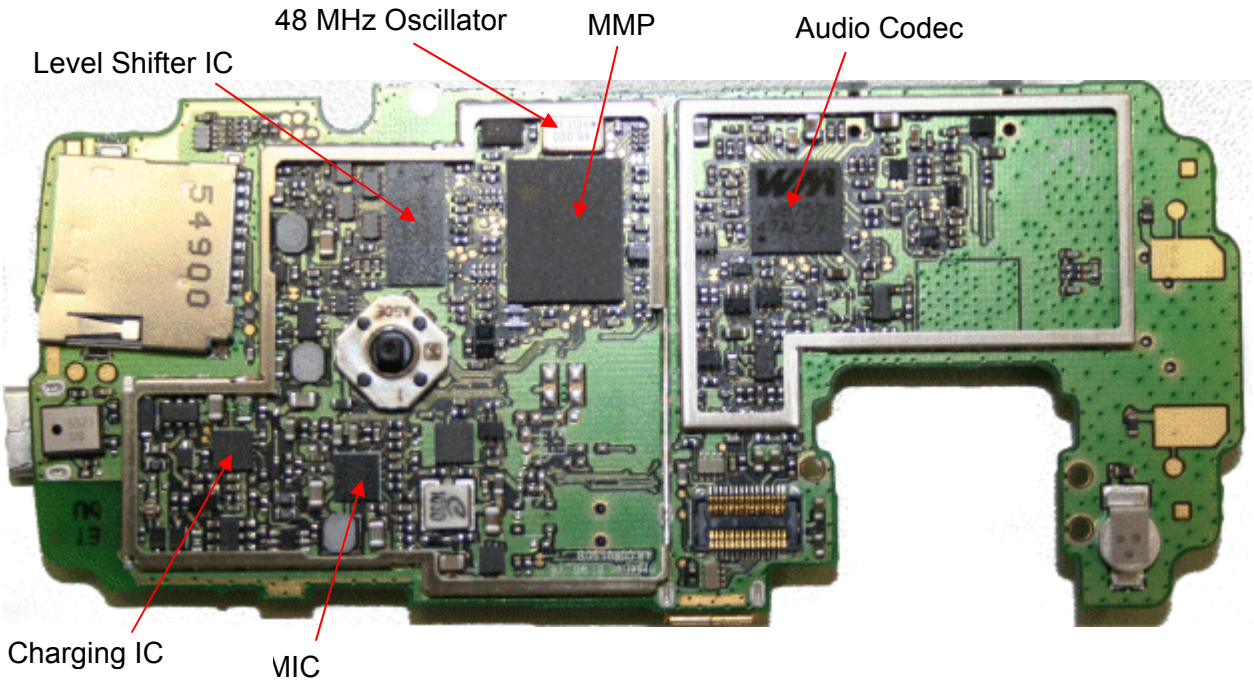
5 PCB Main Board Overview

PCB Main Board Back Side



PCB Main Board Top Side



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6 Radio Part Introduction

The radio part is realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

Transmitter and Receiver are never active at the same time. Simultaneous receiving in the EGSM900 and GSM1800 band is impossible. Simultaneous transmission in the EGSM900 and GSM1800 band is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

The RF-part is dimensioned for triple band operation (EGSM900, DCS1800, PCS19000).

The RF-circuit consists of the following components:

- Hitachi Bright 6E chip set (HD155165BP) with the following functionality:
  - PLL for local oscillator LO1 and LO2 and TxVCO
  - Integrated local oscillators LO1, LO2
  - Integrated TxVCO
  - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
  - 26 MHz reference oscillator
- RF 3166 Transmitter power amplifier with integrated power control circuitry
- GSM Quad Band Antenna Switch Module with Dual low-pass filters CXG1180EQ
- Quartz and passive circuitry of the 26MHz VCXO reference oscillator

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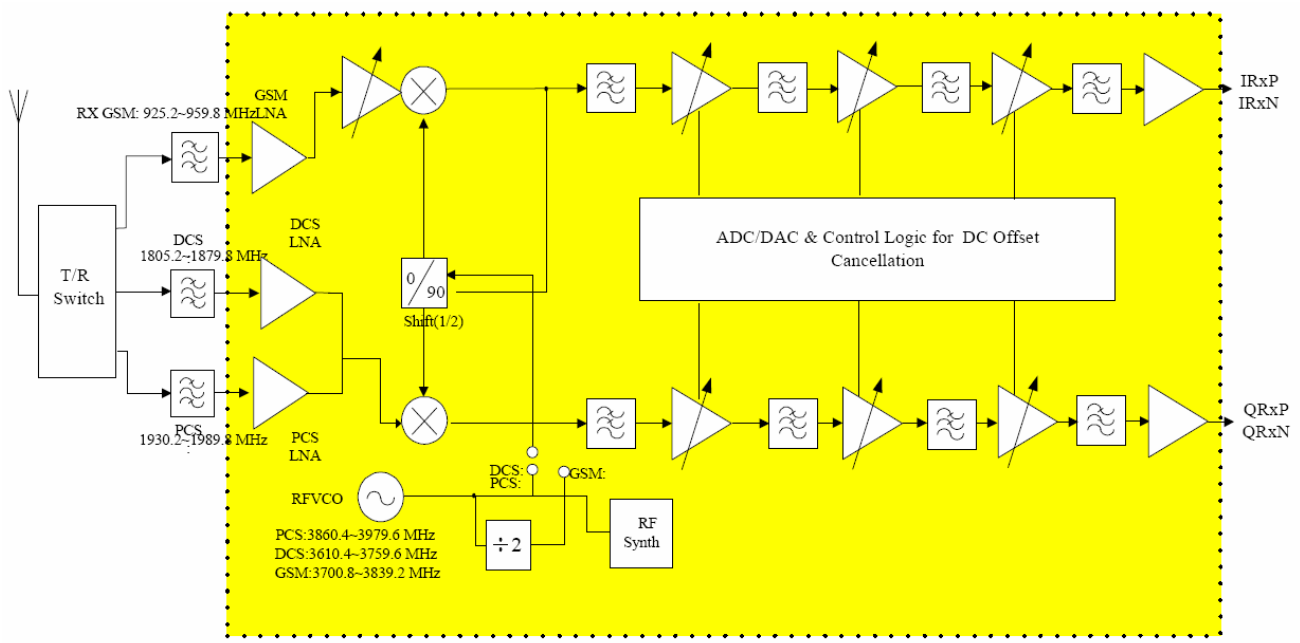
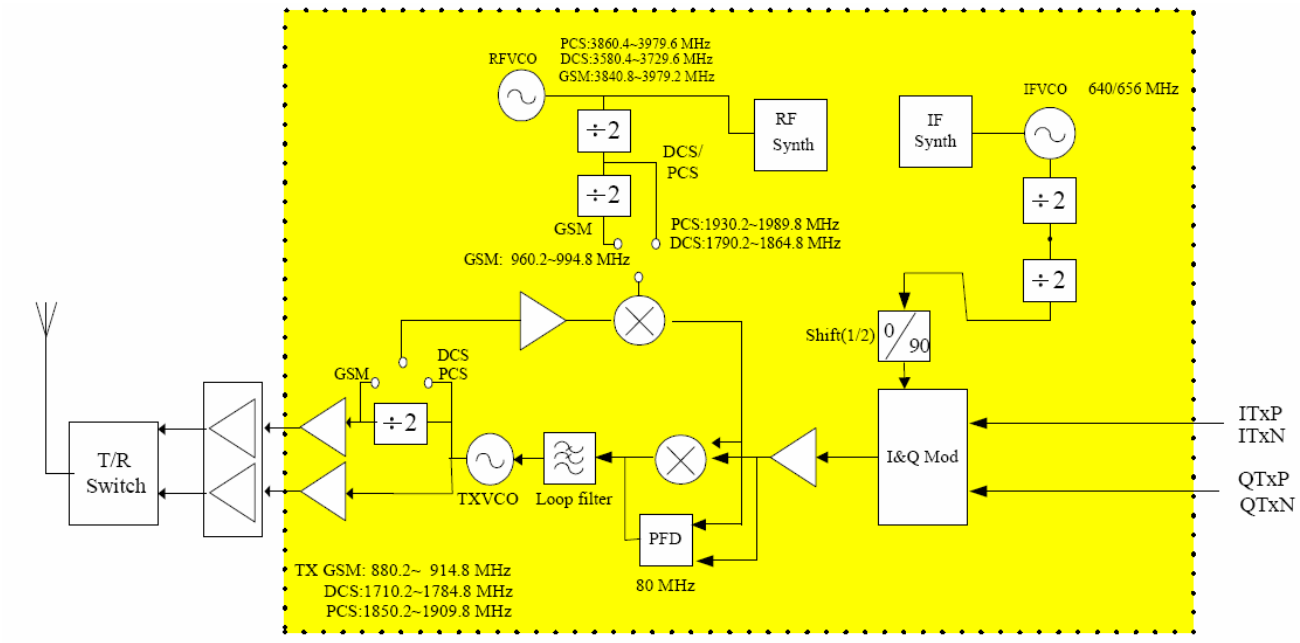
6.1 Block diagrams RF part

RX Part:



TX Part:



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6.2 BRIGHT VI E chipset (HD 155165BP)

6.2.1 First Local Oscillator

The first local oscillator (LO1) consists of a PLL and VCO inside Bright VI E and an internal loop filter

6.2.2 RF-PLL

The frequency-step is 400 kHz in DCS1800/PCS1900 mode and 800kHz in GSM850/EGSM900 mode due to the internal divider by two for DCS1800/PCS1900 and divider by four for GSM850/EGSM900. To achieve the required settling-time in GPRS operation, the PLL can operate in fast-lock mode a certain period after programming to ensure a fast settling. After this the loop filter and current are switched into normal mode to get the necessary phase noise performance. The PLL is controlled via the tree-wire-bus (SDI G2.H11, SCLK G2.J14 and SEN G2.J12) of Bright VI E.

6.2.3 RF VCO (LO1)

The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. The full oscillation range is divided into 256 sub-bands. To do so, a control voltage for the LO1 is used, gained by a comparator. This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the G2, according to the network channel requirements.

6.2.4 Second local oscillator (640~656MHz)

The second local oscillator (LO2) consists of a PLL and VCO inside Bright (IC201) and an internal loop filter. Due to the direct conversion receiver architecture, the LO2 is only used for transmit-operation. The LO2 covers a frequency range of at least 16 MHz (640MHz – 656MHz).
Before the LO2-signal gets to the modulator it is divided by 8. So the resulting TX-IF frequencies are 80/82 MHz (dependent on the channel and band). The LO2 PLL and power-up of the VCO is controlled via the tree-wire-bus of Bright (G2 signals SDI G2.H11, SCLK G2.J14 and SEN G2.J12). To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2nd PLL with the 26 MHz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.

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6.2.5 Receiver

The filters are centred to the band frequencies. The symmetrical filter output is matched to the LNA input of the Bright .The Bright 6E incorporates three RF LNAs for GSM850/EGSM900, GSM1800 and GSM1900 operation. The LNA/mixer can be switched in High- and Low-mode to perform an amplification of ~ 20dB. For the “High Gain“ state the mixers are optimised to conversion gain and noise figure, in the “Low Gain“ state the mixers are optimised to large-signal behaviour for operation at a high input level. The Bright performs a direct conversion mixer, which are IQ-demodulators. For the demodulation of the received GSM signals the LO1 is required. The channel depending LO1 frequencies for 1800MHz/1900MHz bands are divided by 2 and by 4 for 850MHG/900MHz band. Furthermore the IC includes a programmable gain baseband amplifier PGA (90 dB range, 2dB steps) with automatic DC-offset calibration. LNA and PGA are controlled via G2 (SDI G2.H11, SCLK G2.J14 and SEN G2.J12). The channel-filtering is realized inside the chip with a three stage baseband filter for both IQ chains. The IQ receive signals are fed into the A/D converters in the IOTA (BIN IOTA.D10, BIP IOTA.D9 BQP IOTA.C10, BQN IOTA.C9).

6.2.6 Transmitter

Transmitter: Modulator and Up-conversion Loop

The generation of the GMSK-modulated signal in Bright is based on the principle of up conversion modulation phase locked loop. The incoming IQ-signals from the baseband are mixed with the divided LO2-signal. The modulator is followed by a lowpass filter (corner frequency ~80 MHz) which is necessary to attenuate RF harmonics generated by the modulator. A similar filter is used in the feedback-path of the down conversion mixer.
With help of an offset PLL the IF-signal becomes the modulated signal at the final transmit frequency. Therefore the GMSK modulated RF-signal at the output of the TX-VCOs is mixed with the divided LO1-signal to a IF-signal and sent to the phase detector. The I/Q modulated signal with a centre frequency of the intermediate frequency is send to the phase detector as well.
The output signal of the phase detector controls the TxVCO and is processed by a loop filter whose component C619 is external to the Bright. The TxVCO which is realized inside the Bright chip generates the GSMK modulated frequency.

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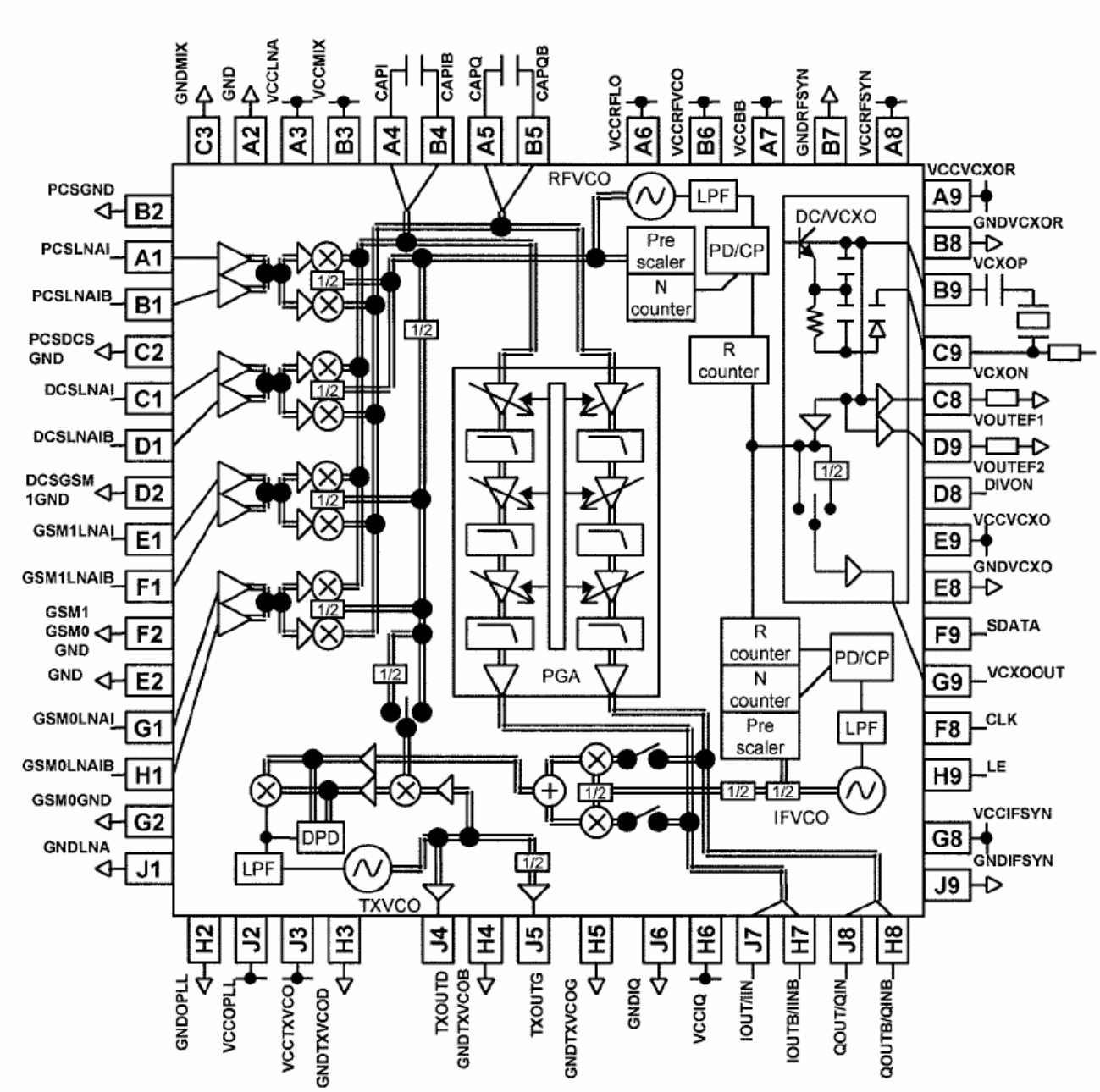
6.2.7 Bright IC Overview



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6.3 Antenna switch (electrical/mechanical)

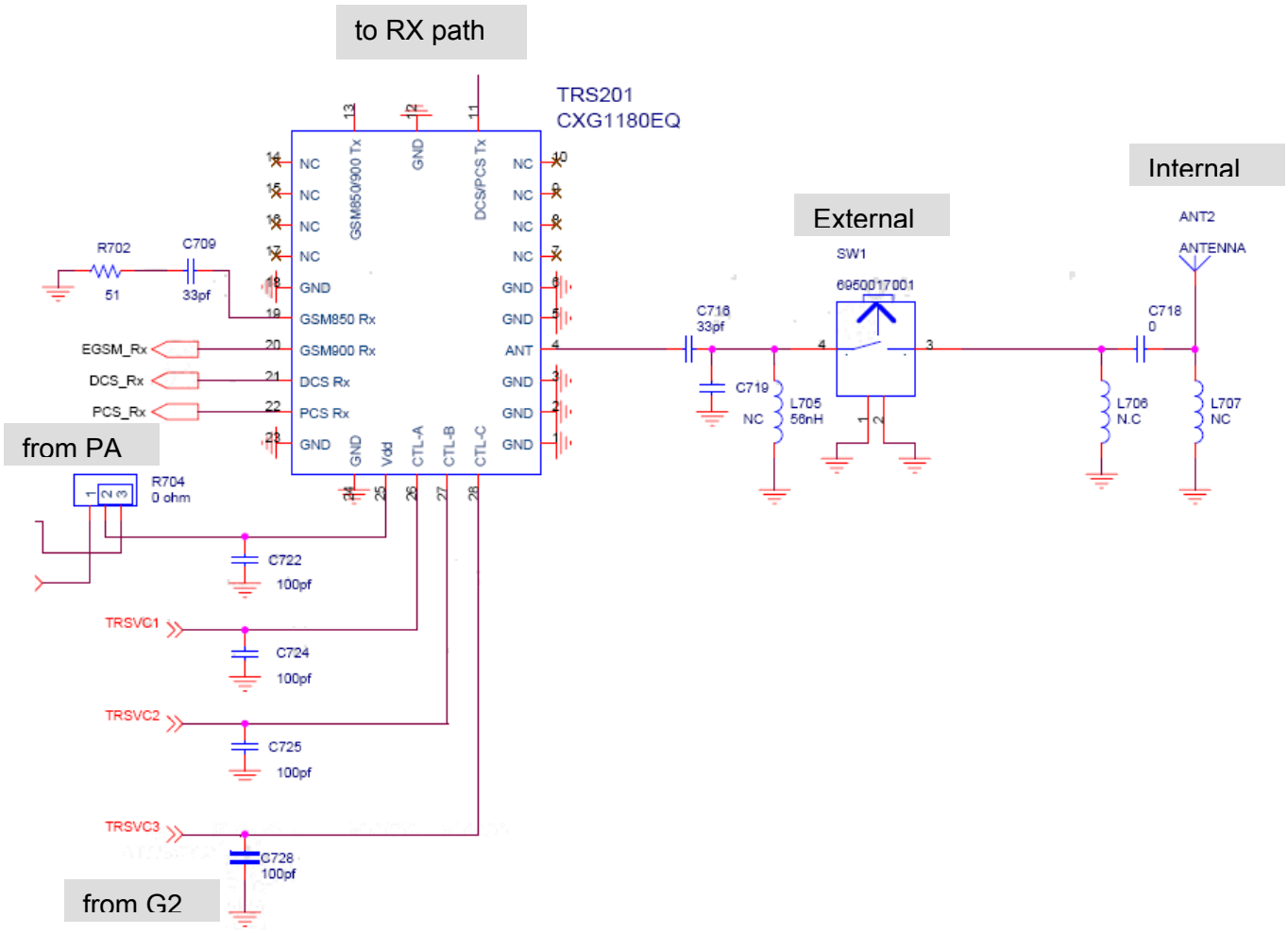
Internal/External <> Receiver/Transmitter

The S88 mobile have two antenna switches.

a) The mechanical antenna switch SW1 for the differentiation between the internal and external antenna.

b) The electrical antenna switch TRS201, for the differentiation between the receiving and transmitting signals.

To activate the correct tx pathes of this diplexer, the G2 signals TRSVC1 G2.M14, TRSVC2 G2.L12 and TRSVC3 G2.L13 are required.



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6.4 RF Micro Devices transmitter power amplifier RF3166

The RF3166 is a quad-band GSM850, EGSM900, DCS1800, and PCS1900 power amplifier module that incorporates an indirect closed loop method of power control. The indirect closed loop is driven directly from the output of the Bright chipset GSMPA IC201.J5 and DCSPA IC201.J4.

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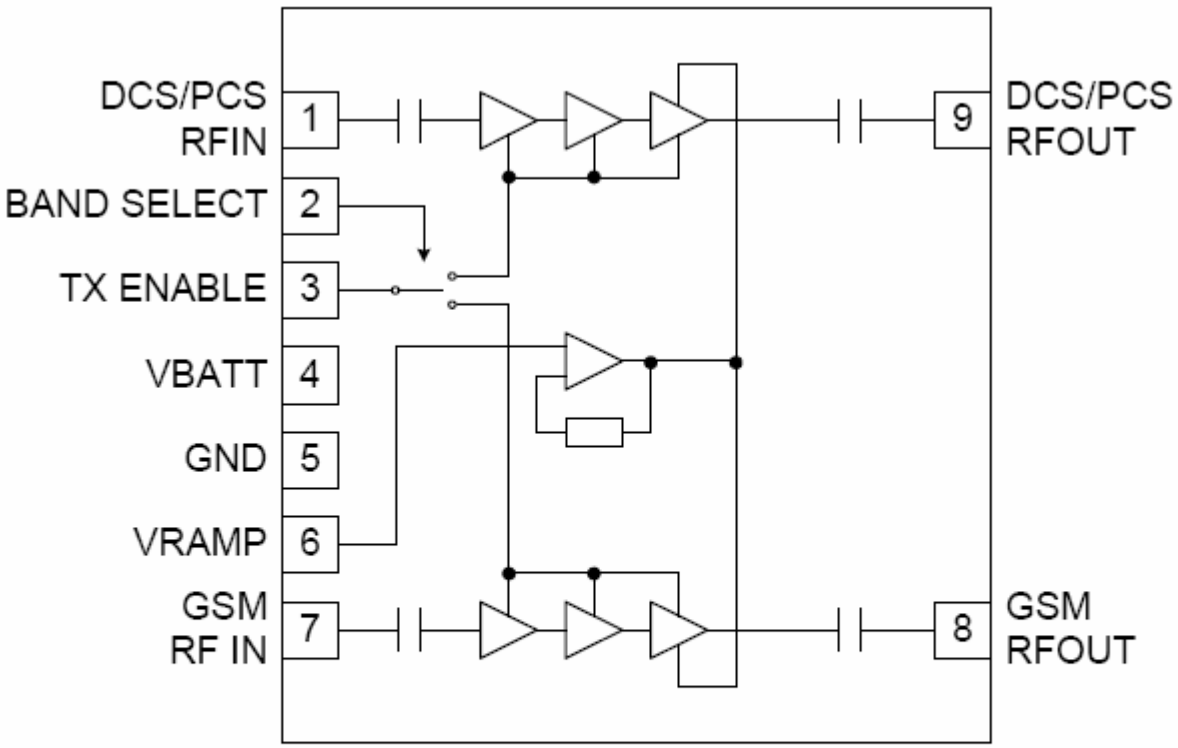

Functional Block Diagram

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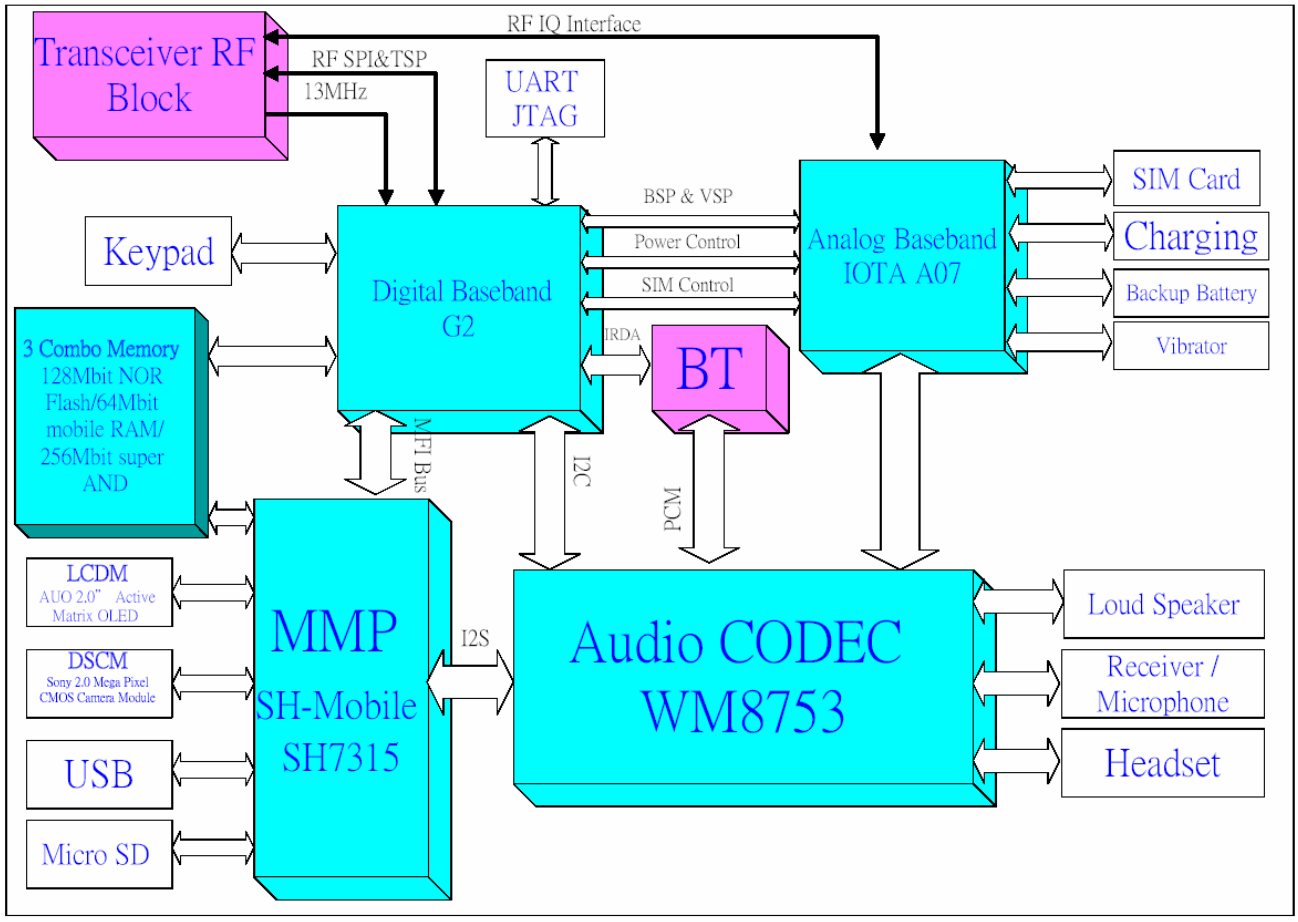
7 Logic / Control Introduction

S88 utilizes TI chipsets (CALYPSO and IOTA) and RENESAS chipset (SHJ2) as base-band solution. Base-band is composed with three parts: Logic, Analog/Codec and MMP. CALYPSO is a GSM/GPRS digital base-band logic solution included microprocessor, DSP, and peripherals. IOTA is a combination of analog/codec solution and power management which contain base-band codec, voice-band codec, several voltage regulators and SIM level shifter etc. SHJ2 is a multimedia solution included microprocessor, DSP, internal memory, and interrupt controller. In addition, S88 integrates with other features such as LED backlight, OLED display, CMOS DSC module, Micro-SD card, vibration, melody and charging etc.

7.1 S88 Logic Block Diagram



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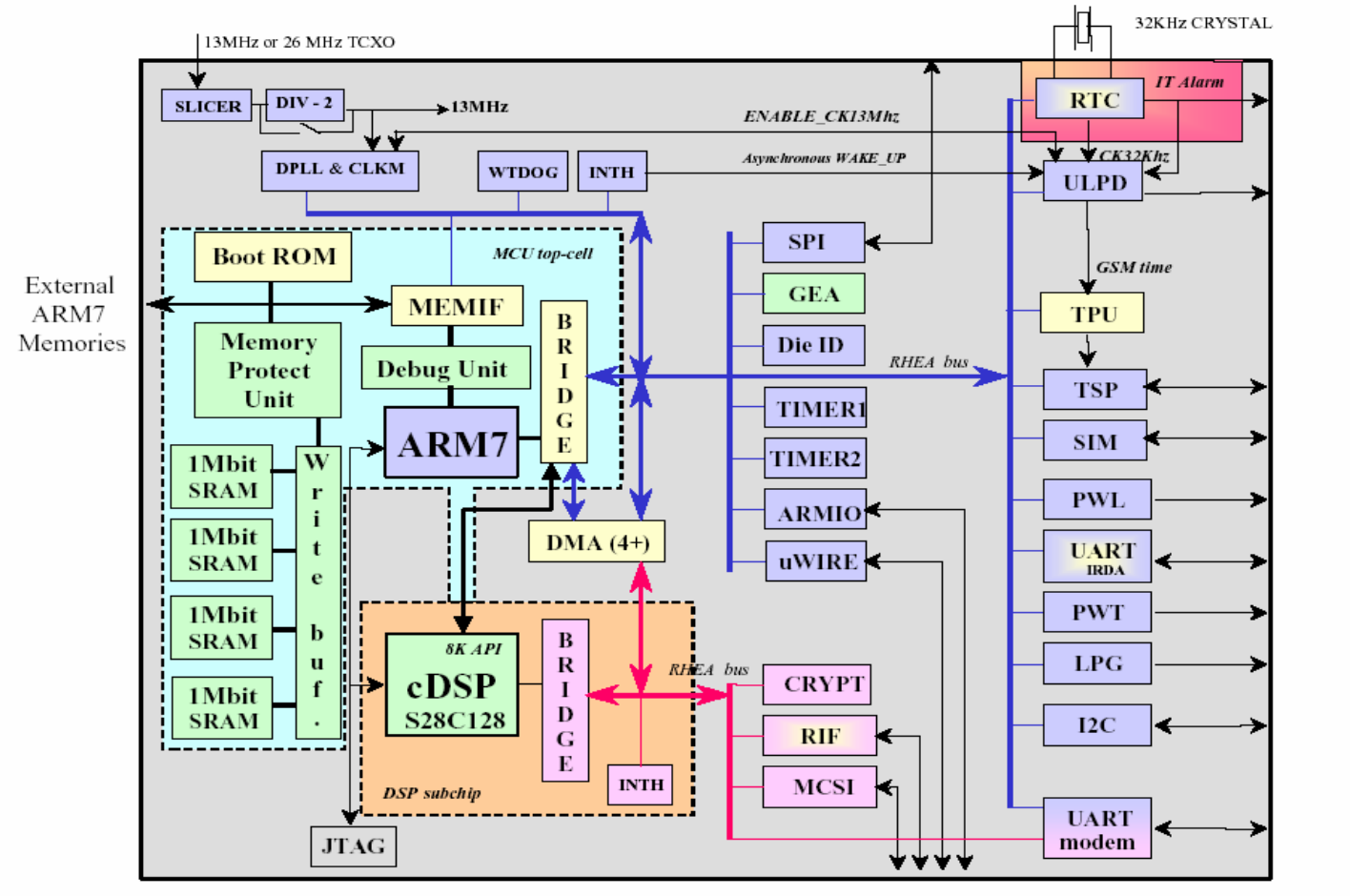
7.2 Calypso - TWL3014

Block diagram



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7.2.1 Operation theory

CALYPSO (HERCROM400) is a chip implementing the digital base-band processor of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE) and an internal 4M-bit RAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.
Major functions of this chip are as follows:

Real Time Clock (RTC)
The RTC block is an embedded RTC module fed with an external 32.768KHz Crystal. Its basic functions are:

- Time information (seconds/minutes/hours)
- Calendar information (Day/Month/Year/ Day of the week) up to year 2099
- Alarm function with interrupts (RTCINT is generated to wake up ABB)
- 32KHz oscillator frequency gauging

Pulse Width Light (PWL)
This module allows the control of the backlight of LCD and keypad by employing a 4096 bit random sequence.

MODEM-UART
This UART interface is compatible with the NS 16C750 device which is devoted to the connection to a MODEM through a standard wired interface. The module integrates two 64 words (9 and 11 bits) receive and transmit FIFOs which trigger levels are programmable. All modem operations are controllable either via a software interface or using hardware flow control signals. In Hyperion B1, we implement software flow control by only two signals: TXD and RXD.

I2C master serial interface (I2C)
The I2C (Philips standard) is a half-duplex serial port using 2 lines (data and clock) for data transmission with software addressable external devices. In Hyperion B1, we employ I2C bus to control CLI in Audio Codec.

The I2C signals are defined as follows:
I2C_SCL: programmed to the fast transmission mode (400KHz)
I2C_SDA: the serial bi-directional data of the Audio Codec controller

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General Purposes I/O (GPIO)

Calypso provides 16 GPIOs configurable in read or write mode by internal registers. In Hyperion B1, we utilize all of them as follows:

IO0: Let MMP power-on reset; 'Low active'
IO1: Enable OLED Power; 'H' enable, 'L' disable
IO2: Control MMP's MFI mode; 'H'68-type mode, 'L'80-type mode
IO3: Camera/Video Mode switch select; 'H' Camera mode, 'L' Video mode
IO4: MMP's MFI INT request; 'Low active'
IO5: SIM power control
IO6: MMP PMIC mode switch; 'H' normal mode, 'L' standby mode
IO7: Reset of external device: For Hyperion B1, Reset for 3 combo memory and OLED
IO8: Indicates whether MMP is in software standby mode
IO9: OLED brightness control; 'H' Brighter, 'L' Dimmer
IO10: Detection of T-Flash card; 'H' No plugged in, 'L' plugged in
IO11: OLED brightness control
IO12: OLED brightness control
IO13: INT request for MMP
IO14: SRAM high-byte enable
IO15: SRAM low-byte enable

Serial Port Interface (SPI)

The SPI is a full-duplex serial port configurable from 1 to 32 bits and provides 3 enable signals programmable either as positive or negative edge or level sensitive. This interface is working on 13MHz and is used for the GSM/GPRS baseband and voice A/D, D/A with IOTA

Memory Interface and internal Static RAM

For external memory device (Flash and SRAM), this interface performs read and write access with adaptation to the memory width. It also provides 6 chip-select signals corresponding each to an address range of 8 mega bytes. One of these chip-select is dedicated to the selection of an internal memory. In Hyperion B1, we employ nCS0/nCS1 (nCS0_NROM/nCS1_NROM) for external Flash and nCS2 (nCS2_NSRAM) for external SRAM. A 4Mbit SRAM is embedded on the die and memory mapped on the chip-select nCS6 of the memory interface.

SIM Interface

The Subscriber Identity Module interface will be fully compliant with the GSM 11.11 and ISO/IEC 7816-3 standards. Its external interface is 3 Volts only. 5 Volts adaptation will be based on external level shifters.

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Time Serial Port (TSP)

The TPU is a real-time sequencer dedicated to the monitoring of GSM/GPRS baseband processing. The TSP is a peripheral of the TPU which includes both a serial port (32 bits) and a parallel interface. The serial port can be programmed by the TPU with a time accuracy of the quarter of GSM bit. The serial port is uni-directional (transmit only) when used with IOTA. The serial port provides 4 enable signals programmable either as positive or negative edge or level sensitive. This serial port is derived from 6.5MHz and used to control the real time GSM windows for the baseband codec and the windows for ADC conversion.

TSP Parallel interface (ACT)

The parallel interface allows control 13 external individual outputs and 1 internal signal with a time accuracy of the quarter of GSM bit. These parallel signals are mainly used to control the RF activity. In Hyperion B1, we employ 8 of them to control RF activity.

TSPACT0:	TR switch power
TSPACT1:	TR switch control_A
TSPACT2:	TR switch control_B
TSPACT3:	TR switch control_C
TSPACT5:	Band selection
TSPACT6:	PA enable
TSPACT8:	Crystal enable
TSPACT10:	Three wires latch enable

Radio Interface (RIF)

The RIF (Radio Interface) Module is a buffered serial port derived from the BSP peripheral module of the defined for TMS320C5X. The external serial data transmission is supported by a full-duplex double-buffered serial port interface. The interface is used for transfer of baseband transmit and receive data and also to access all internal programmation registers of the device.

Miscellaneous:

Some important Baseband /RF interface signals are defined as follows:

- CLKTCXO: 13MHz VTCXO Clock from RF circuit
- TCXOEN: 13MHz VTCXO Clock Enable signal

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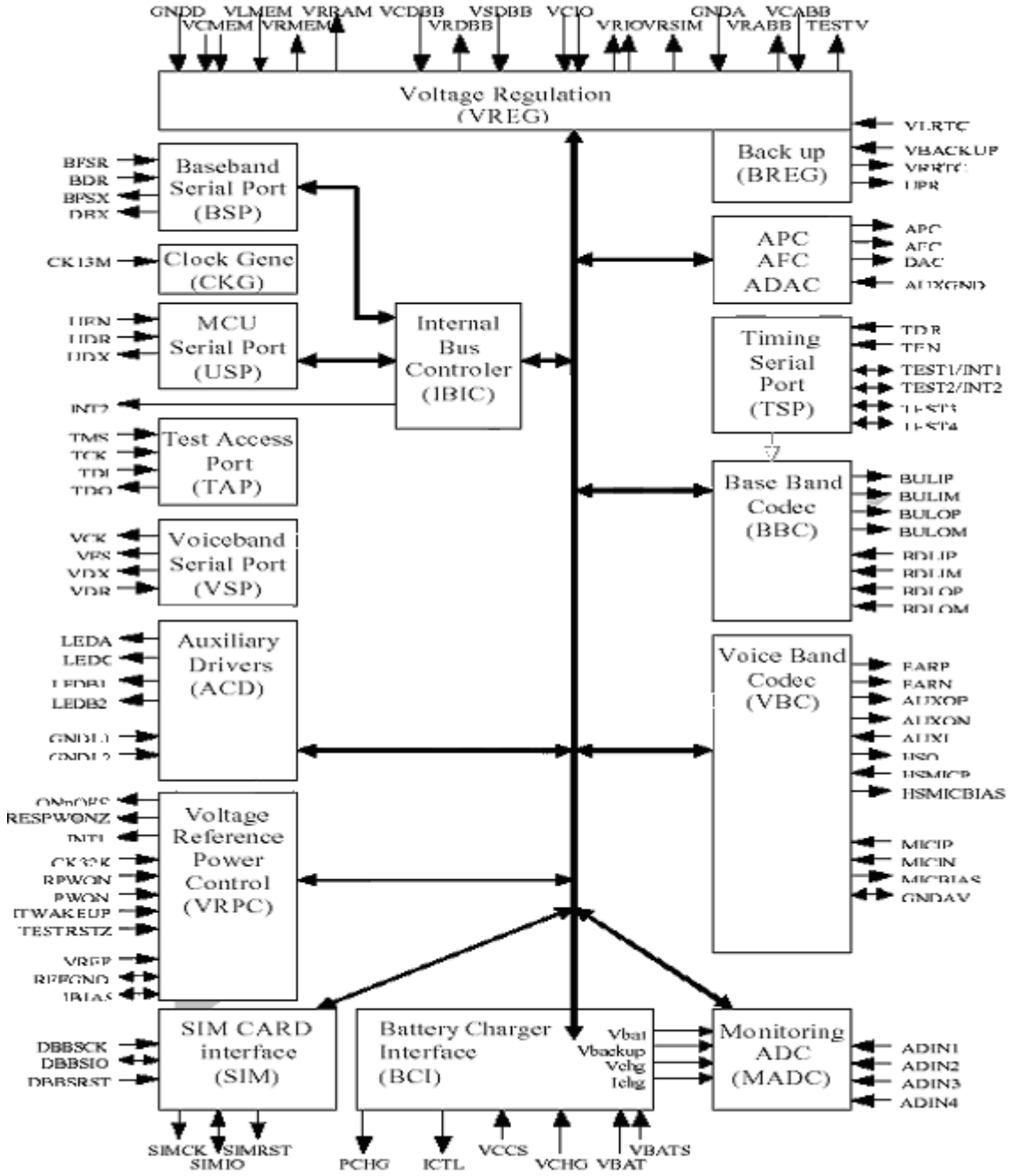
7.3 IOTA – TWL3025

Block diagram



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7.3.1 Operation theory

Together with a digital base-band device (Calypso), IOTA is part of a TI DSP solution intended for digital cellular telephone applications including GSM 900, DCS 1800 and PCS 1900 standards (dual band capability). It includes a complete set of base-band functions to perform the interface and processing of voice signals, base-band in-phase (I) and quadrature (Q) signals which support single-slot and multi-slot mode, associated auxiliary RF control features, supply voltage regulation, battery charging control and switch ON/OFF system analysis. IOTA interfaces with the digital base-band device through a set of digital interfaces dedicated to the main functions of CALYPSO, a base-band serial port (BSP) and a voice-band serial port (VSP) to communicate with the DSP core (LEAD), a micro-controller serial port to communicate with the micro-controller core and a time serial port (TSP) to communicate with the time processing unit (TPU) for real time control. IOTA includes also on chip voltage reference, under voltage detection and power-on reset circuits.
Major functions of this chip are as follows:

Baseband Codec (BBC)

The baseband codec includes a two-channel uplink path and a two-channel downlink path. The baseband uplink path (BUL) modulates the bursts of data coming from the DSP via the baseband serial port (BSP) and to be transmitted at the antenna. Modulation is performed by a GMSK modulator. The GMSK modulator implemented in digital technique generates In-phase (I) and Quadrature (Q) components, which are converted into analog base-band by two 10 bits DACs filters. It also includes secondary functions such as DC offset calibration and I/Q gain unbalance. The baseband downlink path converts the baseband analog I & Q components coming from the RF receiver into digital samples and filters these resulting signals through a digital FIR to isolate the desired data from the adjacent channels. During reception of burst I & Q digital data are sent to the DSP via the baseband serial port at a rate of 270 KHz.

Automatic Frequency control (AFC)

The automatic frequency control function consists of a digital to analog converter optimized for high resolution DC conversion. Its purpose is to control the frequency of the GSM 13MHz oscillator to maintain mobile synchronization on the base station and allow proper transmission and demodulation.

Automatic Power Control (APC)

Purpose of the Automatic Power Control (APC) is to generate an envelope signal to control the power ramping up, ramping down and power level of the radio burst. The APC structure is intended to support single slot and multi-slots transmission with smooth power transition when consecutive bursts are transmitted at different power level. It includes a DAC and a RAM in which the shape of the edges (ramp-up and ramp-down) of the envelope signals are stored digitally. This envelope signal is converted to analog by a 10 bits digital to analog converter. Timing of the APC is generated internally and depends of the real time signals coming from the TSP and the content of two registers which control the relative position of the envelope signal versus the modulated I & Q.

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Time serial port (TSP)

Purpose of the time serial port is to control in real time the radio activation windows of IOTA which are BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration and BDL receive and the ADC conversion start.

These real time control signals are processed by the TPU of DBB and transmitted serially to ABB via the TSP, which consists in a very simple two pins serial port. One pin is an enable (TEN) the other one the data receive (TDR). The master clock CK13M divided by 2 (6.5MHz) is used as clock for this serial port.

Voice band Codec (VBC)

The VBC processes analog audio components in the uplink path and transmits this signal to DSP speech coder through the voice serial port (VSP). In the downlink path the VBC converts the digital samples of speech data received from the DSP via the voice serial port into analog audio signal. Additional functions such as programmable gain, volume control and side-tone are performed into the voice band codec.

Micro-controller serial port (USP)

The micro-controller serial port is a standard synchronous serial port. It consists in three terminals, data transmit (UDX), data receive (UDR) and port enable (UEN). The clock signal is 13MHz clock. The USP receives and sends data in serial mode from and to the external micro-controller and in parallel mode from and to the internal GSM Baseband a Voice A/D D/A modules. The micro-controller serial port allow read and write access of all internal registers under the arbitration of the internal bus controller.

SIM card shifters (SIMS)

The SIM card digital interface in ABB insures the translation of logic levels between DBB and SIM card, for transmission of 3 different signals; a clock derived from a clock elaborated in DBB, to the SIM card (DBBSCK➔SIMCLK). a reset signal from DBB to the SIM card (DBBSRST➔SIMRST), and serial data from DBB to SIM card (DBBSIO➔SIMIO) and vice-vera. he SIM card interface can be programmed to drive a 1.8V and 3 V SIM card

Voltage Regulation (VREG)

Linear regulation is performed by several low dropout (LDO) regulators to supply analog and digital baseband circuits.

(1) LDO VRDBB generates the supply voltage (1.8V, 1.5V,and 1.2V) for the digital core of DBB. In Hyperion B1, it is programmed to 1.5V. This regulator takes power from the battery voltage.
(2) LDO VRABB generates the supply voltage 2.8V for the analog function of ABB. It is supplied by the battery.
(3) LDO VRIO generates the supply voltage 2.8V for the digital core of ABB and digital I/O's of DBB and ABB. It is supplied from battery voltage.

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(4) LDO VRMEM generates the supply voltages 2.8V for DBB memory interfaces I/O's.
(5) LDO VRRAM generates the supply voltages 2.8V for DBB memory interfaces I/O's.
(6) LDO VRRTC generates the supply voltages (1.8,1.5, or 1.2V) and supply voltage 1.5V for the following block of DBB (real time clock and 32K oscillator). It's supplied by UPR.
(7) LDO VRSIM generates the supply voltages (1.8V, 2.9V) for SIM card interface I/O's.

Baseband Serial Port (BSP)

The BSP serial interface is used for both configuration of the GSM baseband and voice A/D D/A (read and write operation in the internal registers), and transmission of the radio data to the DSP during reception of a burst by the downlink part of the GSM baseband & voice A/D D/A. Four pins are used by the serial port: BFSR and BDR for receive, BFSX and BDX for transmit. BDX is the transmitted serial data output. BFSX is the transmit frame synchronization and is used to initiate the transfer of the transmit data. BDR is the received serial input. BFSR is the receive frame synchronization and is used to initiate the reception data.

Battery charger Interface (BCI)

The main function of the ABB charger interface is the charging control of either a 1-cell Li-ion Battery or 3-serie Ni-MH cell batteries with the support of the micro-controller. The battery monitoring uses the 10 bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage. The magnitude of the charging current is set by the 10 bits of a programming register converted by an 10 bit Digital to Analog Converter, whose output sets the reference input of the charging current control loop. The battery charger interface performs also some auxiliary functions. They are battery pre-charge, battery trickle charge and back-up battery charge if it is rechargeable.

Monitoring ADC (MADC)

The MADC consists in a 10-bit analog to digital converter combined with a nine inputs analog multiplexer. Out of the nine inputs five are available externally, the four remaining being dedicated to main battery voltage, back up battery voltage, charger voltage and charger current monitoring. On the five available externally three are standard inputs intended for battery temperature, battery type measurements.

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Reference Voltage / Power on Control (VRPC)

An integrated band-gap generates a reference voltage. This reference is available on an external pin for external filtering purpose only. This filtered reference is internally used for analog functions. The external resistor connected between pin IBIAS and GNDREF sets, from the band-gap voltage, the value of the bias currents of the analog functions. The VRPC block is in charge to control the Power ON, Power OFF, Switch On, and Switch OFF sequences. Even in Switch OFF state some blocks functions are performed. These “permanent” functions are functions, which insure the wake-up of the mobile such as ON/OFF button detection or charger detection. Interrupts are generated at power-down detection of the PWON button and when abnormal voltage conditions are detected.

Internal bus and interrupt controller (IBIC)

Read and write access to all internal registers being possible via both the BSP and USP, purpose of the internal bus controller is to arbitrate the access on the internal bus and to direct the read data to the proper serial port. During reception of a burst the internal bus controller assign the transmit part of the BSP to the base-band downlink to transfer the I & Q samples to the DSP.
This block also handles the internal interrupts generated by the MADC, BCI and VRPC blocks and generates the micro-controller interrupt signal INT2.

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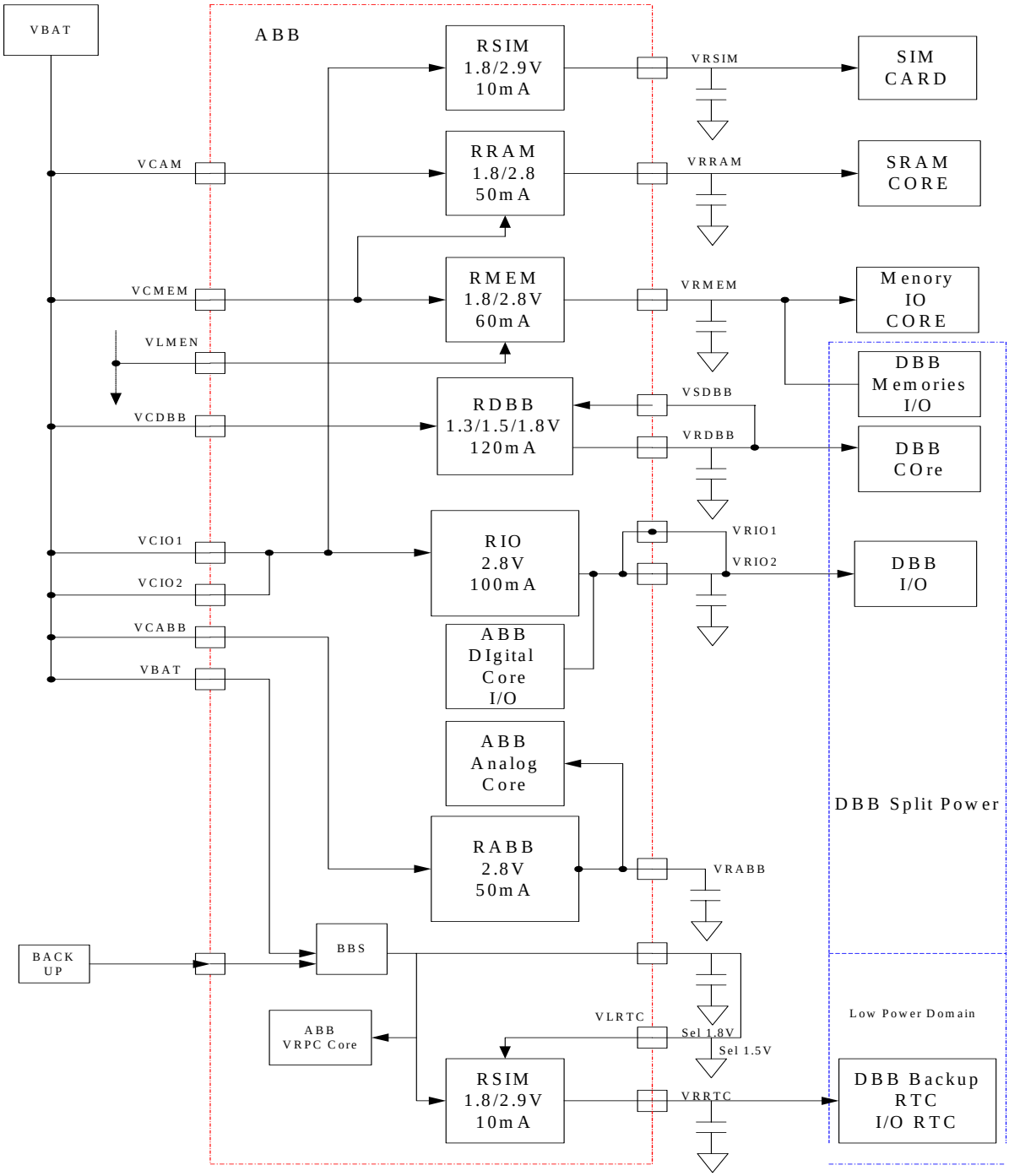
7.3.2 Power Supply diagram



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Description:
The voltage regulators embedded in IOTA consists of seven sub blocks. Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators supply power to internal analog and digital circuit, to DBB processor, and to external memory.

- LDO (VRDBB IOTA.J1) is a programmable regulator that generates the supply voltages (1.8V,1.5V and 1.3V) for the core of the DBB processor. The main battery supplies VRDBB.
- LDO (VRIO IOTA.B1.B2) generate the supply voltage (2.8V) for the digital core and I/O of the TWL3025 device. The main battery supplies VRIO.
- LDO (VRMEM IOTA.G1) is a programmable regulator that generates the supply voltages (2.8V and 1.8V) for external memories (typically flash memories) and DBB memory interface I/O. The main battery supplies VRMEM.
- LDO (VRRAM IOTA.F1) is a programmable regulator that generate the supply voltages(2.8V and 1.8V) the external memory (typically SRAM memories) and DBB memory interface I/Os. The main battery supplies VRRAM.
- LDO (VRABB IOTA.H10) generates the supply voltage (2.8V) for the analog functions of the TWL 3014 devices. The main battery supplies VRABB.
- LDO (VRSIM IOTA.B1) is a programmable regulator that generates the supply voltages (2.9V and 1.8V) SIM card and SIM card devices. The main battery supplies VRSIM.
- LDO (VRRTC IOTA.D1) is a programmable regulator that generates the supply voltage (1.8V.1.5Vand 1.3V) for real time clock and the 32-KHZ oscillator located in the DBB device during all modes. The main or backup battery supplies VRTC.

7.3.3 System power on/off Sequence

Power on mode
On the plug-in of the valid main battery or backup battery, an internal reset is generated (POR). After a power-on sequence, the IOTA device is in the BACKUP or OFF state. When these conditions occur in the power on state, the hardware power on sequence starts:

1. Enable band-gap (VREF and IREF)
2. Check if Main Battery voltage is greater than 3.2V
3. Enable charge VRDBB-VRABB-VRMEM-VRRAM
4. Regulator OK.
5. ON_nOFF=1, ABB RESETz=1
6. NRESET IOTA.D3 pin is set from ‘L’ to ‘H’
7. 13MHz clock oscillator is enabled

Power off mode
This state is reached when there is not enough voltage in the main battery and backup battery or when both batteries are disconnected.

1. Send INT1 IOTA.H6
2. Start 5*T watchdog Timer , T= 32K period
3. ON_nOFF=0
4. ABB RESETz=0
5. Disable the LDO’s using MSKOFF content and the band-gap
6. “MBATLOW”=0

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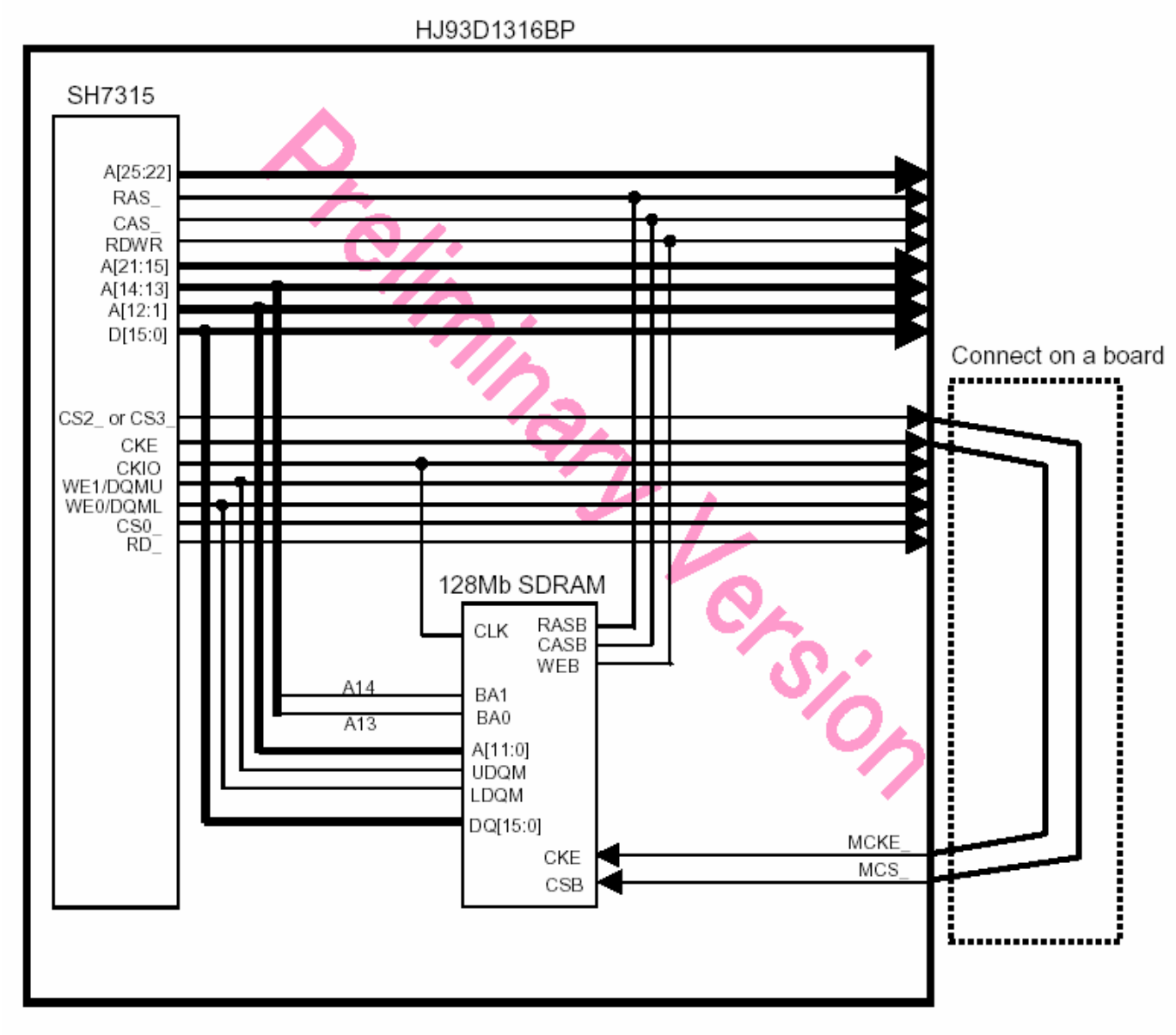
7.4 Application Processor SHJ2 + SD128

HJ93D1316BP is a SiP (System in Package) which integrates an application processor for mobile phone called SH-Mobile J2 (SH7315), and 128-Mbit SDRAM.



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7.4.1 Multimedia Processor SH7315

SH7315 is a single-chip RISC microprocessor that integrates an extended 32-bit RISC-type SuperH architecture CPU with a digital signal processing (DSP) extension as its core, together with a large-capacity 32-kbyte cache memory, a 16-kbyte X/Y memory, a 32-kbyte U memory, and an interrupt controller.
High-speed data transfers can be performed by an on-chip direct memory access controller (DMAC), and an external memory access support function enables direct connection to different kinds of memory. SH7315 also includes powerful peripheral functions that are essential to system configuration, such as a serial interface which has a large FIFO.
Moreover, SH7315 realizes various functions which are needed for the next generation of mobile phone applications, such as an easy-to-use camera interface, sound input/output, MPEG4 encoding/decoding accelerator, and USB function module. A powerful built-in power-management function keeps power consumption low, even during high-speed operation. SH7315 is ideal for use in electronic devices such as those for applications that require both high-speed operation and low power consumption simultaneously.
Major features of this chip are as follows:

CPU

- Renesas Technology Original SuperH architecture
- Upper compatibility with SH-1, SH-2, and SH3-DSP at object code level
- 32-bit internal data bus
- General-register file
  - -Sixteen 32-bit general registers (eight 32-bit bank registers)
  - -Five 32-bit control registers
  - -Four 32-bit system registers
- RISC type instruction set
  - -Instruction length: 16-bit fixed length for improved code efficiency
  - -Load/store architecture
  - -Delayed branch instruction
  - -Instruction set based on C language
- Instruction execution time: One instruction/cycle for basic instructions
- Logical address space: 4 Gbytes
- Space identifier ASID: 8 bits, 256 logical address spaces
- Five-stage pipeline

DSP

- Mixture of 16-bit and 32-bit instructions
- 32-/40-bit internal data bus
- Multiplier, ALU, barrel shifter, and register file
- 16-bit × 16-bit → 32-bit one cycle multiplier
- Large-capacity DSP data register file
- Six 32-bit data registers
- Two 40-bit data registers
- Extended Harvard architecture for DSP data buses

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• Two data buses
• One instruction bus
• Up to four parallel operations: ALU, multiply, two loads, and store
• Two address units to generating addresses for two memory access
• DSP data addressing modes: Increment, index register addition (with or without modulo addressing)
• Zero-overhead repeat loop control
• Conditional execution instructions
• User DSP mode and privileged DSP mode

Memory management unit (MMU)

• 4-Gbyte address space, 256 address spaces (8-bit ASID)
• Page unit sharing
• Supports multiple page sizes: 1 kbyte or 4 kbytes
• 128-entry, 4-way set associative TLB
• Specifies replacement way by software and supports random replacement algorithm
• Address assignment allows direct access to TLB contents

Interrupt controller (INTC)

• Seven external interrupt pins (NMI, IRQ5 to IRQ0)
• NMI: Fall/rise selectable
• IRQ: Fall/rise/high level/low level selectable
• On-chip peripheral interrupt: Sets priority for each module

Bus state controller

• Physical address space is provided to support areas of up to 64 Mbytes and 32 Mbytes.
• Each area allows independent setting of the following functions:
• Bus size (8 or 16 bits). An access wait cycle count with a different size to be supported is provided for
each area (some area is allowed to set an independent wait for read/write operation).
• Sets of idle wait cycle (for the same or different area)
• Supports SRAM, page mode ROM, SDRAM, and pseudo SRAM (ready for page mode) by specifying memory to be connected to each area.
• Outputs chip select signals to corresponding areas, such as CS0, CS2 to CS4, CS5A/CS5B, and CS6A/CS6B

Direct memory access controller (DMAC)

• Number of channels: Six channels
• Address space: 4 Gbytes on architecture
• Data transfer length: Bytes, words (2 bytes), longwords (4 bytes), 16 bytes (longword×4)
• Maximum number of transfer times: 16,777,216 times
• Address mode: Dual address mode
• Transfer request: Selectable from on-chip peripheral module request, and auto request

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• Bus mode: Selectable from cycle steal mode (normal mode and intermittent mode) and burst mode
• Priority: Selectable from channel priority fixed mode and round robin mode
• Interrupt request: Supports interrupt request to CPU at the end of data transfer

Serial IO with FIFO (SIOF)

• Internal 64-byte transmit/receive FIFO
• Supports 8-/16-/16-bit stereo sound input/output
• Sampling rate clock input selectable from Pφ and external pin
• Internal prescaler for Pφ
• SPI mode
• Provides continuous full-duplex communication with SPI slave device in fixed master mode.
• Transmit/receive data length of fixed 8 bits
• With interrupt request and DMAC request

Clock pulse generator (CPG)

• Clock mode: Input clock selectable from external clock (EXTAL) and crystal oscillator
• Output clock: Bus clock (CKIO)
• Generates three types of clocks
• CPU clock(Iφ): Maximum 120 MHz
• Bus clock(Bφ): Maximum 60 MHz
• Peripheral clock(Pφ): Maximum 33 MHz
• Supports power-down mode
• Software standby mode
• Module standby mode
• U-standby mode (allows the power to be turned off from outside (by enabling the notification signal output for restoring) except RCLK operation area in order to reduce areas with current flowing as well as entire standby current.)
• Asserting CA pin places LSI in U-standby mode
• U-standby mode is cancelled when:
    (1) Compare match is output by CMT.
    (2) Key input is detected
    (3) NMI is asserted
• In the above cases, a STBYEND signal is output externally to notify a cancellation request. When an RWDT overflow is detected, an MFIINT signal is output to notify externally.
• U-standby mode is recovered only at a power-on reset (power to CPU may be turned off)

Serial communication with FIFO

• Internal two channels
• Internal 64-byte transmit/receive FIFO
• High-speed UART for Bluetooth
• Supports CTS/RTS (only on channel 0)
• Internal prescaler for Pφ
• With interrupt request and DMAC request

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Sound interface unit (SIU)
- 16-bit stereo/mono selectable
- Supports PCM and I2S formats
- IEC60958 (SPDIF) supports stereo consumer mode
- One system for sound output and one system for sound input
- Sampling rate conversion (such as 32k or 48k into 44.1 kHz)
- FIR low-pass filter processing function at sound I/O time (7, 15, 31, 63 TAP FIR filters)
- Serial I/O can be directly connected to external A/D or D/A converter.
- Supports slave mode
- With interrupt request and DMAC transfer request

I2C
- Supports single master transmission/reception

Multifunction interface (MFI)
- Interface providing high-speed data transfer to/from external devices that cannot share any system buses Data can be read/written in 32 bits to on-chip RAM (MFRAM: 4 kbytes)
- 8-/16-bit switchable parallel interface
- 68/80 interface switchable at a reset
- MFRAM is accessible from MFI/CPU.
- Data can be transferred between this LSI and external devices using MFRAM and interrupt function as with software. This LSI can be connected to an external device that cannot release bus mastership.
- Internal boot access that considers MFRAM a reset vector
- Providing various through modes
- MFI-related interface signal is automatically sent directly to memory bus during a power-on reset, standby, or U-standby (standby through mode)
- Data and control signals from baseband side can be sent directly to LCD even in active state (active through mode, SRAM I/F R/W supported)
- Issues an interrupt when a restore request is made during U-standby, and providing
- Capable of identifying a restore source generated by KEYSC, RWDT, CMT, or NMI
- Internal semaphore register in MFI that allows read modify write transfer when reading data from baseband side
- Seven internal/external source bits for controlling 128 types of interrupts

SD host interface (SDHI)
- SD memory I/O card interface
- Card detection
- With interrupt request and DMAC request

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Video I/O (VIO)

- 4-Gbyte address space, 256 address spaces (8-bit ASID)
- Page unit sharing
- Supports multiple page sizes: 1 kbyte or 4 kbytes
- 128-entry, 4-way set associative TLB
- Specifies replacement way by software and supports random replacement algorithm
- Address assignment allows direct access to TLB contents

Video processing unit (VPU)

- A module for detecting and compensating MPEG-4 motions as well as accelerating DCT/IDCT operations
- Bus clock operation
- QCIF15fps encoding or decoding by 20-MHz bus clock*
- Maximum image size is CIF
- Performing motion vector detection, motion compensation, DCT operation, and IDCT operation in macro blocks
- Programmable controller controls SIMD arithmetic unit
- 32 processor elements
- Programmable operations
- Supports multiple algorithms
- Simultaneous search of 32 motion vectors
- Hardware dedicated to DCT/IDCT
- Processes one macro block by 350 clocks
- Cache function
- Cache size of ten macro blocks
- Transfers 16 pixels by one clock between cache memory and SIMD arithmetic unit
- With interrupt request and without DMAC request (with bus master function)

Note: * Depends on the performance of MPEG-4 middle software processing unit

USB function module

- Conforms to USB 1.1
- Internal USB transceiver
- Supports ten endpoints as a whole, the number of endpoints is selectable
- Supports control (endpoint 0), bulk-transfer format (to up to four endpoints), interrupt (to up to three endpoints), and isochronous (to up two endpoints)
- The USB standard commands are supported, and class and vender commands are handled by firm ware
- On-chip FIFO buffer for endpoints
- Module input clock: 48 MHz
- With interrupt request and DMAC request

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AND/NAND flash memory controller (FLCTL)
- Direct-connected memory interface with NAND-/AND-type flash memory
- Read/write in sectors
- Two types of transfer modes: Command access mode and sector access mode (512-byte data + 16-byte management code: with ECC)
- With interrupt request and DMAC transfer request

Key scan interface (KEYSC)
- Ready for KEY scanning: Five inputs and six outputs (with anti-chattering function for detecting a KEY input interrupt)
- Generates a KEY input interrupt during standby or U-standby (when inputting RCLK)

User debug interface (H-UDI)
- Supports E10A emulator
- Realtime branch trace
- 1-kbyte on-chip memory for executing high-speed emulation program

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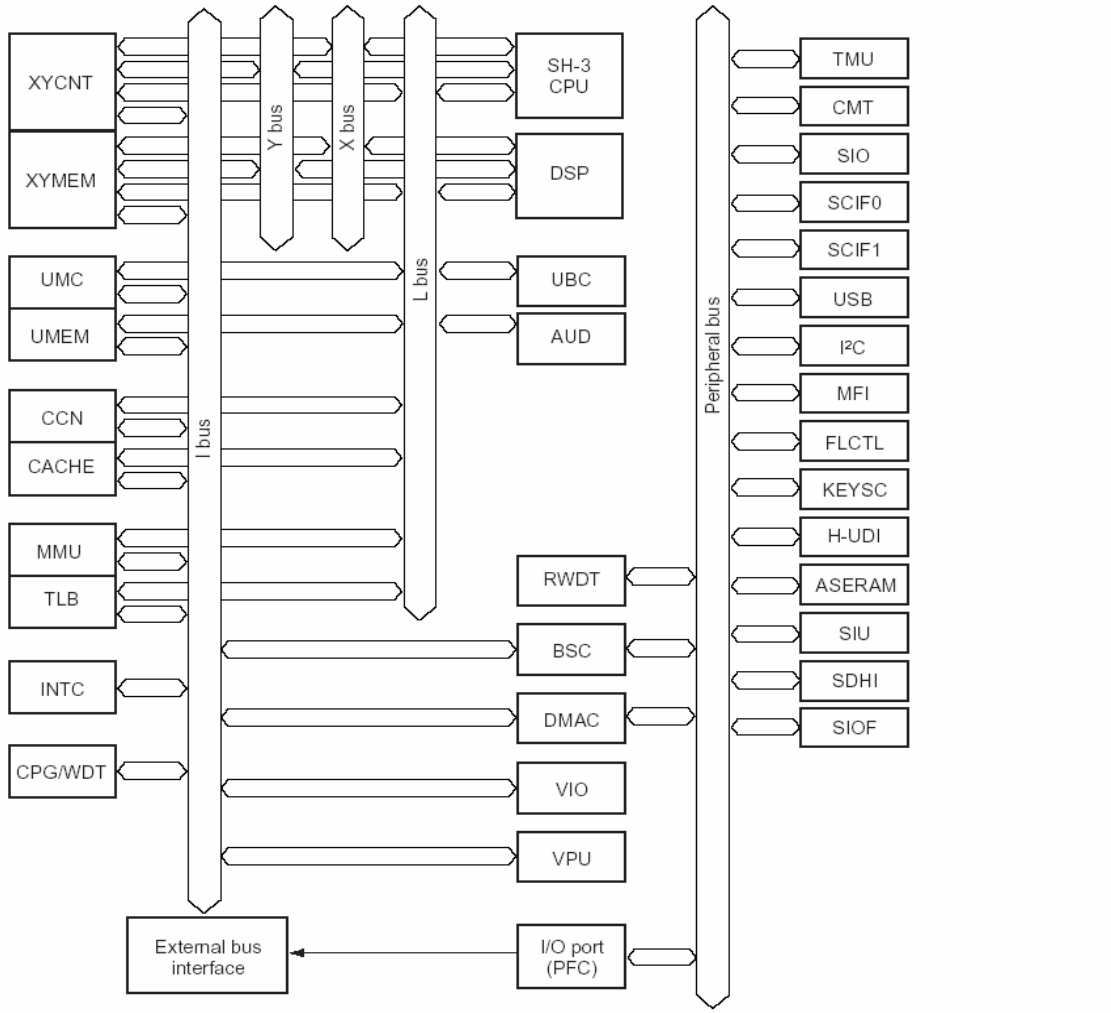
Block diagram:



[Legend]

XYCNT:	X/Y memory controller
XYMEM:	X/Y memory
UMC:	U memory controller
UMEM:	U memory
CACHE:	Cache memory
CCN:	Cache memory controller
MMU:	Memory management unit
TLB:	Translation look-aside buffer
INTC:	Interrupt controller
CPG/WDT:	Clock pulse generator/watchdog timer
CPU:	Central processing unit
DSP:	Digital signal processor
UBC:	User break controller
AUD:	Advanced user debugger
RWDT:	RCLK operation watchdog timer
BSC:	Bus state controller
DMAC:	Direct memory access controller

TMU:	16-bit timer unit
CMT:	Compare match timer
SIO:	Serial I/O
SIOF:	Serial I/O with FIFO
SCIF:	Serial communication interface with FIFO
I²C:	I²C controller
MFI:	Multifunctional interface
VIO:	Video I/O
FLCTL:	AND/NAND flash memory interface
KEYSC:	Key scan interface
H-UDI:	High-performance user debugging interface
ASERAM:	ASE memory
PFC:	Pin function controller
SIU:	Sound interface unit
VPU:	Video processing unit
SDHI:	SD host interface
USB:	Universal serial interface

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7.5 Combo Memory Chip M6MGA157F2LCWG

The M6MGA157F2LCWG consists of 128M-bit NOR type Flash memory, 256M-bit superAND Flash memory and 64Mbit mobileRAM in a 144-ball Stacked CSP(Chip Scale Package) for lead free use.

128M-bit NOR type Flash memory is a high performance non-volatile memory having the advantage of BGO function. 256M-bit superAND Flash memory is a high performance non-volatile memory, which uses AND type multi-level memory cell. The superAND Flash memory doesn't need complicated operations such as sector management for defect sector and error check correction.

64M-bit mobileRAM is a 4,194,304 words high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM. The M6MGA157F2LCWG is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

The 128-Mbit NOR type Flash Memory 3rd Generation is a high-performance 134,217,728-bit CMOS boot block Flash memory device, organized as 8,388,608-word by 16-bit. The device uses a single VCC of 2.7 V to 3.0 V to perform read, erase and program operations. The device supports alternating Background Operation (BGO). By dividing the 128-Mbit memory space into six banks, the device is capable of reading data from one bank while programming, erasing, software command writing, or data loading in one of the other five banks. This feature allows a host system to perform code pre-fetching in one bank while background programming or erasing data in another bank. It is suitable for communication products and cellular phones. The device also provides high-performance eight-word page reads. The device is manufactured using the architecture that enables fast erase operations (0.1 seconds per block).

256M superAND Flash Memory is a CMOS flash memory, which uses cost effective and high performance AND type multi-level memory cell technology. Current AND flash memory requires us to support complicated operations such as sector management for defect sector and error check correction. But this Flash Memory doesn't need such operations. Beside it supports wear leveling function, which is sector replacement function in case of that certain sector, reaches certain erase/write times. And auto read function is available. It enables to read the data without command and address input.

64M-bit mobileRAM is a 4,194,304-word high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM. The cells are automatically refreshed and the refresh control is not required for system. The device also has the partial block refresh scheme and the power down mode by writing the command. The RENESAS mobileRAM is suitable for a high performance cellular phone and a mobile PC requiring small mounting area, light weight and low power dissipation.

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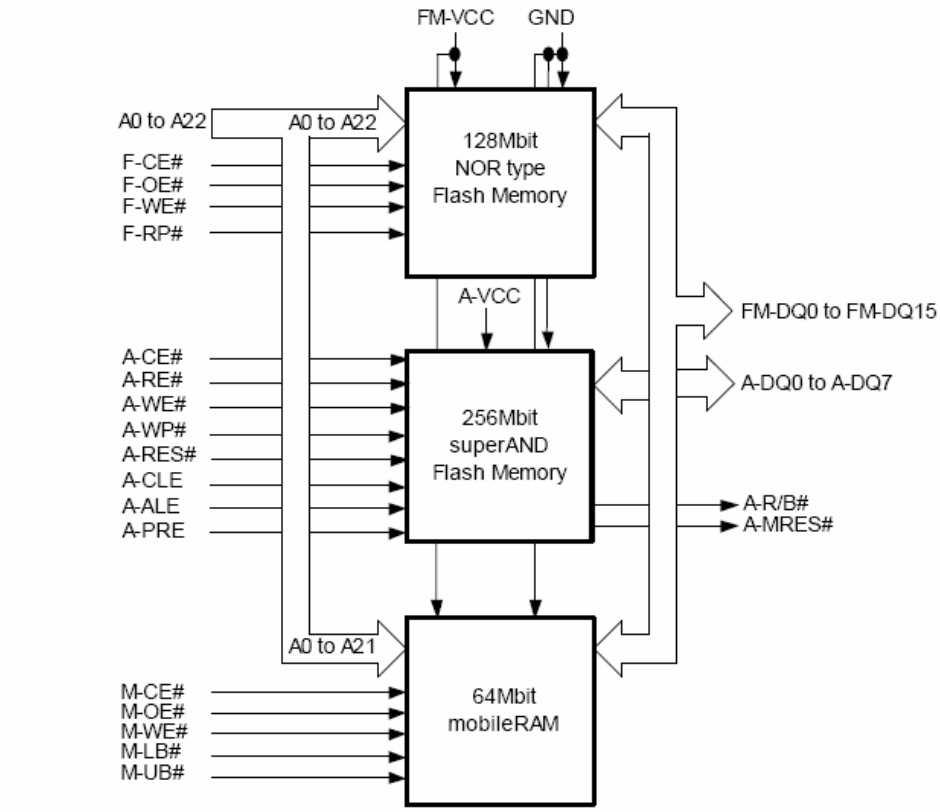
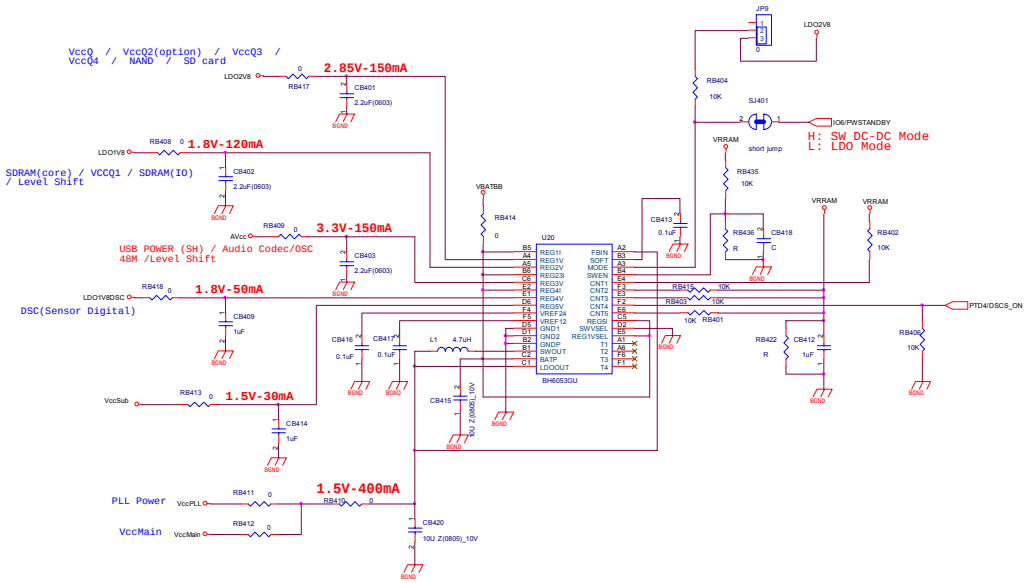
Block diagram:



7.5.1 MMP Power—PMIC

Power management IC BH6053GU U20 is designed for MMP. U20 provides voltages 2.8V LDO2V8 U20.A4, 1.8V LDO1V8 U20.A5, 1.5V LDO2V8 U20.D6 and 3.3V AVcc8U20.C6 for Multimedia processor (MMP), DSC module, LCD module, NAND FLASH and audio CODEC.



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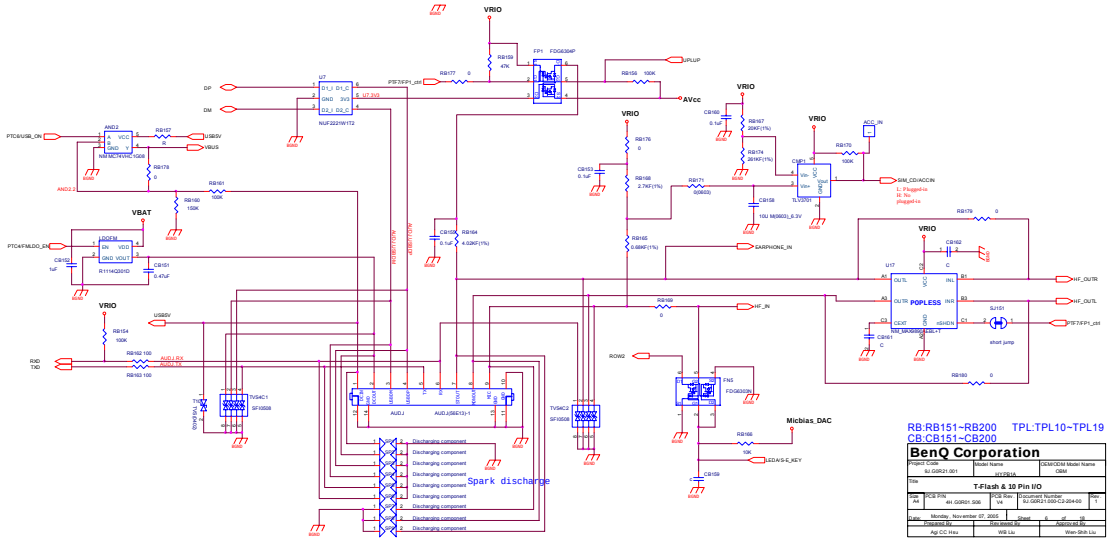
7.6 BC3-ROM

The Bluetooth main chip – BC3-ROM deals with BT RF signal from chip antenna and baseband signal from G2 including down/up-converting, de/- modulation and de/- coding … The BC3-ROM could accept clock frequency from 8MHz to 40MHz. In our application, we feed the chip with 26MHz clock from a external crystal. The BC3-ROM is also controlled by G2 via IRDA UART port. The Voice data between BC3-ROM and G2 are transmitted and received via MCSI interface and the other data are via UART. The SPI interface is reserved for status checking or firmware downloading for BT chip. The power BT chip needed outside is 2.8V the same with voltage level of I/O interface of G2.

7.7 10 pin I/O

Schematic



Pin No.	Pin Definition	Function description
1	DC in/USB 5V	External accessory power supply to the mobile phone
2	DC out(default)	Internal power provides for any powered accessory
3	USB data -	USB differential data line: D-
4	USB data +	USB differential data line: D+
5	UART Tx	UART data out line
6	UART Rx	UART data in line
7	Stereo out(right channel)	Use of the right audio path of the handfree and the accessory plug in detection
8	Mono out(left channel)	The left audio path of the handfree
9	Mic	The microphone of the handfree
10	Ground	Connect to system ground

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Description
The 10pin I/O Jack is used for 4 kinds of BenQ type accessory service: mono headset, stereo headset, UART data cable, and pure USB cable. Whenever the accessory plugs into the mobile, the SIM_CD will be pull to low level. And then according to the difference identified resistances mounted on the accessory, the system will get the difference ADC value from the EARPHONE_IN pin and recognize what type accessory has plugged in. The CMP1 is used to detect the voltage on the pin 9. In non-plugged-in situation, the pin 9 always has 2.8v potential voltage, and the output pin is high level (2.8v). Until the accessory plugs in, the Vin of the CP1 will detect a voltage under 2.6v, and the Vout connecting to SIM_CD will fall down to low level(0.0v). At the same time the line voltage is changed by the plugged in accessory. When the system polls low level from SIM_CD, it will read the current line voltage and convert it to digital value from the EARPHONE_IN pin. Each ADC value represent different type accessory.

For audio type accessories, the microphone bias provides a mechanism to act on the send/end key for mono or stereo type accessory. When each kind of audio type accessory plugs in, it will tune on the microphone bias. In this place FN5 plays an important role. FN5 is a dual NMOS package IC. If the microphone bias tune on, the first of the MOS in FN5 tunes into saturation. Until the send/end key is pressed, pin 9 connecting to the ground, the 1st NMOS will tune off and 2nd NMOS will tune on and go into saturation area. At this moment system gets a row2 pulled low information and send/drop the call.
When user sets up a call without the mono/stereo HF, the LEDA will tune on and the 2nd NMOS is forbidden to act.

7.8 T-FLASH card

The SD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode. Host System can choose either one of modes. Same Data of the SD Card can read and write by both modes. SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel.

Command:
Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line. A response is a token to answer to a previous received command. Responses are sent from a addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa. Data is transferred via the data lines.

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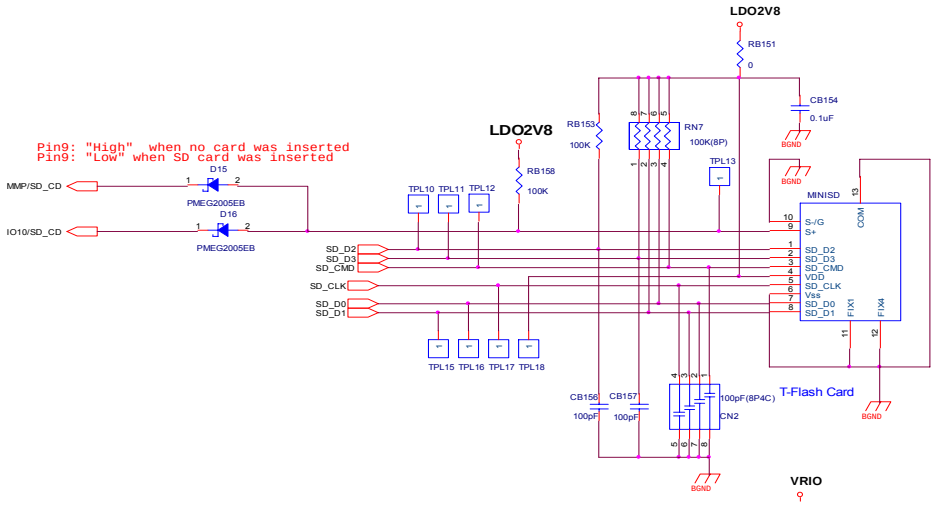
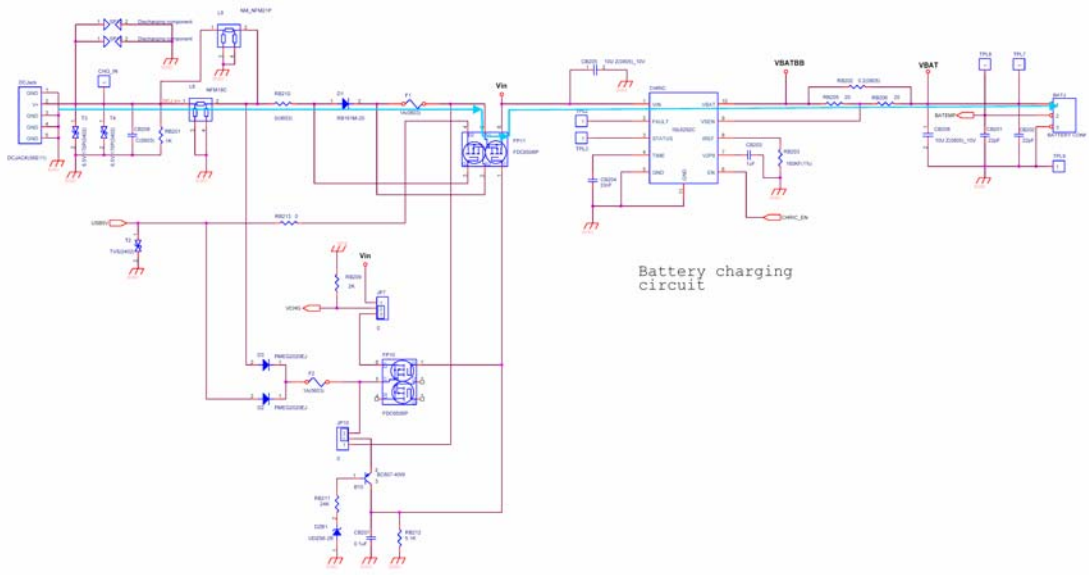
Schematic



7.9 Charging circuit

Schematic - Charging from AC Adaptor



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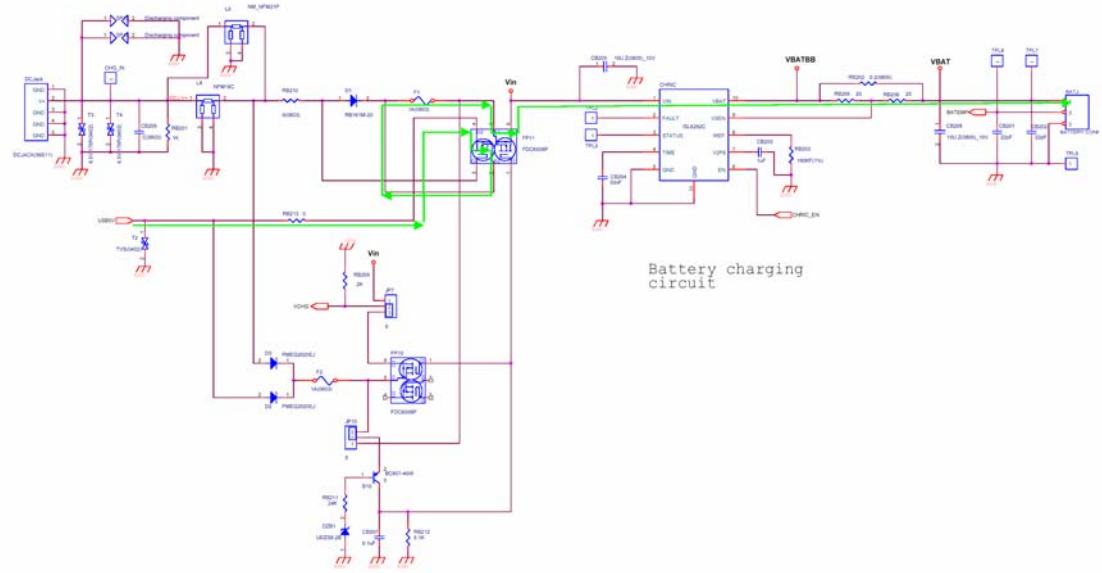
Schematic - Charging from USB



Description

S88 can charge the Li-ion/Li Polymer Battery from AC adaptor and USB, As Schematic - Charging from AC Adaptor, blue line is the charging route from adaptor show the route of USB and Schematic - Charging from USB, green line is the charging route from USB. While USB and adaptor have plugged in at the same time, FP11 allows charging only from adaptor. D1 avoids charging current flowing back to adaptor when USB is charging. Over voltage protection can be done by DZB1, B10 and FP10 whatever adaptor or USB is plugged in, there will be a voltage on VCHG pin, VCHG informs IOTA adaptor or USB is plugged in and IOTA controls CHRIC. HRIC ISL 6292C is described as below.

7.10 Li-ion/Li Polymer Battery Charger ISL6262C

The ISL6292C is an integrated single-cell Li-ion or Li polymer battery charger capable of operating with an input voltage as low as 2.4V. This charger is designed to work with various types of ac adapters or a USB port.

The ISL6292C operates as a linear charger when the ac adapter is a voltage source. The battery is charged in a CC/CV (constant current/constant voltage) profile. The charge current is programmable with an external resistor up to 1.5A. The ISL6292C can also work with a current-limited adapter to minimize the thermal dissipation, in which case the ISL6292C combines the benefits of both a linear charger and a pulse charger. The ISL6292C features charge current thermal foldback to guarantee safe operation when the printed circuit board is space limited for thermal dissipation. Additional features include preconditioning of an over-discharged battery, automatic recharge, and thermally enhanced DFN package.

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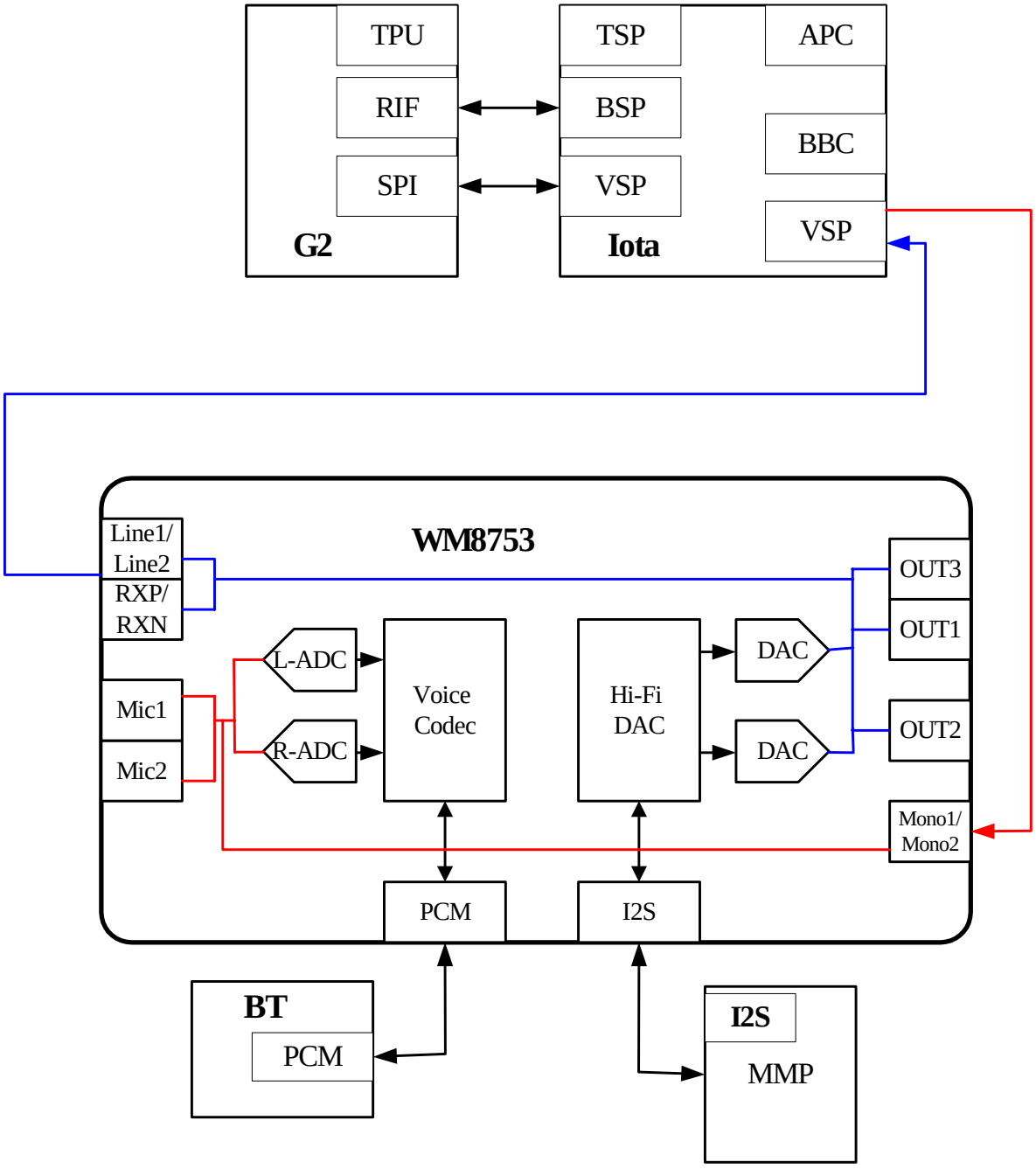
7.11 Audio Codec and Audio amplifier

Audio Codec Function Block



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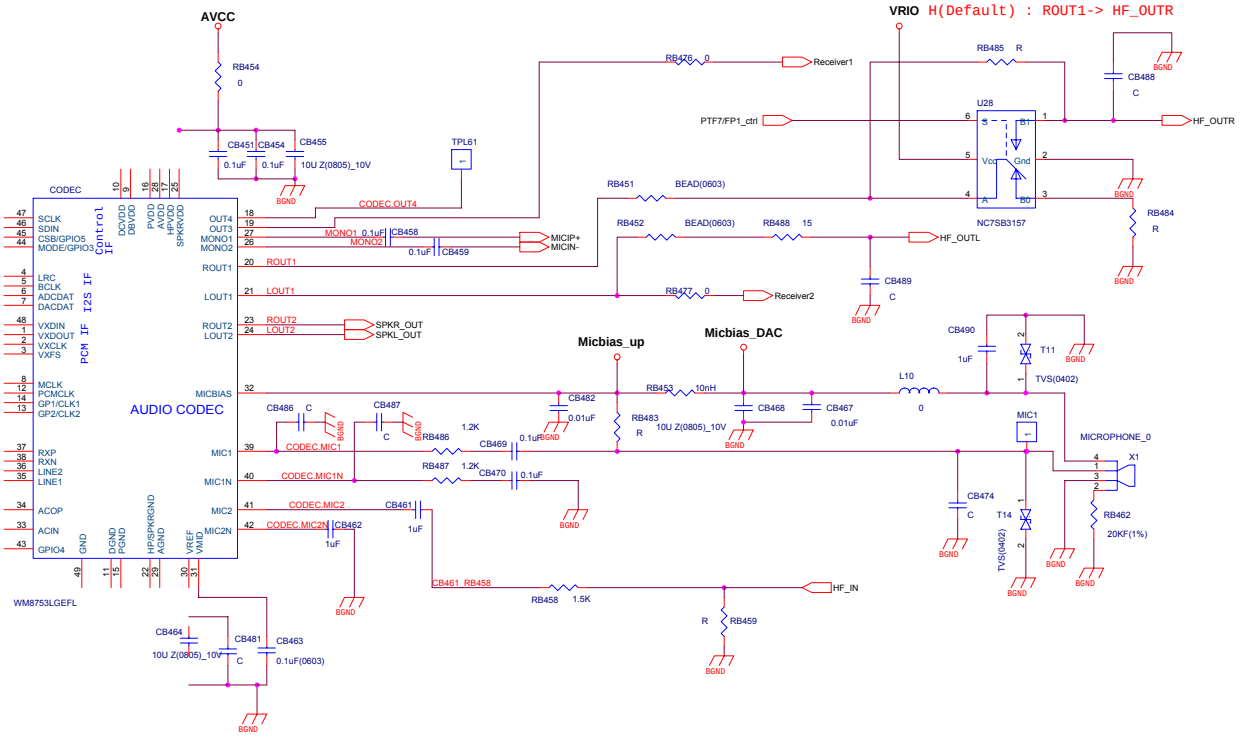
Description

The audio circuit uses the Wolfson WM8753 for audio total solution. The WM8753 is a low power, high quality stereo Codec with integrated voice CODEC designed for portable digital telephony application with Hi-Fi playback capability. The device integrates dual interfaces to two differentially connected microphones, and includes drivers for speakers, headphone and earpiece. Advanced on-chip digital signal processing performs tone control, Bass Boost and automatic level control for the microphone or line output through the ADC. The two ADCs may be used to support Voice noise cancellation in a partnering DSP, or for stereo recording.

So that all the voice signals, digital and analog, sink in the codec WM8753. For MP3, software midi playback ,and audio recording, the I2S interface provides a connection with the MMP. And it connects to analog base-band voice codec for mobile phone speech process. It uses the PCM interface to support the BlueTooth voice solution.

The schematic circuit design for speech paths



The voice input used to audio codec microphone port transmission the voice signal. Microphone input path to handheld and handfree application. The handheld used to differential input for main path .However handfree used to signal input transmission voice the uplink path.

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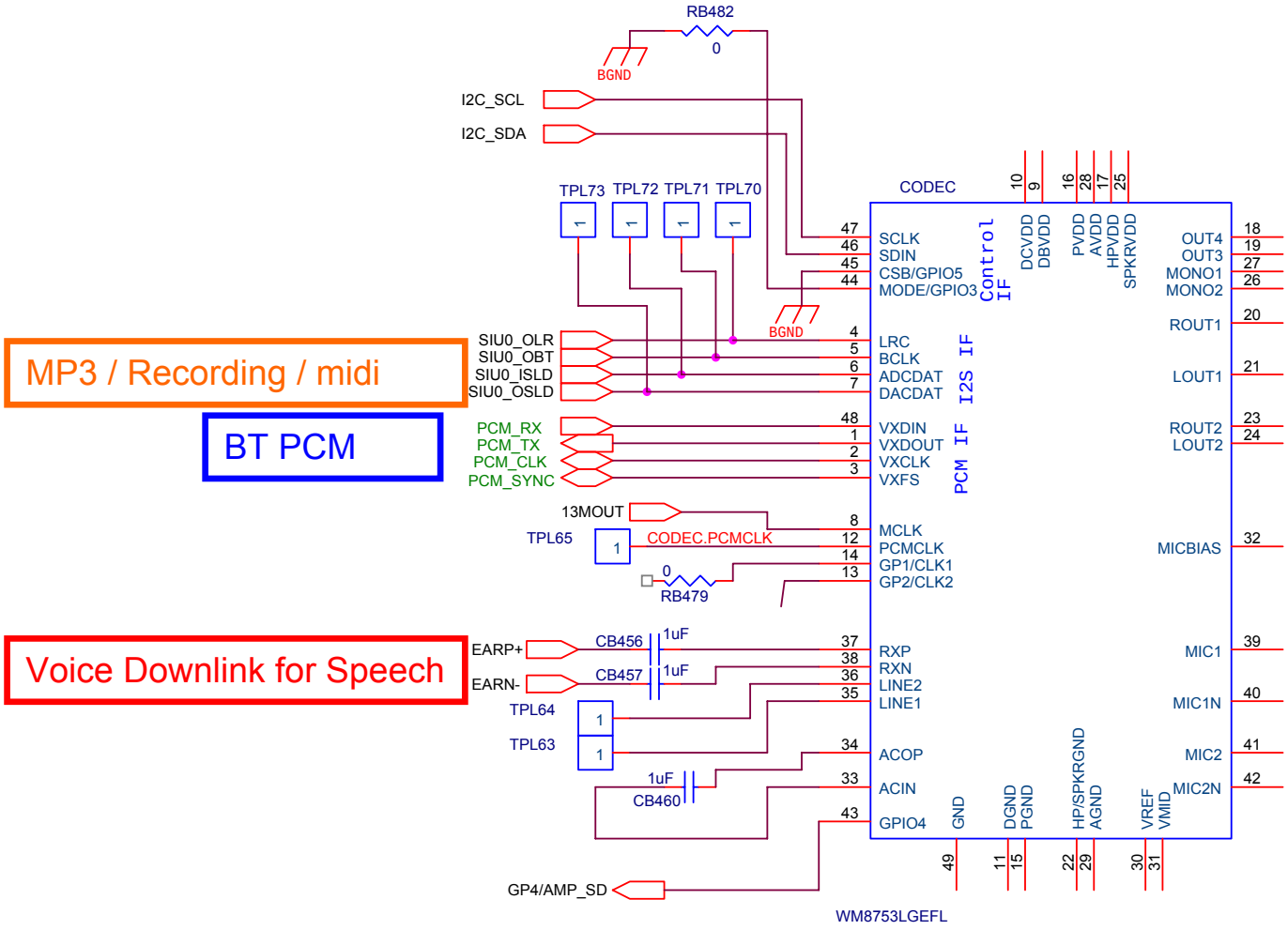
Multimedia application input path circuit design



The two signal input is used to voice path apply to bypass IOTA downlink signal and FM radio. However one differential input path used to melody function the transmission. The MP3 and Recoder to utilize audio codec digital input control, data transmission the I2C digital voice input transfer, the I2C control for audio codec command.

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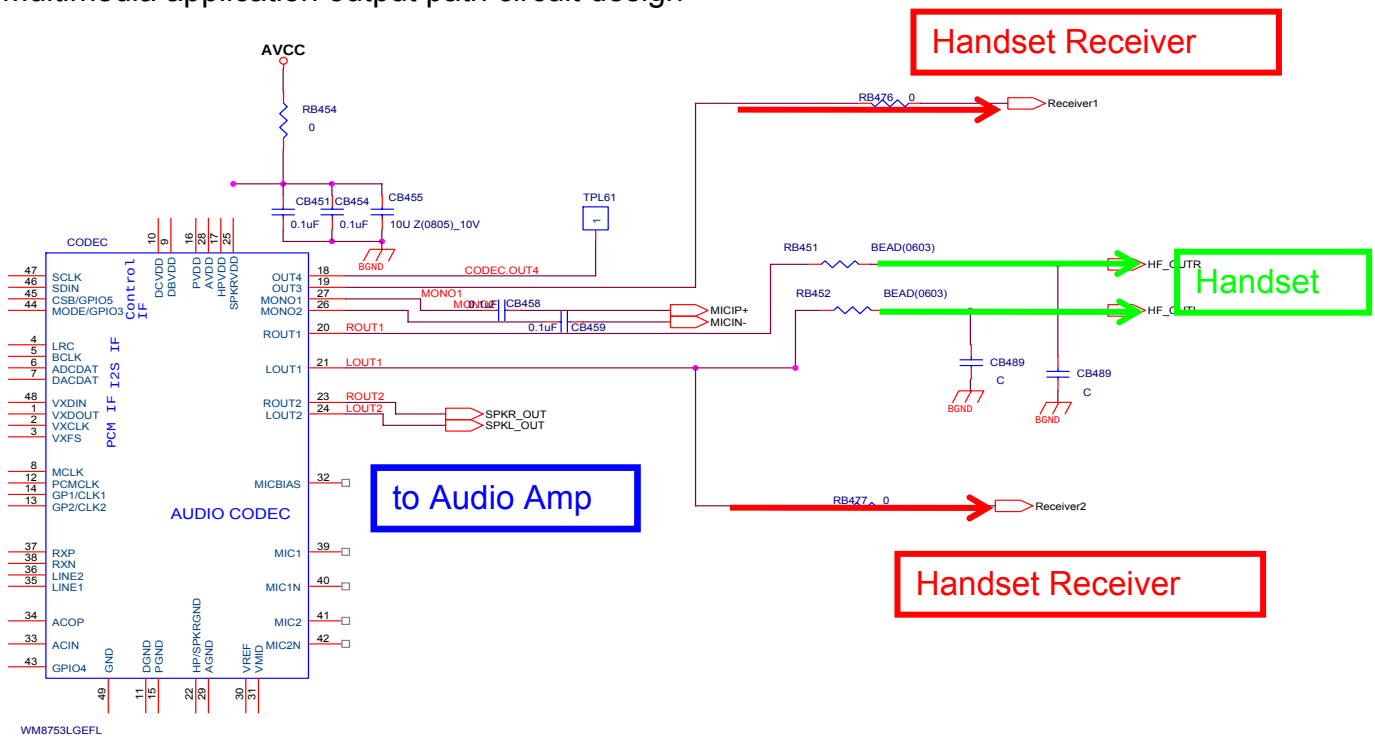
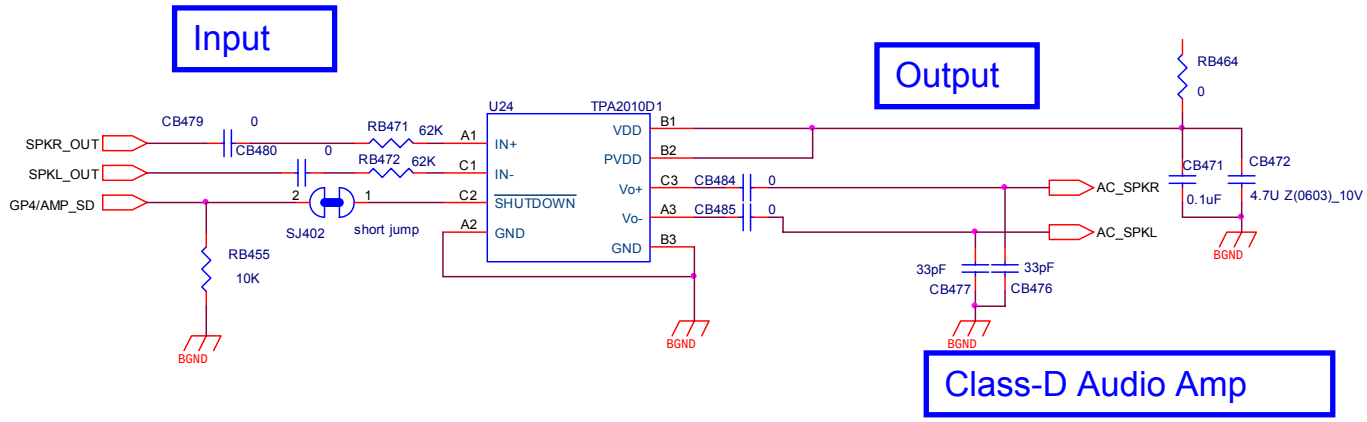
Multimedia application output path circuit design



Loudspeaker output path and D-amplifier design



The audio codec provides output path application, two mono output and one stereo output. A mono output used to differential signal applies to uplink voice output transfer IOTA produce. The mono2 output used to differential signal for Loukspeaker function, but design addition the D amplifier for gain amplifier provides MP3 play, melody and speaker phone function the application .The stereo output apply to handfree part. The Class-D audio amplifier has a high efficiency of the power transformation.

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7.12 OLED Module

AMOLED panel driving section

Pin no	Symbol	I/O	Description	Remark
1	/WR	I/O	Write enable signal for CPU interface	
2	/CS	I/O	Chip select signal	
3	/RESET	I/O	Reset signal	
4	GND	I	Ground	
5	D0	I/O	Data/command bus	
6	D2	I/O	Data/command bus	
7	D4	I/O	Data/command bus	
8	D6	I/O	Data/command bus	
9	D8	I/O	Data/command bus	
10	D10	I/O	Data/command bus	
11	D12	I/O	Data/command bus	
12	D14	I/O	Data/command bus	
13	GND	I	Ground	
14	FB	I	Voltage Feedback Input. FB regulates to 0.6V nominal. Connect FB to an external resistive divider	
15	RS	I/O	Data/command bus	Note 2
16	/RD	I/O	Read enable signal for CPU interface	
17	VDD_enable	I/O	OLED_Vdd power chip(MAX8560) enable signal	Note 3
18	CTRL	I/O	OLED_Vdd switching control signal	Note 4
19	VCC	I	Power supply for driver IC	
20	VDDIN	I	Power supply for OLED_Vdd curcuit	
21	GND	I	Ground	
22	VCOUT1	I/O	frame signal	
23	GND	I	Ground	
24	D15	I/O	Data/command bus	
25	D13	I/O	Data/command bus	
26	D11	I/O	Data/command bus	
27	D9	I/O	Data/command bus	
28	D7	I/O	Data/command bus	
29	D5	I/O	Data/command bus	
30	D3	I/O	Data/command bus	
31	D1	I/O	Data/command bus	
32	DTX	I/O	16+2 /16- bit mode switching signal	Note 5
33	GND	I	Ground	
34	OLED_VSS	I	OLED_Vss	Note 6

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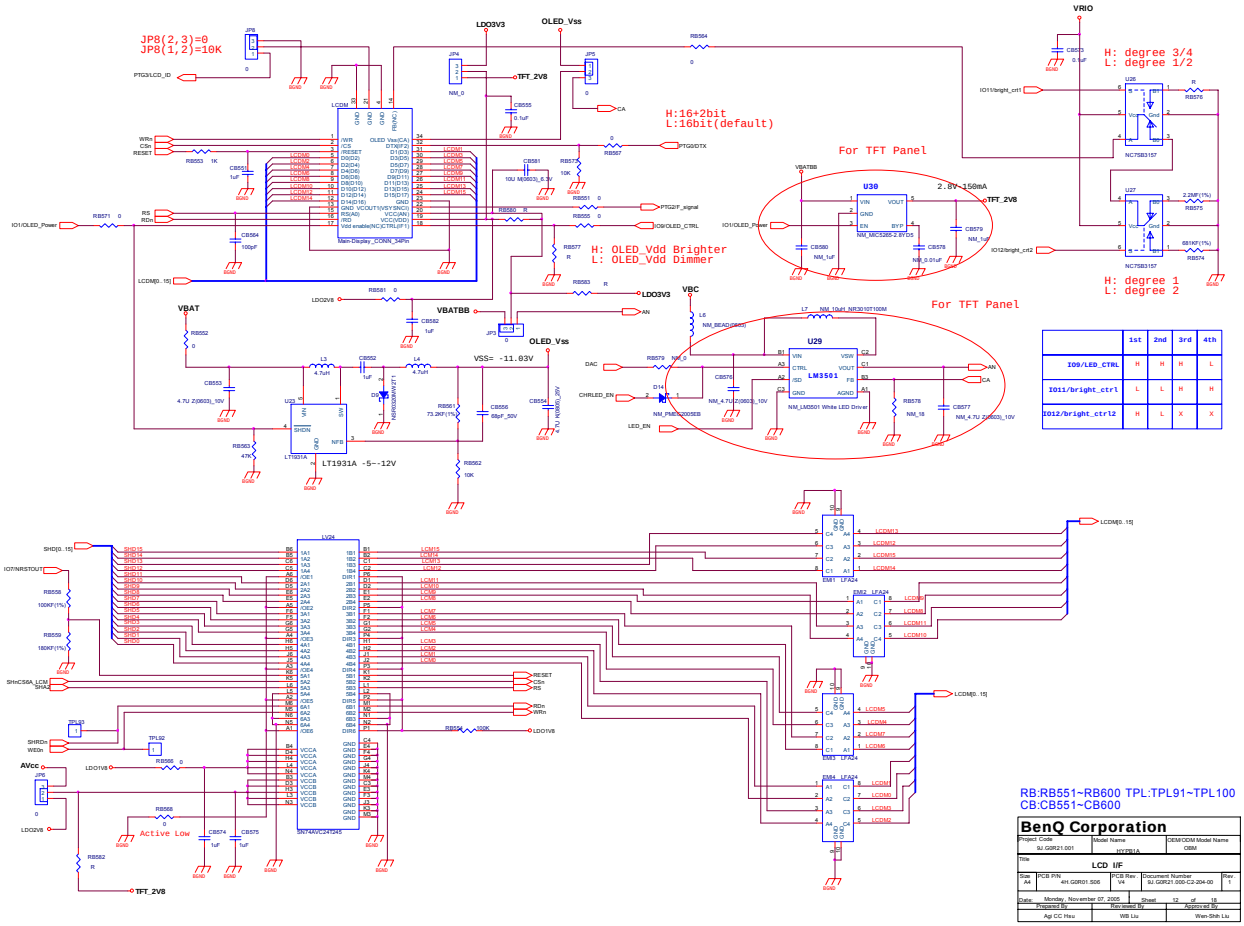
OLED introduction

OLED (Organic Light Emitting Diode or Organic Light Emitting Display) is a kind of advanced display technology with the following superior characteristics.

- Self-emissive
- Very thin form factor
- High luminance
- High luminous efficiency
- High contrast
- Fast response time
- Wide viewing angle
- Low power consumption
- Wide temperature operation range
- Potential of flexible substrate

OLED schematic



	1st	2nd	3rd	4th
IO9/LED_CTRL	H	H	H	L
IO11/bright_ctrl	L	L	H	H
IO12/bright_ctrl2	H	L	X	X

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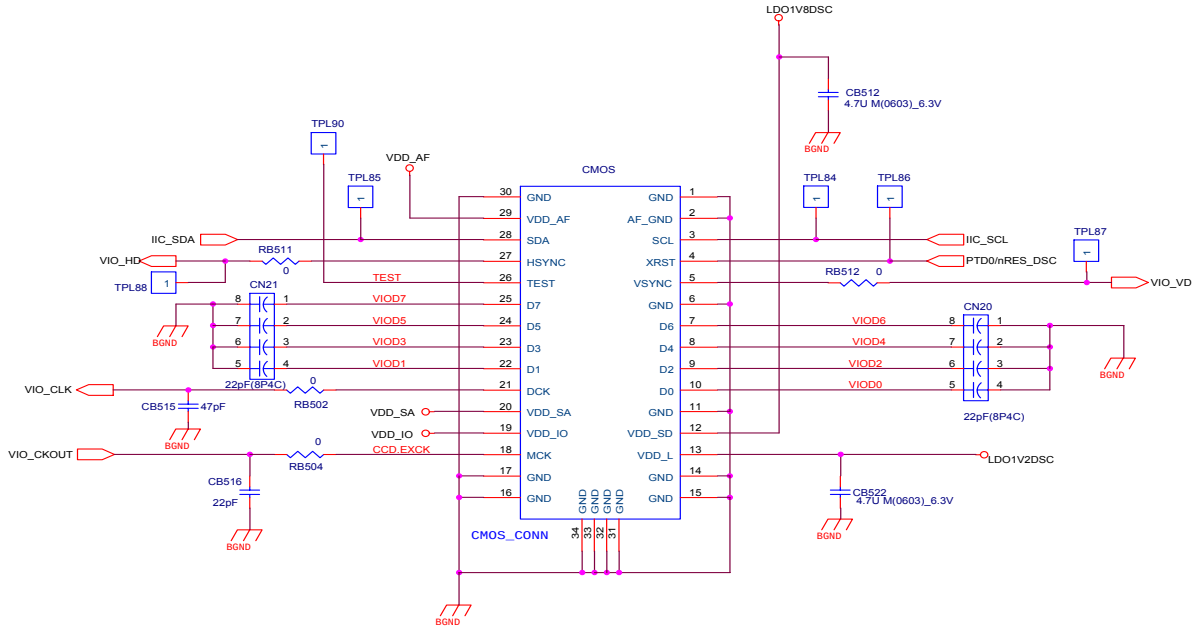
7.13 Camera module

Description

The SONY module MCB772-Q is 2.0 Mega Pixel CMOS Camera Module with auto focus function for mobile application. It contains a 2M CMOS Sensor, a set of lens, an AF driver, a camera DSP and EEPROM.

MCB772-Q requires three different voltages of power supplies, which include VDD_AF.PIN29 (for auto focus). VDD_SA PIN20 (for sensor analog), VDD_IO PIN19 (for DSP IO) = 2.8V, LDO1V8DSC PIN12 (for sensor digital) = 1.8V and LDO1V2DSC PIN29 (for DSP core) = 1.2V. This module is controlled by the SH-Mobile J2, the multimedia processor, using the standard I2C control interface. Other interfaces between this module and J2 includes 8-bit YUV data bus, an external 24MHz clock input MCK provided by J2, an output clock DCK and the synchronous signal of VSYNC and HSYNC from DSC module. XRST is controlled by the SH-Mobile multimedia processor.

Camera Connector and Pin Assignment



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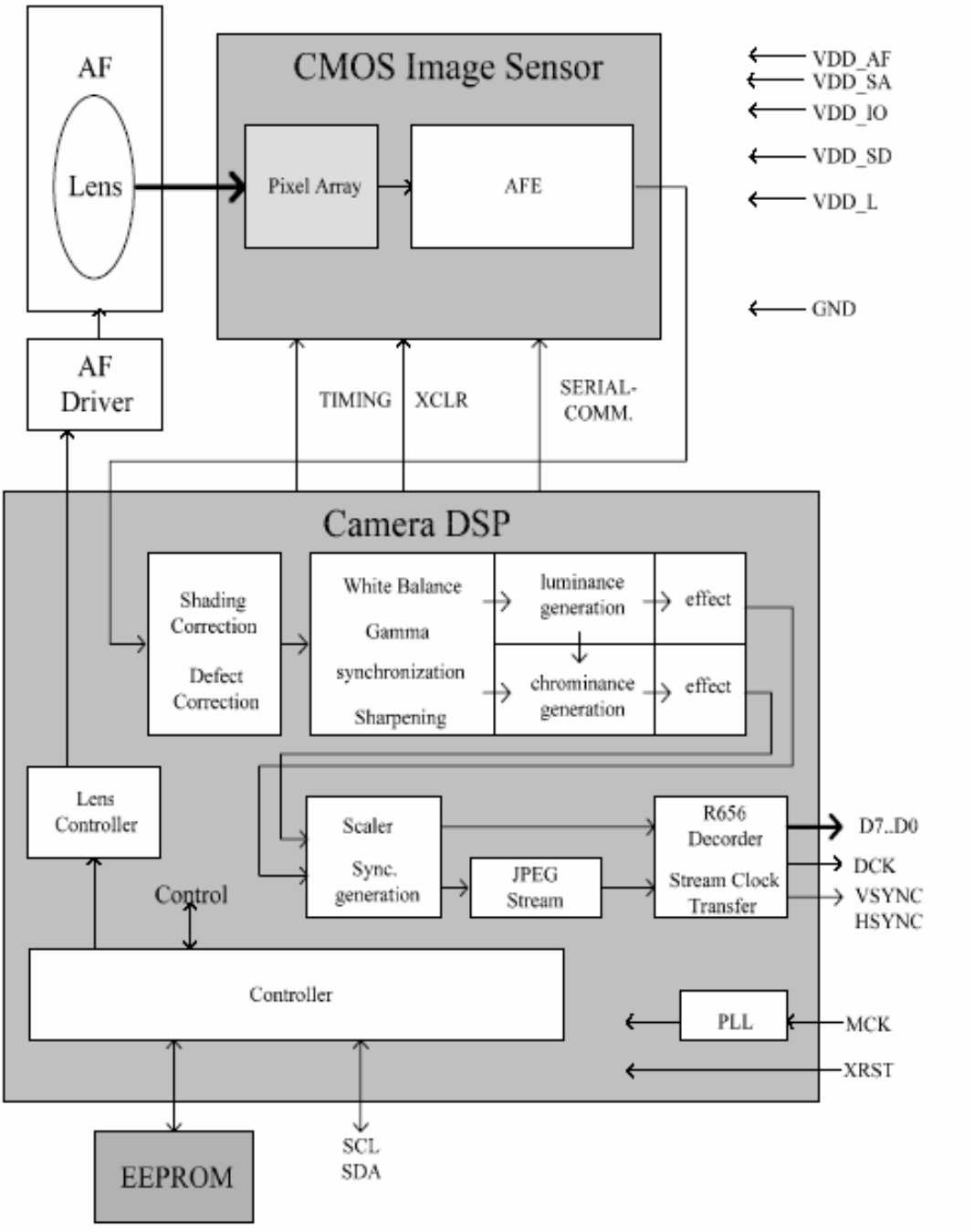
Module Block Diagram



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7.14 Flash LED driver circuit

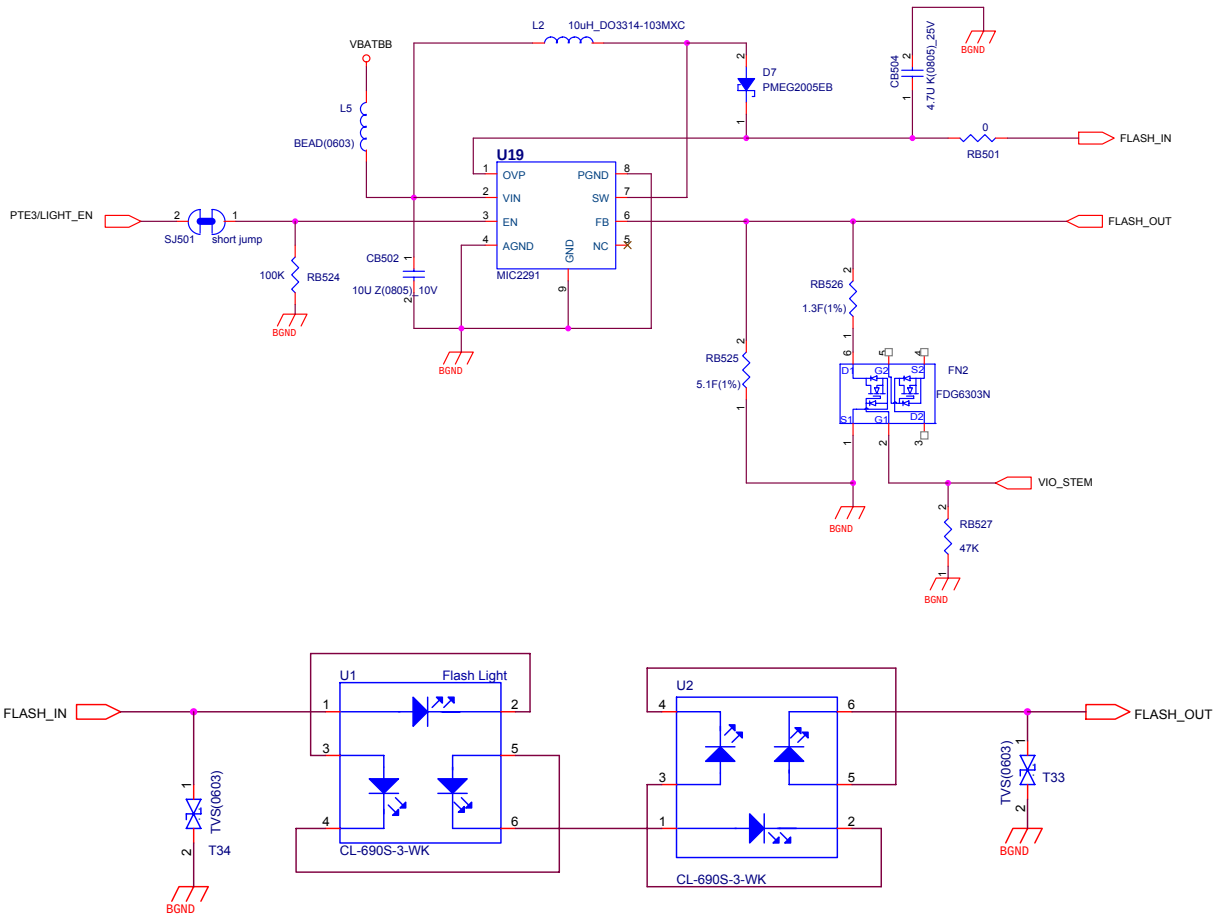
Description

The MIC2291 U19 is a 1.2MHz Pulse Width Modulation (PWM) boost-switching regulator that is optimized for high-current white LED photo flash application. It implements a constant frequency 1.2MHz PWM control space by reducing external component sizes. The added benefit of the constant frequency PWM scheme is much lower noise and input ripple injected back to the battery source than with variable frequency topologies.

The Feedback pin is the output voltage sense mode. Connect the cathode of the LED to this pin. A resistor from this pin to ground sets the LED current. The feedback voltage is set to 95mV on MIC2291.

On camera preview mode, we turn on EN PTE3/LIGHT_EN.PIN3 pin to supply 18mA to Flash LED. On camera capture mode, turn on VIO_STEM pin from SH-Mobile J2 to adjust the resistor on feedback pin to get 70mA.

Schematic



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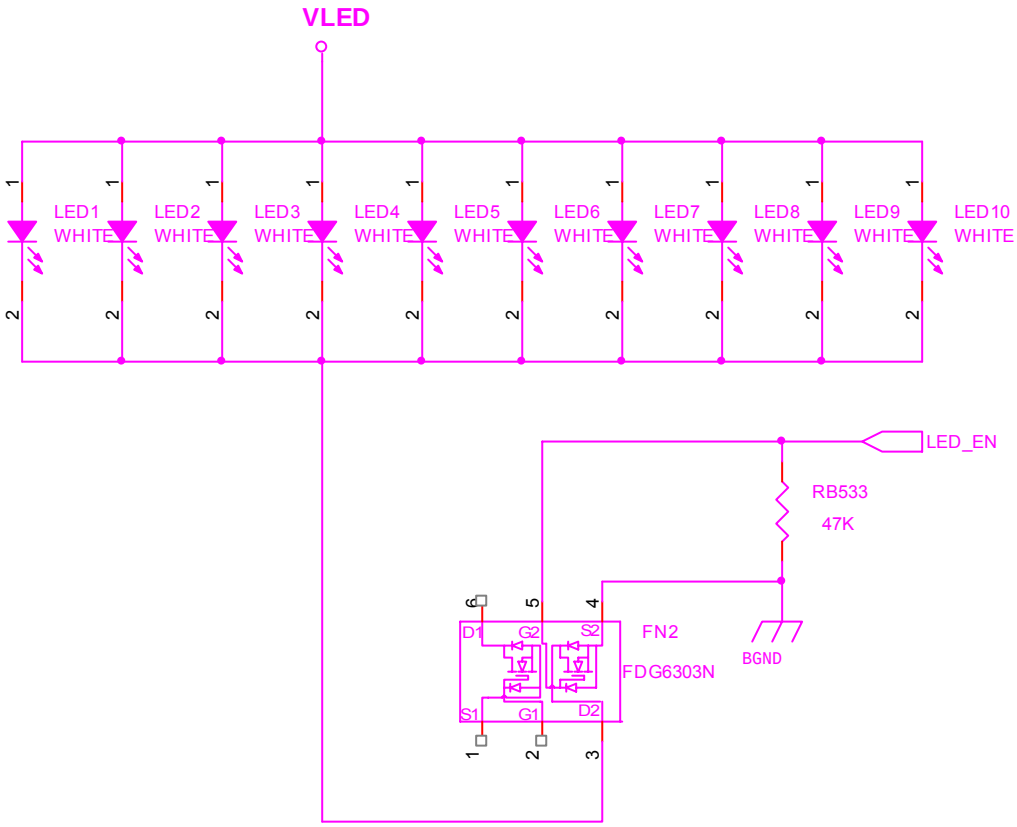
7.15 Keypad LED circuit

Description

S88 employs ten white LEDs for keypad backlight. The ON_OFF timing of LED is controlled by FN2. When LED_EN are set to “H”, Keypad LEDs are turned on; otherwise the Keypad LEDs are turned off.

Schematic



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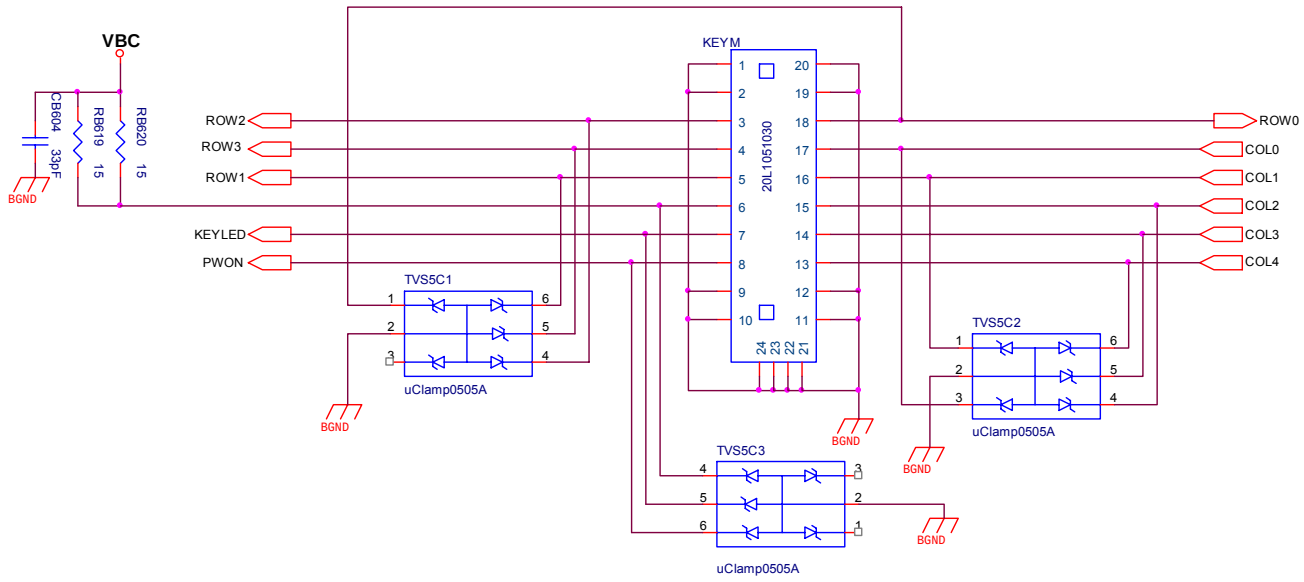
7.16 Keypad

Description

The keypad is made of a 5 Column × 5 Row matrixes. The keypad matrix is as follows.

	COL0	COL1	COL2	COL3	COL4	
ROW0		Vol. Up	3	2	1	Shutter section 1
ROW1		Vol. Down	6	5	4	Shutter section 2
ROW2	SOFT LEFT	SEND	9	8	7	HF_S/E KEY
ROW3	SOFT RIGHT		#	0	*	END/POWER
ROW4	MENU (OK)	UP	LEFT	DOWN	RIGHT	

Schematic



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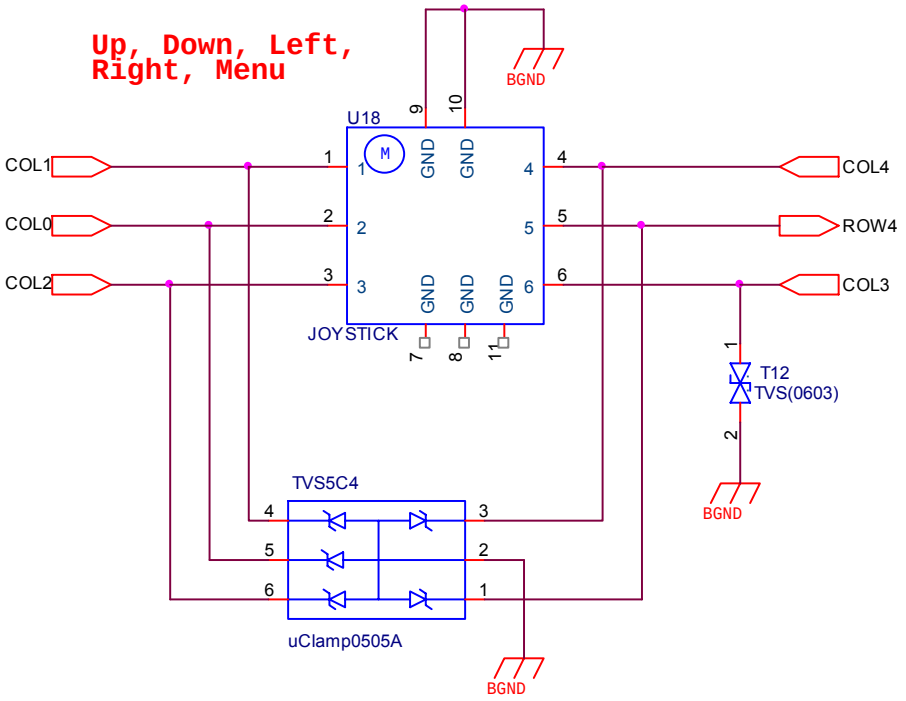

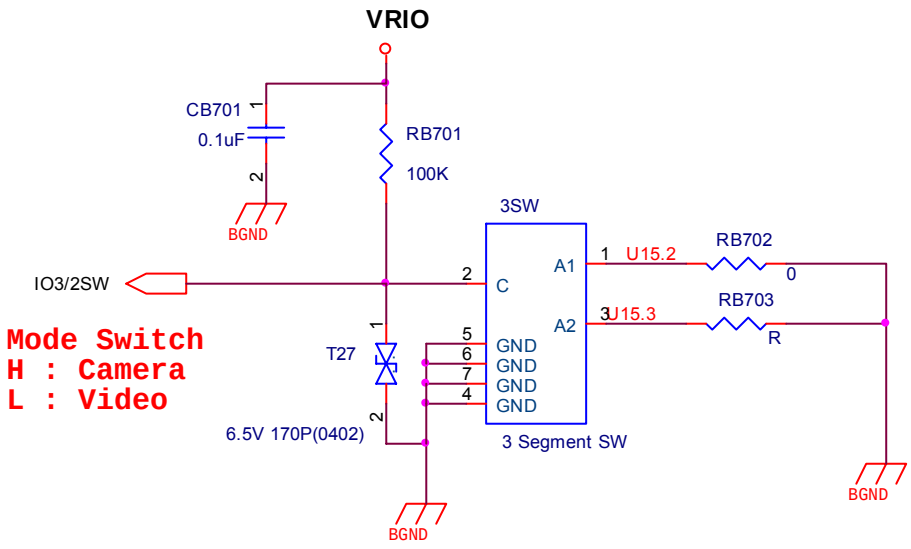

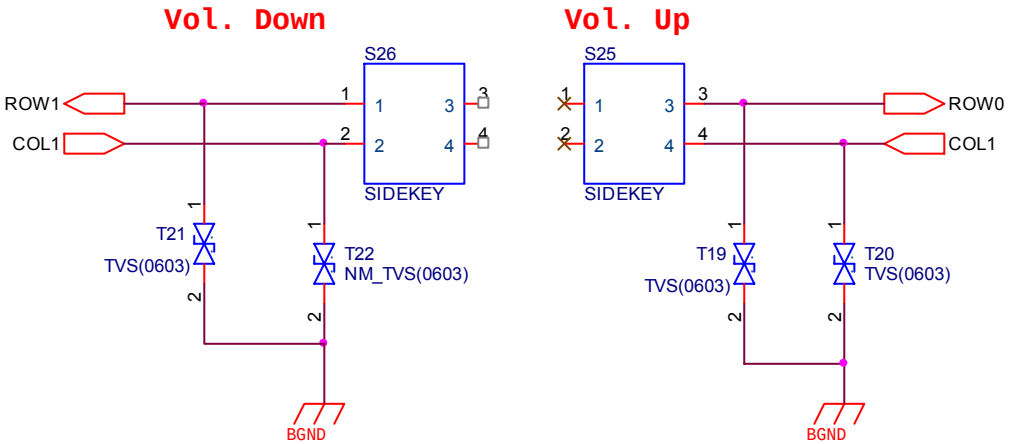

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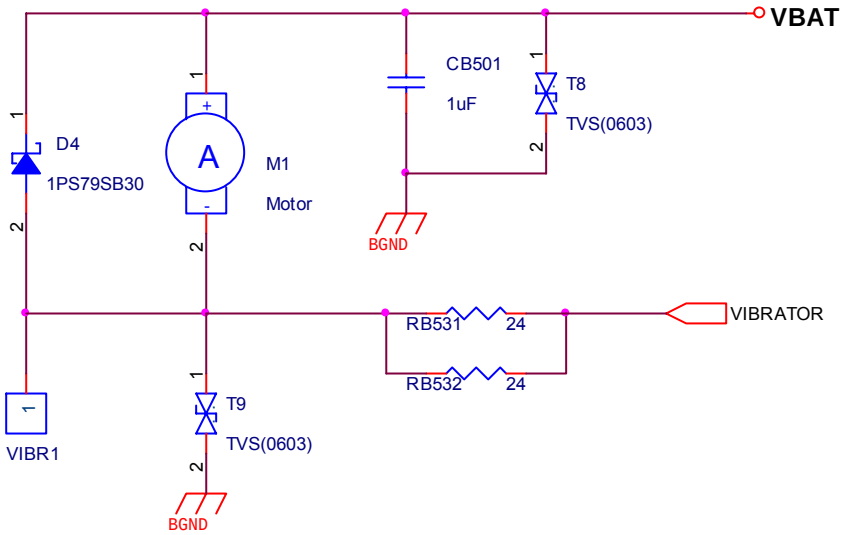
7.17 Vibrator circuit

Description

Vibrator is enabled by LEDB1 IOTA.B10 (LEDB2) control logic in IOTA. When the logic of LEDB is set to “H”, the vibrator will activate. The D4 is used to reduce EMF. The default VBAT is 3.8 volt.

Schematic



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