



MOTOROLA

Personal Communications Sector

 **GSM**
Service Support
Level 3 Authorized



GSM Service Support

Training - Documentation - Engineering

W388



Level 3
Circuit Description
20 May 200*
V1.0

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Receive

1.1 Band selection

The radio frequency signal is received from internal antenna (EU band: PIFA type, US band: FICA type). Received GSM RF signal enters to PCB through the RF switch JP201. At this moment the T/R switch combined in PA U201 is switched to RX mode to let the signal input to next stage. Then the signal goes into SAW filter, BF201 and BF202, which reject out-band signal and transfer the signal from single-end to balanced. And the matching circuits between T/R switch and SAW filter reduce the unwanted RF signal reflection and provide a flat frequency response in the operation band. Finally the received signal will be fed into Locosto U101 DRP core through a balanced MLCC matching network. The following table describes the control voltages of PA.

| W230 EU | V _{LOGIC} | TX_En | BS |
|---------|--------------------|-------|----|
| Standby | 0 | X1 | X1 |
| RX 900 | 1 | 0 | 0 |
| RX 1800 | 1 | 0 | 1 |
| TX 900 | 1 | 1 | 0 |
| TX 1800 | 1 | 1 | 1 |

The RF signal is received by internal antenna, and the signal is passing through the RF switch JP201 and then fed into T/R switch in PA. The low band (GSM900) RX received signal is transmitted from U201 (Pin 7) and input to low-band SAW filter BF201, while the high band (DCS1800) RX received signal from U201 (Pin 6) and then input to high-band SAW filter BF202. The last stage of RX on PCB is Locosto U101, and the DRP process will make the signal into binary data.

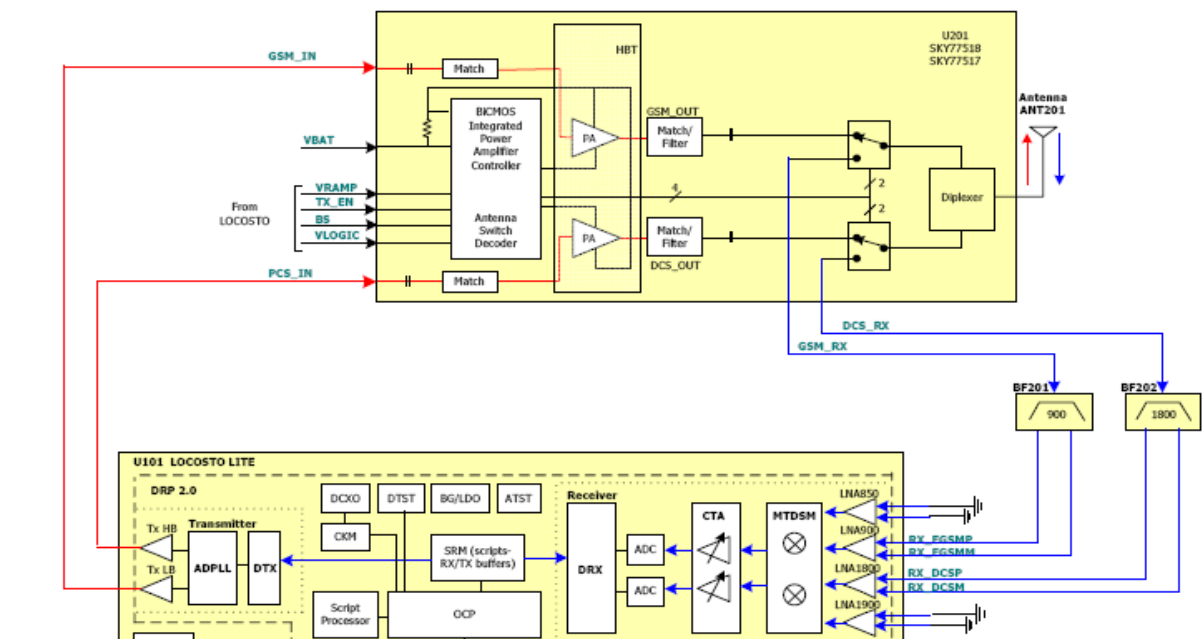


Figure 1: Locosto TX/RX Paths Description

1.2 Locosto RX Mode

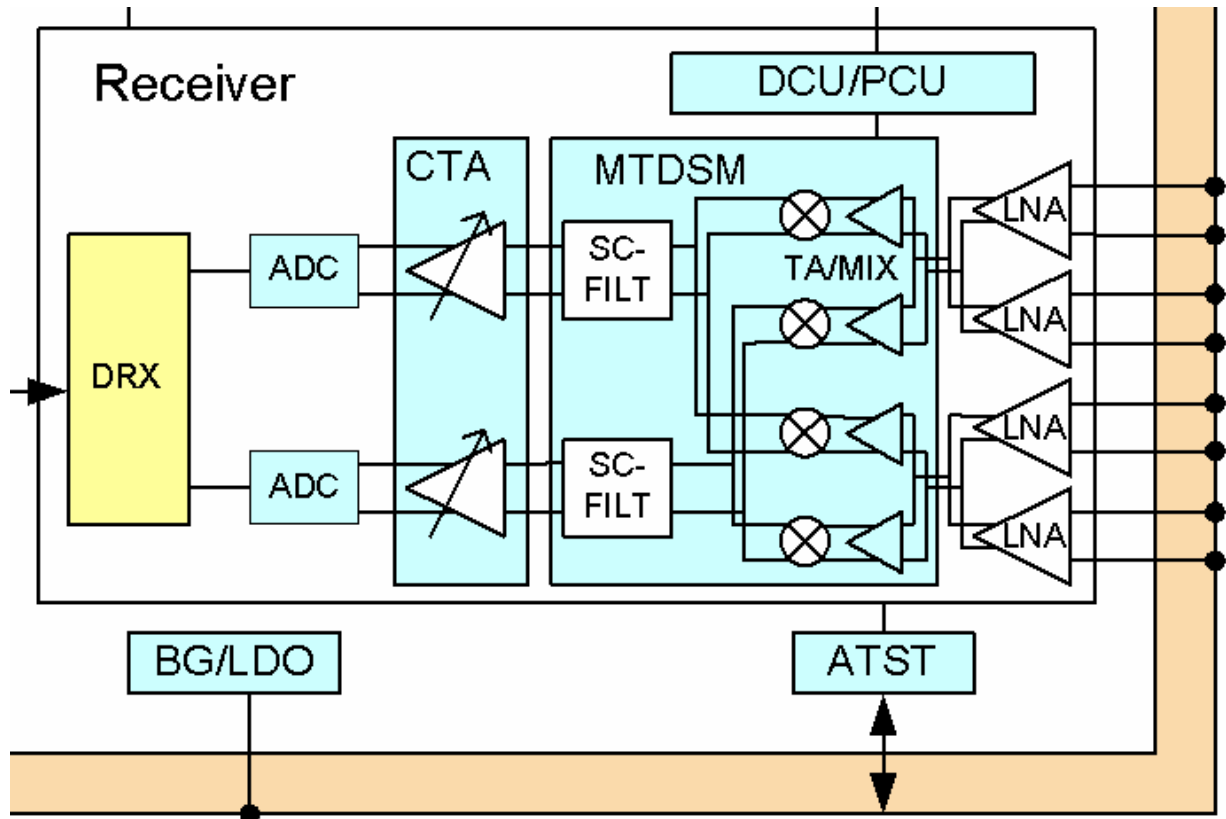
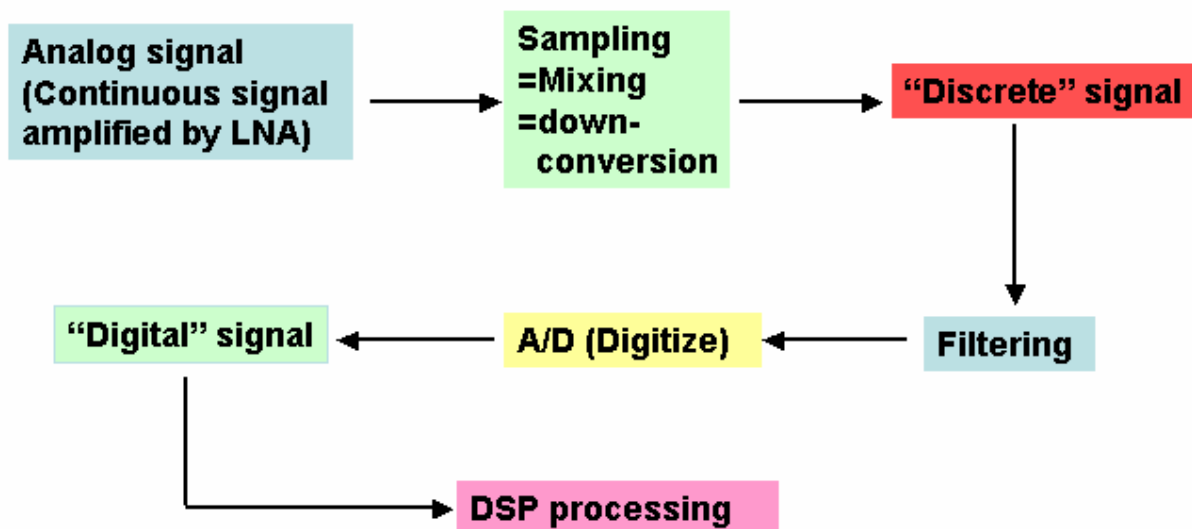


Figure 2: Locosto RX Signal Process

As described in Figure 2, when the RF signal is input to Locosto, it will be amplified by a differential LNA in advance, in order to obtain a better NF in the last receiving stage. And then it will be turned into discrete IF signal by a high-speed mixer. After passing through a filter and an A/D converter, the discrete signal will become digital signal and then input to Locosto core to do DSP process. The detail RX signal route is depicted as below:



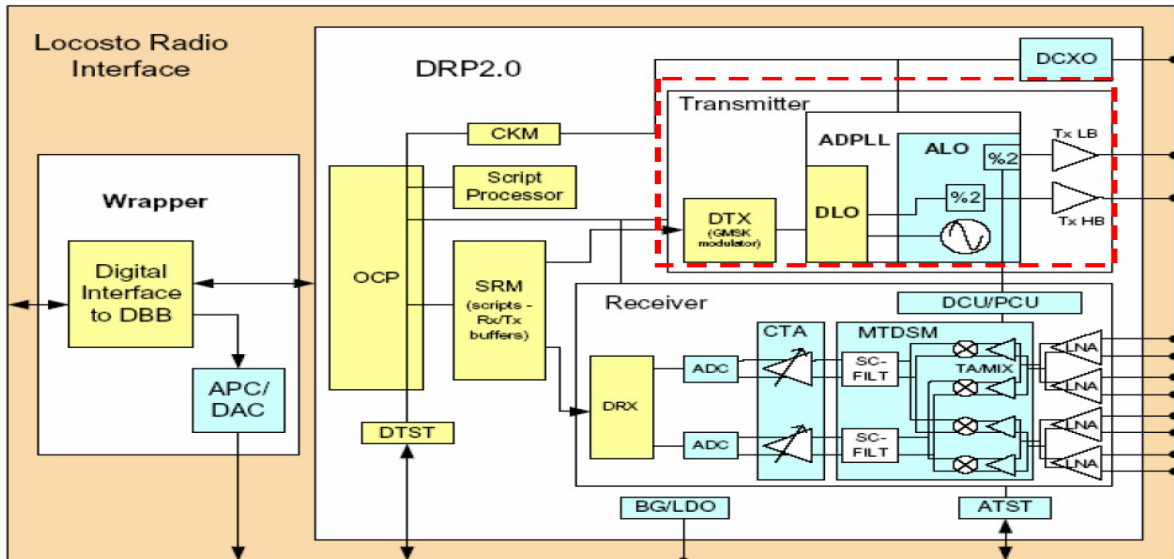


Figure 3: Baseband Downlink Block Diagram

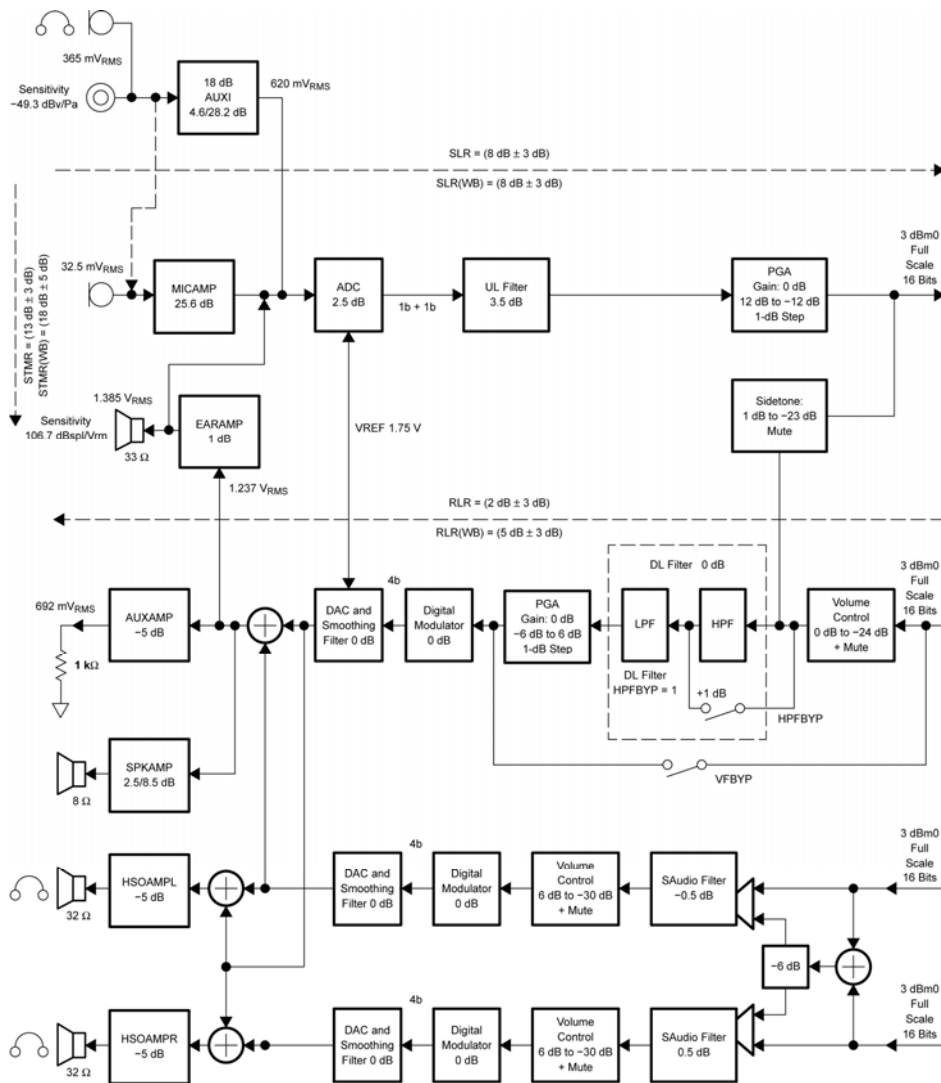


Figure 4: Audio Codec Block Diagram

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1.3 Audio Codec

The Audio codec consist of a voice codec dedicated to GSM application and an audio stereo line. The voice codec circuitry processes analog audio components in the uplink path and applies this signal to the voice signal interface for eventual baseband modulation. In the downlink path, the codec circuitry changes voice component data received from the voice serial interface into analog audio. The voice codec support an 8/16 kHz sampling frequency. The stereo audio path converts audio component data received from the I2S serial interface into analog audio. The following paragraphs describe these uplink/downlink and audio stereo functions in more details.

1.3.1 Voice Downlink Patch

The voice downlink path receives speech samples at the rate of 8 kHz from the DSP via the voice serial interface VSP and converts them to analog signals to drive the external transducers.

The digital speech coming from the [Locosto-Plus IC U101 \(DSP\)](#) is first fed to a speech digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate from 8 kHz up to 40 kHz to allow the digital-to-analog conversion to be performed by an over-sampling digital modulator. The second function is to band-limit the speech signal with both low-pass and high-pass transfer functions. The filter, the PGA gain, and the volume gain can be bypassed by programming.

The interpolated and band-limited signal is fed to a second order Σ - Δ digital modulator sampled at 1 MHz to generate a 4-bit (9 levels) over-sampled signal. This signal is then passed through a dynamic element-matching block and then to a 4-bit digital-to-analog converter (DAC).

Due to the over-sampling conversion, the analog signal obtained at the output of the 4-bit DAC is mixed with a high frequency noise. Because a 4-bit digital output is used, a first-order RC filter (included in the output stage) is enough to filter this noise.

The volume control and the programmable gain are performed in the RX digital filter. Volume control is performed in steps of 6 dB from 0 dB to -24 dB. In mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from -6 dB to +6 dB in 1-dB steps to calibrate the system depending on the earphone characteristics. The earphone amplifier provides a full differential signal on the terminals [EARP Triton-Lite Pin J2](#) and [EARN Triton-Lite Pin H2](#). The 8-Ohm speaker amplifier provides a differential signal on the terminals (SPKPA, SPKPD) and (SPKNA, SPKND).

1.4 Earpiece Receiver

The Receiver [J605 \(Pin1 and Pin2\)](#) are connected to [EARP Triton-Lite Pin J2](#) and [EARN Triton-Lite Pin H2](#).

1.5 Headset

The headset uses a standard 2.5mm phone jack. The interrupt for the headphones is detected on the [HS_DETECT \(U101 Pin K7\)](#) line from Pin 6 of Headset Jack [J604](#). This signal will be pulled to low when the headset is connected.

1.6 Speaker Phone

When the handset set the hand-free mode, the [Triton-Lite](#) will switch from [EARP/EARN](#) to [SPKP/SPKN](#) trace and receiver signal will be through Audio amplifier [U601](#) to [Speaker](#).

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1.7 Data Download Path

The External download cable is connected to the USB Jack J501. The download path is routed from J501 Pin2 and Pin 3 to DM_TXD_SPK_L and DP_RXD_MIC_R. The DM_TXD_SPK_L and DP_RXD_MIC_R signal connect to Triton-Lite IC U103 Pin A7 and Pin A8 to provide this capability. When software is set to download/upload mode, and detect USB_ID (J501 Pin 4) is floating, the phone will entered to download/upload state till download cable pulls out.

1.8 FM radio

The headphone antenna is used with a standard 2.5mm phone jack (J604). Silicon Lab Si4703 (U202) demodulated the FM radio. The left and right audio channels are driven by Triton_Lite (U103) audio amplifier onto left and right audio path and common audio connector (J604) is used for the audio return path and FM antenna.

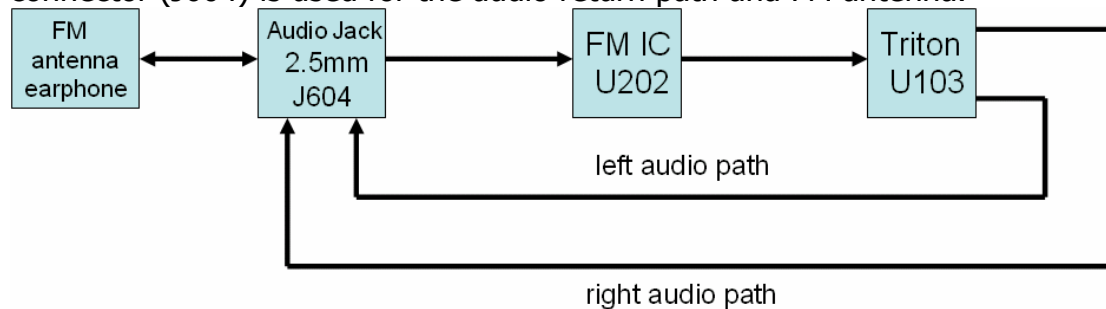


Figure 5: FM Block Diagram

2 Transmit

2.1 Audio (Voice uplink Patch)

The VUL path includes two input stages. The first stage is a microphone amplifier, compatible with electric microphones containing a FET buffer with open drain output. The microphone amplifier has a gain of typically 25.6 dB and provides an external voltage of 2.5V to bias the microphone (MICBIAS Triton-Lite Pin G6).

The headset microphone input HSMIC and the auxiliary input can be used as differential inputs of the handset *microphone amplifier* (low input level) or other devices (higher input level): HSMIC = HSMICIP and AUXI = HSMICIN, handset microphone input terminals are then set to a high impedance state and a biasing voltage be available on LDO(U603 2.8V). In this configuration, the *microphone amplifier* has a different gains: 25.6 dB (microphone input type).

The microphone amplification stage is used to amplify the FM radio left channel (amplifier gain is 4.9 dB), while the auxiliary amplification stage is used to amplify the FM radio right channel. The other input terminals are discarded and set to a high impedance state. In that configuration, the microphone amplification stage output is not connected to the ADC input, but to an audio output stage through a logarithmic "PGA" gain stage. The amplification stage performs single to differential conversion.

The resulting fully differential signal is fed to the analog-to-digital converter (ADC). The ADC conversion slope depends on the value of the internal voltage reference.

Analog-to-digital conversion is performed by a third-order $\Sigma\text{-}\Delta$ modulator with a

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sampling rate of 1MHz/2MHz. Output of the ADC is fed to a speech digital filter, which performs the decimation down to 8kHz/16kHz and band-limits the signal with both low-pass and high-pass transfer functions. Programmable gain can be set digitally from -12 dB to +12 dB in 1 dB steps and is programmed with the VULPG bits of the VULGAIN register. The speech samples are then transmitted to the DSP via the voice serial interface (VSP) at a rate of 8kHz /16kHz. Programmable functions of the voice uplink path, power-up, input selection, and gain are controlled using the BSP or the USP serial interfaces. The uplink voice path can be powered down with the VULR bit of the TOGB register.

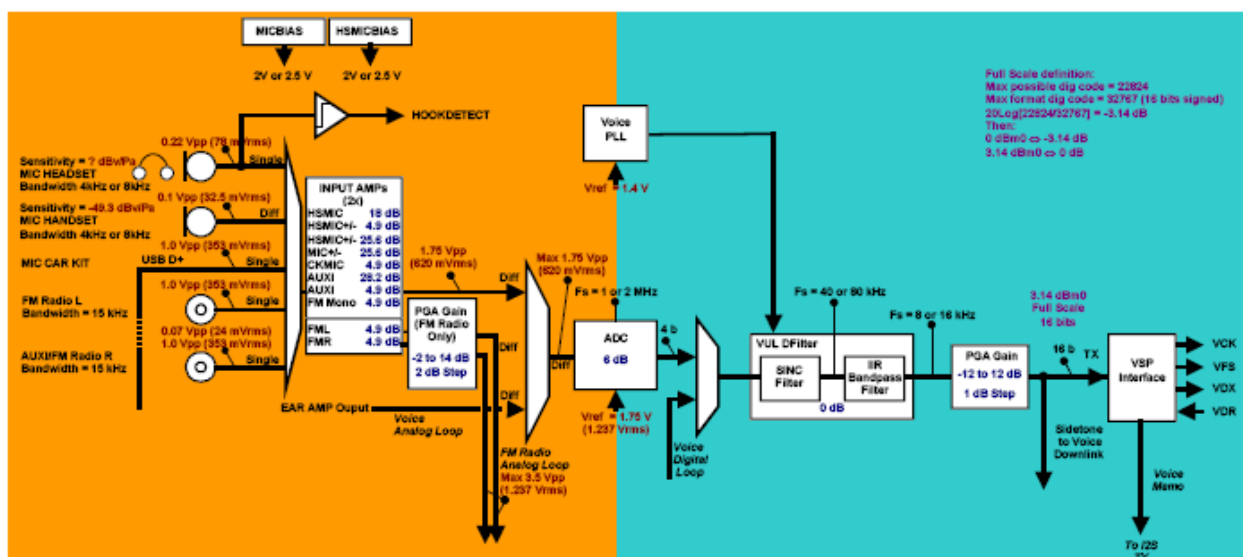


Figure 6: Voice Uplink Paths

2.2 Data Upload Path

The External download cable is connected to the USB Jack **J501**. The upload path is routed from **J501 Pin2** and **Pin 3** to **DM_TXD_SPK_L** and **DP_RXD_MIC_R**. The **DM_TXD_SPK_L** and **DP_RXD_MIC_R** signal connect to **Triton-Lite IC U103 Pin A7 and Pin A8** to provide this capability. When software is set to download/upload mode, and detect **USB_ID (J501 Pin 4)** is floating, the phone will entered to download/upload state till download cable pull out.

2.3 Stereo Audio Path

The stereo audio path receives Left and right signal samples at the rate of a programmable frequency, from 8kHz to 48kHz, via the I2S serial interface and converts them to analog signals to drive the external audio signal or speech transducers.

The digital audio signal is first fed to an audio digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate to allow the digital-to-analog conversion to be performed by an over-sampling digital modulator. The second function is to band-limit the audio signal with a low-pass transfer functions. The interpolated and band-limited signal is fed to a second order Σ - Δ digital modulator sampled at f_{S1} frequency to generate a 4-bit (9 levels) over-sampled signal. This signal is then passed through a dynamic element matching block and then to a 4-bit digital-to-analog converter (DAC).

Due to the over-sampling conversion, the analog signal obtained at the output of the

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4-bit DAC is mixed with a high frequency noise. Because a 4-bit digital output is used, a first-order RC filter (included in the output stage) is enough to filter this noise.

The volume control is performed in the audio digital filter. Volume control is performed in steps of 1 dB from 0 dB to -30 dB. In mute state, attenuation is higher than 40 dB. The gain is independently programmable on the Left and Right channels, using the AUDLGAIN and AUDRGAIN. A common adjustment of gain is possible at 0dB or +6dB. A digital Left/Right adder and -6dB attenuator allows output of a mono audio path.

The Left and right headset amplifiers provide the stereo signal on terminals **HSOL (U103 Pin G1)** and **HSOR (U103 Pin F1)**. The mono audio signal may be provided on the Right or the Right and Left headset outputs. The mono audio signal may be sum to the speech signal and provided on the Auxiliary, Earphone and/or 8Ohm Speaker outputs. The Audio Stereo/Mono path can be powered down and configure with the TOGBREG, CTRL1, CTRL2, CTRL3, CTRL4, CTRL5 and CTRL6 registers.

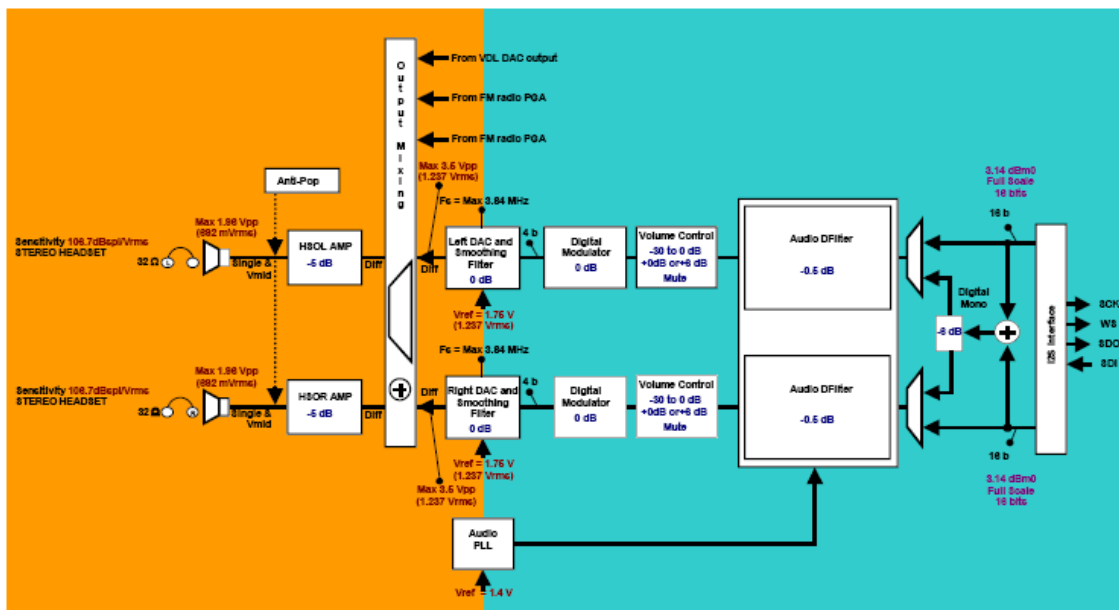


Figure 7: Stereo Audio Path

2.4 Modulation

As illustrated in Figure 8, GMSK 0.3 is generated with Gaussian low-pass filtered bipolar data, applied to a DC coupled FM modulator, set to a modulation index of 0.5.

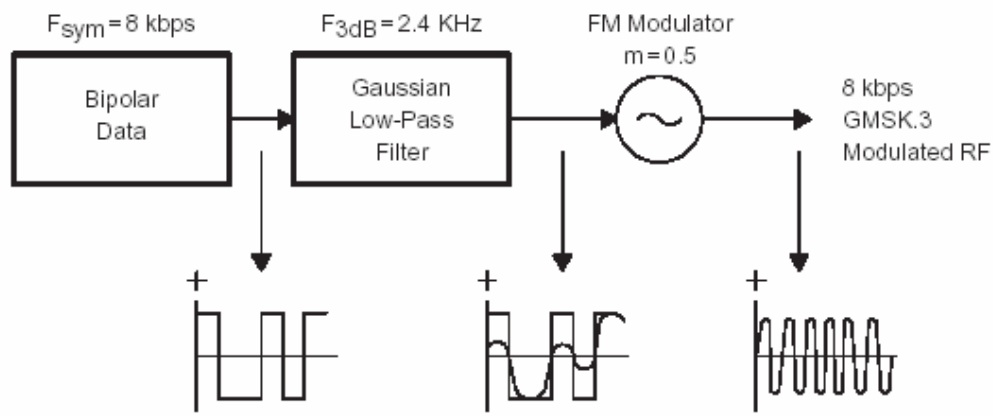


Figure 8: GMSK Modulation

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2.4.1 Transmit Section

As compared with a traditional VCO, TI takes advantage of DCO scheme to design the main TX oscillator in Locosto. DCO stands for “digitally controlled oscillator”, which uses some digital switched capacitances to do frequency tuning, but it should be noticed that the oscillator core is still analog. And Locosto DRP uses ADPLL (all digital phase lock loop) architecture to design a digital synthesizer, and its reference frequency is provided by 26MHz DXCO. The ADPLL output signal will be pre-amplified by a digital controlled pre-PA and then fed into PA module. The TX signals output at **TXLB Locosto Pin F17** (low-band) and **TXHB Locosto Pin G17** (high-band).

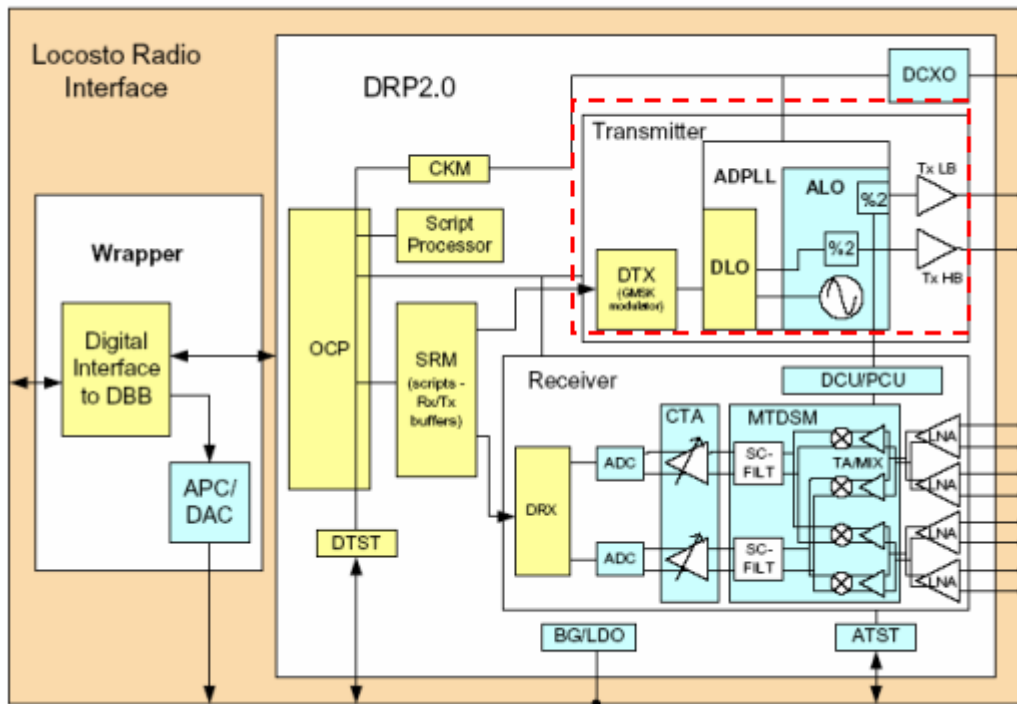


Figure 9: Locosto Transmit Block Diagram

2.4.2 Digitally- Controlled Crystal Oscillator (DCXO)

The DCXO system comprises an external crystal Y101, DCXO core based on Colpitts oscillator, a switching capacitor array, amplitude control loop and a current DAC. It also includes a startup system to control the startup sequence of the bandgap reference and the LDO voltage regulator for the DCXO that is based on a 32 KHz clock. DCXO (Digitally Controlled Crystal Oscillator) is a digitally tunable crystal oscillator centered at 26MHz for GSM applications with the step size of $\sim 0.01\text{ppm}$ of the 26MHz. Both the amplitude and the frequency of oscillation are digitally controllable. Figure 10 shows the top level schematic of DCXO. Major components of DCXO includes a Colpitts oscillator core with negative resistance, 14-bit AFC fine frequency control capacitor DAC, plus an 10-bits coarse frequency control capacitor DAC; an 8-bit programmable current source (IDAC), a peak detector circuit, an ADC, a digital amplitude control loop, and an output buffer.

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consists of separate GSM900 PA and DCS1800 PA blocks, impedance-matching circuitry for 50Ω input and output impedances, and a Power Amplifier Control (**APC SKY77518 Pin 3**) block with an internal current-sense resistor.

The amplified RF output signal feeds out of **SKY77518** from **Pin 19** for high-band and **Pin 17** for low-band and then enters the RF switch **JP201 Pin 1**.

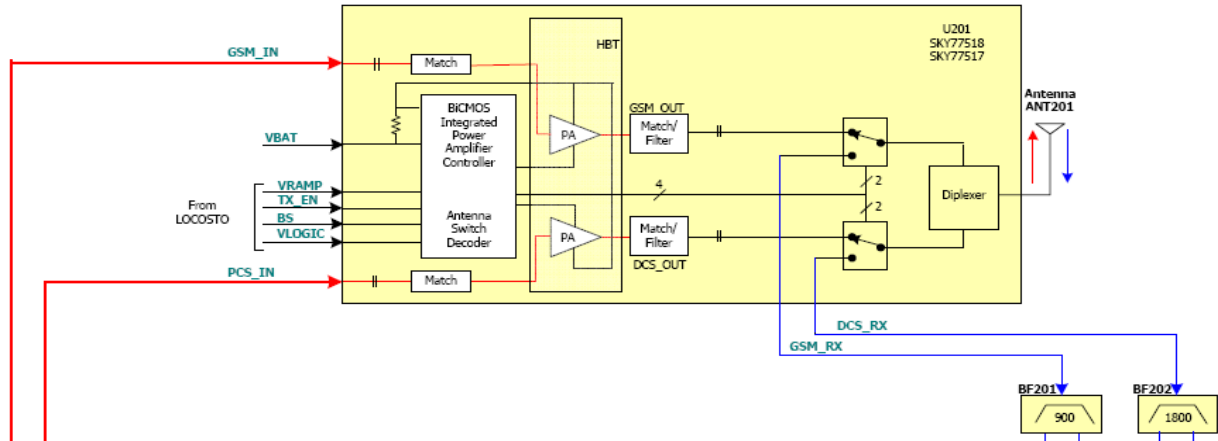


Figure 11: Power Amplifier

2.6 TX PA Power Control in SKY77518 U201

Figure 12 shows the Integrated Power Amplifier Control (iPAC) function along with **SKY77518** proven dual-band PA architecture and BiCMOS current buffering bias scheme. The iPAC circuitry generally operates independently of other device subcircuits and serves to make the RF output power a predictable function of the **APC SKY77518 Pin 3** (V_{APC}) control voltage over variations in supply, temperature, and process. Top-level performance specifications, with exception of those directly associated with power control (or the range of **APC** control voltage), are not altered by placing the device into internal closed loop operation with the **PAENA** (PAC Enable) signal. Thus, the iPAC function of the **SKY77518** can be analyzed separately from the general power amplifier performance.

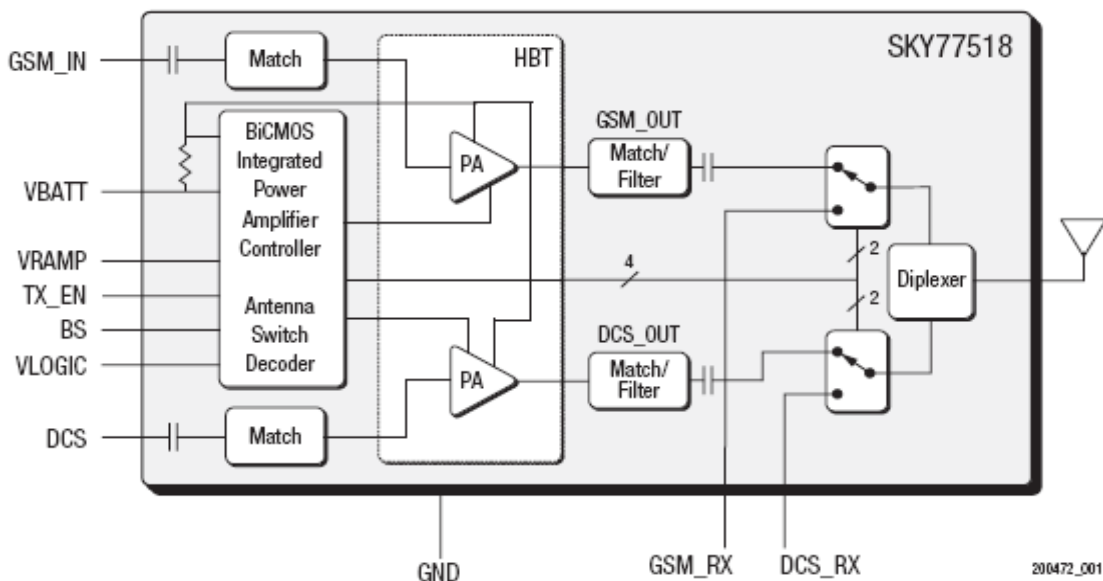


Figure 12: Skyworks 77518/77517 Function Block Diagram

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3 Triton-Lite Monitoring ADC(MADC)

The Monitoring ADC (MADC) consists of a 10bit analog to digital converter ADC combined with 9 input analog multiplexer.

| Chan nel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|-------------|----------|--------------|-----------------|----------|----------|----------|----------|----------|----------|
| Type | External | External | External | Internal | Internal | Internal | Internal | Internal | Internal |
| Name | ADCIN3 | BT ADCIN4 | BTEMP ADCIN5 | USBVBUS | VBKP | ICHG | VCHG | VBAT | HOTDIE |

- Six internal analog values:
 - Die temperature sensing: HOTDIE
 - Battery voltage (**VBAT**)
 - Battery charger voltage (**VCHG**)
 - Current charger (current-to-voltage (I-to-V) converter) (**ICHG**)
 - Backup battery voltage (**VBKP**)
 - USB VBUS voltage (**USBVBUS**)
- Five external analog values:
 - ADIN3: No use
 - ADIN4: No use
 - ADIN5: **ADCIN5** (Triton_Lite Pin F8) for monitor the battery temperature.

4 Voice Serial Port (VSP)

The voice serial port (VSP) is bi—directional (TX/RX) configurable serial port. It consists four terminals:

- VSP_CLK: Clock signal
- VSP_VDR: Data receive
- VSP_VDX: Data transmit
- VSP_VFS: Frame synchronization signal

The format is 16bit data packet with a frame synchronization.

5 Stereo Audio Serial Port (I2S)

LBI Triton supports I2S audio interface master mode. It consist four terminals.

- I2S_WS: Word select
- I2S_SCK: Continuous Serial Clock
- I2S_SDR: Serial data to receive
- I2S_SDX: Serial data to transmit

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6 General purposes I/O (GPIO)

The general purpose interface of the Locosto device combines three general purpose input/output (GPIO) banks: GPIO1,GPIO2 and GPIO3 .

Each GPIO module provides 16 general purpose pins with input and output capabilities. Therefore, the general purpose interface supports up to 48 (3X16) pins.

| W388 GPIO (General Purpose IO) definition | | | |
|---|----------|------------------------------|--|
| Pin No. | GPIO No. | Software select mode | Description |
| M6 | IO_00 | CAM_D1 | CAM_D1 for SW DSC |
| K8 | IO_01 | In:Pull_OFF | Detect HW_ID:EU/US Band type Configuration H: GSM900/1800 L: GSM850/1900 |
| T3 | IO_02 | In: interrupt (pull: off) | T Flash detect (T_DET) ("L": T Flash inserted) |
| T10 | IO_03 | USB Boot | USB boot |
| R9 | IO_04 | CDI | I2S CODEC serial data input interface |
| N9 | IO_05 | TSPACT8 | Triton's ADC control signal (STARTADC) |
| F3 | IO_06 | ADD21 | External memory interface (A21) |
| G6 | IO_07 | CAM_D2 | CAM_D2 for SW DSC |
| F10 | IO_08 | KBR4 | Keyboard matrix (KBR4) |
| B12 | IO_09 | KBC4 | Keyboard matrix (KBC4) |
| C11 | IO_10 | In: Pull_Off | RF_CONN_DET (RF cable attached: "H", no RF cable: "L") |
| D10 | IO_11 | Out: low(Pull_OFF) | SIM enable (nSIM_EN) ("L": SIM enable, "H": SIM disable) |
| B11 | IO_12 | In:Pull_OFF | LCD_ID:Toppoly or 2nd source (L:Toppoly ; H: 2nd source) |
| E10 | IO_13 | LCD_nCS0 | LCD controller chip select (LCD_nCS0) |
| B10 | IO_14 | Out : High | LCD_RDZ |
| F9 | IO_15 | LCD_RnW | LCD read/write (LCD_WRZ) |
| D9 | IO_16 | LCD_RS | Data & command selection (LCD_RS) ("H": data on address bus, "L": command on address bus) |
| B9 | IO_17 | Dithering(Out:low/Pull off) | Dithering(for sovling Phase Error) |
| A6 | IO_18 | CAM_PWDN(Out:high/Pull high) | CAM_PWDN for SW DSC |
| F8 | IO_19 | CAM_HS | CAM_HS for SW DSC |
| E7 | IO_20 | CAM_D3 | CAM_D3 for SW DSC |
| A5 | IO_21 | CAM_LCLK | CAM_LCLK for SW DS |
| C6 | IO_22 | CAM_XCLK | CAM_XCLK for SW DS |
| G9 | IO_23 | SPI_CLK | SPI_CLK |
| F7 | IO_24 | SPI_SOMI | SPI_SOMI |
| C5 | IO_25 | SPI_SIMO | SPI_SIMO |
| E6 | IO_26 | Out: low(Pull_OFF) | Keypad backlight switch (KEY_BL) ("H": LED on; "L": LED off) |
| G8 | IO_27 | SPI_EN2(Out:high/Pull off) | SPI_EN2 |
| C4 | IO_28 | CAM_D7 | CAM_D7 for SW DSC |
| G7 | IO_29 | CAM_D6 | CAM_D6 for SW DSC |
| B3 | IO_30 | CAM_D5 | CAM_D5 for SW DSC |

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| | | | |
|----|-------|---|--|
| C3 | IO_31 | In: interrupt (pull: down) | FM interreup(FM_INT) (H: No action;L: Interrupt occur) |
| F6 | IO_32 | 1. In: Pull off (Check HW ID) 2. Out : Low | 1.HW_ID:Harvey vga or Wildwood vga (H:Wildwood vga ; L: Harvey vga) 2.Re-send (HS attached:High ; no HS: low) |
| H8 | IO_33 | Out: low(Pull_OFF) | FM radio tuner reset (FM_nRESET) ("H": release reset, "L": insert reset) |
| C2 | IO_34 | Out: low(Pull_OFF) | LCM backlight driver enable (LCMBL_EN) ("H":backlight ON; "L":backlight OFF) |
| F5 | IO_35 | Out: low | Audio amplifier select (AUDAMP_SD) ("H": enable; "L": disable) |
| D2 | IO_36 | Interrupt (Pull_Off) | Detect the send_end key function (send_end) ("L": press key) |
| H7 | IO_37 | ADD23 | External memory interface (A23) |
| E3 | IO_38 | nCS0 | PSRAM chip select (nCS0) ("H": disable; "L":enable) |
| G5 | IO_39 | ADD22 | External memory interface (A22) |
| M3 | IO_40 | nRDYM | External memory interface (WAIT) |
| J7 | IO_41 | ADV | External memory interface (ADV) |
| L6 | IO_42 | CKM | External memory interface (CKM) |
| N3 | IO_43 | LCM_FP(In:Pull_off) | LCM Read (LCM_FP) ("L": Read) |
| M5 | IO_44 | CAM_VS(In:Pull_off) | CAM_VS for SW DSC |
| P2 | IO_45 | In: interrupt (pull: off) | Headset detect (HS_DETECT) ("L": headset inserted; "H:headset removed") |
| K7 | IO_46 | Out:low | Flash hardware write protect input (nFWP) ("L": disable write to Flash) |
| N5 | IO_47 | CAM_D0 | CAM_D0 for SW DSC |

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7 TFT LCD Display

This display is a **color TFT Liquid Crystal Display** of glass construction with black pixels on a white background. The display consists of 128(RGB) x 160 pixels with **65K colors** based on software settings.

Driver IC in chip-on-glass(COG) package. This LCM is used two chip LEDs on the Backlight.

- i. Display Type: **LTPS TFT**
- ii. Reflector Type: **Transmissive**
- iii. Pixel Resolution: 128 x RGB x 160
- iv. Pixel Pitch: **0.073mm(W) x 0.219mm(H)**
- v. Number of Colors or Levels of Grayscale: **65K/8** based on software setting
- vi. Active Area: **28.032mm(W) x 35.04mm(H)**
- vii. Viewable Area: **30.032mm(W) x 37.04mm(H)**
- viii. Overall LCD Thickness: **2.75 mm**
- ix. Glass Dimensions: Top Glass:38.74 x 31.64 x 0.5, Bottom Glass:41.96 x 31.64 x 0.5
- x. Operating Temperature Range: - 20°C to + 70°C without loss of function.
- xi. Storage Temperature Range: - 40°C to + 85°C without loss of function.
- xii. Outline Dimension (WxHxT) : **36.7mm(W) x 47.4mm(H) x 2.75 mm**

The TFT LCD display is controlled by the Parallel interface. shows the pin connections between TFT LCD. And the functions of those pins are described as the following:

| Pin number | Pin description | Notes |
|------------|-----------------|-------------------------------|
| 1 | GND | Ground |
| 2 | TE | Tearing Effect Output |
| 3 | /CS | Chip Select input |
| 4 | /RD | Read enable |
| 5 | D7 | Data bus7 |
| 6 | D5 | Data bus5 |
| 7 | D3 | Data bus3 |
| 8 | D1 | Data bus1 |
| 9 | GND | Ground |
| 10 | A0(D/C) | Data/Command select input pin |
| 11 | GND | Ground |
| 12 | LED+ | Anode of LED1,LED2 |
| 13 | /WR | Write enable |
| 14 | D0 | Data bus0 |
| 15 | D2 | Data bus2 |
| 16 | D4 | Data bus4 |
| 17 | D6 | Data bus6 |
| 18 | VSS | Ground |
| 19 | /Reset | Reset |
| 20 | VDDIO | I/O supply 1.8V |
| 21 | VCI | DC-DC Supply 2.8V |
| 22 | ID | ID Pin(Connect to Ground) |

7.1 Display Backlights

The Display backlights are provided by the control signal **LCMBL_EN Locosto Pin C2**. After **LCMBL_EN Locosto Pin C2** control signal turned on, **Charge Pump U401** will charge the flying capacitor (**C412**) to supply 5V for single LED in LCM. On another side, when **KEY_BL Locosto Pin E6** control signal is high, the keypad light will be turned on.

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8 Camera Module

The camera module (**CCS-6003**) is a sensor on-board 300Kpixel camera and lens module designed for mobile application.

CCS-6003 can be programmed to provide image output in various fully processed and Automatic image function include AEC, AGC, AWB... and image quality control such as color saturation, hue, gamma, edge enhancement functions. Also the Figure 14 has shown the pin connections of camera module. The functions of those pins between the camera module and **Locosto** are described as the following:

CAM_D0~D7 – YUV/RGB Video Output, total are 8 bits.

SCL– SCCB serial interface clock input

SDA – SCCB serial interface data input and output

CAM_XCLK – System clock input

CAM_LCLK – Pixel clock output

CAM_HS – Horizontal synchronization output

CAM_VS – Vertical synchronization output

CAM_PWDN – Power Down Mode Selection, 0: Normal mode, 1: power down mode

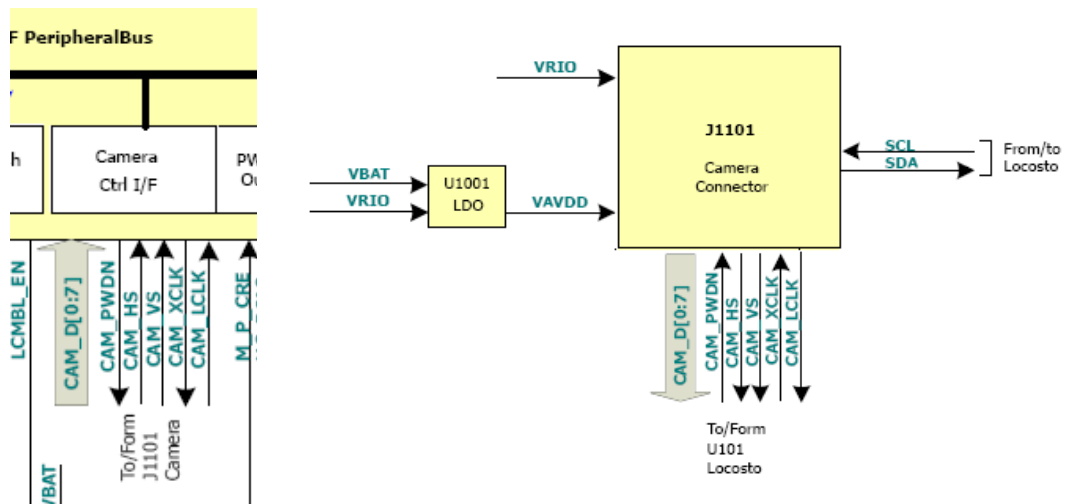


Figure 13: Camera interface

9 32kHz RTC

The Real-time Clock Interface is part of the **Triton U103** in use with the crystal **Y102**. The clock signal is running on 32kHz as reference for the clock module and as deep sleep clock.

10 Universal Subscriber Identity Card (USIM)

To allow the use of both 1.8V and 3V SIM card types, there is a SIM level-shifter module in the [Locosto U101](#). The SIM card digital interface ensures the translation of logic levels between the [Locosto U101](#) device and the SIM card [J702](#) for the transmission of four different signals:

USIM_IO – SIM interface data in out line

USIM_CLK – SIM data Clock

USIM_RST – SIM Reset

VRSIM – is SIM card power that generates from Triton LDO.

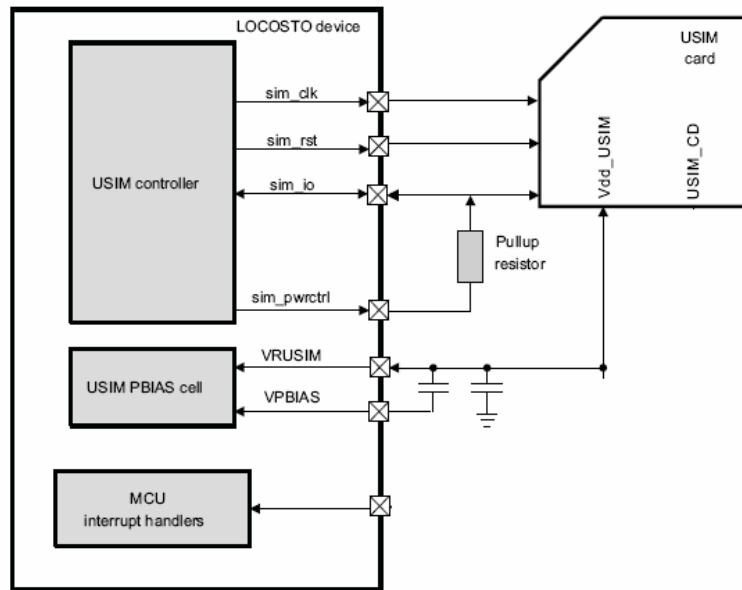


Figure 14: SIM interface

11 Keypad

The keyboard is connected to the chip using:

ROW0-ROW4 (**KBR[0:5]**) input pins for row lines

COL0-COL4 (**KBC[0:5]**) output pins for column lines

If a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted.

To allow key press detection, all input pins (**KBR[0:5]**) are pulled up to VCC and all output pins (**KBC[0:5]**) are driving a low level. Any action on a button will generate an interrupt to the microcontroller which will, as answer, scan the column lines with the sequence describe below.

This sequence is written to allow detection of simultaneous press actions on several key buttons.

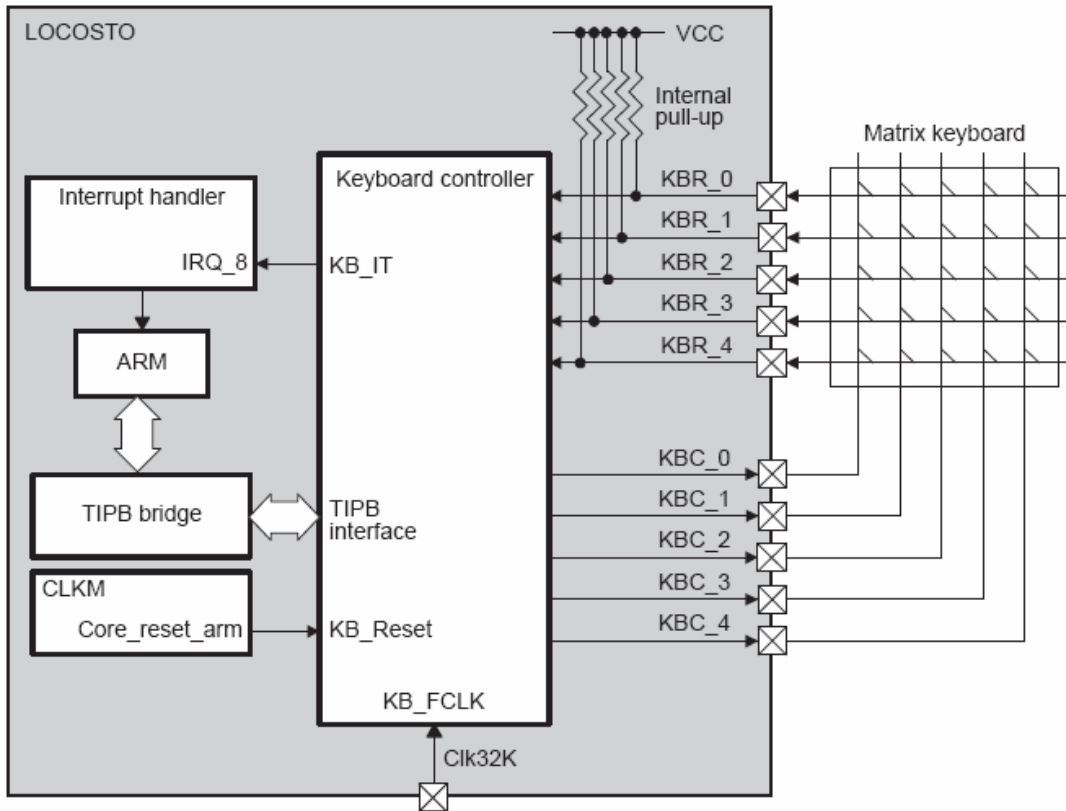


Figure 15: Keyboard controller overview

11.1 Keypad Matrix

The keypad matrix is as follow:

| Function | Key | Col 0 | Col 1 | Col 2 | Col 3 | Col 4 | Row 0 | Row1 | Row 2 | Row 3 | Row 4 |
|-----------|-------|-------|-------|-------|-------|-------|-------|------|-------|-------|-------|
| 1 | S1017 | | | | | V | V | | | | |
| 2 | S1006 | | V | | | | V | | | | |
| 3 | S1005 | V | | | | | | | | | V |
| SEND | S1004 | V | | | | | | | V | | |
| 4 | S1003 | V | | | | | | V | | | |
| 5 | S1015 | | | V | | | | V | | | |
| 6 | S1008 | | V | | | | | | V | | |
| UP | S1002 | V | | | | | V | | | | |
| 7 | S1009 | | V | | | | | | | V | |
| 8 | S1010 | | V | | | | | | | | V |
| 9 | S1012 | | | V | | | | | V | | |
| DOWN | S1007 | | V | | | | | | V | | |
| * | S1018 | | | | | V | | V | | | |
| 0 | S1014 | | | | V | | V | | | | |
| # | S1020 | | | | | V | | | | V | |
| LEFT | S1021 | | | | | V | | | | | V |
| SOFT-L | S1011 | | | V | | | V | | | | |
| MENU | S1019 | | | | | V | | | V | | |
| SOFT-R | S1013 | | | V | | | | | | | V |
| RIGHT | S1016 | | | | V | | | | | V | |
| POWER/END | S30 | | | | | | | | | | V |

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12 Vibrator circuit

Triton U103 Pin U12 is used to control the vibrator level. D701 is used to protect the vibrator. The vibrator's drain current is around 80mA.

13 Memory

The Harvery VGA project uses the stacked combination memory parts that include NOR flash die and PSRAM die. The NOR Flash memory is 256Mbit size and the PSRAM memory is 128Mbit size.

A/D [0:15] – Data/Address Bus

A [16:23] – Address Bus

F1-VCC – Flash digital power.

P-VCC – PSRAM digital power

VCCQ – Flash IO power

CKM – Flash clock

nFADV – Address valid

RnW –Flash/PSRAM memory write enable.

nFOE –Flash/PSRAM memory output enable (Active Low).

FDP – The Flash reset/deep power-down mode control. Usually connect to memory flash pin.

nCS3 – Flash chip select.

nCS0 –PSRAM chip select.

nBHE –PSRAM High Byte enable

nBLE –PSRAM Low Byte enable.

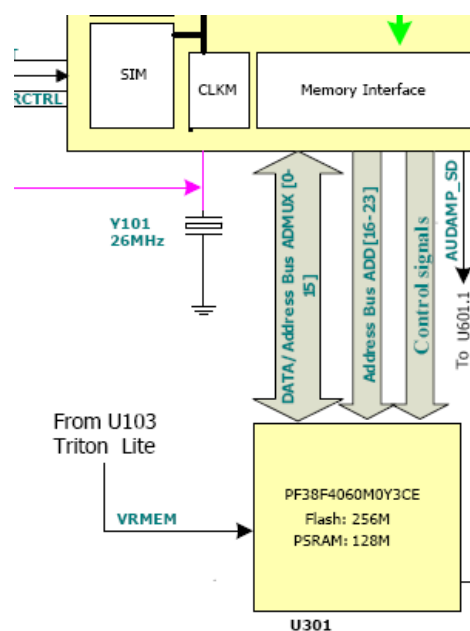


Figure 16: Memory interface

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14 Power

14.1 Low-Dropout Voltage Regulators

The voltage regulation block consists of nine subblocks.

Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators supply power to internal analog and digital circuits, [Locosto U101 \(DSP\)](#) processor, and external memory.

The first LDO ([VRPLL Triton-Lite Pin T12](#)) is a programmable regulator that generates the supply voltage 1.3 V for [Locosto U101](#).

The second LDO ([VRABB Triton-Lite Pin B2](#)) generates the supply voltage 2.8 V for the [Triton-Lite](#) analog parts.

The third LDO ([VRRTC Triton-Lite Pin N17](#)) is a power rail for embedded 32K real time clock using.

The fourth LDO ([VREXTH Triton-Lite Pin I17](#)) is a programmable regulator that generates the supply voltage 2.8 V for external peripheral of [Locosto U101](#).

The fifth LDO ([VREXTL Triton-Lite Pin G17](#)) generates the supply voltage 1.3V for external peripheral of [Locosto U101](#).

The sixth LDO ([VRMMC Triton-Lite Pin T10](#)) is a programmable regulator that generates the supply voltage 2.8V for external MMC device.

The seventh LDO ([VRSIM Triton-Lite Pin A3](#)) is a programmable regulator that generates the supply voltage 2.8V for SIM-card and SIM-card device.

The eighth LDO ([VRIO Triton-Lite Pin J16](#)) is a programmable regulator that generates the supply voltage 1.8V for the I/O of [Locosto U101](#).

The ninth LDO ([VRMEM Triton-Lite Pin U11](#)) is a programmable regulator that generates the supply voltage 1.8V for the external Flash memory.

The [Triton-Lite U103](#) allows three operating modes for each of these voltage regulators:

1. ACTIVE mode during which the regulator is able to deliver its full power.
2. SLEEP mode during which the output voltage is maintained with very low power consumption but with a low current capability (1mA).
3. OFF mode during which the output voltage is not maintained and the power consumption is null.

The regulators rise up in ACTIVE mode only and each of them has a regulation ready signal RSU. In switched-off and backup states of the mobile phone, the voltage regulators will be set to the SLEEP or OFF mode based on the system request. The regulator voltages are decoupled by the low ESR capacitors which connect across the corresponding VCC and ground terminals. Besides noise filtering function, these capacitors also have energy storage function that could offer the delay time for data protection purpose when the main battery is unplugged .

The third LDO ([VRRTC Triton-Lite Pin N17](#)) is a programmable regulator that generates the supply voltages 1.8 V for the real-time clock and the 32kHz oscillator of [Locosto U101 \(DSP\)](#) under all modes.

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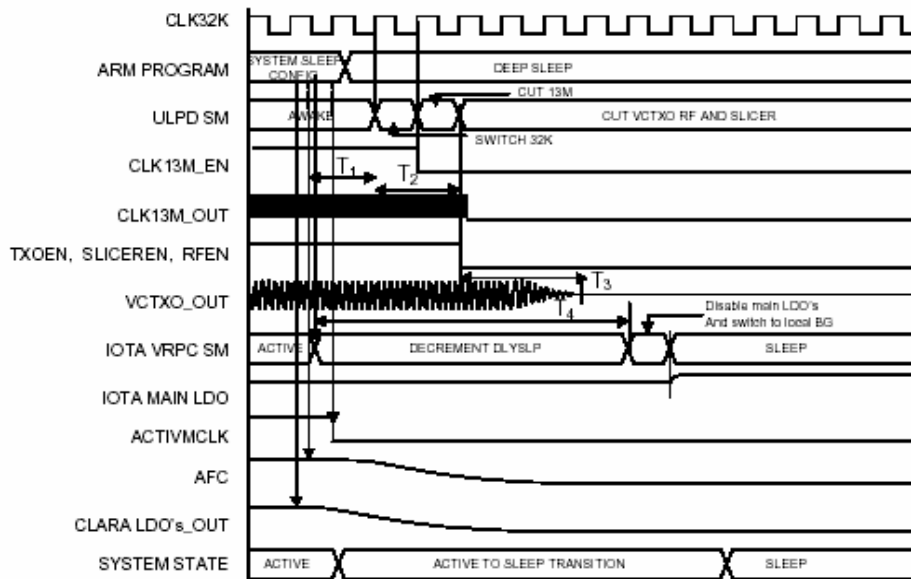
The phone enters power-down mode under one of the following conditions:

1. Press **POWER/END** key
2. Short **PWON TP11** to GND
3. When the low battery voltage is detected by software through **VBATS Pin K8** (software default value is 3.53V).

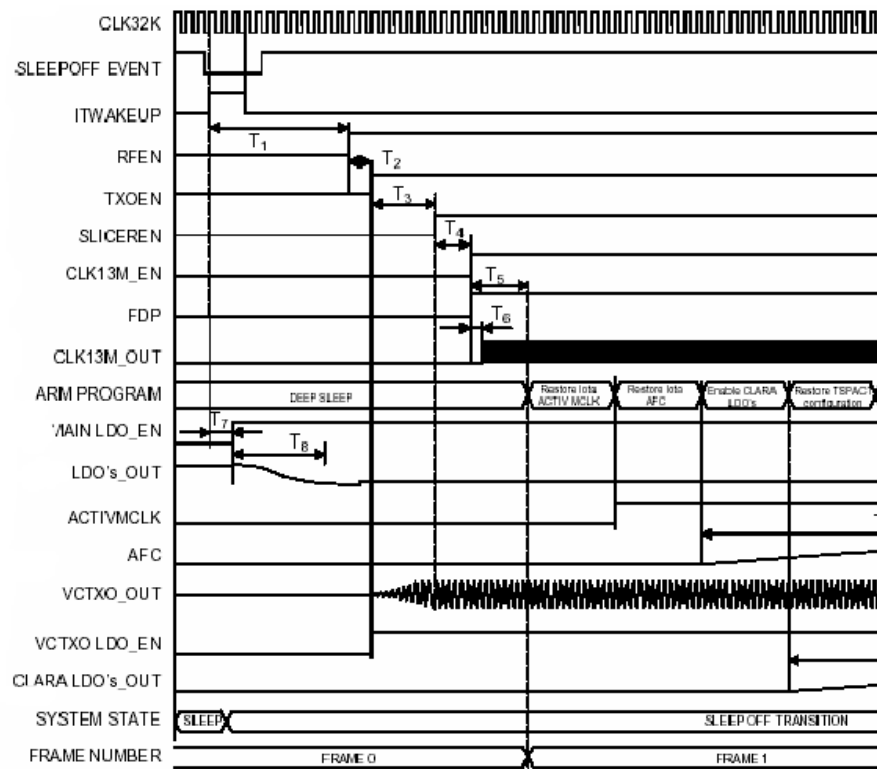
15 Sleep Module

The Sleep Module provides the optimal power savings for **Triton-Lite U103** internal LDOs (VRIO, VRMEM, VRSIM, VRABB, VREXTL, VRPLL) under the idle mode.

15.1 Sleep Up Sequence



15.2 Sleep off Sequence



16 Power Tree

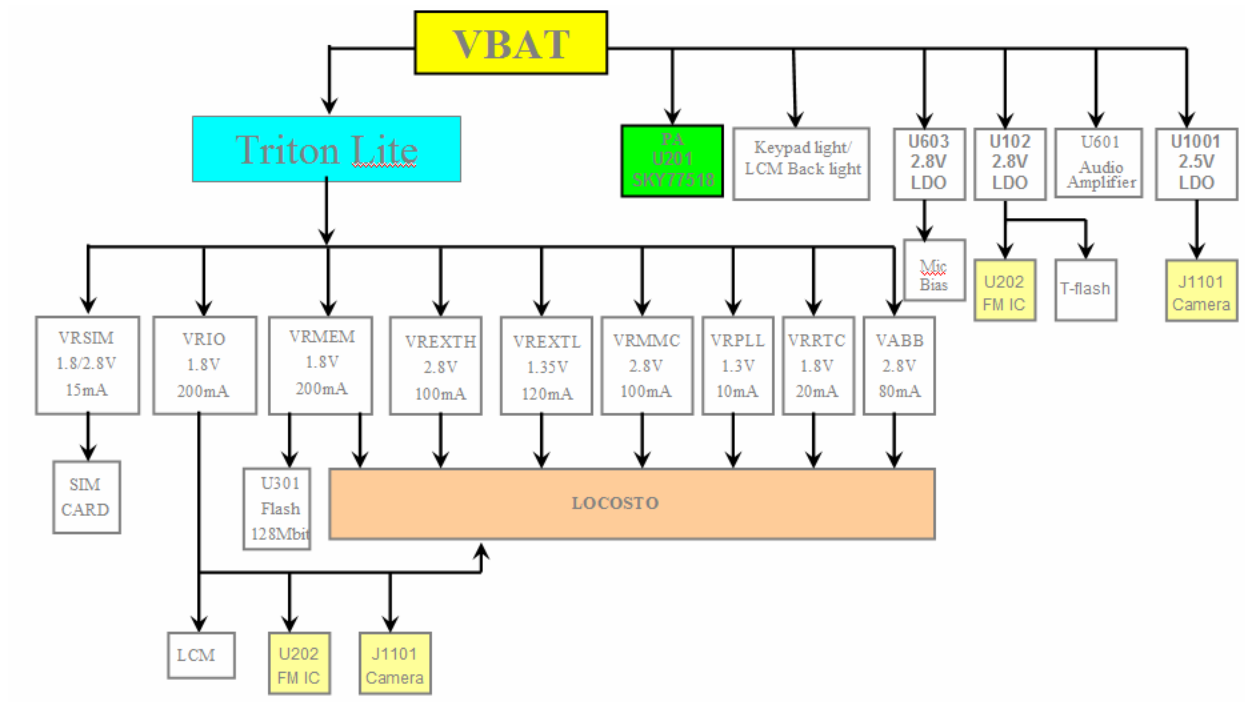


Figure 17: Power Distribution Tree

17 Charging Circuit and External Power

Phone is powered by battery and external charger; however, phone doesn't support the function "accessory plugged-in & battery absent".

17.1 Battery Support

The pin definitions of [Battery connector J703](#) are as follow,

- ◆ Pin 1 – BATT- : (GND)
- ◆ Pin 2 – Therm is used to measure the battery temperature during charging. The system gets the battery temperature under charging via [Triton-Lite U103 Pin F8](#).
- ◆ Pin 3 – DATA : no used.
- ◆ Pin 4 – VBAT+

17.2 Charger Support

When the battery voltage is less than 3.2V, and adapter is inserted, the charging system will enter the 'Pre-CHARGE' mode. The pre-charging current flow through [Triton-Lite](#) pre-charge path and charger IC [U501 \(BQ24314DSJ\)](#). The current limit resistor R505 make the pre-charge current under 100mA.

When a charger is plugged in and [VBUS](#) is less than 6.0V, the [Triton-Lite](#) enables [U502 \(P-MOSFET\)](#) to start charging process until [VBAT](#) is full.

When the battery voltage is less than 3.2V (deep discharge), the Battery Charge Interface (BCI) of [Triton-Lite](#) enters the pre-charge mode (charging current is under 100mA) as soon as the charger is plugged-in. At this moment, software cannot control the charging process until [VBAT](#) is larger than 3.2V, [Triton-Lite](#) and [Locosto](#) wake up and then enter

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the normal charging status. The normal charge mode starts at constant current mode (MAX charging current is 450mA). When the battery voltage reaches 4.15V, charging system enters the constant voltage mode till the charging current is less than 50mA, then the charge process is completed. In addition, when the battery voltage **VBAT** is higher than 4.2V, system will disable **U502 (P-MOSFET)** to stop charging.