

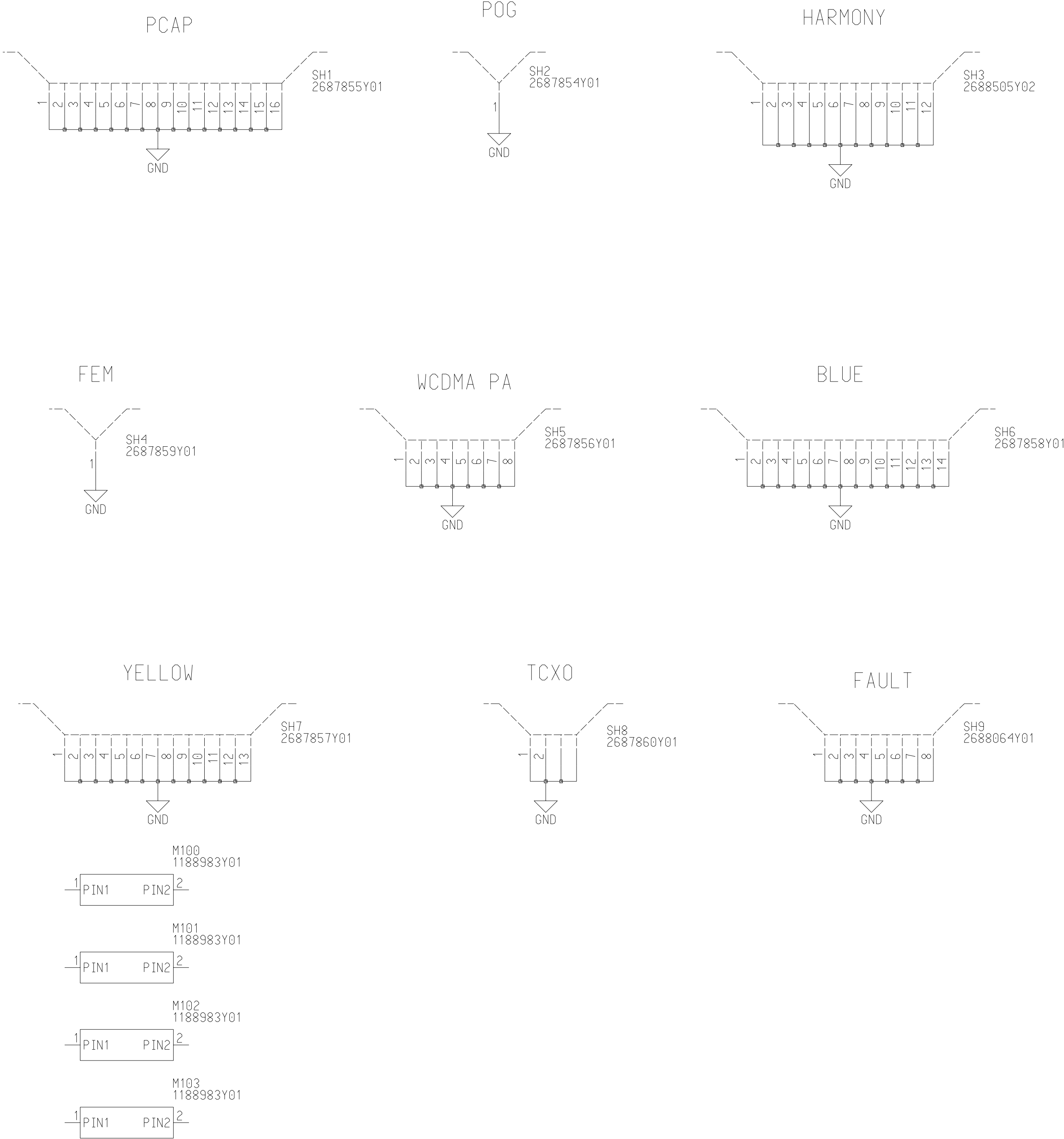
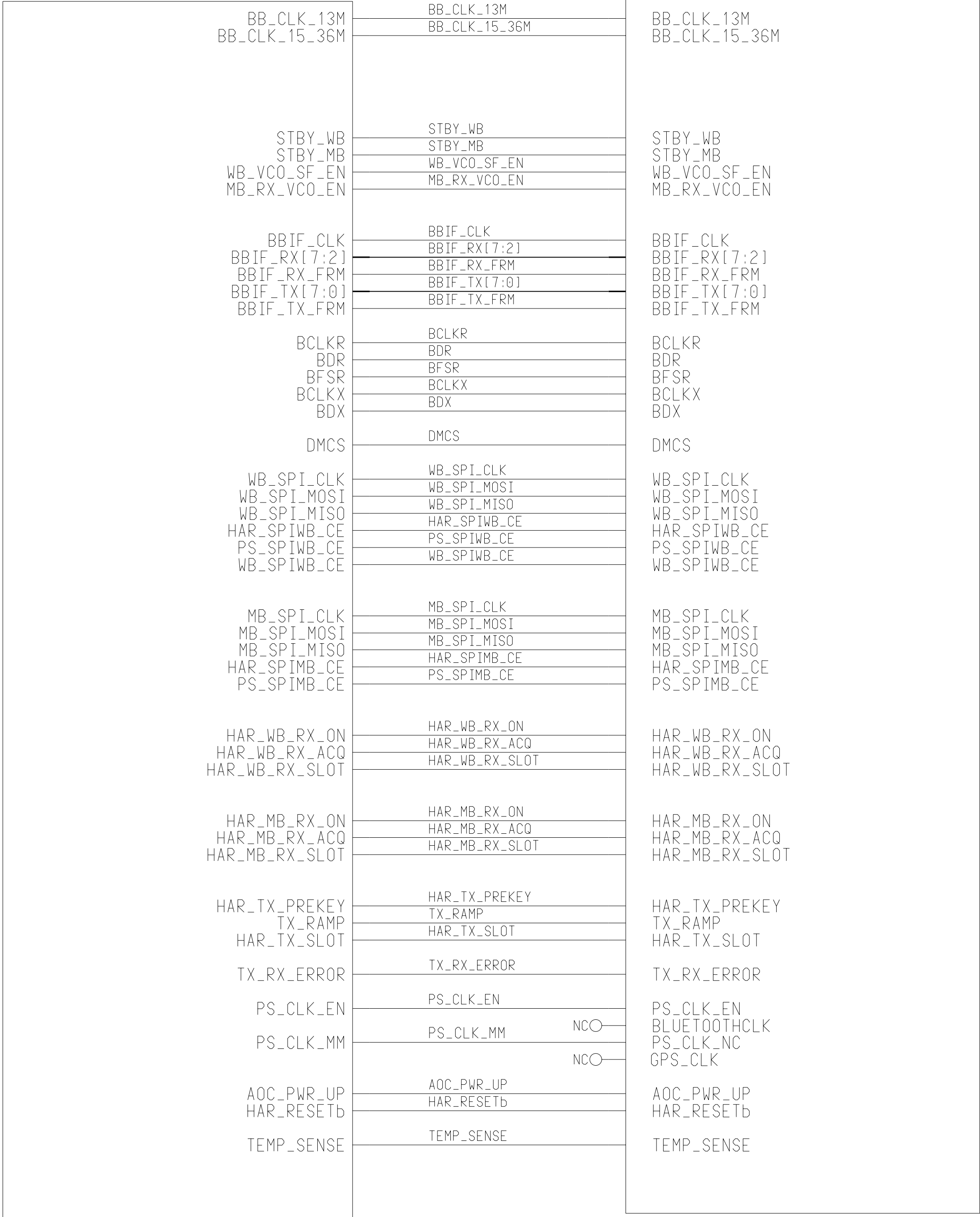
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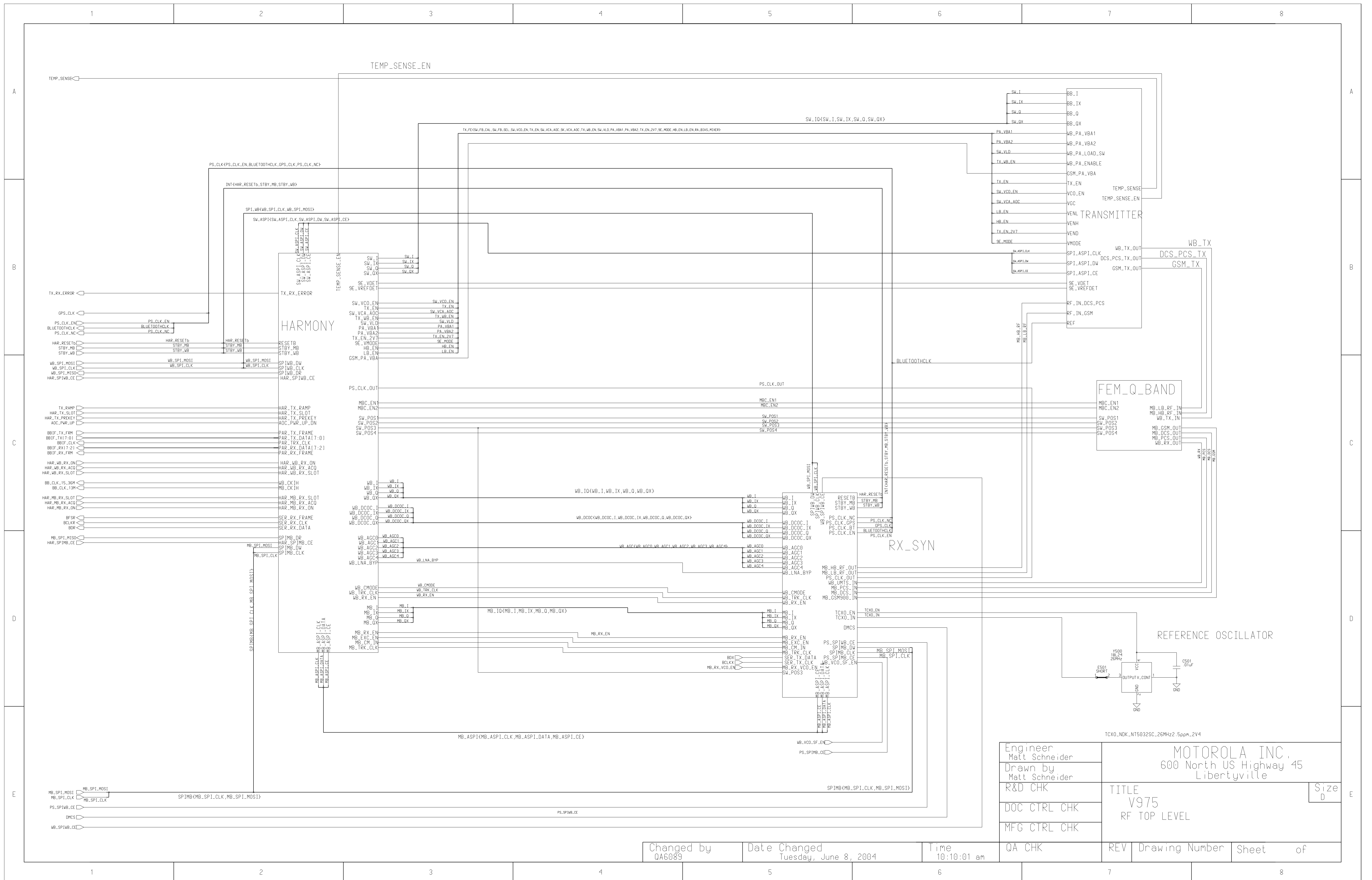


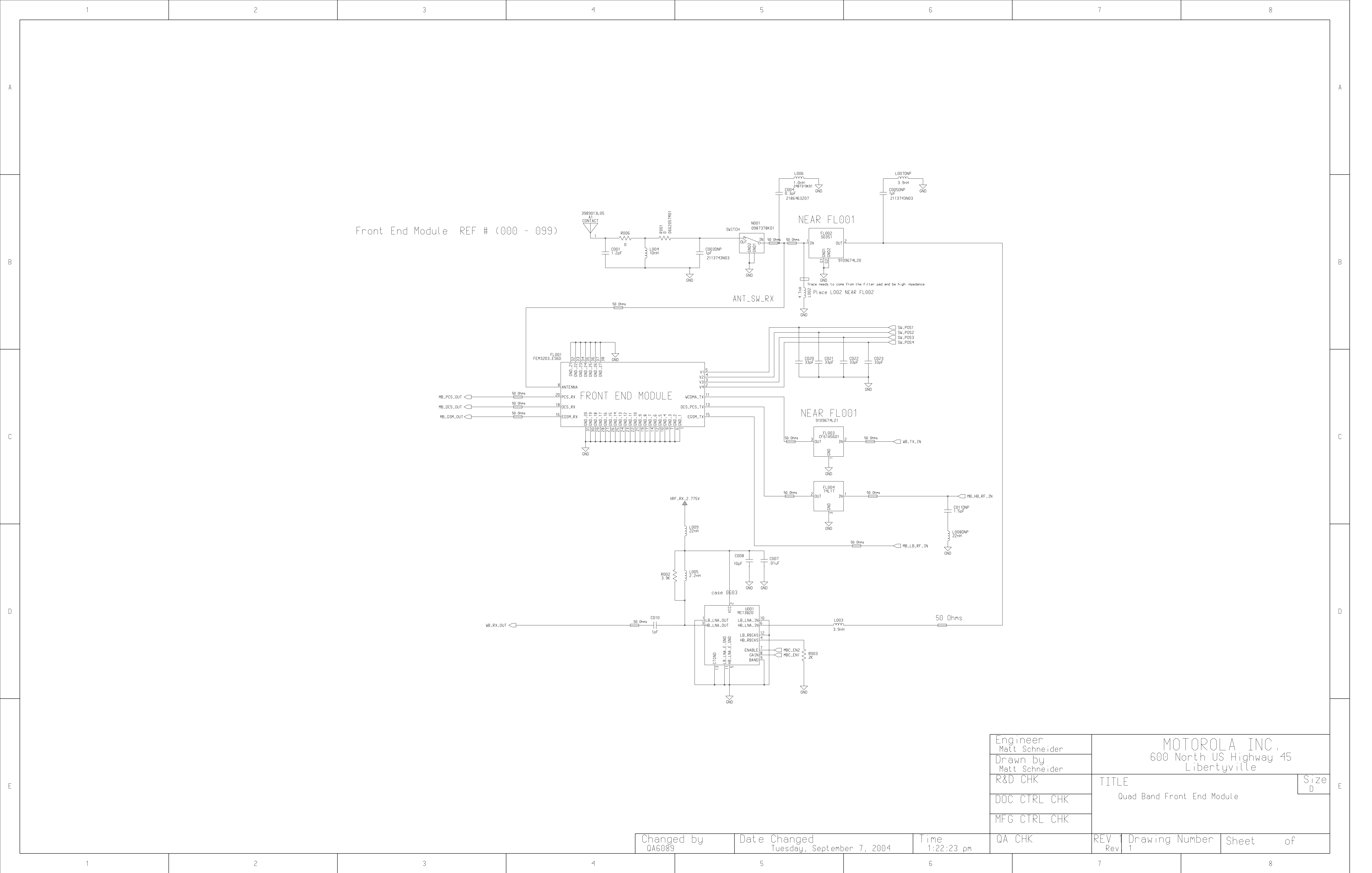
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Drawn by:				
R&D CHK:	REV: 0			Size:
DOC CTRL CHK:	Drawing Number: 8487724Y10			Page:
MFG CTRL CHK:	QA CHK:			Of:
Changed by:	Date:			Time:

BB

RF







Engineer Matt Schneider	MOTOROLA INC. 600 North US Highway 45 Libertyville		
Drawn by Matt Schneider			
R&D CHK	TITLE Quad Band Front End Module		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV Rev 1	Drawing Number	Sheet of

Changed by QA6089	Date Changed Tuesday, September 7, 2004	Time 1:22:23 pm
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TP placeholders for pins with NC

SYNTHESIS CAPACITORS CLOSE TO HARMONY

SUPPLIES INTERCONNECTIONS FAR FROM HARMONY

ALL CAPACITORS CLOSE TO HARMONY

ALL CAPACITORS CLOSE TO HARMONY

HARMONY

U100

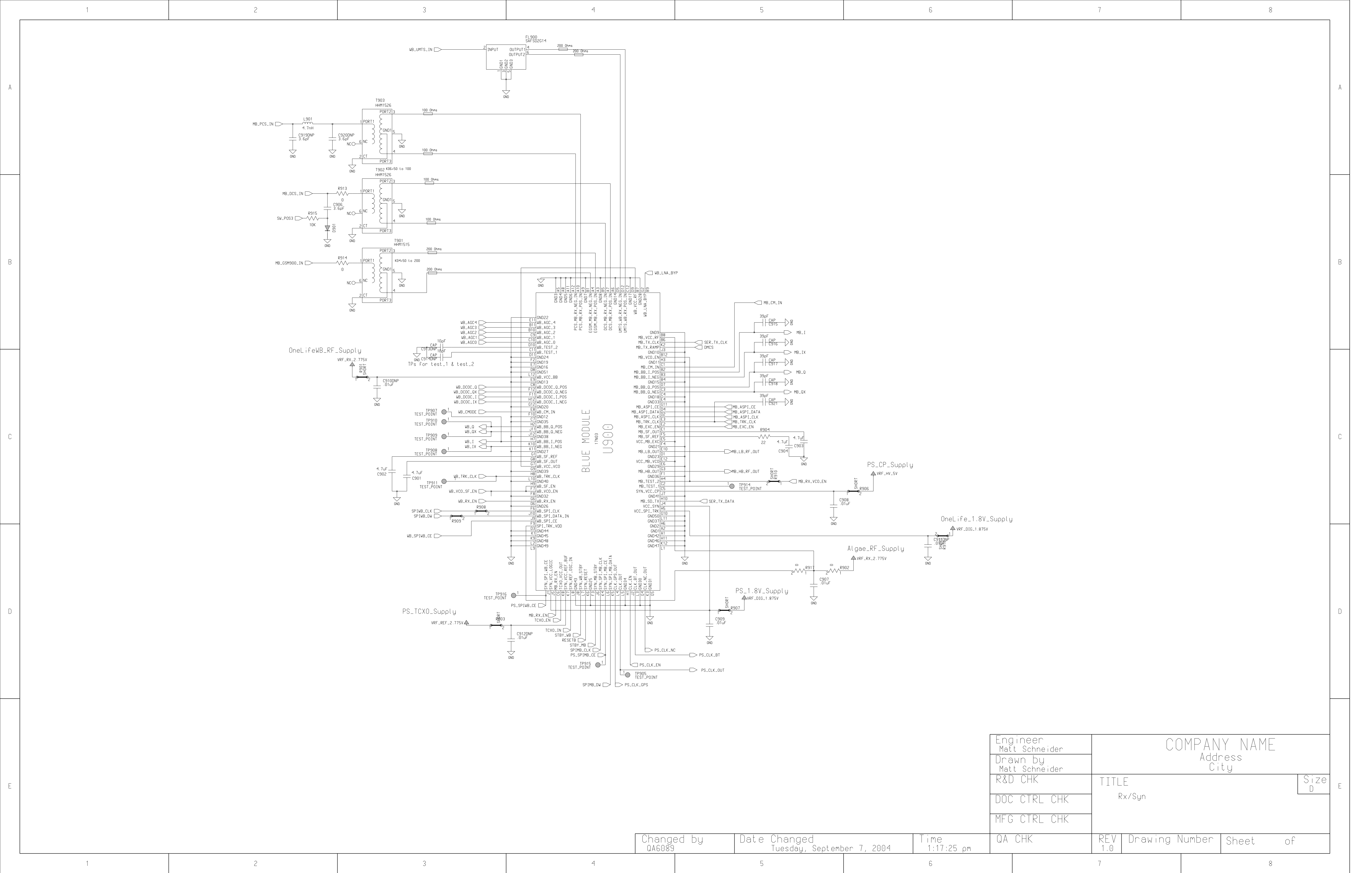
50R23

Engineer Matt Schneider	MOTOROLA INC. 600 North US Highway 45 Libertyville		
Drawn by Matt Schneider			
R&D CHK	TITLE HARMONY		Size D
DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	REV 1	Drawing Number	Sheet of

Changed by
QA6089

Date Changed
Thursday, July 15, 2004

Time
6:38:48 pm

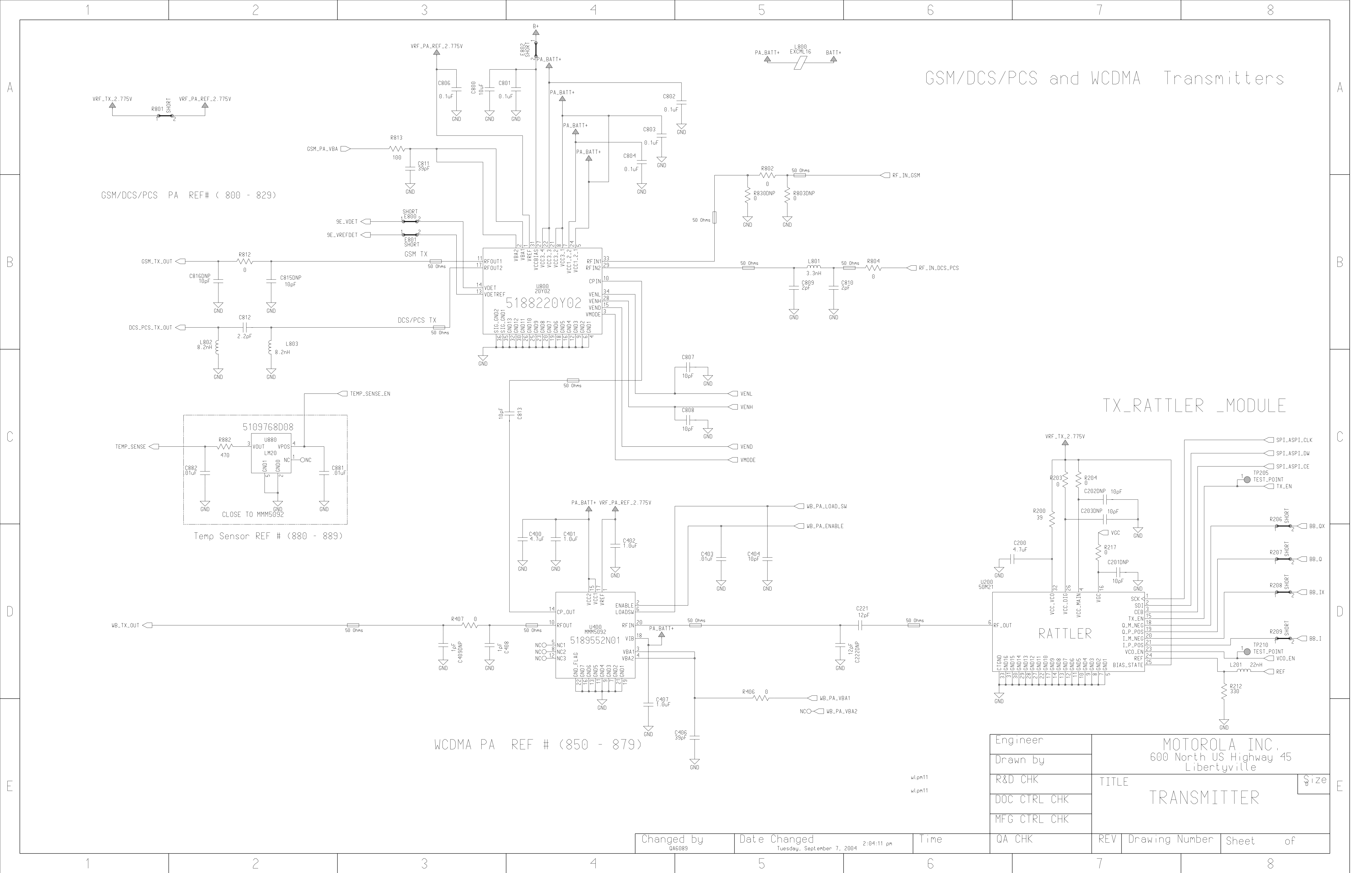


Engineer Matt Schneider	COMPANY NAME Address City		
Drawn by Matt Schneider			
R&D CHK	TITLE Rx/Syn		Size D
DOC CTRL CHK			
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QA CHK	REV 1.0	Drawing Number	Sheet of

Changed by
QA6089

Date Changed
Tuesday, September 7, 2004

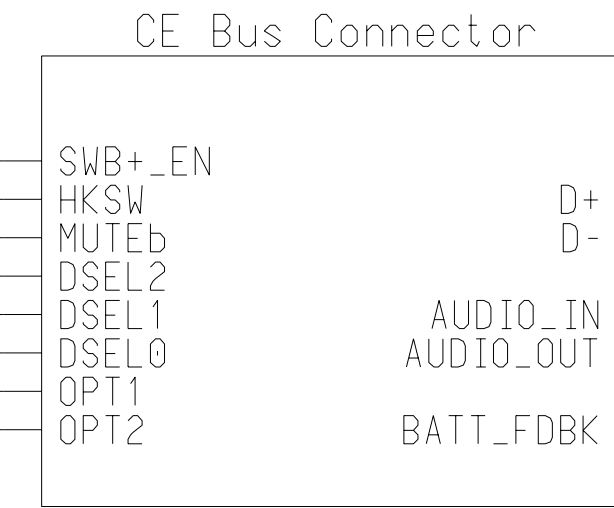
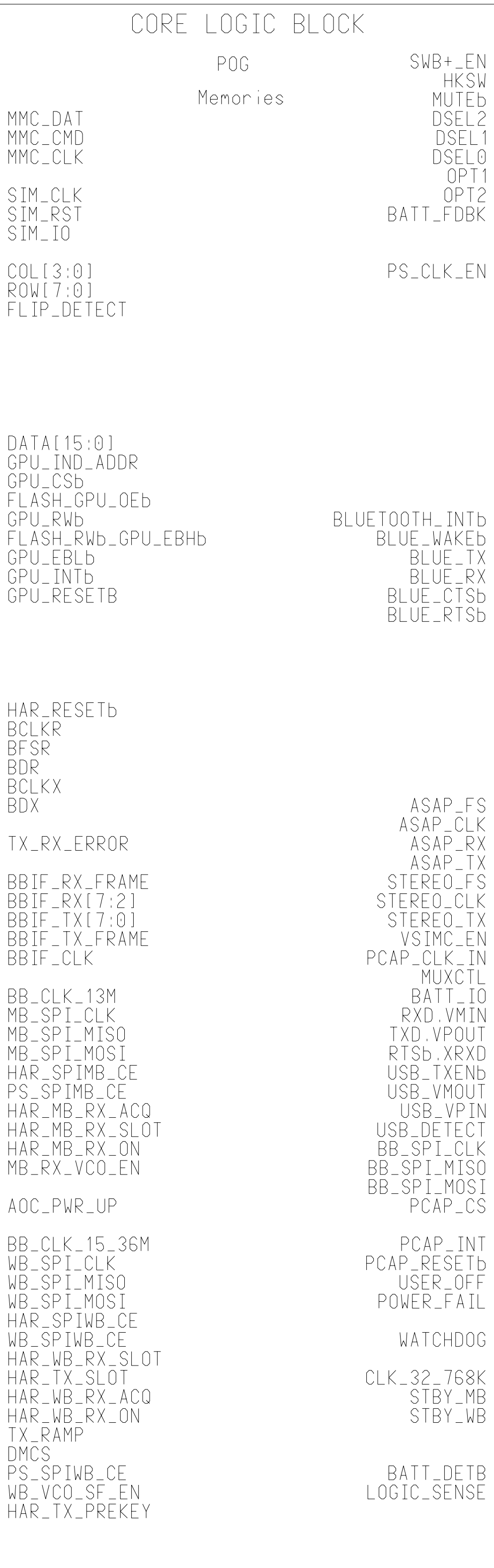
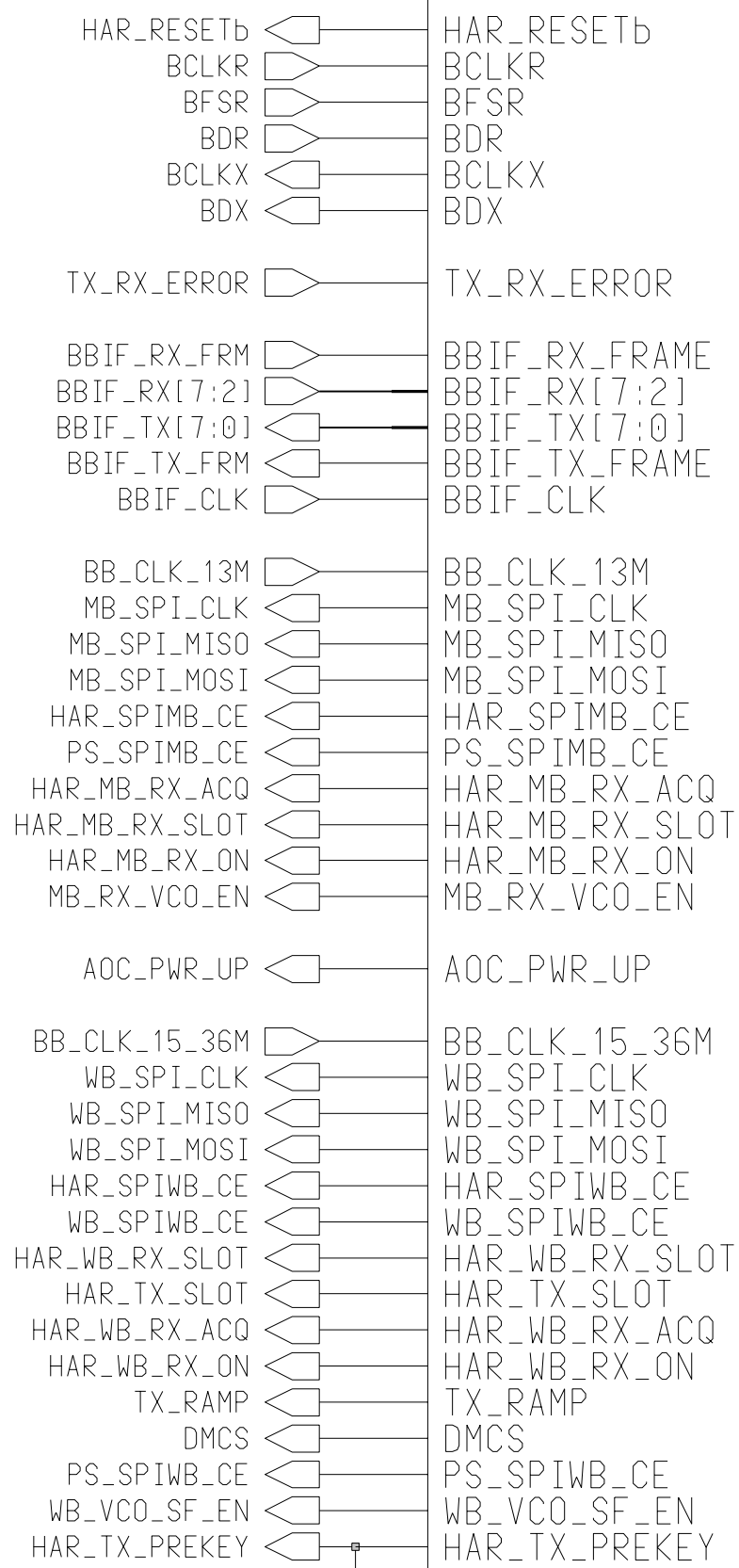
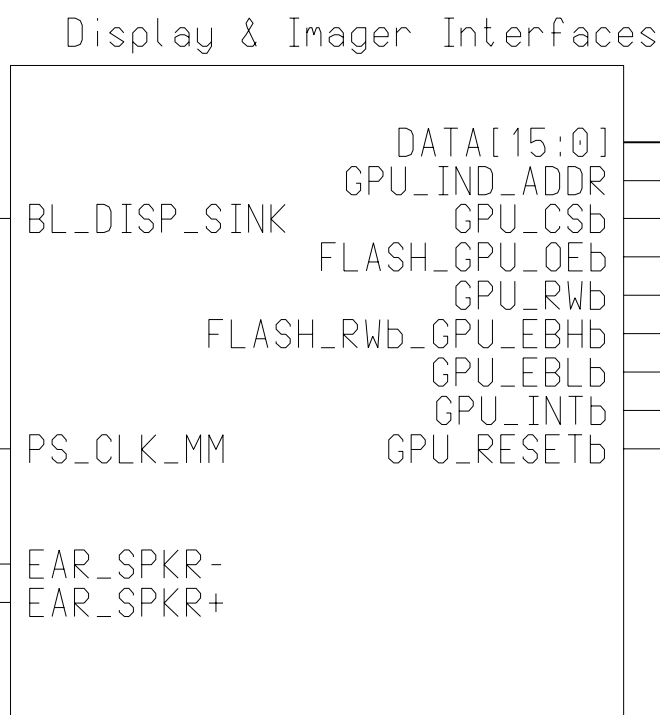
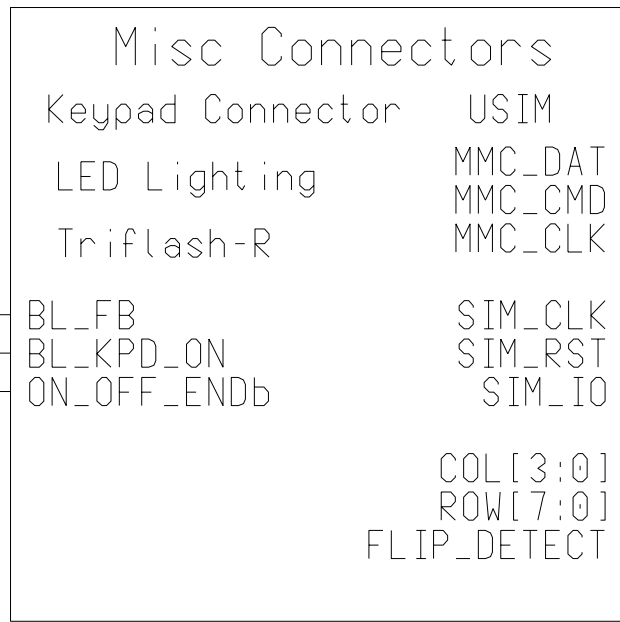
Time
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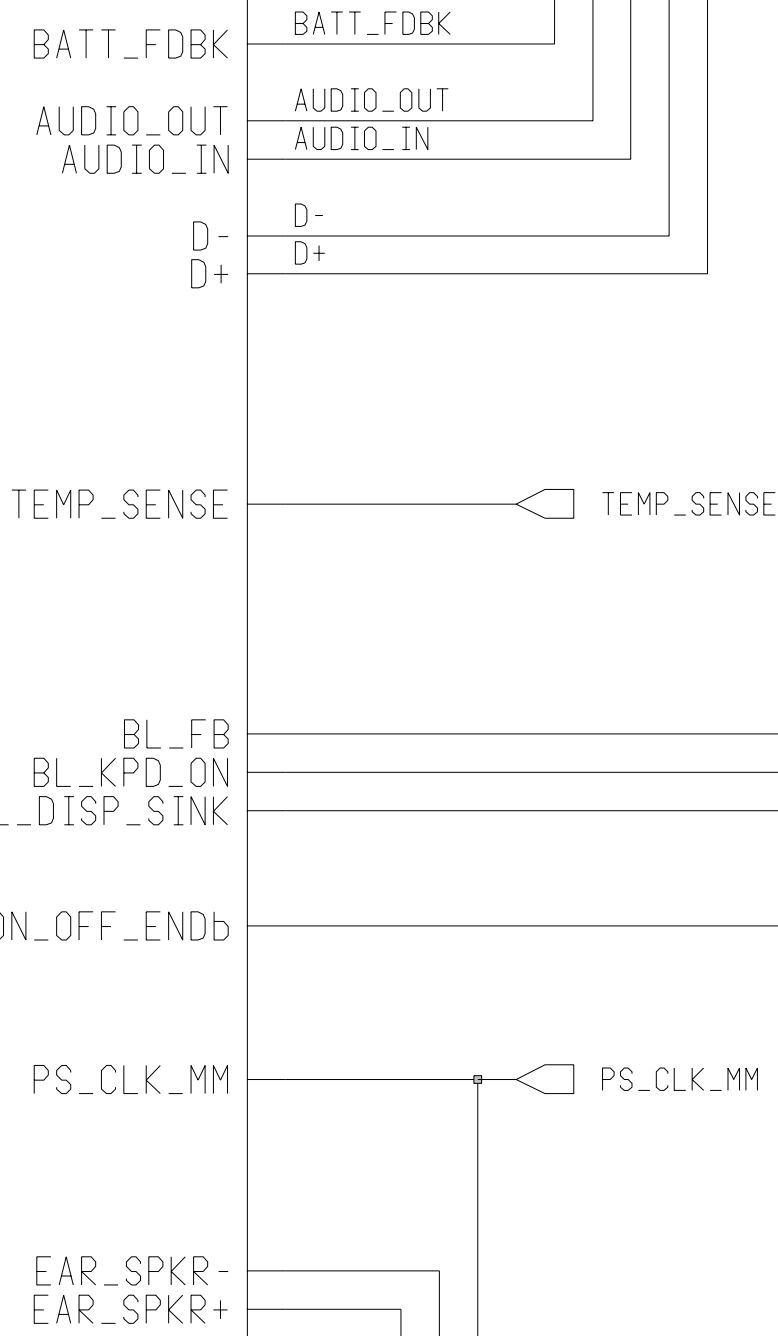
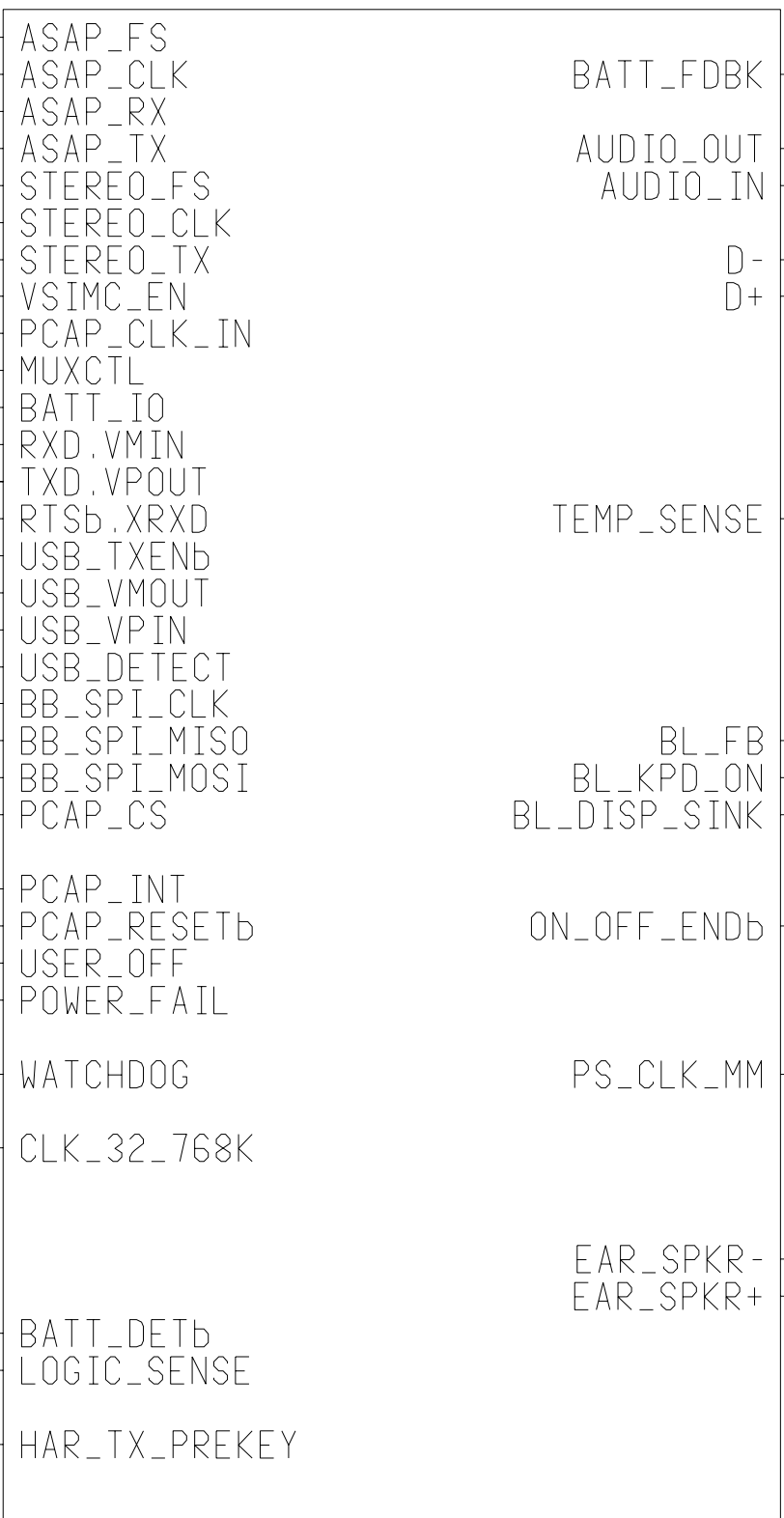
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Engineer:	TITLE: V980 Baseband Top Level				Size:
Drawn by:					
R&D CHK:	REV: 0 Drawing Number: 8487724Y10 Page: Of:				
DOC CTRL CHK:					
MFG CTRL CHK:	Date:				Time:
QA CHK:					
Changed by:					



PCAP2 (Power/Audio)



HAR_TX_PREKEY

EAR_SPKR+

EAR_SPKR-

PS_CLK_MM

BL_DISP_SINK

ON_OFF_ENDb

BL_KPD_ON

BL_FB

1

2

3

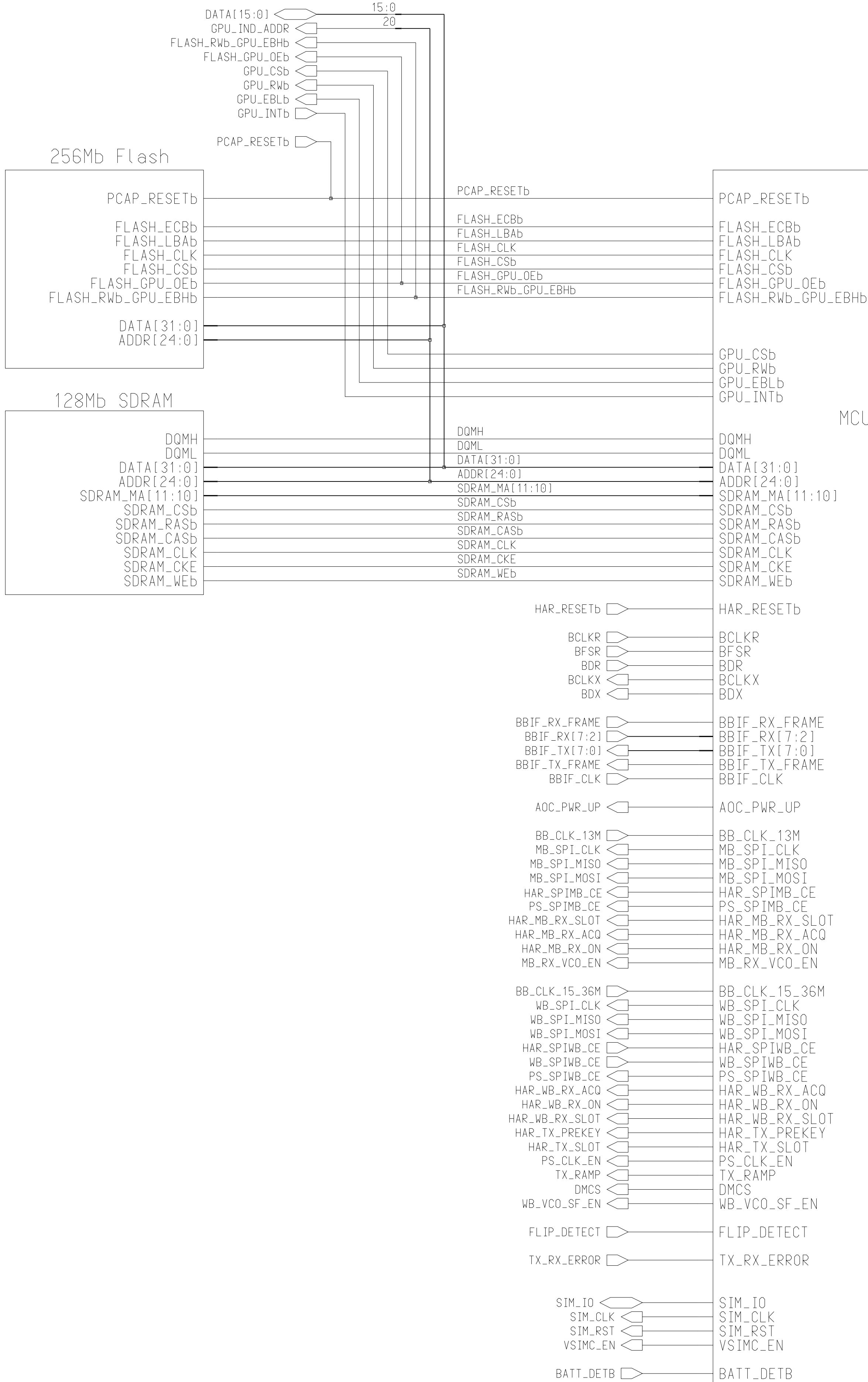
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A

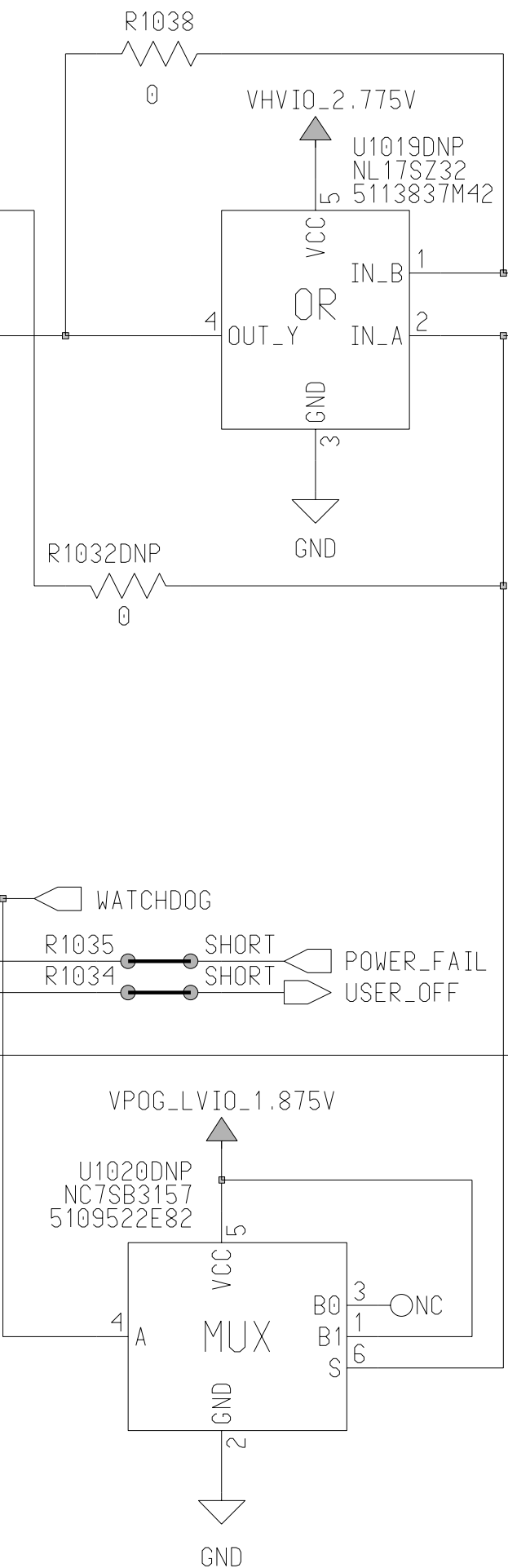
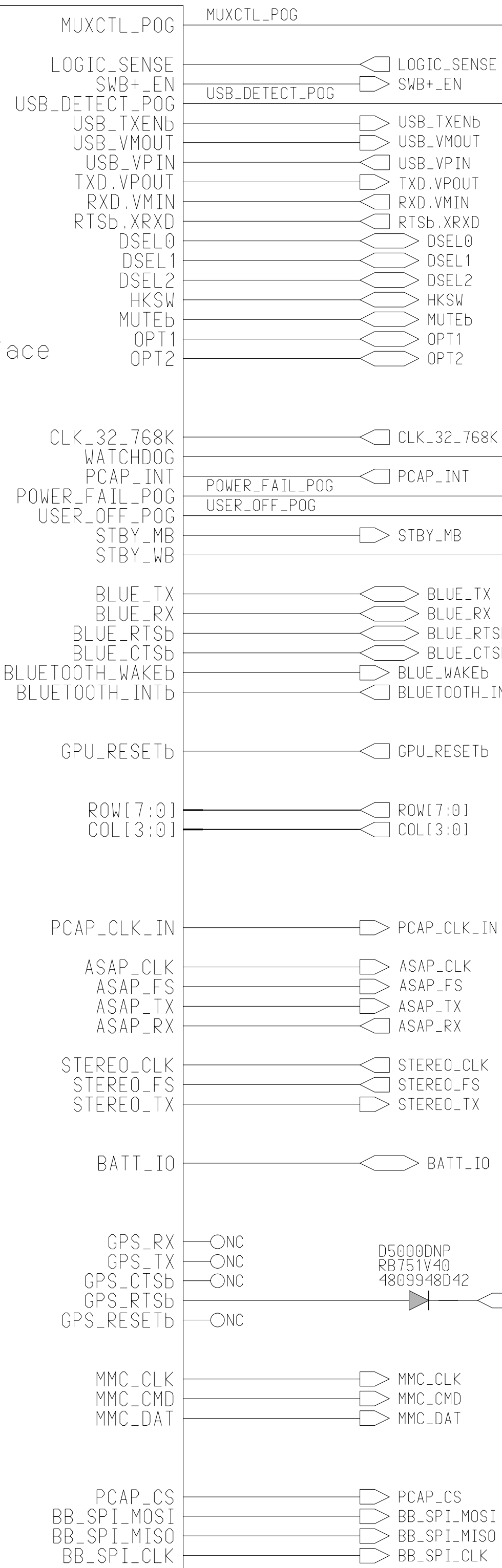
B

C

D



POG Hierarchy Block
4 Sheets
MCU and IPCM Peripheral Interface
Memory & Test Interface
DSP Interface
Power
Wingboard Interface



Engineer:	MOTOROLA INC.		
Drawn by:			
R&D CHK:	TITLE: V980	Size:	
DOC CTRL CHK:	POG & Memories		
MFG CTRL CHK:	REV: 0	Drawing Number: 8487724Y10	Page: Of:
QA CHK:	Date:		Time:
Changed by:			

Product ion
U1019DNP
R1038
R1032DNP
U1020DNP

Development
U1019
R1038DNP
R1032
U1020

Desense Cap
C1000
39pF

MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer :

 **MOTOROLA INC.**

Drawn by:

R&D CHK:

TITLE:	V980	Size:
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DOC CTRL CHK:

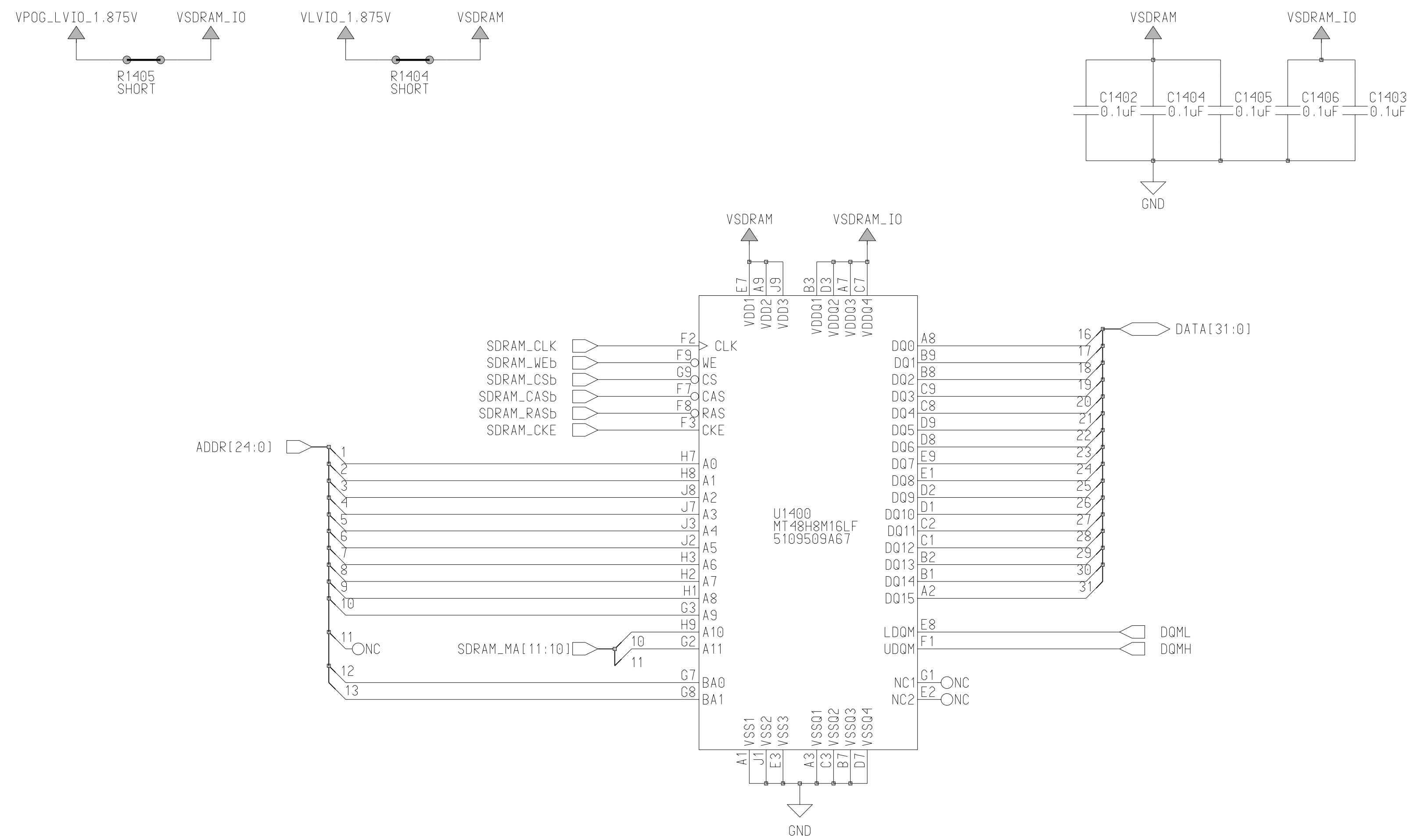
SDRAM Memory

QA CHK:

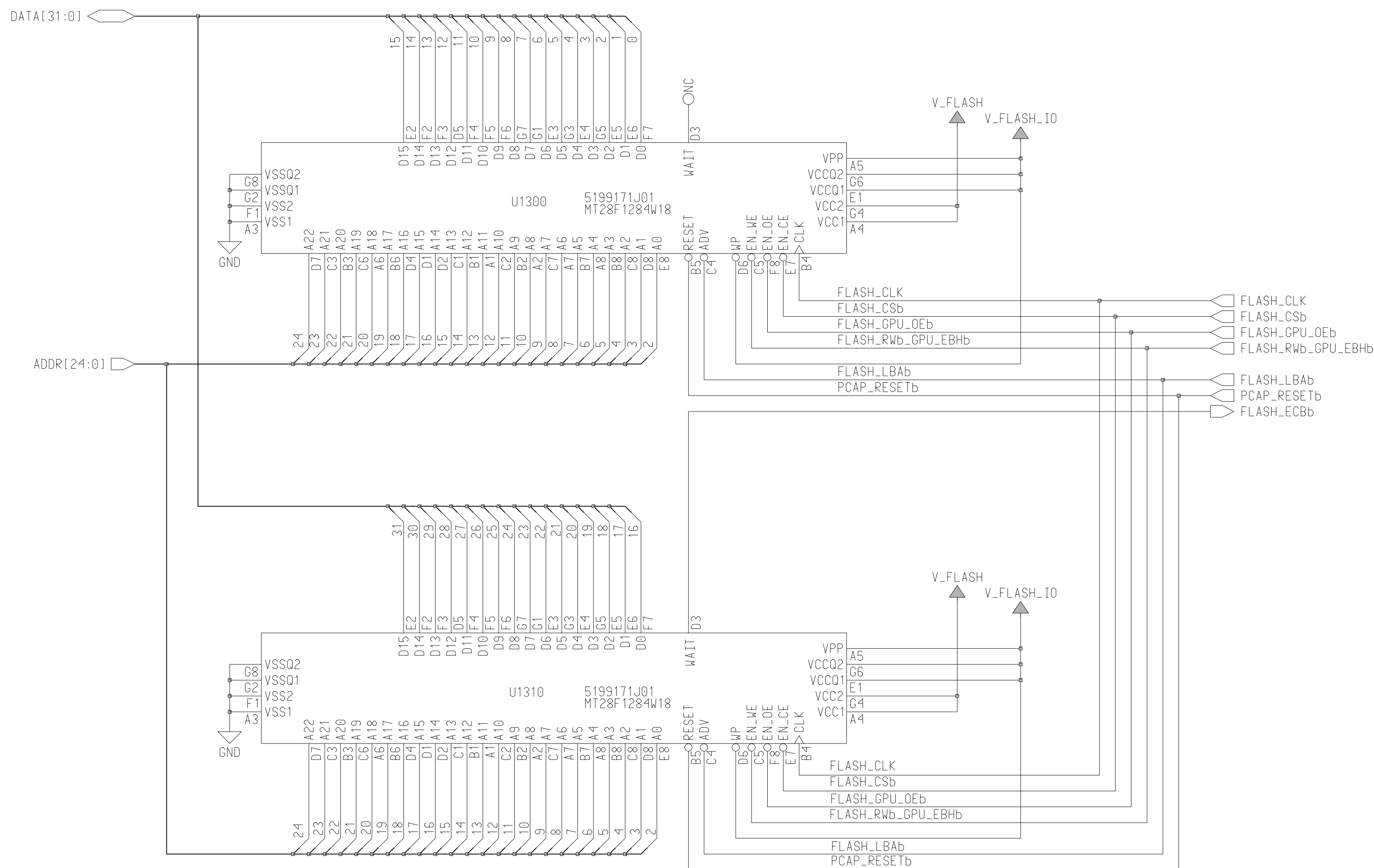
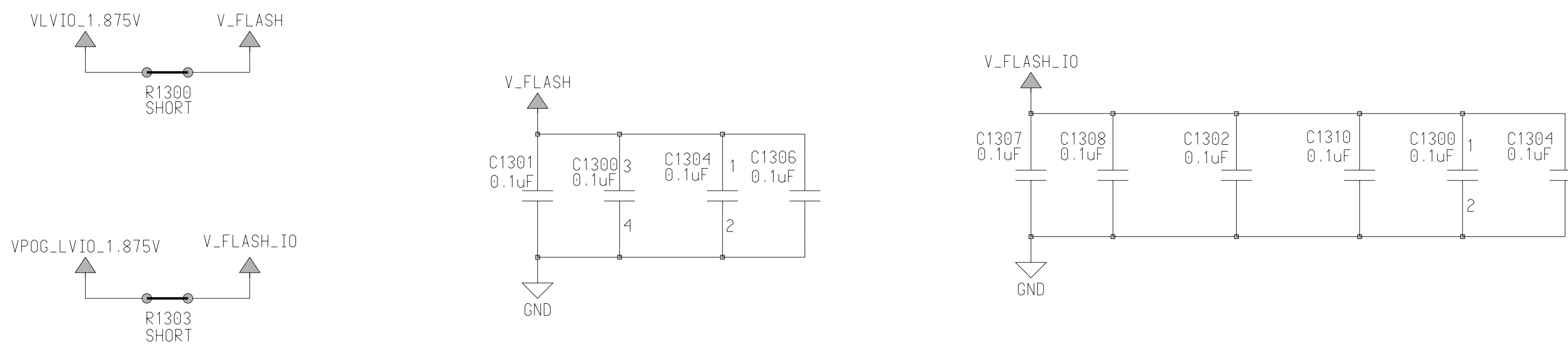
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Changed by:

Date:	Time:
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 **MOTOROLA INC.**

TITLE:	V980	Size:
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Misc Connectors

REV: 0	Drawing Number: 8487724Y10	Page:	Of:
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Date:	Time:
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C

[illegible]

The schematic diagram illustrates the Triflash-R Connector circuit. It features a J3901 3989655N02 connector with the following pin connections:

- VMMC_2.775V**: Connected to PIN1, PIN2, PIN3, PIN4, PIN5, and PIN6. A resistor R3902 (SHORT) is connected between this supply and the connector.
- MMC_CMD**: Connected to PIN4 (CD/DAT3) and PIN5 (CMD).
- MMC_CLK**: Connected to PIN7 (CLK).
- MMC_DAT**: Connected to PIN8 (VSS), PIN9 (VSS), PIN10 (DAT0), PIN11 (SH), and PIN12 (SH).

The circuit also includes the following components:

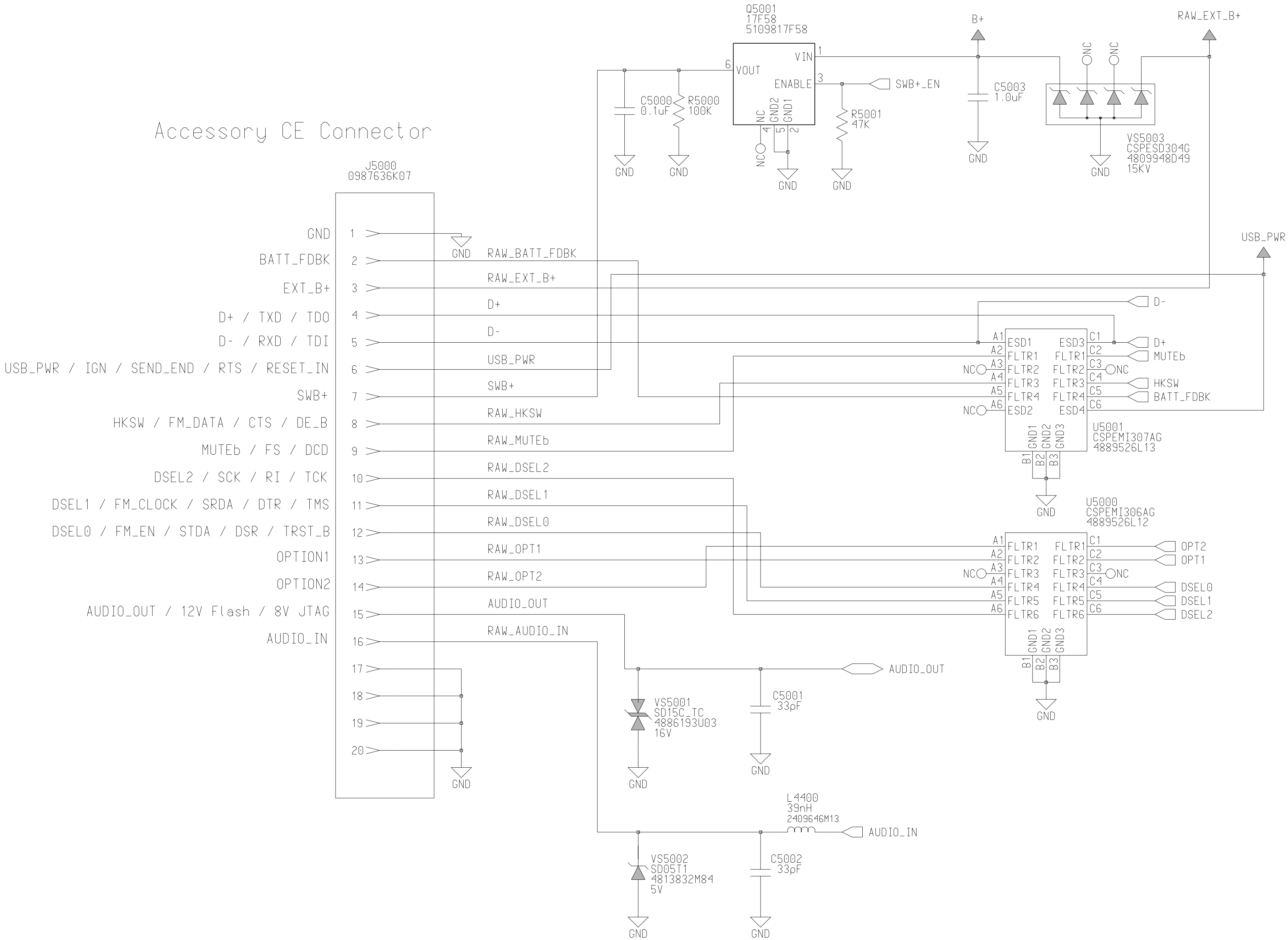
- Resistors**: R3900 (10K) and R3901 (75K) are connected between the VMMC_2.775V supply and the MMC_CMD and MMC_CLK lines, respectively.
- Capacitors**: C3906 (33pF), C3910 (0.1uF), and C3911DNP (1.0uF) are connected to the VMMC_2.775V supply and the MMC_DAT line.
- Diode**: VS5102 (NZQA6V8AXV5T1 4813832M85) is connected between the MMC_DAT line and GND.

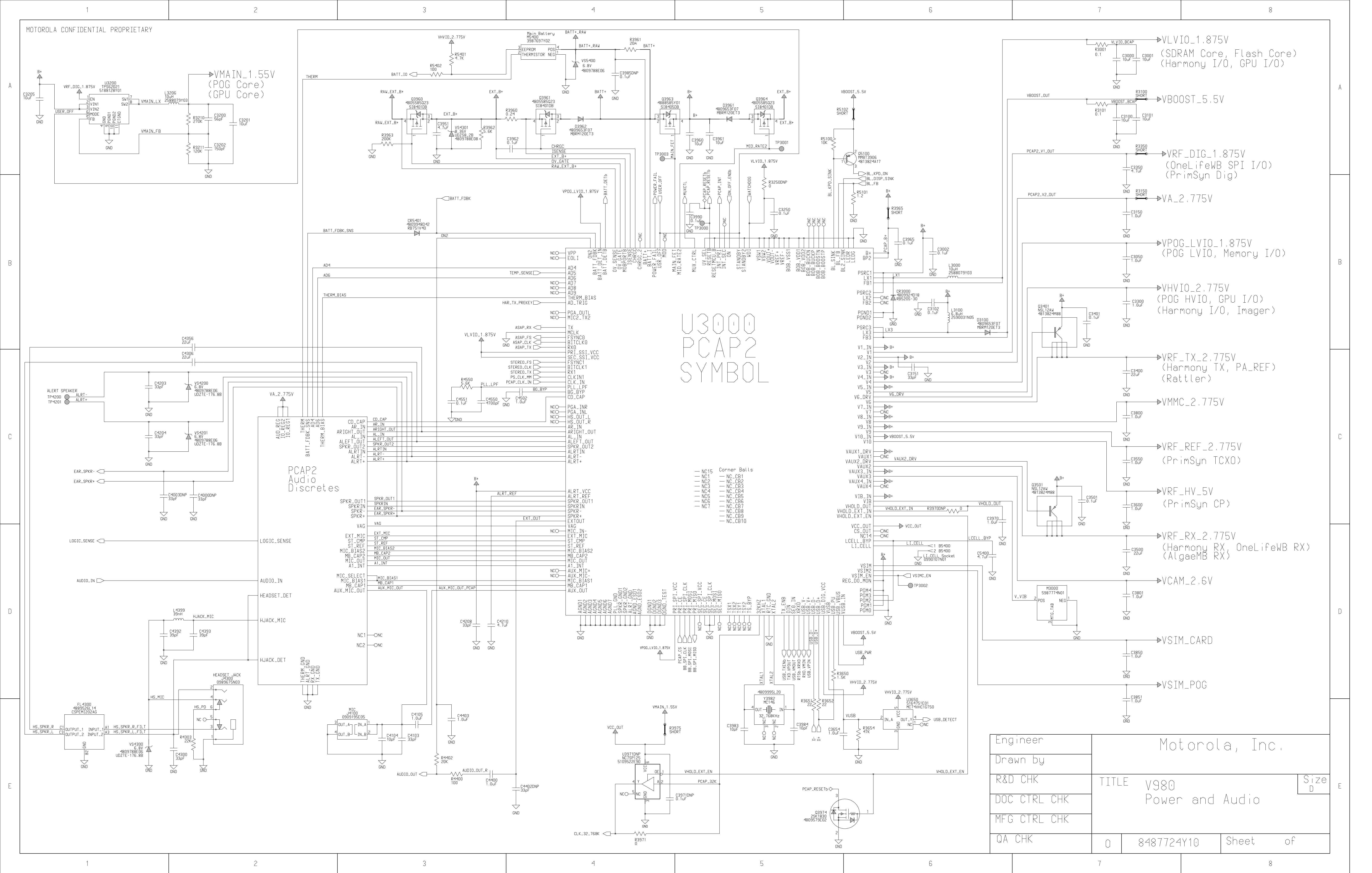
MOTOROLA CONFIDENTIAL PROPRIETARY



Engineer:	V980 CE Connector			
Drawn by:				
R&D CHK:	TITLE:		Size:	
DOC CTRL CHK:	REV: 0		Drawing Number: 8487724Y10	Page:
MFG CTRL CHK:	QA CHK:		Of:	
Changed by:	Date:		Time:	

Accessory CE Connector



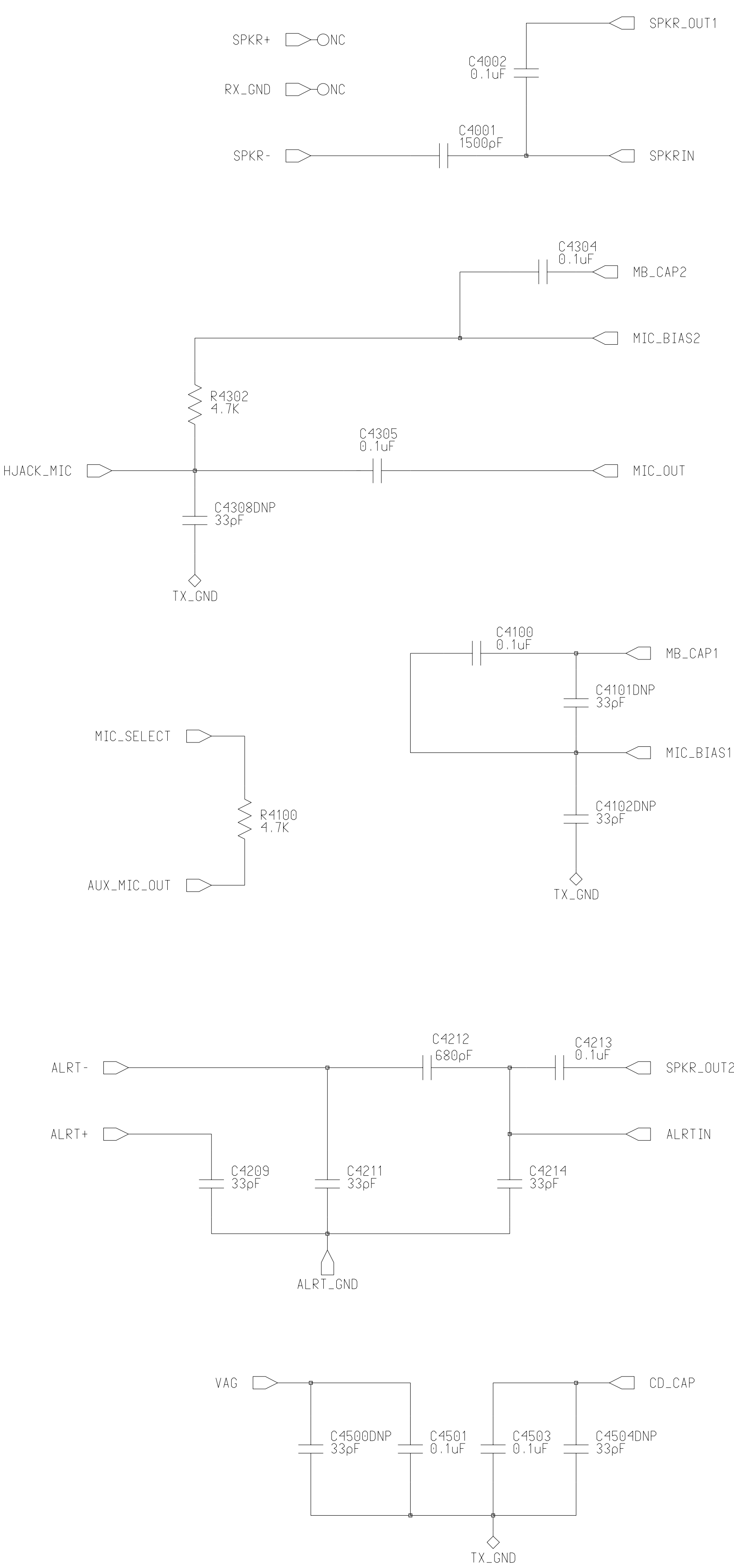
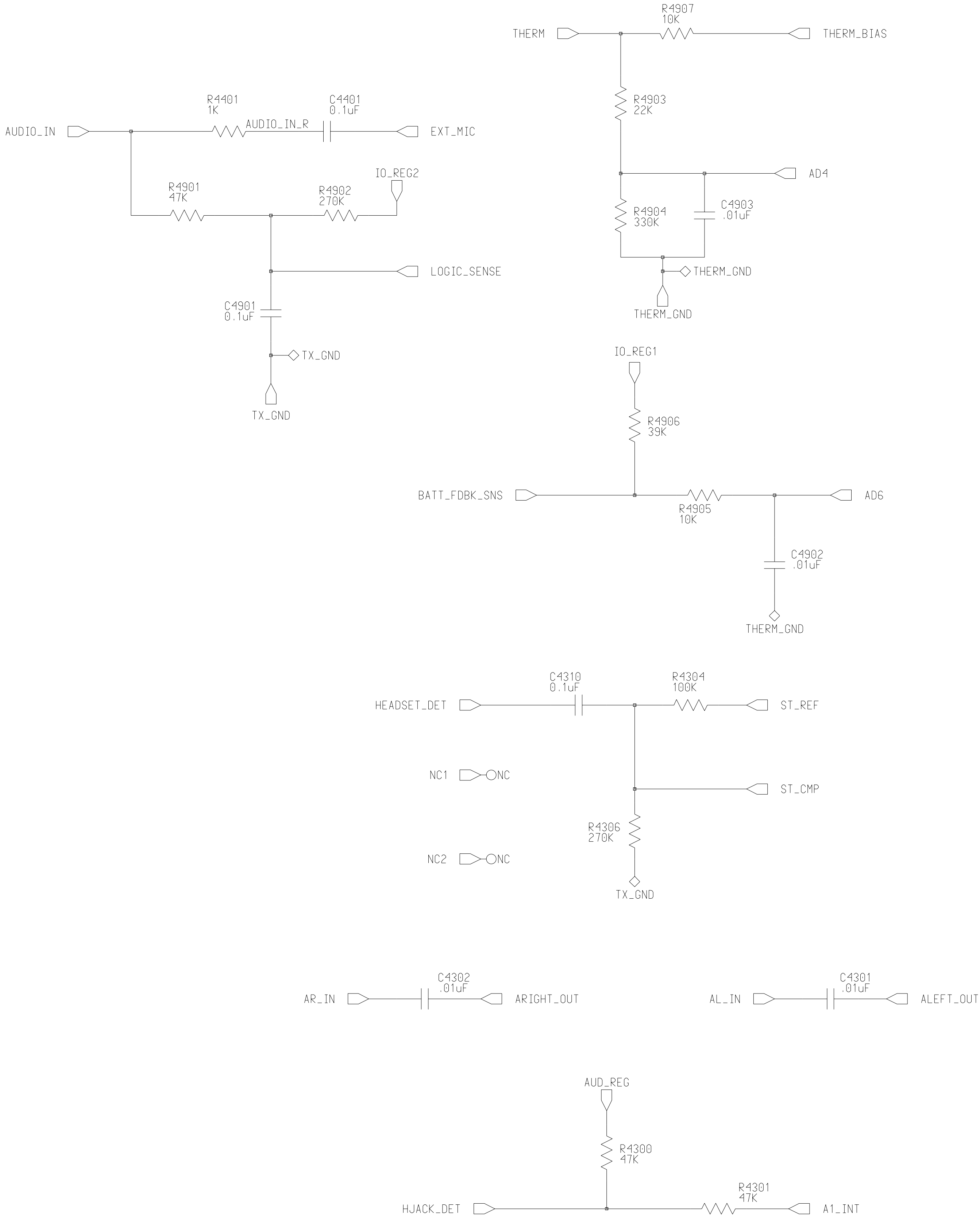


Engineer	Motorola, Inc.		
Drawn by			
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DOC CTRL CHK			
MFG CTRL CHK			
QA CHK	0	8487724Y10	Sheet of

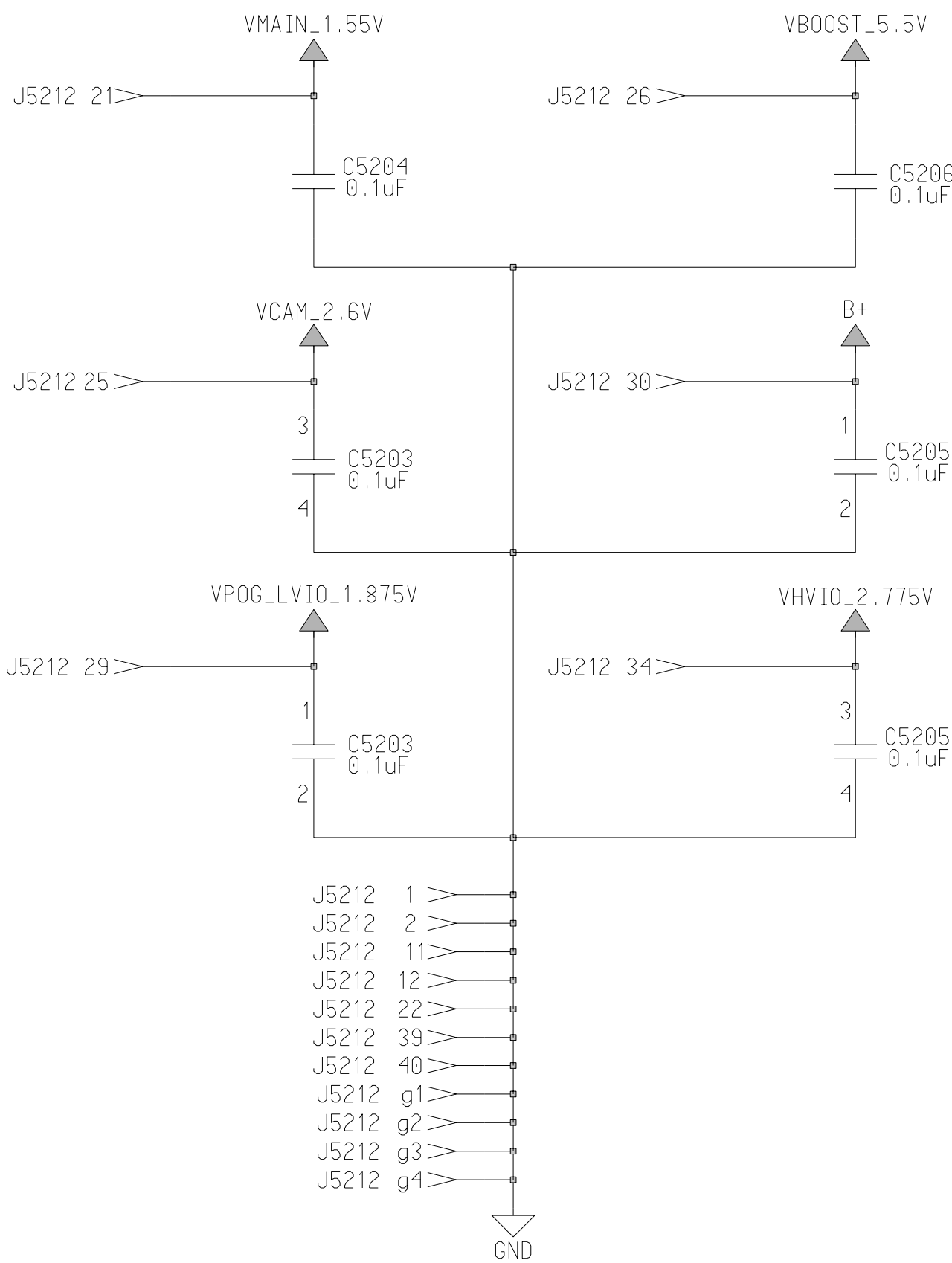
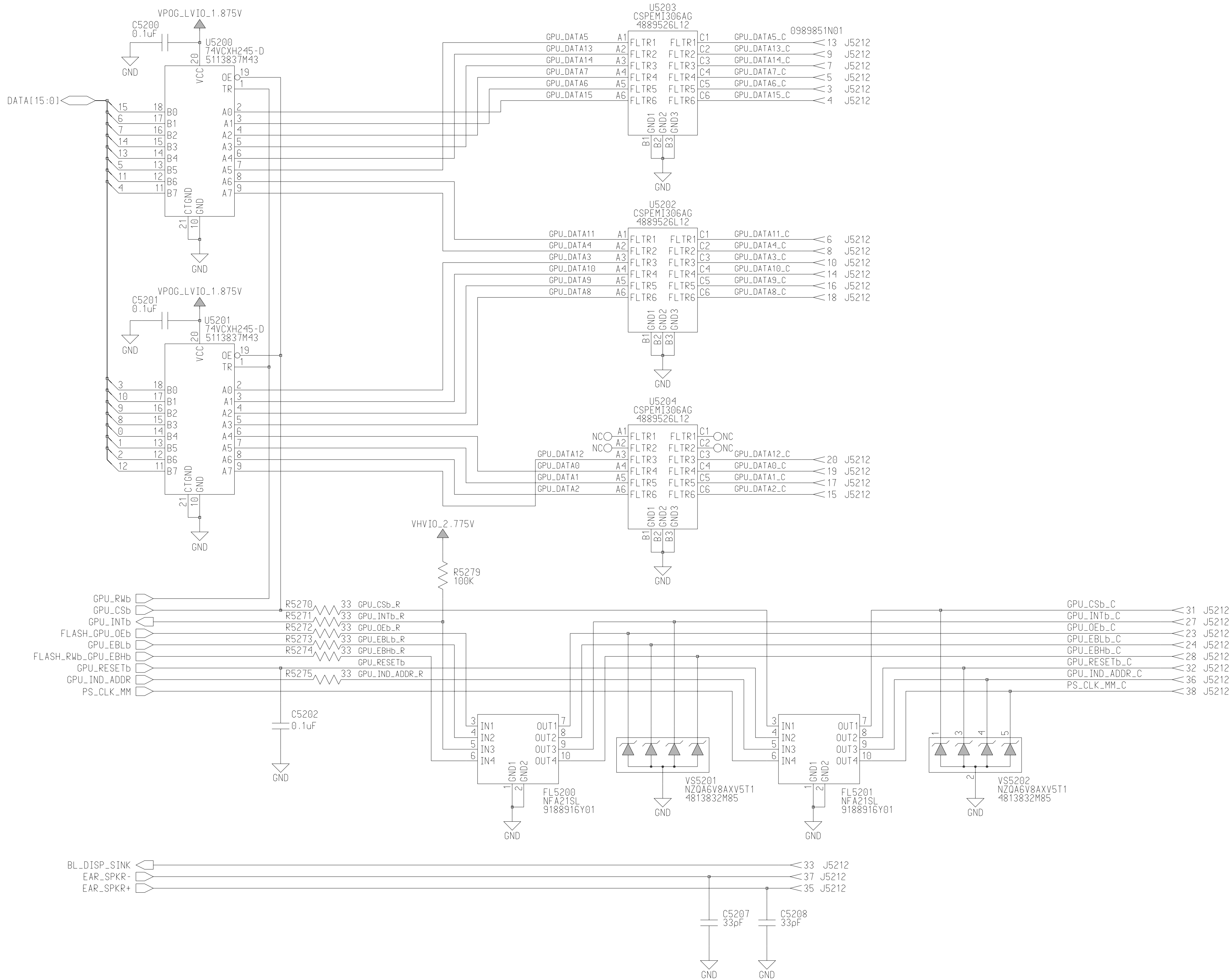
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Engineer:	TITLE: V980 / V975 PCAP Audio Discretes				Size:
Drawn by:					
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DOC CTRL CHK:					
MFG CTRL CHK:	Date:				Time:
QA CHK:					
Changed by:					



Engineer:	MOTOROLA INC.			
Drawn by:				
R&D CHK:	TITLE: V980		Size:	
DOC CTRL CHK:			GPU & Flip Connector	
MFG CTRL CHK:				
QA CHK:	REV: 0	Drawing Number: 8487724Y10	Page:	Of:
Changed by:	Date:			Time:



MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer:	 MOTOROLA INC.		
Drawn by:			
R&D CHK:	TITLE: V980		Size:
DOC CTRL CHK:	POG		
MFG CTRL CHK:	Peripheral Interface		
QA CHK:	REV: 0	Drawing Number: 8487724Y10	Page: Of:
Changed by:	Date:		Time:

A

C

1

