Triplets Theory of Operation

Level 3

Release 1.0

MOTOROLA™

DIGITAL WIRELESS TELEPHONE

Model V600/ V500/ V300

PCS 1900MHz/ DCS 1800MHz/ GSM 900MHz/ GSM 850MHz

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Theory of Operation

Introduction

Motorola V600/V300 telephones are small and lightweight global system for mobile communications (GSM) general packet radio service (GPRS) wireless application protocol (WAP)-enabled mobile phones. The V600/V300 incorporates a new user interface (UI) for easier operation, allows short message service (SMS) text messaging, and includes personal information manager (PIM) functionality. The supported bands for each phone are listed below.

V600

- GSM 850/900/1800/1900 MHz GPRS (2U/4D)

V300

- GSM 900/1800/1900 MHz GPRS (2U/4D)
- GSM 850/900/1900 MHz GPRS (2U/4D)
- GSM 850/1800/1900 MHz GPRS (2U/4D)

V600/V300 telephones support GPRS and SMS in addition to traditional circuit switched transport technologies.

V600/V300 telephones have a clam form factor. They have an externally viewable 96 x 32 pixel display for caller identification and date/time, an internal 176 x 220 pixel display, and the speaker located in the flip. The bottom part of the clam (front housing) contains the keypad, transceiver printed circuit board (PCB), microphone, flex connection, external accessory connector, smart button, volume buttons, and voice button. The standard Lithium Ion (Li Ion) battery fits behind a removable back cover. For V300/V303/V500, standard battery capacity is 650 mAh, for V600 is 750 mAh.

The phone accepts both 3V and 5V mini subscriber identity module (SIM) cards which fit into the SIM holder underneath the battery. The antenna is a fixed stub type antenna. Inexpensive direct connection to a computer or handheld device via RS232 or USB for data and fax calls, and for synchronizing phonebook entries with TrueSync® software, can be accomplished by using the optional data cable and soft modem.

V600/V300 telephones use advanced, self-contained, sealed, custom integrated circuits to perform the complex functions required for GSM GPRS communication. Aside from the space and weight advantage, microcircuits enhance basic reliability, simplify maintenance, and provide a wide variety of operational functions.

Figure 1. V600/V500/V303/V300

V300 **V303/V500** **V600**

Features available in this family of telephones include:

- GSM 850/900/1800/1900 MHz GPRS (2U/4D)
- Built in VGA Camera (640x480 pixels)
- 65K TFT Active Color Display
- External CLI Display (Transflective Reversed)
- Polyphonic Speaker
- Speaker Phone
- Bluetooth™ (V600 only)
- Metal Housings (V600 only)
- Changeable covers (V600 only)
- Situation Lights (V600 only)
- Video Clip Playback (V600 only)
- 5MB User Memory

Antenna Circuit

In order for the phone to report accurate receive level of an incoming signal, the efficiency of the antenna must be taken into account. When a cabled accessory connection is made the plane of reference is shifted to the connector and RX level measurements need to be adjusted accordingly.

The signal ANT_DETB is normally low when a connection to the antenna is present. This signal alerts the software to account for a phased offset to accurately reflect the power of an incoming signal at the antenna. When a cabled accessory is inserted, the path to ground is broken and a pull-up resistor to VDD asserts the ANT_DETB line and signals that the plane of reference is now the accessory port.

Since the signal is normally low and is shunted to ground via a resistive path, the 69 kohm pull-up resistor inside the Neptune LTS / LTE maintains a steady state current drain that is unacceptable for deep sleep requirements. Therefore the ANT_DETB line is configured as a bidirectional line, where it is an input during the time it is begin polled to determine if an antenna is present, and then switched to an output that is always asserted low to eliminate current drain.

Figure 2. Radiated RF

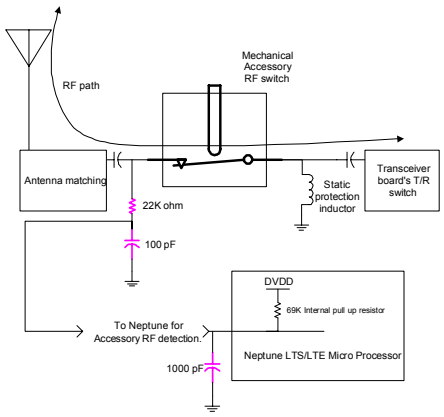
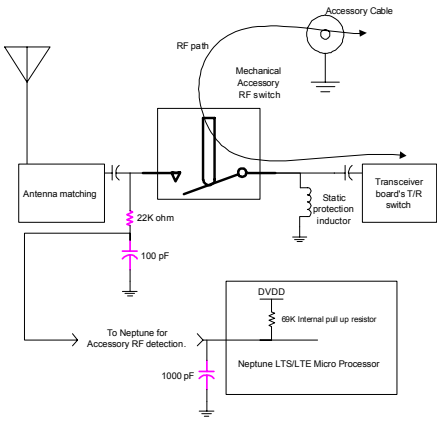


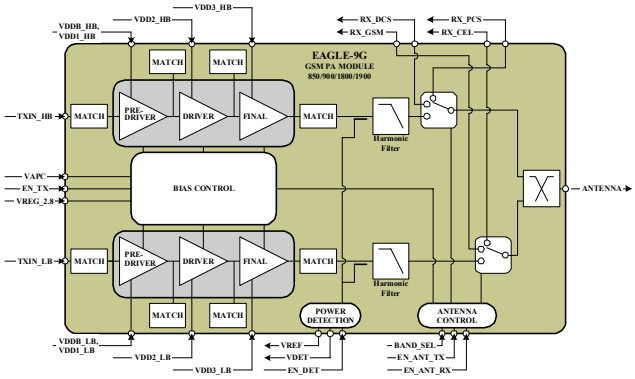
Figure 3. Conducted RF



Eagle 9G

EAGLE-9G is a 2W TX front end module for quad-, tri-, and dual-band GSM handset applications. It is compatible with GSM/GPRS operating modes. Power amplification, power coupling, power detection, low pass filtering, and antenna switching functions are integrated to simplify radio front-end design requirements. Output power is controlled through a single analog voltage pin. Transmit/receive path and enable functions are controlled through 0/2.75V logic inputs.

Figure 4. Eagle-9G Functional Block



Algae MB

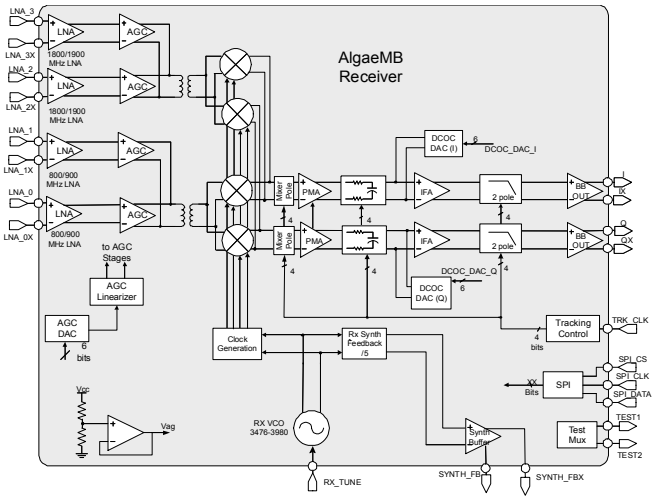
AlgaeMB will replace Algae as part of a low-cost cellular platform that is in production as of July 2002.

The chip set was initially targeted for the GSM and DCS market, but has now been designed for 850GSM/GSM/DCS/PCS. In general, the architecture has been optimized to reduce cost for all four of these frequency bands and additional functionality to support other protocols has not been included.

The AlgaeMB IC is designed in the CDR1BiCMOS process with the SiGe, MIM, and thick copper metal options.

The receiver block diagram is shown in Figure 5. Four LNAs are provided to eliminate the need for external RF switches when using the available receiver frequency bands. On the IC two hi band LNAs (DCS and PCS bands) and two low band LNAs (850GSM and GSM) are grouped together to share the same transformers at the output. The LNAs have differential inputs which will be connected in pairs as hiband-lowband (GSM+DCS, 850GSM+PCS) to the receive saw filter with dual single ended inputs and dual differential outputs. The groupings of LNAs at the inputs are driven

Figure 5. Algae MB Receiver



by the market requirements. The dual band saw filters with single ended inputs and differential outputs come in GSM+DCS bands for European market and 850GSM+PCS bands in the North American market. The LNAs drive AGC current steering stages that feed integrated transformer matching networks. The transformer drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q. The output of the mixer connects directly to the post-mixer amplifier. Large integrated capacitors are used to provide a low-frequency, low-pass corner at the output of the mixer. The signal then passes through baseband amplification and anti-aliasing filtering before going to an off-chip analog-to-digital converter on Neptune/Harmony.

The LO signal is provided by a fully integrated VCO

that drives either a divide-by-two or divide-by-four quadrature generator. In addition, a divide-by-3or5 circuit is used to feed back the LO signal to the synthesizer. The divide-by-3or5 circuit drives a differential output stage that provides the appropriate power level to the synthesizer. This output stage is shared with the TX path and provides the synthesizer feedback signal in both transmit and receive.

Figure 6. Algae MB Transmitter

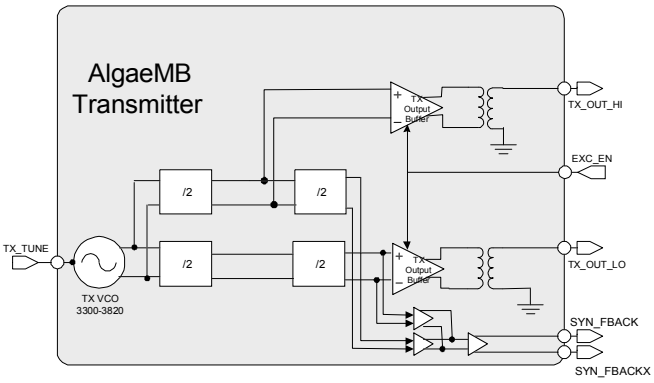


Figure 6 shows the block diagram for the transmitter section of the Algae IC. An integrated VCO is used for the transmit path. Due to the stringent sideband noise requirements for GSM, extreme care must be taken in the design of the VCO and buffer stages. A single VCO is used for transmit. A low noise floor divide-by-2 stage drives the high band output. The low band output is driven by a divide-by-4 stage.

Two transmit output stages are provided. Both stages have integrated output matches in order to reduce the required number of discrete components. The integrated matches are implemented as differential to single-ended transformers.

The transmit signal is fed back to the synthesizer through a differential output stage that is shared with the receiver.

Power Distribution

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are listed below.

Figure 7. PCAP Regulators - 1

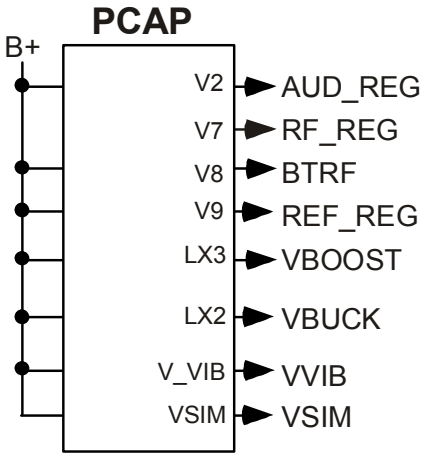
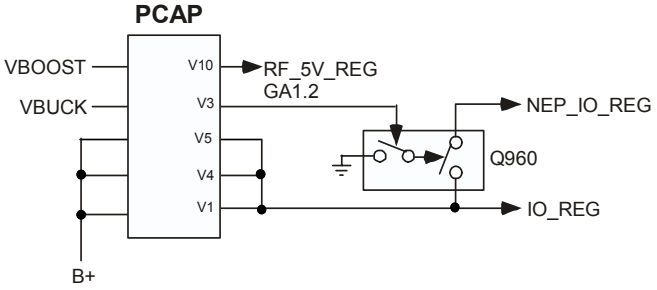


Figure 8. PCAP Regulators - 2



Vbuck, 1.875V +/- 4%

Sources Neptune Core

Vboost 5.6V +/- 5%

Source for V10 & keypad backlights

V1 = I/O REG, 2.875V +/- 3%, Neptune I/O Reg 2.875 +2/-4%

Sources Neptune I/O, ATI Graphics Accel I/O Ring, Camera, SPI interfaces

V3 = VA1.2, Starts at 1.575V then SW selected to 1.275 +/-3%

Sources ATI Graphics Accel core

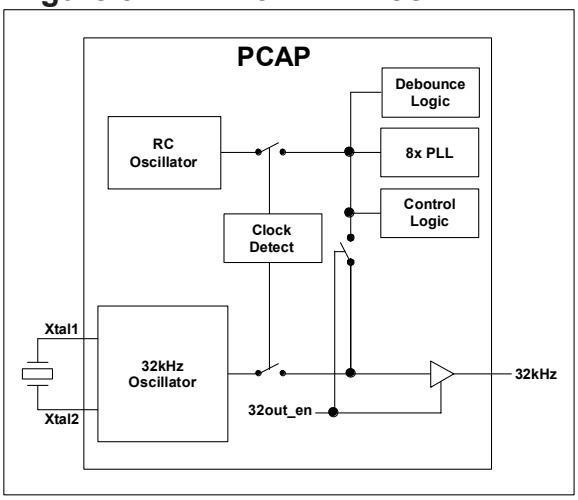
V4/V5 = tied to V1, programmed to OFF, but source internal PCAP circuitry
V6 = NC
V7 = RF_REG, 2.875V +/- 3%
Sources Algae and Support circuitry.
V8 = BTRF, 1.875V +/- 3%
Sources Blue Tooth circuitry
V9 = REF_REG, 1.575 V +/- 3%
RTC and Neptune reference
V10 = RF_5V_REG, 5V +/- 3%
Sources Neptune TX/RX Charge pump

Clock Generation

PCAP can generate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Neptune requires for optimal performance, therefore, an external 32.768kHz crystal is used.

The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Figure 9. PCAP 32kHz Clock



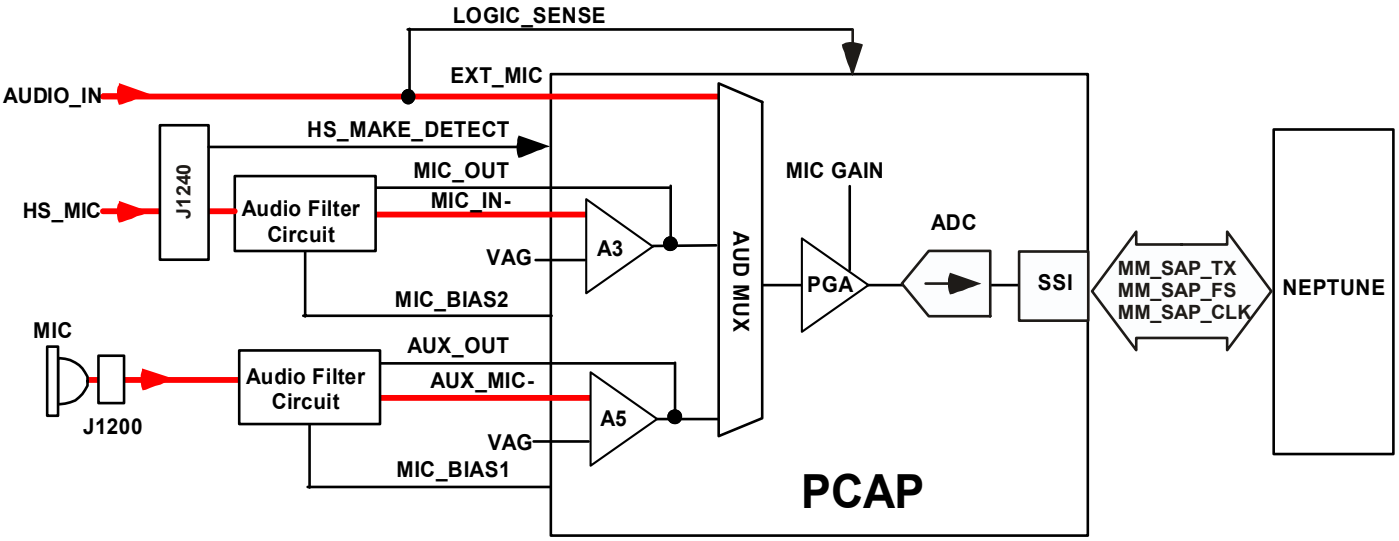
PCAP TX Audio

The mobile phone supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single-ended with respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R1000 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C1000 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C1001, R1001, and R1002 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R1003 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

The headset microphone path is biased through R1020, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C1020 connected to pin MB_CAP2. From here the signal is routed through C1021, R1021, and R1023 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off by R1022 to connect the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HJACK_DET line monitors the presence of a headset by using R1040 as a pullup resistor and detecting the voltage at A1_INT of PCAP, which passes through R1041. A switching mechanism integrated in the headset jack will open or close the HJACK_DET path to ground, depending on whether the headset is attached or not.

Figure 10. TX Audio Functional Block



The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through R1051, C1050, and L1050 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

PCAP RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R1210 and R1211 respectively, and then connected to the transducer. Off the Speaker- path, SPKR_IN is routed through C1011 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C1010, R1013, and C1011 to Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

The headset uses a standard 2.5mm phone jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

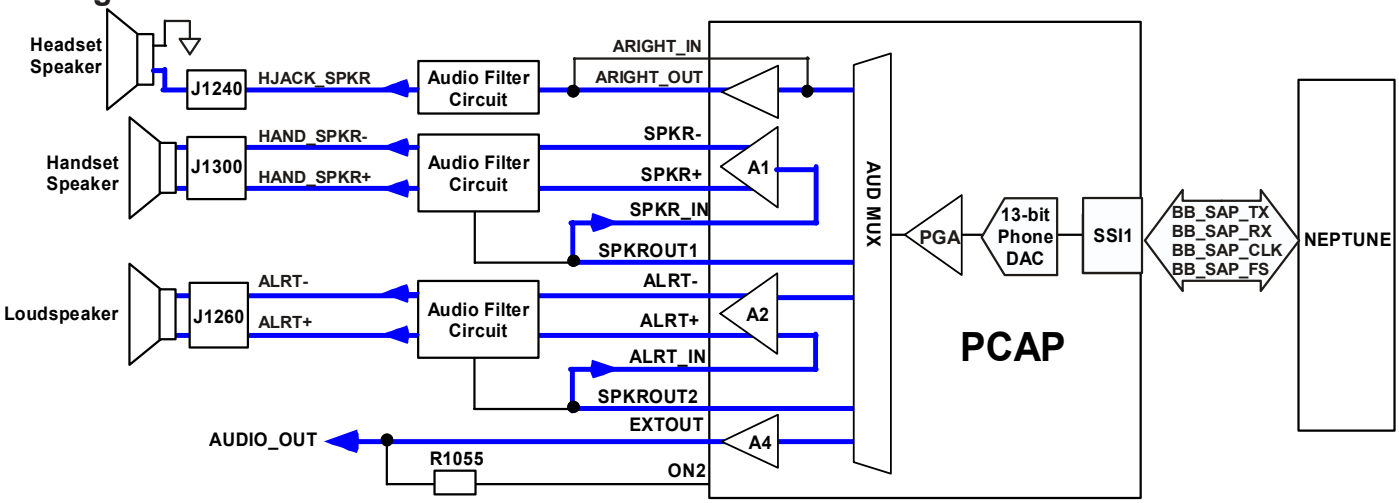
The Headset Speaker is driven by PCAP's internal Right amplifier. Following the speaker path from the PCAP pins ARight_Out, the signal is routed through C1030,

R1030, and L1030. It is then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C1033 for the inverting input of the audio amp ARIGHT.

The External Speaker is connected to pin 15 of J1400 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed from EXTOUT, of the PCAP, through R1054, C1056, and L1400. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R1055 and D1055 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R1061 and R1062 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C1060 and R1060 to ALRT- which is the DAC output of the CODEC.

Figure 11. RX Audio Functional Block



Battery Interface

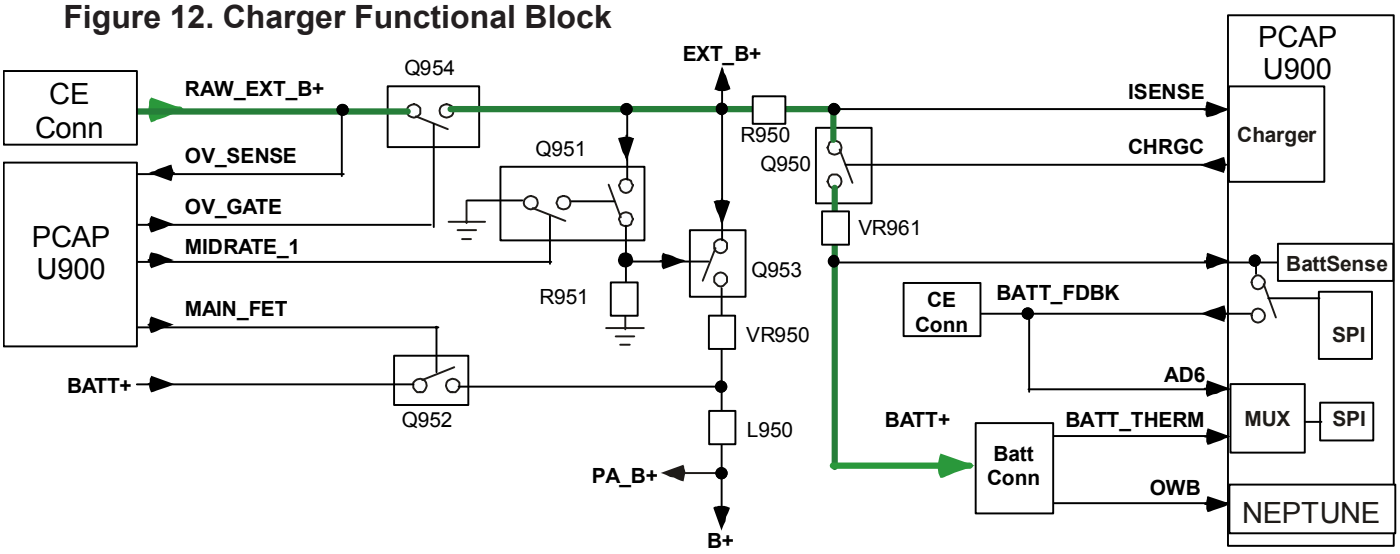
Batteries interface to the main transceiver board via a 4-pin connector (M1700). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q952 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U900) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J1400). During full rate charging, Q953 is turned ON so that current can be supplied from the external source to B+. Q952 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q950. A sense resistor (R950) provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J1400). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 12. Charger Functional Block



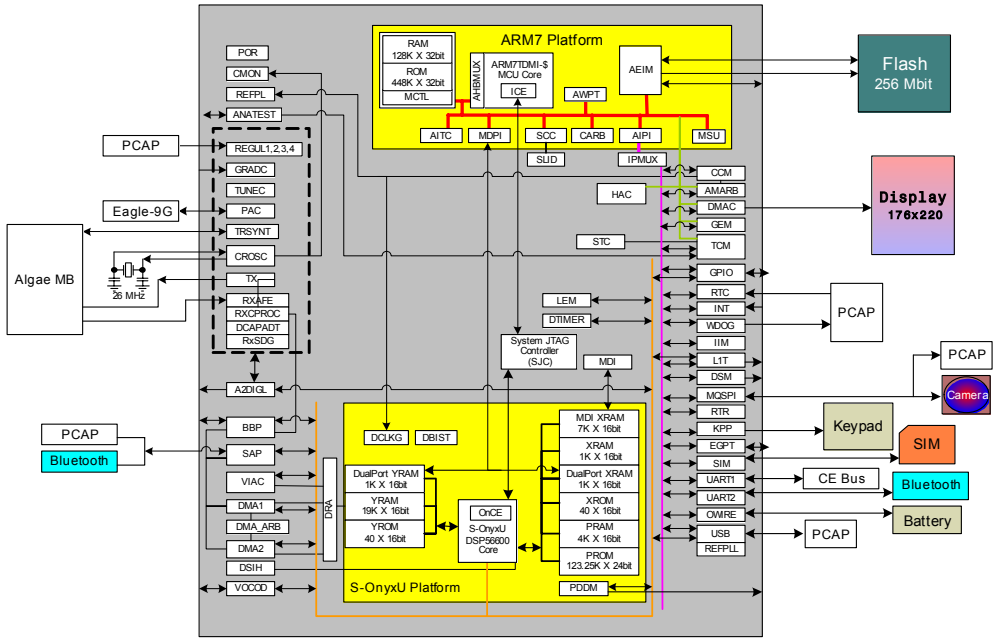
Neptune LTE

The Neptune LTE Baseband IC is a digital baseband processor for the 2.75G GSM Market. The design is derived from Neptune LTS with changes to memory configuration and several module enhancements. It is a dual-core processor that contains a Synthesizable Onyx DSP core (56600), an ARM7TDMI-S microcontroller, and custom peripherals.

The Neptune LTE IC is derived from the Neptune LT IC with the following key changes:

- Addition of Platform Independent Security Architecture (PISA) modules:
  - — Security Controller (SCC),
  - — Memory Separation Unit (MSU)
  - — HASH Accelerator (HAC)
- On-chip memory:
  - — Changed MCU RAM size from 436Kbytes to 512Kbytes for GPRS production version, 256Kbytes for EDGE production version
  - —Decreased MCU ROM size from 3168Kbytes to 1792Kbytes
  - — Increased DSP X, Y, and P RAM and ROM sizes to support new features including EDGE
- Addition of OWIRE peripheral to support removable battery
- Addition of 2nd UART to support e.g. optional applications coprocessor
- Pin and GPIO muxing changes including
  - — support for PCS's CE bus
  - — parallel DMAC
  - — dedicated BBP transmit pins for interface to external EDGE transmit IC
- DSP subsystem changes to support 130MHz required for EDGE
- Neptune LT MCU "PIG" peripheral bus has been omitted. All "PIG" peripherals are now accessed through the "IP" peripheral bus, and their base addresses have been changed (internal register organization remains the same).

Figure 13. Neptune LTE Functional Block



Memory Interface

The portable will be using a memory part containing 3 memory die: two stacked 128Mbyte Burst Flash (Tyax) die and a 32Mbyte PSRAM die. The portable products will be operating at 1.8V core voltages and will have a 1.8V interface to Neptune LTE.
Neptune LTS's AEIM will be interfaced to the stacked memory device and consists of the external address lines, data lines, chip selects, and memory control lines.

The two Tyax memory die contained in the stacked CSP each have a separate chip select signals. In order to access both of these parts through a single CS line and present a contiguous block of memory to the baseband processor, external glue logic is used to create two chip selects from the A24 and CS0 signals.

Keypad Interface

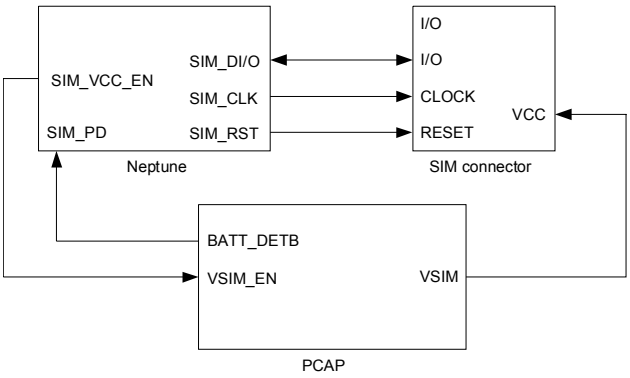
The Keypad Port is a 16-bit peripheral, used generally for keypad matrix scanning, or as a GPIO port up to 16 bits wide. The keypad matrix can be configured up to 8 rows by 8 columns, with unused pins as GPIOs.

For this phone, the keys are mapped as specified in the Synergy keypad matrix, and each row and column will be set as inputs; there is no need to strobe the columns. When a key is pressed, an interrupt will be generated and software will detect which pair of row(s) and/or column are low, then read the four bytes for each pair.

SIM Interface

The SIM interface block is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards. The card itself stores important information including the subscriber telephone number, phone numbers, the users' PIN, and other information to be able to complete a phone call. The card holds all this information for the user and therefore must be protected from electro-static discharge that could destroy the card. We prevent this event by also requiring the user to attach a battery. Batteries on Motorola product are arranged in such a way to fully cover the SIM block.

Figure 14. SIM Interface



The SIM block has two ports that can be used to interface with the various cards. The interface with the MCU is a 16-bit connection via the AIPI Controller and the IP-Bus Interface. Figure 13 shows the signals and direction of propagation between the different device modules.

PCAP can supply the SIM block with either 1.875 V or 3.0 V. The bit VSIM_0 determines the voltage. This is bit number 18 in the AUX_VREG register (location 07). The 5 V SIM cards are not supported with this architecture.

The VSIM regulators on and off state will be controlled by one SPI bit (VSIM_EN) and one external pin (SIM_VCCEN). SIM_VCCEN is a pin on Neptune that connects to the VSIM_EN pin of PCAP. The SIM regulator will be on only when the SIM_VCCEN pin and the VSIM_EN SPI bit are logic high. The voltage supply to the card must be shut down before the SIM card is removed and the card loses contact with the radio. Because of the nature of the removable SIM card the SIM regulator must be able to withstand a short

circuit at its output without sustaining any damage.

The SIM module contains a block designed specifically for generating the clocks used internal to the SIM module, and the clocks provided to the SIM cards.

There are no interrupt sources generated by the SIM clock generator block.

The SIM Transmitter block contains the transmit state machine, transmit shift register, and transmit FIFO. The SIM Receiver block contains the receive state machine, receive FIFO, and control logic.

On power up, the phone checks for connected accessories and for the validity of battery voltage. If the battery voltage is valid then the SIM Card is secure and the phone attempts to read data from the SIM on the SIM_I/O line. If no data is read then that indicates that a card is not present and S/W should write "CHECK CARD" to the display.

The SIMPD input allows for detection of the insertion or removal of a SIM card. A maskable interrupt can be generated when a SIMPD event occurs. An internal 69k pullup is present on the SIMPD pin for Neptune. This will provide for a high to low transition on the SIMPD pin when a SIM card is removed.

The SIM port control block contains hardware that provides the correct sequence to power down a SIM card. The software must perform the power-up sequence.

The power down sequence is:

RST transitions from high to low
CLK is turned off to a low
I/O transitions from tri-state to low
SIM Vcc is turned off

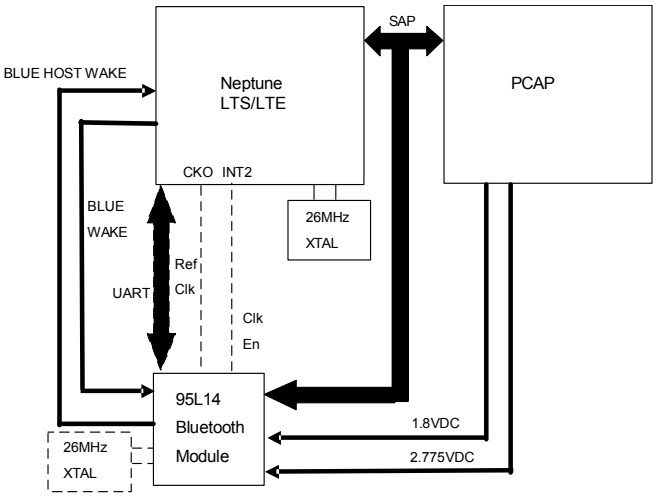
The SIM module is capable of forcing a SIM card power down. It is similar to the auto power down feature, except that it is not dependent upon either the state of the SIM card auto power down enable bit, or triggering of a presence detect event.

Bluetooth (V600/V500 only)

The HCI interface will utilize an UART. There are two data signals (TXD and RXD) and two flow control signals (RTS and CTS). The BT module assumes a role as DTE and the Neptune LTS/LTE acts as a DCE. Therefore when the BT module is connected to Neptune LTS/LTE the RXD and TXD lines must be crossed, while CTS and RTS on Neptune connect directly to CTS and RTS on the BT module. RXD and TXD have been crossed on the BT module already; therefore, BLUE_TX (pin 5) of the BT module is connected to TXD2 (pin N13) and BLUE_RX (pin 33) of the BT module is connected to RXD2 (pin N17) on Neptune LTS/LTE 257 pin package.

The Bluetooth UART is a dedicated UART from Neptune LTS/LTE. This bus is not shared with external peripherals.

Figure 15. Bluetooth System Block



Although most signaling is done over the HCI, wake-up signaling is done with dedicated signals. Neptune LTS/LTE uses a GPIO (PC14/pin B15) to wake up the BT module. The BT module uses a dedicated signal BLUE_HOST_WAKEB (Pin 9) connected to a Neptune LTS/LTE interrupt (INT 5) to wake-up the host processor.

The codec is connected onto a shared 4 wire bus with Neptune LTS/LTE and PCAP referred to as the BB_SAP (Base Band Serial Audio Codec Port). The PCAP acts as the master and provides the clock and frame sync signals for the bus. The labeling on the Bluetooth module is in reference to the Neptune LTS/LTE. Therefore, the ASAP_TX line is an input and ASAP_RX is the output from Bluetooth.

Bluetooth is reset in a number of different ways. When software first initializes Bluetooth, it sends an HCI reset command over the UART interface to place the BCM2035 into a known state.

If software fails to detect a response to the initial HCI reset command, it will power cycle the RF and Core voltages thus forcing a power on reset on the BCM2035.

Additionally, Neptune LTS/LTE can reset Bluetooth using the RESET_OUT signal (pin W5). A level shifted version RESET_OUT at 2.775 V is connected to RESET_N (pin 22) of the BT module. RESET_N is active low. This option would be used when the software initiates a soft reset, but power supplies or the main RESETB signals are not asserted.

The Broadcom chipset requires two different frequency references, a lower frequency low power reference (32.768 kHz), and a high frequency main reference (15.36 MHz, 26 MHz, etc.). The low power reference is a standard frequency available on the GSM phone whenever the phone is powered. As such, this reference is directly connected to CLK_32KHZ, the buffered port from the oscillator on PCAP.

As this module will be primarily used on GSM platform, PLL components on the module were tuned for 26 MHz with the intent to share the crystal frequency oscillator of the phone, Neptune LTS XTAL OSC.

Unlike the low power reference, the Neptune XTAL OSC, is not available all the time and does not provide a dedicated buffered output. When Bluetooth requires this reference when being paged, it must wake up its host processor (Neptune LTS) if it is in deep sleep. When the Bluetooth switches to the main reference it should not disturb the Neptune LTS XTAL OSC circuit in regards to frequency, or noise performance, thereby dictating some amount of isolation or buffering.

This option would use a 2.5 x 3.2 mm discrete 26 MHz crystal with two shunt capacitors (15 pF). The XTAL circuit oscillator is contained on the BCM2035 and enables itself without any control from the host processor.

The host processor, though, must program a trim value to the Bluetooth module via an HCI command every time the Bluetooth module is POR. This trim value is programmed in the phone's SEEM at the time of factory phasing.

CKO is a multiplexed clock output available from Neptune LTS.

Software will need to program Neptune LTS/LTE to configure the CKO pin to use this uncorrected clock on every POR. Enabling signal for this option will be via the BLUE_CLK_ENB signal which is connected to interrupt INT2 of Neptune LTS/LTE.

Software will also need to provide a trim value to the Bluetooth module on every POR as with the case for the discrete Oscillator Buffer described above.

Flip Interface

The Flip Display Module functions as a core display subassembly that also supports an external Caller ID (CLI) display in 96x32 B/W LCD formats.

Customization of this module for a specific product application is done by combining this module through its interfaces with a product-specific PF (Personality Flex), and optional CLI module assy.

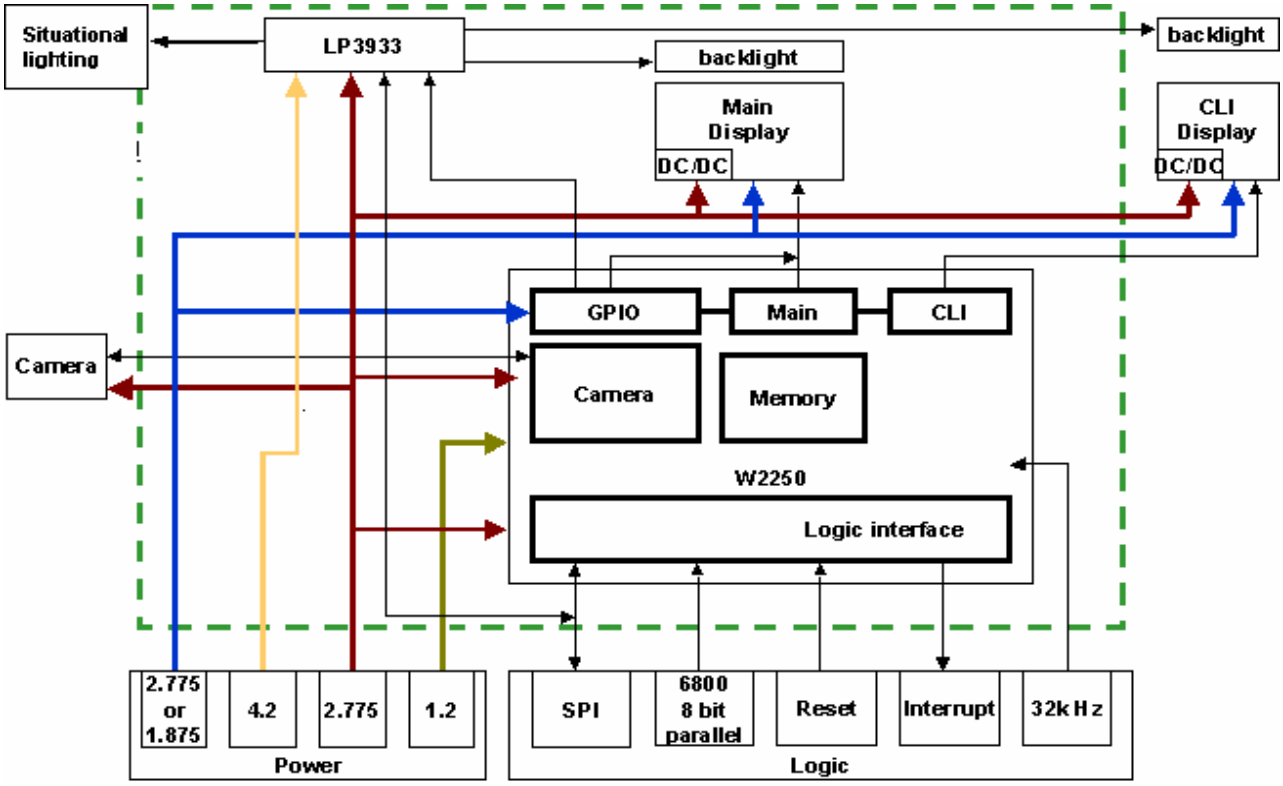
The PF interface is a 30 pin board-to-board connector designed to accept a product-specific PF. The characteristics of a product-specific PF are typically determined by the product team, and must include a connector interface to the phone, along with possible interfaces to various phone components such as speaker, vibrator, camera…etc.

The Caller ID interface is a 13 pin ZIF connector designed to mate with a 96x32 B/W CLI module.

The Situational lighting interface is a 20 pin Board-to-Board connector designed to mate with RGB LEDs.

The Camera interface is a 20 pin ZIF connector designed to mated with the CMOS camera module.

Figure 16. Flip Display Module



Block Diagram

A block diagram of the V600/V300 is illustrated below.

Figure 17. V600/V300 RF Block Diagram