MOTOROLA

Level 3 Service Manual

V265, V262, V260
Digital Wireless Telephone

CDMA 1900 MHz, CDMA 800 MHz, Analog 800 MHz

Introduction

Motorola® Inc. maintains a worldwide organization that is dedicated to provide responsive, full-service customer support. Motorola products are serviced by an international network of company-operated product-care centers as well as authorized independent service firms.

Available on a contract basis, Motorola Inc. offers comprehensive maintenance and installation programs that enable customers to meet requirements for reliable, continuous communications.

To learn more about the wide range of Motorola service programs, contact your local Motorola products representative or the nearest Customer Service Manager.

Product Identification

Motorola products are identified by the model number on the housing. Use the entire model number when inquiring about the product. Numbers are also assigned to chassis and kits. Use these numbers when requesting information or ordering replacement parts.

Product Names

Product names are listed on the front cover. Product names are subject to change without notice. Some product names, as well as some frequency bands, are available only in certain markets.

Regulatory Agency Compliance

This device complies with Part 15 of the FCC Rules. Operation is subject to the following conditions:

- This device may not cause any harmful interference
- This device must accept interference received, including interference that may cause undesired operation

This class B device also complies with all requirements of the Canadian Interference-Causing Equipment Regulations (ICES-003).

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Computer Program Copyrights

About this Service Manual

Using this service manual and the suggestions contained in it assures proper installation, operation, and maintenance. Refer questions about this manual to the nearest Customer Service Manager.

Audience

This service manual aids service personnel in testing and repairing V265 and V260 telephones. Service personnel should be familiar with electronic assembly, testing, and troubleshooting methods, and with the operation and use of associated test equipment.

Use of this manual assures proper installation, operation, and maintenance of Motorola products and equipment. It contains all service information required for the equipment described and is current as of the printing date.

Scope

This manual provides basic information relating to V265 and V260 telephones, and also to provides procedures and processes for repairing the units at Level 1 and 2 service centers including:

- Unit swap out
- Repairing of mechanical faults
- Basic modular troubleshooting
- Testing and verification of unit functionality
- Initiate warranty claims and send faulty modules to Level 3 or 4 repair centers

Conventions

The following special characters and typefaces are used in this manual to emphasize certain types of information.

Note: Emphasizes additional information pertinent to the subject matter.

Caution: Emphasizes information about actions that may result in equipment damage.

Warning: Emphasizes information about actions that may result in personal injury.

Keys to be pressed are represented graphically. For example, instead of "Press the Menu Key", you will see "Press ".

Information from a screen is shown in text as similar as possible to what displays on the screen. For example, ALERTS or ALERTS or ALERTS.

Information that you need to type is printed in **boldface type**.

Warranty Service Policy

The product is sold with the standard 12-month warranty terms and conditions. Accidental damage, misuse, and extended warranties offered by retailers are not supported under warranty. Non warranty repairs are available at agreed fixed repair prices.

Out-of-Box Failure Policy

The standard out of box failure criteria applies. Customer units that fail very early on after the date of sale, are to be returned to Manufacturing for root cause analysis, to guard against epidemic criteria. Manufacturing will bear the costs of early life failure.

Product Support

Customer's original units will be repaired but not refurbished as standard. Appointed Motorola Service Hubs will perform warranty and non-warranty field service for level 2 (assemblies) and level 3 (limited PCB component). The Motorola High Technology Centers will perform level 4 (full component) repairs.

Customer Support

Customer support is available through dedicated Call Centers and in-country help desks. Product Service training is available through the local Motorola Support Center.

Parts Replacement

When ordering replacement parts or equipment, include the Motorola part number and description used in the service manual or supplement.

When the Motorola part number of a component is not known, use the product model number or other related major assembly along with a description of the related major assembly and of the component in question.

In the U.S.A., to contact Motorola, Inc. on your TTY, call: 800-793-7834

Accessories and Aftermarket Division (AAD)

Order replacement parts, test equipment, and manuals from AAD.

U.S.A.	Outside U.S.A.
Phone: 800-422-4210	Phone: 847-538-8023
FAX: 800-622-6210	FAX: 847-576-3023

In EMEA call +49 461 803 1638.

In Asia call +65 648 62995.

Specifications

General Function	Specification
Frequency Range 1900 MHz PCS	1931.250 -1988.750 MHz Rx 1851.250 -1908.750 MHz Tx
Frequency Range 800 MHz CDMA/ AMPS	869.04 - 893.97 Rx 824.04 - 848.97 Tx
Channel Spacing	50 kHz PCS 30 kHz CDMA/AMPS
Channels	1200 PCS 832 CDMA/AMPS
Modulation	1M25D1W (1.25 MHz bandwidth) CDMA 3G1XRTT (1.25 MHz bandwidth) CDMA-1X F3 +12 kHz for 100% at 1 kHz AMPS
Transmitter Phase Accuracy?	5 Degrees RMS, 20 Degrees peak
Duplex Spacing	80 MHz PCS 45 MHz AMPS
Frequency Stability	± 300 Hz (CDMA) ± 2.5 ppm (AMPS)
Power Supply	3.6V Li Ion 750 mAh battery
Average Transmit Current	310 mA at +13dBm)
Average Stand-by Current	3.40 mA
Dimensions (with 820 mAh Li ion battery)	46.5mm x 91mm x 22.8mm 1.83 in. x 3.58 in. x 0.89 in.
Size (Volume)	80 cc (4.88 $in.^3$) without antenna
Weight	≤110g (3.88 oz) with battery
Operating Temperature Range	-30° C to +60° C (-22° F to +140° F)
Humidity	80% Relative Humidity at 50° C (122° F)
Battery Life, 820 mAh Li Ion Battery	Digital Talk Time: 178 Minutes (IS95/IS2000 Cell/PCS, CDG Suburban Profile with 40% VAF ~ + 110.6dBm) Digital Standby Time: 264 Hours (IS95/IS2000 Cell/PCS Slot Cycle 1) Analog Talk Time: 65 Minutes (AMPS Power Step 2) Analog Standby Time: 15 Hours (AMPS DRX)
	All talk and standby times are approximate and depend on network configuration, signal strength, and features selected.

Transmitter Function	Specification
RF Power Output	0.20 watts +23 dBm into 50 ohms (CDMA/PCS nominal) 0.60 watts +27.0 dBm into 50 ohms (AMPS nominal)
Input/Output Impedance	50 ohms (nominal)
Transmit Audio Response	6 dBm/octave pre-emphasis
Modulation	1M25DIW (1.25 MHz bandwidth) CDMA
CDMA Transmit Waveform Quality (Rho)	0.94

Receiver Function	Specification
Receive Sensitivity	-116 dBm (AMPS, SINAD, C-MSG weighted) Sinad 12dB or greater -104 dBm (CDMA/PCS, 0.5% Static FER) 0.5% or less
Audio Distortion	Less than 5% at 1004 Hz, +/- 8 kHz peak frequency deviation (transmit and receive)
Adjacent and Alternate Channel Desensitization	3% BER max at 107 dBm signal; -94 dBm/30 kHz, -65 dBm/60 kHz
IM (AMPS)	Greater than 65 dB

Product Overview

Motorola V265 and V260 mobile telephones feature Code Division Multiple Access (CDMA) technology. The mobile telephone uses a simplified icon and Graphical user interface (GUI) for easier operation, allow Short Message Service (SMS) text messaging, and include clock, alarm, datebook, calculator, and caller profiling personal management tools. The V265 only includes a built in camera. Both phones provide 32 Embedded ring tones including VibraCall vibrating alert and 32 Downloadable/Customizable iMelody ring tones. The V265 and V260 are dual band phones that allow roaming within the CDMA 800 MHz, PCS 1900 MHz, and Analog 800 MHz bands.

The V265 and V260 CDMA phones consist of a main housing assembly and a flip assembly. The phone has the main circuit board, battery, headset jack, and accessory connector in the main housing assembly. The display and camera on the V265 are located in the hinged flip assembly.

The flip assembly contains the entire hinge mechanism. It is attached to the main housing by four screws. The main display is on the inside of the flip assembly and a one line LED display on the outside of the flip assembly. The main display is a 128 x 128 65k CSTN LCD. The external display is a 96 x 32 STN LCD. The camera is a 350K pixel, VGA CMOS Sensor Camera.

The main housing assembly includes a battery cover, chassis, main circuit board, keypad plastic front housing, and retractable antenna.

The main circuit board contains the Receiver, Transmitter, Synthesizer and Control Logic Circuitry which together comprise the dual band tri-mode phone electronics.

The telephones are made of polycarbonate plastic. The display and speaker, as well as the 18-key keypad, transceiver printed-circuit board (PCB), microphone, charger and headphone connectors, and power button are contained within the flip form-factor housing. The 750 mAh Lithium Ion (Li Ion) battery provides up to 178 minutes of talk time in CDMA mode with up to 264 hours of standby time[1].

Features

V265 and V260 telephones use advanced, self-contained, sealed, custom integrated circuits to perform the complex functions required for CDMA communication. Aside from the space and weight advantage, microcircuits enhance basic reliability, simplify maintenance, and provide a wide variety of operational functions.

Features available in this family of telephones include:

- 1.3 M-pixel Camera with Integrated Flash
- Integrated VGA Camera (V265)
- 128 x 128 65K CSTN Display
- Qualcomm MSM 6100 Chipset
- BREW 2.1
- Location Based Services Capable
- Multimedia Messaging Service
- Office Quality Speakerphone
- Speaker Independent Voice Dial
- 64 Level Polyphonic

1. All talk and standby times are approximate and depend on network configuration, signal strength, and features selected. Standby times are quoted as a range from DRX=2 to DRX=9. Talk times are quoted as a range from DTX off to DTX on.

- Consumer Postponable
- AFLT/aGPS location services[2]

Simplified Text Entry

iTAP™ predictive text entry. Press a key to generate a character and a dynamic dictionary uses this to build and display a set of word or name options. The iTAP™ feature may not be available in all languages.

Personal Information Management

The V265, V260 telephones contain a built in date book with alarm reminders message center and a 100 number capacity phonebook.

2. Network, subscription or service provider dependent feature. Not available in all areas.

LOGIC THEORY OF OPERATION

Turn-On Sequence

There are two ways that the unit will turn on. Either the user presses and holds the turn on/off button for more than 1 second or a valid external power source is applied to the CE connector.

During power up U3000 (PM6000) will place PON_RESETB low and keep U1000 (MSM) in a reset state. During this time regulated voltages VREG_MSMA, VREG_MSMC, VREG_MSMP, and VERG_TCXO are allowed to come online and stabilize. Also when VREG_TCXO is brought online, U250 (TCXO) starts to oscillate at 19.2MHz and routes the signal to U3000 pin 4. After approximately 20mSEC, PON_RESETB will go high, TCXO_OUT is enabled (19.2MHz to MSM) and the MSM will start to run bootloader code and access U2000 (Flash) and U2100 (PSRAM). From this point going forward the MSM will must set PS_HOLD to a logic high within 200mSEC or U3000 will power down the unit.

There is an additional 50mSEC delay added to VDD_MSMP to ensure that all other voltages are present and stable prior to applying voltage to the core memory of U1000 (MSM). This voltage is delayed by the start up circuit Q3900 and uses RC time constant of C3900 and R3901 with input voltage VDD_MSMC to delay VDD_MSMP.

U3500 is 1.85VDC voltage regulator and buffer to produce VDD_MSMC and VDD_MEM which are used by U1000 (MSM), U2000 (Flash) and U2100 (PSRAM).

Battery Charging

When external power is connected at the CE connector, this power is applied to Pin1 of U3000 (PM) IC and to Q3000 as EXT_B+. If the EXT_B+ is a valid voltage source and BATT_PLUS on pin 2 is greater than 2.9VDC, U3000 will set BAT_FETB to a logic low with will turn on Q3002, and will adjust the charge current through Q3000 and Q3001 with control signal CHG_CNTB.

EXT_B+ must be between 3.3VDC and 5.6VDC for U3000 to enable battery charging mode. If the External voltage is less than 3.3VDC, U3000 will not switch to external power mode, but continue to draw power from the battery. If EXT_B+ is between

5.6.VDC and 14VDC, U3000 will not enable the battery charging operation, but will regulate EXT_B+ to B+ for phone operation.

At the same time U3000 (PM) starts the charge operation. U1000 (MSM) checks the BATT_FDBK line (Pin Y21) to verify that there is a valid charger connected. If a valid charger is not connected, U1000 will stop the charging operation using the SBI to U3000 (PM).

During charging operation U1000 (MSM) communicates with the battery through the BATT_SER_DT line to determine the battery charge state. When the battery reports that it is fully charged, U1000 (MSM) will put U3000 (PM) into trickle charge. If U1000 (MSM) does not get a valid read on the BATT_SER_DT line the handset will display “Invalid Battery” during power up and U1000 (MSM) will keep U3000 (PM) from charging the battery. This is to protect the user from any potential damage from overcharging the Lithium-Ion battery.

If at any time the temperature of the battery drops below -10c or above +60c as monitored by control line BATTERY_THERM to U3000 (PM) and U1000 (MSM). U3000 (PM) will stop charging the battery and U1000 (MSM) handset display will show "Unable to Charge". This is to protect the battery, phone, and user as at extreme temperatures the battery ROM could be reporting inaccurate charge state information to U1000 (MSM) and could cause potential damage to the battery.

Table 1 is a quick guide to the requirements for U3000 (PM) to enter into charging mode.

	Normal Charge	**Trickle Charge**
Battery Voltage	2.9VDC - 4VDC	2.9VDC< or >4.1VDC
EXT_B+ Voltage	3.3VDC - 5.6VDC	3.3VDC - 5.6VDC
Battery Temp.	-10c to +60c	-10c to +60c
BATT_FDBK	20K or 80K	20K or 80K
BATT_SER_DT	Valid ROM	Valid ROM

Table 1

A valid external charger will have an internal resistor connected to EXT_B+ line. For a mid-rate charger this is a 20K ohm resistor, for a high-rate charger this is an 80K ohm resistor. If BATT_FDBK line is left floating when EXT_B+ and ground are connected to the CE Connector, the unit will self power on. If the BATT_FDBK line has a resistance other than 20K or 80K, the unit will display "Unable to Charge".

Internal Audio Routing

The microphone is a press fit and is connected to J4100. The microphone audio is routed through C4100 to U1000 (MSM) as MIC1. U1000 (MSM) buffers the audio and routes it to the Mic_Amp2 network as MIOCOUT_P and MICOUT_N. The Mic_Amp2 network is used for filtering and bias control of the amplifier in U1000 (MSM). The output of Mic_Amp2 is MICFB_P and MICFB_N which is routed to U1000 (MSM).

The earpiece audio is routed from U1000 (MSM) to ESD Filter FL4000 as EAR10_P and EAR10_N. From FL4000 the audio is routed to J6000 as SPKR_P and SPKR_N. This audio is routed from J6000 via the hinge flex to the earpiece located in the flip assembly.

Speakerphone Audio Routing

Speakerphone transmit audio uses the microphone connected to J4100. The microphone audio is routed through C4100 to U1000 (MSM) as MIC1. U1000 (MSM) buffers the audio and routes it to the Mic_Amp2 network as MIOCOUT_P and MICOUT_N. The Mic_Amp2 network is used for filtering and bias control of the amplifier in U1000 (MSM). The output of Mic_Amp2 is MICFB_P and MICFB_N which is routed to U1000 (MSM).

Speakerphone receive audio is routed from U1000 (MSM) to amplifier U4500 as AUXO_N. When speakerphone mode is selected by the user control signal SPK_DRV_EN goes low enabling U4500. The amplified audio is routed to the speaker through LS4500 as VO_POS and VO_NEG.

Headset Jack

When a headset is plugged into the headset jack SWI (Pin2) is shorted to GND (Pin1). This caused Q4320 to shutoff and HEADSET_DET line to go high and is routed to U1000 (MSM) Pin AC11.

Headset microphone audio comes in on MIC (Pin 4) and is routed to U1000 (MSM) as MIC2_P and MIC2_N. MICBIAS and MICBIAS_HPH provide DC bias to the microphone and send/end detection circuitry. When a headset with a send/end pushbutton is used in the headset jack and the pushbutton is pressed. MIC (Pin 4) is connected to GND (Pin 1). This DC low is applied to in the inputs of U4300 (Pins 1and 3) and SEND_END_DET_N (pin 4) will go low. The SEND_END_DET_N is routed to U1000 (MSM).

Headset speaker audio is routed from the MSM as EAR20 to DC blocking capacitor C4326 to pin 3 of the headset jack.

U1000 (MSM)

The MSM is the microprocessor for the radio. U1000 (MSM) provides for all interface operations between the baseband, RF, display, keyboard, audio, and camera.

Audio interface

Microphone audio comes in on MIC1_P (Pin AD19) and MIC1_N (Pin AC18). This audio is routed back out as MICOUT_P (Pin AA18) and MICOUT_N (Pin AC19) to a filter network. The filtered audio comes in as MICFB_P (Pin AD20), MICFB_N (Pin AD21), MICIN_P (Pin AC20) and MICIN_N (Pin AA19). MICBIAS (Pin Y19) is used to provide DC bias to the microphone

Earpiece audio is routed from the MSM to ESD Filter FL4000 as EAR10_P (Pin AA16) and EAR10_N (Pin AD16).

Speakerphone audio is routed from the MSM as AUX0_N (Pin AA17) and the speakerphone enable in SPK_DRV_EN (Pin J20). The speakerphone is also used for the alert.

Headset microphone audio comes in as MIC2_P (Pin Y18) and MIC2_N (Pin Y17). MICBIAS (Pin Y19) and MICBIAS_HPH (Pin AD12) provide DC bias to the microphone and headset detection circuitry.

Headset speaker audio is routed from the MSM as EAR20 (Pin AD17)

HEADSET_DET (Pin AC11) is used to detect the presence of a headset in the headset jack. This will enable the MSM to route the audio to and from the headset. SEND_END_DET_N (Pin AA14) is used when the user has a headset with the built in send/end button and can answer and end a call with this signal.

CE Bus audio has AUXI_P (Pin AC17) and AUXI_N (Pin AD18) for incoming audio and AUXO_P (Pin Y16) for outgoing audio. SW_B_PLUS_EN (Pin A10) is used to provide B+ to external devices on the CE connector such as the FM stereo and MP3 players.

Camera interface

When the user selects camera mode, CAM_PWR_ON (Pin F24) will go high to turn on the camera. When the camera is on data is continuously transferred to the

MSM on data lines CAMIF_DATA0 – CAMIF_DATA7 (Pins A14, A15, B13, B14, D13, D14, E13, E14).

CAMIF_VSYNC (Pin K20), CAMIF_HSYNC (Pin K24), and CAMIF_PCLK (Pin L20) provide the MSM with sync clocks. CAM_PWRDWN (Pin AA12) is used by the MSM to power down the camera. GP_CLK (Pin E20) is routed to R1700 and will become the master camera clock CAMIF_CLKIN to the camera module.

Display interface

The MSM sends data to the Main and CLI display on data lines (PINS AA8, AA9, AC7, AC8, AC9, AD7, AD8, Y9). LCD_CS_N (Pin AA10) is used to select the main display and CLI_CS_N (Pin Y11) is used to select the CLI display. WE2_N is used to enable write time to both displays and DISPLAY_RS (Pin AC3) provides the clock to both the main and CLI display. RESOUT_N (Pin N21) is the reset for both displays. LED_EN (Pin G24) provides the display backlight control.

Keyboard interface

The MSM scans the keyboard and volume buttons with KEYBD_C0 – KEYBD_C6 (Pin A8, B9, B15, D9, D10, E10, E15) and detects which keypad or volume is activated with input lines KEYDB_R0 – KEYBD_R4 (Pins A11, A13, B11, D11, E12). Table 2 shows the grid layout for easy identification of a stuck signal. Flip detection is done by input signal FLIP_OPEN_DET (Pin U1). The input signal LIGHT_SENS_ADC (Pin W21) is used by the MSM to keep the backlights off when the background light detection switch (DS6020) detects strong ambient light.

	KEYBD_ R0	**KEYBD_ R1**	**KEYBD_ R2**	**KEYBD_ R3**	**KEYBD_ R4**
KEYBD _C0	SW_UP	SW_2		SW_ CSFT	Volume UP (S6000)
KEYBD _C1	SW_DN	SW_8	SW_CLR	SW_ RSFT	Volume Down (S6001)
KEYBD _C2	SW_ LEFT	SW_4	SW_ CARRIER	SW_ LSFT	Smart Switch (S6002)
KEYBD _C3	SW_RT	SW_6	SW_SND		Smart Voice (S6003)
KEYBD _C4	SW_9		SW_7	SW_3	
KEYBD _C5	SW_0	SW_ MENU	SW_5		
KEYBD _C6	SW_ POUND (#)		SW_ STAR (*)	SW_1	

Table 2

Memory interface

Address (Pins A4,A5, B4, B5, D1, D2, D5, D6, E1, F2, F4, F5, G1, G2, J1, J2, M1, M2, M4, M5, N2, N4, N5, R1) and Data (Pins B3, C2, E4, E5, E6, F1, G4,

G5, H1, H2, H4, H5, K1, K2, L4, L5) lines are used to transfer the program information to and from the U2000 (Flash) and U2100 (PSRAM). ROM1_CS_NO (Pin P2), and ROM1_CS_N1 (Pin T1) are used to select upper or lower memory locations in U2000 (Flash). RAM_CS_N (Pin P4) is used to select U2100 (PSRAM) memory. LB1_N (Pin P1) and UB1_N (Pin L1) are also used to select upper or lower memory blocks on U2000 (Flash) and U2100 (PSRAM). OE1_N (Pin P5) is the Output Enable (Read) and WE1_N (Pin J5) is the Write Enable to U2000 and U2100. WAIT_N (Pin K4) is an input from U2000 (Flash). PSRAM_CRE (Pin R4) is the output reset line to U2000 and U2100. CLK (Pin R2) is the clock to U2000 and U2100. If the code runs properly then MSM will set PS_HOLD (Pin D15) to keep U3000 (PM) running.

RF interface

When the RF IC's are lock onto the band and channel set by the MSM, SYNTH_LOCK (Pin Y14) will be a logic high. Intelligence data is sent to U210 (RFT) as TXI (Pin H20), TXQ (Pin D24), TXI_N (Pin G20) and TXQ_N (E24). Power control is maintained by monitoring RF_DETECT (Pin AB23) and changing control line TX_AGC_ADJ (Pin R24). In analog mode the RF is also monitored by input signal DAC_REF (Pin E23). TX_ON (Pin N24) enables U210 (RFT) to transmit. PA_R1 (Pin P21), PA_ON0 (Pin F24) and PA_ON1 (Pin C23) are used to select and enable the appropriate PA for transmit.

ANTENNA_UP (Pin D21) is used to detect the position of the antenna and RF_CONN_DET (Pin N23) is used to detect if an external antenna is connected to the phone.

FM_LNA_RANGE (Pin M21) is used to change the LNA setting in analog mode on U100. TRK_LO_ADJ (Pin L23) is used to adjust the TCXO to accommodate for any frequency drift of the RF circuit.

U3000 (PM)

The U3000(PM) regulates the voltages, charges the battery, and provides the clocks to the U1000(MSM).

When a logic low is detected on Pin 29 (KBDPWR_ON) or when EXT_B+ is applied to pin 1, U3000 starts the power up sequence. Initially PON_RESETB (pin 23) is held low to keep all other IC held in a reset condition so that the regulated voltages and system clocks can come up and stabilize. Regulated voltages VREG_MSMA (Pin 30), VREG_MSMC (Pin 32), VREG_MSMP (Pin 33), and VREG_TCXO (Pin 7) automatically power up during the turn on sequence. Regulated voltages VREG_SYNTH (Pin 9), VREG_RF_TX (Pin 19), and VREG_RF_RX (Pin17) are programmable regulators and are controlled by U1000 (MSM).

After 20mSEC PON_RESETB (Pin 23) will go high and buffered TCXO will be sent to U1000 (MSM) on Pin 5. The U1000 (MSM) has 200mSEC to set PS_HOLD (Pin 24) high. If U1000 (MSM) ever fails to keep this line high, U3000 will time out after 200mSEC and shut down. This is used so that if ever U1000 (MSM) freezes or if U1000 (MSM) never initializes, U3000 (PM) does not continue to drain the battery. This is also used to prevent the user from getting a false indication from the display that the unit is working (The display maintains the last loaded image in display memory).

The external sleep clock is connected to Pin 14 (Clock In) and Pin 15 (Clock Out). This external clock is buffered by U3000 (PM) and sent to U1000 (MSM) on Pin12 (SLEEP_CLK) and is used only during digital sleep time when the TCXO clock is powered down to save current.

When EXT_B+ is connected to the radio and is detected by Pin 1, CHG_CNTB (Pin 48) will be a variable DC output to control the current flow through Q3000 and Q3001. ICHARGE (Pin 47) and ICHARGE_OUT (Pin 46) provide a DC feedback to U3000 (PM) to monitor for over current conditions. If U3000 (PM) ever detects a voltage drop across R3011, U3000 (PM) will shut down preventing damage to the radio. When charging BAT_FETB (Pin 3) is a logic low enabling Q3002 to allow current flow to the battery. When the unit is operating from the battery BAT_FETB will also be a logic low to allow current to flow from the battery to the radio as B+. VBAT (Pin 2) is used to monitor the battery voltage to ensure that U3000 (PM) shuts down during low voltage conditions. Also U3000 (PM) provides an ADC count to U1000 (PM) which will update the battery icon on the display.

PHONE_THERM (Pin 40) and BATT_THERM (Pin 38) are inputs to U3000 (PM) which will provide an ADC count to U1000 (MSM) to monitor the temperature of the Phone and Battery respectively.

VIB_DRV (Pin 34) provides a logic high to enable the vibrator. D3003 is used to help filter the DC while the vibrator is active to prevent noise from feeding back into the U3000 (PM) and causing noise on the regulated power lines.

KEYBD_DRV (Pin 20) is used to control the backlights on the keyboard. This will be a logic high when the keyboard backlights are on.

RECEIVER THEORY OF OPERATION

Antenna RF path

When the phone is operating in normal user mode without a Car Kit, external antenna, or test equipment attached to the RF connector jack (J10), the antenna is used to couple the incoming RF to the PCB. This RF is directly coupled from the antenna to Contact M10. C10, L10, L11, and L16 make up an antenna matching circuit and C16 is a DC blocking cap. The RF is routed through J10 and through DC blocking cap C330 to Triplexer FL330.

The network L13, L12, R10, and R14 make up the RF Connection Jack Detection Circuit. During normal operation (No RF plug attached to J10), there is a ground path from L13 through J10 and L12 which places a logic low on the RF_CONN_DET line (R10 and R14). This logic low is used by the MSM (U1000) to cut back the TX RF power levels when the antenna is in the retracted (Down) position (Detected by mechanical switch S10). C15, C13, L12, and L13 provide for RF filtering so that the RF does not affect VREG_RF_TX or FR_CONN_DET lines and cause desense or spurious emissions.

If a connector is attached to J10 the ground path from L13 is broken and VREG_RF_TX is applied to the RF_CONN_DET line as a logic high. This will cause the MSM (U1000) to disable the RF Cutback routine and ignore the position of the antenna as the RF is being directed to an external load.

800MHz CDMA and Analog path

From Triplexer FL330 the 800MHz signal is routed to Duplexer FL305. C305, L305, and L306 make up a matching network between FL330 and FL305.

The receive RF is routed from pin 5 of FL305 through matching network C100, C101, and L100 to the input of the RF Low Noise Amplifier (RFL) U100 (Pin 1). At a predetermined level the LNA with amplify the signal (See U100 RFL theory for table). The output on Pin13 is applied to the input of FL102 though matching inductor L103. L104 is an RF choke. The output of FL102 is a balanced output (Pins 8 and 9) and is applied to the Balance network C105, C106, C107, L105, L106 and L107 and into receiver IC U130.

1900MHz PCS path

From Triplexer FL330 the 1900MHz signal is routed to Duplexer FL325. C325, C331, and L325 make up a matching network between FL330 and FL325.
The receive RF is routed from pin 5 of FL325 through matching network C120, C121, and L121 to the input of the RF Low Noise Amplifier (RFL) U100 (Pin 4). At a predetermined level the LNA with amplify the signal (See U100 RFL theory for table). The output on pin 11 is applied to the input of FL102 through matching network C128 and L123. L124 is an RF choke. The output of FL102 is a balanced output (Pins 6 and 7) and is applied to the Balance network C125, C126, C127, L125, L126, and L127 and into the receiver IC U130.

GPS Path

From Triplexer FL330 the GPS signal is routed to the U130 (RFR) IC (Pin 12) through matching network C111, C112, L112.

U100 (RFL)

The U100 (RFL) IC includes two LNA circuits, one optimized for the Cellular band and one for PCS. The two LNAs are dedicated to different frequency bands; the CLNA supports Cellular bands while the PLNA supports PCS bands. The PLNA gain is always controlled via the Serial Bus Interface (SBI) with three valid settings: Max, Mid, and Low. Three CLNA gain states are also controlled via the SBI for CDMA signal reception, but only two gain states are available for FM operation (Max and Low). When operating in the Cellular-FM mode, the CLNA gain is controlled by a dedicated MSM signal applied to pin 6 (FM_STEP) rather than the SBI.

The IC operating mode and LNA bias currents are automatically adjusted via software to minimize DC power consumption. The IC is placed in Sleep, Rx, and Rx/Tx modes depending upon the handset's status, with LNA bias current also adjusted to meet RF performance requirements with minimal power dissipation when active.

	Gain (dB)		
	Low	Mid	High
Analog	-20dB	N/A	+13dB
800 CDMA	-20dB	-2dB	+15dB
1900 PCS	-20dB	-9dB	+15dB

Table 1

L102, L122, and R102 provide for gain bias of the U100. L102 is for the 800MHz LNA bias and L122 is for the PCS LNA bias. R102 sets the bias of both LNA's in U100.

U130 (RFR)

The U130 (RFR) IC is a zero-IF receiver IC that converts the incoming RF into analog baseband by using an external VCO signal (From Y240) that is 2x the RX frequency for 800MHz operation and 1x+200MHz for 1900MHz operation. For GPS operation the U130 uses an internal VCO frequency that is adjusted by the GVCO_Tune Line which comes from U210 (RFT) IC. The GVCO_Tune line is also used to adjust the frequency of Y240. The Analog baseband signal (RXI and RXQ) is used by the U1000 (MSM) IC to produce all required receive functions.

The U130 has an internal PLL circuit that is used to ensure that the U130 is lock onto the required channel in either the 800MHz or 1900MHz operation. This PLL is programmed by the U1000 (MSM) through the SBI lines and the second input to the PLL is the External VCO frequency from Y240. U250 (TCXO) provides U130 with a stable clock and if the PLL is locked then U130 will route the External VCO to U210 (RFT) IC on the LO_Out line (Pin 19).

Y240

Y240 is a VCO module that provides U130 (RFR) IC with the required frequency to down mix the incoming RF into U130. This VCO is tuned by adjusting the DC input line GVCO_Tune. The device can be turned off for current savings by placing logic low on pin 3 (EXT_VCO_EN) from the U1000 (MSM) IC.

U250 (TCXO)

U250 is a precision 19.2MHz reference oscillator that provides the reference frequency for the entire radio. This is used by both the RF and Baseband. The output frequency can be adjusted to compensate for drift and component age of the device by adjusting DC voltage input (TRK_LO_ADJ) from U1000 (MSM).

TRANSMIT THEORY OF OPERATION

During transmit time, the U1000 (MSM) IC provides analog baseband signals TXI and TXQ to the U210 (RFT) IC. This data is up mixed into the transmit frequency using a Zero-IF setup. The output frequency of the U210 (RFT) IC will be the transmit frequency at the antenna.

800MHz path

The U210 (RFT) IC produces the 800MHz RF on output pin 23 (CELL_RFT). This is applied to bandpass filter FL300 through DC blocking capacitor C200. The output of FL300 is applied to the 800MHz amplifier U300 (Pin 4) through the DC blocking capacitor C300. U300 provides approximately 25dB of gain to the signal (See U300 Theory of Operation for table) and outputs the signal to Coupler U305 through matching circuit C301, L301 and L302. The RF is passed through the non-coupled output of U305 to Duplex Filter FL305. The RF is passed to FL330 through Matching circuit C305, L305 and L306 to Triplexer FL330. The RF is passed to J10 through DC blocking capacitor C330. If there is no RF plug attached to J10, the RF will be passed to the antenna through antenna matching circuit C10, C11, C16, L10, L11 and L16 to antenna contact pad M10. The RF is directly coupled to the antenna from contact pad M10.

1900MHz path

The U210 (RFT) IC produces the 1900MHz RF on output pin 27 (PCS_RFT). This is applied to bandpass filter FL320 through DC blocking capacitor C220. The output of FL320 is applied to the 1900MHz amplifier U320 (Pin 4) through the DC blocking capacitor C320. U320 provides approximately 25dB of gain to the signal (See U320 Theory of Operation for table) and outputs the signal to Coupler U325 through matching circuit C321, C327 and L322. The RF is passed through the non-coupled output of U325 to Duplex Filter FL325. The RF is passed to FL330 through Matching circuit C325, C331 and L325 to Triplexer FL330. The RF is passed to J10 through DC blocking capacitor C330. If there is no RF plug attached to J10, the RF will be passed to the antenna through antenna matching circuit C10, C11, C16, L10, L11 and L16 to antenna contact pad M10. The RF is directly coupled to the antenna from contact pad M10.

Power Control

The power control circuit consists on U305, U325, RT349, U340 and associated parts. There are 3 types of power control on the V26x product:

CDMA/PCS OPEN LOOP
CDMA/PCS CLOSED LOOP
ANALOG

During the initial registration, the unit is in Open Loop control the MSM will subtract the Received Signal Strength (RSSI) from -73dBm (CDMA) or -76dBm (PCS) to

generate the initial TX Power level. (Example: If the CDMA RSSI = -73dBm the TX out put power will be 0dBm TX= -73-(RSSI) or TX = -73-(-73)).

In Closed Loop control the base station is controlling the TX output by sending either up commands or down commands in the RX data which U1000 (MSM) will apply to the TX system. The power detect circuit is used by the MSM to ensure that the TX power does not exceed +/- 10dB of the expected TX output power using the open loop equation.

In Analog Mode U1000 (MSM) will set the TX power to power step 2. During a call the base station monitors the Supervisory Audio Tone (SAT) and the incoming RSSI and will direct the MSM to change power steps. The power detect circuit is used to monitor the TX power to ensure that the TX power does not exceed the current power step setting.

Thermistor RT349 is used to detect the PCB temperature and provide a DC feedback to the MSM. The MSM will use the temperature feedback and adjust the TX power out of the PA's to maintain power control.

U340 converts the sampled RF from couplers U320 and U325 into the DC signal RF_Detect.

U210 (RFT)

During normal operation, U1000 (MSM) will program U210 (RFT) to the desired band and channel through the SBI interface (Pins 3-5). This will program the GCVO tune line (Pin 19) which provides a DC steering voltage to both the External VCO (Y240) and to U130 (RFR) IC.

The U210 (RFT) contains an internal PLL circuit that uses the SBI data, RXLO input (Pin 15) and TCXO (Pin 8) to validate that the RXLO is on the correct frequency. The TCXO input is the reference frequency and is used to maintain proper sampling rate by the PLL. If the RXLO and the programmed band/channel information loaded into the internal PLL match, then Synth_Lock (Pin 6) will be a logic high. The Synth_Lock signal is an output to U1000 (MSM) and is used by the MSM as a verification that both U130 (RFR) and U210 (RFT) are on the correct channel. If Synth_Lock is low, U1000 (MSM) will not allow the unit to transmit.

During transmit time TX_ON (Pin 2) will be a logic high (From U1000 (MSM)) and U1000 (MSM) provides the intelligence (Data) to U210 (RFT) through TXI and TXQ (Pins 33 – 36). This data is mixed with the RXLO signal to produce the modulated transmit RF signal that will be sent to either the 800MHz PA (Pin 23) or the 1900MHz PA (Pin 27).

Power control is maintained by the MSM by adjusting TX_AGC_ADJ into the RFT IC (Pin 30). The output line DAC_REF (Pin 37) is a variable DC line to the MSM which is used to monitor the output RF from U210 (RFT) in Analog (FM) mode.

As the RXLO is able to provide the required TX frequency, the TX charge pump is not required and has a direct DC input for biasing of an internal PLL. Any modulation on this line will cause spurious emissions and the phone to drop the call as the signal would "drift".

U300 (800MHz PA)

U300 is a constant gain PA with high and low gain mode. The gain mode is controlled by U1000 (MSM) through signal PA_R1 (Pin 2). Transmit RF is applied to Pin 4 from FL300 and the unit is amplifying when VCC (Pin 5, 6) and VREG_RF_TX (Pin 1) is applied to the device. The amplified RF outputs the device on pin 8 to U305.

When PA_R1 is high, the PA is in low gain mode: Gain = 24dB and the maximum RF output = 18dBm. When PA_R1 is low, the PA is in high gain mode: Gain = 28dB and the maximum RF output = 31dBm

Q300 is a voltage buffer to isolate any logic noise from the PA. When PA_ON0 is high, VREG_RF_TX is applied to pin 1 of the PA.

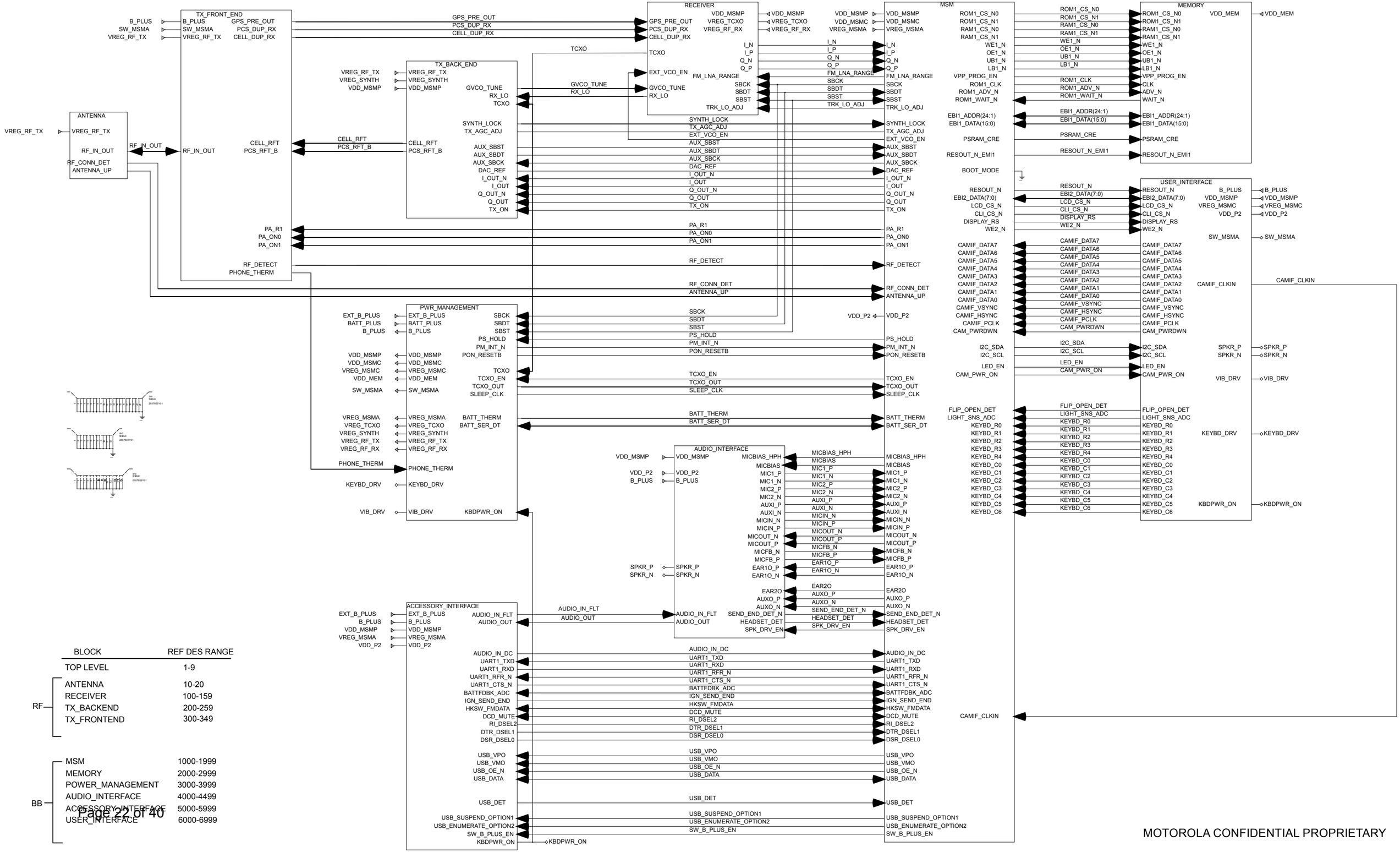
U230 (1900MHz PA)

U320 is a constant gain PA with high and low gain mode. The gain mode is controlled by U1000 (MSM) through signal PA_R1 (Pin 4). Transmit RF is applied to Pin 2 from FL320 and the unit is amplifying when VCC (Pin 1, 10) and VREG_RF_TX (Pin 5) is applied to the device. The amplified RF outputs the device on pin 8 to U325.

When PA_R1 is high, the PA is in low gain mode: Gain = 25dB and the maximum RF output = 28.5dBm. When PA_R1 is low, the PA is in high gain mode: Gain = 26dB and the maximum RF output = 28.5dBm

Q320 is a voltage buffer to isolate any logic noise from the PA. When PA_ON1 is high, VREG_RF_TX is applied to pin 5 of the PA.

V260/V262/V265 Block Diagram

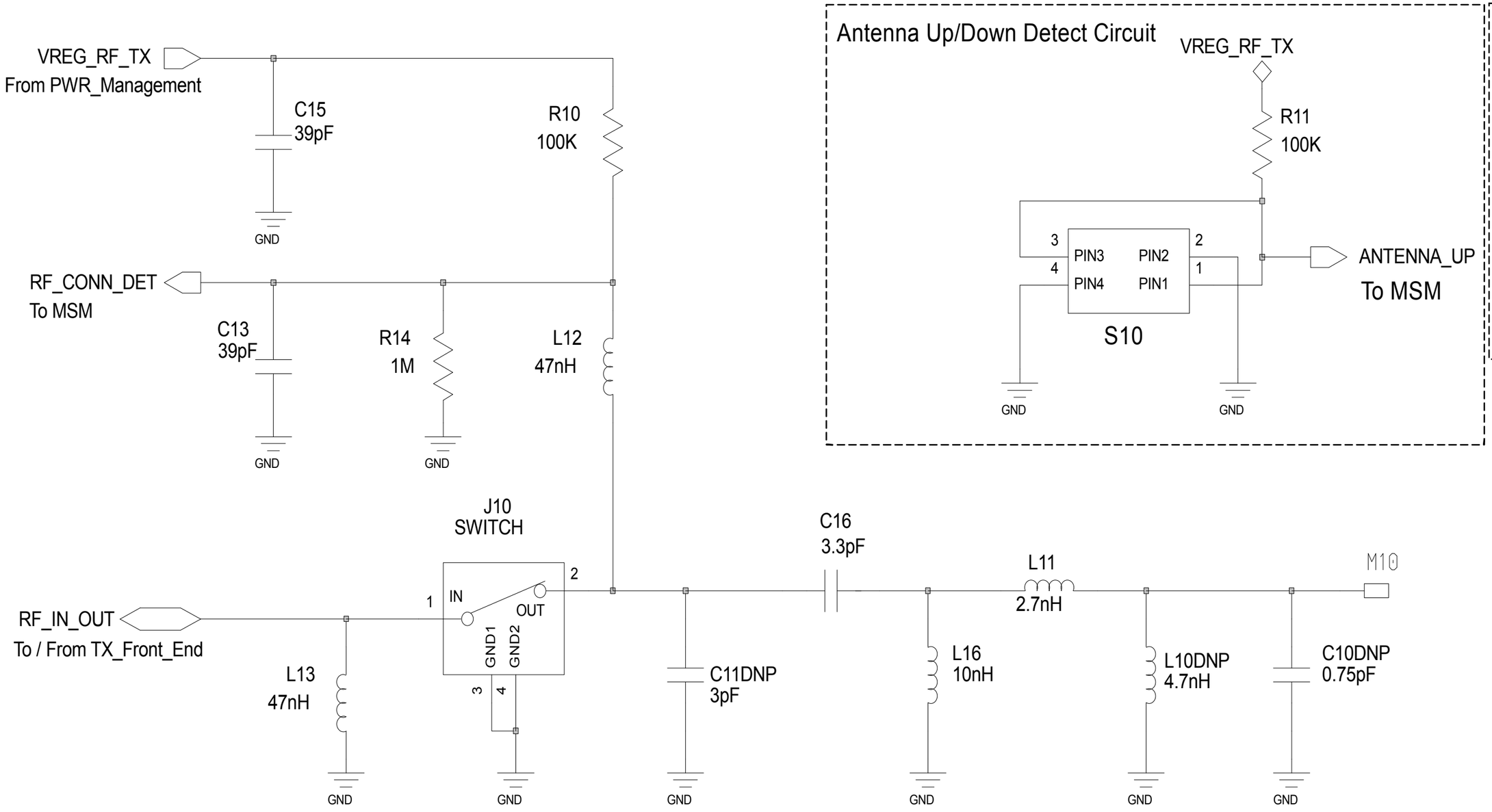


BLOCK	REF DES RANGE
TOP LEVEL	1-9
ANTENNA	10-20
RECEIVER	100-159
TX_BACKEND	200-259
TX_FRONTEND	300-349
MSM	1000-1999
MEMORY	2000-2999
POWER_MANAGEMENT	3000-3999
AUDIO_INTERFACE	4000-4499
ACCESSORY_INTERFACE	5000-5999
USER_INTERFACE	6000-6999

RF

BB

ANTENNA
REF 10-20



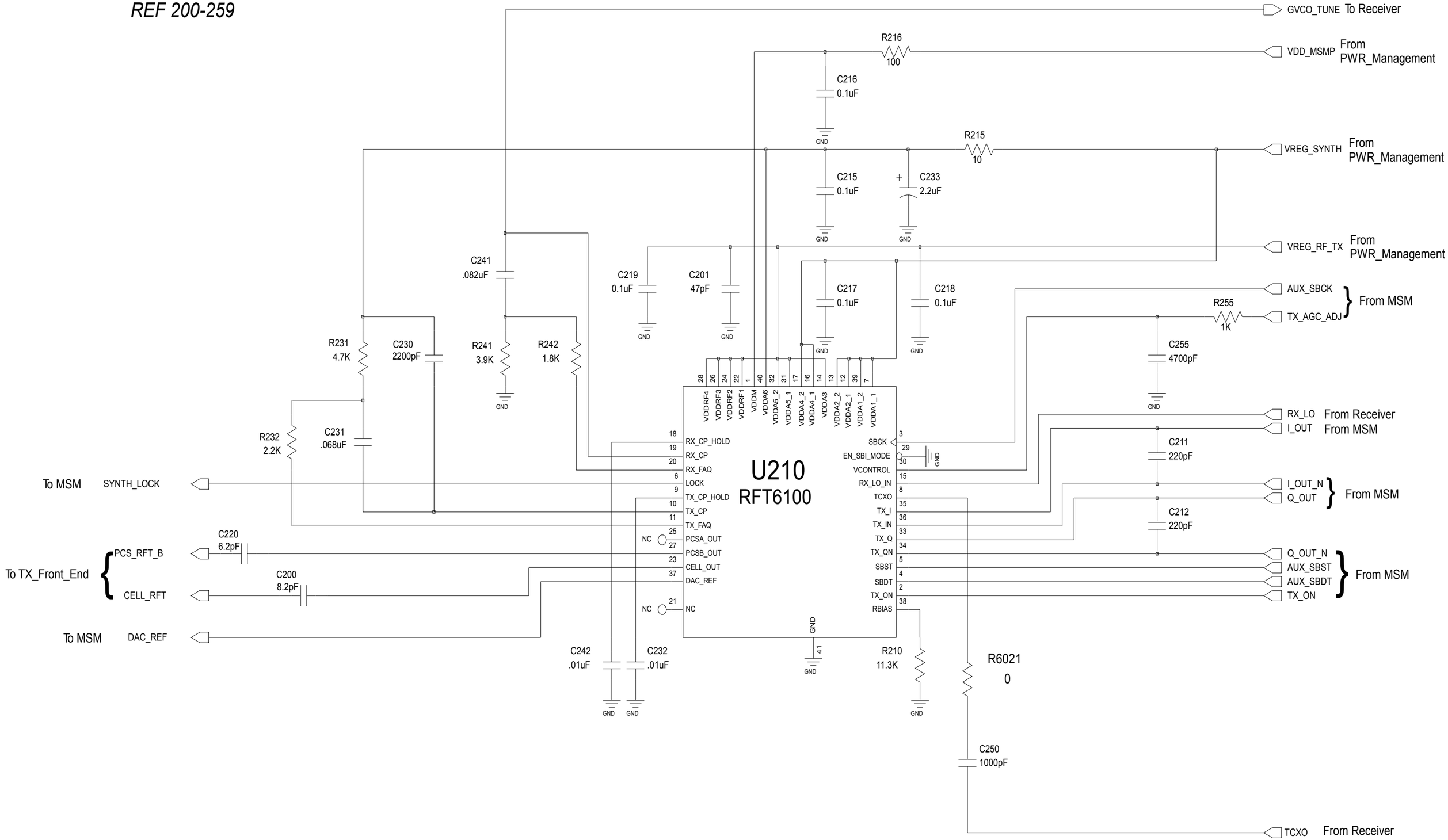
L13 provides the logic low to RF_CONN_DET when the RF is directed to the antenna (M10). When an RF plug is connected to J10 this ground path is broken and logic goes high.

From PWR_Management { VDD_MSMP, VREG_TCXO
From MSM TRK_LO_ADJ
From MSM SBCK
VREG_RF_RX
From PWR_Management
From TX_Front_End CELL_DUP_RX
From MSM FM_LNA_RANGE
From TX_Front_End PCS_DUP_RX
From TX_Front_End GPS_PRE_OUT
From MSM { SBST, SBDT
From MSM EXT_VCO_EN

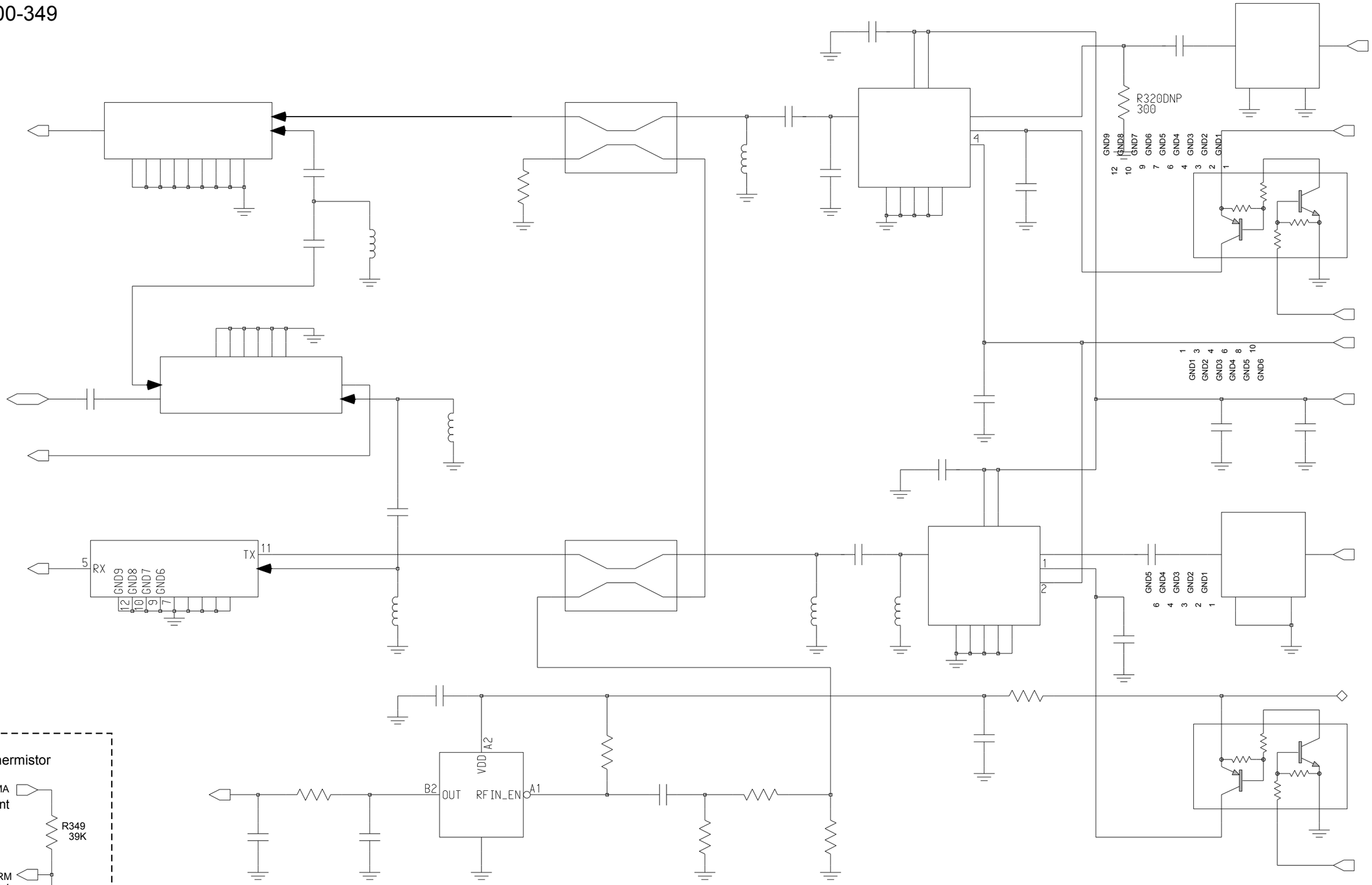
R250 100
R251 51
C251 1000pF
C252 .01uF
C254 .01uF
C253 0.1uF
U250 VCON OUTPUT VCC GND 19.2MHz
TCXO To TX_Back_End PWR_Management
C131 1000pF
R115 100
C130 1000pF
L115 47nH
C129 0.1uF
C104 100pF
C124 100pF
C116 100pF
R104 22
R124 22
L104 22nH
L124 10nH
L103 12nH
C101 39pF
L100 8.2nH
C118 0.1uF
C100 .01uF
U100 RFL6000
SBCK CLNA_IN PLNA_IN FM_STEP SBST SBDT VDDM VDDA CLNA_OUT PLNA_OUT CLNA_BIAS PLNA_BIAS R_BIAS GND1 GND2 GND3 GND4
L123 2.7nH
C128DNP 1pF
L121 3.9nH
L122 18nH
C122 100pF
C120 1pF
C121 12pF
L102 82.0nH
R102 5.76K
FL102
CELL_IN PCS_IN CELL_OUT_POS CELL_OUT_NEG PCS_OUT_POS PCS_OUT_NEG GND1 GND2 GND3 GND4
C105 6.2pF
L107DNP 15nH
C107 0.1uF
L105 10nH
L106 10nH
C106 6.2pF
C125 6.2pF
L127 10nH
C127 0.1uF
L125 3.9nH
L126 3.9nH
C126 6.2pF
C137 0.1uF
C134 47pF
C139 47pF
C135 0.1uF
R135 100
R136 10
C145 47pF
E130
U130 RFR6000
TCXO SBCK CELL_INP CELL_INM PCS_INP PCS_INM GPS_INM GPS_INP LO_INM LO_INP GVCO_TUNE SBST SBDT R_BIAS
VDDA1_1 VDDA1_2 VDDA1_3 VDDA1_4 VDDA2 VDDA3 VDDA4_1 VDDA4_2 VDDM
LO_OUT RX_IM RX_IP RX_QM RX_QP NC1 NC2
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_SLUG
RX_LO To TX_Back_End
I_N To MSM
R133 5.76K
I_P
Q_N } To MSM
R134 5.76K
Q_P To MSM
L112 6.8nH
C112 1.5pF
C113 100pF
R131 11.3K
C133 47pF
C111 15pF
C132 47pF
GVCO_TUNE From TX_Back_End
R243 1K
C243 0.1uF
C240 5600pF
Y240 VEN VTUN VCC OUT GND1 GND2 GND3 GND4 1752MHz
C244DNP 3.9pF
C245DNP 3.9pF
C146 1.0uF
C144 10.0uF

TX BACK END

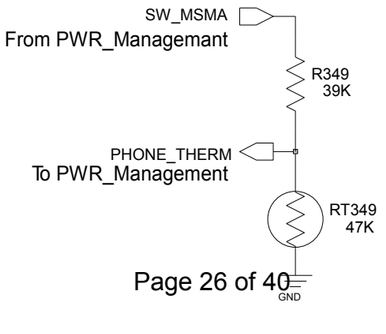
REF 200-259



TX FRONT END
REF 300-349



Phone Thermistor



To Audio_Interface
Acc_Interface
User_Interface

From PWR_Management VREG_MSMA — E1200 — C1201 .01uF, C1202 .01uF, C1203 .01uF, C1204 .01uF, C1205 .01uF — VDD_P2 — VDD_A

E1201 — SHORT_RES0402 — C1206 .01uF — VDD_PLL

From PWR_Management VDD_MSMP — E1100 — C1104 .01uF, C1105 .01uF, C1106 .01uF, C1107 .01uF — VDD_P3P4

E1002 — C1013 0.1uF

From PWR_Management VDD_MSMC — E1001 — C1011 0.1uF, C1012 .01uF, C1014 .01uF — VDD_P1

E1000 — C1000 4.7uF, C1001 0.1uF, C1002 0.1uF, C1015 .01uF, C1016 .01uF, C1003 .01uF, C1004 .01uF — VDD_C

E1005

Y1000 is for USB communication IS not used by the MSM for any other operation. If there is a USB failure and serial communication works. Verify Y1000 is working.

Y1000
48.0MHz

TCXO_OUT
JTAG_TCK
JTAG_RTCK
SLEEP_CLK
NC

WDOG_EN
R1004dnp
Place Outside Shields
0

Place a 0 ohm resistor at R1004 to keep MSM running during Turn on failures. This will allow analyzing of the logic circuits.

KEYBD_R4
KEYBD_R3
KEYBD_R2
KEYBD_R1
KEYBD_R0
PON_RESETB
RESOUT_N
RESOUT_N_EMI1
BOOT_MODE
NC
NC

UART1_CTS_N
UART1_RFR_N
JTAG_TMS
JTAG_TRST_N

LB1_N
UB1_N
WE1_N
OE1_N
NC
NC
WE2_N
NC

RF_DETECT
NC
BATT_THERM
BATTFDBK_ADC
LIGHT_SNS_ADC
NC

USB_VPO
USB_VMO
USB_OE_N
USB_DATA
NC
NC
UART1_TXD
UART1_RXD
NC
NC
AUDIO_IN_DC
AUX_SBCK
NC
NC
AUX_SBDT
AUX_SBST
I_P
I_N
Q_P
Q_N
FM_LNA_RANGE
JTAG_TDI

U1000
MSM6100

CONNECTED FOR BGA ANCHORING

CONNECTED FOR BGA ANCHORING

EXT_VCO_EN
RF_CONN_DET
USB_DET
GP_CLK
JTAG_TDO
RAM1_CS_N1
HEADSET_DET
LCD_CS_N
LCD_EN
TP1002
CLI_CS_N
USB_ENUMERATE_OPTION2
ROM1_CS_N1
USB_SUSPEND_OPTION1
RAM1_CS_N0
ROM1_CS_N0
ROM1_CLK
PSRAM_CRE
ROM1_ADV_N
ROM1_WAIT_N
EBI1_ADDR(24:1)
R1400 680
C1400 0.1uF
TRK_LO_ADJ
FLIP_OPEN_DET
NC
DISPLAY_RS
EBI1_DATA(15:0)
EBI2_DATA(7:0)
ANTENNA_UP
SPK_DRV_EN
NC
CAM_PWR_ON
LED_EN
MICOUT_P
MICOUT_N
EAR1O_P
EAR1O_N
EAR2O
AUXO_P
AUXO_N
MICBIAS

VDD_MSMP
R1600 2.2K
R1601 2.2K
I2C_SCL
I2C_SDA

VDD_MSMP
C1008 0.1uF
R1407 10K
C1403 .01uF
DAC_REF
SYNTH_LOCK
PA_R1
R1500 1K
C1500 .01uF
TX_AGC_ADJ

GP_CLK
R1700
C1700dnp 12pF
CAMIF_CLKIN

JTAG TESTPOINTS

VDD_MSMP
TP1200
TP1201 PS_HOLD
TP1202 WDOG_EN
TP1203 JTAG_TCK
TP1204 JTAG_RTCK
TP1205 JTAG_TDO
TP1206 JTAG_TDI
TP1207 JTAG_TMS
TP1208 JTAG_TRST_N
TP1209 PON_RESETB
TP1210

See Block Diagram for signal routing

VDD_MEM
From PWR_Management

R2032
0

Q2030DNP

VPP_PROG_EN
From MSM

R2031DNP
100K

R2030DNP
100K

C2000
0.1uF

C2001
0.1uF

C2002
0.1uF

C2003
0.1uF

C2100
0.1uF

C2101
0.1uF

U2000
Synchronous
Burst
NOR Flash

F_VPP
WAIT
F_WP
ADV
F_RST
F1_CE
F2_CE
F3_CE
F1_OE
F2_OE
F_WE
R_LB
S_CS2
R_WE
P1_CS
R_UB
R_OE
S_CS1
P2_CS
P_VCC
S_VCC
P_MODE
CLK
F1_VCC2
F1_VCC1
F2_VCC2
F2_VCC1
VCCQ3
VCCQ2
VCCQ1

To MSM WAIT_N
From MSM ADV_N
ROM1_CS_N0
ROM1_CS_N1
CLK From MSM

EBI1_DATA(15:0)
To / From MSM

From MSM LB1_N
WE1_N
RAM1_CS_N1
UB1_N
OE1_N

From MSM RESOUT_N_EMI1
R2017DNP
0

From MSM PSRAM_CRE
R2018
0

RESOUT_N_EMI1
R2019DNP
0
PSRAM_CRE
R2020
0

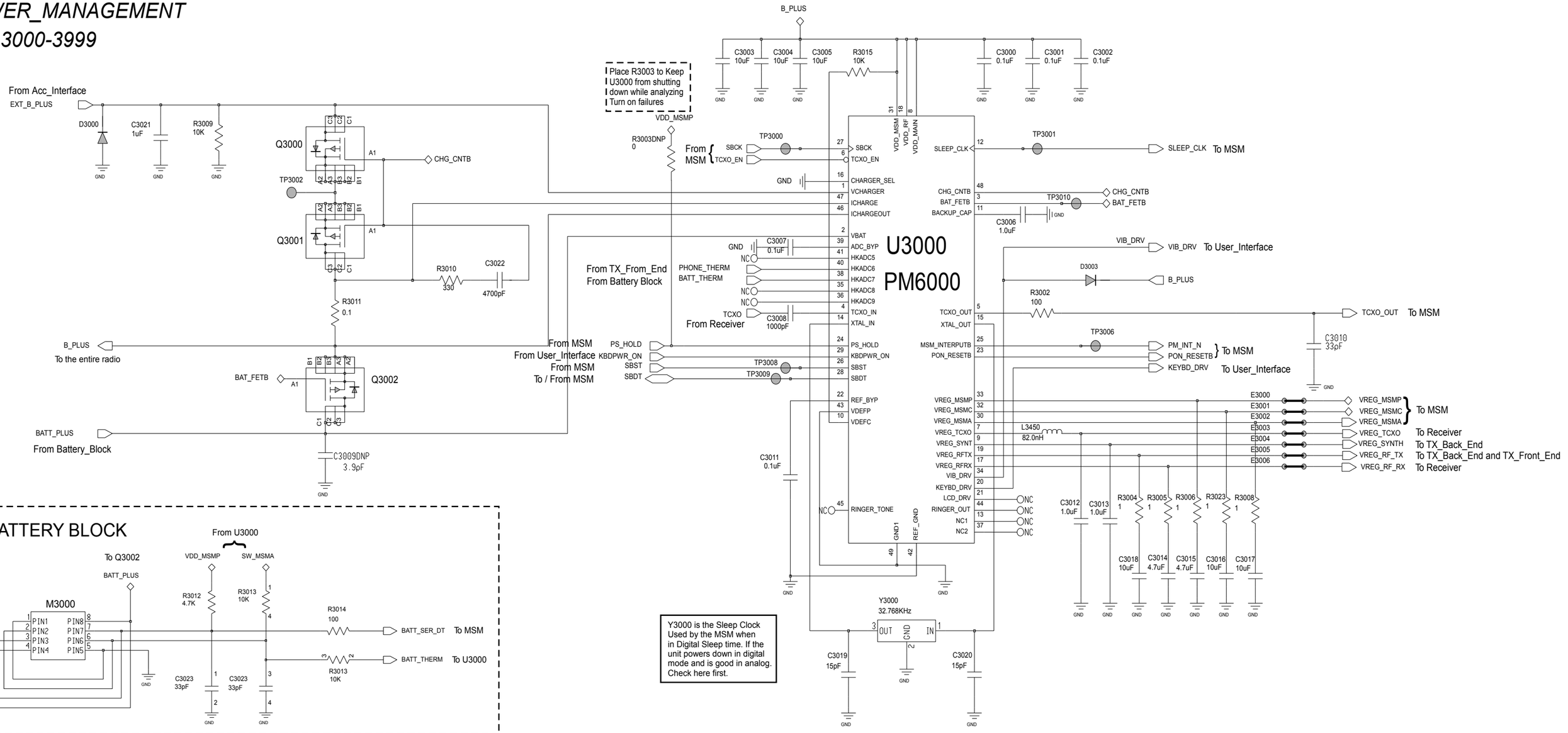
EBI1_ADDR(24:1)
From MSM

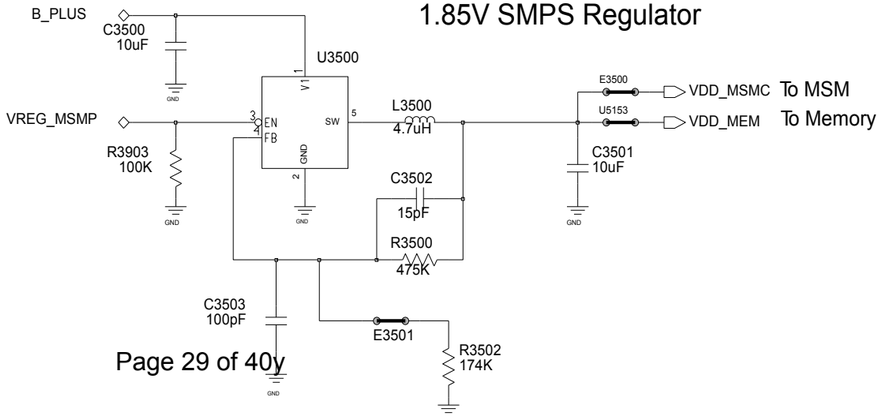
U2100
Synchronous
Burst
PSRAM

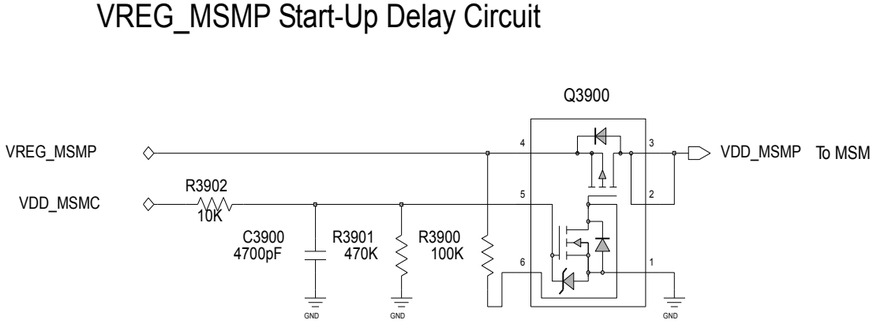
CLK
ADV_N
WE1_N
RAM1_CS_N0
UB1_N
LB1_N
OE
WAIT
OE1_N
WAIT_N
EBI1_DATA(15:0)

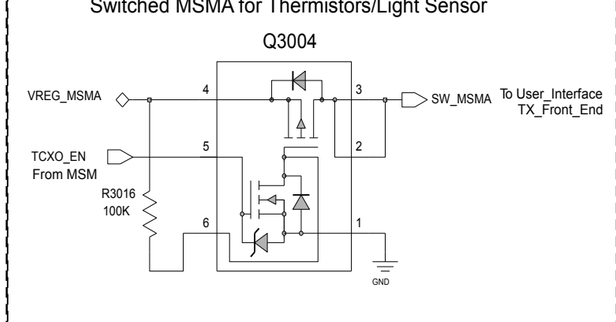
MEMORY
REF 2000-2999

POWER_MANAGEMENT
REF 3000-3999

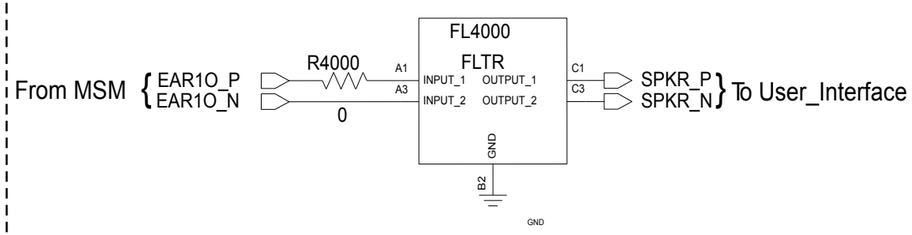




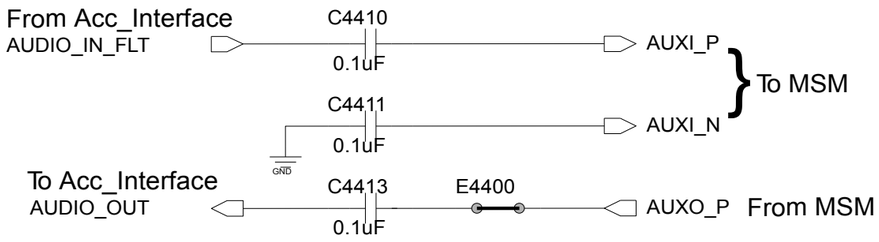




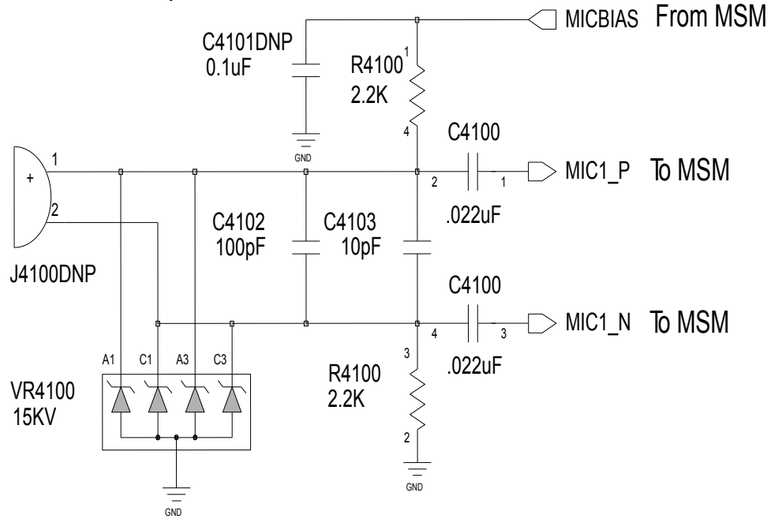
Internal SPKR ESD Protection



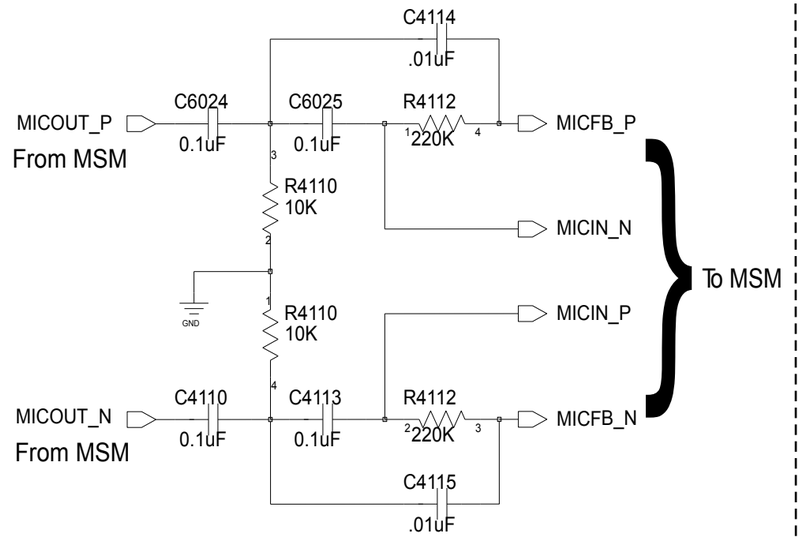
CE Bus Audio



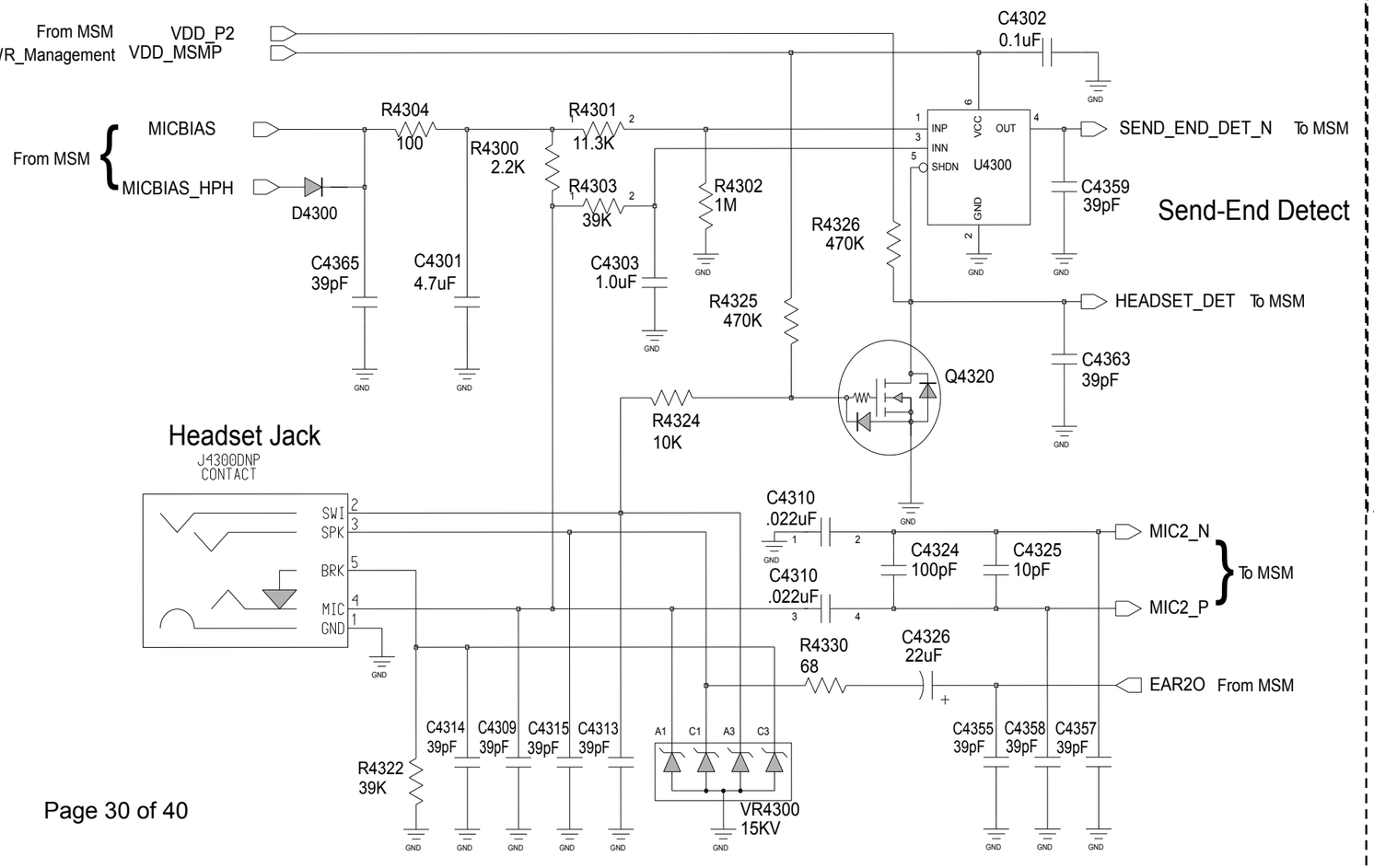
Internal Microphone



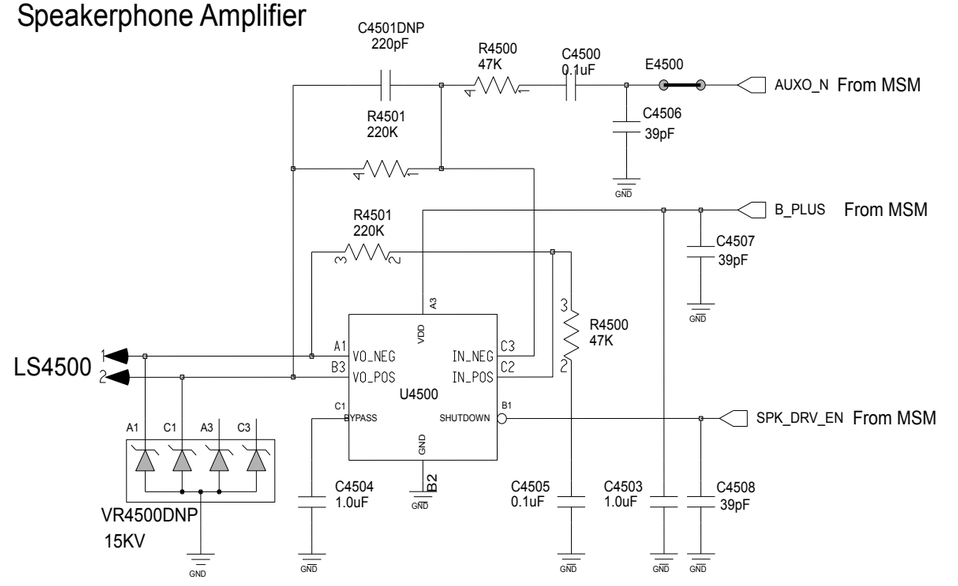
Mic Amp 2 - Two Pole Butterworth



Headset Jack Audio

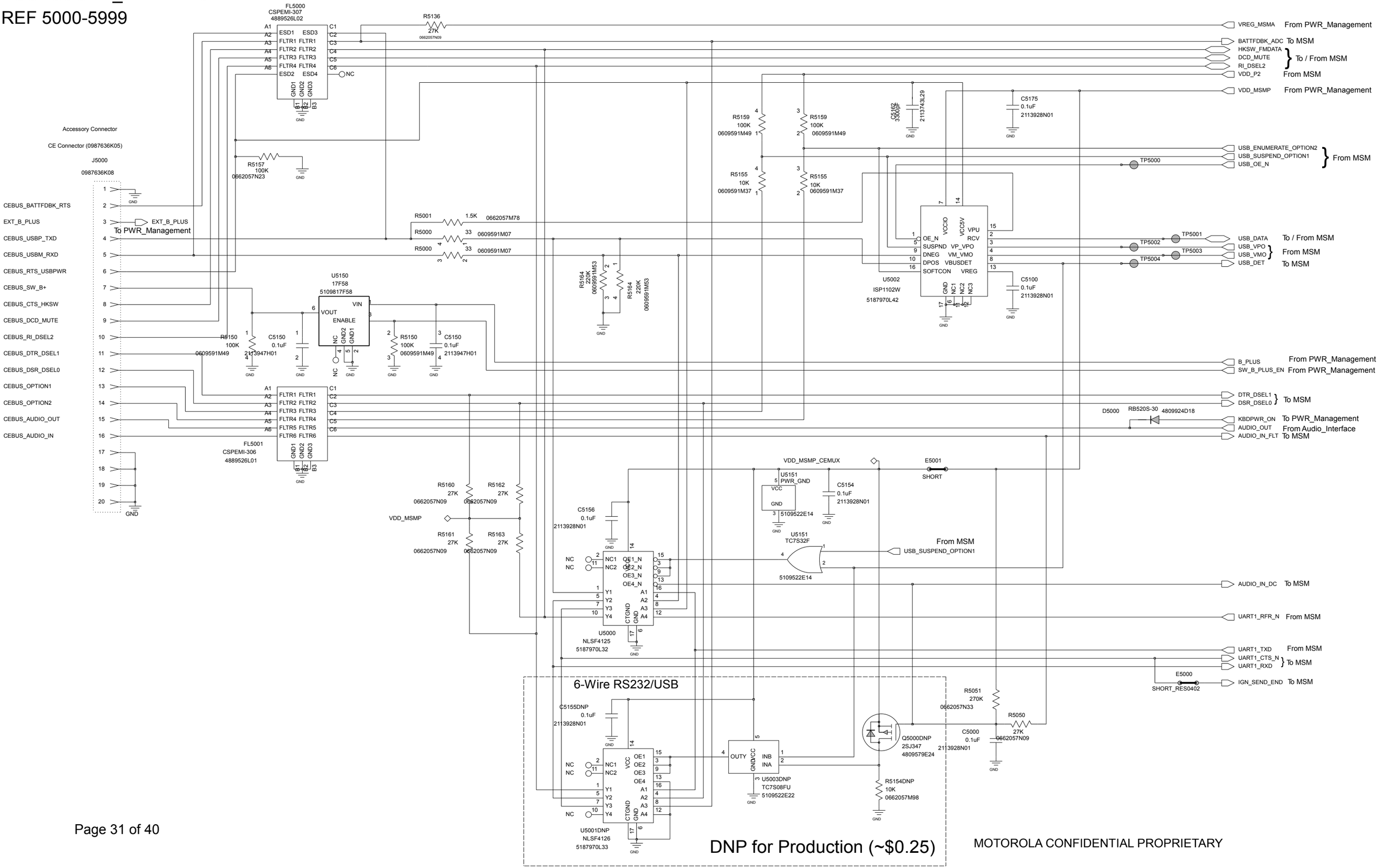


Speakerphone Amplifier



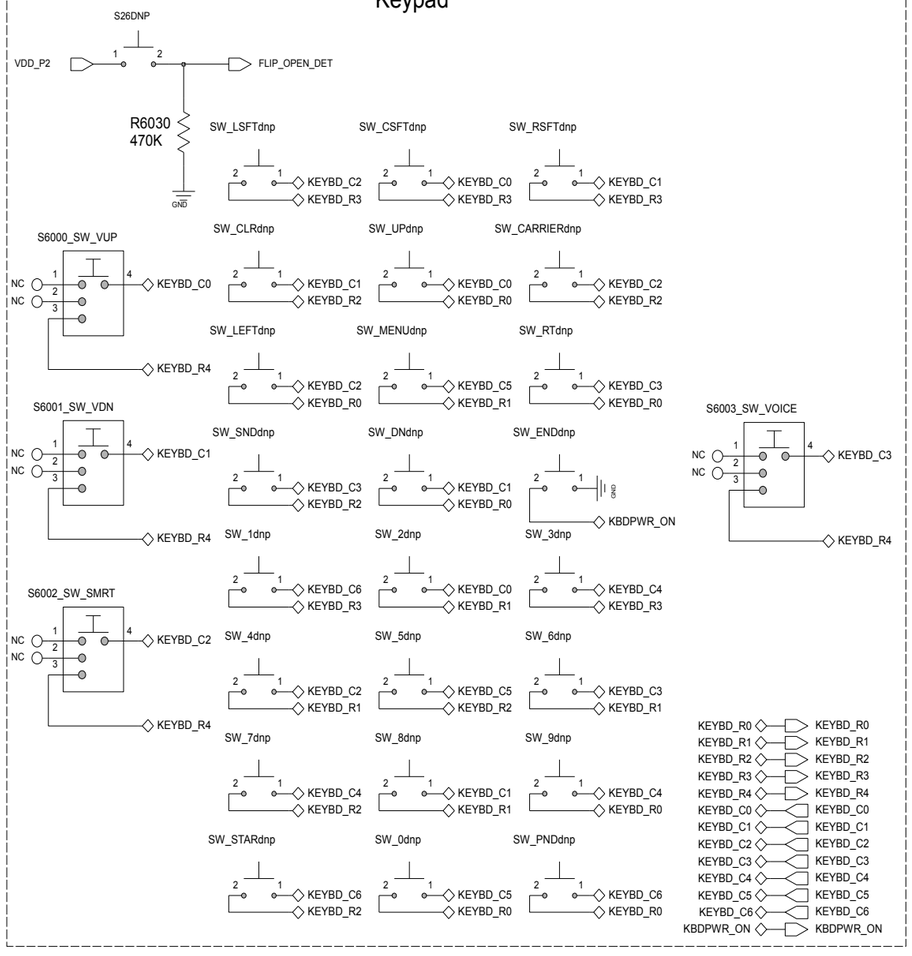
AUDIO INTERFACE
REF 4000-4499

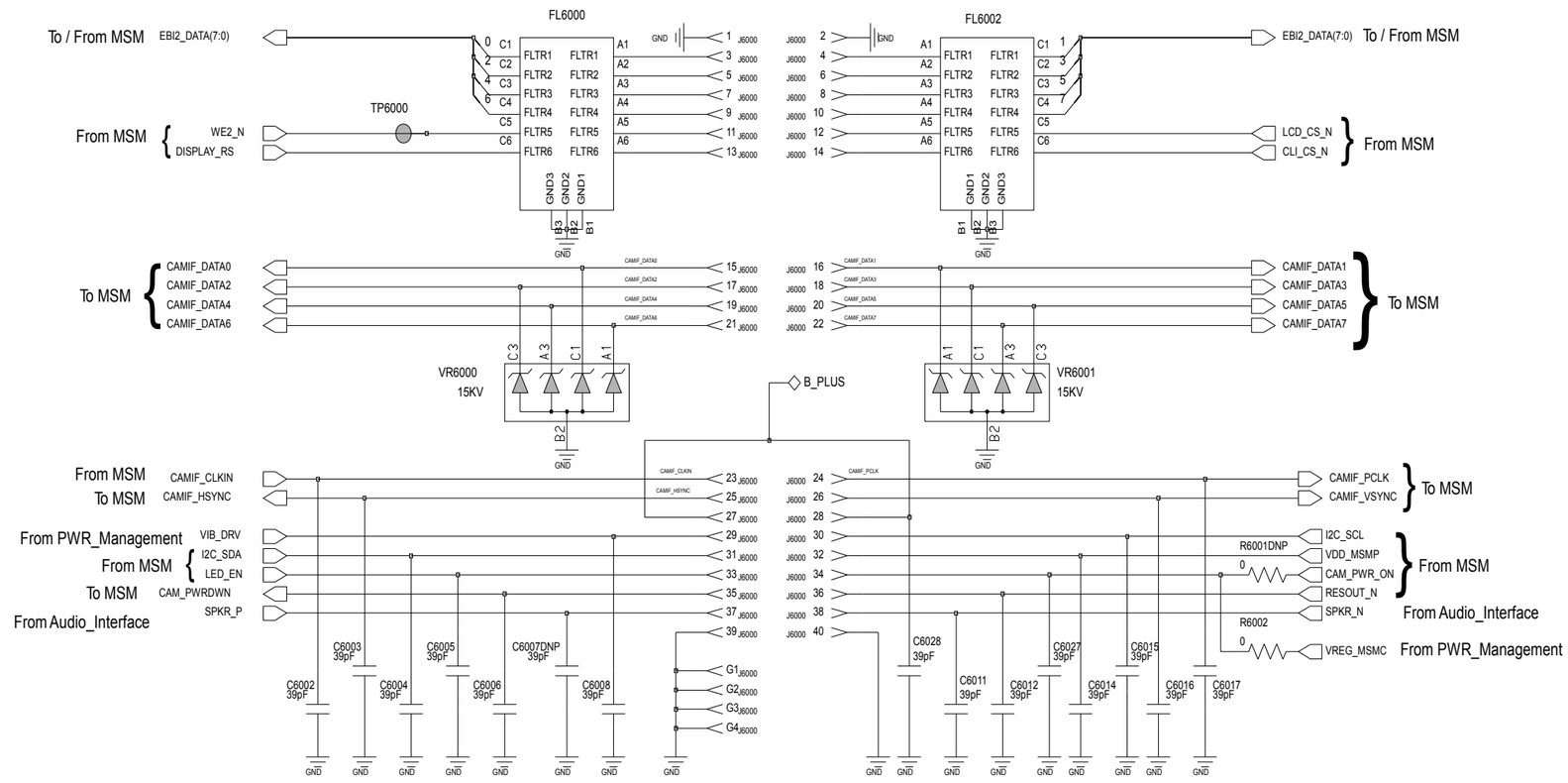
ACCESSORY_INTERFACE
REF 5000-5999



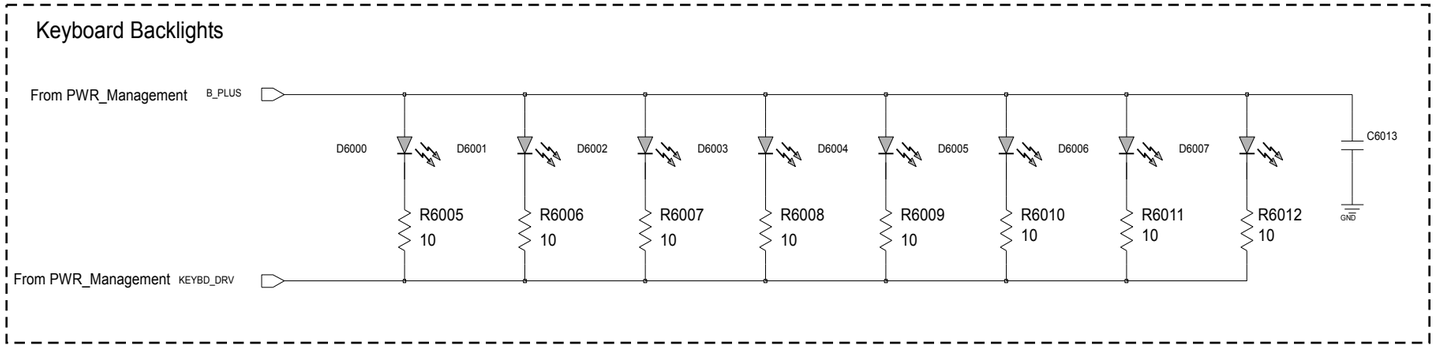
USER INTERFACE
REF 6000-6999

Keypad

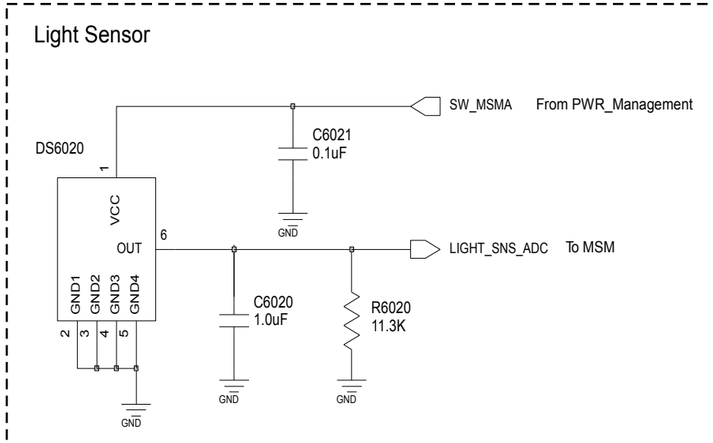




Keyboard Backlights



Light Sensor



A B C D

1 2 3

DS6020
TP3001
TP3010
SW_*
SW_7
SW_4
SW_1
SW_SEND
SW_CLEAR
SW_LSFT
R3011
R5050
R5155
D 3000
C5156
R5159
R5001
TP5000
TP5001
TP5003
TP5002
TP5004
U 5002
R5157
E5000
R5161
R5163
U5001
U 5000
C5155
C5154
R5136
E5001
J4100
R6005
D6000
TP3008
TP3006
TP6000
TP3009
TP3000
U5152
TP1002
TP1001
D6007
R6012
D6003
R6013
R6016
D6005
SW_LEFT
SW_0
SW_8
SW_5
SW_2
SW_DOWN
SW_MENU
SW_UP
SW_CSFT
R6008
D6001
C6013
D6004
R6009
R6007
D6002
R6017
D6006
SW_RIGHT
S26
R4100
C4102
VR4100
C4101
SW_#
SW_9
SW_6
SW_3
SW_END
SW_CARRIER
SW_RSFT
C15
R10
TP1209
TP1207
TP1205
TP1203
TP1201
TP1200
TP1208
TP1206
TP1204
TP1202
TP1210

V265/V262/V260
PCB Side 1
P5

A B C D

1 2 3

U2100 U2000 U1000 U5151 S10 S6003 M10 J10 FL305 LS4500 U4500 FL325 FL330 J5000 FL5001 FL5000 C3500 L3500 C3501 C3016 C3005 U3500 U5150 U3000 Y1000 Y3000 C3015 C3017 C3003 C3018 C3014 Q3900 FL6002 FL6000 J6000 U210 U300 U320 FL300 FL320 C304 U325 Y240 U130 U250 U100 FL102 M3000 C3004 Q3002 C144 J4300 C4326 S6002 S6001 S6000

V265/V262/V260
PCB Side 2
P5.0

Reference Designator	PCB Side	Location	Part number
C10	Side 2	D1	DNP
C100	Side 2	C3	2113945B02
C1000	Side 2	B2	2187906N01
C1001	Side 2	A2	2113946B04
C1002	Side 2	B2	2113946B04
C1003	Side 2	B1	2113945B02
C1004	Side 2	B1	2113945B02
C1008	Side 2	B2	2113946B04
C101	Side 2	D3	2113944A32
C1011	Side 2	A2	2113946B04
C1012	Side 2	A2	2113945B02
C1013	Side 2	B2	2113946B04
C1014	Side 2	A1	2113945B02
C1015	Side 2	B1	2113945B02
C1016	Side 2	B2	2113945B02
C104	Side 2	C3	2113944A40
C105	Side 2	C3	2113743N21
C106	Side 2	C3	2113743N21
C107	Side 2	C3	2113946B04
C11	Side 2	D1	DNP
C1104	Side 2	B2	2113945B02
C1105	Side 2	B1	2113945B02
C1106	Side 2	B1	2113945B02
C1107	Side 2	B1	2113945B02
C111	Side 2	C2	2113944A27
C112	Side 2	C2	2113743N07
C113	Side 2	C2	2113944A40
C116	Side 2	C2	2113944A40
C118	Side 2	C2	2113946B04
C120	Side 2	D3	2113743N02
C1201	Side 2	B2	2113945B02
C1202	Side 2	B2	2113945B02
C1203	Side 2	B2	2113945B02
C1204	Side 2	B2	2113945B02
C1205	Side 2	B1	2113945B02
C1206	Side 2	B1	2113945B02
C121	Side 2	D2	2113944A26
C122	Side 2	D3	2113944A40
C124	Side 2	C2	2113944A40
C125	Side 2	C2	2113743N21
C126	Side 2	C2	2113743N21
C127	Side 2	C2	2113946B04
C128	Side 2	C3	DNP
C129	Side 2	C2	2113946B04
C13	Side 2	D1	2113944A32
C130	Side 2	C3	2113945A09
C131	Side 2	C2	2113945A09
C132	Side 2	C2	2113944A33
C133	Side 2	C2	2113944A33
C134	Side 2	C2	2113944A33
C135	Side 2	C2	2113946B04
C137	Side 2	C2	2113946B04
C139	Side 2	C3	2113944A33
C1400	Side 2	B2	2113946B04
C1403	Side 2	B1	2113945B02
C144	Side 2	C2	2311049A69
C145	Side 2	C2	2113944A33
C146	Side 2	C2	2187893N01
C15	Side 1	D3	2113944A32
C1500	Side 2	B2	2113945B02
C16	Side 2	D1	2104801Z20
C200	Side 2	C2	2113944A23
C2000	Side 2	A2	2113946B04
C2001	Side 2	A2	2113946B04
C2002	Side 2	A2	2113946B04
C2003	Side 2	A2	2113946B04
C201	Side 2	B2	2113944A33
C2100	Side 2	A1	2113946B04
C2101	Side 2	A1	2113946B04
C211	Side 2	B1	2113945A01
C212	Side 2	B1	2113945A01
C215	Side 2	B1	2113946B04
C216	Side 2	B1	2113946B04
C217	Side 2	B2	2113946B04
C218	Side 2	B2	2113946B04
C219	Side 2	B1	2113946B04
C220	Side 2	C2	2113743N21
C230	Side 2	B2	2113945A11
C231	Side 2	B2	2113946B03
C232	Side 2	B2	2113945B02
C233	Side 2	B1	2311049A76
C240	Side 2	C2	2113743L35
C241	Side 2	B2	2113946B05
C242	Side 2	B2	2113945B02
C243	Side 2	B2	2113946B04
C245	Side 2	C2	2113743N10
C250	Side 2	C2	2113945A09
C251	Side 2	B2	2113945A09
C252	Side 2	B3	2113945B02
C253	Side 2	B2	2113946B04
C254	Side 2	B2	2113945B02
C255	Side 2	C1	2113945A13
C300	Side 2	C1	2113944A32
C3000	Side 2	B3	2113946B04
C3001	Side 2	A3	2113946B04
C3002	Side 2	A3	2113946B04
C3003	Side 2	B2	2113928Z10
C3004	Side 2	C2	2113928Z10
C3005	Side 2	A2	2113928Z10
C3006	Side 2	B3	2187893N01
C3007	Side 2	A3	2113946K02
C3008	Side 2	A3	2113945A09
C3009	Side 2	C2	2113743N10
C301	Side 2	C1	2113944A21
C3010	Side 2	A3	2113944A31
C3011	Side 2	B3	2113946B04
C3012	Side 2	B3	2187893N01
C3013	Side 2	A3	2187893N01
C3014	Side 2	B3	2187906N01
C3015	Side 2	B2	2187906N01
C3016	Side 2	B2	2113928Z10
C3017	Side 2	B2	2113928Z10
C3018	Side 2	B3	2113928Z10
C3019	Side 2	B3	2113944A27
C3020	Side 2	B3	2113944A27
C3021	Side 2	A2	2113743A31
C3022	Side 2	A3	2113945A13
C3023	Side 2	C2	2113947B05
C303	Side 2	C1	2113945A09
C304	Side 2	C2	2113928Z10
C305	Side 2	D2	2113944A25
C306	Side 2	C1	2113945A09
C320	Side 2	C2	2113944A26
C321	Side 2	C2	2113944A17
C322	Side 2	C1	2113945A09
C323	Side 2	C2	2113944A26
C324	Side 2	C2	2113946B04
C325	Side 2	D2	2113944A25
C326	Side 2	C2	2113945A09
C330	Side 2	D2	2113944A32
C331	Side 2	D2	2113944A21
C340	Side 2	C1	2113945A11
C341	Side 2	C1	2113944A32
C342	Side 2	C1	2113946B04
C343	Side 2	C1	2113944A32
C3500	Side 2	A2	2113928Z10
C3501	Side 2	B2	2113928Z10
C3502	Side 2	A2	2113944A27
C3503	Side 2	A2	2113944A40
C3900	Side 2	B2	2113945A13
C4100	Side 2	A1	2113947G01
C4102	Side 1	A3	2113944A40
C4103	Side 2	A1	2113944A25
C4104	Side 1	A3	DNP
C4110	Side 2	B2	2113946B04
C4113	Side 2	B2	2113946B04
C4114	Side 2	B2	2113945B02
C4115	Side 2	B2	2113945B02
C4301	Side 2	D3	2187906N01
C4302	Side 2	D2	2113946B04
C4303	Side 2	D2	2187893N01
C4309	Side 2	D3	2113944A32
C4310	Side 2	D3	2113947G01

Reference Designator	PCB Side	Location	Part number
C4313	Side 2	D3	2113944A32
C4314	Side 2	C3	2113944A32
C4315	Side 2	D3	2113944A32
C4324	Side 2	D3	2113944A40
C4325	Side 2	D3	2113944A25
C4326	Side 2	D3	2311049A89
C4355	Side 2	D3	2113944A32
C4357	Side 2	D3	2113944A32
C4358	Side 2	D3	2113944A32
C4359	Side 2	D2	2113944A32
C4363	Side 2	D2	2113944A32
C4365	Side 2	D3	2113944A32
C4410	Side 2	B2	2113946B04
C4411	Side 2	B2	2113946B04
C4413	Side 2	B2	2113946B04
C4500	Side 2	D2	2113946B04
C4501	Side 2	D2	DNP
C4503	Side 2	D2	2187893N01
C4504	Side 2	D2	2187893N01
C4505	Side 2	D2	2113946B04
C4506	Side 2	D2	2113944A32
C4507	Side 2	D2	2113944A32
C4508	Side 2	D2	2113944A32
C453	Side 2	C1	DNP
C5000	Side 2	A3	2113946B04
C5100	Side 2	A2	2113946B04
C5150	Side 2	A3	2113947H01
C5154	Side 1	A2	2113946B04
C5156	Side 1	A2	2113946B04
C5162	Side 2	A2	2113945A12
C5175	Side 2	A2	2113946B04
C6002	Side 2	B3	2113944A32
C6003	Side 2	B2	2113944A32
C6004	Side 2	B2	2113944A32
C6005	Side 2	B2	2113944A32
C6006	Side 2	B2	2113944A32
C6007	Side 2	B2	DNP
C6008	Side 2	B2	2113944A32
C6011	Side 2	B2	2113944A32
C6012	Side 2	B2	2113944A32
C6013	Side 1	A2	2113945A09
C6014	Side 2	B2	2113944A32
C6015	Side 2	B2	2113944A32
C6016	Side 2	B3	2113944A32
C6017	Side 2	B3	2113944A32
C6020	Side 2	A3	2187893N01
C6021	Side 2	A3	2113946B04
C6024	Side 2	B2	2113946B04
C6025	Side 2	B2	2113946B04
C6027	Side 2	B2	2113944A32
C6028	Side 2	B2	2113944A32

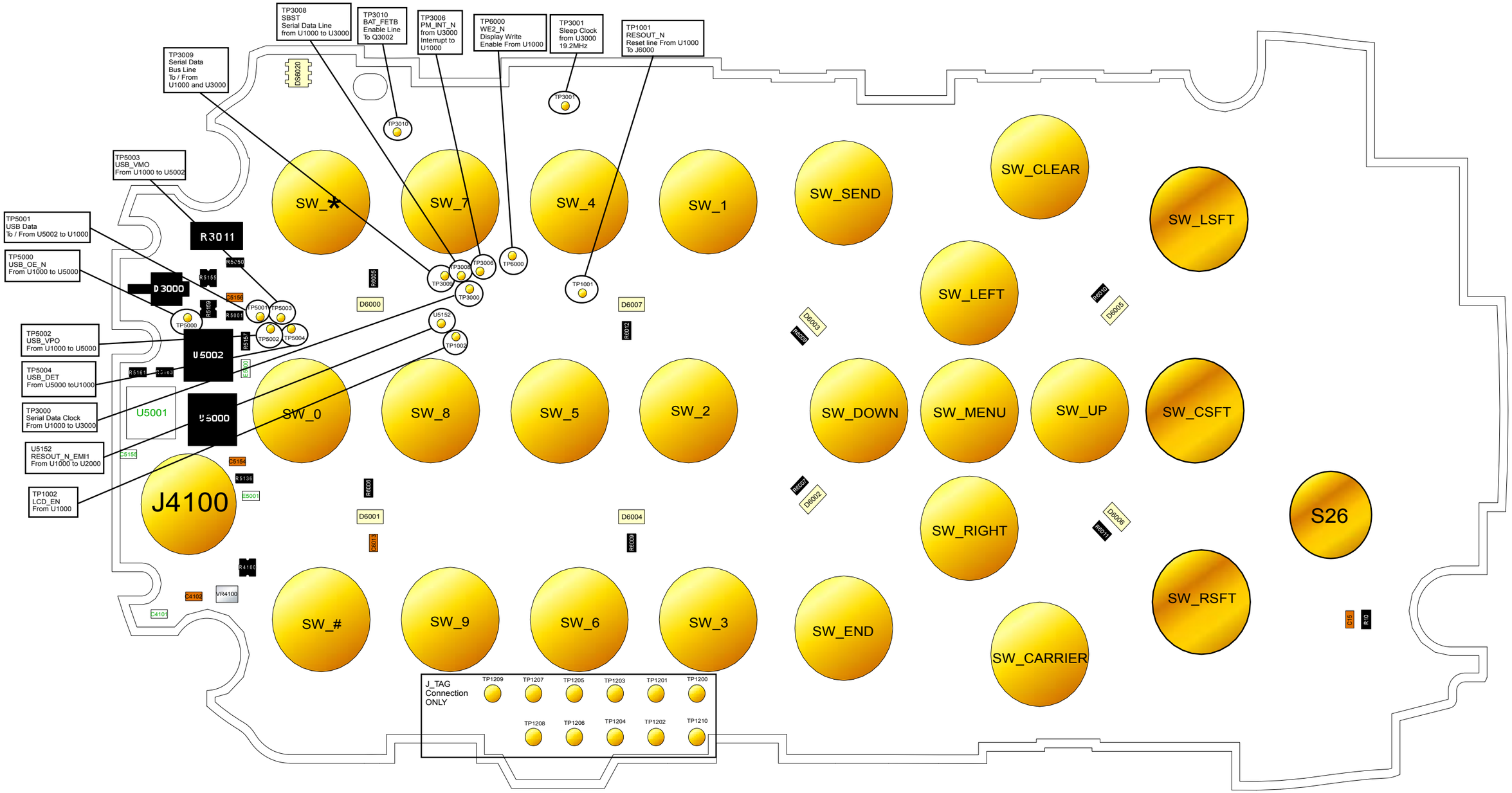
Reference Designator	PCB Side	Location	Part number
D3000	Side 1	A2	4809653F07
D3003	Side 2	B3	4809924D18
D4300	Side 2	B3	4809948D40
D5000	Side 2	B1	4809924D18
D6000	Side 1	A2	4888112M12
D6001	Side 1	A2	4888112M12
D6002	Side 1	B2	4888112M12
D6003	Side 1	B2	4888112M12
D6004	Side 1	B2	4888112M12
D6005	Side 1	C2	4888112M12
D6006	Side 1	C2	4888112M12
D6007	Side 1	B2	4888112M12
DS6020	Side 1	A1	4888938N01
E1000	Side 2	B2	DNP
E1001	Side 2	A2	DNP
E1002	Side 2	B2	DNP
E1005	Side 2	B2	DNP
E1100	Side 2	B2	DNP
E1200	Side 2	B2	DNP
E1201	Side 2	B1	DNP
E130	Side 2	C2	DNP
E3000	Side 2	A2	DNP
E3001	Side 2	B2	DNP
E3002	Side 2	B2	DNP
E3003	Side 2	B3	DNP
E3004	Side 2	B3	DNP
E3005	Side 2	B3	DNP
E3006	Side 2	B3	DNP
E3500	Side 2	B2	DNP
E3501	Side 2	A3	DNP
E4400	Side 2	B2	DNP
E4500	Side 2	D2	DNP
E5000	Side 1	A2	DNP
E5002	Side 1	A2	DNP
FL102	Side 2	C3	9109474K06
FL300	Side 2	C1	9103913K21
FL305	Side 2	C1	9109170T12
FL320	Side 2	C2	9109239M36
FL325	Side 2	D2	9109170T07
FL330	Side 2	D2	4889695L17
FL4000	Side 2	B2	4889526L15
FL5000	Side 2	A2	4889526L13
FL5001	Side 2	A2	4889526L12
FL6000	Side 2	B2	4889526L12
FL6002	Side 2	B2	4889526L12
J10	Side 2	D1	0987378K01
J4300	Side 2	D3	DNP
J5000	Side 2	A2	0987636K08
J6000	Side 2	B3	0989851N01
L10	Side 2	D1	DNP
L100	Side 2	D3	2488090Y12

Reference Designator	PCB Side	Location	Part number
L102	Side 2	C3	2409154M47
L103	Side 2	C3	2488090Y14
L104	Side 2	C3	2488090Y17
L105	Side 2	C3	2488090Y13
L106	Side 2	C3	2488090Y13
L107	Side 2	C3	DNP
L11	Side 2	D1	2489711L01
L112	Side 2	C2	2488090Y12
L115	Side 2	C2	2488090Y21
L12	Side 2	D1	2488090Y21
L121	Side 2	D2	2488090Y07
L122	Side 2	C2	2488090Y16
L123	Side 2	C2	2488090Y06
L124	Side 2	C2	2488090Y13
L125	Side 2	C2	2488090Y08
L126	Side 2	C2	2488090Y08
L127	Side 2	C2	2488090Y13
L13	Side 2	D2	2488090Y21
L16	Side 2	D1	2489711L11
L17	Side 2	D2	DNP
L301	Side 2	C1	2488090Y14
L302	Side 2	C1	DNP
L305	Side 2	D1	DNP
L306	Side 2	D2	2488090Y17
L321	Side 2	C2	DNP
L322	Side 2	C2	2488090Y13
L325	Side 2	D2	2488090Y11
L3450	Side 2	B3	2409154M47
L3500	Side 2	A2	2589195N04
LS4500	Side 2	D2	3988194N01
M10	Side 2	D1	3987746Y01
M3000	Side 2	C2	3987522K03
Q2030	Side 2	B1	DNP
Q300	Side 2	C1	4809939C39
Q3000	Side 2	A2	4809807C41
Q3001	Side 2	A2	4809807C41
Q3002	Side 2	C2	4809807C41
Q3004	Side 2	B2	4809579E57
Q320	Side 2	C2	4809939C39
Q3900	Side 2	B2	4809579E57
Q4320	Side 2	D2	4809579E02
Q5000	Side 2	A3	DNP
R10	Side 1	D3	0613952R25
R1003	Side 2	B2	DNP
R1004	Side 2	B1	DNP
R102	Side 2	C3	0613952M74
R104	Side 2	C3	0613952Q33
R11	Side 2	B1	0613952R25
R115	Side 2	C2	0613952Q49
R124	Side 2	C2	0613952Q33
R131	Side 2	C3	0613952N06

Reference Designator	PCB Side	Location	Part number
R133	Side 2	C3	0613952M74
R134	Side 2	C3	0613952M74
R135	Side 2	C2	0613952Q49
R136	Side 2	C2	0613952Q25
R14	Side 2	D1	0662057V55
R1400	Side 2	B2	0613952Q69
R1407	Side 2	B2	0613952R01
R1500	Side 2	B2	0613952Q73
R1600	Side 2	B1	0613952Q81
R1601	Side 2	B1	0613952Q81
R1700	Side 2	B1	0613952R66
R1701	Side 2	B1	DNP
R2017	Side 2	A2	DNP
R2018	Side 2	A2	0613952R66
R2019	Side 2	A1	DNP
R2020	Side 2	A1	0613952R66
R2030	Side 2	B1	DNP
R2032	Side 2	B1	0613952R66
R210	Side 2	B1	0613952N06
R215	Side 2	B1	0613952Q25
R216	Side 2	B1	0613952Q49
R2301	Side 2	B1	DNP
R231	Side 2	B2	0613952Q89
R232	Side 2	B2	0613952Q81
R241	Side 2	B2	0613952Q87
R242	Side 2	B2	0613952Q79
R243	Side 2	B2	0613952Q73
R250	Side 2	B3	0613952Q49
R251	Side 2	B2	0613952Q42
R255	Side 2	C1	0613952Q73
R3002	Side 2	A3	0613952Q49
R3003	Side 2	B1	DNP
R3004	Side 2	B3	0613952Q01
R3005	Side 2	B3	0613952Q01
R3006	Side 2	B2	0613952Q01
R3008	Side 2	B2	0613952Q01
R3009	Side 2	A2	0613952R01
R3010	Side 2	A3	0613952Q61
R3011	Side 1	A1	0689437N01
R3012	Side 2	B2	0613952Q89
R3013	Side 2	D2	0609591M37
R3014	Side 2	C2	0613952Q49
R3015	Side 2	A3	0613952R01
R3016	Side 2	B2	0613952R25
R3023	Side 2	A2	0613952Q01
R305	Side 2	C1	0613952Q42
R320	Side 2	C2	DNP
R340	Side 2	C1	0613952R01
R341	Side 2	C1	0613952Q73
R342	Side 2	C1	0613952Q25
R343	Side 2	C1	0613952Q59
R344	Side 2	C1	0613952Q45
R345	Side 2	C1	0613952Q45
R349	Side 2	C2	0613952R15
R3500	Side 2	A2	0613952P66
R3502	Side 2	A2	0613952P24
R3900	Side 2	B2	0613952R25
R3901	Side 2	B2	0613952R41
R3902	Side 2	B2	0613952R01
R3903	Side 2	A2	0613952R25
R4000	Side 2	B2	0613952R66
R4100	Side 1	A3	0609591M29
R4110	Side 2	B2	0609591M37
R4112	Side 2	B2	0609591M53
R4300	Side 2	D2	0613952Q81
R4301	Side 2	D2	0613952N06
R4302	Side 2	D2	0613952P66
R4303	Side 2	D2	0613952R15
R4304	Side 2	D3	0613952Q49
R4322	Side 2	C2	0613952R15
R4324	Side 2	D2	0613952R01
R4325	Side 2	D2	0613952R41
R4326	Side 2	B2	0613952R41
R4330	Side 2	D3	0613952Q45
R4500	Side 2	D2	0609591M45
R4501	Side 2	D2	0609591M55
R5000	Side 2	A2	0609591M07
R5001	Side 1	A2	0613952Q77
R5050	Side 1	A1	0613952R11
R5051	Side 2	A3	0613952R35
R5136	Side 1	A2	0613952R11
R5150	Side 2	A3	0609591M49
R5154	Side 2	A3	DNP
R5155	Side 1	A2	0609591M37
R5157	Side 1	A2	0613952R25
R5159	Side 1	A2	0609591M49
R5160	Side 2	A1	0613952R11
R5161	Side 1	A2	0613952R11
R5162	Side 2	A2	0613952R11
R5163	Side 1	A2	0613952R11
R5164	Side 2	A2	0609591M53
R6001	Side 2	B2	DNP
R6002	Side 2	B2	0613952R66
R6005	Side 1	A2	0613952Q25
R6006	Side 1	A2	0613952Q25
R6007	Side 1	B2	0613952Q25
R6008	Side 1	B2	0613952Q25
R6009	Side 1	B2	0613952Q25
R6010	Side 1	C2	0613952Q25
R6011	Side 1	C2	0613952Q25
R6012	Side 1	B2	0613952Q25
R6020	Side 2	A3	0662057V09
R6021	Side 2	B2	0613952R66
R6030	Side 2	A2	0613952R41
RT349	Side 2	C2	0685660C01
S10	Side 2	B1	0187654Y01
S6000	Side 2	C3	4087635K01
S6001	Side 2	C3	4087635K01
S6002	Side 2	B3	4087635K01
S6003	Side 2	C1	4087635K01
SH1	Side 2		2687603Y01
SH2	Side 2		2687601Y01
SH3	Side 2		2688716Y01
TP1001	Side 1	B2	DNP
TP1002	Side 1	B2	DNP
TP1200	Side 1	B3	DNP
TP1201	Side 1	B3	DNP
TP1202	Side 1	B3	DNP
TP1203	Side 1	B3	DNP
TP1204	Side 1	B3	DNP
TP1205	Side 1	B3	DNP
TP1206	Side 1	B3	DNP
TP1207	Side 1	B3	DNP
TP1208	Side 1	B3	DNP
TP1209	Side 1	B3	DNP
TP1210	Side 1	B3	DNP
TP3000	Side 1	B2	DNP
TP3001	Side 1	B1	DNP
TP3002	Side 2	A2	DNP
TP3006	Side 1	B2	DNP
TP3008	Side 1	B2	DNP
TP3009	Side 1	B2	DNP
TP3010	Side 1	A1	DNP
TP3010	Side 1	A1	DNP
TP5000	Side 1	A2	DNP
TP5001	Side 1	A2	DNP
TP5002	Side 1	A2	DNP
TP5003	Side 1	A2	DNP
TP5004	Side 1	A2	DNP
TP6000	Side 1	B1	DNP
U100	Side 2	C3	5109944C56
U1000	Side 2	B2	5109962C31
U130	Side 2	C2	5109944C57
U2000	Side 2	A2	5199175J01
U210	Side 2	B1	5109944C58
U2100	Side 2	A1	5109509A69
U250	Side 2	B3	4809718L25
U300	Side 2	C1	5109908K83
U3000	Side 2	A3	5187970L53
U305	Side 2	C1	5885811G09
U320	Side 2	C2	5109908K94
U325	Side 2	C2	5885811G07
U340	Side 2	C1	5109817F79

Reference Designator	PCB Side	Location	Part number
U3500	Side 2	A2	5109920D39
U4300	Side 2	D2	5109731C39
U4500	Side 2	D2	5109731C44
U5000	Side 1	A2	5187970L32
U5001	Side 1	A2	DNP
U5002	Side 1	A2	5187970L42
U5003	Side 2	A3	DNP
U5150	Side 2	A2	5109817F58
U5151	Side 2	B1	5109522E14
U5152	Side 1	B2	DNP
U5153	Side 2	B2	DNP
VR4100	Side 1	A3	4809948D49
VR4300	Side 2	D3	4809948D49
VR4500	Side 2	D2	DNP
VR6000	Side 2	B3	4809948D49
VR6001	Side 2	B3	4809948D49
Y1000	Side 2	B2	4887820K03
Y240	Side 2	B2	4889251N01
Y3000	Side 2	B3	4809995L18

V265/V262/V260 Major Signal Test Points
Quick Reference Guide



V265/V262/V260
PCB Side 1
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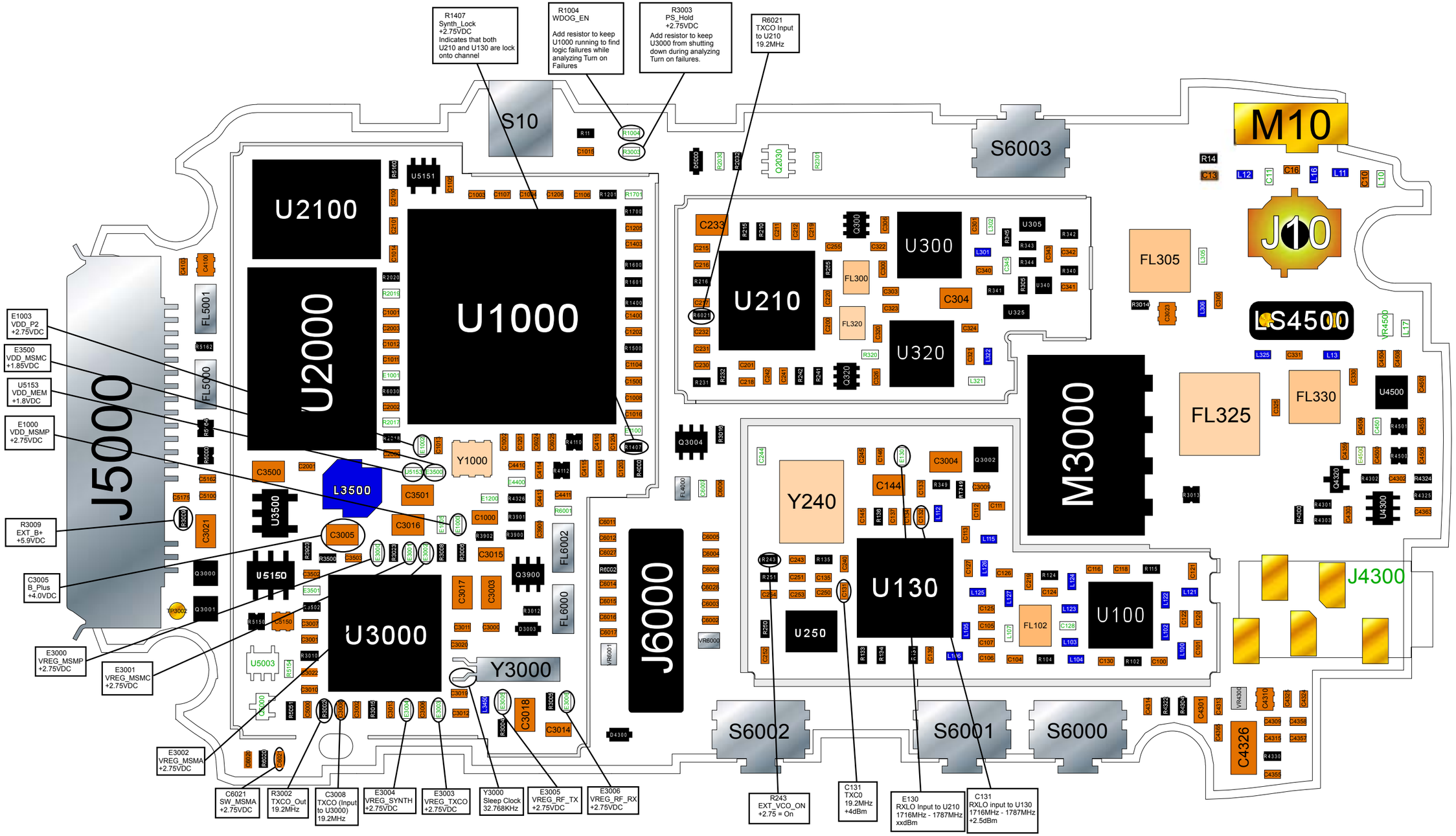
V265/V262/V260 Major Signal Test Points
Quick Reference Guide



V265/V262/V260
PCB Side 2
P5.0