

OV7670/OV7171 CMOS VGA (640x480) CAMERACHIP™ with OmniPixel™ Technology

General Description

The OV7670/OV7171 CAMERACHIP™ is a low voltage CMOS image sensor that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7670/OV7171 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 30 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise (FPN), smearing, blooming, etc., to produce a clean, fully stable color image.



Note: The OV7670/OV7171 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable apps
- Standard SCCB interface compatible with I2C interface
- Supports VGA, CIF, and under CIF for RGB (GRB 4:2:2), YUV (4:2:2) and YCbCr (4:2:2) formats
- VarioPixel™ method for sub-sampling
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), and anti-blooming
- ISP includes noise reduction and defect correction
- Supports LED strobe
- Supports scaling

Ordering Information

Product	Package
OV7670-VL2A (Color, lead-free)	24 pin CSP2
OV7171-VL2A (B&W with microlens, lead-free)	24 pin CSP2

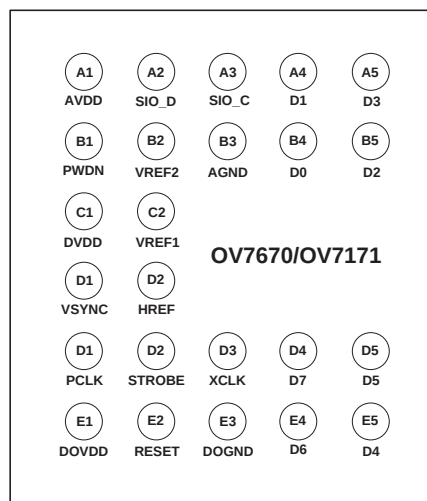
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Array Element (VGA)		640 x 480
Power Supply	Digital Core	1.8VDC $\pm 10\%$
	Analog	2.45V to 3.0V
	I/O	1.8V to 3.3V
Power Requirements	Active	TBD
	Standby	< 20 μ A
Temperature Range	Operation	-30°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB 4:2:2 • Raw RGB Data
Lens Size		1/6"
Chief Ray Angle		TBD
Maximum Image Transfer Rate		30 fps for VGA
Sensitivity		TBD
S/N Ratio		TBD
Dynamic Range		TBD
Scan Mode		Progressive
Electronics Exposure		Up to 510:1 (for selected fps)
Pixel Size		3.6 μ m x 3.6 μ m
Dark Current		TBD
Well Capacity		TBD
Image Area		2.36 mm x 1.76 mm
Package Dimensions		3785 μ m x 4235 μ m

Figure 1 OV7670/OV7171 Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of the OV7670/OV7171 image sensor. The OV7670/OV7171 includes:

- Image Sensor Array (640 x 480 resolution)
- Analog Signal Processor
- A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

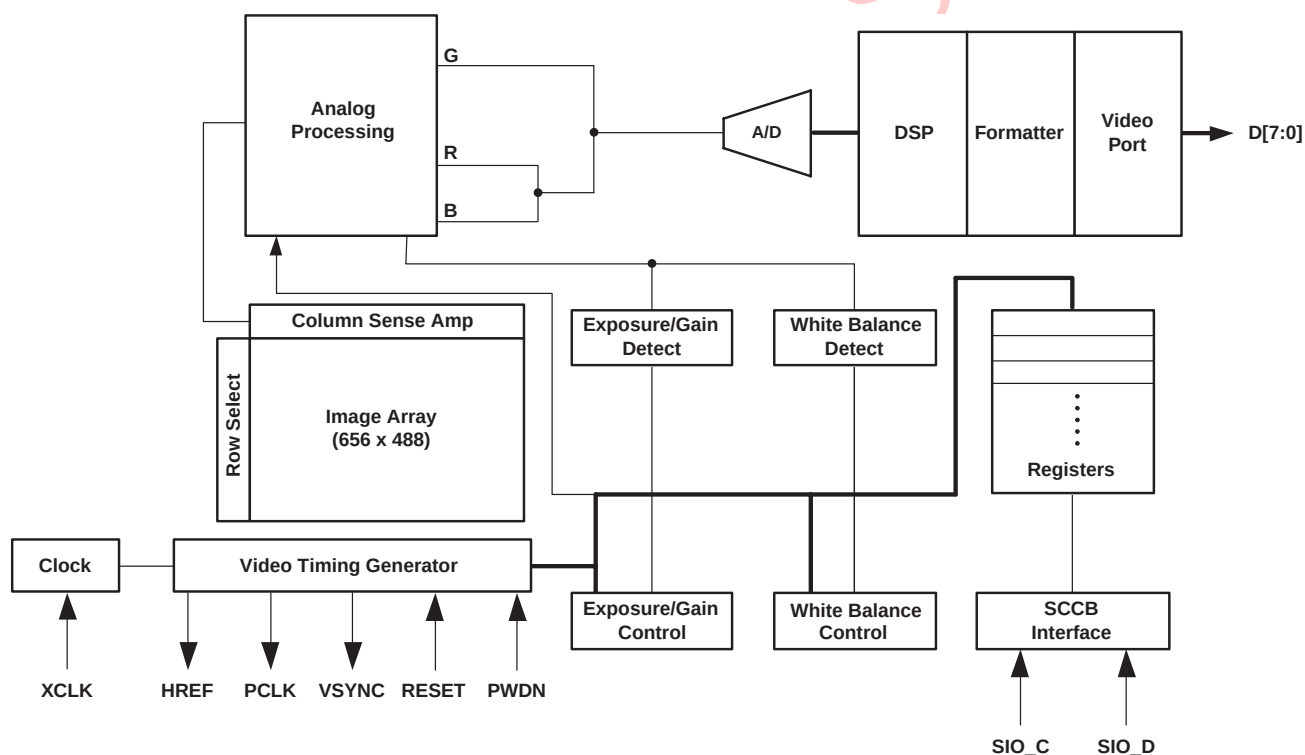
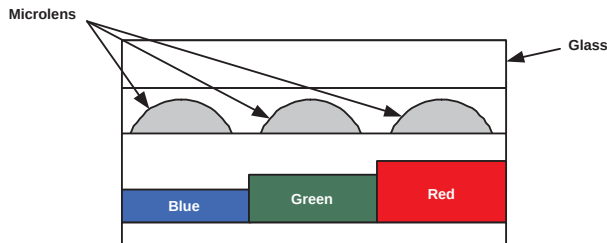


Image Sensor Array

The OV7670/OV7171 sensor has an active image array of 640 columns x 480 rows (307,200 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to a 10-bit analog-to-digital (A/D) converter shared by G and BR channels. This A/D converter operates at speeds up to 12 MHz and is fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to [OmniVision Technologies Serial Camera Control Bus \(SCCB\) Specification](#) for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	AVDD	Power	Analog power supply
A2	SIO_D	I/O	SCCB serial interface data I/O
A3	SIO_C	Input	SCCB serial interface clock input
A4	D1 ^a	Output	YUV/RGB video component output bit[1]
A5	D3	Output	YUV/RGB video component output bit[3]
B1	PWDN	Input (0) ^b	Power Down Mode Selection 0: Normal mode 1: Power down mode
B2	VREF2	Reference	Reference voltage - connect to ground using a 0.1 μ F capacitor
B3	AGND	Power	Analog ground
B4	D0	Output	YUV/RGB video component output bit[0]
B5	D2	Output	YUV/RGB video component output bit[2]
C1	DVDD	Power	Power supply (+1.8 VDC) for digital logic core
C2	VREF1	Reference	Reference voltage - connect to ground using a 0.1 μ F capacitor
D1	VSYNC	Output	Vertical sync output
D2	HREF	Output	HREF output
E1	PCLK	Output	Pixel clock output
E2	STROBE	Output	LED/strobe control output
E3	XCLK	Input	System clock input
E4	D7	Output	YUV/RGB video component output bit[7]
E5	D5	Output	YUV/RGB video component output bit[5]
F1	DOVDD	Power	Digital power supply for I/O ($V_{DD-IO} = 2.5$ to ($V_{DD-A}+0.3V$))
F2	RESET	Input (0)	Clears all registers and resets them to their default values. 0: Normal mode 1: Reset mode
F3	DOGND	Power	Digital ground
F4	D6	Output	YUV/RGB video component output bit[6]
F5	D4	Output	YUV/RGB video component output bit[4]

a. D[7:0] for 8-bit YUV or RGB (D[7] MSB, D[0] LSB)

b. Input (0) represents an internal pull-down resistor.

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40°C to +95°C
Supply Voltages (with respect to Ground)	V _{DD-A}	4.5 V
	V _{DD-C}	3 V
	V _{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V _{DD-IO} +0.5V
Lead-free Temperature, Surface-mount process		245°C
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DD-A}	DC supply voltage – Analog	–	2.45	2.75	3.0	V
V _{DD-C}	DC supply voltage – Digital Core	–	1.62	1.8	1.98	V
V _{DD-IO}	DC supply voltage – I/O power	–	1.8	–	3.3V	V
I _{DDA}	Active (Operating) Current	See Note ^a		TBD		mA
I _{DDS-SCCB}	Standby Current	See Note ^b		1		mA
I _{DDS-PWDN}	Standby Current			10	20	μA
V _{IH}	Input voltage HIGH	CMOS	0.7 x V _{DD-IO}			V
V _{IL}	Input voltage LOW				0.3 x V _{DD-IO}	V
V _{OH}	Output voltage HIGH	CMOS	0.9 x V _{DD-IO}			V
V _{OL}	Output voltage LOW				0.1 x V _{DD-IO}	V
I _{OH}	Output current HIGH	See Note ^c	8			mA
I _{OL}	Output current LOW		15			mA
I _L	Input/Output Leakage	GND to V _{DD-IO}			± 1	μA

- a. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
I_{DDA} = Σ{I_{DD-IO} + I_{DD-C} + I_{DD-A}}, f_{CLK} = 24MHz at 30 fps YUV output, no I/O loading
- b. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
I_{DDS:SCCB} refers to a SCCB-initiated Standby, while I_{DDS:PWDN} refers to a PWDN pin-initiated Standby
- c. Standard Output Loading = 25pF, 1.2KΩ

Table 4 Functional and AC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			18	dB
	Red/Blue Adjustment Range			12	dB
Inputs (PWDN, CLK, RESET)					
f _{CLK}	Input Clock Frequency	10	24	48	MHz
t _{CLK}	Input Clock Period	21	42	100	ns
t _{CLK:DC}	Clock Duty Cycle	45	50	55	%
t _{S:RESET}	Setting time after software/hardware reset			1	ms
t _{S:REG}	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f _{SIO_C}	Clock Frequency			150	KHz
t _{LOW}	Clock Low Period	1.3			μs
t _{HIGH}	Clock High Period	600			ns
t _{AA}	SIO_C low to Data Out valid	100		900	ns
t _{BUF}	Bus free time before new START	1.3			μs
t _{HD:STA}	START condition Hold time	600			ns
t _{SU:STA}	START condition Setup time	600			ns
t _{HD:DAT}	Data-in Hold time	0			μs
t _{SU:DAT}	Data-in Setup time	100			ns
t _{SU:STO}	STOP condition Setup time	600			ns
t _R , t _F	SCCB Rise/Fall times			300	ns
t _{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[7:0] (see Figure 5, Figure 6, Figure 7, Figure 9, and Figure 10)					
t _{PDV}	PCLK[↓] to Data-out Valid			5	ns
t _{SU}	D[7:0] Setup time	15			ns
t _{HD}	D[7:0] Hold time	8			ns
t _{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t _{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	- V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 2.5V, V_{DD-IO} = 2.5V - Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum - Input Capacitance: 10pf - Output Loading: 25pF, 1.2KΩ to 2.5V - f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

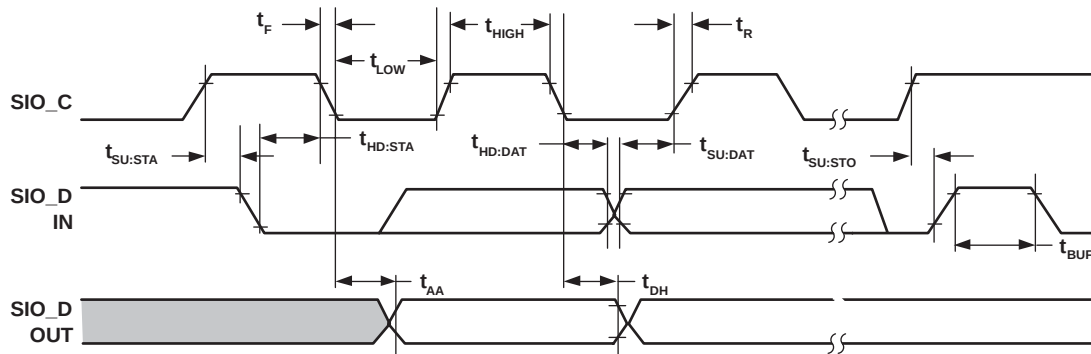


Figure 5 Horizontal Timing

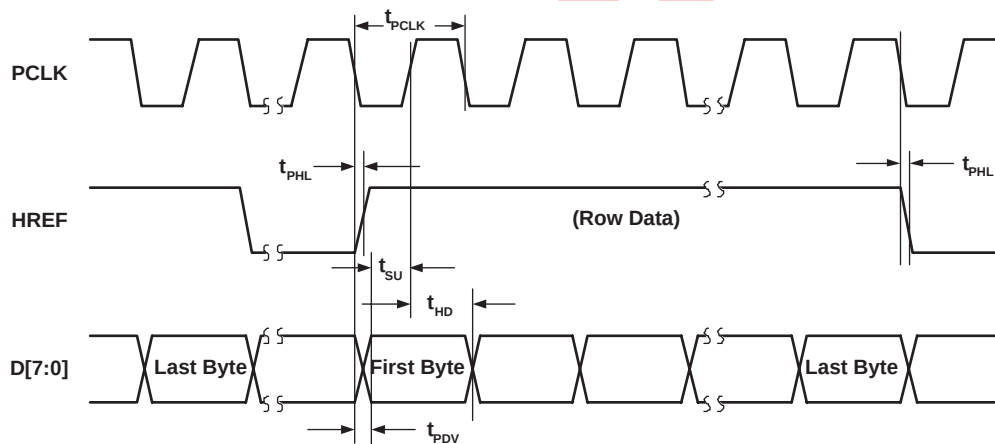
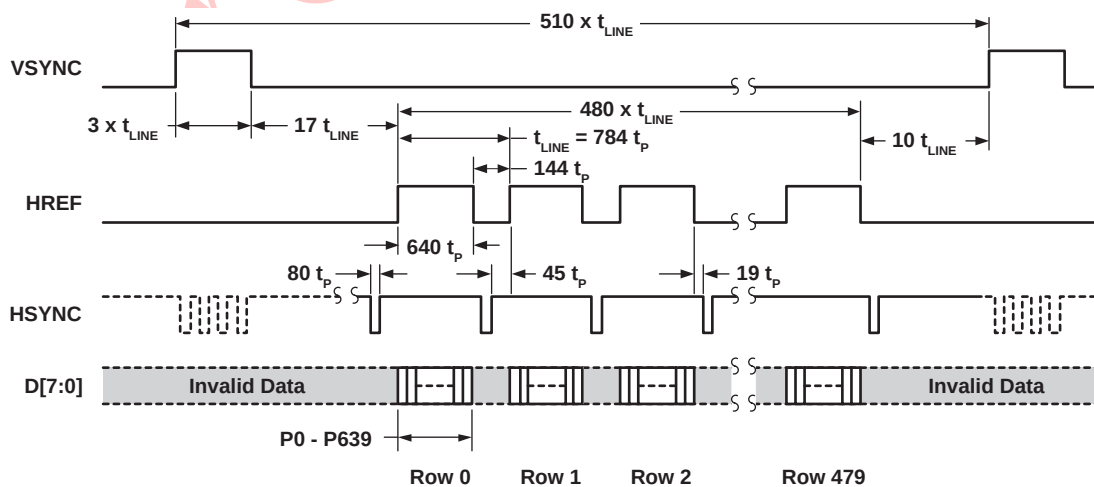


Figure 6 VGA Frame Timing



NOTE:

For Raw data, $t_p = t_{PCLK}$

For YUV/RGB, $t_p = 2 \times t_{PCLK}$

Figure 7 QVGA Frame Timing

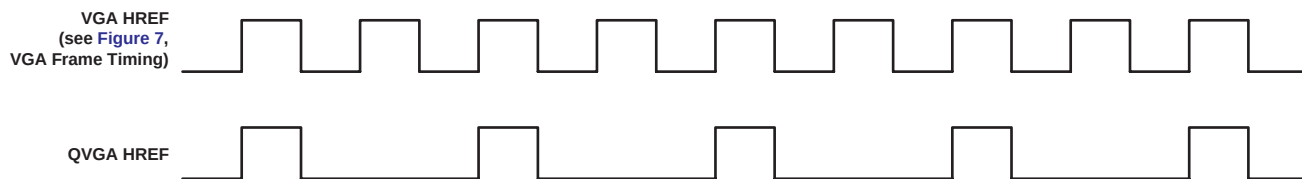


Figure 8 QQVGA Frame Timing

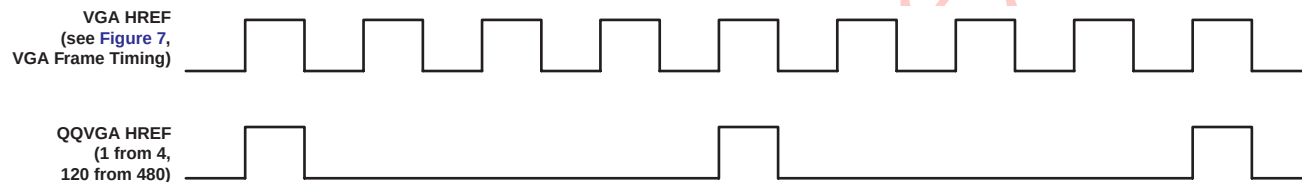


Figure 9 CIF Frame Timing

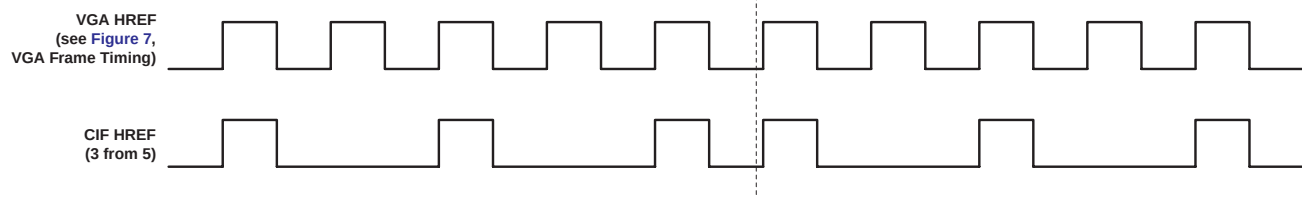


Figure 10 QCIF Frame Timing

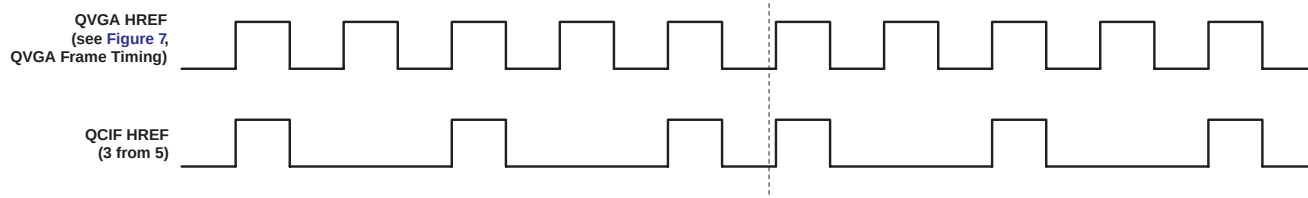


Figure 11 QQCIF Frame Timing

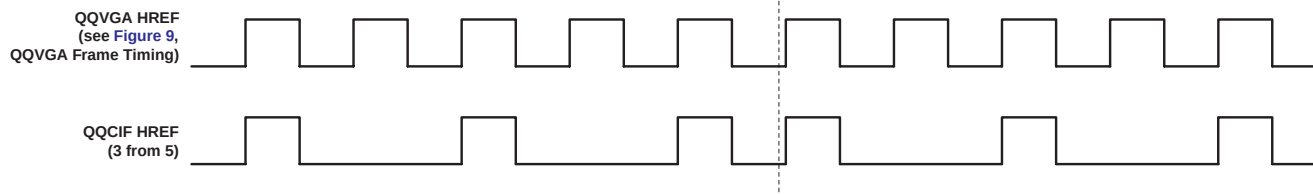


Figure 12 RGB 565 Output Timing Diagram

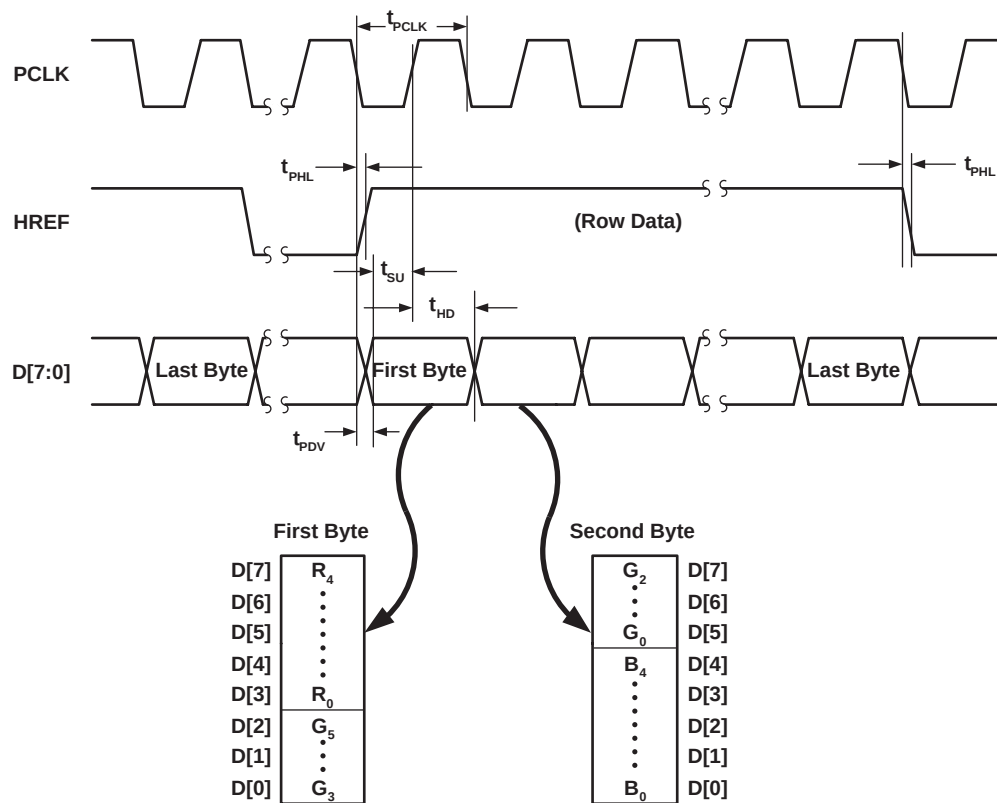
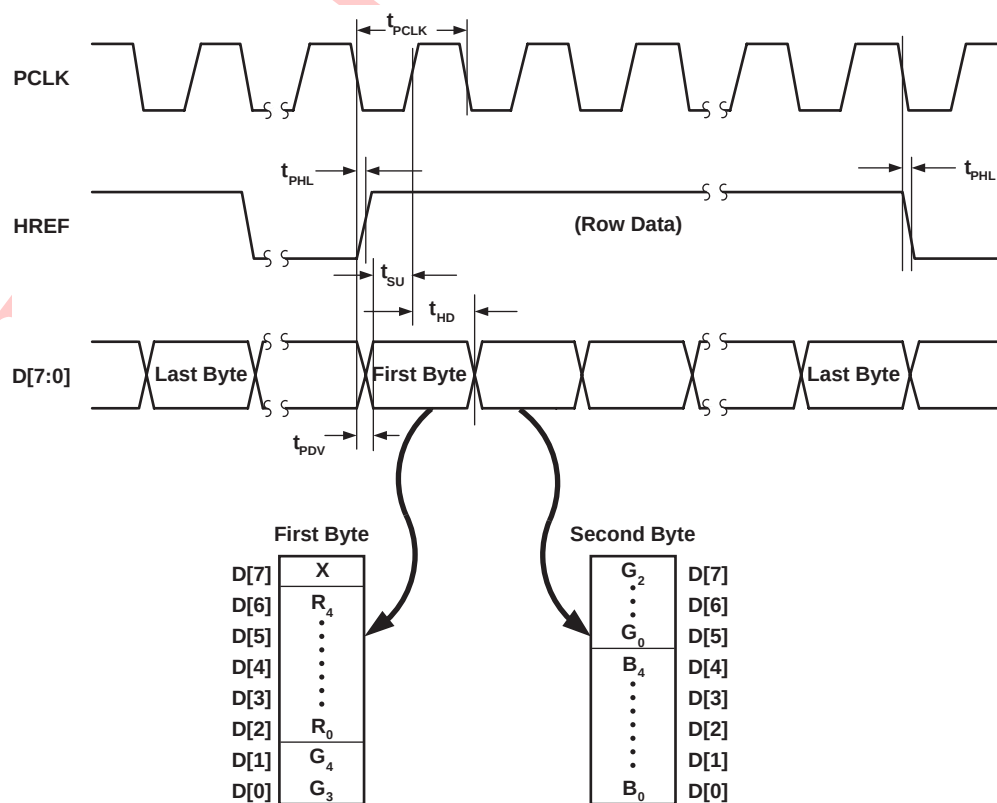


Figure 13 RGB 555 Output Timing Diagram



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV7670/OV7171. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 42 for write and 43 for read.

Table 5 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting • Range: [00] to [FF]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF]
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF]
03	VREF	03	RW	Vertical Frame Control Bit[7:6]: AGC[9:8] digital gain Bit[5:4]: Reserved Bit[3:2]: VREF end low 2 bits (high 8 bits at VSTOP [7:0]) Bit[1:0]: VREF start low 2 bits (high 8 bits at VSTRT [7:0])
04	COM1	00	RW	Common Control 1 Bit[7]: Reserved Bit[6]: CCIR656 format Bit[5:4]: Reserved Bit[3:2]: HREF skip option 00: No skip 01: YUV/RGB skip every other row for YUV/RGB, skip 2 rows for every 4 rows for Raw data 1x: Skip 3 rows for every 4 rows for YUV/RGB, skip 6 rows for every 8 rows for Raw data Bit[1:0]: AEC low 2 LSB (see registers AECHH for AEC[15:10] and AECH for AEC[9:2])
05	BAVE	00	RW	U/B Average Level Automatically updated based on chip output format
06	GbAVE	00	RW	Y/Gb Average Level Automatically updated based on chip output format
07	AECHH	00	RW	Exposure Value - AEC MSB 5 bits Bit[7:6]: Reserved Bit[5:0]: AEC[15:10] (see registers AECH for AEC[9:2] and COM1 for AEC[1:0])
08	RAVE	00	RW	V/R Average Level Automatically updated based on chip output format

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Reserved Bit[1:0]: Output Drive Capability 00: 1x 01: 2x 10: 2x 11: 4x
0A	PID	76	R	Product ID Number MSB (Read only)
0B	VER	70	R	Product ID Number LSB (Read only)
0C	COM3	00	RW	Common Control 3 Bit[7]: Reserved Bit[6]: Output data MSB and LSB swap Bit[5]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[4]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[3]: DCW enable (valid only when COM14[3] = 1) Bit[2]: Scale enable (valid only when COM14[3] = 1) Bit[1:0]: Reserved
0D	COM4	40	RW	Common Control 4 Bit[7:6]: Reserved Bit[5:4]: Average option (needs to change whenever bits COM17[7:6] changes) 00: Full window 01: 1/2 window 10: 1/4 window 11: 1/4 window Bit[3:0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7]: System digital PLL option If the system clock is 48 MHz, this bit should be set to high Bit[6:1]: Reserved Bit[0]: Exposure step can be set longer than VSYNC time 1: In Normal mode, AEC changes by 1/16 and in Fast mode, AEC changes by double

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description															
0F	COM6	43	RW	Common Control 6 Bit[7]: Output of optical black line option 0: Disable HREF at optical black 1: Enable HREF at optical black Bit[6]: BLC input selection 0: Use electrical black line as BLC signal 1: Use optical black line as BLC signal Bit[5]: Digital BLC enable Bit[4]: HREF is high from optical black line Bit[3:2]: Reserved Bit[1]: Reset all timing when format changes Bit[0]: Reserved															
10	AECH	40	RW	Exposure Value Bit[7:0]: AEC[9:2] (see registers AECHH for AEC[15:10] and COM1 for AEC[1:0])															
11	CLKRC	80	RW	Data Format and Internal Clock Bit[7]: Digital PLL option 0: Disable double clock option, meaning the maximum PCLK can be as high as half input clock 1: Enable double clock option, meaning the maximum PCLK can be as high as input clock Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) Range: [0 0000] to [1 1111]															
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Reserved Bit[5]: Output format - CIF selection Bit[4]: Output format - QVGA selection Bit[3]: Output format - QCIF selection Bit[2]: Output format - RGB selection (see below) Bit[1]: Reserved Bit[0]: Output format - Raw RGB (see below) <table><tr><td></td><td>COM7[2]</td><td>COM7[0]</td></tr><tr><td>YUV</td><td>0</td><td>0</td></tr><tr><td>RGB</td><td>1</td><td>0</td></tr><tr><td>Bayer RAW</td><td>0</td><td>1</td></tr><tr><td>Processed Bayer RAW</td><td>1</td><td>1</td></tr></table>		COM7[2]	COM7[0]	YUV	0	0	RGB	1	0	Bayer RAW	0	1	Processed Bayer RAW	1	1
	COM7[2]	COM7[0]																	
YUV	0	0																	
RGB	1	0																	
Bayer RAW	0	1																	
Processed Bayer RAW	1	1																	

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit (used only in fast condition and when COM5[0] is low) 0: Fast condition change maximum step is VSYNC 1: Unlimited step size Bit[5]: Banding filter ON/OFF - In order to turn ON the banding filter, BD50ST (0x9D) or BD60ST (0x9E) must be set to a non-zero value. Bit[4:3]: Reserved Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable
14	COM9	4A	RW	Common Control 9 Bit[7]: Reserved Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x Bit[3]: Reserved Bit[2]: Data format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than VSYNC Bit[0]: Freeze AGC/AEC
15	COM10	00	RW	Common Control 10 Bit[7]: Reserved Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: PCLK always output 1: No PCLK output when HREF is low Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: VSYNC option 0: PCLK valid on falling edge 1: PCLK valid on rising edge Bit[1]: VSYNC negative Bit[0]: HSYNC negative
16	RSVD	XX	–	Reserved
17	HSTART	11	RW	Output Format - Horizontal Frame (HREF column) start high 8-bit (low 3 bits are at HREF[2:0])

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
18	HSTOP	61	RW	Output Format - Horizontal Frame (HREF column) end high 8-bit (low 3 bits are at HREF[5:3])
19	VSTRT	03	RW	Output Format - Vertical Frame (row) start high 8-bit (low 2 bits are at VREF[1:0])
1A	VSTOP	7B	RW	Output Format - Vertical Frame (row) end high 8-bit (low 2 bits are at VREF[3:2])
1B	PSHFT	00	RW	Data Format - Pixel Delay Select (delays timing of the D[7:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	MVFP	00	RW	Mirror/VFlip Enable Bit[7:6]: Reserved Bit[5]: Mirror 0: Normal image 1: Mirror image Bit[4]: VFlip enable 0: Normal image 1: Vertically flip image Bit[3]: Reserved Bit[2]: Black sun enable Bit[1]: Black sun delay 1 Bit[0]: Black sun delay 0
1F	LAEC	00	RW	Reserved
20	ADCCTR0	04	RW	ADC Control Bit[7:4]: Reserved Bit[3]: ADC range adjustment 0: 1x range 1: 1.5x range Bit[2:0]: ADC range adjustment 000: 0.8x 100: 1x 111: 1.2x
21	ADCCTR1	02	RW	Bit[7:0]: Reserved
22	ADCCTR2	01	RW	Bit[7:0]: Reserved
23	ADCCTR3	80	RW	Bit[7:0]: Reserved
24	AEW	75	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	63	RW	AGC/AEC - Stable Operating Region (Lower Limit)

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: Upper limit of 4 MSB Bit[3:0]: Lower limit of 4 LSB
27	BBIAS	80	RW	B Channel Signal Output Bias (effective only when COM6[3] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
28	GbBIAS	80	RW	Gb Channel Signal Output Bias (effective only when COM6[3] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
29	RSVD	XX	–	Reserved
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7:4]: 4 MSB for dummy pixel insert in horizontal direction Bit[3:2]: HSYNC falling edge delay 2 MSB Bit[1:0]: HSYNC rising edge delay 2 MSB
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	RBIAS	80	RW	R Channel Signal Output Bias (effective only when COM6[3] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
2D	ADVFL	00	RW	LSB of insert dummy lines in vertical direction (1 bit equals 1 line)
2E	ADVFLH	00	RW	MSB of insert dummy lines in vertical direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	HSYST	08	RW	HSYNC Rising Edge Delay (low 8 bits)
31	HSYEN	30	RW	HSYNC Falling Edge Delay (low 8 bits)
32	HREF	80	RW	HREF Control Bit[7:6]: HREF edge offset to data output Bit[5:3]: HREF end 3 LSB (high 8 MSB at register HSTOP) Bit[2:0]: HREF start 3 LSB (high 8 MSB at register HSTART)
33	CHLF	08	RW	Array Current Control Bit[7:0]: Reserved
34	ARBLM	03	RW	Array Reference Control Bit[7:0]: Reserved
35-36	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
37	ADC	04	RW	ADC Control Bit[7]: Negative charge pump control 1: Bypass negative pump Bit[6]: Charge pump control 1: Bypass charge pump Bit[5:0]: Reserved
38	ACOM	12	RW	ADC and Analog Common Mode Control Bit[7:0]: Reserved
39	OFON	00	RW	ADC Offset Control Bit[7:0]: Reserved
3A	TSLB	0C	RW	Line Buffer Test Option Bit[7:5]: Reserved Bit[4]: UV output value 0: Use normal UV output 1: Use fixed UV value set in registers MANU and MANV as UV output instead of chip output Bit[3:2]: Output sequence 00: Y U Y V 01: Y V Y U 10: V Y U Y 11: U Y V Y Bit[1:0]: Reserved
3B	COM11	00	RW	Common Control 11 Bit[7]: Night mode 0: Night mode disable 1: Night mode enable - Frame rate will adjust based on COM11 [6:5] before. Also, ADV FH and ADV FL will be automatically updated. Bit[6:5]: Night mode insert frame option 00: Normal frame rate 01: 1/2 frame rate 10: 1/4 frame rate 11: 1/8 frame rate Bit[4]: D56_Auto 1: Use 50/60 auto detect result Bit[3]: Banding filter value select 0: Select BD60ST [7:0] (0x9E) as Banding Filter Value 1: Select BD50ST [7:0] (0x9D) as Banding Filter Value Bit[2]: Reserved Bit[1]: Exposure timing can be less than limit of banding filter when light is too strong Bit[0]: Reserved
3C	COM12	40	RW	Common Control 12 Bit[7]: HREF option 0: No HREF when VREF is low 1: Always has HREF Bit[6:0]: Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3D	COM13	99	RW	Common Control 13 Bit[7]: Gamma enable Bit[6]: UV adjust enable Bit[5:0]: Reserved
3E	COM14	0E	RW	Common Control 14 Bit[7:5]: Reserved Bit[4]: Bit[3]: Scale down separate Bit[2:0]: PCLK divider (only when COM14[4] = 1) 000: 1x 001: 1/2x 010: 1/4x 011: 1/8x 100: 1/16x 101: 1/32x 110: 1/64x 111: 1/128x
3F	EDGE	88	RW	Edge Enhancement Adjustment Bit[7:5]: Reserved Bit[4:0]: Edge enhancement factor
40	COM15	C0	RW	Common Control 15 Bit[7:6]: Data format - output full range enable 0x: Output range: [10] to [F0] 10: Output range: [01] to [FE] 11: Output range: [00] to [FF] Bit[5:4]: RGB 555/565 option (must set COM7[2] = 1 and COM7[0] = 0) x0: Normal RGB output 01: RGB 565 11: RGB 555 Bit[3:0]: Reserved
41	COM16	10	RW	Common Control 16 Bit[7:6]: Reserved Bit[5]: Enable edge enhancement for YUV output 0: Disable 1: Enable Bit[4]: De-noise enable 0: Disable 1: Enable Bit[3]: AWB gain enable Bit[2]: Reserved Bit[1]: Color matrix coefficient double option Bit[0]: Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
42	COM17	08	RW	Common Control 17 Bit[7:6]: AEC window (need to change COM4[5:4] whenever these bits change) 00: Normal 01: 1/2 10: 1/4 11: 1/4 Bit[5:4]: Reserved Bit[3]: DSP color bar enable Bit[2:0]: Reserved
43	AWBC1	F0	RW	Reserved
44	AWBC2	14	RW	Reserved
45	AWBC3	45	RW	Reserved
46	AWBC4	61	RW	Reserved
47	AWBC5	51	RW	Reserved
48	AWBC6	79	RW	Reserved
49	RSVD	XX	–	Reserved
4A	DNSTH	00	RW	De-noise Threshold
4B-4E	RSVD	XX	–	Reserved
4F	MTX1	40	RW	Matrix Coefficient 1
50	MTX2	34	RW	Matrix Coefficient 2
51	MTX3	0C	RW	Matrix Coefficient 3
52	MTX4	17	RW	Matrix Coefficient 4
53	MTX5	29	RW	Matrix Coefficient 5
54	MTX6	40	RW	Matrix Coefficient 6
55	BRIGHT	00	RW	Brightness Control
56	CONTRAS	40	RW	Contrast Control
57	CONTRAS-CENTER	80	RW	Contrast Center
58	MTXS	1E	RW	Matrix Coefficient Sign for coefficient 5 to 0 Bit[7:6]: Reserved Bit[5:0]: Matrix coefficient sign 0: Plus 1: Minus
59-61	RSVD	XX	–	AWB Control
62	LCC1	00	RW	Lens Correction Option 1
63	LCC2	00	RW	Lens Correction Option 2

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
64	LCC3	10	RW	Lens Correction Option 3
65	LCC4	80	RW	Lens Correction Option 4
66	LCC5	00	RW	Lens Correction Control Bit[7:3]: Reserved Bit[2]: Lens correction control select Bit[1]: Reserved Bit[0]: Lens correction enable
67	MANU	80	RW	Manual U Value (effective only when register TSLB[4] is high)
68	MANV	80	RW	Manual V Value (effective only when register TSLB[4] is high)
69	GFIX	00	RW	Fix Gain Control Bit[7:6]: Fix gain for Gr channel 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[5:4]: Fix gain for Gb channel 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[3:2]: Fix gain for R channel 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[1:0]: Fix gain for B channel 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x
6A	GGAIN	00	RW	G Channel AWB Gain
6B	DBLV	3A	RW	Bit[7:6]: PLL control 00: Bypass PLL 01: Input clock x4 10: Input clock x8 11: Input clock x16 Bit[5]: Reserved Bit[4]: Charge pump clock control 1: Bypass regulator Bit[3:0]: Clock divider control for DSP scale control (valid only when COM14[3] = 1)
6C		02	RW	AWB Control 3
6D		55	RW	AWB Control 2

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6E		00	RW	AWB Control 1
6F		9A	RW	AWB Control 0
70	SCALING_XSC	4A	RW	Bit[7]: Test_pattern[0] - works with test_pattern[1] test_pattern: 00: No test output 01: Data out pin short test 10: Solid color bar 11: Fade to gray color Bit[6:0]: Horizontal scale factor
71	SCALING_YSC	35	RW	Bit[7]: Test_pattern[1] - works with test_pattern[0] test_pattern: Bit[6:0]: Vertical scale factor
72	SCALING_DCWCTR	11	RW	DCW Control Bit[7:0]: DCW control parameter
73	SCALING_PCLK_DIV	00	RW	Bit[7:6]: Negative charge pump clock control 00: Input clock 01: Input clock/2 10: Input clock/4 11: Output of PLL Bit[5:4]: Charge pump clock control 00: Input clock 01: Input clock/2 10: Input clock/4 11: Output of PLL Bit[3:0]: Clock divider control for DSP scale control (valid only when COM14[3] = 1)
74		00	RW	Bit[7:5]: Reserved Bit[4]: DG_Manu 0: Digital gain control by REG74[1:0] 1: Digital gain control by VREF[7:6] Bit[3:2]: Reserved Bit[1:0]: Digital gain manual control 00: Bypass 01: 1x 10: 2x 11: 4x
75		0F	RW	Bit[7:5]: Reserved Bit[4:0]: Base1

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
76		01	RW	Bit[7]: Reserved Bit[6]: White pixel correction enable 0: Disable 1: Enable Bit[5]: White pixel correction enable 0: Disable 1: Enable Bit[4:0]: Base2
77		10	RW	Bit[7:0]: Offset
78-79	RSVD	XX	–	Reserved
7A-8A	GAMA	XX	RW	Gamma Curve Parameters
8B-91	RSVD	XX	–	Reserved
92	DM_LNL	00	RW	Dummy Line low 8 bits
93	DM_LNH	00	RW	Dummy Line high 8 bits
94-9C	RSVD	XX	–	Reserved
9D	BD50ST	99	RW	50 Hz Banding Filter Value (effective only when COM8[5] is low and COM11[3] is high)
9E	BD60ST	7F	RW	60 Hz Banding Filter Value (effective only when COM8[5] is low and COM11[3] is low)
9F-AB		XX	–	Histogram-based AEC/AGC Control
AC-AF	RSVD	XX	–	Reserved
B0-C8		XX	–	Digital BLC Control
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7670/OV7171 uses a 24-ball Chip Scale Package 2 (CSP2). Refer to Figure 14 for package information, Table 6 for package dimensions and Figure 15 for the array center on the chip.



Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 14 OV7670/OV7171 Package Specifications

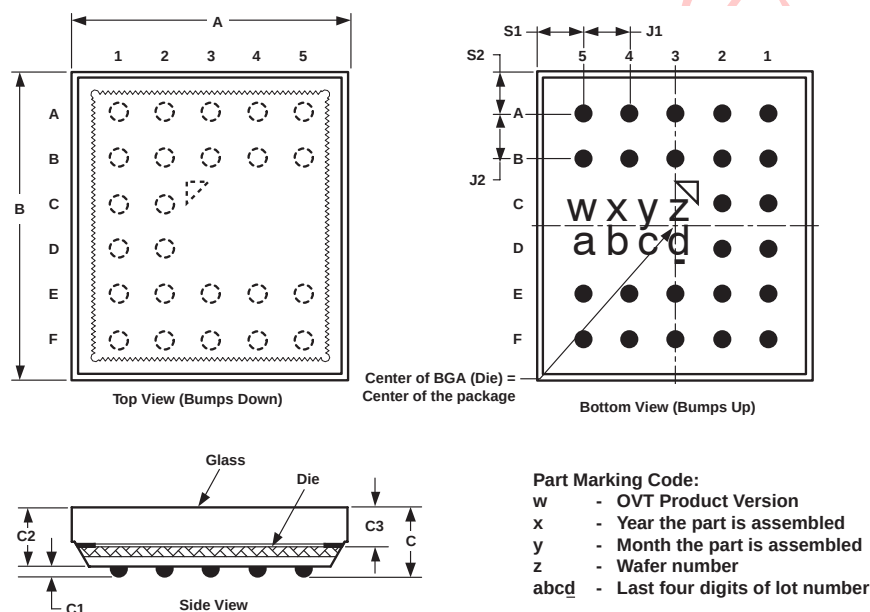
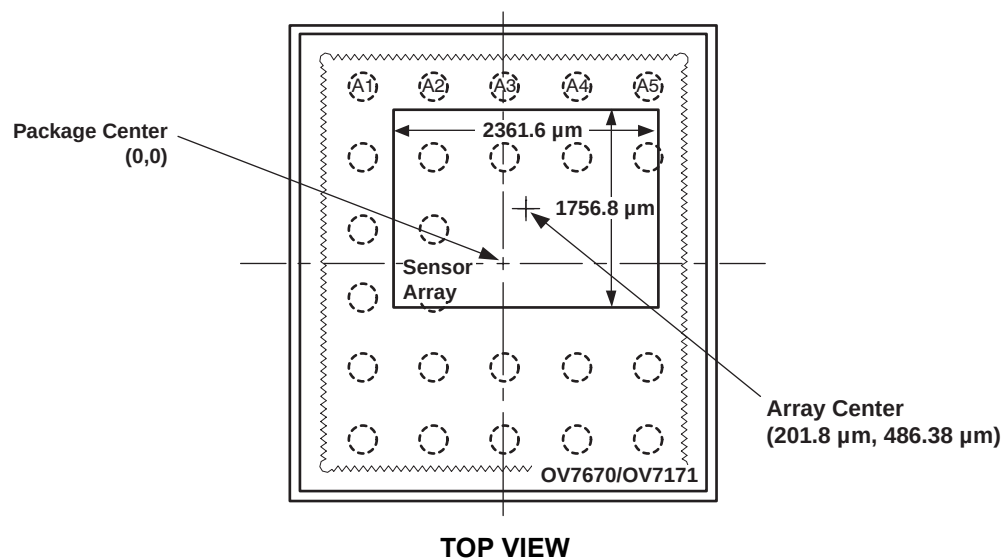


Table 6 OV7670/OV7171 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	3760	3785	3810	μm
Package Body Dimension Y	B	4210	4235	4260	μm
Package Height	C	925	985	1045	μm
Ball Height	C1	130	160	190	μm
Package Body Thickness	C2	780	825	870	μm
Thickness of Glass Surface to Wafer	C3	525	545	565	μm
Ball Diameter	D	270	300	330	μm
Total Pin Count	N		24		
Pin Count X-axis	N1		5		
Pin Count Y-axis	N2		6		
Pins Pitch X-axis	J1		620		μm
Pins Pitch Y-axis	J2		620		μm
Edge-to-Pin Center Distance Analog X	S1	623	653	683	μm
Edge-to-Pin Center Distance Analog Y	S2	538	568	598	μm

Sensor Array Center

Figure 15 OV7670/OV7171 Sensor Array Center



- NOTES:**
1. This drawing is not to scale and is for reference only.
 2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A5 oriented down on the PCB.

IR Reflow Ramp Rate Requirements

OV7670/OV7171 Lead-Free Packaged Devices



Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 16 IR Reflow Ramp Rate Requirements

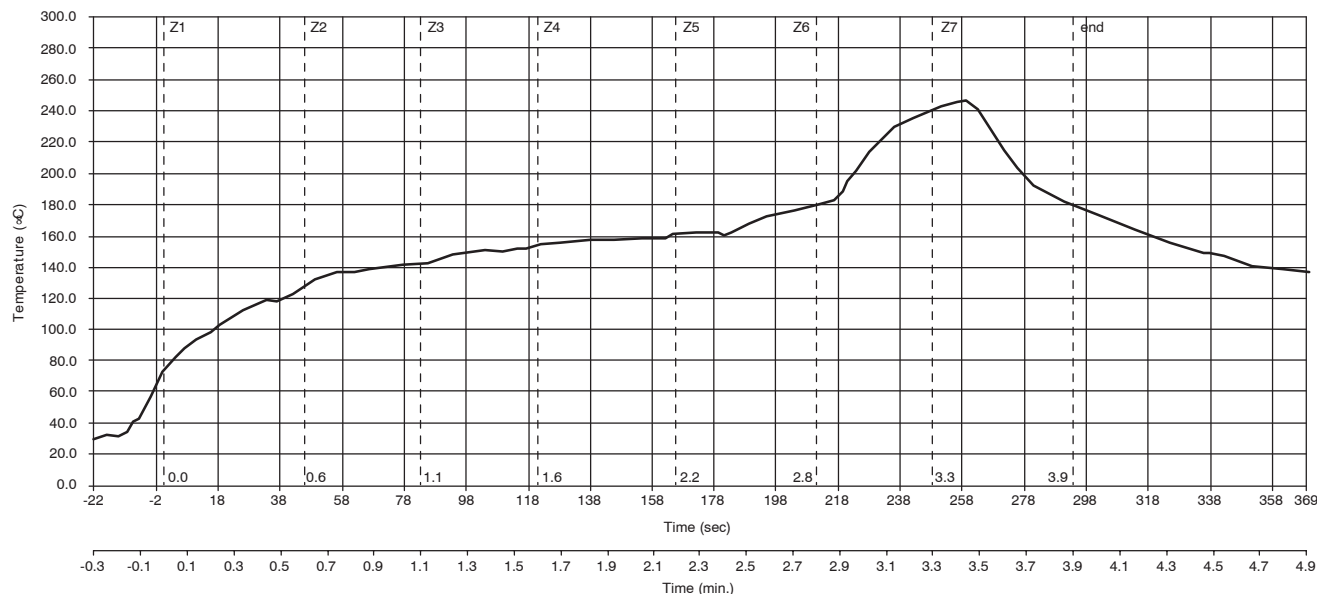


Table 7 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 255°C	No greater than 390 seconds

Environmental Specifications

Table 8 OV7670/OV7171 Reliability Test Results

Parameter	Test Condition
Temperature/Humidity	85°C/85% Relative Humidity, 1000 hrs. ^a
Temperature Cycling (Air-to-Air)	-25°C / +125°C, 72 cycles/day, 1000 cycles ^a
Highly Accelerated Stress Test (HAST)	110°C / 85% Relative Humidity, 168 hrs. ^a
High Temperature Storage (HTS)	150°C, 1000 hrs. ^a
High Temperature Static Bias (HTSB)	125°C, 1000 hrs. ^a

a. Pre-Condition (Moisture Level II): 125°C, 24h → 85°C/60% RH/168h → IR Reflow 235°C, 10 sec, 3 cycles

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (<http://www.ovt.com>) to obtain the current versions of all documentation.*
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Pre-Release