



MPX
Debug Guide
Rev. 1.0



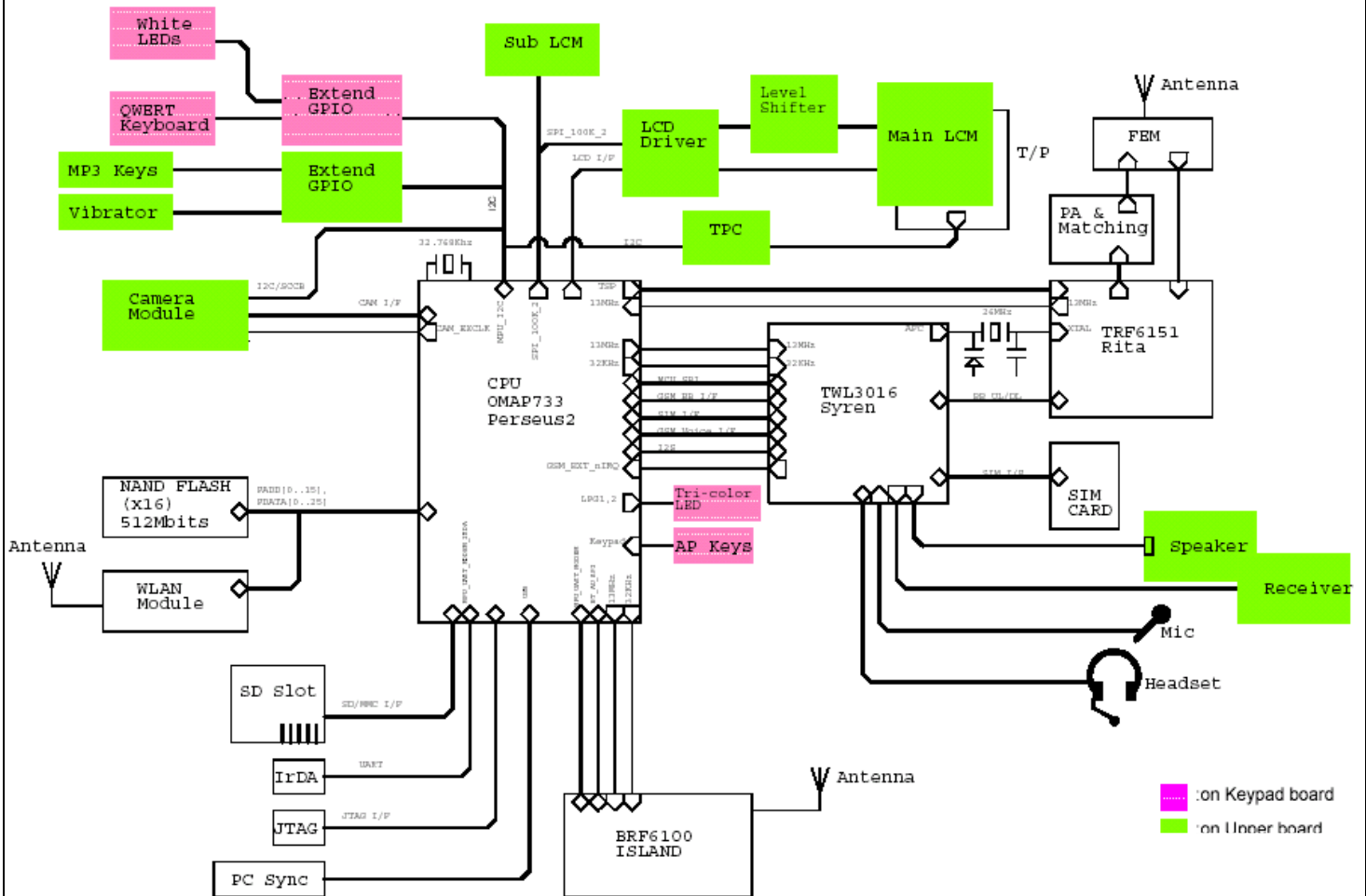
Applicable Range

P7T series produces

1. Purpose:

This document description of the complete circuit and describe the repair flow chart of component level.

2. MPx Block Diagram:

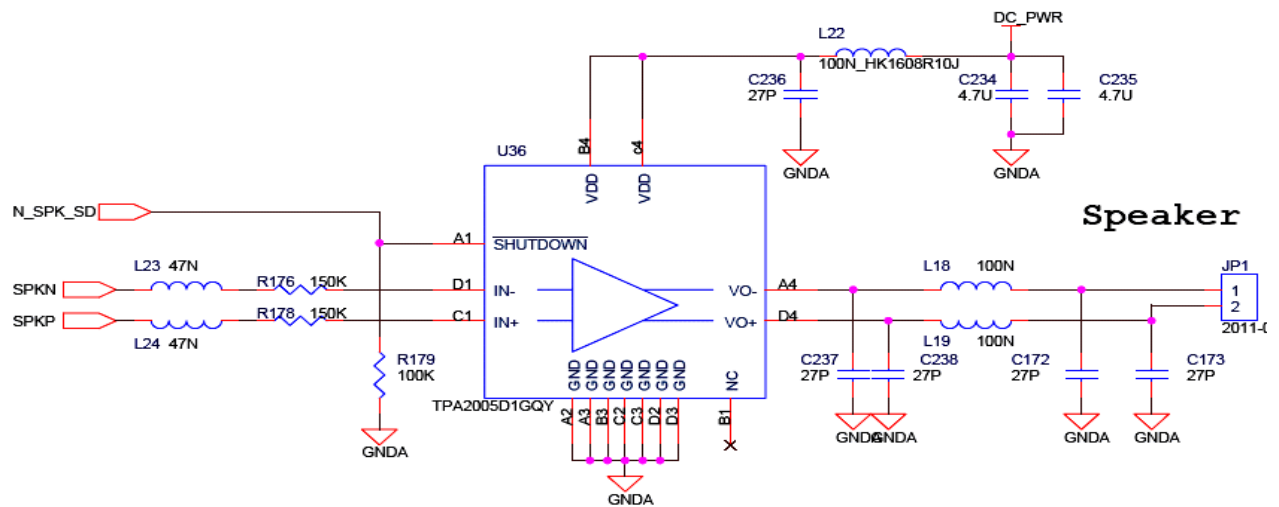




3. Repair Flow Chart

3-1. Speaker Circuit

3-1-1. Speaker circuit description



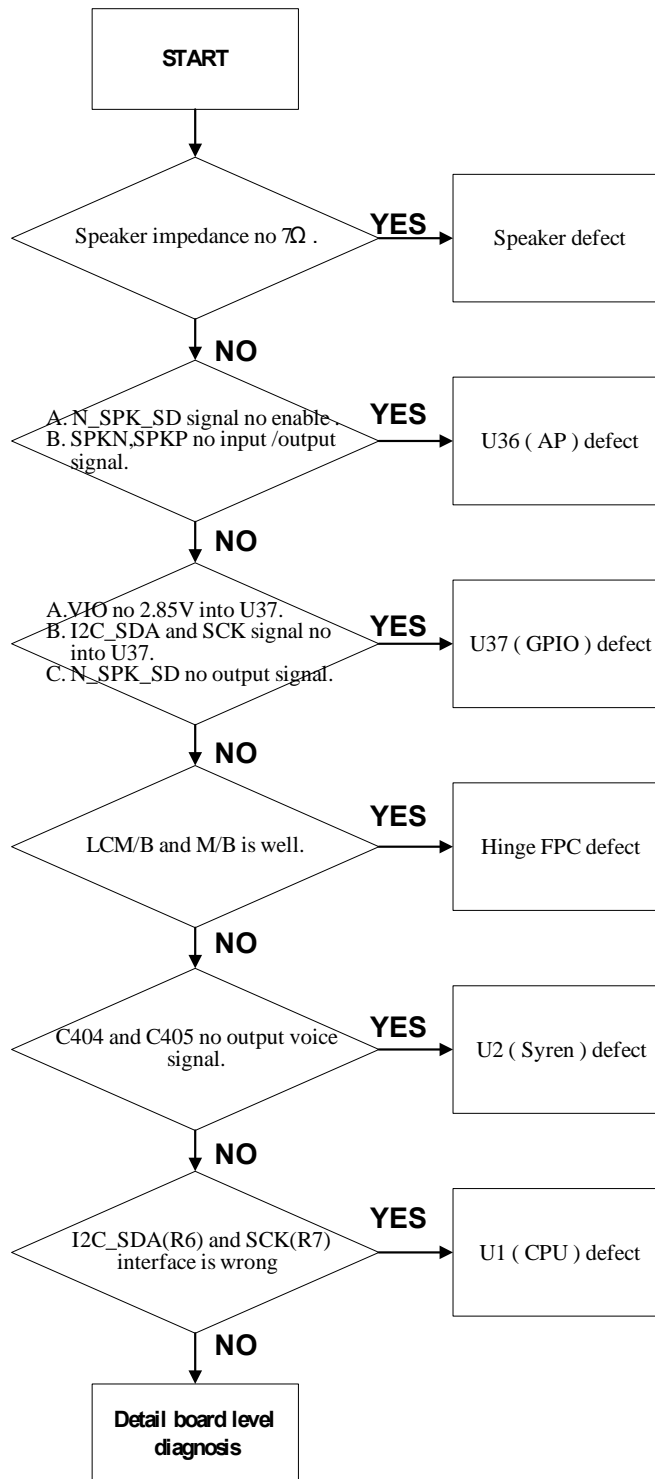
Description

- N_SPK_SD** :S/W enable U37(GPIO) and control U36(AMP) on/off.
- SPKN,SPKP**:Front U2(Syrne) and control Audio output signal to speaker OP.

Application

- CPU enable U37(GPIO) and Syrne send signal to U36 (to amplify) then output signal to pass through L/C (filter) at the same time.

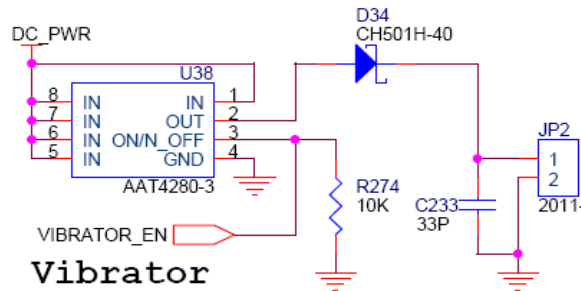
3-1-2. Speaker function failure analysis Flow Chart



3-2. Vibrator Circuit



3-2-1. Vibrator circuit description



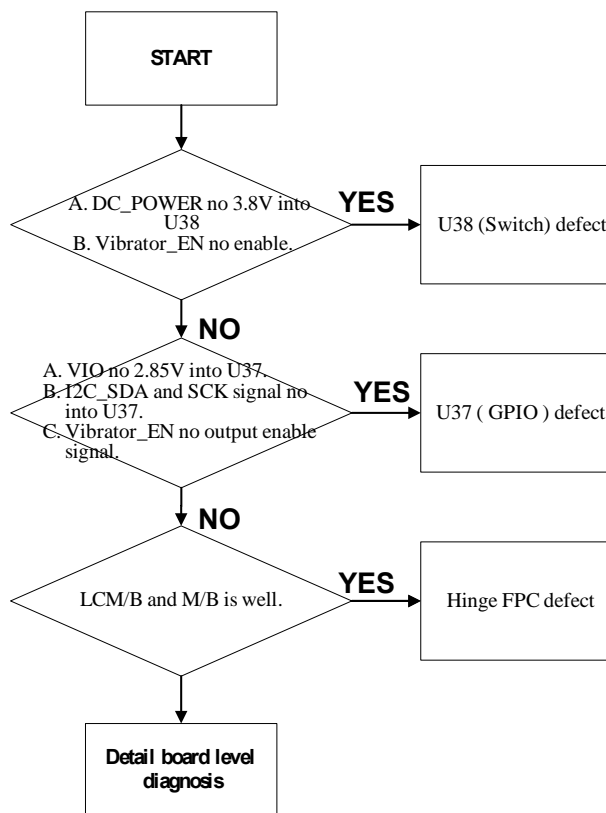
Description

Vibrator_EN: S/W enable U38 (switch) on/off.

Application

CPU control signal to U37 (GPIO) then enable U38 to control Vibrator on/off.

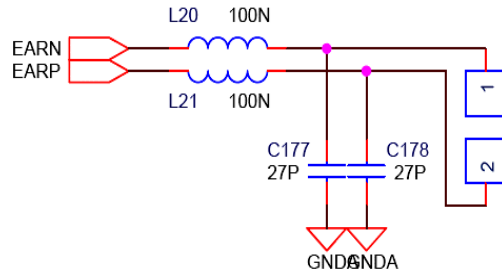
3-2-2. Vibrator function failure analysis Flow Chart



3-3. Receiver Circuit



3-3-1. Receiver circuit description



Description

EARN, EARP : come from U2(Syrne) and control output voice signal.

Application

U2 control voice signal to pass through L/C (filter) to receiver.

3-4. Camera Flashlight Circuit

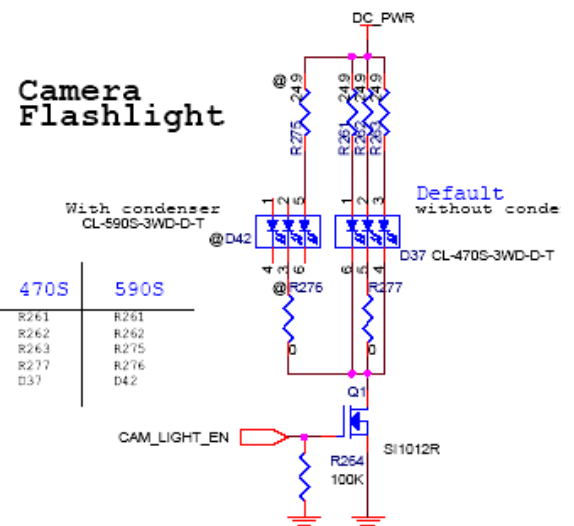
3-4-1. Camera Flashlight circuit description

Description

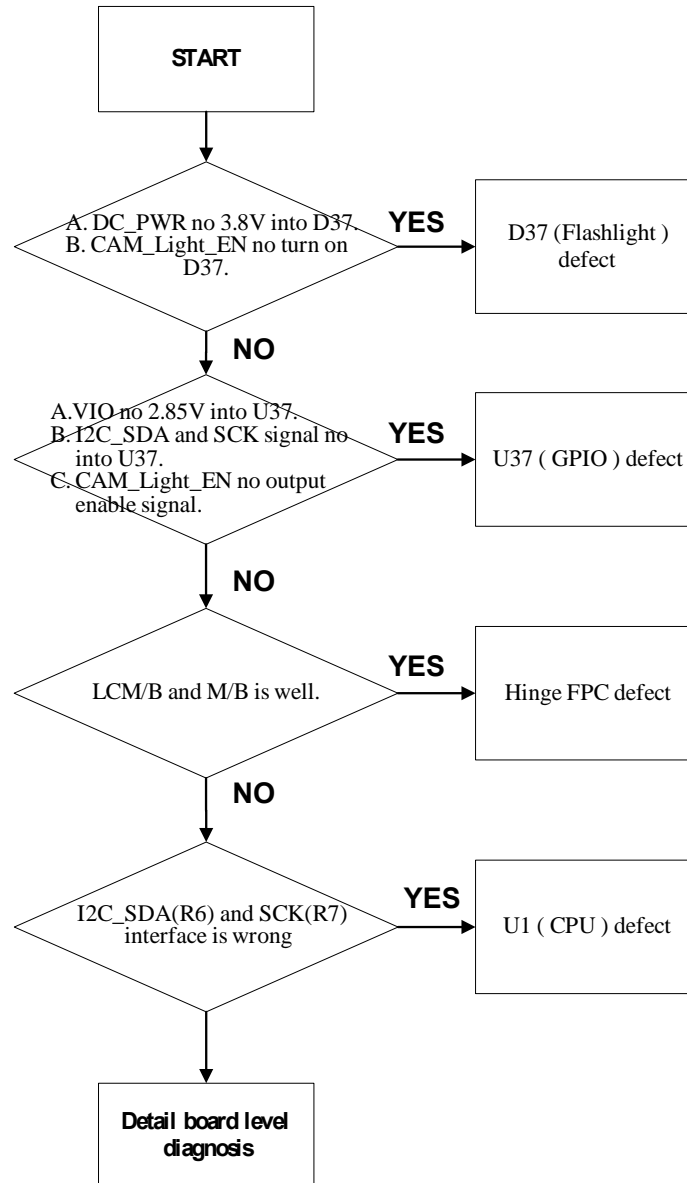
CAM_LIGHT_EN :S/W enable U37(GPIO) to control Q1 on/off.

Application

CPU send signal to U37(GPIO) then enable Q1 to control Flashlight on/off.



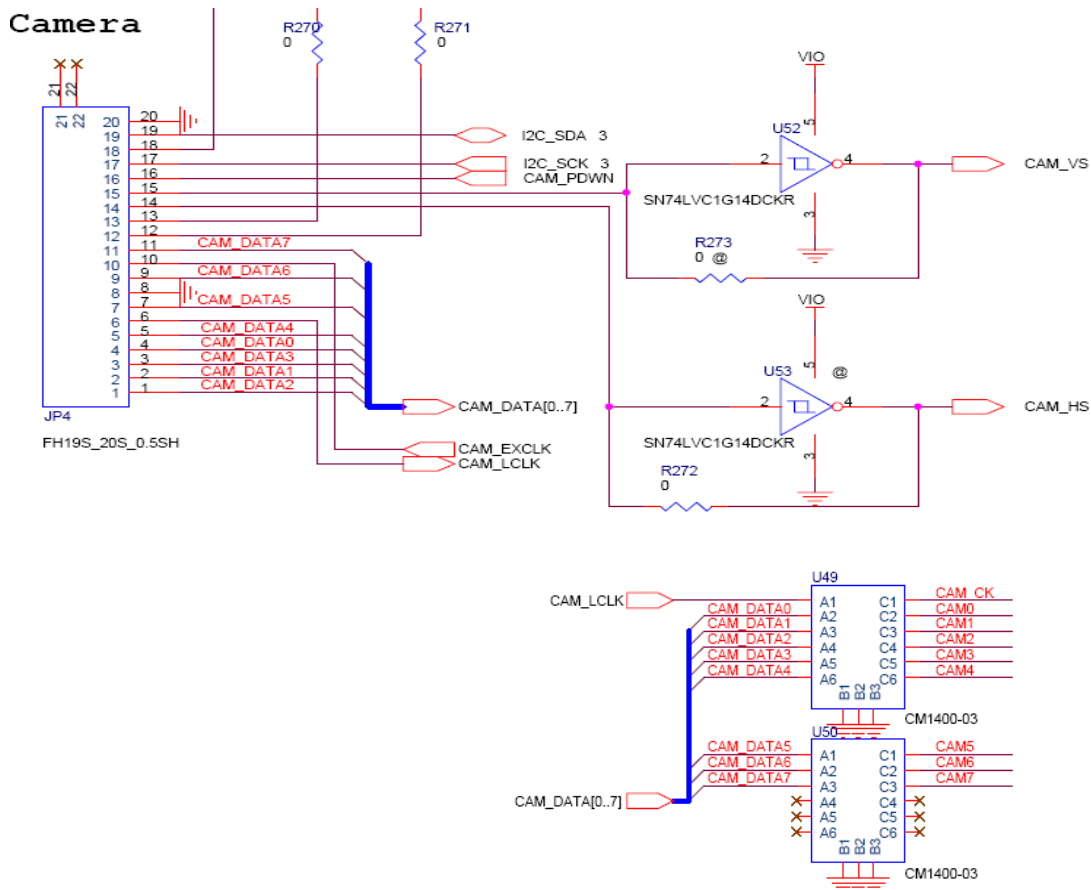
3-4-2. Camera Flashlight function failure analysis Flow Chart





3-5. Camera Circuit

3-5-1. Camera circuit description



Description

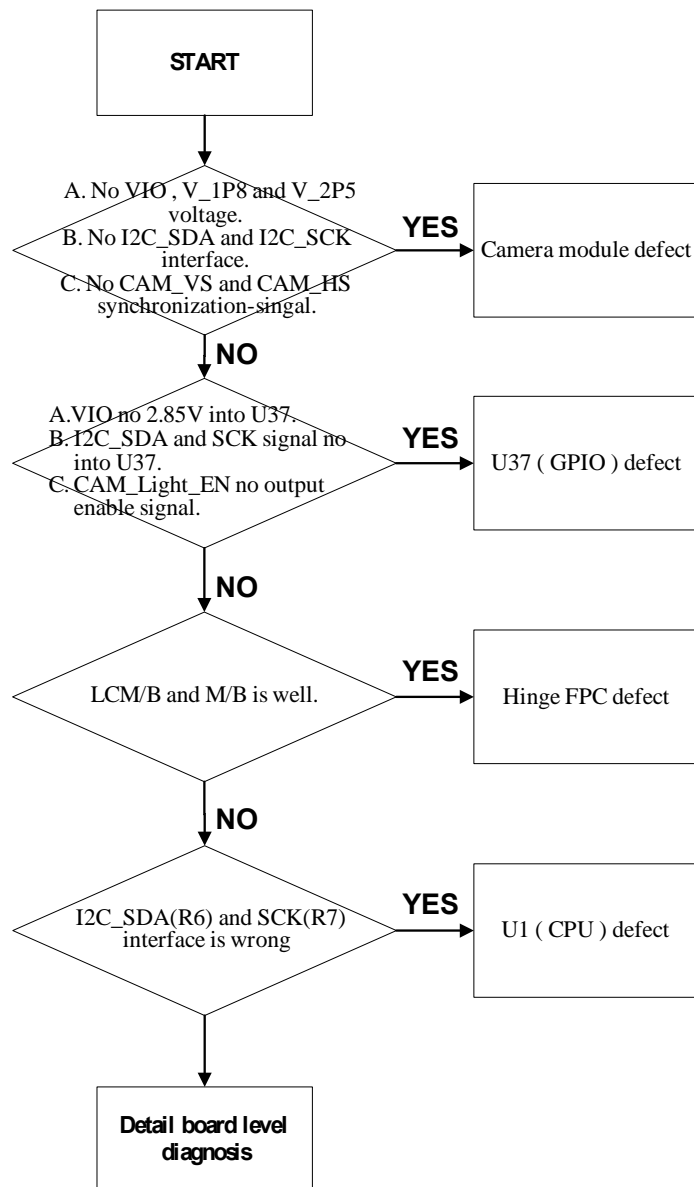
- a: **CAM_PDWN** : S/W enable control camera module on/off.
- b: **CAM_VS,CAM_HS** : control vertical and level synchronization-signal.
- c: **I2C_SDA,I2C_SCK** : Camera control interface.
- d: **CAM_DATA** : send camera DATA to pass through U49,U50(filter) then into CPU.

Application

CPU control signal to U37(GPIO) then enable Camera Module on/off.



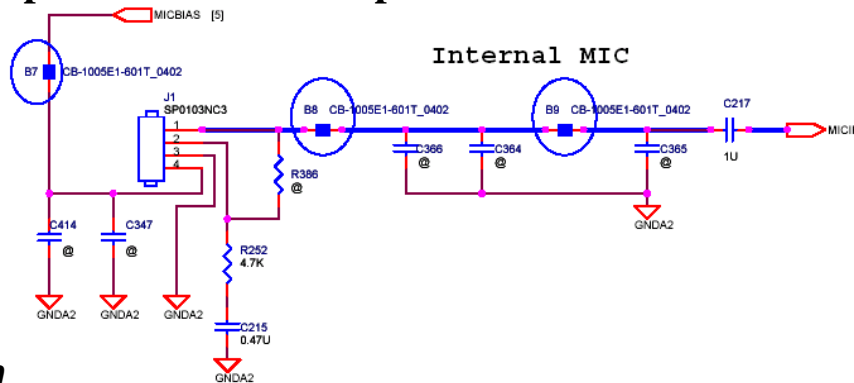
3-5-2. Camera function failure analysis Flow Chart





3-6. Microphone Circuit

3-6-1. Microphone circuit description



Description

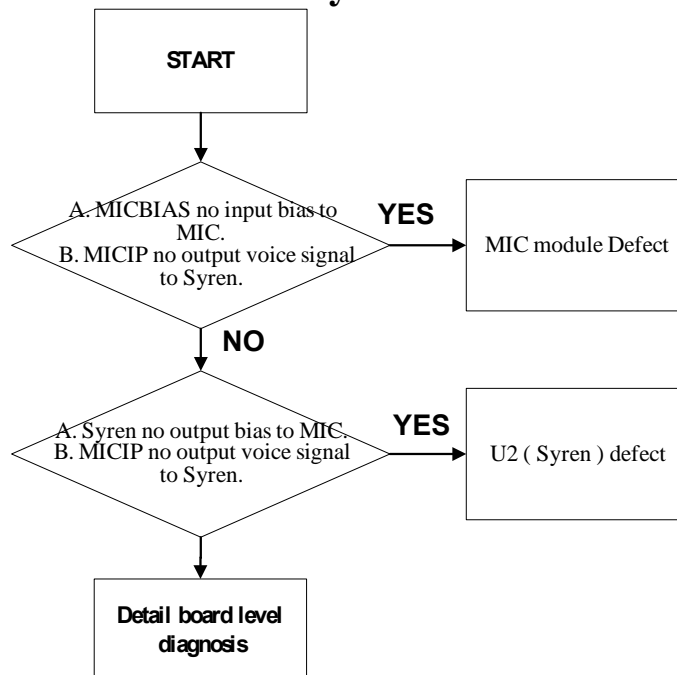
a: **MICBIAS** : Syren output a bias to MIC and control on/off.

b: **MICIP** : Output voice-signal to Syren.

Application

Syren enable MIC then output voice-signal to pass through L/C (filter) into Syren.

3-6-2. Microphone function failure analysis Flow Chart





3-7. SD slot Circuit

3-7-1. SD slot circuit description

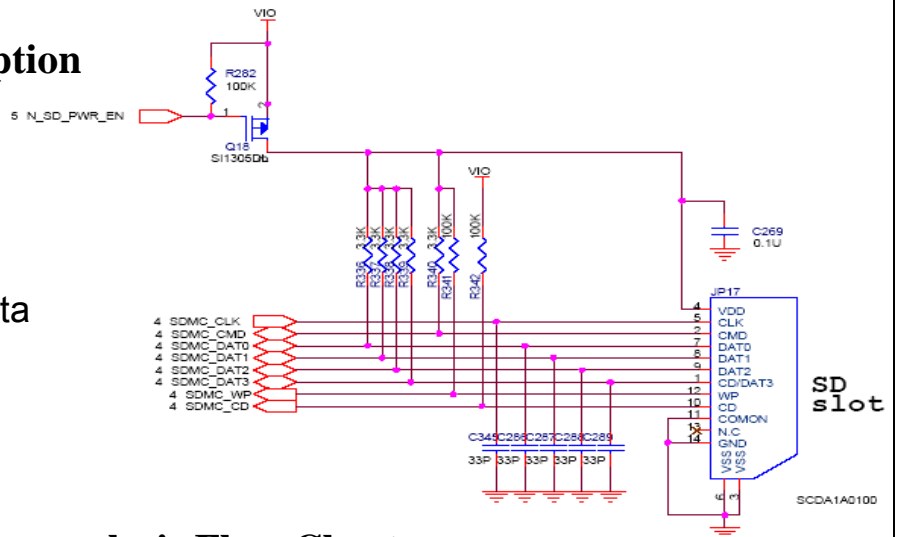
Description

a: **N_SD_PWR_EN** :

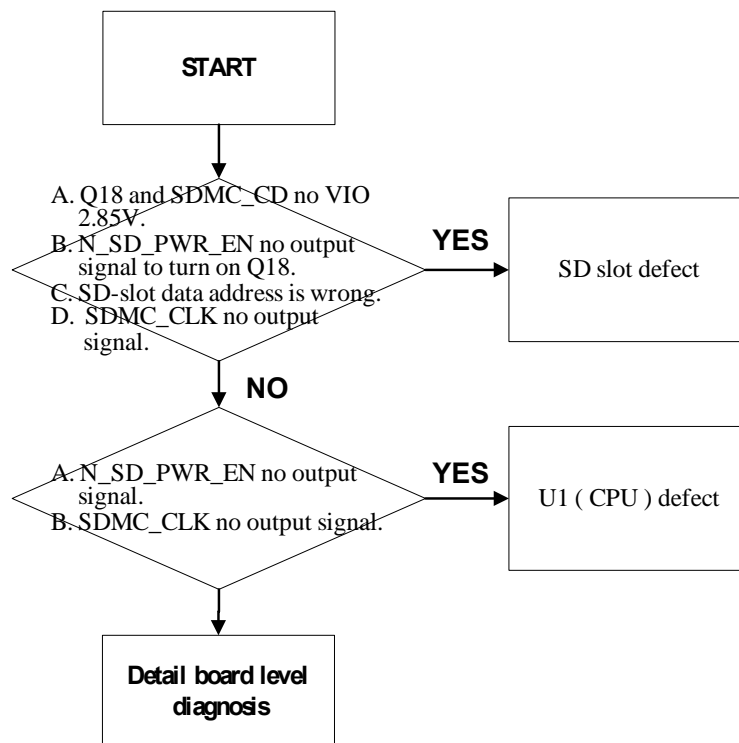
On/Off SD card power

b: **SDMC_DAT0-DAT3** :

Between CPU and SD card data



3-7-2. SD slot function failure analysis Flow Chart



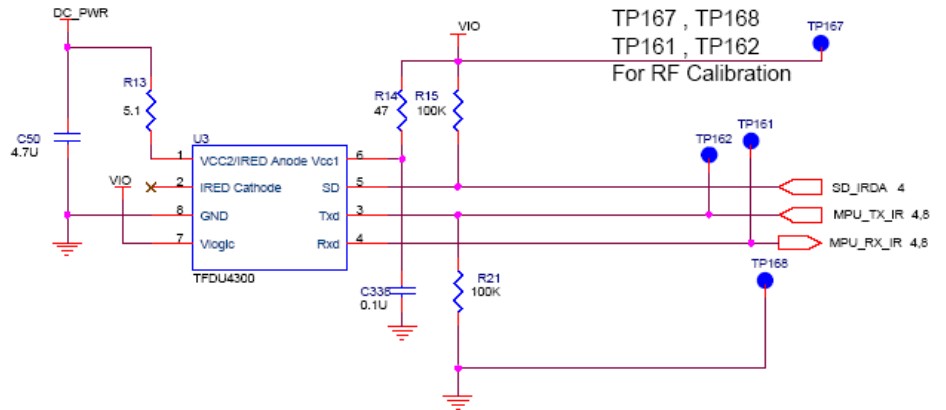


3-8. IrDA Circuit

3-8-1. IrDA circuit description

Description

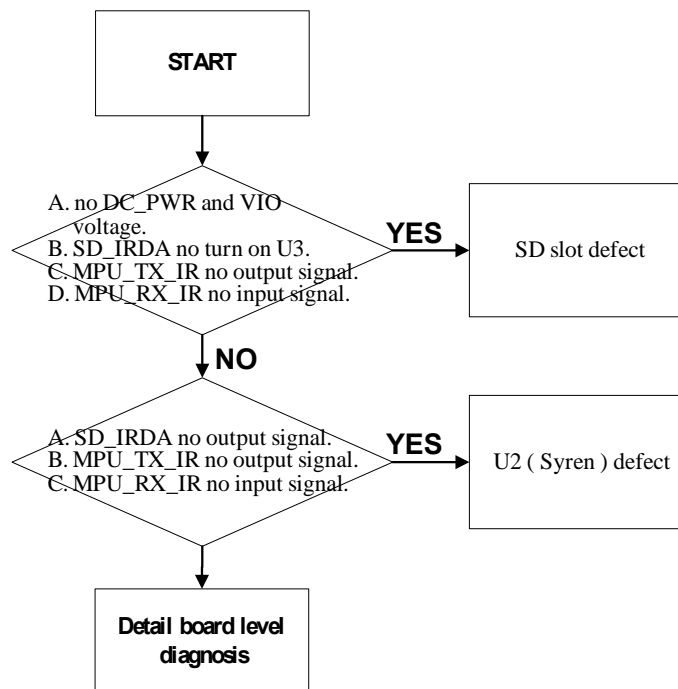
- a: SD_IRDA :S/W enable U3 on/off.
- b: MPU_TX_IR :TX Path.
- c: MPU_RX_IR :RX Path.



Application

CPU turn on U3 and MPU_TX_IR send 115.2khz pulse-signal to search ,if get signal MPU_RX_IR feedback 115.2khz pulse-signal into CPU.

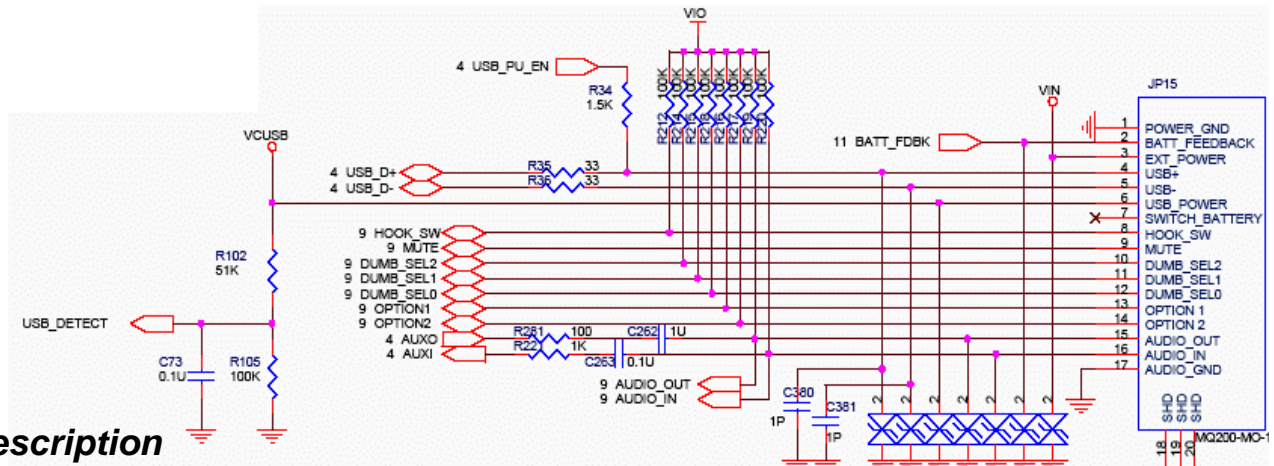
3-8-2. IrDA function failure analysis Flow Chart



3-9. USB Circuit



3-9-1. USB circuit description



Description

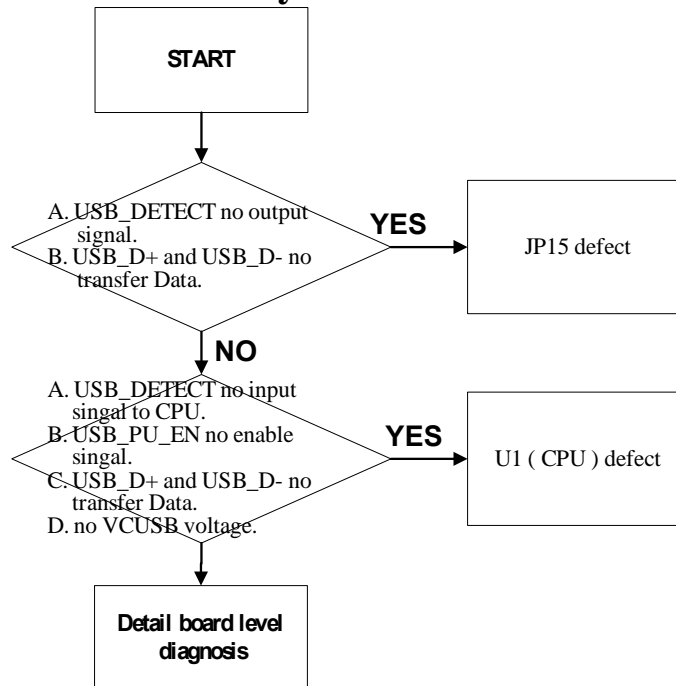
A: **USB_DETECT** : Inform CPU work.
 C: **USB_D+,USBD-** : Transfer DATA

B: **USB_PU_EN** :S/W enable on/off

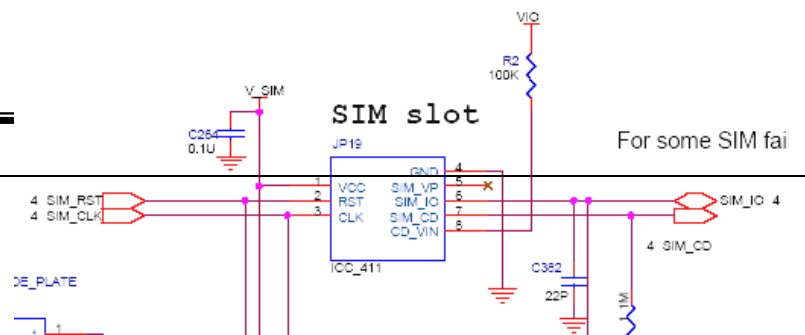
Application

USB_DEFECT inform CPU then CPU enable turn on USB.

3-9-2. USB function failure analysis Flow Chart



3-10. SIM slot Circuit





3-10-1. SIM slot circuit description

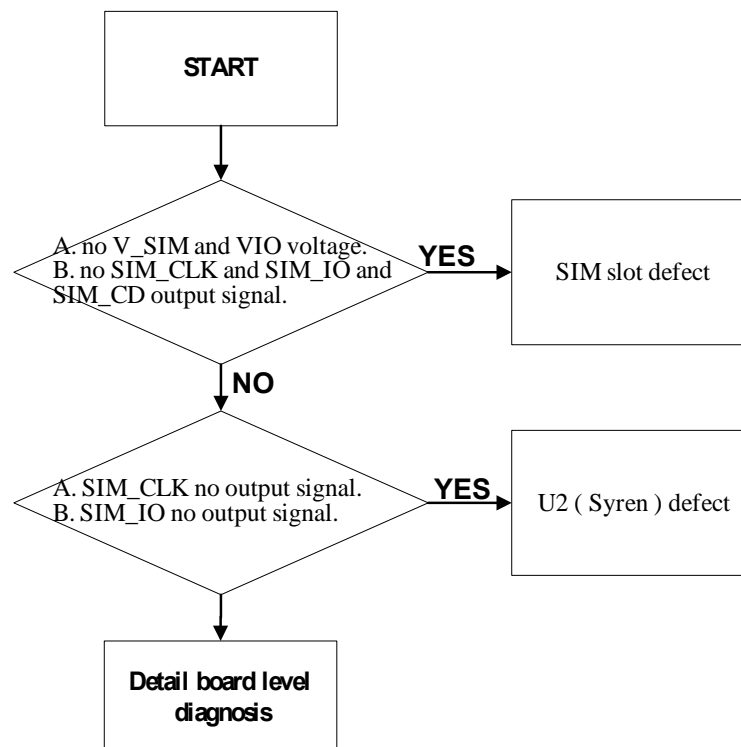
Description

- A:SIM_RST :RESET
- B:SIM_CLK : CLCK
- C:SIM_IO : SIM DATA I/O
- D:SIM_CD : Detect SIM Card
plug in

Application

SIM Card plug in → "SIM_CD" assert →notice CPU →system warm boot
→CLK, data transfer → SIM function start work

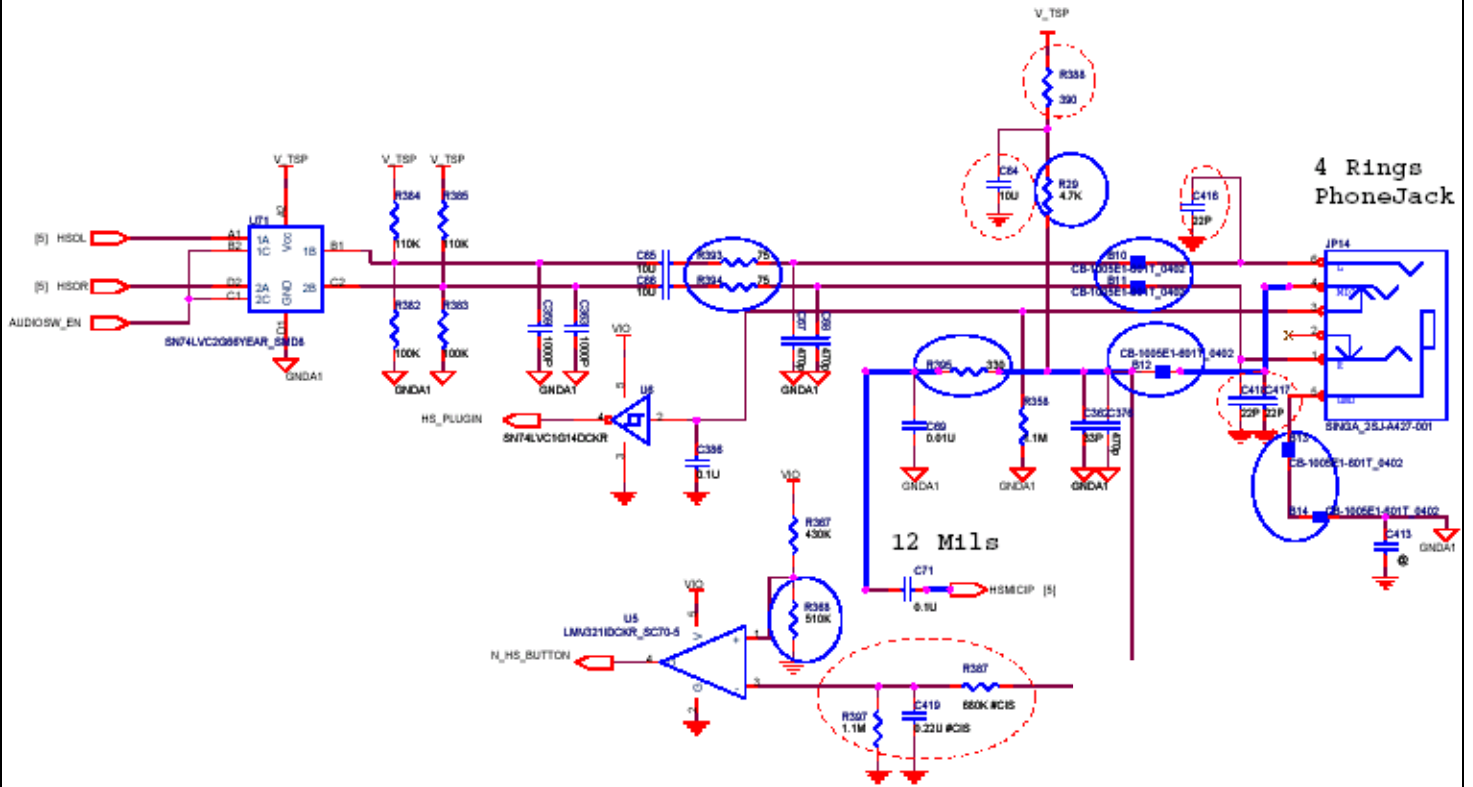
3-10-2. SIM slot function failure analysis Flow Chart



3-11. Phonejack Circuit



3-11-1. Phonejack circuit description



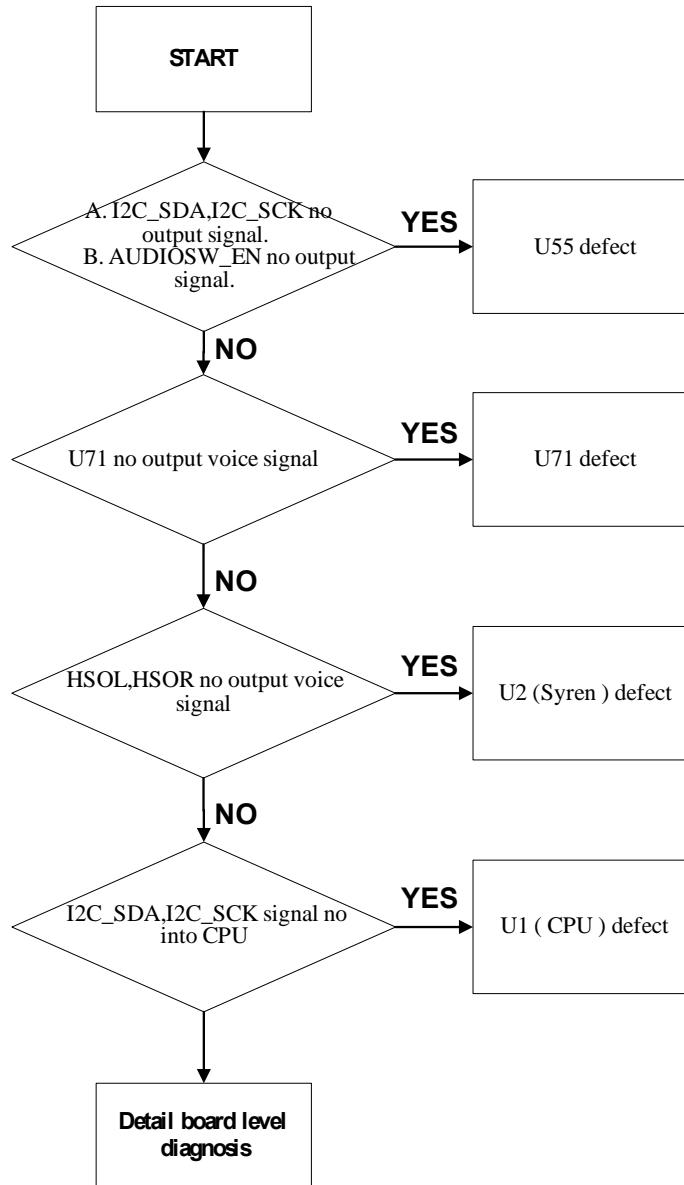
Description

- A. **HS_PLUGIN** : Detect Phonejack
- B. **Audiosw_sw** : SW enable
- C. **HSOL , HSOR** : voice signal output

Application

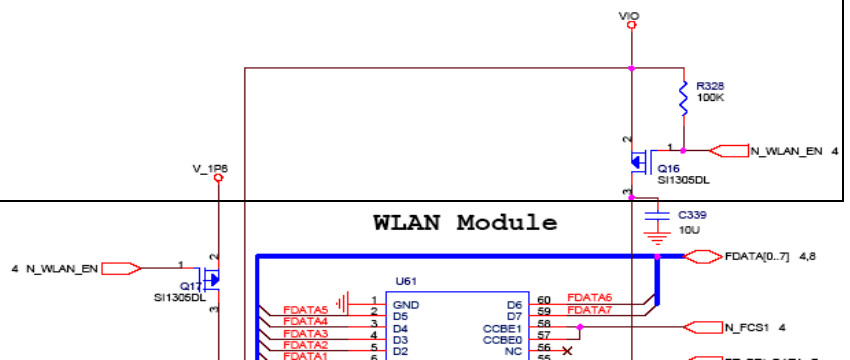
HS_PLUGIN to U55(GPIO) -> output **AUDIOSW_EN**. U55 I2C inform CPU -> Syren output signal (**HSOR,HSOL**).

3-11-2. Phonejack function failure analysis Flow Chart



3-12. WLAN Circuit

Rev: 1.0





3-12-1. WLAN circuit description

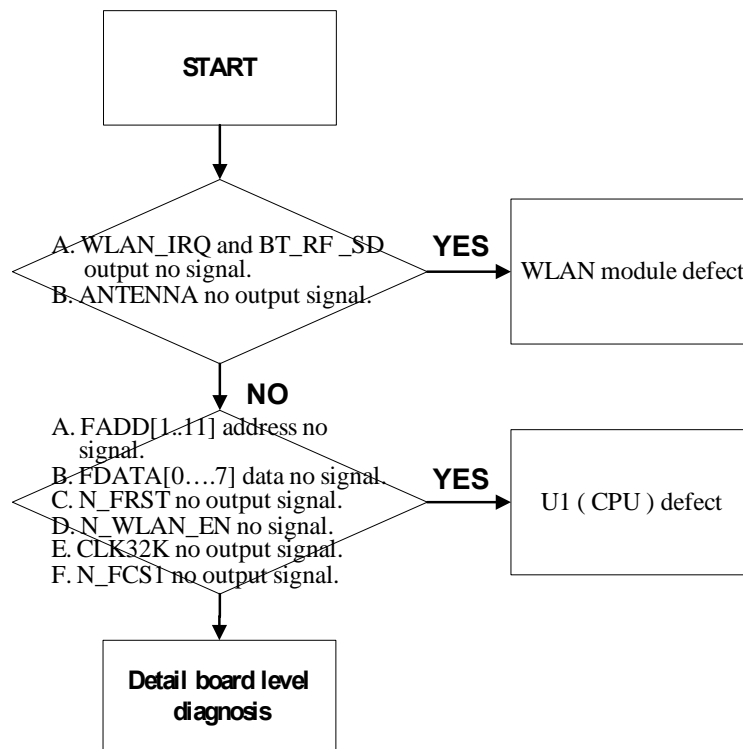
Description

A: CLK32K : CLCK

B: N_WLAN_EN : SW enable

C: N_FCS1: chip select

3-12-2. WLAN function failure analysis Flow Chart



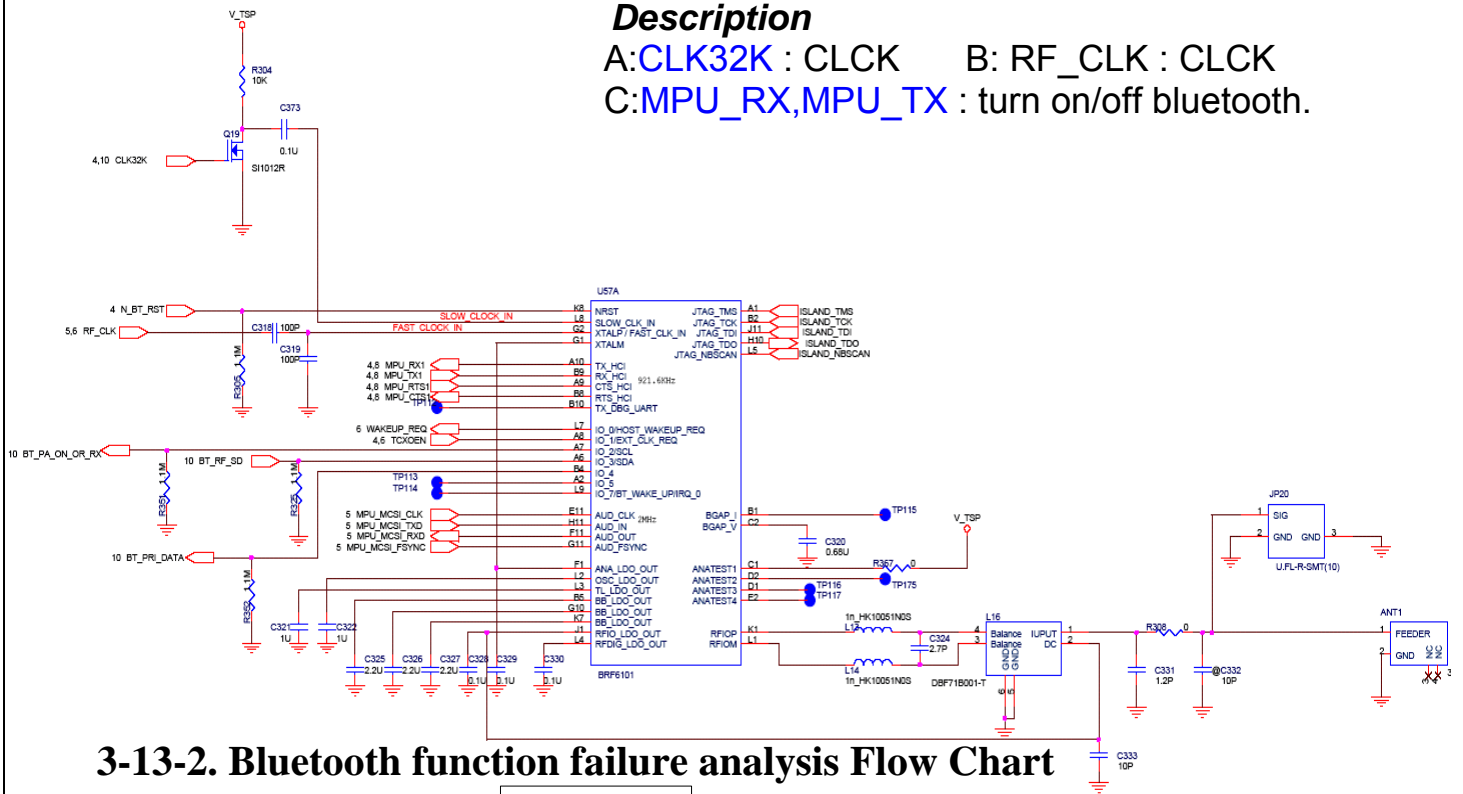
3-13. Bluetooth Circuit

3-13-1. Bluetooth circuit description

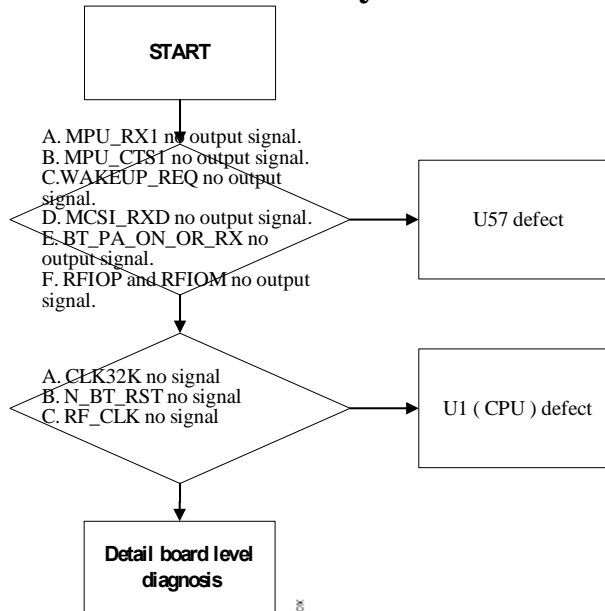


Description

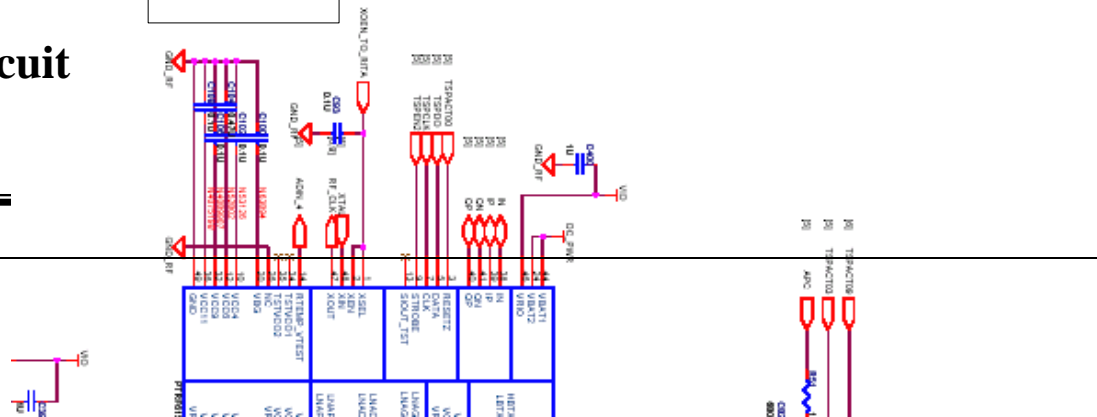
A:CLK32K : CLCK B: RF_CLK : CLCK
 C:MPU_RX,MPU_TX : turn on/off bluetooth.



3-13-2. Bluetooth function failure analysis Flow Chart



3-14. RF Circuit

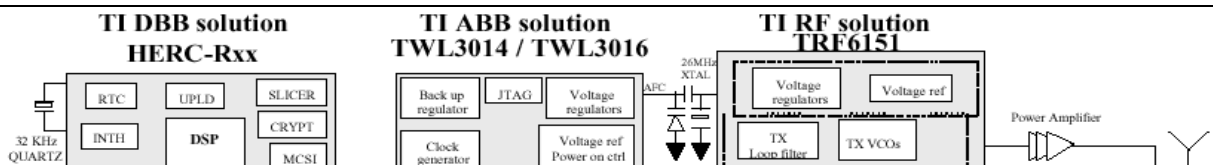


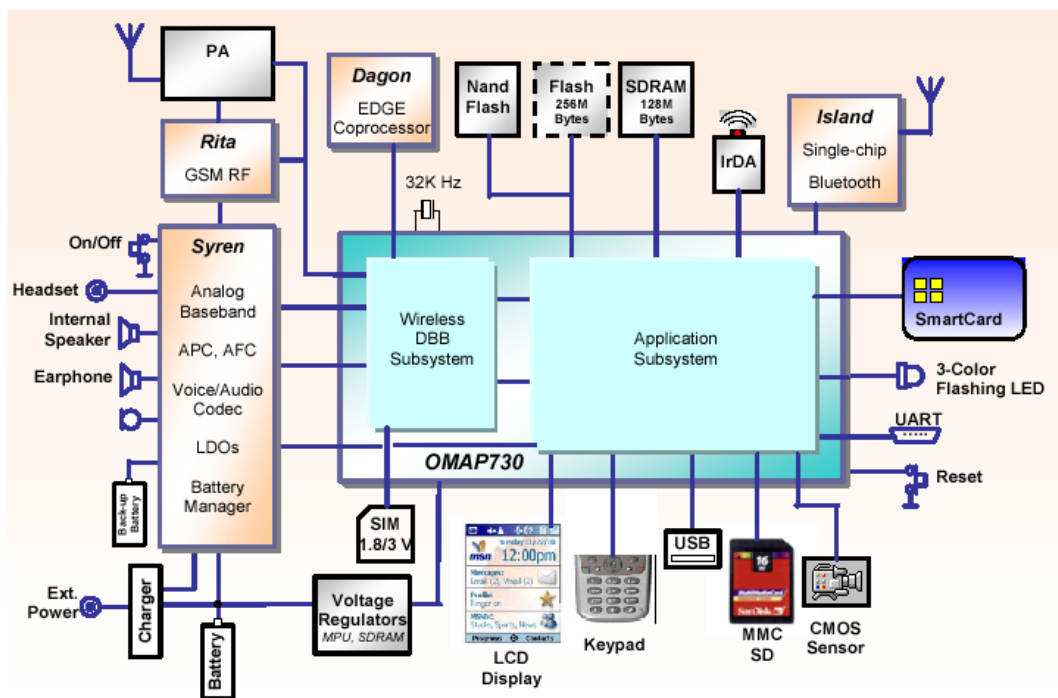


3-14-1. RF circuit description A. Introduction

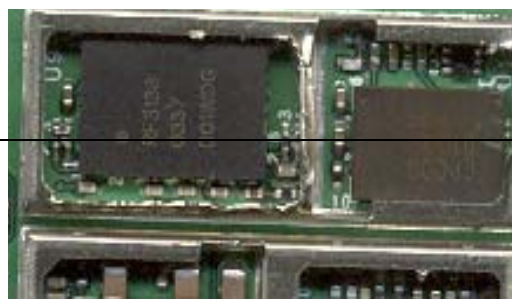
TI chipset = HERC-Rxx + TWL3014 / TWL3016 + TRF6151

Rev: 1



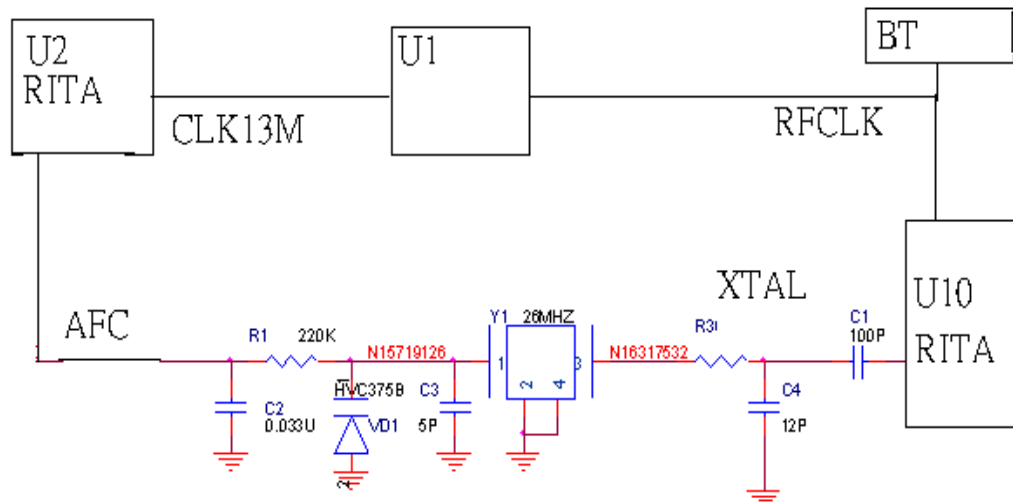


B. RF PCB appearance

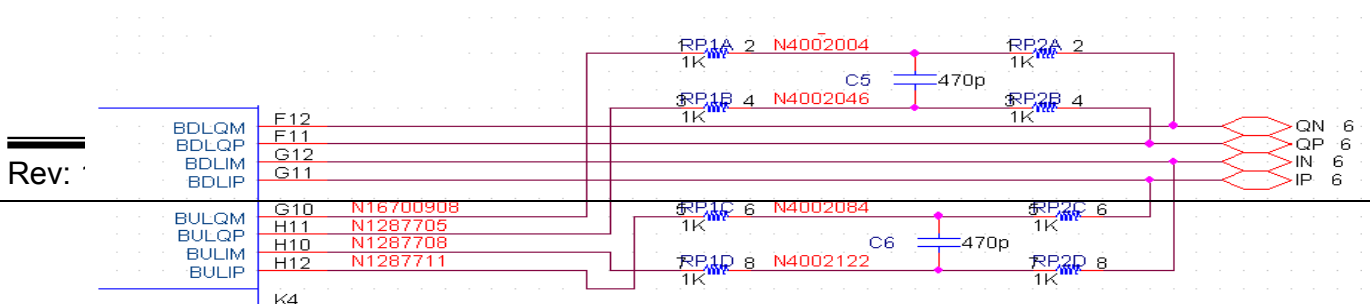




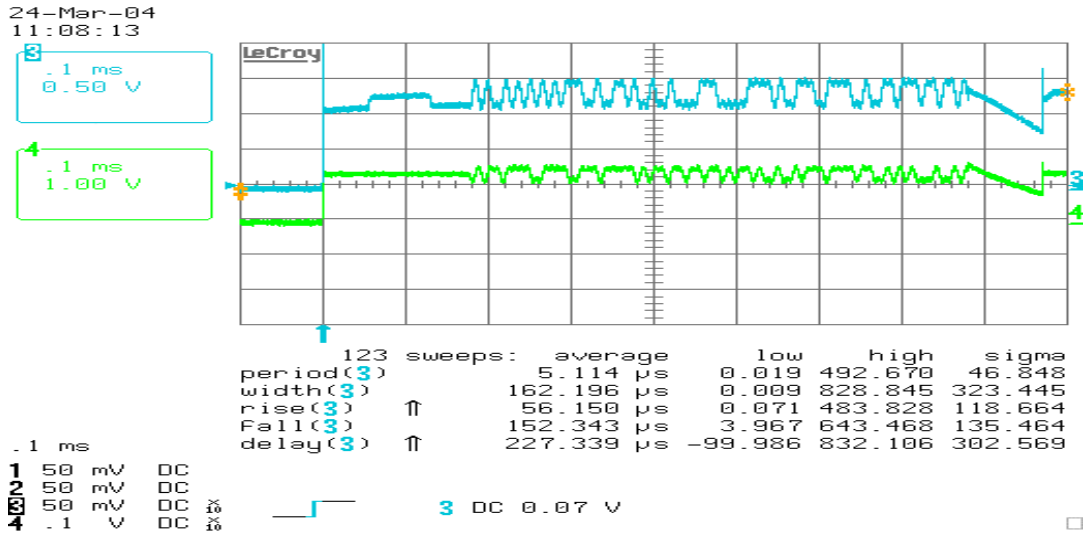
C. External crystal (AFC circuit loop)



D. I/Q



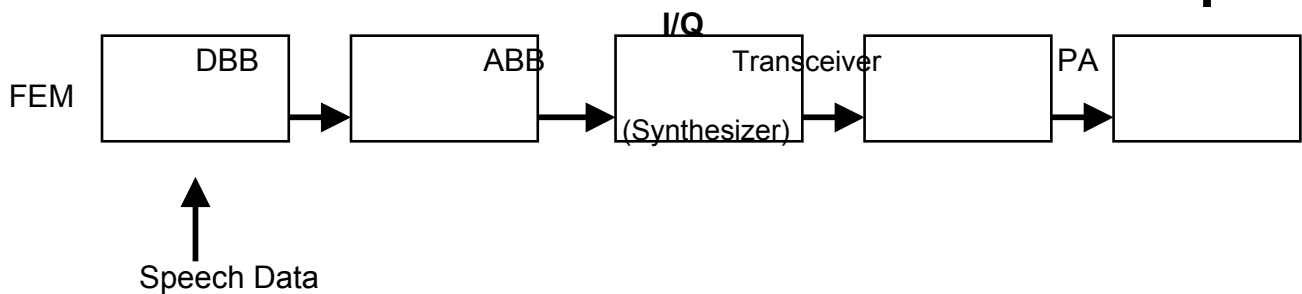
Rev:



E. Transmitter path

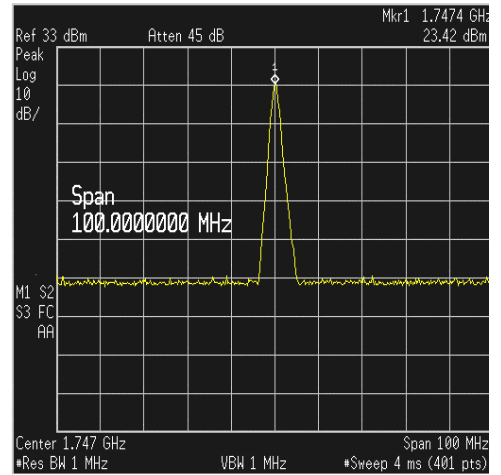
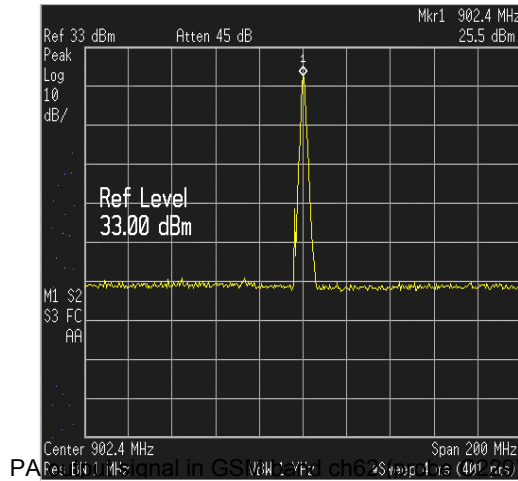
ANT

1. Function block

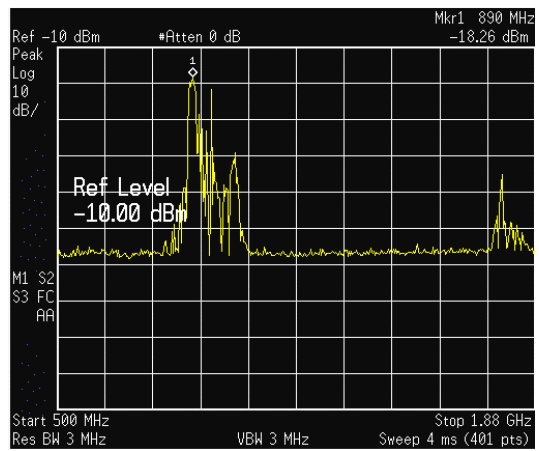
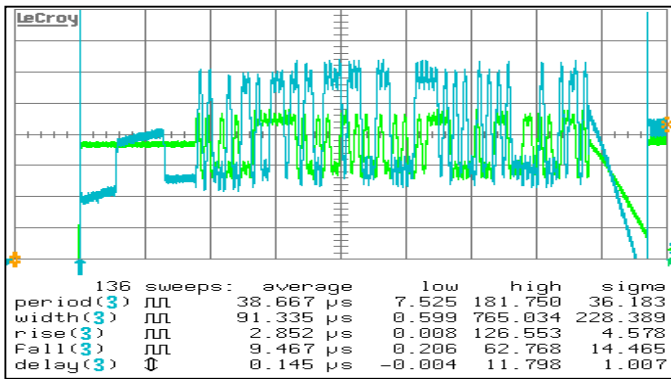


2. System view

SYREN (I/Q) --> RITA (RF) --> PA --> FEM --> RF connector --> Ant(Radio)

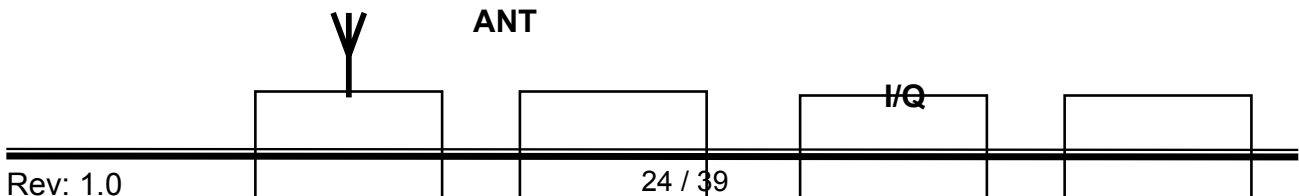


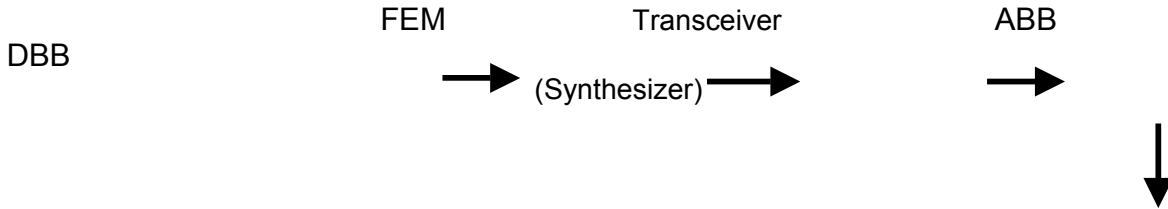
PA output signal in DCS band ch036 (probe C250)



F. Receive path

1. Function block

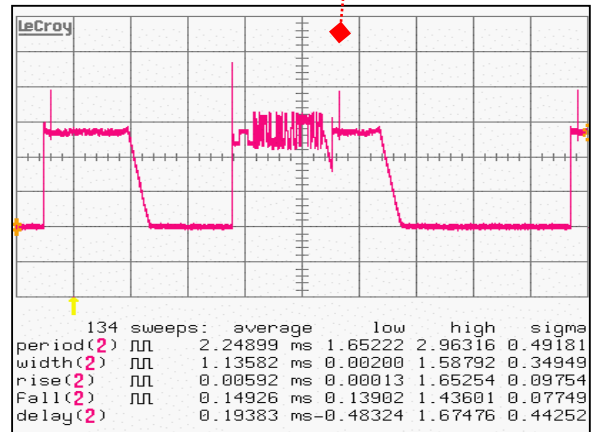
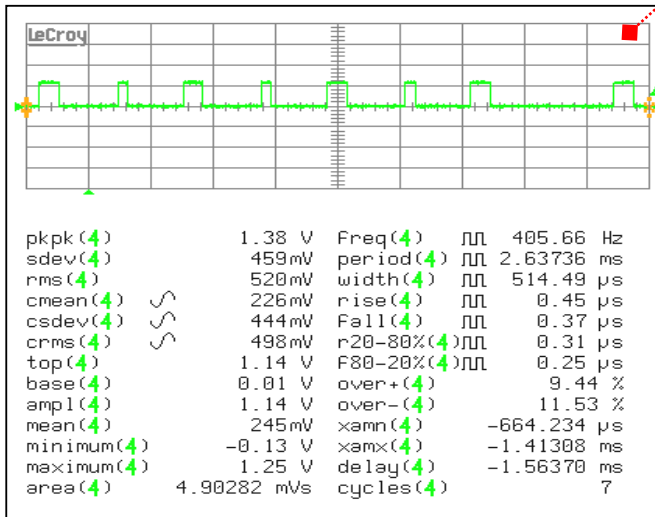




Speech Data

2. System view

Ant(Radio) --> RF connector --> FEM --> RITA (I/Q) --> SYREN



3-14-2. Transmitter failure analysis Flow Chart

1. Signal Tracking.

-> Must make sure B.B is OK first ,like all clock , power are OK.



2. TX Control Signal

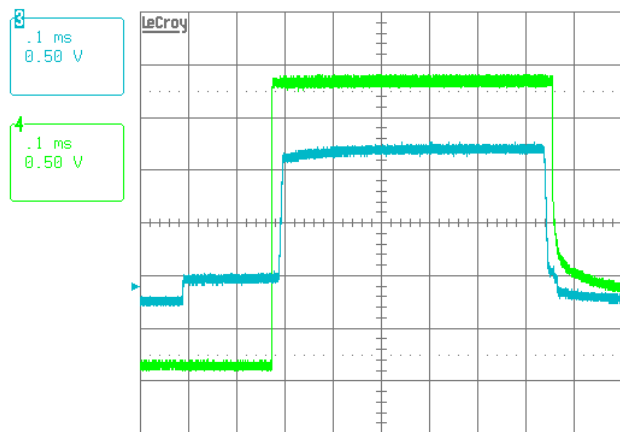
Band select pin2 (U9): switch PA works in which band from U1.

Tx enable pin3 (U9): enable PA works in burst mode from U1.

Tx switch on pin7, 8, 9 (U15): enable PA tx power through FEM to RF connector.

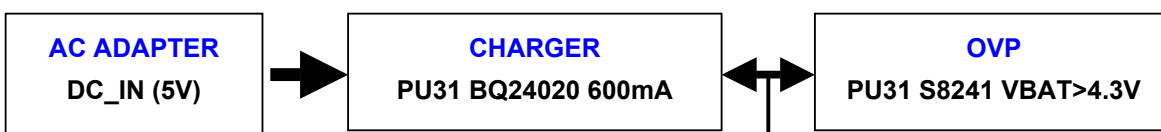
Switch	TX850/900	TX1800/1900	RX850
CTRL1	2.8V	0V	0V
CTRL2	0V	2.8V	0V
CTRL3	0V	0V	2.8V
All 0V for RX900/RX1800/RX1900			

Vramp pin 6 (U9): ramp signal from U2.



3-15. Charging & Power circuit description

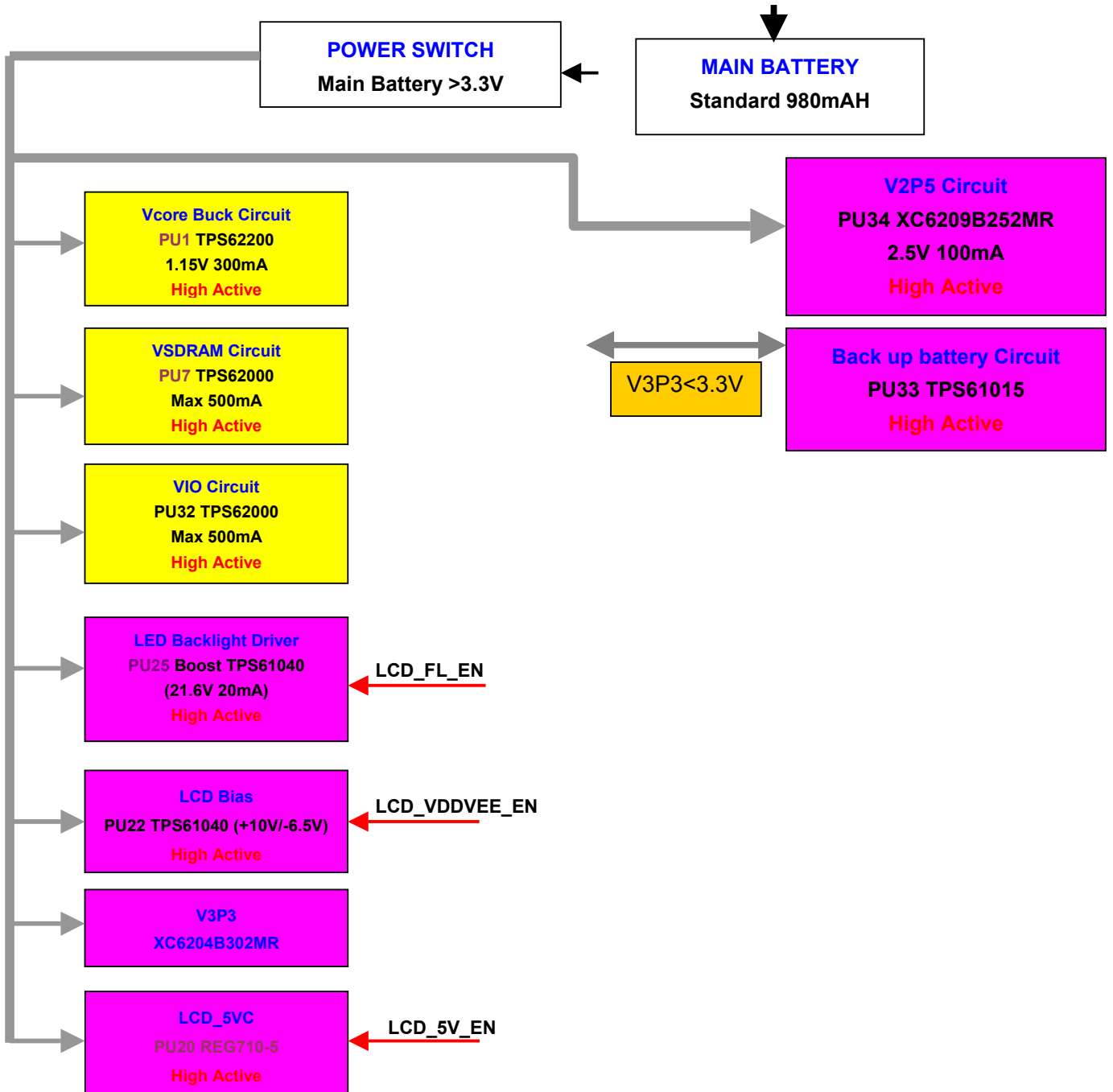
Power System Block Diagram

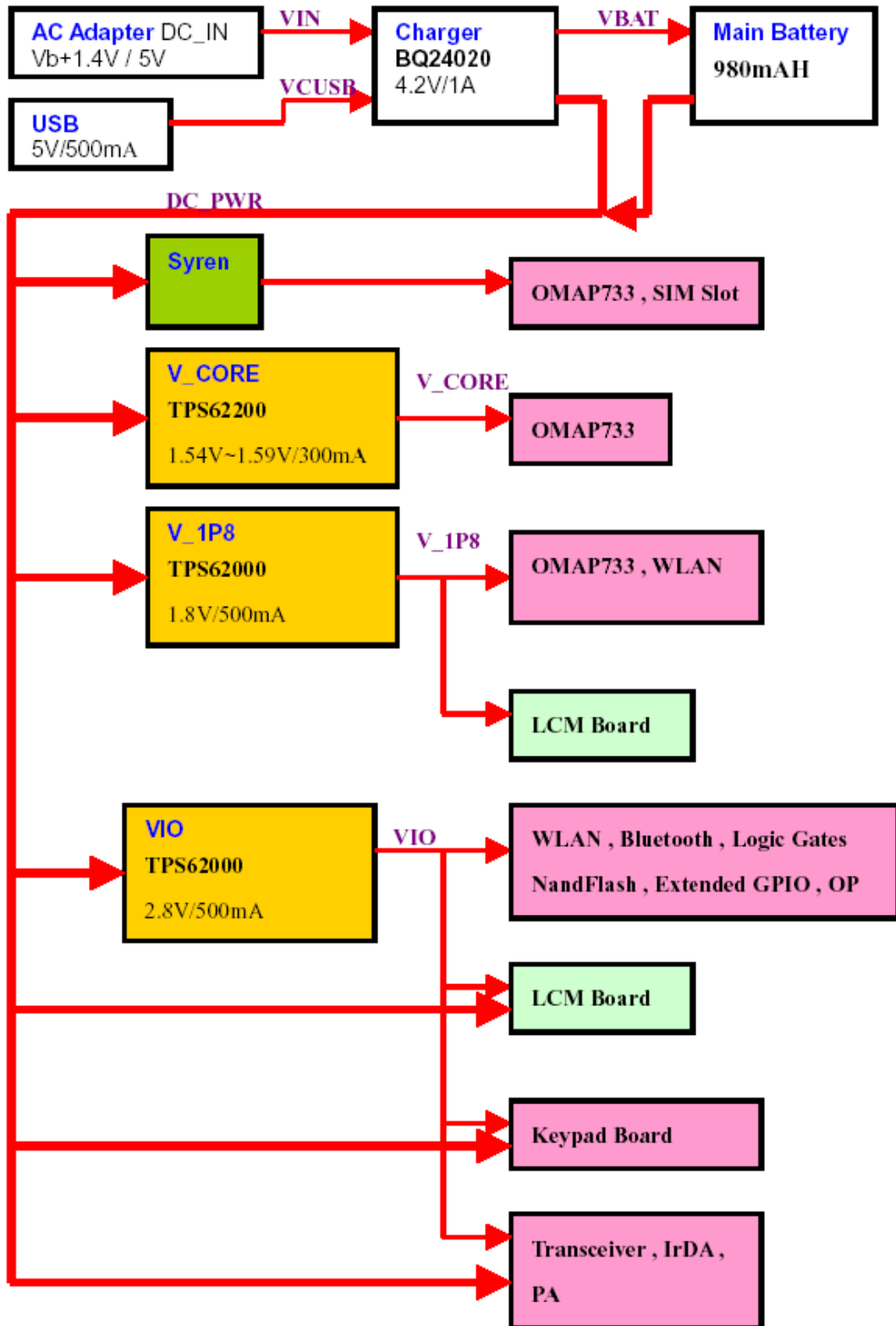




Control Document

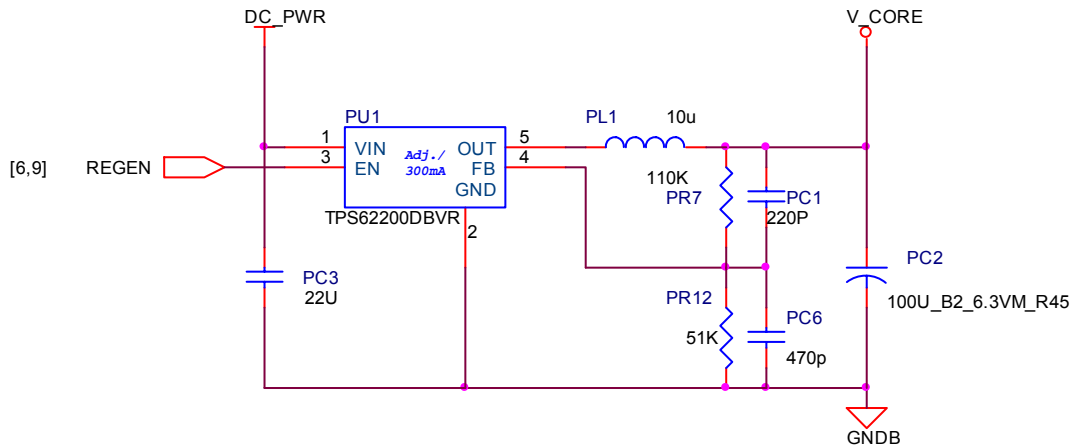
Doc. No:





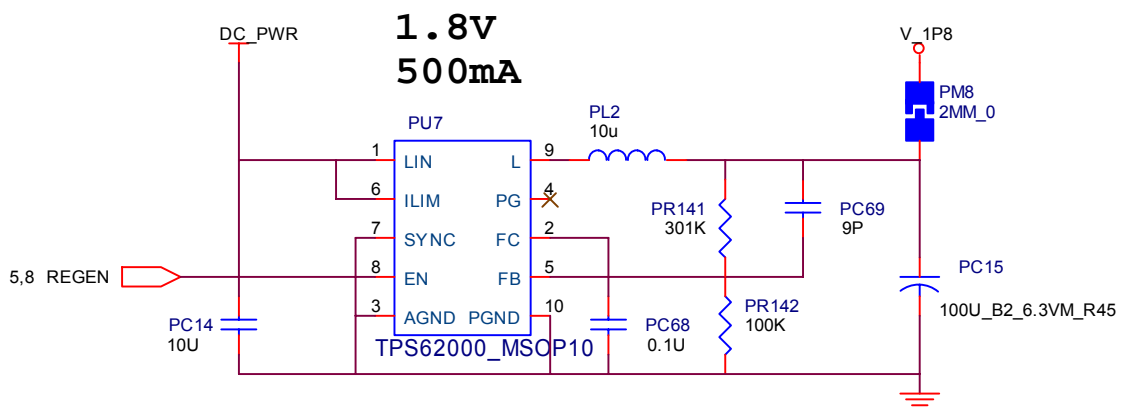


3-15-1. V_CORE power 1.5VDC



	MIN	TYPICAL	MAX	
PR7	108900	110000	111100	ohm
PR12	50589	51100	51611	ohm
VFB	0.485	0.5	0.515	V
VCORE	1.508357	1.576321	1.646007	V

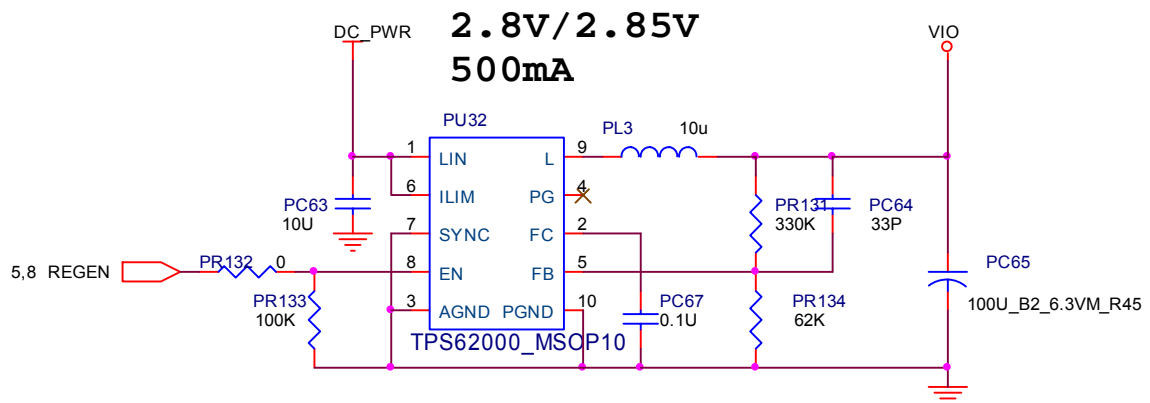
3-15-1. VSDRAM power 1.8V





	MIN	TYPICAL	MAX	
PR141	297990	301000	304010	ohm
PR142	99000	100000	101000	ohm
PU8.FB	0.4365	0.45	0.468	V
V_3P3	1.724348	1.8045	1.905138	V

3-15-2. VIO power 1.8VDC

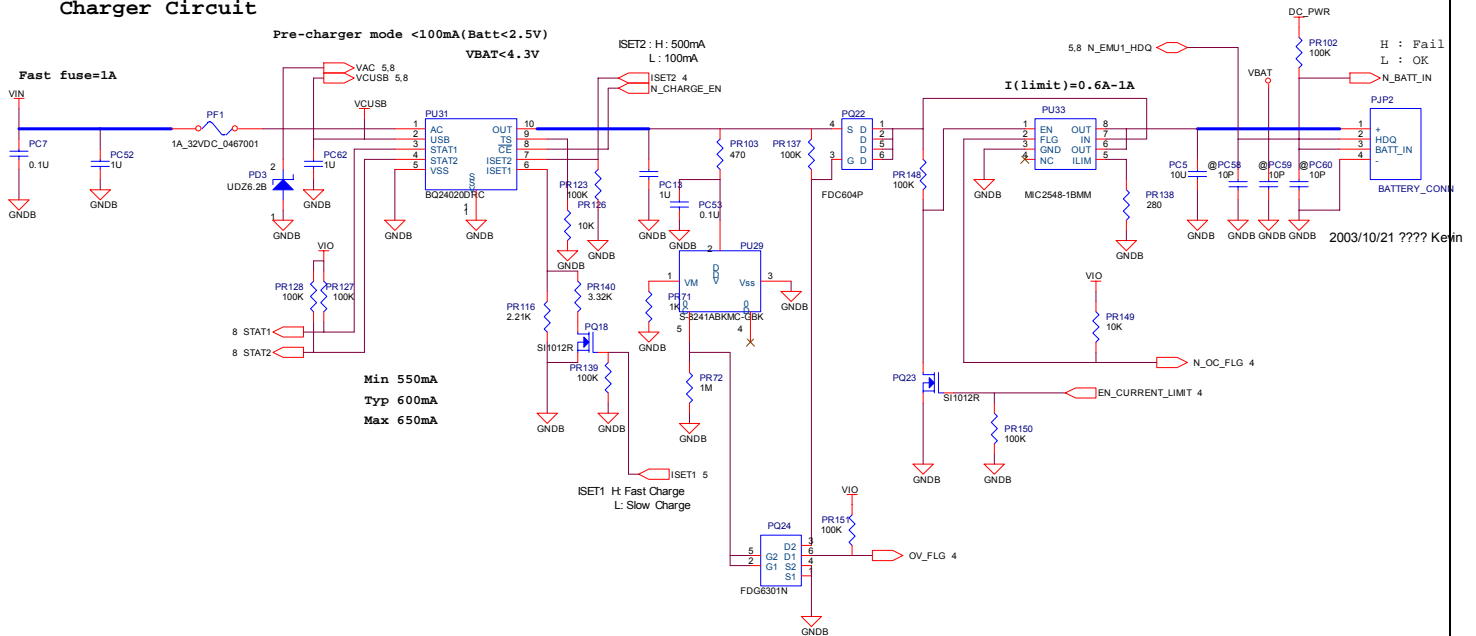


	MIN	TYPICAL	MAX	
PR131	328680	332000	335320	ohm
PR134	61380	62000	62620	ohm
PU8.FB	0.4365	0.45	0.468	V
V_3P3	2.727602	2.859677	3.024692	V



3-15-3. Charger circuit power

Charger Circuit



● FEATURES

Charges and Powers Systems from Either AC Adapter or USB With Autonomous Power-Source Selection

- * Integrated USB Control With Selectable 100 mA and 500 mA Charge Rates
- * Ideal for Low-Dropout Charger Designs for Single-Cell Li-Ion or Li-Pol Packs in Space Limited Portable Applications
- * Integrated Power FET and Current Sensor for Up to 1-A Charge Applications From AC Adapter
- * Pre-charge Conditioning With Safety Timer
- * Power Good (AC Adapter Present) Status Output
- * Optional Battery Temperature Monitoring Before and During Charge
- * Automatic Sleep Mode for Low-Power Consumption
- * Criteria For Main PCB Power

- I (out) = 600mA
- I (usb)=500mA/100mA

The bqTINY-II offers on-chip current regulation with programmable set point. The resistor connected between the ISET1 and VSS, RSET, determines the AC charge rate. The V(SET) and K(SET) parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}}$$



Control Document

Doc. No:

During a charge cycle if the battery voltage is below the V (LOWV) threshold, the bqTINY-II applies a pre-charge current, I_o (PRECHG), to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and V_{ss}; R_{SET}, determines the pre-charge rate. The V (PRECHG) and K (SET) parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{O (PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}}$$

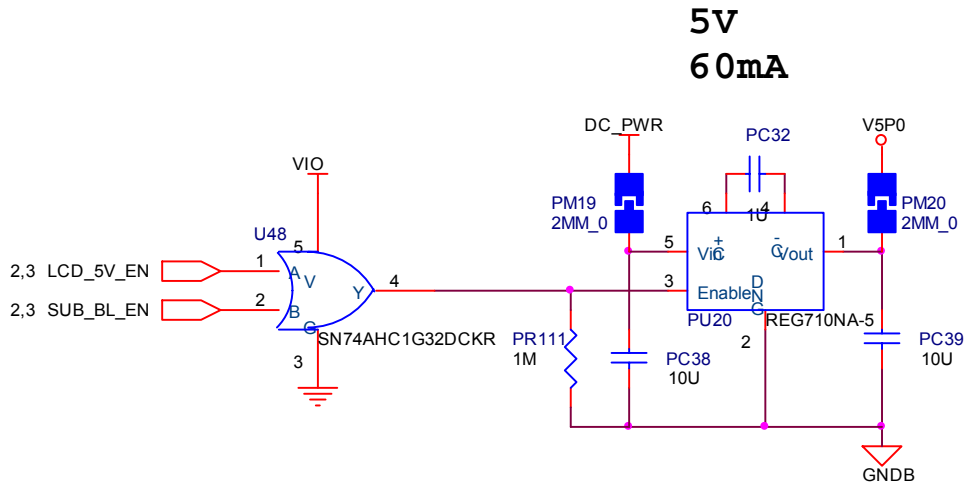
	MIN		MAX
MIC2548	184	230	276
			(MAX)1A
SET RES(OHM)(+/-0.5%)	278.6	280	281.4
SET CURRENT(A)	0.653873	0.821429	0.990668

SET RES(OHM)(+/-0.5%)	2198.95	2210	2221.05	
K(SET)	307	322	337	
V(SET)	2.463	2.5	2.538	
I(out)	0.340443	0.364253	0.388961	mA
				<400mA
SET RES(OHM)(+/-0.5%)	3303.4	3320	3336.6	
RSET	1320.165	1326.799	1333.433	
K(SET)	307	322	337	
V(SET)	2.463	2.5	2.538	
I(out)	0.567063	0.606723	0.647878	mA
				<653.87mA

Follow mic2548 current limit



3-15-4. LCD_5V 5VDC



● FEATURES

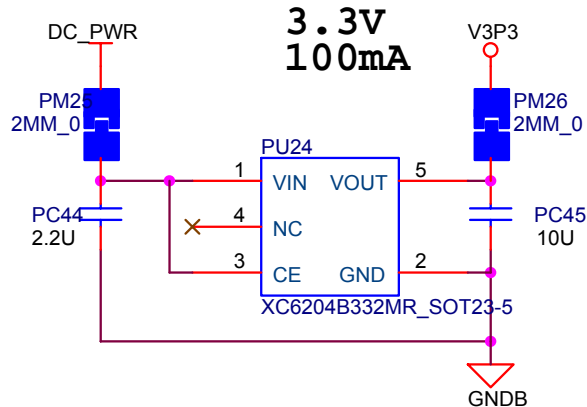
- _ Wide Input Range: 1.8V to 5.5V
- _ Automatic Step-Up/Step-Down Operation
- _ Low Input Current Ripple
- _ Low Output Voltage Ripple
- _ Minimum Number of External Components~No Inductors
- _ 1MHz Internal Oscillator Allows Small Capacitors
- _ Shutdown Mode
- _ Thermal and Current Limit Protection
- _ Six Output Voltages Available: 5.5V, 5.0V, 3.3V, 3.0V, 2.7V, 2.5V
- _ Small Packages: - SOT23-6 - TSOT23-6 (REG71055 and REG71050 Only)
- _ Evaluation Modules Available:
REG710EVM-33, REG710EVM-5

■ Criteria For Main PCB Power

- $I_p = 60\text{mA}$
- $V_{rp-p} \leq 150\text{mV}$
- Load regulation (max) : $\pm 3\%$
- Turns on : quiescent current (max) 30uA
- PWR_EN = LCD_5V_EN



3-15-5. V3P3 power 3.3VDC



● FEATURES

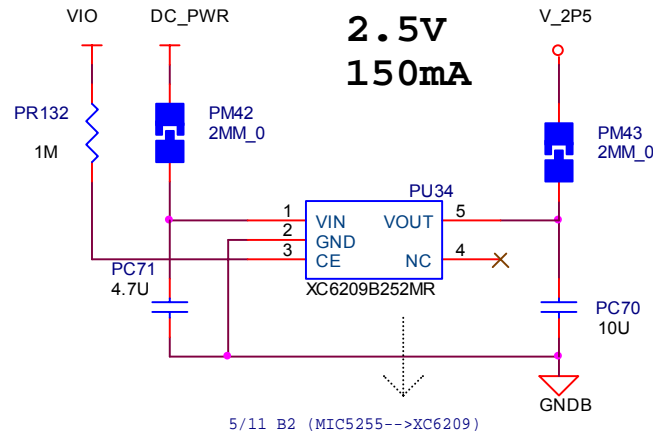
Maximum Output Current: 150mA
Dropout Voltage: 200mV (I_{OUT} = 100mA)
Maximum Operating Voltage: 10V
Output Voltage Range: 1.8V ~ 6.0V in 50mV increments
Highly Accurate : ± 2%
Low Power Consumption : TYP 75µA
Standby Current : less than 0.1µA
Low Output Noise : 30µVrms
Low ESR Capacitor Compatible: Ceramic capacitor

Criteria For Main PCB Power

- I_p = 100mA
- V_{rp-p} 99mV
- Load regulation (max) : ±3%
- Turns on: quiescent current (max) 3µA



3-15-6. V2P5 power 2.5VDC



● FEATURES

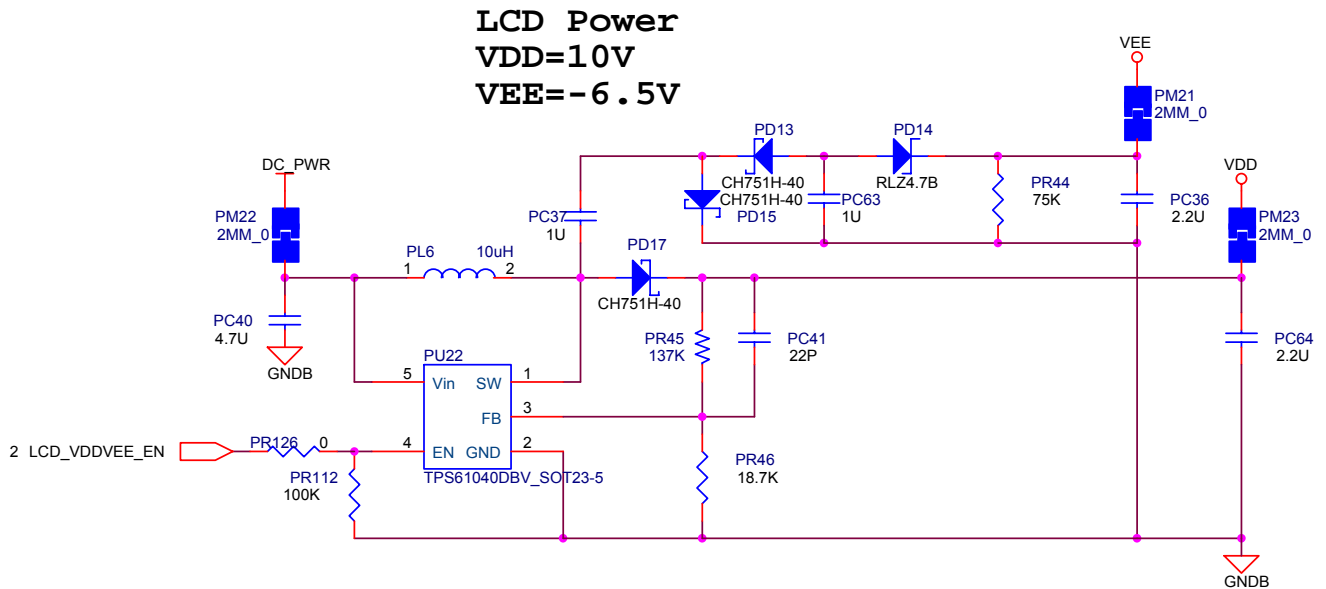
- Applications _ Low Power Consumption : 25 μ A (TYP)
- _ Dropout Voltage: 30mA @ 60mV : 100mA @ 200mV
- _ Maximum Output Current : 200mA
- _ Highly Accurate: $\pm 2\%$ (± 30 mV less than 1.5V)
- _ Output Voltage Range : 0.9V ~ 6.0V (50mV Step)
- _ Low ESR capacitor compatible

Criteria For Main PCB Power

- $I_p = 100$ mA
- $V_{rp-p} \leq 75$ mV
- Load regulation (max) : $\pm 2\%$
- Turns on: quiescent current (max) 3 μ A



3-15-7. LCM power VDD VEE



● FEATURES

- 1.8V to 6V Input Voltage Range
- Adjustable Output Voltage Range to 28V
- 400mA Internals Switch Current
- Up to 1MHz Switching Frequency
- 28uA Typical No Load Quiescent Current
- 1uA Typical Shutdown Current
- Internal Soft start
- Output Voltage Regulation



	min	typical	max
PR45	135630	137000	138370ohm
PR46	18909	19100	19291ohm
PU22.VFB	1.208	1.233	1.258V
VDD	9.701134	10.07703	10.46364V

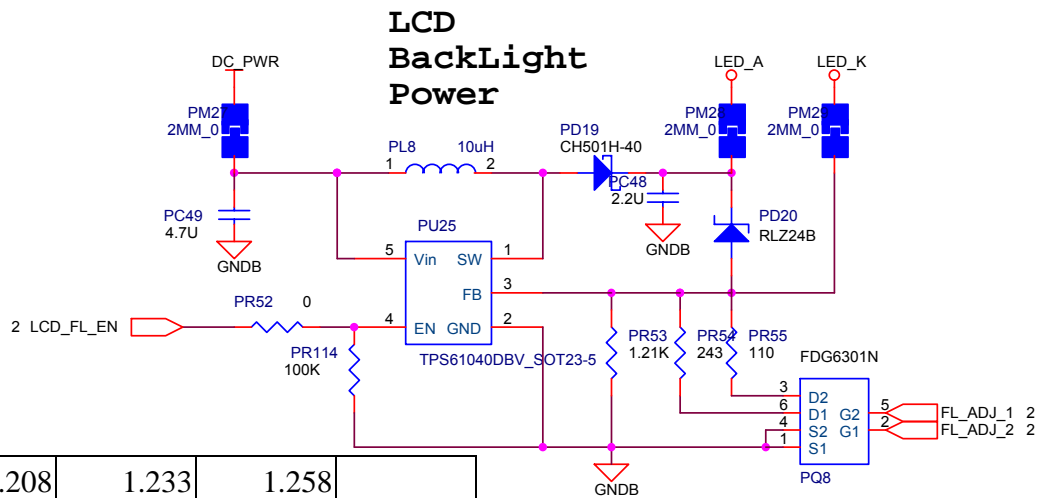
Follow the zener diode curve, we need give -6.5V
 $-6.5V/75000=86\mu A$

VEE max 10uA

From PD14 76uA

Find Zener diode -3.5V RLZ4.7V

3-15-8. LCD back light power 15VDC



PU25.VFB	1.208	1.233	1.258	
PR53	1197.9	1210	1222.1	
PR54	240.57	243	245.43	
PR55	108.9	110	111.1	
STEP1	0.988462	1.019008	1.050171	mA
STEP2	5.910436	6.093082	6.279418	mA
STEP3	11.86155	12.2281	12.60205	mA
STEP4	16.78352	17.30217	17.8313	mA

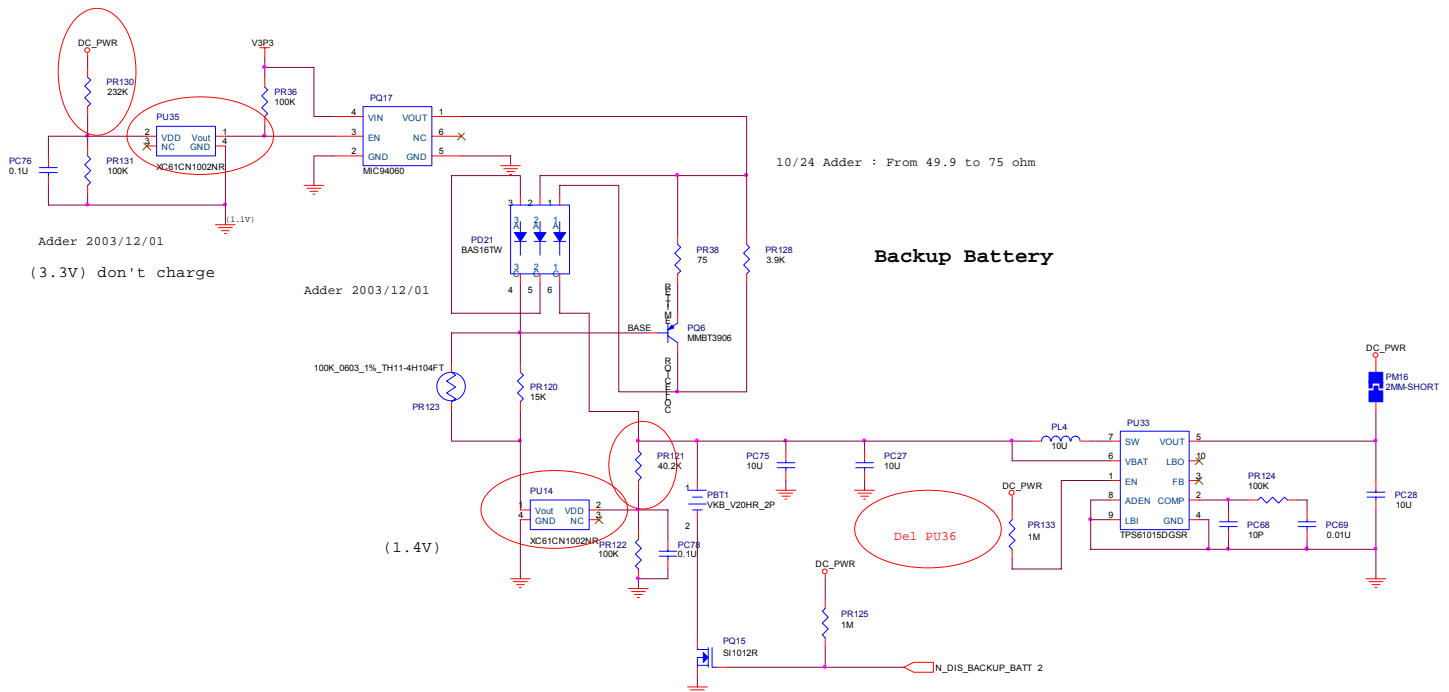


output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{OUT}	Adjustable output voltage range			28	V	
V _{ref}	Internal voltage reference		1.233		V	
I _{FB}	Feedback input bias current	V _{FB} = 1.3 V		1	μA	
V _{FB}	Feedback trip point voltage	1.8 V ≤ V _{in} ≤ 6.0 V	1.208	1.233	1.258	V
	Line regulation (see Note 3)	1.8 V ≤ V _{in} ≤ 6.0 V; V _{out} = 18 V; I _{load} = 10 mA C _{ff} = not connected		0.05		%/V
	Load regulation (see Note 3)	V _{in} = 2.4 V; V _{out} = 18 V; 0 mA ≤ I _{out} ≤ 30 mA		0.15		%/mA

NOTE 3: The line and load regulation depend on the external component selection. Refer to the application section for further information.

3-15-9. Backup battery power 3.0VDC



● FEATURES

- * Integrated Synchronous Rectifier for Highest Power Conversion Efficiency (>95%)
- * Start-Up Into Full Load With Supply Voltages as Low as 0.9 V, Operating Down to 0.8 V.
- * 200-mA Output Current From 0.9-V Supply.
- * Power save-Mode for Improved Efficiency at Low Output Currents.
- * Auto discharge Allows to Discharge Output Capacitor During Shutdown.
- * Device Quiescent Current Less Than 50 mA _ Ease-of-Use Through Isolation of Load From Battery During Shutdown of Converter _ Integrated Anti-ringing Switch Across Inductor.
- * Integrated Low Battery Comparator
- * Micro-Small 10-Pin MSOP Package
- * Applications Include All Single- or Dual-Cell Battery Operated Products Like Internet Audio Players, Pager, Portable Medical Diagnostic Equipment, Remote Control, Wireless Headsets ACTUAL SIZE



■ Criteria For Main PCB Power

- $I_p = 5\text{mA}$
- $V_{rp-p} \square 99\text{mV}$
- Load regulation (max): $\pm 3\%$
- Efficiency: 80% at 1Vdc input (only calculate LED)
Full load: $I_{load} = 5\text{mA}$
- Turn on quiescent current (max): 46uA

* Charge back up battery:

Using current limit, Estimate $1s355 V_F = 0.55$ 2PCS $0.65 * 2 = 1.3\text{V}$
MMBT3094 $V_{be} = 0.8\text{V}$, so PR33 terminal voltage is 0.3V
 $0.3 / 49.9 \text{ ohm} = 0.005\text{A}$ charge current.

XC61CN1002MR, PR21 and PR22 are voltage detect point.

If voltage $> 1.4\text{V}$ we will stop charge back up battery.

NTC resistance is following battery thermal compensation; we need to regulate full charge voltage to protect battery.

Output Voltage Regulation

PR121	26730	27000	27270	
PR122	99000	100000	101000	
PU14	1.078	1.1	1.122	
Back up	1.363296	1.397	1.43106	V