



Numonyx™ StrataFlash® Wireless Memory (L18)

512-Mbit LX Family with LPSPDRAM (x16)

Datasheet

Product Features

- Device Architecture
 - Flash die density: 128- or 256-Mbit
 - LPSPDRAM die density: 128- or 256-Mbit
 - Async SRAM die density: 8-Mbit
 - Top, Bottom or Dual flash parameter configuration
- Device Voltage
 - Core: $V_{CC} = 1.8\text{ V}$ (Typ)
 - I/O: $V_{CCQ} = 1.8\text{ V}$ (Typ)
- Device Packaging
 - Ball count: 103 Active balls
 - Area: 9x11 mm
 - Height: 1.2 mm to 1.4 mm
- SDRAM Architecture and Performance
 - Clock rate: 104 MHz
 - Four internal banks
 - Burst length: 1, 2, 4, 8 or full page
- SRAM Performance
 - 70 ns initial access at 1.8 V I/O
- Quality and Reliability
 - Extended Temperature $-25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
 - Minimum 100K Flash Block Erase cycles
 - 0.13 μm ETOX™ VIII Process
- Flash Performance
 - 85 ns Asynchronous single-word read
 - 25 ns Asynchronous four-word page read
 - 14 ns Synchronous read (t_{CHQV})
 - 54 MHz CLK
 - Buffered Enhanced Factory Programming: 5 $\mu\text{s}/\text{byte}$ (typ.) per die
 - Buffered programming at 7 $\mu\text{s}/\text{byte}$ (typ.) per die
- Flash Architecture
 - Hardware Read-While-Write/Erase
 - Asymmetrical blocking structure
 - 8-Mbit or 16-Mbit partition size
 - 16-KWord parameter blocks (Top or Bottom); 64-KWord main blocks
 - 2-Kbit One-Time Programmable (OTP) Protection Register
 - Zero-latency block locking
 - Absolute write protection with block lock-down using F-VPP and F-WP#
- Flash Software
 - Numonyx™ FDI, Numonyx™ PSM and Numonyx™ VFM
 - Common Flash Interface (CFI)
 - Basic/Extended Command Set

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Revision History

Date	Revision	Description
July 19, 2003	-001	Initial Release.
July 24, 2003	-002	Editing changes.
September 5, 2003	-003	Ordering information changes; edits.
November 17, 2003	-004	Fixed Internet pdf presentation problem, and added tracking number.
November 20, 2003	-005	Added the following: Line items, new package information (High Performance DRAM Ballout), Flash + SRAM Bus Operations, SRAM DC and AC specifications. Made the following edits: Various text edits, the subtitle.
January 7, 2004	-006	Added line items and made minor edits.
April 16, 2004	-007	Added product 256L18+128SD with device name LZ38F4060L0YBB0 to Table 25.
July 9, 2004	-008	Modified UT-SCSP mechanical specs - (not applicable in rev -009). Updated the line items in order table.
October, 2004	-009	Various text edits and updates to the document to reflect current products available within the LX family. Remove any irrelevant information from the datasheet.
January, 2005	-010	Updated Mechanical Specifications for x16D (103 balls) Package 9x11x1.2 mm.
May, 2005	-011	Added line items to ordering table
May, 2006	-012	Added product 256L18+256L18+256SD and device name PF38F4470LLYBB0.
June 2007	013	Updated the RAM "Row to column delay" & "Row precharge time" from 28.5ns to 30.0ns. Updated hold times from 1.0 ns to 1.5 ns. Updated VCCQ, S-VCC, and D-VCC voltage MAX from +2.45 V to +2.3 V. Updated the ordering information table with the ordering matrix we now use and it will have the Samsung line item in it. Updated format and changed document number (from FD1006 to FD317623) to be consistent with current document tracking implementation.
July 2007	014	Updated ordering information
November 2007	15	Applied Numonyx branding.

1.0 Introduction

This document contains information pertaining to the products in the Numonyx™ StrataFlash® Wireless Memory (L18 SCSP), 512-Mbit LX family with LPSPDRAM (x16). The LX family offers a variety of stacked combinations that includes, flash only, flash + SDRAM, and flash + SDRAM + SRAM. The intent of this document is to provide information where this product differs from the Numonyx™ StrataFlash® Wireless Memory (L18) discrete datasheet.

Refer to the latest revision of the Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet (order number 251902) for specific flash product details not included in this document.

The Numonyx™ StrataFlash® Wireless Memory (L18 SCSP), 512-Mbit LX with LPSPDRAM family offers a variety of flash plus xRAM combinations. This L18 flash die uses the latest generation of Numonyx™ StrataFlash® Wireless Memory featuring flexible, multiple partitions, hardware read-while-erase / read-while-write operations, with high performance asynchronous and synchronous burst reads. The LPSPDRAM is a low-power, high-performance volatile memory operating up to 104 MHz with configurable burst lengths. The LX family integrates up to four flash dies and two xRAM dies in a common x16D (103 balls) package footprint and signal ballout. With a common package footprint signal ballout, higher memory density and flash/xRAM combination migrations can be easily supported without any PCB changes.

1.1 Nomenclature

0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
CFI	Common Flash Interface
CUI	Command User Interface
DU	Do Not Use
ETOX	EPROM Tunnel Oxide
Numonyx™ FDI	Numonyx™ Flash Data Integrator (software solution)
K (noun)	1 thousand
Kb	1024 bits
KB	1024 bytes
Kword	1024 words
M (noun)	1 million
Mb	1,048,576 bits
MB	1,048,576 bytes
OTP	One-Time Programmable
LR	(Protection) Lock Register
PR	Protection Register

PRD	Protection Register Data
Numonyx™ PSM	Numonyx™ Persistent Storage Manager (software solution)
RCR	Read Configuration Register
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package
SR	Status Register
SRD	Status Register Data
Word	16 bits
WSM	Write State Machine

1.2 Conventions

Group Membership Brackets: Square brackets are used to designate group membership or to define a group of signals with a similar function, such as A[21:1] and SR[4,1].

VCC vs. V_{CC} : When referring to a signal or package-connection name, the notation used is VCC. When referring to a timing or electrical level, the notation used is subscripted such as V_{CC} .

Device: This term is used interchangeably throughout this document to denote either a particular die, or both die in the SCSP.

F[4:1]-CE#: This is a group reference to multiple chip-enable pins in a flash device. Note that this group reference is different from an individual reference to a single chip-enable pin. For example, a reference to a single chip enable pin in a flash device is F1-CE# for die #1, F2-CE# for die #2, and so on until F4-CE# for die #4. Any F-CE# not used in the LX device should be treated as a Reserved for Future Use (RFU) signal ball.

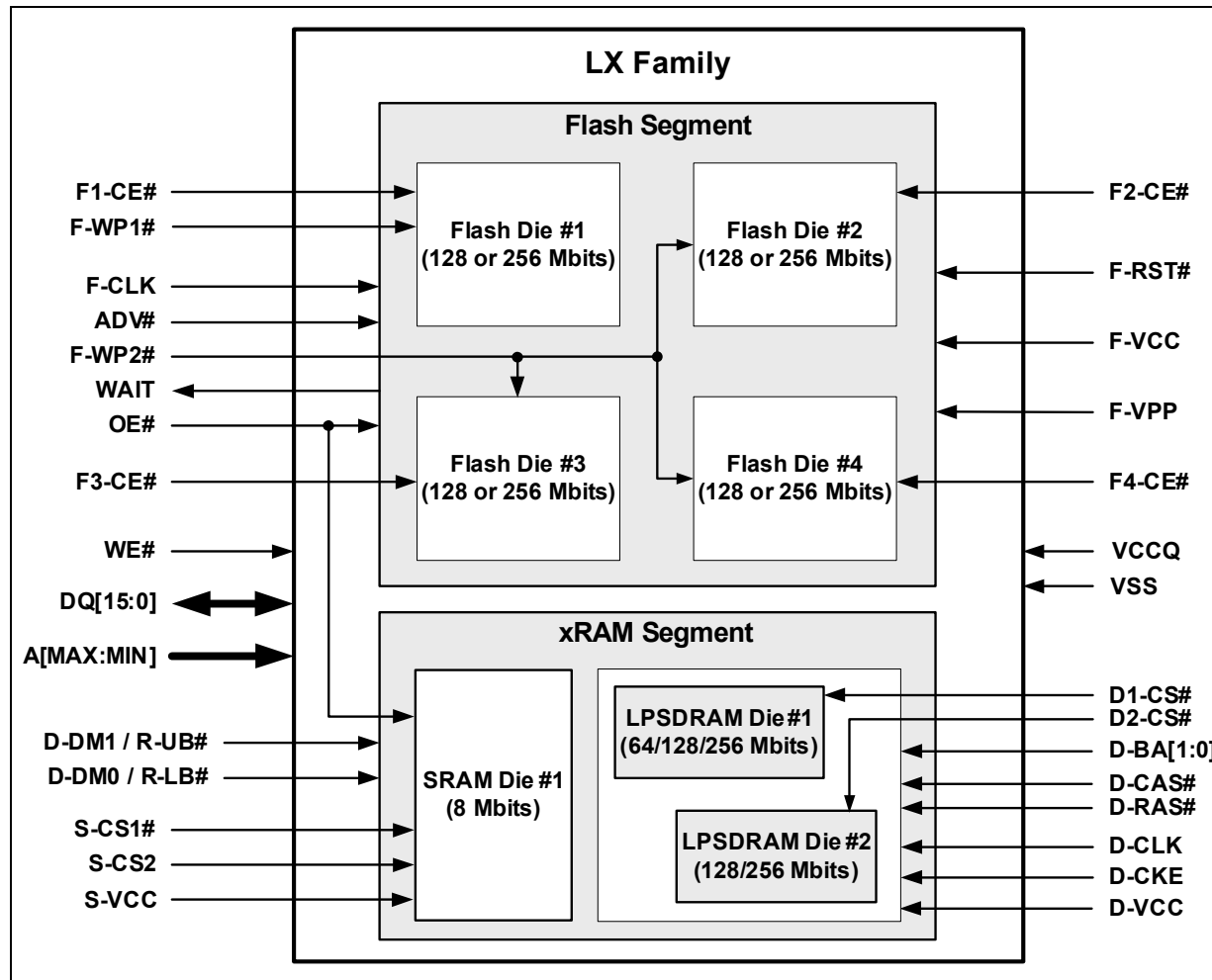
F-VCC, D-CAS#, S-VCC: When referencing flash memory signals or timings, the notation is prefixed with "F-" (e.g. F-VCC, F- V_{CC}). When the reference is to SDRAM signals or timings, the notation is prefixed with "D-" (e.g., D-CAS#, D-RAS#). When the reference is to SRAM signals or timings, the notation is prefixed with "S-" (e.g., S-VCC, S-CS1#).

2.0 Functional Overview

The LX family encompasses multiple flash and xRAM die combinations in top/bottom or dual parameter configurations.

Figure 1 shows the device capability and internal package connections for the LX product family.

Figure 1: LX Family Block Diagram

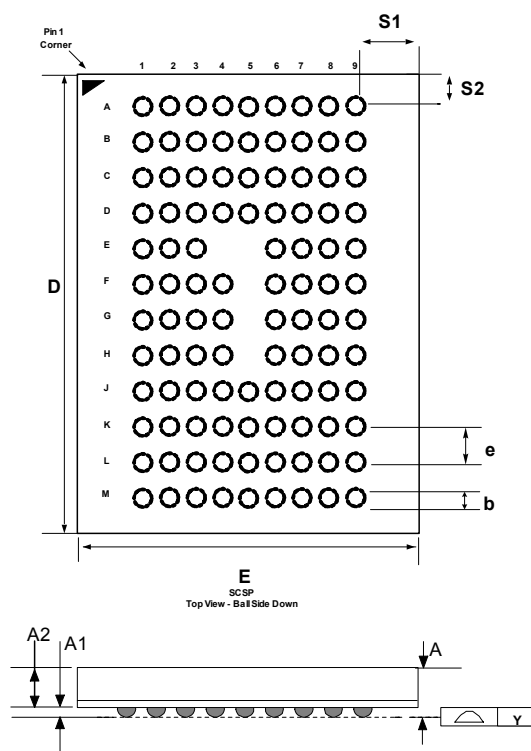


3.0 Package Information

The following package dimensions are available for the 512-Mbit LX Family x16:

- Figure 2, "Mechanical Specifications for x16D (103 balls) Package (9x11x1.4 mm)" on page 9
- Figure 3, "Mechanical Specifications for x16D (103 balls) Package (9x11x1.2 mm)" on page 10

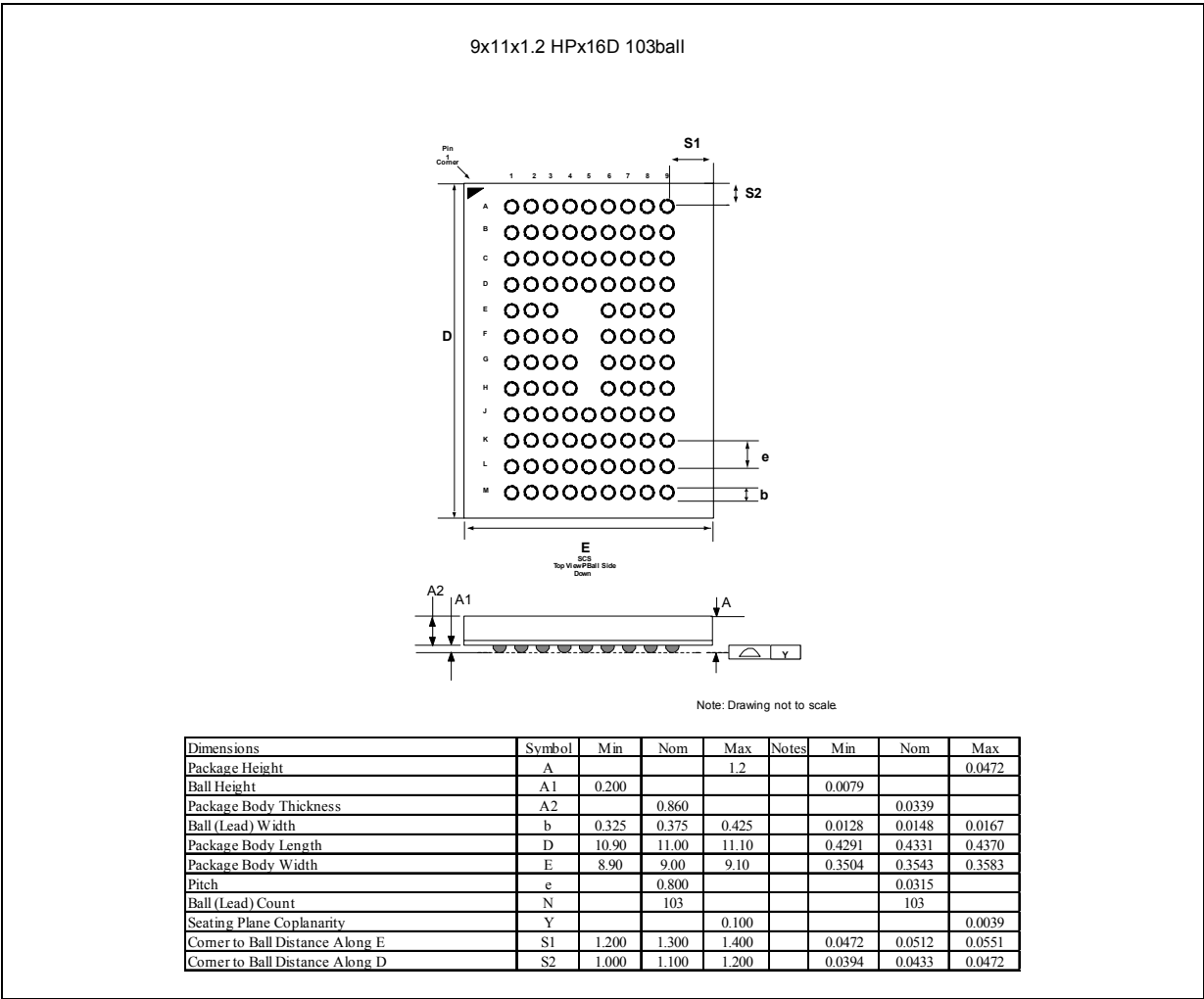
Figure 2: Mechanical Specifications for x16D (103 balls) Package (9x11x1.4 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	8.90	9.00	9.10		0.3504	0.3543	0.3583
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		103				103	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.200	1.300	1.400		0.0472	0.0512	0.0551
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 3: Mechanical Specifications for x16D (103 balls) Package (9x11x1.2 mm)

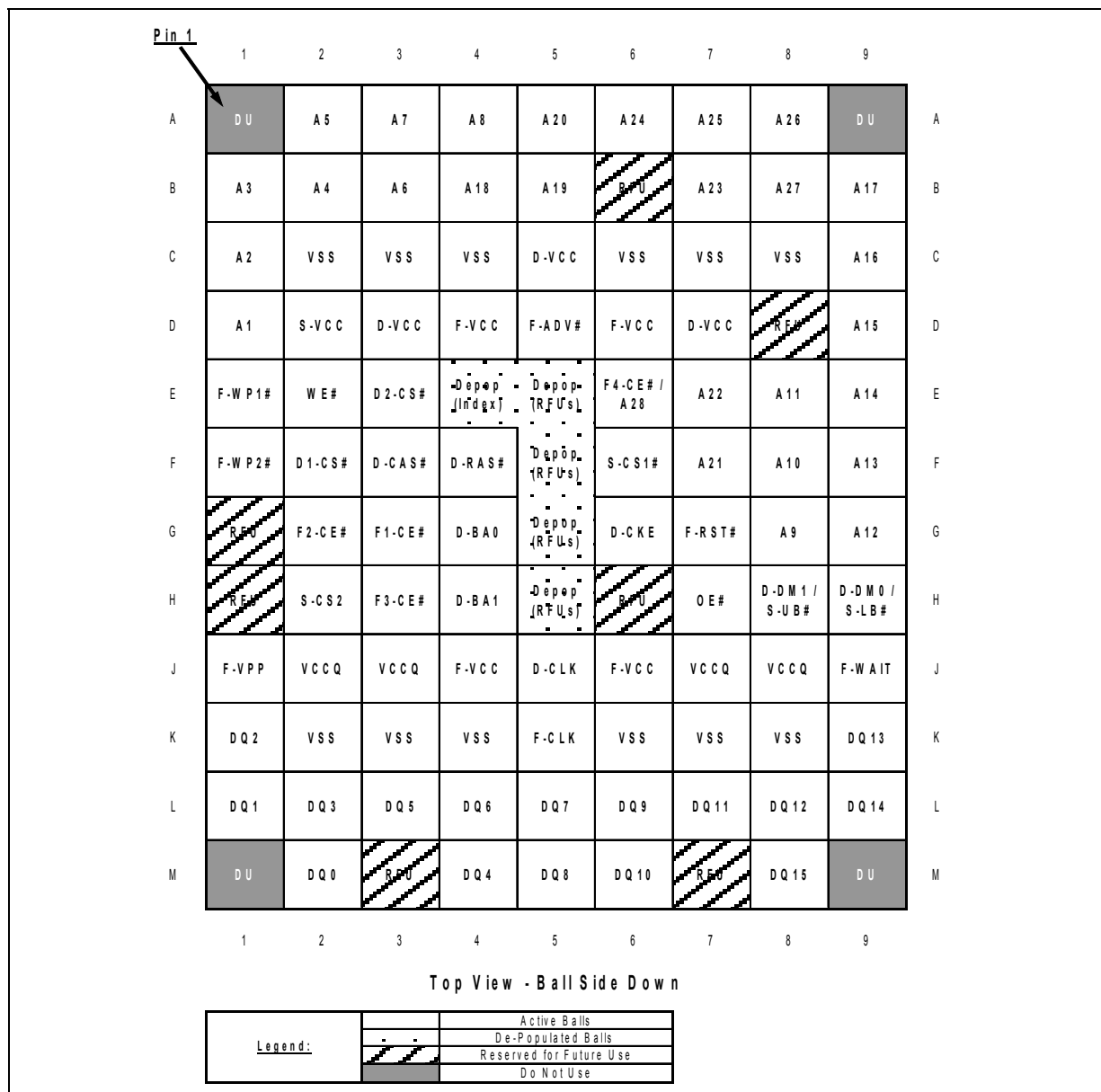


4.0 Ballout and Signal Descriptions

4.1 Device Electrical Ballout

The LX family is available in the x16D (103 balls) package ballout (Figure 4). See Section 3.0, "Package Information" on page 9 for the mechanical package dimensions for each ballout. See Table 1, "Signal Descriptions" for electrical connections details on the SCSP combination intended in this datasheet.

Figure 4: x16D (103 balls) Performance Electrical Ballout for LX Device Family



4.2 Signal Descriptions

Table 1: Signal Descriptions (Sheet 1 of 3)

Symbol	Type	Name and Function	Notes
A[MAX:1]	Input	ADDRESS: Global device signals. Share inputs for all memory die addresses during read and write operations. LPSDRAM Address inputs also provide the op-code during a Mode Register Set or Special Mode Register Set command. 256-Mbit die: AMAX = A24 128-Mbit die: AMAX = A23 64-Mbit die: AMAX = A22 32-Mbit die: AMAX = A21 8-Mbit die: AMAX = A19 - A[13:1] are the row and A[9:1] are the column addresses for 256-Mbit LPSDRAM - A[12:1] are the row and A[9:1] are the column addresses for 128-Mbit LPSDRAM - A11 defines the Auto Precharge. During a LPSDRAM Precharge command, A11 is sampled to determine if all banks are to be precharged (A11 = High). <i>Note:</i> A1 is the lowest-order x16 address.	
DQ[15:0]	Input/ Output	DATA INPUT/OUTPUTS: Global device signals. Inputs data and commands during write cycles, outputs data during read cycles. Data signals float when the device or its output are deselected. Data are internally latched during writes on the device.	
ADV#	Input	ADDRESS VALID: Low-true input. During synchronous flash read operations, addresses are latched on the rising edge of ADV#, or on the next valid F-CLK edge, whichever occurs first. In asynchronous flash read operation, addresses are latched on the rising edge ADV#, or are continuously flow-through when ADV# is kept asserted.	
F[4:1]-CE#	Input	FLASH CHIP ENABLE: Low-true input. F[4:1]-CE# low selects the associated flash memory die. F[4:1]-CE# high deselects the associated flash die. When deasserted, the associated flash die is deselected, power is reduced to standby levels, data and WAIT outputs are placed in high-Z state. - F1-CE# is dedicated as flash die #1. - F[4:2]-CE# controls any subsequent individual flash die.	1
F-CLK, D-CLK	Input	DEVICE CLOCK: Synchronizes the selected memory die to the system's bus clock in synchronous operations. - F-CLK is a flash signal. Synchronizes the flash die to the system's flash bus frequency in synchronous operations. - D-CLK is a LPSDRAM input signal. Synchronizes the LPSDRAM die to the system's memory bus clock. LPSDRAM is sampled on the positive edge of D-CLK.	
OE#	Input	OUTPUT ENABLE: Global device signal. Low-true input. OE# low enables the output drivers of the selected die. OE# high places the output drivers of the selected die in high-Z.	
F-RST#	Input	FLASH RESET: Flash specific signal. Low-true input. F-RST# low resets internal operations and inhibits write operations. F-RST# high enables normal operation. Exit from reset places the flash device in asynchronous read array mode.	
WAIT	Output	DEVICE WAIT: Flash device signal. Indicates data is valid in synchronous array or non-array sync flash reads. Configuration Register bit 10 (CR.10, WT) determines its polarity when asserted. With F-CE# and OE# at V_{IL}, WAIT's active output is V_{OL} or V_{OH}. WAIT is high-Z if F-CE# or OE# is V_{IH}. - In synchronous array or non-array flash read modes, WAIT indicates invalid data when asserted and valid data when deasserted. - In asynchronous flash page read, and all flash write modes, WAIT is deasserted.	
WE#	Input	WRITE ENABLE: Global device signal. Low-true input. WE# low selects the associated memory die for write operation. WE# high deselect the associated memory die, data are placed in high-Z state. With LPSDRAM operation, WE# is latched on the positive clock edge in conjunction with the D-RAS# and D-CAS# signals. The WE# input is used to select the Bank Activate or Precharge command and Read or Write command.	

Table 1: Signal Descriptions (Sheet 2 of 3)

Symbol	Type	Name and Function	Notes
F-WP[2:1]#	Input	FLASH WRITE PROTECT: Flash specific signals. Low-true input. F-WP# low enables the Lock-Down mechanism. Blocks in a lock-down state cannot be unlocked with the Unlock command. F-WP# high overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. F-WP1# controls flash die #1; F-WP2# are common to all other remaining flash dies.	
D-CKE	Input	LPSDRAM CLOCK ENABLE: High-true input - If D-CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle. - The state of the outputs and the burst address is halted. - When all banks are in the idle state, D-CKE is high, the LPDRAM enters into Power Down and Self-Refresh modes. - D-CKE is synchronous except after the device enters Power Down and Self-Refresh modes, where D-CKE becomes asynchronous until exiting the same mode. The input buffers, including D-CLK, are disabled during Power Down and Self-Refresh modes, providing low standby power.	
D-BA[1:0]	Input	LPSDRAM BANK SELECT: D-BA0 and D-BA1 defines to which bank the Bank Activate, Read, Write, or Bank Precharge command is being applied. The bank address D-BA0 and D-BA1 is used latched in Mode Register set.	
D-RAS#	Input	LPSDRAM ROW ADDRESS STROBE: Low-true input. - The D-RAS# signal defines the operation commands, with the D-CAS# and WE# signals. - The D-RAS# is latched at the rising edges of D-CLK. When D-RAS# and D-CS# are asserted and D-CAS# is deasserted, either the Bank Activate command or the Precharge command is selected by the WE# signal. - WE# is deasserted, the Bank Activate command is selected and the bank designated by D-BA[1:0] is turned on to the active state.	
D-CAS#	Input	LPSDRAM COLUMN ADDRESS STROBE: Low-true input. - D-CAS# signal defines the operation commands in conjunction with the D-RAS# and WE# signals and is latched at the rising edges of D-CLK. - D-RAS# is deasserted and D-CS# is asserted, the column access is started by asserting D-CAS#. Read or Write command then is selected by asserting WE# low or high.	
D[2:1]-CS#	Input	LPSDRAM CHIP SELECT: Low-true input. D[2:1]-CS# low selects the associated LPSPDRAM memory die. All commands are masked when D[2:1]-CS# high. D[2:1]-CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code. - D1-CS# controls LPSPDRAM die #1. - D2-CS# controls LPSPDRAM die #2.	
D-DM[1:0]	Input	LPSDRAM INPUT Mask: Data Input Mask. - D-DM[1:0] are byte selects. Input data is masked when D-DM[1:0] are sampled HIGH during a write cycle. D-DM1 masks DQ[15:8], and D-DM0 masks DQ[7:0]. - The D-DM[1:0] latency for Read is 2 Clocks and for Write is 0 Clocks.	2
S-CS1# S-CS2	Input	SRAM CHIP SELECTS: SRAM specific signal. Low-true input. When both SRAM chip selects are asserted, SRAM internal control logic, input buffers, decoders, and sense amplifiers are active. When either or both SRAM chip selects are deasserted (S-CS1# = V _{IH} and/or S-CS2 = V _{IH}), the SRAM is deselected and its power is reduced to standby levels. S-CS1# and S-CS2 are available on stacked combinations with SRAM die, and are RFU on stacked combinations without SRAM die.	3
R-UB# R-LB#	Input	SRAM UPPER/ LOWER BYTE ENABLES: Low - true inputs. During SRAM read and write cycles, R-UB# low enables the SRAM high-order byte on DQ[15:8], and R-LB# low enables the SRAM low-order byte on DQ[7:0]. R-UB# and R-LB# are available on stacked combinations with SRAM die, and are RFUs on stacked combinations without SRAM die.	2, 3
F-VPP	Power	FLASH ERASE/ PROGRAM VOLTAGE LEVEL: Flash specific signal. Valid F-VPP voltage on this ball allows block erase or program functions. Flash memory array contents cannot be altered when F-V _{PP} ≤ V _{PPLK} . Block erase and program at invalid F-VPP voltage should not be attempted.	

Table 1: Signal Descriptions (Sheet 3 of 3)

Symbol	Type	Name and Function	Notes
F-VCC	Power	FLASH CORE VOLTAGE LEVEL: Flash specific signals. Flash core source voltage. Flash operations are inhibited when $F-V_{CC} \leq V_{LKO}$. Operations at invalid F-VCC voltage should not be attempted.	
VCCQ	Power	OUTPUT VOLTAGE LEVEL: Global device signals. Device output-driver source voltage. This balls can be tied directly to the respective memory type VCC if operating within its V_{CC} range.	
D-VCC	Power	RAM POWER SUPPLY: Supplies power to the RAM dies. Performance ballout: D-VCC supplies power for LPSDRAM operation.	
S-VCC	Power	SRAM POWER SUPPLY: Supplies power to the SRAM die. S-VCC is available on stacked combinations with SRAM die, and is RFU on stacked combinations without SRAM die.	3
VSS	Power	GROUND: Global ground reference for device memory core type voltages. Connect all VSS to system ground. Do not float any VSS connections.	
DU	-	DO NOT USE: This ball must be left floating. This ball should not be connected to any power supplies, signals, or other balls.	
RFU	-	RESERVED for FUTURE USE: Reserved by Numonyx for future device functionality and enhancement.	

Notes:

1. F4-CE# is a shared signal with A28 for the 103-Active Ball High-Performance DRAM package.
2. D-DM[1:0] are shared signals with R-UB# and R-LB# respectively.
3. Only available in the 103-Active Ball High-Performance DRAM package.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Numonyx sales office that you have the latest datasheet before finalizing a design.

Table 2: Flash Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Case Temperature under Bias (T_C)	-25	+85	°C	
Storage Temperature	-55	+125	°C	
Voltage On Any Signal (except F- V_{CC} , F- V_{PP} , D- V_{CC} , S- V_{CC} and V_{CCQ})	-0.2	+2.0	V	1
F- V_{CC} Voltage	-0.2	+2.50	V	1
V_{CCQ} , S- V_{CC} and D- V_{CC} Voltage	-0.2	+2.3	V	1
F- V_{PP} Voltage	-0.2	+10.0	V	1,2,3
I_{SH} Output Short Circuit Current	-	50	mA	4

Notes:

1. All Specified voltages are relative to V_{SS} . Minimum DC voltage is -0.2 V on input/output signals, F- V_{CC} , D- V_{CC} , V_{CCQ} and F- V_{PP} signals. During transitions, this level may overshoot to -1.0 V for periods < 5 ns. Maximum DC voltage on F- V_{CC} is F- V_{CC} + 0.5 V, which during transitions may overshoot to F- V_{CC} + 2.0 V for periods < 20 ns. Maximum DC voltage on input/output signals and V_{CCQ} is V_{CCQ} + 0.5 V, which during transitions may overshoot to V_{CCQ} + 2.0V for periods < 20 ns.
2. Maximum DC voltage on F- V_{PP} may overshoot to +10.0 V for periods < 20 ns.
3. Program/erase voltage is typically 1.7 V - 2.0 V. 9.0 V can be applied for 80 hours maximum total, to any blocks for 1000 cycles maximum. 9.0 V program/erase voltage may reduce block cycling capability.
4. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 3: Device Operating Conditions

Symbol	Parameter	Flash + xRAM		Unit
		Min	Max	
T_C	Operating Temperature	-25	+85	°C
F- V_{CC}	Flash Supply Voltage	1.7	2.0	V
V_{CCQ} D- V_{CC} , S- V_{CC}	Flash and LPSPDRAM I/O Voltage LPSPDRAM Supply Voltage	1.7	1.9	V
V_{PPL}	F- V_{PP} Voltage Supply (Logic Level)	0.9	2	V
V_{PPH}	Factory word programming F- V_{PP}	8.5	9.5	V
Note: In typical operation, the F- V_{PP} program voltage is V_{PPL} . F- V_{PP} can be connected to 8.50 V - 9.50 V for 1000 cycles on main blocks and 2500 cycles on parameter blocks.				

6.0 Electrical Specifications

6.1 Flash DC Characteristics

Refer to the Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet (order number 251902) for flash DC characteristics.

6.2 SRAM and LPSDRAM DC Characteristics

NOTICE: DC Characteristics of all die in a SCSP device need to be considered accordingly, depending on the SCSP device operation.

Table 4: LPSDRAM DC Characteristics (Sheet 1 of 2)

Parameter	Description	Test Conditions		Min	Typ	Max	Unit	Notes
D-VCC	Voltage Range		Density	1.7	—	1.9	V	
I_{CC1} (One Bank Active)	Operating Current at min cycle time Burst Length = 1	I _{IO} = 0mA t _{CK} = min	128-Mbit	—	—	60	mA	
			256-Mbit	—	—	75		
I_{CC2P}	Precharge Standby Current: Power Down Mode (All banks idle)	D-CKE = L, D-CS# = H t _{CK} = min	128-Mbit	—	—	600	μA	
			256-Mbit	—	—	700		
I_{CC2N}	Precharge Standby Current: Non-Power Down Mode (All banks idle)	D-CKE = H, D-CS# = H t _{CK} = min	128-Mbit	—	—	15	mA	
			256-Mbit	—	—	15		
I_{CC3P}	Active Standby Current in Power Down Mode (All banks active)	D-CKE = L, t _{CK} = min	128-Mbit	—	—	5	mA	
			256-Mbit	—	—	5		
I_{CC3N}	Active Standby Current: Non-Power Down Mode (All banks active)	D-CKE = H, t _{CK} = min	128-Mbit	—	—	20	mA	3
			256-Mbit	—	—	25		
I_{CC4} (4 Banks active)	Operating Current Burst Mode	I _{IO} = 0mA t _{CK} = min	128-Mbit	—	—	70	mA	
			256-Mbit	—	—	80		
I_{CC5}	Auto-Refresh Current	t _{RC} > t _{RCmin}	128-Mbit	—	—	130	mA	2
			256-Mbit	—	—	150		
I_{CC6}	Self-Refresh Current	Address & Data toggling at min cycle time	128-Mbit	—	—	500	μA	4
			256-Mbit	—	—	600		
I_{CC7}	Deep Power Down Current	Address & Data toggling at min cycle time	128-Mbit	—	15	—	μA	
			256-Mbit	—	15	—		
V_{OH}	Output High Voltage	I _{OH} = -100 μA	—	V _{CCQ} - 0.15	—	—	V	
V_{OL}	Output Low Voltage	I _{OL} = 100 μA, V _{CCQmin}	—	-0.1	—	0.2	V	
V_{IH}	Input High Voltage	—	—	V _{CCQ} - 0.4	—	V _{CCQ} + 0.2	V	

Table 4: LPSPDRAM DC Characteristics (Sheet 2 of 2)

V_{IL}	Input Low Voltage	—	—	-0.2	—	0.3	V	
I_{IL}	Input Leakage Current	$-0.2V < V_{IN} < V_{CCQ} + 0.2V$	—	-2	—	+2	μA	1

Notes:

1. Input leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.
2. Input signals are toggled at max frequency to simulate SCSP condition, where another device may be active.
3. No accesses in progress.
4. See Table 5, "LPSPDRAM Self-Refresh Current".

Table 5: LPSPDRAM Self-Refresh Current

Parameter	Description	Test Condition	Set Temperature	# of Banks			Unit
				All Banks Refreshed	Bank 0 & 1 Refreshed	Bank 0 Refreshed	
ICC6 (128-Mbit)	Self-Refresh Current (All Banks Refreshed)	D-CKE < 0.2 V t _{CK} = Infinity	85 °C max	500	400	300	μA
			70 °C max	440	350	280	
			45 °C max	390	290	260	
			15 °C max	350	240	240	
ICC6 (256-Mbit)	Self-Refresh Current (All Banks Refreshed)	D-CKE < 0.2 V t _{CK} = Infinity	85 °C max	600	450	315	μA
			70 °C max	525	375	295	
			45 °C max	450	300	270	
			15 °C max	375	250	250	

Note: Other than ICC6 for all Banks at 85°C, the Self-Refresh currents are verified during device characterization and not 100% tested.

Table 6: SRAM DC Characteristics (Sheet 1 of 2)

Parameter	Description	Test Conditions	1.8 V SRAM		Unit
			MIN	MAX	
S-V_{CC}	Voltage Range	—	1.7	1.9	V
V_{DR}	S-V _{CC} for Data Retention	—	1.0	—	V
I_{CC}	Operating Current at minimum cycle time	I _{IO} = 0 mA	—	35	mA
I_{CC2}	Operating Current at maximum cycle time (1 μs)	I _{IO} = 0 mA	—	6	mA
I_{SB}	Standby Current	S-CS1# ≥ S-V _{CC} -0.2 V or S-CS2 ≤ V _{SS} +0.2 V Address/Data toggling at minimum cycle time	—	20	μA
I_{DR}	Current in Data Retention mode	S-V _{CC} = 1.0 V	—	10	μA
V_{OH}	Output High Voltage	I _{OH} = -100 μA	S-V _{CC} - 0.15	—	V
V_{OL}	Output Low Voltage	I _{OL} = 100 μA, V _{CCMIN}	-0.1	0.2	V

Table 6: SRAM DC Characteristics (Sheet 2 of 2)

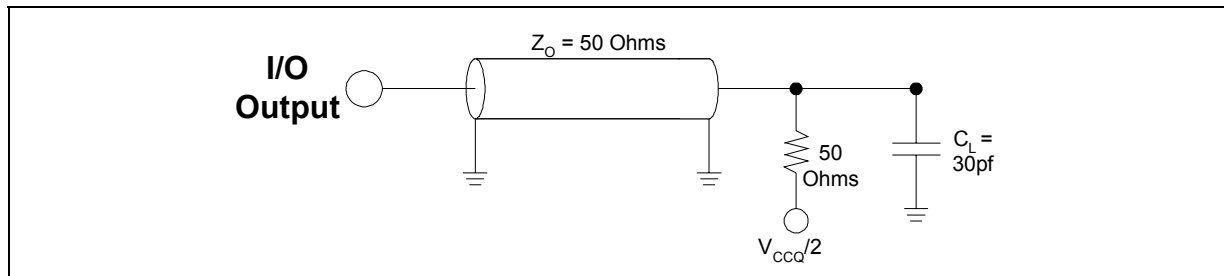
V_{IH}	Input High Voltage	—	$S-V_{CC} - 0.4$	$S-V_{CC} + 0.2$	V
V_{IL}	Input Low Voltage	—	-0.2	0.4	V
*I_{IL}	Input Leakage Current	$-0.2 < V_{IN} < S-V_{CC} + 0.2 \text{ V}$	-1	+1	μA
*I_{LDR}	Input Leakage Current in Data Retention Mode	$-0.2 < V_{IN} < S-V_{CC} + 0.2 \text{ V}$ $S-V_{CC} = V_{DR}$	-1	+1	μA

Note: * Input leakage currents include High-Z output leakage for bi-directional buffers with tri-state outputs.

7.0 AC Characteristics

7.1 AC Test Conditions

Figure 5: Transient Equivalent Testing Load Circuit



Notes:

1. Test configuration component value for worst case speed conditions.
2. C_L includes jig capacitance

7.2 Flash AC Characteristics

7.2.1 Capacitance

Refer to the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for detailed information.

7.2.2 AC Read Specifications

Refer to the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for detailed information.

7.2.3 Flash AC Write Specifications

Refer to the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for detailed information.

7.2.4 Flash Program and Erase Characteristics

Refer to the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for detailed information.

7.3 SRAM and LPSDRAM AC Characteristics

7.3.1 SRAM and LPSDRAM Capacitance

Table 7: SRAM and LPSDRAM Capacitance

Symbol	Parameter	MAX (SRAM)	MAX (LPSDRAM)	Unit	Condition
C _{IN}	Input Capacitance	6	5	pF	V _{IN} = 0 V
C _{OUT}	Output Capacitance	7	7	pF	V _{OUT} = 0 V

Note: Sampled, not 100% tested. T_C = 25 °C, f = 1 MHz.

7.3.2 LPSDRAM AC Characteristics

Table 8: LPSDRAM AC Characteristics—Read-Only Operations

Symbol	Parameter	Test Condition	Min	Max	Unit	Notes
t _{RC}	Clock Cycle Time	CL = 3 D-CLK = 104 MHz	9.5	—	ns	1,2
t _{CKH}	Clock High Level Pulse Width		3	—	ns	1,2
t _{CKL}	Clock Low Level Pulse Width		3	—	ns	1,2
t _T	Transition Time		0.5	1.0	ns	1,2
t _{CKEH}	D-CKE Hold Time		1.5	—	ns	1,2
t _{CKES}	D-CKE Setup Time		2	—	ns	1,2
t _{AH}	Address Hold Time		1.5	—	ns	1,2
t _{AS}	Address Setup Time		2	—	ns	1,2
t _{IH}	Data Input Hold Time		1.5	—	ns	1,2
t _{IS}	Data Input Setup Time		2	—	ns	1,2
t _{CMH}	D-CS#, D-RAS#, D-CAS#, WE#, D-DM Hold Time		1.5	—	ns	1,2
t _{CMS}	D-CS#, D-RAS#, D-CAS#, WE#, D-DM Setup Time		2	—	ns	1,2
t _{AC}	Clock to valid output delay (positive edge of clock)	CL = 3	—	7	ns	1,2
t _{OH}	Data Out Hold Time		2.0	—	ns	1,2
t _{LZ}	Clock to Output in Low-Z		1	—	ns	1,2
t _{HZ}	Clock to Output in High-Z	CL = 3	—	7	ns	1,2
t _{RAS}	Row Active time (Active to Precharge command)		60	100K	ns	1,2
t _{RC}	Row Cycle time (Active to Active command on same bank)		90	—	ns	1,2
t _{RCD}	Row to column delay (Active to Read/Write)		30	—	ns	1,2
t _{RP}	Row Precharge Time		30	—	ns	1,2
t _{REF}	Refresh Period (4096 rows)		—	64	ms	1,2
t _{RFC}	Auto-Refresh Period		110	—	ns	1,2
t _{SREX}	Self-Refresh Exit Time (Self refresh to active)		120	—	ns	1,2

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required by clock cycle time.
2. LPSDRAM AC specs are guaranteed only when normal output driver strength is used. See [Table 23, “LPSDRAM Configurable Output Driver Strength” on page 34.](#)

Table 9: LPSDRAM AC Characteristics—Write Operations

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{WR}	Write Recovery Time		20	—	ns
t_{RRD}	Active bank a to Active Bank b command		20	—	ns
t_{DAL}	Last data input to Active Delay		—	$t_{WR} + t_{RP}$	ms
t_{CDL}	Last data input to New Read/Write Command		—	1	t_{CK}
t_{BDL}	Last data input to Burst Terminate Command		—	1	t_{CK}
t_{CCD}	Read/Write command to Read/Write command		—	1	t_{CK}
t_{DQW}	D-DM write mask latency		—	0	t_{CK}
t_{DQZ}	D-DM data out mask latency		—	2	t_{CK}
t_{MRD}	Load Mode Register Command to Active/Refresh Command		—	2	t_{CK}
t_{WR}	Write Recovery Time	$t_{WR} / t_{CK} < 1$	—	1	t_{CK}
		$1 < t_{WR} / t_{CK} < 2$	—	2	
t_{PHZ}	Data out to High Z from Precharge command	CL = 3	—	3	t_{CK}
		CL = 2	—	2	
		CL = 1	—	—	
t_{INI}	Initialization Delay		200	—	μs

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required by clock cycle time.
2. LPSDRAM AC specs are guaranteed only when Normal Output Driver Strength is used. See [Table 23](#).

7.3.3 SRAM AC Read Specifications

Table 10: SRAM Asynchronous Read Specifications (Sheet 1 of 2)

#	Symbol	Parameter	MIN	MAX	Unit	Notes
R1	t_{RC}	Read Cycle Time	70	—	ns	
R2	t_{AA}	Address to Output Delay	—	70	ns	
R3	t_{CO1}	S-CS ₁ # to Output Delay	—	70	ns	
R3	t_{CO2}	S-CS ₂ to Output Delay	—	70	ns	
R4	t_{OE}	OE# to Output Delay	—	35	ns	
R5	t_{BA}	R-UB#, R-LB# to Output Delay	—	70	ns	
R6	t_{LZ}	S-CS ₁ # or S-CS ₂ to Output in Low-Z	5	—	ns	1,2
R7	t_{OLZ}	OE# to Output in Low-Z	0	—	ns	1
R8	t_{HZ}	S-CS ₁ # or S-CS ₂ to Output in High-Z	0	25	ns	1,2,3
R9	t_{OHZ}	OE# to Output in High-Z	0	25	ns	1,3
R10	t_{OH}	Output Hold (from Address, S-CS ₁ #, S-CS ₂ , or OE# change, whichever occurs first)	0	—	ns	

Table 10: SRAM Asynchronous Read Specifications (Sheet 2 of 2)

R11	t_{BLZ}	R-UB#, R-LB# to Output in Low-Z	0	—	ns	1
R12	t_{BHZ}	R-UB#, R-LB# to Output in High-Z	0	25	ns	1

Notes:

1. Sampled, not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (MAX) is less than t_{LZ} (MAX) for a given device and from device-to-device interconnection.
3. Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

7.3.4 SRAM AC Write Specifications**Table 11: SRAM Asynchronous Write Specifications**

#	Symbol	Parameter ¹	70 ns		85 ns		Notes
			MIN	MAX	MIN	MAX	
W1	t_{WC}	Write Cycle Time	70	—	85	—	
W2	t_{AS}	Address Setup to WE# and R-UB#, R-LB# going low	0	—	0	—	4,6
W3	t_{WP}	WE# Pulse Width	55	—	60	—	2,3,6
W4	t_{DW}	Data to Write Time Overlap	30	—	35	—	
W5	t_{AW}	Address Setup to WE# going high	60	—	70	—	6
W6	t_{CW}	S-CS1# Setup to WE# going high	60	—	70	—	6
W7	t_{DH}	Data Hold from WE# High	0	—	0	—	6
W8	t_{WR}	Write Recovery	0	—	0	—	5,6
W9	t_{BW}	R-UB#, R-LB# setup to WE# going high	60	—	70	—	6

Notes:

1. See also [Figure 6, "AC Waveform SRAM Write Operation" on page 23](#).
2. A write occurs during the overlap (t_{WP}) of low CS1# and low WE#. A write begins when S-CS1# goes low and WE# goes low with asserting R-UB# or R-LB# for single byte operation or simultaneously asserting R-UB# and R-LB# for double byte operation. A write ends at the earliest transition when S-CS1# goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.
3. t_{WP} is measured from S-CS1# going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as S-CS1# or WE# going high.
6. The same-e timing parameters apply if the Write operation is performed by toggling S-CS2 instead of S-CS1#. S-CS2 is asserted high while S-CS1# is asserted low

Figure 6: AC Waveform SRAM Write Operation

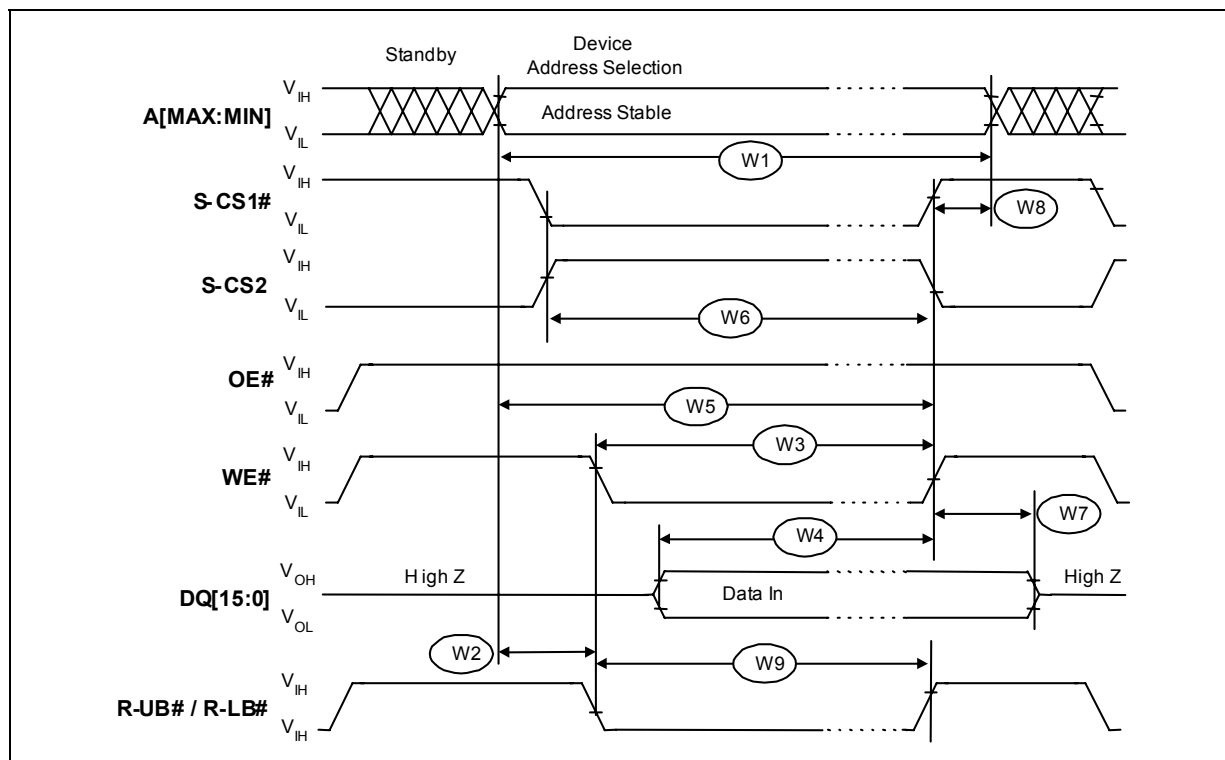
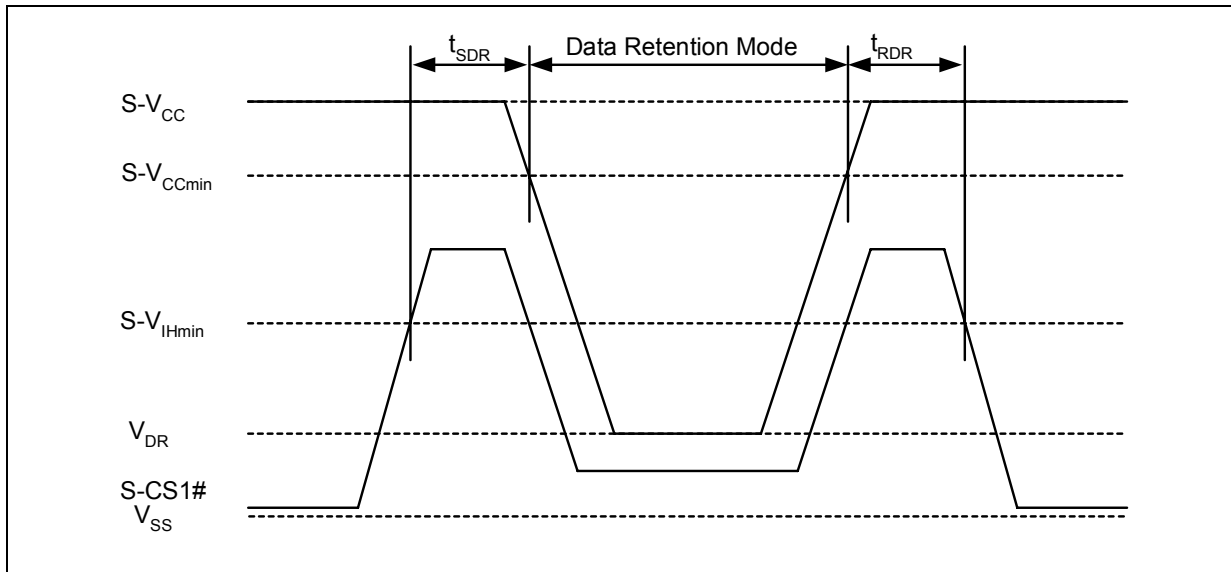


Table 12: SRAM Data Retention Timing

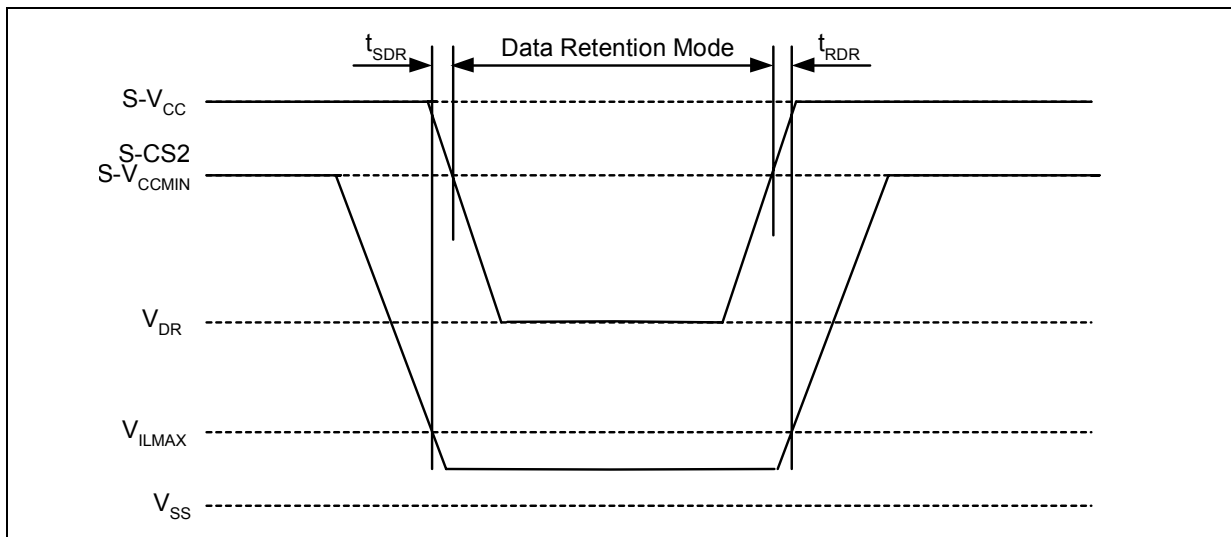
Parameter	Description	MIN	MAX	Unit
t_{SDR}	Data Retention Set-up Time	0	–	ns
t_{RDR}	Data Retention Recovery Time	70 or 85	–	ns

Figure 7: SRAM Data Retention Waveform (S-CS1# Controlled)



Note: $S-CS1\# \geq S-V_{CC} - 0.2 \text{ V}$, $S-CS2 \geq S-V_{CC} - 0.2 \text{ V}$

Figure 8: SRAM Data Retention Waveform (S-CS2 Controlled)



Note: $S-CS2 \leq 0.2 \text{ V}$

8.0 Power and Reset Specifications

8.1 Flash Power and Reset Specifications

Refer to the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for detailed information.

8.2 LPSDRAM Power-up Sequence and Initialization

The LPSDRAM must be powered up and initialized in a predefined manner. Once power is applied to D-VCC and VCCQ simultaneously, and the clock is stable, the LPSDRAM requires a t_{INI} delay prior to issuing any command other than the NOP command. The NOP command should be applied at least once during the t_{INI} delay. After the t_{INI} delay, a Precharge command should be applied to precharge all banks. This must be followed by two back to back Auto-Refresh cycles. After the Auto-Refresh cycles are complete, the Mode Registers must be programmed. The Mode Register will power-up in an unknown state. The Mode Register and the Extended Mode Register should be loaded prior to issuing any operational commands.

9.0 Bus Operations Overview

9.1 Flash, LPSDRAM and SRAM Bus Operations

Bus operations for this L18 SCSP LX family (x16) device involve the control of flash, SRAM, and LPSDRAM inputs. The bus operations are shown in:

- Table 13, "Flash + LPSDRAM Bus Operations"
- Table 14, "LPSDRAM Functional Mode Description: Current State bank n, Command to Bank n"
- Table 15, "LPSDRAM Functional Mode Description: Current State bank n, Command to Bank m"
- Table 16, "Flash + SRAM Bus Operations"

Fully synchronous operations are performed by the LPSDRAM to latch the commands at the positive edges of D-CLK.

See the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for complete descriptions of flash modes and commands, command bus-cycle definitions and flowcharts that illustrate operational routines.

Table 13: Flash + LPSDRAM Bus Operations (Sheet 1 of 3)

Device	Mode	F-RST#	F-CE#	OE#	ADV#	F-VPP	WAIT	WE#	D-CKEn-1	D-CKEn	D-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
Flash Die (#1, #2, #3 or #4)	Sync Array Read	H	L	L	L	X	Active	H	LPSDRAM outputs must be in High-Z									Flash D _{OUT}	1,4,6
	Async Read	H	L	L	X	X	De-asserted	H										Flash D _{OUT}	1,4,5,6
	Write	H	L	H	L	V _{PPL} / V _{PPH}	High-Z	L										Flash D _{IN}	2,3,5,6
	Output Disable	H	L	H	X	X	High-Z	H	Any LPSDRAM mode allowed									Flash High-Z	6
	Standby	H	H	X	X	X	High-Z	X										Flash High-Z	6
	Reset	L	X	X	X	X	High-Z	X										Flash High-Z	6

Table 13: Flash + LPSDRAM Bus Operations (Sheet 2 of 3)

Device	Mode	F-RST #	F-CE #	OE #	ADV #	F-VPP	WAIT	WE #	D-CKE _{n-1}	D-CKE _n	D-CS #	D-RAS #	D-CAS #	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
LPSDRAM Die (#1 or #2)	Active	Flash outputs must be in High-Z						H	H	X	L	L	H	X	V	Row Address		RAM D _{OUT}	6,7
	Read							H	H	X	L	H	L	L/H	V	L	Col Addr	RAM D _{OUT}	6,7,8,10
	With Auto Precharge							H	H	X	L	H	L	L/H	V	H		RAM D _{OUT}	6,7,8,10
	Write							L	H	X	L	H	L	L/H	V	L	X	RAM D _{IN}	6,9,10
	With Auto Precharge							L	H	X	L	H	L	L/H	V	H		RAM D _{IN}	6,9,10
	Burst Stop							L	H	H	L	H	H	X	X	X	X	RAM High-Z	6
	Precharge One Bank							L	H	X	L	L	H	X	V	L	X	RAM High-Z	6
	All Banks							L	H	X	L	L	H	X	X	H		RAM High-Z	6
	Auto-Refresh	Flash must be in High-Z						H	H	H	L	L	L	X	X	X	X	RAM High-Z	6,13
	Self-Refresh Entry							H	H	L	L	L	L	X	X	X	X	RAM High-Z	6,13
	Self-Refresh Exit							H	L	H	L	H	H	X	X	X	X	RAM High-Z	6
		Any flash mode allowed						X	L	H	H	X	X	X	X	X	X	RAM High-Z	6

Table 13: Flash + LPSDRAM Bus Operations (Sheet 3 of 3)

Device	Mode	F-RST#	F-CE#	OE#	ADV#	F-VPP	WAIT	WE#	D-CKE _{n-1}	D-CKE _n	D-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
LPSDRAM Die (#1 or #2)	Load Mode Register	Flash outputs must be in High-Z						L	H	X	L	L	L	X	Operand Code			RAM High-Z	6, 11, 12
	Input/Output Enable							X	H	X				L	X			RAM High-Z	6, 10
	Input Inhibit/Output High-Z	Any flash mode allowed						X	H	X				H	X			RAM High-Z	6, 10
	Clock Suspend Entry	Any flash mode allowed						X	H	L	H	X	X	X	X	X	X	RAM High-Z	6, 14
		Flash outputs must be in High-Z						V			L	V	V						
	Clock Suspend Exit	Flash outputs must be in High-Z						X	L	H	X	X	X	X	X	X	X	RAM High-Z	6
	Power Down Entry	Any flash mode allowed						X	H	L	H	X	X	X	X	X	X	RAM High-Z	6, 15
		Flash outputs must be in High-Z						H			L	H	H						
	Power Down Exit	Any flash mode allowed						X	L	H	H	X	X	X	X	X	X	RAM High-Z	6
		Flash outputs must be in High-Z						H			L	H	H						
	Deep Power Down Entry	Flash outputs must be in High-Z						L	H	L	L	H	H	X	X	X	X	RAM High-Z	6
	Deep Power Down Exit							X	L	H	X	X	X	X	X	X	X	RAM High-Z	6
	Device Deselect (NOP)	Any flash mode allowed						X	H	X	H	X	X	X	X	X	X	RAM High-Z	6
	No Operation (NOP)	Flash outputs must be in High-Z						H	H	X	L	H	H	X	X	X	X	RAM High-Z	6

Notes:

1. WAIT is only valid during synchronous flash reads. Refer to the discrete datasheet for detailed WAIT functionality.
2. OE# and WE# should never be asserted simultaneously.
3. X can be V_{IL} or V_{IH} for inputs, V_{PPL}, V_{PPH} or V_{PPLK} for F-V_{PP}.
4. Flash CFI query and Status Register accesses use DQ[7:0] only, all other reads use DQ[15:0].
5. Refer to the L18 datasheet for valid D_{IN} during flash writes.
6. All states and sequences not shown are illegal or reserved.
7. A[13:1] provide row address for 256-Mbit LPSDRAM. A[12:1] provide row address for 128-Mbit LPSDRAM. A[9:1] provide column address for 128-Mbit or 256-Mbit LPSDRAM.
8. Select bank and column address, and start Read. A11 High enables auto precharge.
9. Select bank and column address, and start Write. A11 High enables auto precharge.
10. Activate or deactivate the data during Writes with zero-clock delay and during Reads with two-clock delay. D-DM0 corresponds to DQ[7:0], D-DM1 corresponds to DQ[15:8].
11. A[11:1] define the operand code to the register.
12. Extended Mode Register is programmed by setting D-BA1 = H and D-BA0 = L. For Mode Register programming, set D-BA1 = D-BA0 = L.
13. All banks must be precharged before issuing an Auto-refresh command.
14. Clock suspend mode occurs when column access or burst is in progress.
15. Power-Down occurs when no accesses are in progress.

Table 14: LPSPDRAM Functional Mode Description: Current State bank n , Command to Bank n

Current State	D-CS#	D-RAS#	D-CAS#	WE#	Command	Action	Notes
Any	H	X	X	X	NOP	Continue previous operation	
	L	H	H	H	NOP	Continue previous operation	
Idle	L	L	H	H	Active	Select and activate row	
	L	L	L	H	Auto refresh	Auto refresh	
	L	L	L	L	Load Mode Register	Mode Register set	
	L	L	H	L	Precharge	NOP	
Row Active	L	H	L	H	Read	Select Column & start read burst	
	L	H	L	L	Write	Select Column & start write burst	
	L	L	H	L	Precharge	Deactivate Row in bank (or banks)	3
Read (without Auto precharge)	L	H	L	H	Read	Truncate read & start new read burst	5
	L	H	L	L	Write	Truncate read & start new write burst	5
	L	L	H	L	Precharge	Truncate read, start precharge	
	L	H	H	L	Burst Terminate	Burst terminate	
Write (without Auto precharge)	L	H	L	H	Read	Truncate write & start new read burst	5
	L	H	L	L	Write	Truncate write & start new write burst	5
	L	L	H	L	Precharge	Truncate write, start precharge	
	L	H	H	L	Burst Terminate	Burst terminate	

Notes:

1. The table applies when both D-CKE_{n-1} and D-CKE_n are high.
2. All states and sequences not shown are illegal or reserved.
3. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
4. A command other than No Operation (NOP), should not be issued to the same bank while a Read or Write Burst with auto precharge is enabled.
5. The new Read or Write command could be auto precharge enabled or auto precharge disabled.

Table 15: LPSPDRAM Functional Mode Description: Current State bank n , Command to Bank m

Current State	D-CS#	D-RAS#	D-CAS#	WE#	Command	Action	Notes
Any	H	X	X	X	NOP	Continue previous Operation	1,2
	L	H	H	H	NOP	Continue previous Operation	1,2
Idle	X	X	X	X	Any	Any command allowed to bank m	1,2
Row Activating, Active, or Precharging	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Read burst	1,2
	L	L	H	L	Precharge	Precharge	1,2

Table 15: LPSDRAM Functional Mode Description: Current State bank n , Command to Bank m

Read with Auto Precharge disabled	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Write with Auto precharge disabled	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Read with Auto Precharge	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Write with Auto precharge	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2

Notes:

1. The table applies when both D-CKE_{n-1} and D-CKE_n are high.
2. All states and sequences not shown are illegal or reserved.

Table 16: Flash + SRAM Bus Operations (Sheet 1 of 2)

Device	Mode	F-RST#	F-CE#	OE#	WE#	WAIT	ADV#	F-VPP	S-CS1#	S-CS2	R-UB#, R-LB#	DQ[15:0]	Notes
Flash (#1, #2, #3 or #4)	Synchronous Array and Non-Array Read	H	L	L	H	Active	L	X	H	X	X	Flash D _{OUT}	1,2,3,5
	Asynchronous Read	H	L	L	H	Deasserted	X	X	H	X	X	Flash D _{OUT}	1,2,3,5
	Write	H	L	H	L	High-Z	L	V _{PPL} OR V _{PPH}	H	X	X	Flash D _{IN}	1,2,3,4
	Output Disable	H	L	H	H	High-Z	X	X	Any SRAM mode allowed			Flash High-Z	1,2,3
	Standby	H	H	X	X	High-Z	X	X				Flash High-Z	1,2,3
	Reset	L	X	X	X	High-Z	X	X				Flash High-Z	1,2,3

Table 16: Flash + SRAM Bus Operations (Sheet 2 of 2)

Device	Mode	F-RST#	F-CE#	OE#	WE#	WAIT	ADV#	F-VPP	S-CS1#	S-CS2	R-UB#, R-LB#	DQ[15:0]	Notes
SRAM	Read	X	H	L	H	High-Z	X	X	L	H	L	SRAM D _{OUT}	1,2,3
	Write	X	H	H	L	High-Z	X	X	L	H	L	SRAM D _{IN}	1,2,3
	Output Disable	Any Flash mode allowed							L	H	X	SRAM High-Z	1,2,3,5,6
	Standby								H	H	X	SRAM High-Z	1,2,3,5,6
	Data Retention								Same as SRAM Standby			SRAM High-Z	1,6

Notes:

- Flash + SRAM Bus Operations only applicable with 103-Active Ball High-Performance DRAM ballout.
- OE# and WE# should never be asserted simultaneously.
- X can be V_{IL} or V_{IH} for flash or RAM inputs. V_{DDL} or V_{DDH} for F-VPP.
- Refer to the latest revision of the L18 datasheet for valid D_{IN} during Flash writes.
- Flash CFI query and Status Register accesses use DQ[7:0] only, all other reads use DQ[15:0].
- The SRAM can be placed into data retention mode by lowering S-VCC to the V_{DR} limit when in standby mode.

10.0 Flash Operations

Refer to the *Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for detailed information on the following:

- Read Operations
- Program Operations
- Erase Operations
- Suspend and Resume Operations
- Block Locking and Unlocking Operations
- Protection Register Operations
- Configuration Operations
- Dual Operations Considerations
- Memory Map and Partitioning
- Flash Write State Machine
- Flash Common Flash Interface
- Flash Flowcharts

11.0 LPSDRAM Register Definition

11.1 Mode Register

The Mode Register is used to define specific modes of operation of the LPSDRAM. This definition includes the selection of a burst length, burst type, a D-CAS# latency, and a write burst mode. The Mode Register settings are illustrated in the Table below. The Mode Register is programmed by the Load Mode Register command and will retain the information until it is reprogrammed, the LPSDRAM loses power, or the LPSDRAM goes in Deep Power-Down mode. The register should be loaded when all banks are idle, and subsequent operation should only be initiated after t_{MRD} .

Addresses A[12, 11, 9, 8] must be set to "0" for all Mode Register programming. D-BA[1:0] should be set to (0,0) to differentiate from Extended Mode Register programming.

Table 17: LPSDRAM Setting for Burst Length

Burst Length		A3	A2	A1
A4 = 0	A4 = 1			
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Full Page	Reserved	1	1	1

Notes:

1. States not mentioned are undefined.
2. The sequential burst will wrap on reaching the last column of the burst length.

Table 18: LPSDRAM Setting for Burst Type

A4	Burst Type
0	Sequential
1	Interleaved

Table 19: LPSDRAM Setting for D-CAS# Latency

A7	A6	A5	CAS# Latency
0	0	1	1
0	1	0	2
0	1	1	3

Note: CAS# Latency not mentioned are undefined.

Table 20: LPSDRAM Setting for Write Burst Mode

A10	Write Burst Mode
0	Programmed Burst
1	Single Word Burst

11.2 LPSDRAM Extended Mode Register

The Extended Mode Register controls two power saving functions: Temperature-Compensated Self-Refresh (TCSR), and Partial-Array Self-Refresh (PASR). Both these features can only be used when the LPSDRAM is under Self-Refresh. In addition, the Configurable Output Driver Strength can be programmed through the Extended Mode Register.

The Extended Mode Register is programmed by the Load Mode Register command and will retain the information until it is reprogrammed, the LPSDRAM loses power, or the LPSDRAM goes in Deep Power-Down mode. The register should be loaded when all banks are idle, and subsequent operation should only be initiated after t_{MRD} .

To program the Extended Mode Register, bank addresses D-BA1 = 1, and D-BA0 = 0 should be used. Addresses A[12:6] should be set to '0'.

Table 21: LPSDRAM Setting for Partial-Array Self-Refresh (PASR)

A3	A2	A1	Self-Refresh Coverage
0	0	0	Four Banks
0	0	1	Two Banks (Bank 0 & Bank 1)
0	1	0	One Bank (Bank 0)

Table 22: LPSDRAM Setting for Temperature-Compensated Self-Refresh

A5	A4	Maximum Ambient Temperature
1	1	85 °C
0	0	70 °C
0	1	45 °C
1	0	15 °C

Table 23: LPSDRAM Configurable Output Driver Strength

A7	A6	Strength	Output Load (pF)
0	0	Normal	30
0	1	Half	TBD
1	0	Reserved	NA
1	1	Reserved	NA

Note: LPSDRAM AC specs are guaranteed only when normal output driver strength is used.

12.0 LPSPDRAM Commands and Operations

12.1 LPSPDRAM No Operation / LPSPDRAM Deselect

The NOP (No Operation) / LPSPDRAM Deselect command is used on a LPSPDRAM that is selected (D-CS# low). It is also used to deselect the LPSPDRAM by preventing new commands from being executed. Operations already in progress are not affected.

12.2 LPSPDRAM Active

The Active command is used to activate a row in particular bank for a subsequent read or write access. The value of the bank D-BA[1:0] and the row address needs to be provided. The row remains active until a precharge command is issued to the bank. A Precharge command must be issued before opening a different row in the same bank.

More than one bank can be active at any time. A read or write command could be issued to that row, subject to the t_{RCD} specification. t_{RCD} (min) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the active command on which the read/write can be entered. A subsequent Active command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive active commands on the same bank is defined by t_{RC} . The minimum time interval between two successive active commands on the different banks is defined by t_{RRD} . This is illustrated in [Figure 11 on page 38](#).

12.3 LPSPDRAM Read Command

Read command is used to initiate a burst read to an active row. The value of D-BA[1:0] select the bank and address inputs select the starting column location. The value of A11 determines whether or not auto precharge is used. Output data appears on the data bus, subject to the logic level on the D-DM[1:0] inputs two clocks earlier. D-DM[1:0] latency for read command is 2 clock cycles.

The burst length is set in the mode register. The starting column and bank address is provided along with the auto precharge option. During read bursts, the starting valid data-out corresponding to the starting column address will be available after CAS latency cycles after the read command. Each subsequent data-out will be valid by the next positive edge of the clock. This is shown in [Figure 12, "LPSPDRAM Example of D-CAS# Latency, CL = 2" on page 38](#) with a CAS latency of 2. Data from a read burst may be truncated by a subsequent read command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new read command can be issued as early as CL-1 cycles before the last desired element. This is shown in [Figure 13, "Consecutive LPSPDRAM Read Bursts with CL = 2" on page 39](#).

[Figure 14 on page 39](#) shows random LPSPDRAM access reads. These can be issued to the same or different banks.

A read burst can be terminated by a subsequent write command, and data from a fixed length read burst can be followed by a write command. The write command may be initiated on the clock edge immediately following the last data element from the read burst, provided the I/O contention could be avoided. D-DM[1:0] can be used to control I/O contention as shown in [Figure 15, "LPSPDRAM Read to LPSPDRAM Write Command" on page 39](#). D-DM[1:0] latency is 2 clocks for output buffers masking, so the D-DM[1:0] signal must be set high at least 2 clocks prior to the write command. D-DM[1:0] latency for write is zero clocks, so D-DM[1:0] must be set low before write command to ensure data written is not masked.

A read burst may be followed by or truncated with a Precharge command, which could be issued t_{RP} cycles before the last desired element. This is shown in Figure 16, “LPSDRAM Read Command Followed by Precharge” on page 40. Following Precharge command, another command to the same bank cannot be issued until t_{RP} is met. Similarly Burst Terminate command can be used to stop a burst as shown in Figure 17, “LPSDRAM Read Followed by Burst Terminate” on page 40.

12.4 LPSDRAM Write Command

The write command is used to initiate a burst write access to an active row. The value of D-BA[1:0] select the bank and address inputs select the starting column location. The value of A11 determines whether or not auto precharge is used. Input data appearing on the data bus, is written to the memory array subject to the D-DM[1:0] input logic level appearing coincident with the data. D-DM[1:0] latency for write command is 0-clock cycle.

The burst length is set in the mode register. The starting column and bank address is provided along with the auto precharge option. The first valid data-in is registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge. Figure 16, “LPSDRAM Read Command Followed by Precharge” on page 40 shows 2 consecutive 4 word write bursts. A write burst may be followed by or truncated with a Precharge command to the same bank. The Precharge should be issued t_{WR} after the clock edge after the last desired input data is entered. In addition, when truncating a Write burst, the D-DM[1:0] signal must be used to mask input data for the clock edge coincident with the precharge command. This is shown in Figure 19 and Figure 20 on page 41, where t_{WR} corresponds to either 1 or 2 clock cycles, respectively. Following the Precharge command, a subsequent command cannot be issued to the same bank until t_{RP} is met.

Write Burst can be truncated with a Burst Terminate command. While truncating, the input data being applied coincident to the burst terminate will be ignored.

Data for any writes may be truncated by a subsequent Read command as shown in Figure 21 on page 41. Once the Read command is registered, the data inputs will be ignored.

12.5 LPSDRAM Power-Down

Power-down occurs if D-CKE is set low coincident with LPSDRAM Deselect or NOP command and when no accesses are in progress. If power-down occurs when all banks are idle, it is Precharge Power-Down. If power-down occurs when one or more banks are active, it is referred to as Active power-down. The LPSDRAM cannot stay in this mode for longer than the refresh period (64 ms) without losing data. The Power-Down state is exited by setting D-CKE high while issuing a LPSDRAM Deselect or NOP command. This is shown in Figure 22 on page 42.

12.6 LPSDRAM Deep Power-Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPSDRAM are stopped and all memory data are lost in this mode. To enter the DPD mode, all banks must be precharged, prior to the DPD command. To exit this mode, the D-CKE is taken high after the clock is stable.

12.7 LPSPDRAM Clock Suspend

This mode occurs when a column access or burst is in progress, and D-CKE is set low. The internal clock gets suspended freezing the LPSPDRAM logic. Any command or data present on the input pins at the time of suspended internal clock is ignored. The output data on the pins stays frozen. This mode is exited by setting D-CKE high, which results in resumption of the operation. [Figure 23 on page 42](#) shown clock suspend during a write burst and [Figure 24 on page 43](#) shows a clock suspend during a read burst.

12.8 LPSPDRAM Precharge

The Precharge is used to deactivate an active row in a particular bank or active row in all banks. The banks will be available for row access after a specified time (t_{RP}) after the Precharge command is issued. If one bank is to be precharged, the particular bank address needs to be addressed. If all banks are to be precharged, A11 should be set high along with the Precharge command.

12.9 LPSPDRAM Auto Precharge

Auto Precharge is accomplished when A11 is high, to enable auto precharge in conjunction with a specific read or write command. This precharges the row after the read or write burst is complete. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst. Another command to the same bank must not be issued until the precharge time (t_{RP}) is completed. Auto precharge does not apply in full-page burst mode. Auto precharge is non-persistent.

12.10 LPSPDRAM Concurrent Auto Precharge

If an access command with Auto Precharge enabled is being executed, it can be interrupted by another access command.

- [Figure 25 on page 43](#) shows a Read with Auto Precharge to Bank n, interrupted by a Read (with or without Auto precharge) to bank m. The Read to bank m will interrupt the Read to Bank n, CAS latency later. The precharge to bank n will begin when the Read to bank m is registered.
- [Figure 26 on page 43](#) shows a Read with Auto Precharge to Bank n, interrupted by a Write (with or without Auto precharge) to bank m. The precharge to bank n will begin when the Write to bank m is registered. D-DM[1:0] should be set high 2 clock before the Write command to prevent bus contention.
- [Figure 27 on page 44](#) shows a Write with Auto Precharge to Bank n, interrupted by a Read (with or without Auto precharge) to bank m. The new command initiates bank n Write recovery (t_{WR}) followed by precharge. The last valid data-in to bank n is 1 clock prior to the Read to bank m.
- [Figure 28 on page 44](#) shows a Write with Auto Precharge to Bank n, interrupted by a Write (with or without Auto precharge) to bank m. The new command initiates bank n Write recovery (t_{WR}) followed by precharge. The last valid data-in to bank n is 1 clock prior to the Write to bank m.

Figure 13: Consecutive LPSDRAM Read Bursts with CL = 2

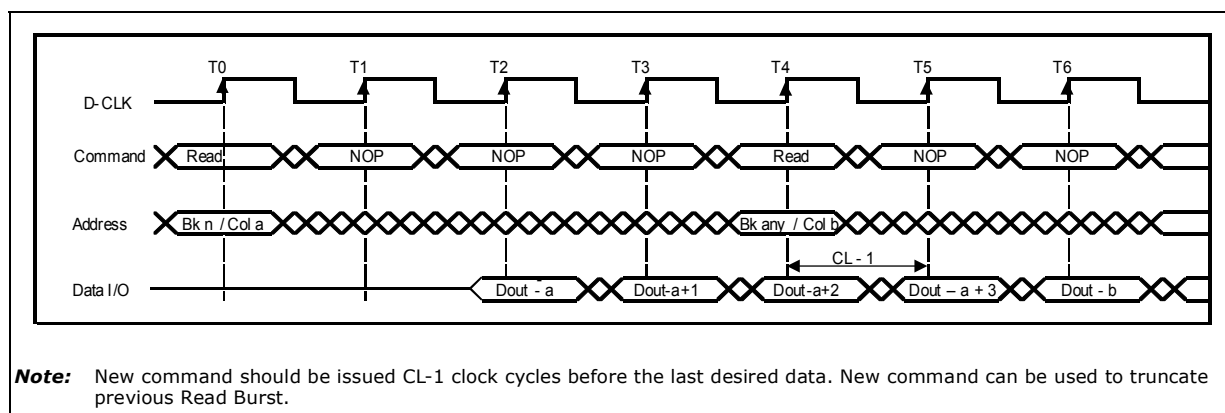


Figure 14: Random LPSDRAM Read Access with CL = 2

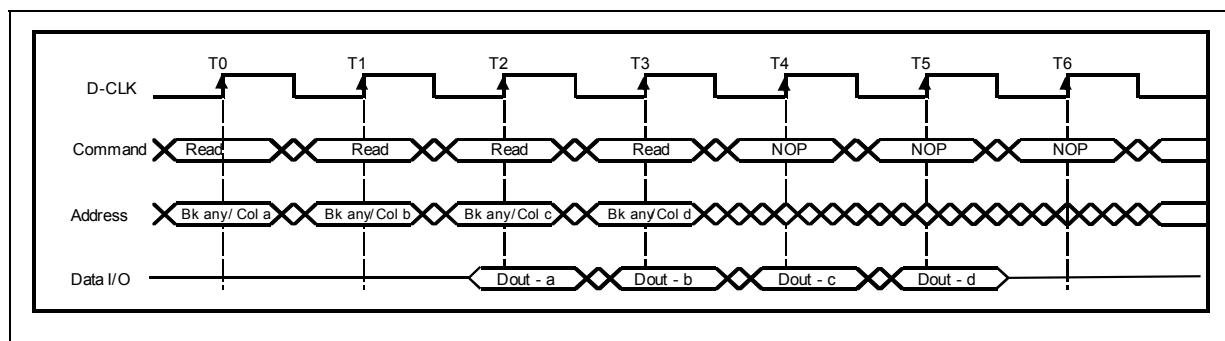


Figure 15: LPSDRAM Read to LPSDRAM Write Command

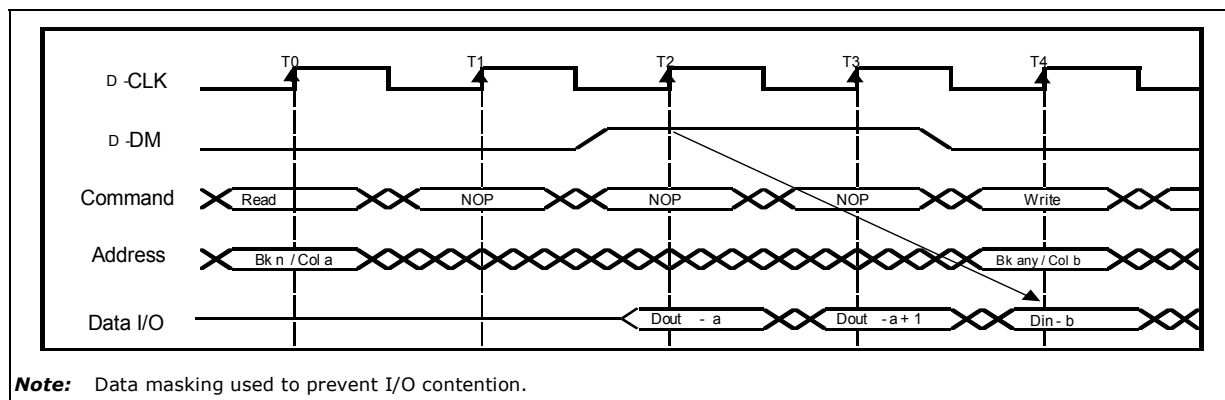


Figure 16: LPSDRAM Read Command Followed by Precharge

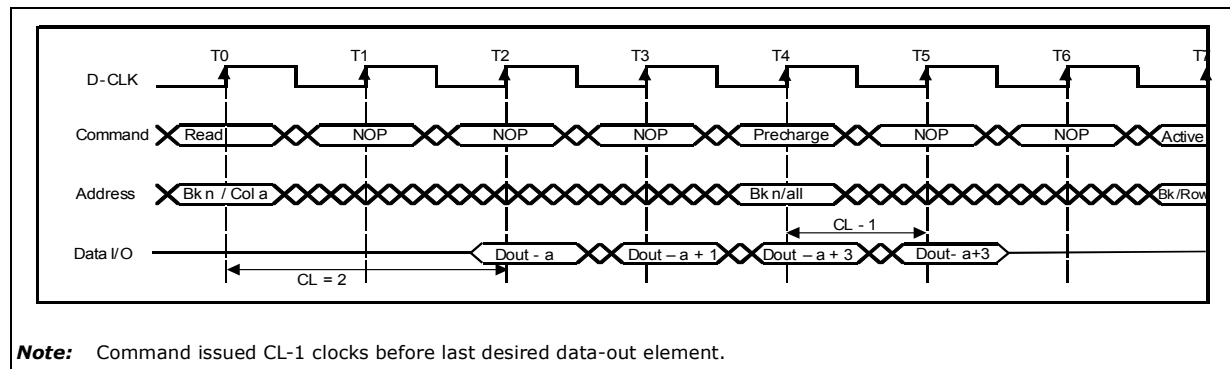


Figure 17: LPSDRAM Read Followed by Burst Terminate

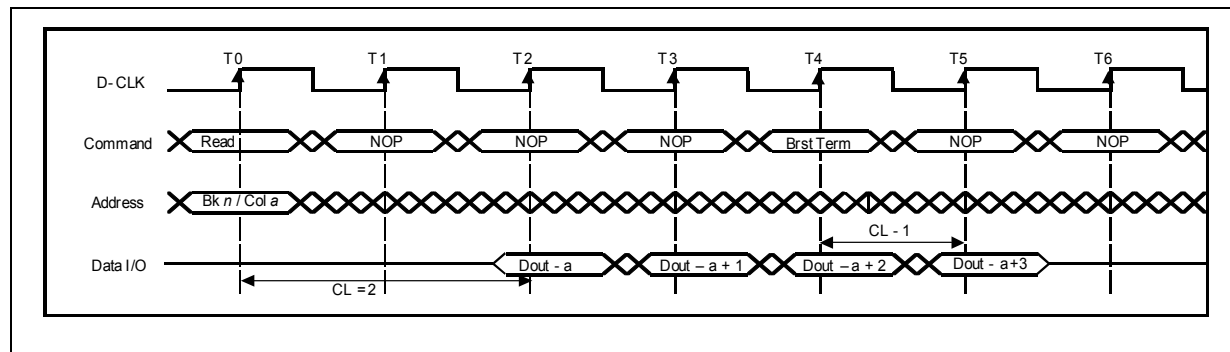


Figure 18: Random LPSDRAM Write to 4-Word Bursts

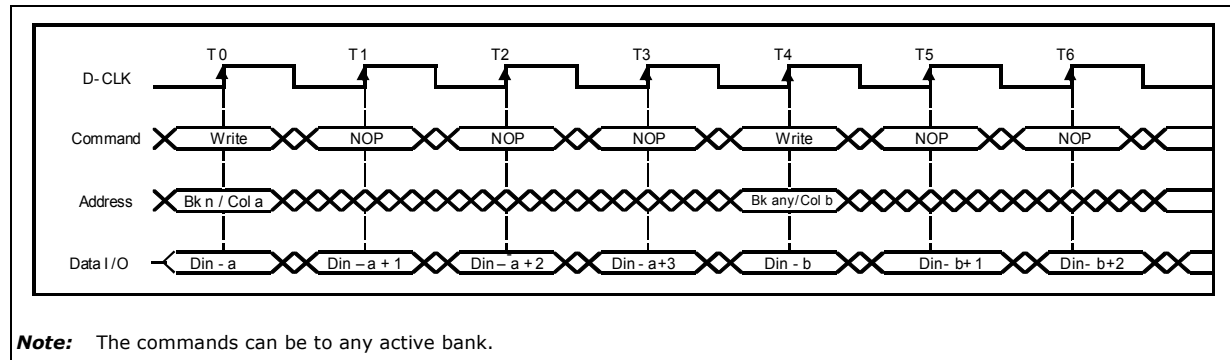


Figure 19: LPSDRAM Write to Precharge Command Where Write Recovery Takes 1 Clock Cycle

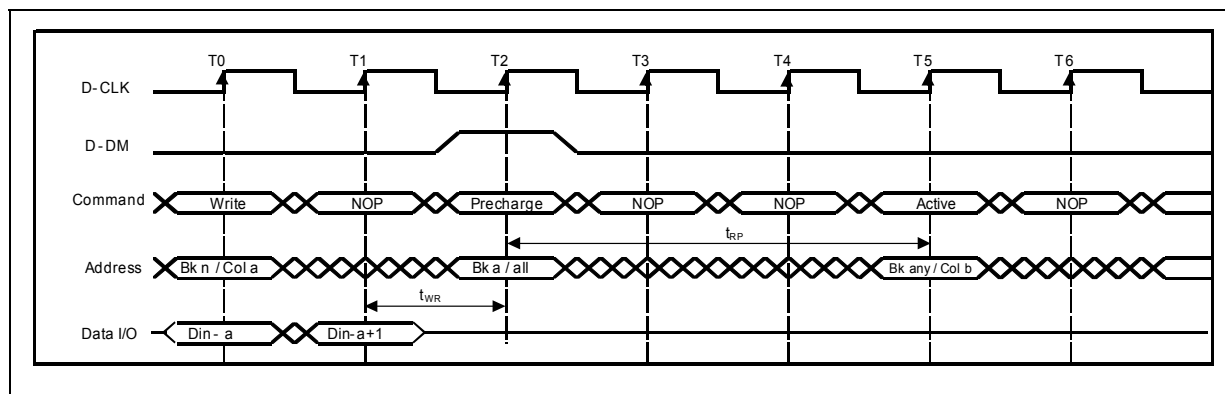


Figure 20: LPSDRAM Write to Precharge Command Where Write Recovery Takes 2 Clock Cycles

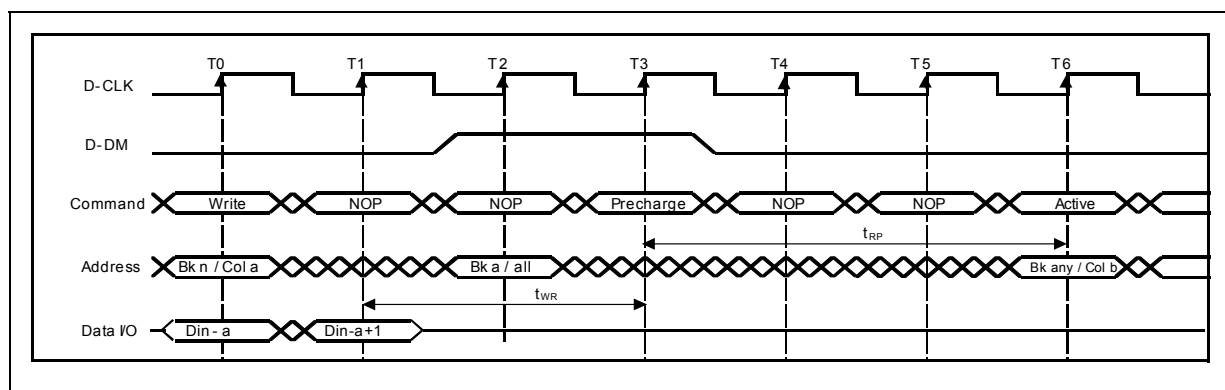
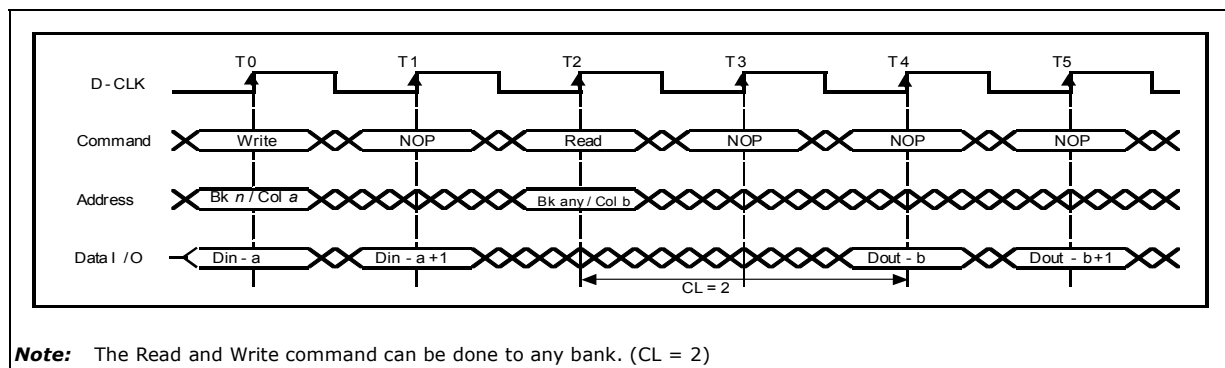


Figure 21: LPSDRAM Write Command Followed by LPSDRAM Read Command



Note: The Read and Write command can be done to any bank. (CL = 2)

Figure 22: LPSDRAM Precharge Power-Down Mode

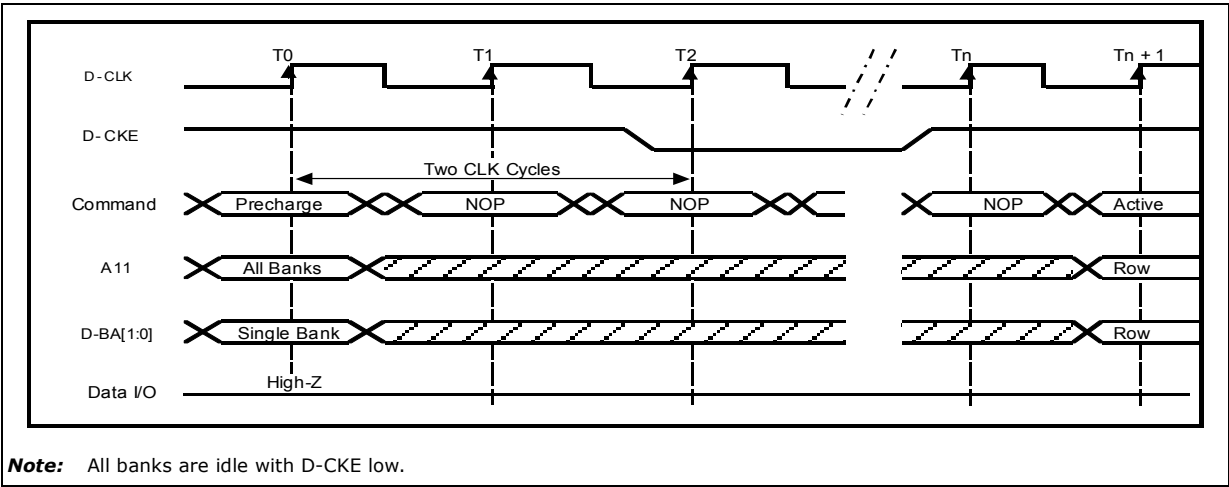


Figure 23: LPSDRAM Clock Suspend During LPSDRAM Write Burst

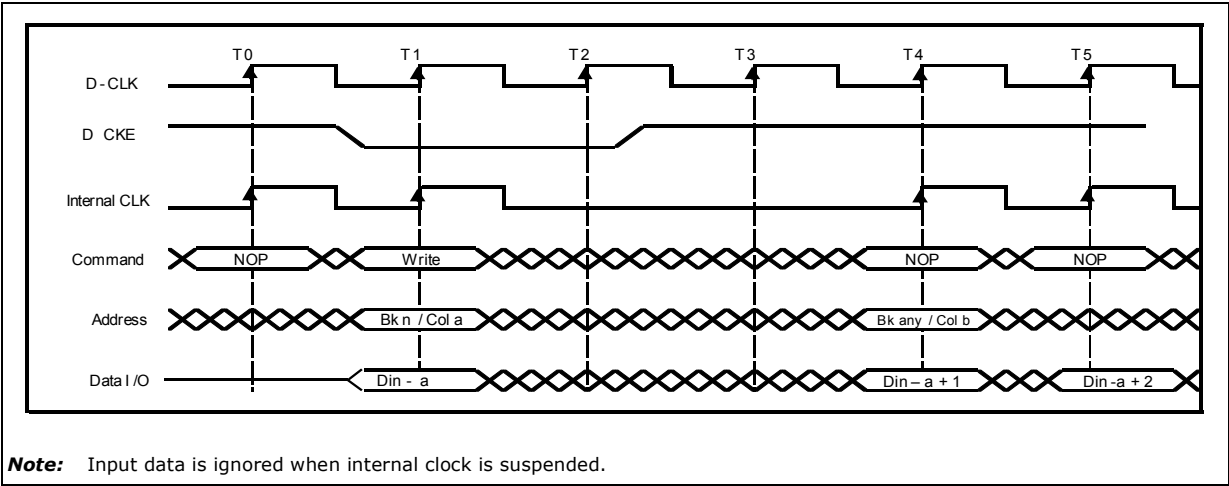


Figure 24: LPSPDRAM Clock Suspend During LPSPDRAM Read Burst (CL = 2)

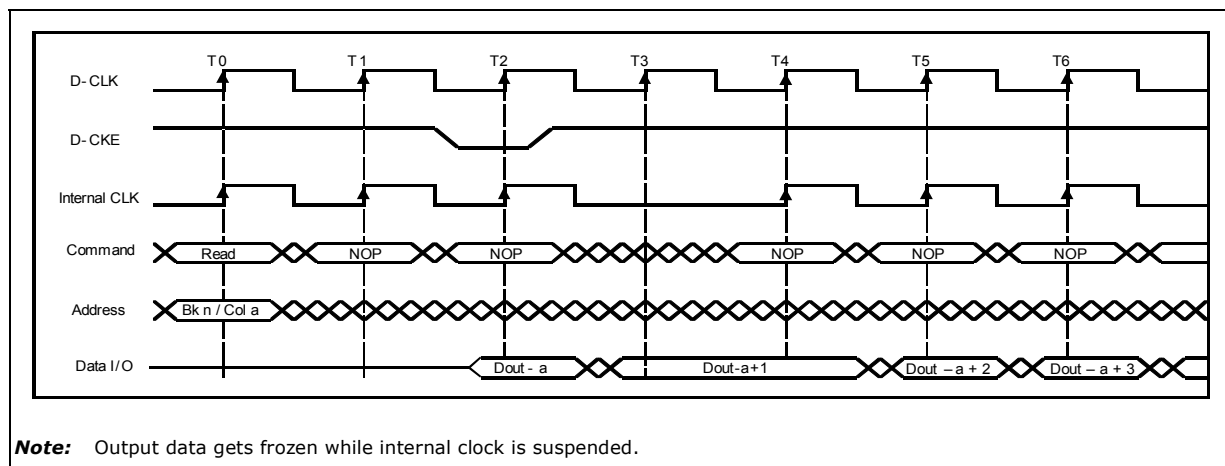


Figure 25: LPSPDRAM Read with Auto Precharge to Bank n Interrupted by Read to Bank m

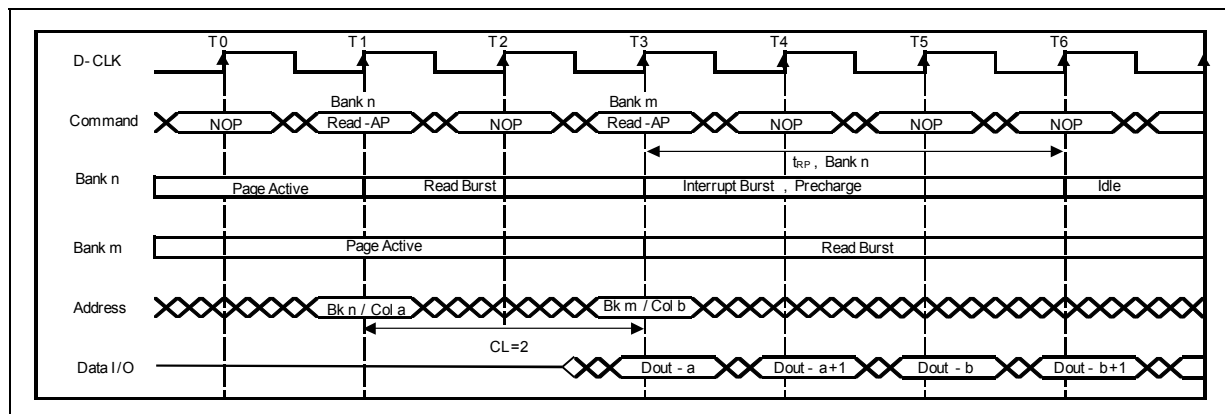


Figure 26: LPSPDRAM Read with Auto Precharge to Bank n Interrupted by Write to Bank m

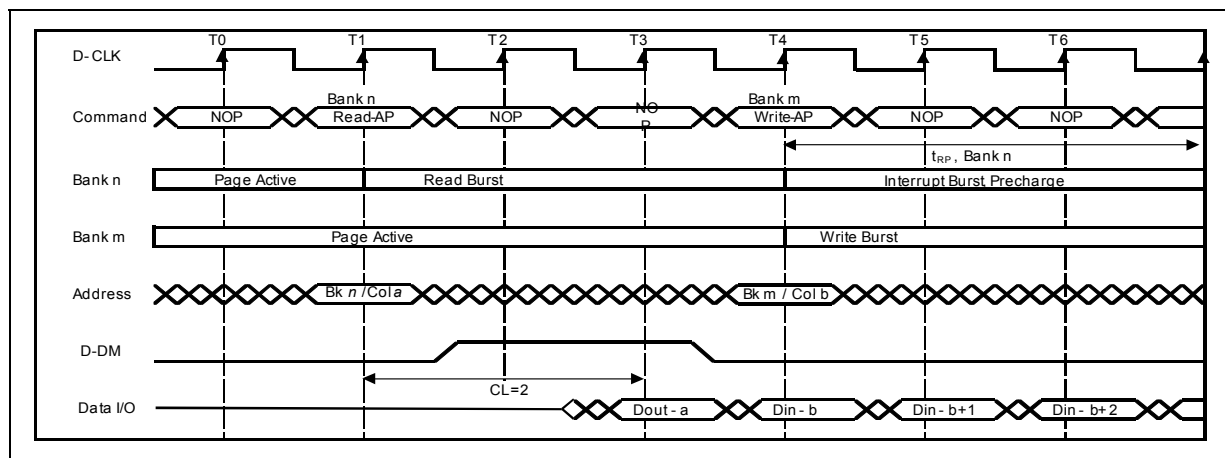
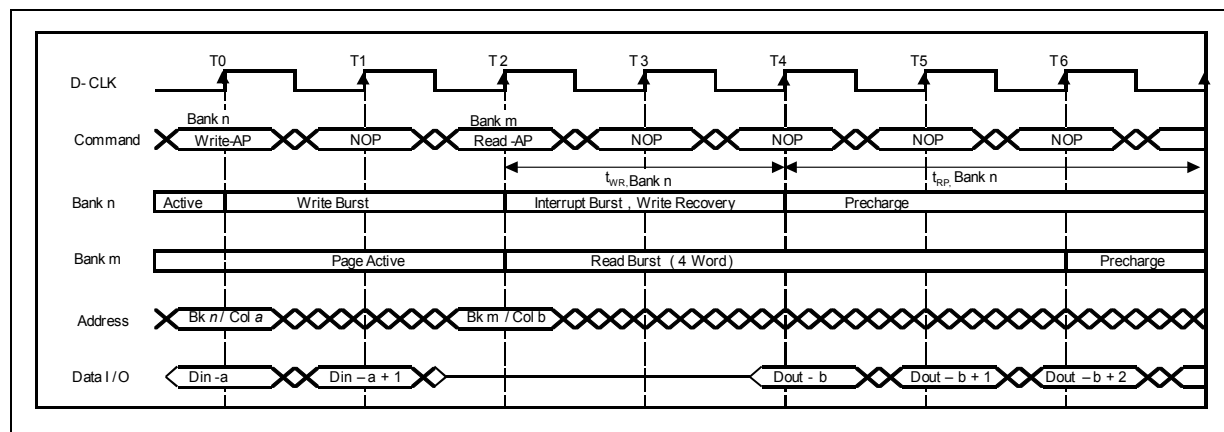
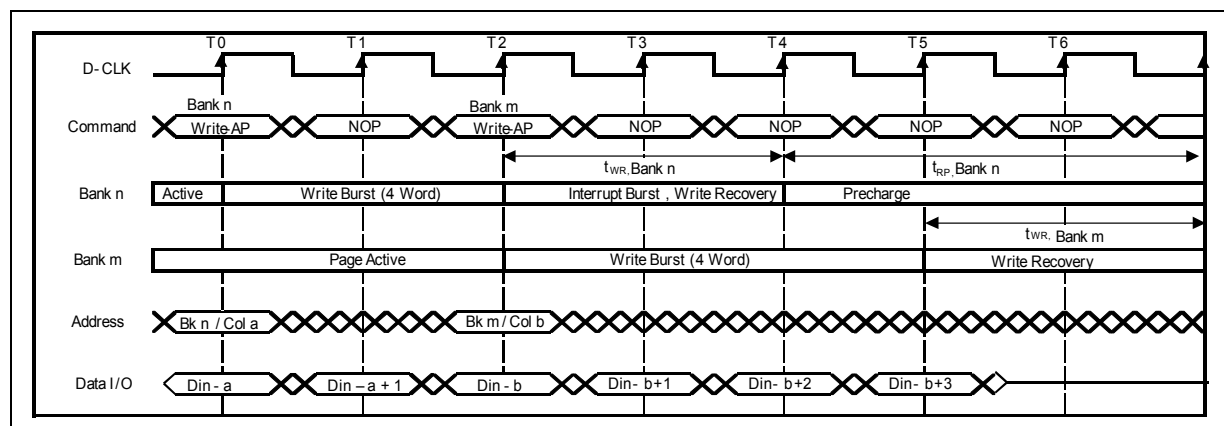


Figure 27: LPSPDRAM Write with Auto Precharge to Bank n Interrupted by Read to Bank m

Figure 28: LPSPDRAM Write with Auto Precharge to Bank n Interrupted by Write to Bank m


12.11 LPSPDRAM Burst Terminate

This command is used to truncate bursts. The most recent command prior to the burst terminate command will be truncated.

12.12 LPSPDRAM Auto-Refresh

This command is used during normal operation of the LPSPDRAM. This command is non-persistent. All banks must be idle before issuing Auto-Refresh command. This command can be issued after a minimum of t_{RP} after the precharge command. The address bits are "Don't care" during the Auto-Refresh command. As an example, the 256-Mbit LPSPDRAM requires 4096 auto refresh cycles (4096 rows/bank) every 64 ms (t_{REF}). Providing a distributed Auto-Refresh command every 15.625 μ s will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4096 refresh command cycles can be issued in a burst at a minimum cycle rate (t_{RFC}), once every 64 ms. [Figure 9 on page 38](#) shows auto refresh cycles.

12.13 LPSPDRAM Self-Refresh

This state retains data in the LPSPDRAM, even as the rest of the system is powered down. The Self-Refresh command is initiated like the auto refresh command, except the D-CKE is disabled (low). All banks must be idle before this command is issued. Once the Self-Refresh command is registered, all inputs become "Don't Care" except D-CKE, which must remain low. The procedure for exiting Self-Refresh mode requires a series of commands. First clock must be stable before D-CKE going high. NOP commands should be issued (minimum of 2 clocks) to meet the refresh exit time (t_{SREX}) limitation. [Figure 10 on page 38](#) shows self refresh entry and exit mode.

Appendix A Ordering Information

To order samples, obtain datasheets or inquire about any stack combination, please contact your local Numonyx representative.

Table 24: 38F Type Stacked Components

PF	38F	5070	M0	Y	0	B	0
Package Designator	Product Line Designator	Product Die/ Density Configuration	NOR Flash Product Family	Voltage/NOR Flash CE# Configuration	Parameter / Mux Configuration	Ballout Identifier	Device Details
PF = SCSP, RoHS RD = SCSP, Leaded	Stacked NOR Flash + RAM	Char 1 = Flash die #1 Char 2 = Flash die #2 Char 3 = RAM die #1 Char 4 = RAM die #2 (See Table 26, "38F / 48F Density Decoder" on page 46 for details)	First character applies to Flash die #1 Second character applies to Flash die #2 (See Table 27, "NOR Flash Family Decoder" on page 47 for details)	V = 1.8 V Core and I/O; Separate Chip Enable per die (See Table 28, "Voltage / NOR Flash CE# Configuration Decoder" on page 47 for details)	0 = No parameter blocks; Non-Mux I/O interface (See Table 29, "Parameter / Mux Configuration Decoder" on page 47 for details)	B = x16D Ballout (See Table 30, "Ballout Decoder" on page 48 for details)	0 = Original released version of this product

Table 25: 48F Type Stacked Components

PC	48F	4400	P0	V	B	0	0
Package Designator	Product Line Designator	Product Die/ Density Configuration	NOR Flash Product Family	Voltage/NOR Flash CE# Configuration	Parameter / Mux Configuration	Ballout Identifier	Device Details
PC = Easy BGA, RoHS RC = Easy BGA, Leaded JS = TSOP, RoHS TE = TSOP, Leaded PF = SCSP, RoHS RD = SCSP, Leaded	Stacked NOR Flash only	Char 1 = Flash die #1 Char 2 = Flash die #2 Char 3 = Flash die #3 Char 4 = Flash die #4 (See Table 26, "38F / 48F Density Decoder" on page 46 for details)	First character applies to Flash dies #1 and #2 Second character applies to Flash dies #3 and #4 (See Table 27, "NOR Flash Family Decoder" on page 47 for details)	V = 1.8 V Core and 3 V I/O; Virtual Chip Enable (See Table 28, "Voltage / NOR Flash CE# Configuration Decoder" on page 47 for details)	B = Bottom parameter; Non-Mux I/O interface (See Table 29, "Parameter / Mux Configuration Decoder" on page 47 for details)	0 = Discrete Ballout (See Table 30, "Ballout Decoder" on page 48 for details)	0 = Original released version of this product

Table 26: 38F / 48F Density Decoder

Code	Flash Density	RAM Density
0	No Die	No Die
1	32-Mbit	4-Mbit
2	64-Mbit	8-Mbit
3	128-Mbit	16-Mbit
4	256-Mbit	32-Mbit
5	512-Mbit	64-Mbit
6	1-Gbit	128-Mbit
7	2-Gbit	256-Mbit
8	4-Gbit	512-Mbit
9	8-Gbit	1-Gbit
A	16-Gbit	2-Gbit
B	32-Gbit	4-Gbit
C	64-Gbit	8-Gbit
D	128-Gbit	16-Gbit
E	256-Gbit	32-Gbit
F	512-Gbit	64-Gbit

Table 27: NOR Flash Family Decoder

Code	Family	Marketing Name
C	C3	Numonyx Advanced+ Boot Block Flash Memory
J	J3v.D	Numonyx Embedded Flash Memory
L	L18 / L30	Numonyx™ StrataFlash® Wireless Memory
M	M18	Numonyx™ StrataFlash® Cellular Memory
P	P30 / P33	Numonyx™ StrataFlash® Embedded Memory
W	W18 / W30	Numonyx™ Wireless Flash Memory
0(zero)	-	No Die

Table 28: Voltage / NOR Flash CE# Configuration Decoder

Code	I/O Voltage (Volt)	Core Voltage (Volt)	CE# Configuration
Z	3.0	1.8	Seperate Chip Enable per die
Y	1.8	1.8	Seperate Chip Enable per die
X	3.0	3.0	Seperate Chip Enable per die
V	3.0	1.8	Virtual Chip Enable
U	1.8	1.8	Virtual Chip Enable
T	3.0	3.0	Virtual Chip Enable
R	3.0	1.8	Virtual Address
Q	1.8	1.8	Virtual Address
P	3.0	3.0	Virtual Address

Table 29: Parameter / Mux Configuration Decoder

Code, Mux Identification	Number of Flash Die	Bus Width	Flash Die 1	Flash Die 2	Flash Die 3	Flash Die 4
0 = Non Mux 1 = AD Mux ¹ 2 = AAD Mux 3 = Full" AD Mux ²	Any	NA	Notation used for stacks that contain no parameter blocks			
B = Non Mux C = AD Mux F = "Full" Ad Mux	1	X16	Bottom	-	-	-
	2		Bottom	Top	-	-
	3		Bottom	Bottom	Top	-
	4		Bottom	Top	Bottom	Top
	2	X32	Bottom	Bottom	-	-
	4		Bottom	Bottom	Top	Top

Table 29: Parameter / Mux Configuration Decoder

Code, Mux Identification	Number of Flash Die	Bus Width	Flash Die 1	Flash Die 2	Flash Die 3	Flash Die 4
T = Non Mux U = AD Mux W = "Full" Ad Mux	1	X16	Top	-	-	-
	2		Top	Bottom	-	-
	3		Top	Top	Bottom	-
	4		Top	Bottom	Top	Bottom
	2	X32	Top	Top	-	-
	4		Top	Top	Bottom	Bottom

1. Only Flash is Muxed and RAM is non-Muxed
2. Both Flash and RAM are AD-Muxed

Table 30: Ballout Decoder

Code	Ballout Definition
0 (Zero)	SDiscrete ballout (Easay BGA and TSOP)
B	x16D ballout, 105 ball (x16 NOR + NAND + DRAM Share Bus)
C	x16C ballout, 107 ball (x16 NOR + NAND + PSRAM Share Bus)
Q	QUAD/+ ballout, 88 ball (x16 NOR + PSRAM Share Bus)
U	x32SH ballout, 106 ball (x32 NOR only Share Bus)
V	x16SB ballout, 165 ball (x16 NOR / NAND + x16 DRAM Split Bus)
W	x48D ballout, 165 ball (x16/x32 NOR + NAND + DRAM Split Bus)