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3G Flash Procedures

Introduction

This document is intended to describe the flashing (firmware upgrade) procedures for 3G terminals. The 3G terminal described in this document will be limited to the E1000.

Firmware upgrades need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the firmware upgrade application database is up-to-date.

Firmware upgrades allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific circumstances, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the 3G terminal.

Power Hardware

1. Fully Charged battery (SNN5743A or equivalent)

2. Full-rate Charger (SPN5049 or equivalent)

Interface Options

1. USB Data Kit (S8951)
   USB Cable (SKN6311A)
   Data Software CD

Software Requirements

The RSD (Remote Software Download) General Release is used to allow functions such as firmware upgrade, Phone Swap, and Multi-refurbish. Contact your local Motorola service representative to receive download information for the RSD and related support files. Also insure that the RSD database has the latest update.

Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1-1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a nonfunctional (Bricked) 3G terminal.

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery
2. Full-Rate Charger w/battery (recommended)

If the user decides on using the battery only solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the flash process. This action may cause unrecoverable failures to the 3G terminal.

RSD Firmware Upgrade Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal.

1. Launch the RSD General application
2. Connect the unit as illustrated in figure 1-1.
3. Power up the 3G terminal
4. If the 3G terminal doesn't power up, refer to the Force Flash section.
5. Once the phone is fully powered up, the Radio Information Panel will be updated.
7. In the Utilities Panel, select Firmware Upgrade.
8. In the Main information Panel, select desired restore and logging options
9. In the Main information Panel, click on the Start button to begin Firmware upgrade.

NOTE: DO NOT interrupt any hardware connections during the flash process. Connection interruptions may cause the flashing process to fail and render the 3G terminal non-operational.

10. When the process is complete, the Main Information Panel will indicate whether the process was successful. At this time you may safely disconnect the 3G terminal.
11. Power up the 3G terminal to insure that the flash procedure was successful.

Figure 1-1. RSD Hardware Configuration

Figure 1-2. RSD General Release GUI

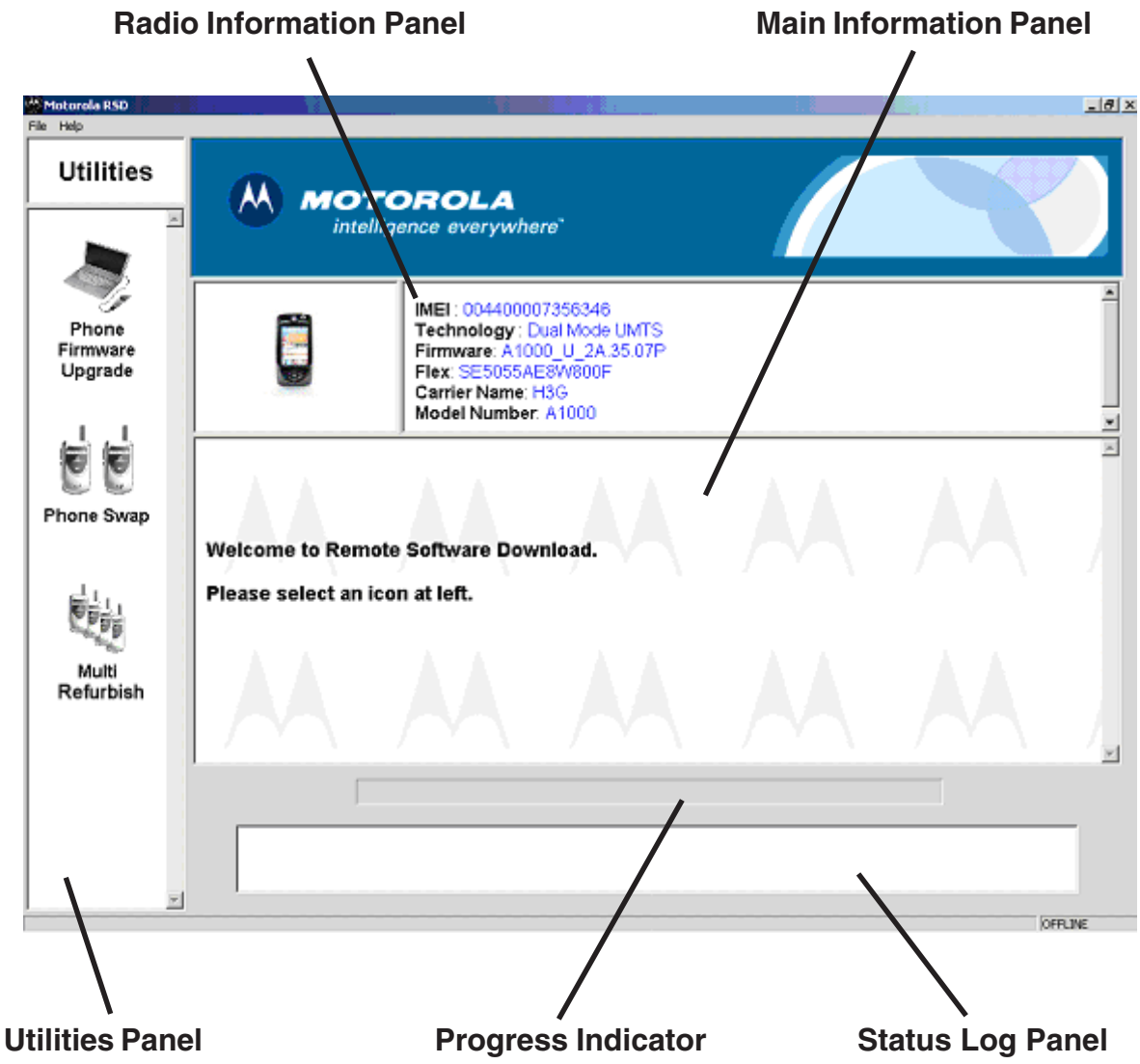
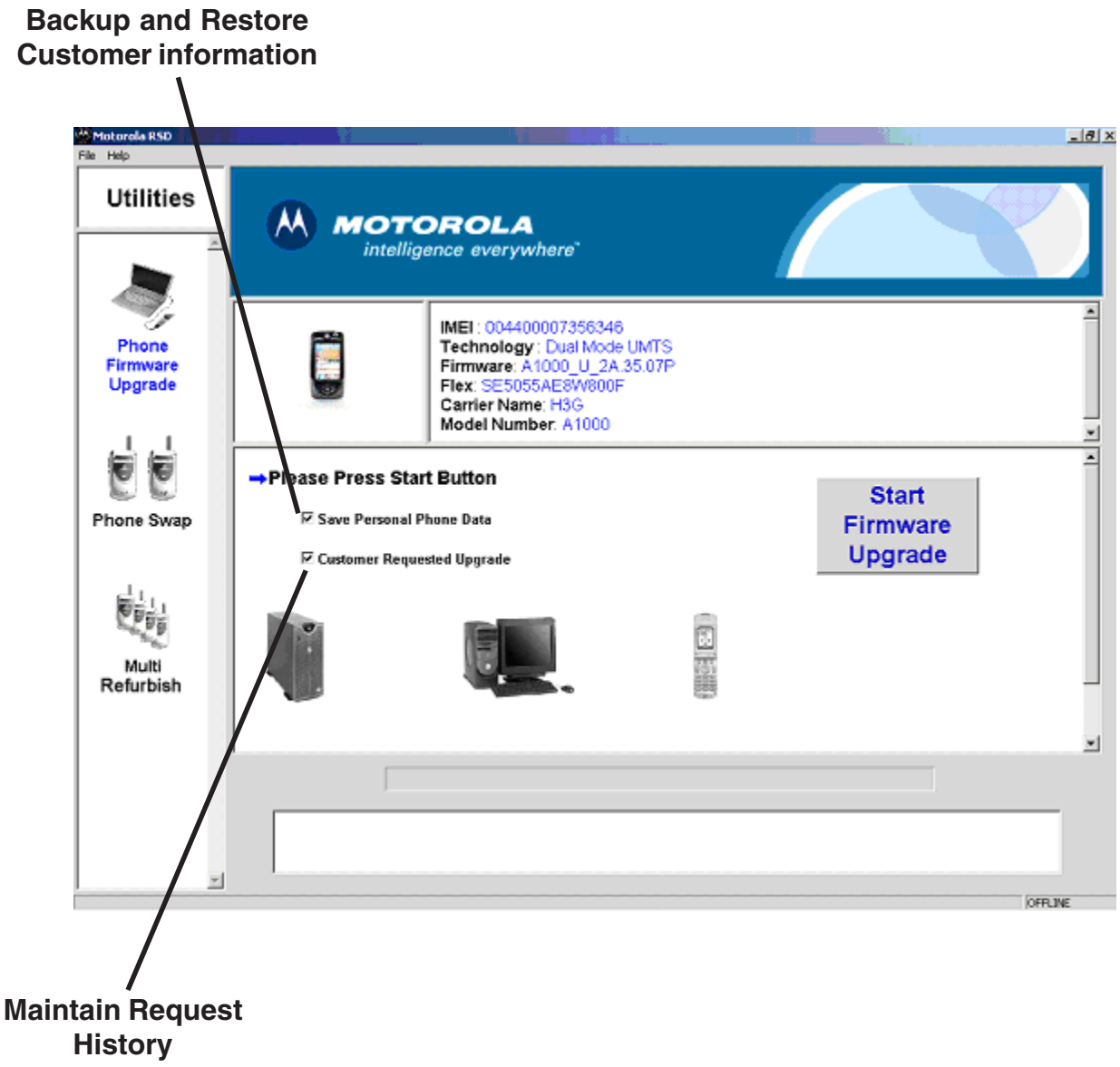


Figure 1-3. Firmware Upgrade



Force Flash Procedures

The procedures described in this section apply only to situations where the 3G terminal will not initiate it's normal power up sequence, but may recover functionality by a repeat flash procedure.

There are two possible alternatives to place the 3G terminal in force flash mode.

Key Hold Solution

Hardware: Refer to Figure 1 (USB solution)

Step 1. Remove the battery from the 3G terminal

Step 2. Prior to connecting the USB cable, press and hold "#" and "*" keys from the 3G terminal

Step 3. Attach the USB cable

Step 4. Verify that the RSD application detects the 3G terminal, if it's not detected, press and hold the gaming keys once again.

Force Flash USB Cable Solution

Hardware: Refer to Figure 1-1 (USB solution), except, replace USB cable (SKN6311A) with force flash cable (SKN6168A)

Step 1. Connect the force flash cable in the same manner described in Figure 1-1.

Step 2. The 3G terminal will automatically be placed in force flash mode. There's no need to press the power key. The RSD application will now detect the 3G terminal

Manual Test Procedures

Introduction

The phone allows computer controlled testing of various test parameters.

This chapter includes the computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

Non-Signaling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signaling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The phasing parameters are stored in an EPROM in the transceiver board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted (phased) with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5743A[1] or equivalent)
- Full-Rate Power Supply (SPN5049A[1])
- Battery Eliminator (5-00-3Y-12000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

RF Interface

- RF Adapter (2-00-4E-10000[2])
- SMA/N type Adapter (0-00-00-40042)
- SMA Cable 0.5m (0-00-00-40047[2])
- USIM (0-00-00-40810[2])

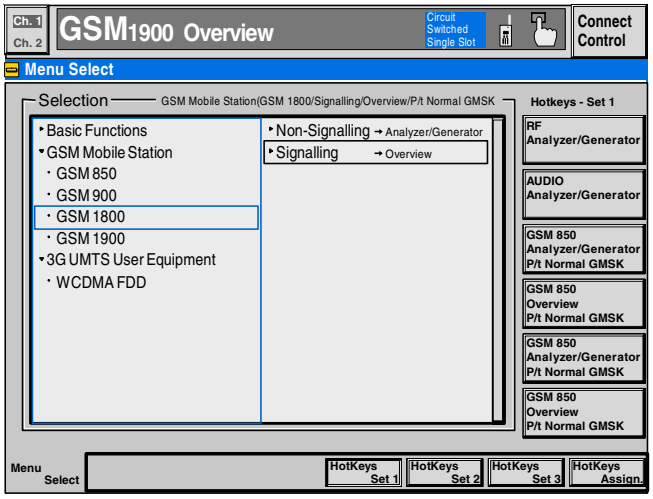
[2]Contact AMS Software and Elektronik GmbH for ordering

Call Origination

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

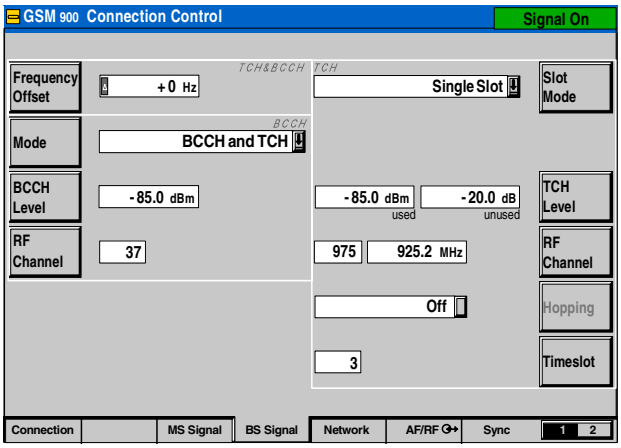
1. Install the test USIM in phone.
2. Connect hardware as illustrated in figure 2-5.

Figure 2-1. GSM Signaling Setup



3. Setup up the test box for GSM, DCS, or PCS Signaling
4. Set Broadcast Channel (BCH) to 120 (GSM), 700 (DCS), or 661 (PCS)
5. Set Broadcast channel level to -85dBm
6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS/PCS)
7. Set Traffic channel level to -85dBm
8. Wait until the phone indicates a receive signal

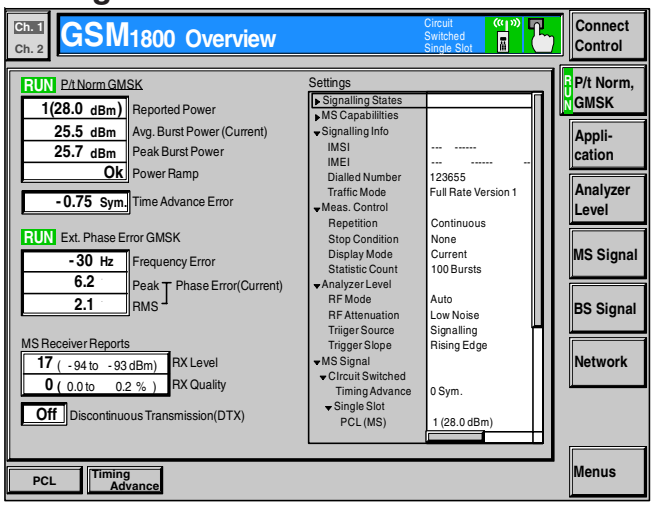
Figure 2-2. GSM Connection Control



9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 2-3. GSM Call Connected



Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-1. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	27	31	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 2-2. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

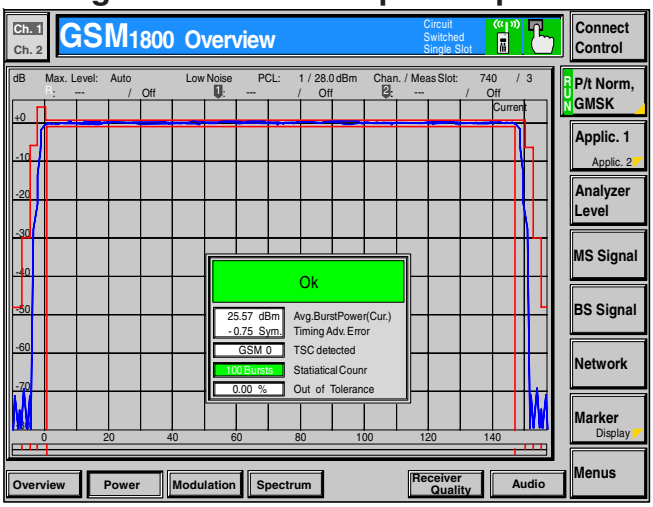
[1]Power Level = 15
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 2-3. PCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 15
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Figure 2-4. Burst Output Shape



Burst Output Shape should fall within the standard limits of the Power Ramp.

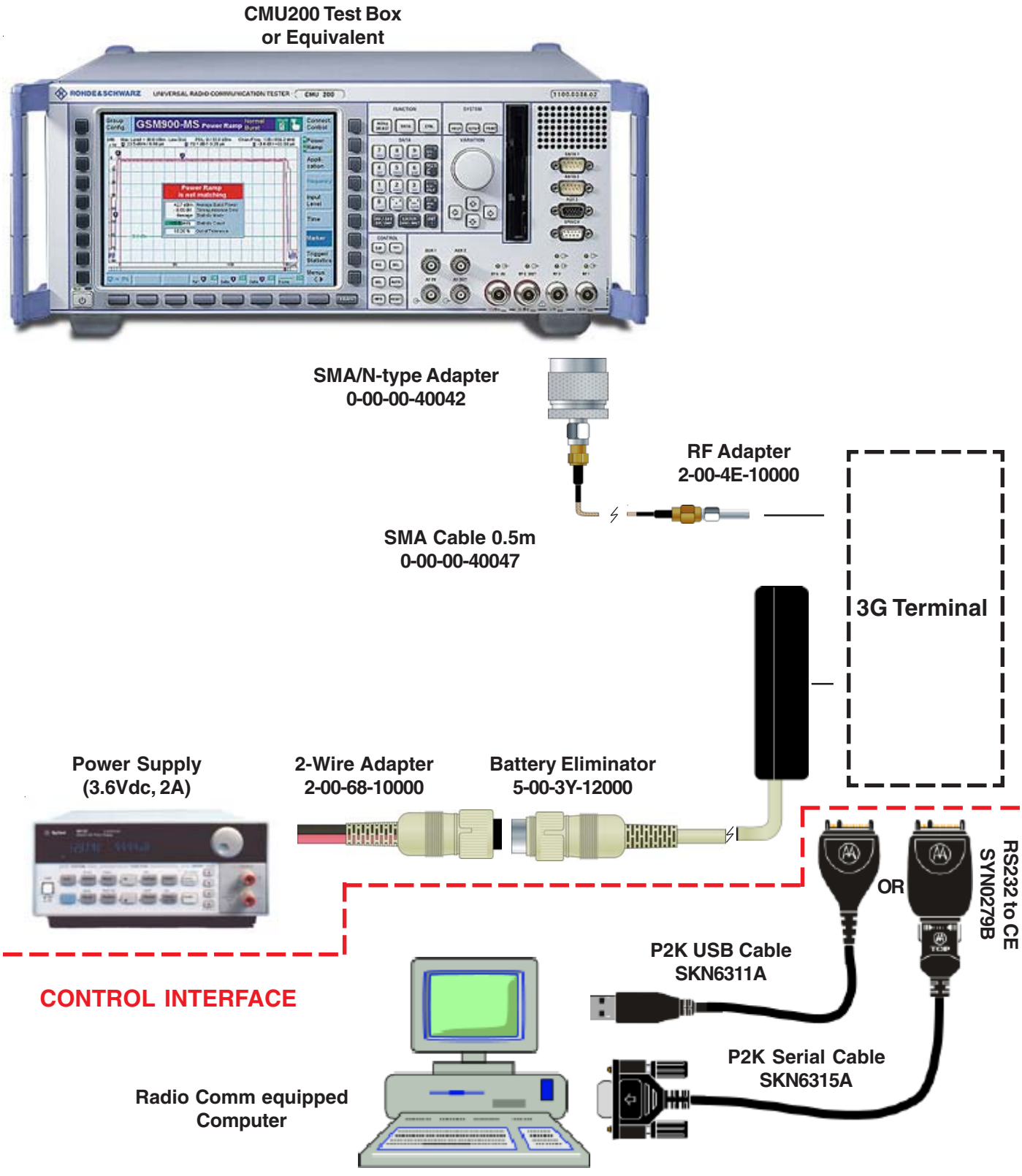
BER measurements is only required if RX Quality reads a value of 4 or greater.

It is recommended that handover procedures be performed as shown in the following table.

Table 2-4. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

Figure 2-5. Manual Test Hardware Configuration



WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 2-5.

Software Requirements

None.

Call Origination (WCDMA)

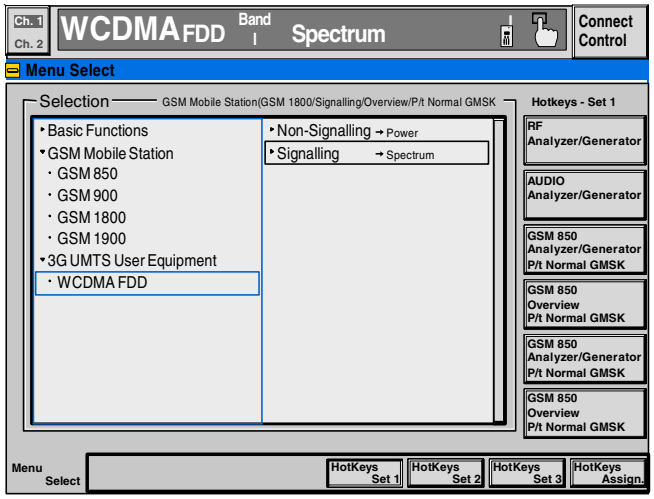
Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signaling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

Figure 2-6. WCDMA Signalling Setup

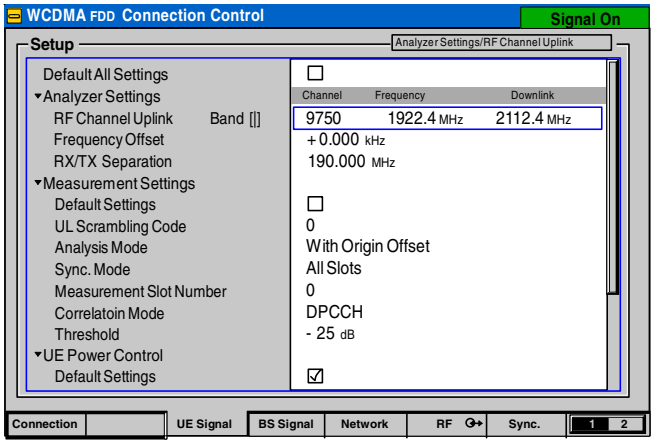


3. Setup up the test box for WCDMA FDD Signaling

4. Set UE Signal, RF Channel Uplink to 9400

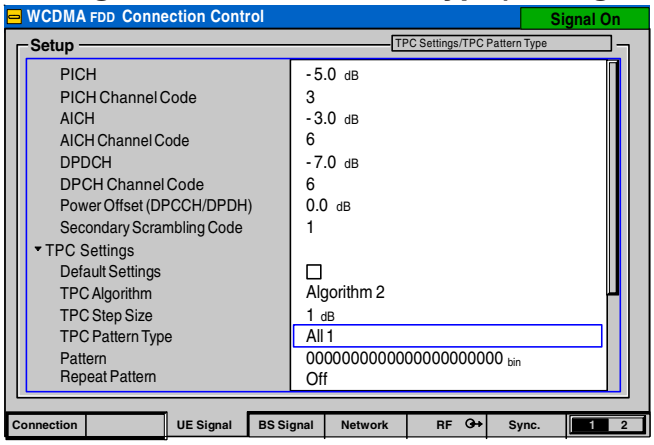
5. Set UE Signal, RF Channel Downlink to 9800

Figure 2-7. Channel Uplink(UE Signal)



6. Set TPC Pattern Type to All 1

Figure 2-8. TPC Pattern Type(UE Signal)

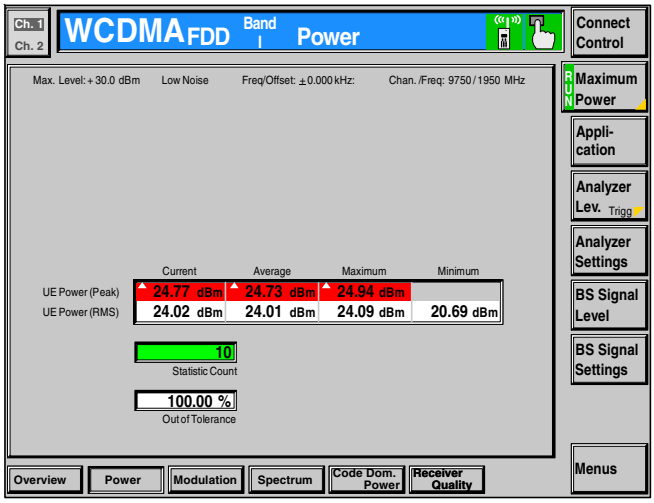


7. Wait until the phone indicates a signal

8. Dial a number from the phone and press the send button.

9. The phone is now connected.

Figure 2-9. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-5. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 2-10. WCDMA Modulation

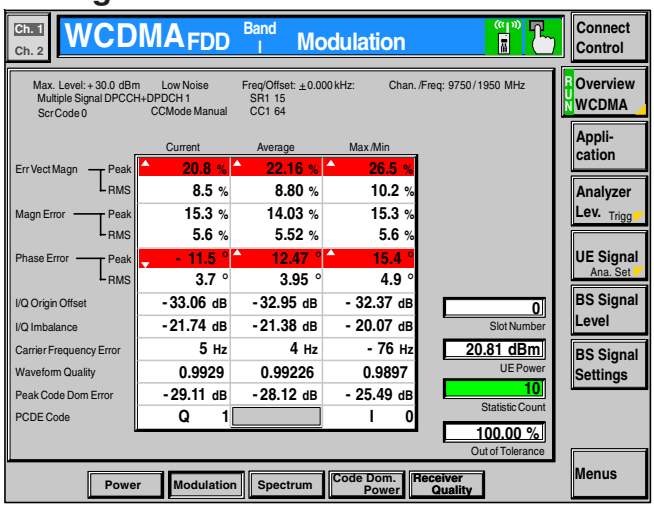
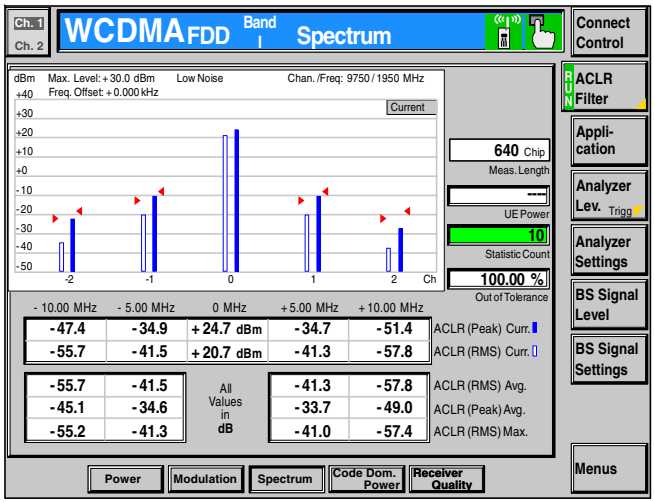


Figure 2-11. ACLR Screen

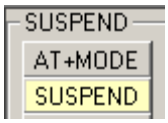


Non-Signaling Test Procedures (GSM/DCS/PCS)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands are sent using a computer.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)



Click SUSPEND (USB Only)

Hardware Requirements

Control Interface Options

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

[1]Contact your local Motorola dealer for ordering

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

Verify TX Power Output (GSM/DCS/PCS)

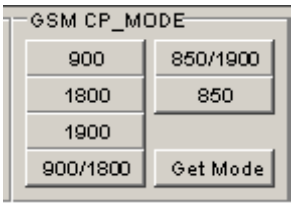
Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-6. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28.2	30	dBm
PCS TX Power Out	28.2	30	dBm

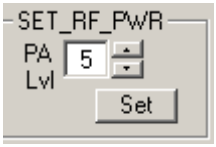
[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

Click on 900/1800 (GSM/DCS) or 1900 (PCS)

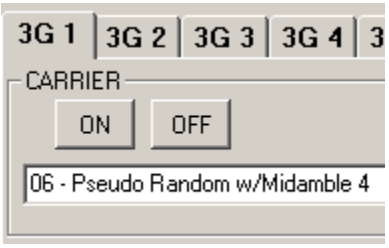


Enter 38 (GSM), 700 (DCS), or 661 (PCS) and then click Set

Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



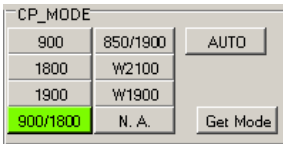
NOTE: Set Training Sequence to 4 on the test equipment.

GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

Broadcast Channel (BCH): 38
Broadcast Channel (BCH) Level: -105 dBm

Click on 850/1900 (GSM/DCS) or 1800 (DCS)



Enter Channel 38
Click INIT

Click Execute

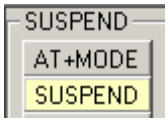
Verify return data is approximately -105 dBm

Non-signaling Test Procedures (WCDMA)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Hardware Requirements

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

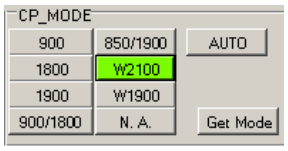
Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-7. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	19.5	22	dBm

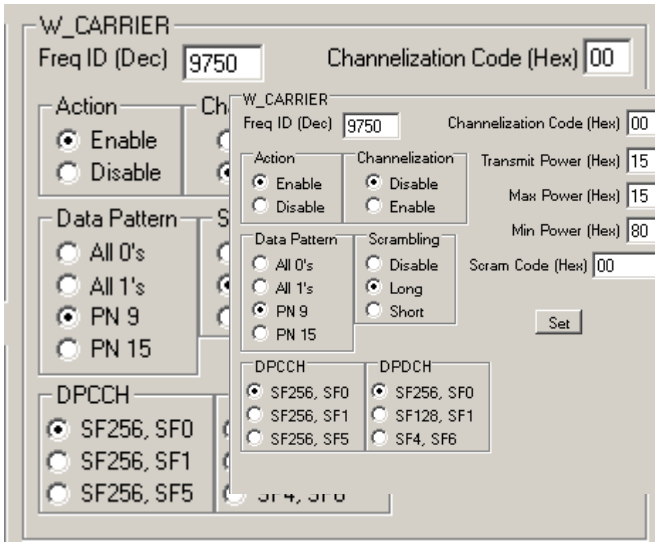
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)

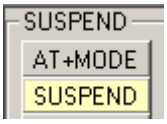


Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

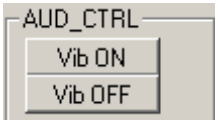
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Vibrator Test

Enable or Disable Vibrator



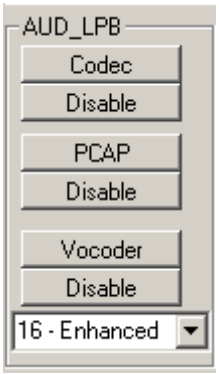
Verification

Verfiy vibration function when enabled.

Handset Mic/Speaker test

Set as illustrated.
Click Set

Select Enhanced Full Rate and click Vocoder



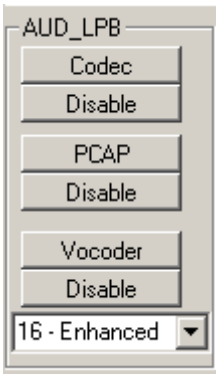
Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

Mono Headset Mic/Speaker test

Set as illustrated
Click Set

Select Enhanced Full Rate and click Vocoder

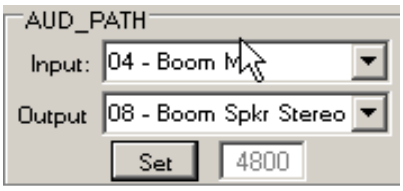


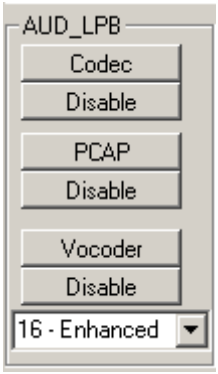
Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Stereo Headset Mic/Speaker test

Set as illustrated
Click Set





Select Enhanced Full Rate and click Vocoder

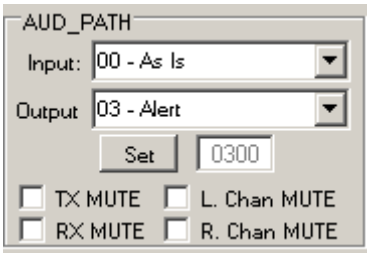
Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

Set AUD_TN_GEN as illustrated and click Start Tones

Set AUD_PATH as ilustrated and Click Set



Verification

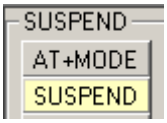
Listen for undistorted audio on the Alert.

Display Test Procedures

This section will describe the proper test procedures to determine the functionality of the color display.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Display Backlight Test

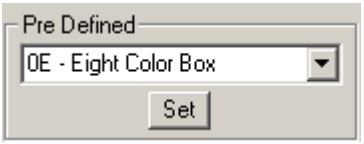
Click "FL Off" to disable backlight
Click "FL On-Full" to enable backlight

Verification

Verify that the backlights respond for each issued command.

Display Color Test

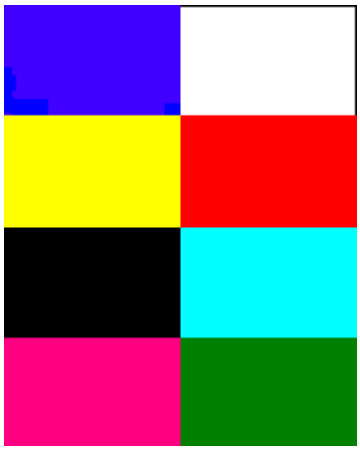
Select Eight Color Box and click "Set"



Verification

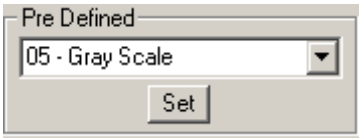
Verify that the color pattern on the phone's display matches the color box in figure 23. Also verify edges (uniform/smooth).

Figure 20. Eight Color Box Pattern



Display Linearity Test

Select Grey Scale and click “Set”



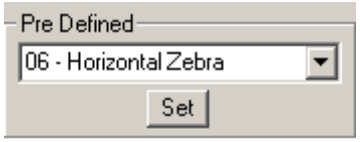
Verification

Verify that the Grey scale block on the phone’s display matches the Grey scale block in figure 14. This test can also be used to confirm that the color intensity is linear.

Figure 21. Grey Scale Block

Display Flicker Test

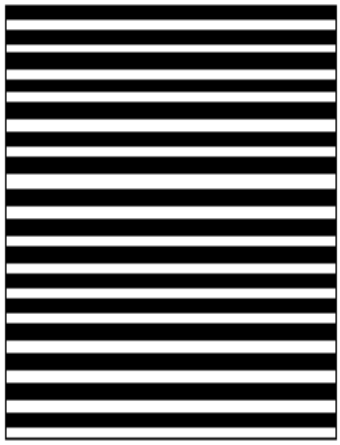
Select Horizontal Zebra and click “Set”



Verification

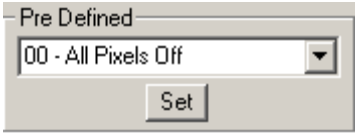
Verify that no noticable flicker exists.

Figure 22. Zebra Pattern



Display Pixel Defect (Bright)

Select All Pixels Off and click “Set”

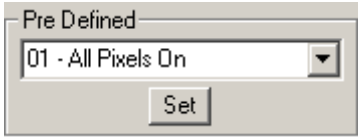


Verification

Verify that no greater than two pixels are off.

Display Pixel Defect (Dark)

Select All Pixels On and click “Set”



Verification

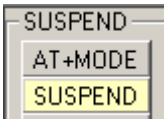
Verify that no greater than two pixels are on.

LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

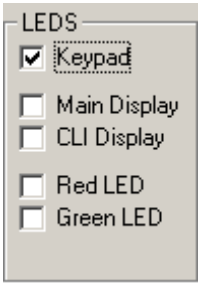
In order to successfully send test commands to the phone under test, the phone doesn’t need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Click AT+MODE (Serial Only)



Keypad Backlight

Select Keypad to enable. Deselect Keypad to disable.



Verification

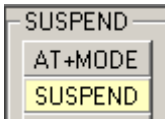
Verify that all keypad backlight LEDs activate.

Camera Testing

This section is intended to describe the procedures that will determine whether the camera function of a Motorola terminal is under normal operating conditions.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

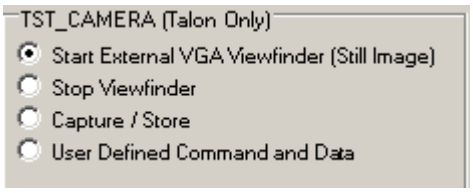
Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



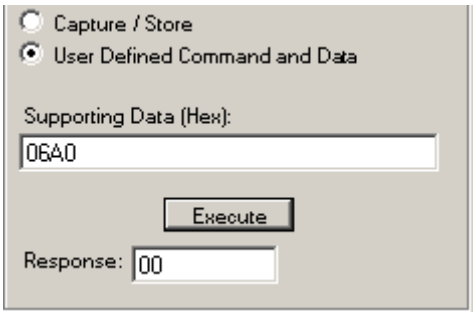
Data Line Integrity Check

When performing this test, RadioComm needs to be switched to GSM for proper responses. Go to the Menu bar and select Main>MA>GSM.

Select Start External Viewfinder



Select User Defined Command, enter 06A0 for data, and click Execute

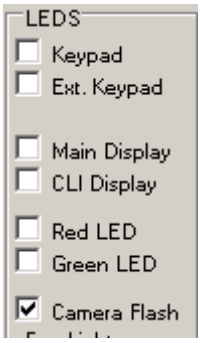


Verification

Verify that the response data returned 00.

Camera Flash Check

Select Camera Flash to enable. De-select Camera Flash to disable.



Verification

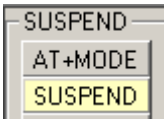
Verify that Camera Flash LED activates.

Bluetooth Tests

Use the following procedures to verify functionality of the Bluetooth device integrated in the phone.

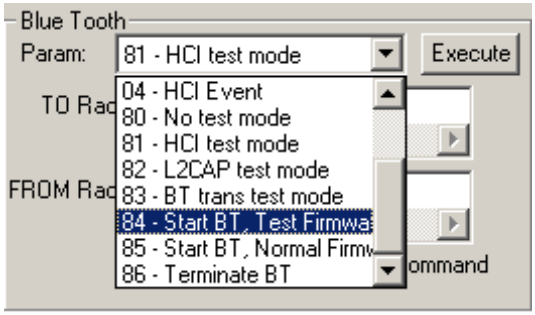
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)

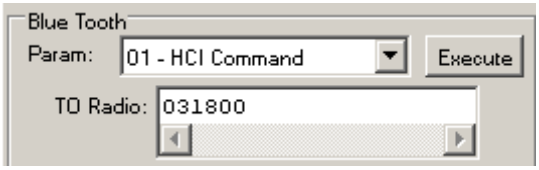


Bluetooth Host and Wake Test

Under Bluetooth, select parameter 86 and click execute, then select 84 and click execute, then select 81 and click execute.

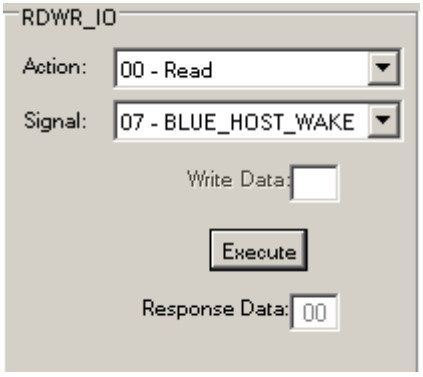


Under Bluetooth, select parameter 01 and enter 031800 in the "TO Radio" field. Click Execute.



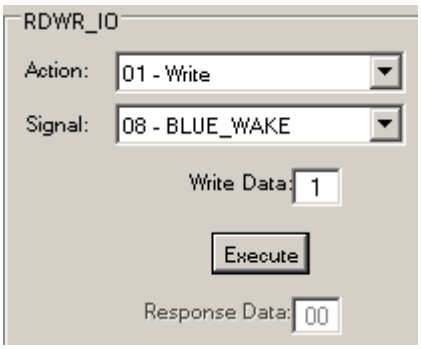
Verification

Under RDWR_IO Select "Read" for Action and "BLUE_HOST_WAKE" for Signal. Click Execute.



Verify that Response data is 00.

Now Select "Write" for Action and "BLUE_HOST" for Signal. Enter "1" for Write Data and click Execute.

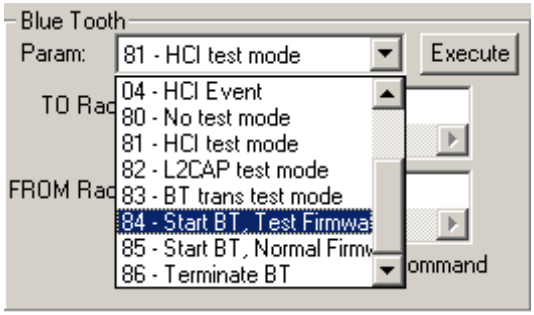


Repeat Reading BLUE_HOST_WAKE.

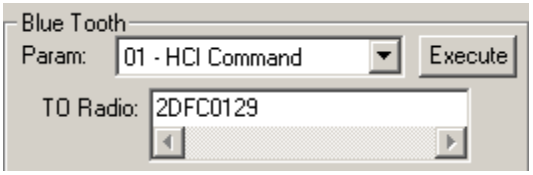
Verify that Response Data is 01

Unmodulated CW TX test

Under Bluetooth, select parameter 84 and click execute, then select 81 and click execute.



Under Bluetooth, select parameter 01, enter the indicated data in the “TO Radio” field.
0AFC0403005500, click Execute
30FC0102, click Execute
2DFC0129, click Execute



Verification

Verify that a 2441MHz signal is present. If the phone is closed, use a RF probe to sniff the strongest signal around near the accessory connector. Signal level should read approximately -10 dBm, ±15 dB.

Theory of Operation

E1000 Overview

The E1000 is a 3G (3rd generation) device that will deliver on the "promise" of 3G by providing high speed network access and rich multimedia content all in a superior voice-centric unit. A video camera and Assisted GPS provide additional value by offering unique business and entertainment solutions.

As a 3G product, the E1000 complies with all key specifications as defined by the 3GPP. Key product features are:

- UMTS: WCDMA 2100, GSM 900/1800 and 1900-MHz Tri-band technology,
- GPRS High speed packet data (64kbps UL, 384 kbps DL)
- 320 x 240 TFT Active Color, 260K colors
- 24MB Integrated Flash Memory, expandable to 256MB with Trans-flash memory.
- Integrated Bluetooth
- MP3 Player
- Enhanced Multimedia Capability (Audio/Video, Games, MMS)
- Unique 5-way Navigation Key
- New graphical user interface
- Enhanced internet browser (XHTML)
- Full Personal Information Manager (PIM) with SyncML Synchronization (OTA, Desktop)
- Integrated Camera 1.2 Mega pixel and GPS
- Voice Recognition Driven Dialing and Menu Shortcuts
- Voice Note Voice Recorder
- Polyphonic Speakerphone
- Programmable (J2ME)
- iTAP™ Predictive Text Entry
- Integrated Stereo Headset Jack

Video Camera Features:

- JPEG Image Capture @ VGA Resolution
- MPEG4 Video Capture @ QCIF Resolution
- Streaming Video
- Tightly Coupled, Ergonomic Design
- Initial User Applications:
- Sending captured Video Clips and Pictures through MMS, Email, or Internet channels
- Simultaneous Voice/Data – Take a picture or

Figure 3-1. E1000 Transceiver

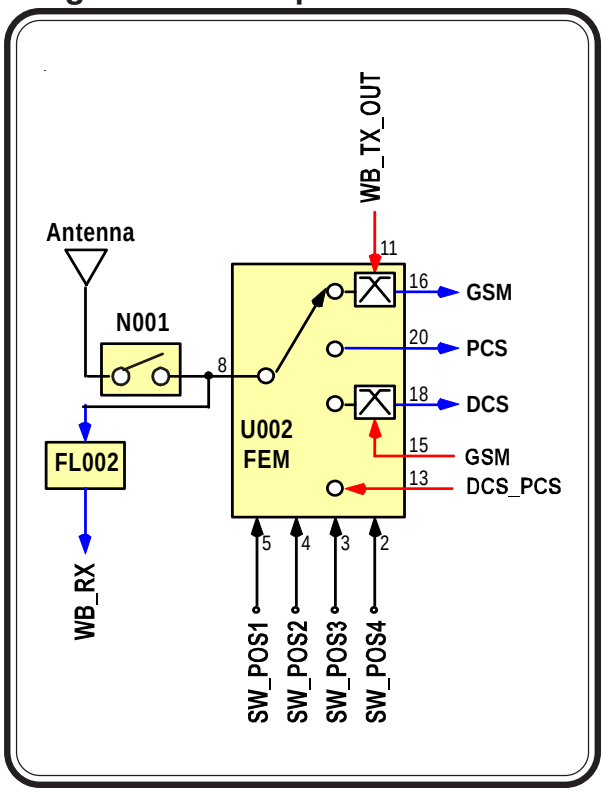
video clip and send while you're on the phone
- Video Conferencing (2-Way Video Telephony)

Location (AGPS) Applications:
- Get to specific location, with appropriate choices of destinations and routes and
- guidance to destination
- Identify local places of interest for hotels, taxi companies, restaurants,
- theatres, sightseeing, and shopping
- Receive information through alerts or display on map ahead of traffic
- congestion.
- Receive roadside assistance, with rescue service network and location information from the cellular network used to complement any information the pedestrian/driver is able to separately give.
- E911 Services: When roaming on a 2-2.5G GSM E-OTD-enabled network the mobile phone will respond to a request for location when making an emergency call.
- Push, Tracking & B2B Applications such as corporate tracking, routing, fleet management, and Buddy tracking (alert)

Front End Module

GSM receive signals from the antenna are fed into the FEM (Front End Module) through an antenna matching network and RF connector (N001). The WCDMA receive signal is directly tapped into the antenna matching network. This WCDMA receive configuration allows the mobile transceiver to receive WCDMA and GSM signals simultaneously, facilitating the ability to handover from a GSM network to UMTS network and vise-versa.

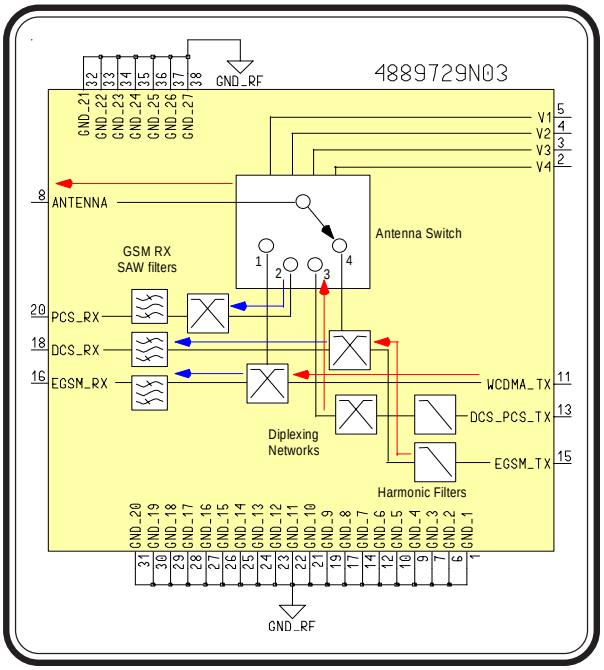
Figure 3-2. RF Top



WCDMA and GSM (all bands) transmit signals are passed through the FEM and fed into the antenna for transmission. If N001 is used, all WCDMA and GSM signals are fed into N001. Also, the internal antenna path will be in an open state when N001 is used.

The FEM integrates a 4-position GaAs antenna switch, diplexers, transmit harmonic filters, SAW filters and matching components on a multilayer low-temperature cofired ceramic (LTCC) module. The module provides band selection and filtering between the EGSM, DCS, PCS, and WCDMA (UMTS) receive and transmit bands in the 3G terminal.

Figure 3-3. FEM Module (U002)



There is a network on each port of the antenna switch that serves several functions. The primary function is to make each switch path behave as an open circuit to incoming signals in the WCDMA receive band (2110 – 2170 MHz). Signals in the WCDMA Rx band are thereby reflected back to the WCDMA receiver. Received signals in the EGSM, DCS or PCS bands are allowed to pass through the switch and undergo some pre-filtering, then pass through SAW filters before leaving the module.

Signals from the WCDMA transmitter are diplexed with EGSM Rx, sharing switch position 1. Similarly, signals from the EGSM transmitter are diplexed with DCS Rx, sharing switch position 4. Switch position 3 is used solely by the DCS/PCS transmitter, and switch position 2 is used only by PCS Rx.

Band Selection in the Front End Module follows the Truth Table shown in table 3-1.

Table 3-1. FEM Truth Table

Band Selected	V1	V2	V3	V4
WCDMA Rx	x	x	x	x
WCDMA Tx, EGSM Rx	1	0	0	0
PCS Rx	0	1	0	0
DCS/PCS Tx	0	0	1	0
EGSM Tx, DCS Rx	0	0	0	1

WCDMA Rx is available in any switch position.
Logic “1” is defined as 2.5 volts minimum.
Logic “0” is defined as 0 volts.

After the FEM, the EGSM or DCS receive signal is fed into one of the two transformers for differential conversion. For PCS, the receive signal leaving the FEM is fed into a high rejection band pass filter (FL005), which allows PCS RX and WCDMA TX/RX signals to pass. The WCDMA RX signal is then fed into an adjustable gain LNA (U001).

U001 operates in two gain modes selectable by MBC_EN2. The nominal gain expected while in high gain mode is ~16dB. During high input signal levels of ~–40dBm or stronger, the LNA will be in low gain mode. Currently, signal levels below ~–55dBm would trigger the high gain mode.

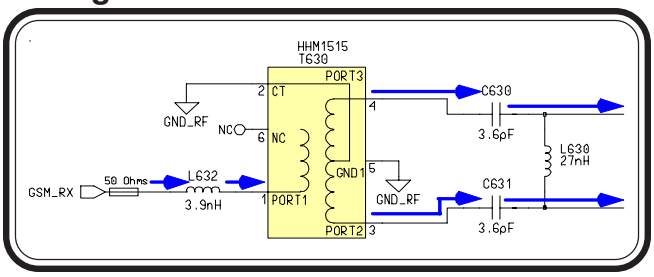
FL004 is a digital filter which is used to pass PCS receive signals to a transformer, for differential conversion, located in the GSM circuit. WCDMA receive signal is passed to the WCDMA circuit.

RF GSM Receiver

BALUN

From the FEM, the GSM singled-end, unbalanced received signals are fed into the Algae MB IC. Since the Algae MB IC expects a balanced differential receive input signal, the EGSM, PCS, and DCS signals must first pass through a differential conversion. Balun transformers provide the conversions from an unbalanced to a balanced line condition.

Figure 3-4. Balun Transformer

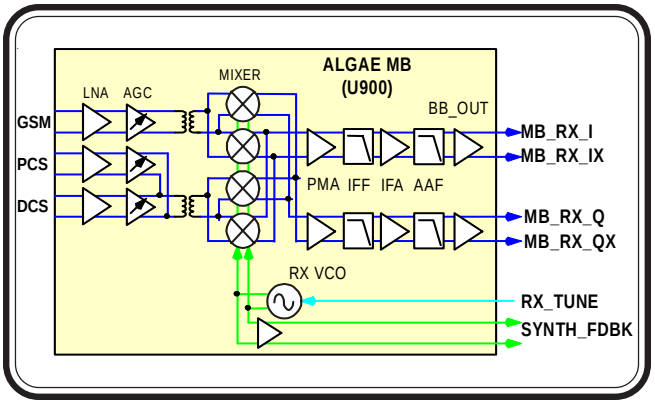


Each GSM band will contain a Balun transformer for differential conversions. The expected insertion loss for the Balun transformer is approximately 0.6 dBm.

BLUE MODULE IC (ALGAE)

Three LNAs are used for each receiver frequency band. Two hi-band LNAs are used for DCS and PCS frequencies and one low-band LNA is used for EGSM. Both hi-band LNAs are grouped together to share the same impedance matching transformer at the output. The low-band EGSM LNAs uses a separate impedance matching transformer at the the output.

Figure 3-5. ALGAE MB (Receiver)



Automatic gain control is provided by an AGC current steering differential pair. This current steering stage diverts current from the LNA load to supply in order to reduce the gain. The current steering differential pair alone would not have the desired transfer function, therefore an AGC linearizer is needed to provide a response that is linear in dB/V.

The LNAs drive AGC current steering stages that feed integrated transformer matching networks. The transformer drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q.

The downmixer converts the RF signal to baseband so that the signal can pass through a low-pass antialiasing filter and be converted to a digital format.

The output of the mixer connects directly to the post-

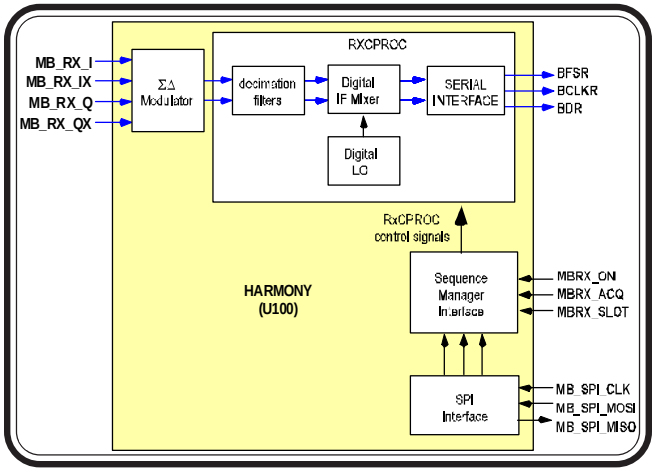
mixer amplifier. Large integrated capacitors are used to provide a low-frequency, low-pass corner at the output of the mixer. The signal then passes through baseband amplification and anti-aliasing filtering. The output of ALGAE MB will be balanced RXI and RXQ signal. It will have a 100kHz Very Low Intermediate Frequency (VLIF) signal that will be sent to the Harmony for Analog to digital conversion.

The LO signal is provided by a fully integrated VCO that drives either a divide-by-two or divide-by-four quadrature generator. In addition, a divide-by-3or5 circuit is used to feed back the LO signal to the synthesizer. The divide-by-3or5 circuit drives a differential output stage that provides the appropriate power level to the synthesizer. This output stage is shared with the TX path and provides the synthesizer feedback signal in both transmit and receive.

HARMONY GSM_RX (U100)

The RXI and RXQ VLIF signal entering the Harmony is sent to the Sigma-Delta modulator which transforms the slow moving analog signal into a high speed digital output. The Sigma-Delta modulator is set as an Analog-to-Digital Converter (ADC). The output of the Sigma-Delta modulator is then fed into the Receive Coprocessor (RxCPROC).

Figure 3-6. Harmony (GSM RX)



The RxCPROC includes the digital signal processing hardware required for the receive transceiver (Rx) after the initial conversion done by the sigma-delta modulator. It's configured to be used in the very low intermediate frequency mode (VLIF). The RxCPROC supports the GSM and EDGE standards.

The RxCPROC is represented by blocks listed as "decimation filters", "digital IF mixer", "digital LO" and "serial interface". The RxCPROC decimates and filters the I and Q quadrature input signals and converts them to baseband. Processed signals are sent serially to the Base Band Port (BBP) to be further handled by the DSP and VIAC.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data to the BBP module in the POG. SDFS is a framing signal which marks the beginning of an I,Q transfer. SDRX is the serial data. The clock used for the serial transfer is SCLK.

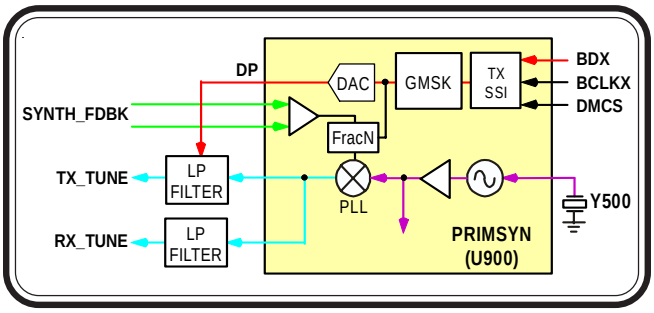
The RxCPROC is controlled via the SEQUENCE MANGER or SPI. Each control line of the Seq. Manager can be overridden by a corresponding line from the SPI (MB_SPI_CLK, MB_SPI_MOSI). Layer One timer signals (MB_RX_ON, MBRX_ACQ, MBRX_SLOT) from POG control the start of major sequences of events.

RF GSM Transmitter

BLUE MODULE IC (PRIMSYN GSM_TX)

The PRIMSYN receives SSI TX data at *DMCS* (digital input to start Tx modulation), *TXCLK* (clock for serial transfer) and *SDTX* (serial Tx data) from POG. This data pattern input to a fractional N synthesizer with a 24-bit resolution. For EGSM the synthesizer output is 880 – 915MHz, DCS is 1710 – 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

Figure 3-7. PRIMSYN (GSM TX)

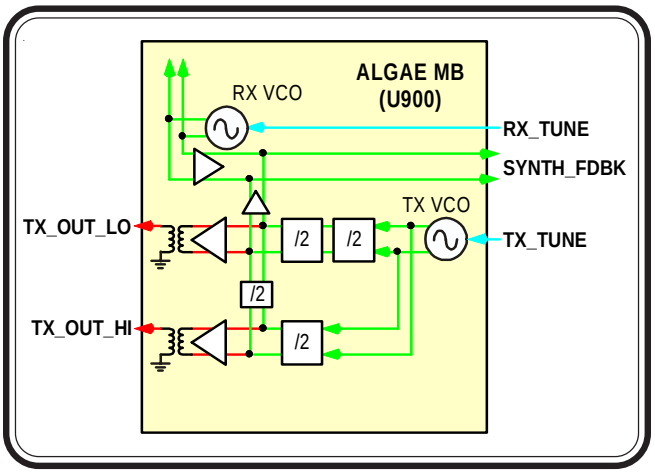


BLUE MODULE (ALGAE)

TRANSMIT SECTION

An integrated VCO is used for the transmit path. A single VCO is used for transmit. A low noise floor divide-by-2 stage drives the high band output. The low band output is driven by a divide-by-4 stage.

Figure 3-8. ALGAE MB (Transceiver)



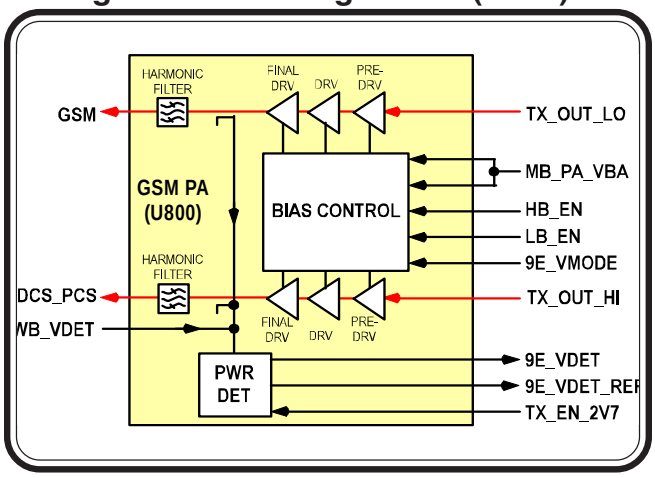
Two transmit output stages are provided. Both stages have integrated output matches in order to reduce the required number of discrete components. The integrated matches are implemented as differential to single-ended transformers.

The transmit signal is fed back to the synthesizer through a differential output stage that is shared with the receiver.

GSM PA (U800)

The TX VCO output signal from the ALGAE MB is injected in the Durango 9E3G via the TX_OUT_LO (Low Band) and TX_OUT_HI (Hi Band). Durango

Figure 3-9. Durango 9E3G (U800)



9E3G is a quad band PA Module for GSM applications in 3G phones. The module uses a dual amplifier lineup which operates in the three separate EGSM, DCS1800, and PCS1900 bands. It is compatible with GSM/GPRS operating modes. The integrated module incorporates coupler/detector for power control, Low pass filtering for harmonic rejection, and is internally input and output matched to 50 ohms.

This Transmit module is to be used as the final amplification stages in the A1000 for the EGSM (900 MHz), DCS (1800 MHz) and PCS (1900 MHz).

The nominal expected maximum gain is ~30dB.

The *VDET* (output) is the RF feedback along the DC reference *V_REF_DET* (output) are used in backend PA Control (PAC) processing by the HARMONY.

VBA_1 and VBA_2 are inputs from HARMONY that controls the PA output level. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases.

The power detector is internal to the PA and is shared among all GSM bands as well as WCDMA. WB_VDET connects WCDMA TX to the power detector

HB_EN enables the high band (DCS/PCS) amplifier lineup. LB_EN enables the low band (EGSM) amplifier lineup. TX_EN_2V7 enables the detector.

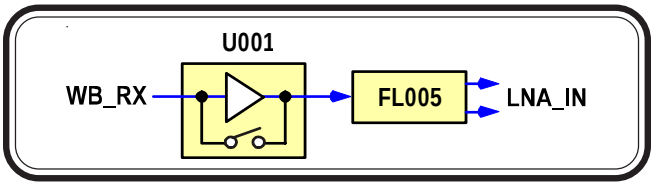
9E_VMODE sets the operating mode of the PA. GMSK and EDGE modes are supported, but only GMSK mode is used in this design. 9E_VMODE is set high during GMSK TX mode. 9E-VMODE is set low when the transmitter is in standby mode. This line is also enabled in WCDMA mode to allow proper WCDMA power detection.

RF WCDMA Receiver

MC13820 (U30)

The first IC in the WCDMA Rx line up is U30 (MC13820), which is a Low Noise Amplifier. The RX frequency will be amplified and passed on to OneLife WB through FL300. The LNA is controlled by Harmony (U100) through two enable lines. MBC_EN1 enables gain for the LNA while MBC_EN2 enables the IC. Both lines can be probed at testpoints located near Harmony (TP120 and TP121). U30 operates from the PCAP supply voltage *VRF_RX_2_775*

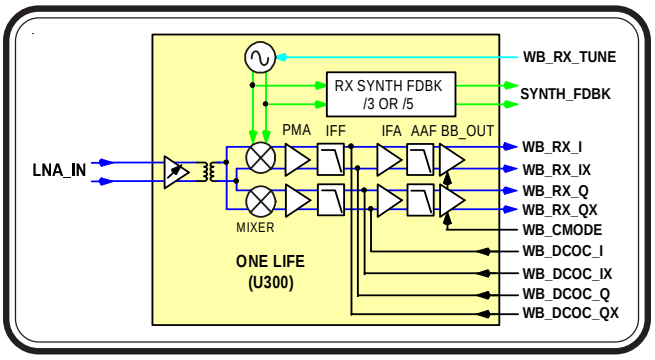
Figure 3-10. WCDMA LNA



BLUE MODULE (ONELife)

ONELife is a full custom mixed signal BiCMOS IC with the SiGe option with electroplated copper inductors. This IC is a fully differential direct-conversion front-end IC and is comprised of a multiband RF section and a single path baseband section. The RF section is comprised of three Low Noise Amplifiers, two sets of quadrature mixers and an integrated 4GHz VCO with a divided prescaler output. Only one LNA is used in this design to cover the WCDMA/UMTS band (2110-1710). The LNA has two gain states; a high gain state and a bypass state with no reverse isolation. The LNA drives the quadrature mixers, via an integrated transformer matching network, that convert the RF signal to baseband, quadrature I and Q. The LO signal is provided by fully integrated VCOs that drives a divide-by-two quadrature generator. In addition, a divide-by-three/five circuit is used to feed back the LO signal to the synthesizer via an open collector output stage.

Figure 3-11. ONELife



The baseband section is comprised of two separate I and Q paths each containing a PMA, an anti-aliasing filter made up of an IFA with an active pole and DCOC, two bi-quad sections, and an output buffer. The baseband signal path has six poles of baseband filtering distributed between mixer pole, the active IFA pole, and the two bi-quad blocks. The PMA has pseudo-continuous gain capability and is part of the AGC system along with the LNAs. The PMA AGC is controlled through five dedicated IC pins. At the output of the PMA stage, a baseband detector circuit provides broadband, strong signal information to the baseband part. DC Offset correction is provided through external differential pins to provide offset corrections to the internal IFA stage. The output buffer receives an input voltage via feedback from the Harmony WB_CMODE line so that OneLifeWB's output signal drives the A/D with the correct common mode voltage.

Control and programming are done through a SPI interface from Harmony. Two supplies are required to power the IC, VRF_DIG_1.875V for SPI lines and VRF_2.775V for RF portions.

Harmony WCDMA_RX (U100)

The RX I an Q baseband signals are fed into the Sigma-Delta modulator of the Harmony. The Sigma-Delta modulator is an A/D converter that converts the I and Q baseband inputs to noise shaped 6-bit digital outputs. These outputs are then next decimated by a ratio of 3 using 3-stage cascaded comb type filters to a sampling rate of 15.36 MHz.

DC offset correction is performed next immediately to minimize the amount of delay in this mixed mode control loop to achieve rapid DC acquisition during *normal mode warmup sequences*. The DC offset correction unit has feedback to the OneLife-WB IC to be able to correct for DC offsets at the inputs to IF amplifier stage.

The matched selectivity filter is designed such that it provides the desired selectivity to meet adjacent channel and blocker specifications in the 2100 and 1800 MHz frequency bands.

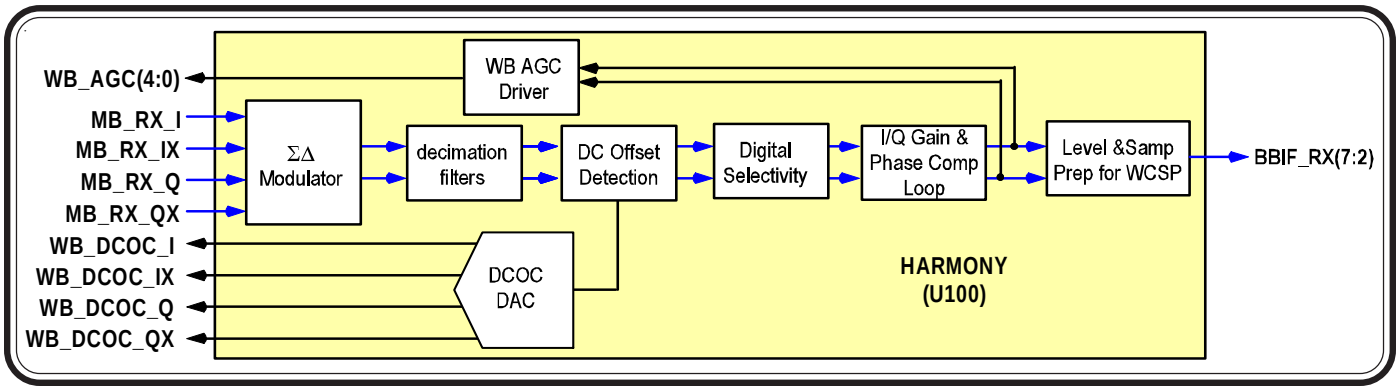
I/Q gain and phase imbalance equalization units located next in the lineup is used to correct for I/Q mismatches due to both the base station transmitter as well as the mobile device.

Next, the outputs of the I/Q gain equalization unit feed into the RF/IF AGC as well as the digital gain compensation control units. These outputs from the I/Q gain equalizer are used by the AGC unit for on-channel power detection. In addition, the AGC unit also receives off-channel power indication from a 2-bit SOS detector data bus from OneLife-WB IC. The on-channel and off-channel power levels are used by the RF/IF AGC unit to control internal and external LNA step attenuator stages as well as the variable gain PMA stage in OneLife-WB IC.

Two bit control lines are used to control each of the external LNA step attenuator stages. Alternately, a 1-bit control line is employed to control the internal LNA in the OneLife IC. In addition, a 5-bit parallel digital bus is employed to control the PMA variable gain control stage in OneLife-WB IC. The AGC unit also supplies the detected RSSI level to the external host device (e.g. POG IC) based upon the current RF, IF, and digital baseband gain control settings as well as the on-channel RSSI detected.

Following the I/Q gain equalization stage, a digital gain compensation unit is located next. The purpose of this gain compensation unit is to provide a 6-bit gain compensated output signal to the WCSP unit given that the input signal's dynamic range is 13 bits. The 15.36 MHz rate I and Q outputs are then interleaved in the BBIF (baseband interface) unit to generate the output I/Q data at a 30.72 MHz rate on a single 6-bit data bus to the external host device.

Figure 3-12. Harmony WCDMA RX (U100)



RF WCDMA Transmitter

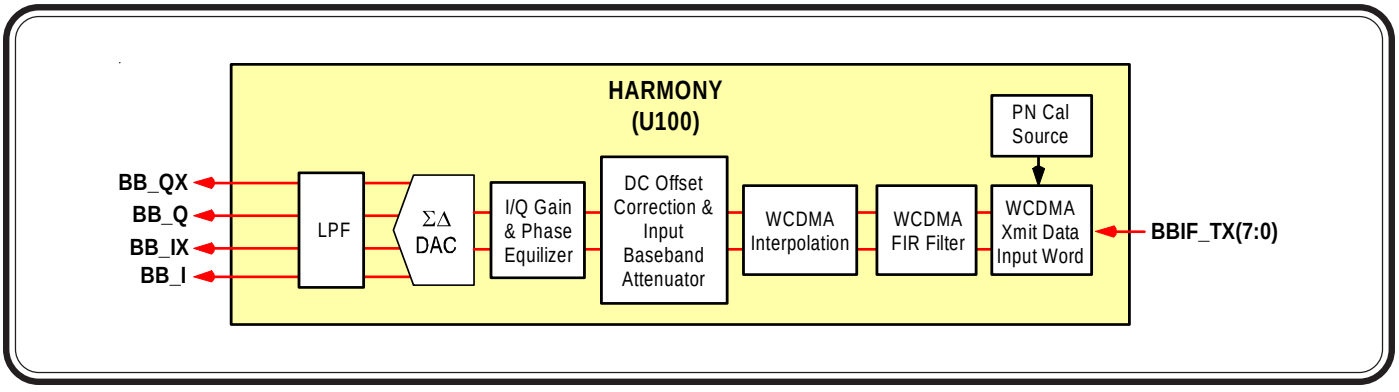
Harmony WCDMA TX (U100)

The Harmony provides pulse shaping and modulation of the 8-bit interleaved TX data coming from the POG. RF carrier suppression and baseband DC offset, I/Q gain and phase equilization will be then be performed. Finally, the I/Q signal is passed through a DAC and fed into the Rattler IC.

An 8-bit parallel interleaved data interface (BBIF_TX) is used to load the I and Q chip data from POG into the WCDMA signal path. Alternately, a PN calibration signal may also be loaded into this signal path for correction of baseband DC offsets and I/Q imbalances during transmitter warmup sequences. The parallel I and Q data from POG is first pulse shaped at a 7.68 MHz sampling rate using 31-tap SRRC FIR filters for the I and Q channels. These filters' outputs are then interpolated to a 30.72 MHz sampling rate using two stages of halfband interpolation filters.

The 12-bit outputs from the baseband pulse shaping and modulation system are fed into this DC and I/Q correction system. The specified 12 bit inputs first pass through the DC offset, I/Q phase and gain equalization blocks. The output samples from the gain equalizer are then fed into the sigma delta DACs at a higher sampling rate to minimize anti-aliasing filtering requirements. Following the DACs, there is an analog gain stage with 5 attenuation settings available for the baseband gain control system. Following this stage, a 2-pole passive filter and a 4th order Butterworth filter is employed in the quadrature signal path to eliminate the shaped noise from the sigma delta D/A's. The outputs of these reconstruction filters feed into the RF modulator IC (Rattler).

Figure 3-13. Harmony WCDMA TX (U100)



MC13786 (U200)

The MC13786 is an integrated I/Q modulator, IF and RF variable gain amplifier, UHF frequency synthesizer with a fully integrated VCO, image-reject upconverter mixer, and linear PA driver.

The synthesizer or phase locked loop (PLL) consists of a buffer amplifier, multi-modulus prescaler (divide by 4, 5, 6, and 7), a sixbit programmable post divider, reference divider, phase detector, and charge pump. The PLL uses a reference frequency of 15.36 MHz. One frequency synthesizer/VCO provides both the main and offset LO functions. The VCO operates over a frequency range of 2114 MHz to 2263 MHz and is fully integrated.

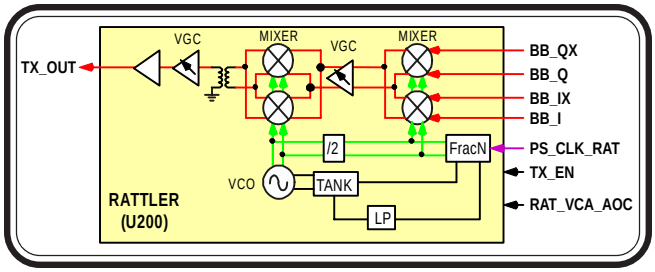
The I/Q Modulator consists of a quadrature generator and two Gilbert Cell active mixers. Using the offset LO and quadrature generator, the active mixers modulate the differential baseband I/Q signals onto a TXIF signal. Depending on the channel selection, the TXIF frequency will range from 274 MHz to 283 MHz.

From the active mixers, the TXIF signal is fed into a IF Variable Gain Amplified (IF VGA). The IF VGA has 70 dB of total typical gain control range and is controlled by the VGC line. The output of the VGA shall have a single pole bandpass tank circuit to provide attenuation to far-out noise.

The upconverter has an image-reject configuration so that the unwanted sideband is rejected to decrease the linearity requirements of the VGA stage. An input polyphase filter shall provide the necessary phase shift for the IR mixer. The TXIF signal is upconverted to a TX carrier frequency ranging from 1920MHz to 1980MHz. An on-chip copper balun shall provide the differential to single ended conversion necessary for the following stages.

The VGA provides a reduction in gain and current to optimize the TX lineup for lower output power levels. The PA driver amplifies the signal to provide sufficient drive for the radio power amplifier.

Figure 3-14. Rattler (U200)

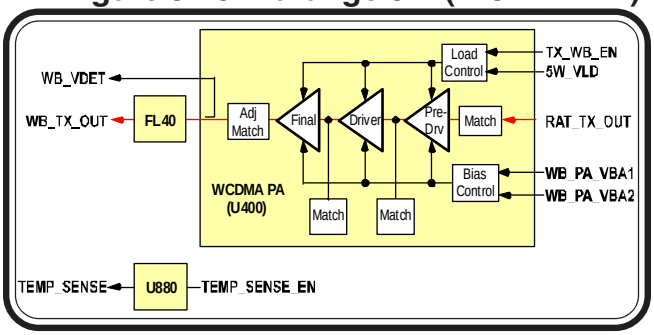


WCDMA PA (U400)

Durango5W is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 – 1980MHz. The nominal expected maximum gain is ~30dB.

A Motorola proprietary high power / low power efficiency enhancement load switch (5W_VLD) is included in the output match. VLD adjusts the output load for optimum efficiency from low power to high power out.

Figure 3-15. Durango 5W (WCDMA PA)



In conjunction with VLD, bias control (WB_PA_VBA1/WB_PA_VBA2) is performed between high and low power ranges.

The amplified WCDMA carrier is fed into a RF coupler device which has an integrated RF detector. An RF detect will pass through the Durango 9E3G (GSM PA) before being fed to the Harmony for power detection.

U880 is used to measure temperature. Its linear output is a voltage signal that corresponds to its physical device temperature. TEMP_SENSE is measured by PCAP and the MCU (POG) retreives the temperature readings every 5 seconds and passes it to the DSP (POG) so that the temperature compensation tables are updated.

The isolator provides a stable 50 ohm PA load. It also protects the PA from interfering with other frequency bands. Finally, it guards against IM products being produced by the transmitter and affecting receiver circuits.

RF Interface

Harmony

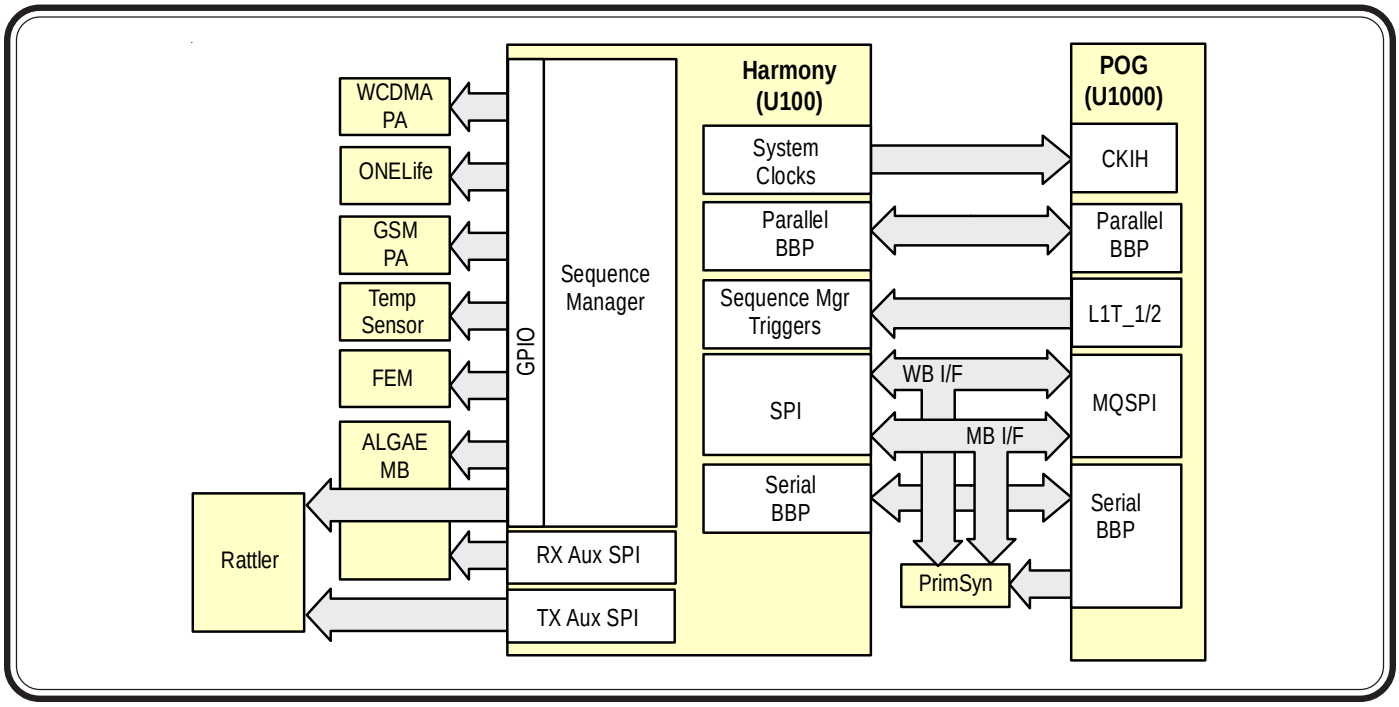
The Harmony IC is a mixed-signal transceiver backend IC intended to support GSM, EDGE and WCDMA services. It includes 2 receive paths: a medium-band path and a wideband path. The medium-band path is intended for GSM and EDGE and is configured to support VLIF receiver architecture. The wideband path is intended for WCDMA and is designed to operate in a direct conversion receiver architecture. Both of these receive signal paths are optimized for non-compressed mode. The transmitter path is designed to operate in a direct-launch transmitter architecture. The IC also includes dual clock synthesizers, as well as general support circuit such as sequence manager and SPI.

The Harmony IC and Base-Band (POG) IC interface consists of two independent sets of SPI lines (WB I/F, MB I/F); 2 chip-enable inputs, 2 clock inputs, 2 data inputs, and 2 data outputs. Harmony interfaces to the Base-band IC as a slave IC, however, it is also a master to two auxiliary ICs (Algae MB and Rattler) using two independent sets of SPI lines (TX AUX, RX AUX). The two auxiliary ICs are programmed by the Base-Band via Harmony.

In order to decrease the overall area required for controlling the sequences, a sequential access strategy was developed. The sequence manager would consist of controllers that would access an SRAM device sequentially. These controllers run of a set of programs that are pre loaded in to an SRAM memory device. In order to eliminate the need for a stack and interrupts each controller is dedicated to a single task. In the sequence manager there exists a controller per task, where the number of maximum tasks would be equivalent to the number of input TIMER lines.

A serial bus consisting of SDFS and SDRX will transmit the GSM RXI and RXQ data in 2's complement format to the Serial BBP module. The RXI and RXQ data will then be handled by the DSP integrated in the

Figure 3-16. RF Interface Block Diagram



POG. The Serial BBP module for TX is not used in this design.

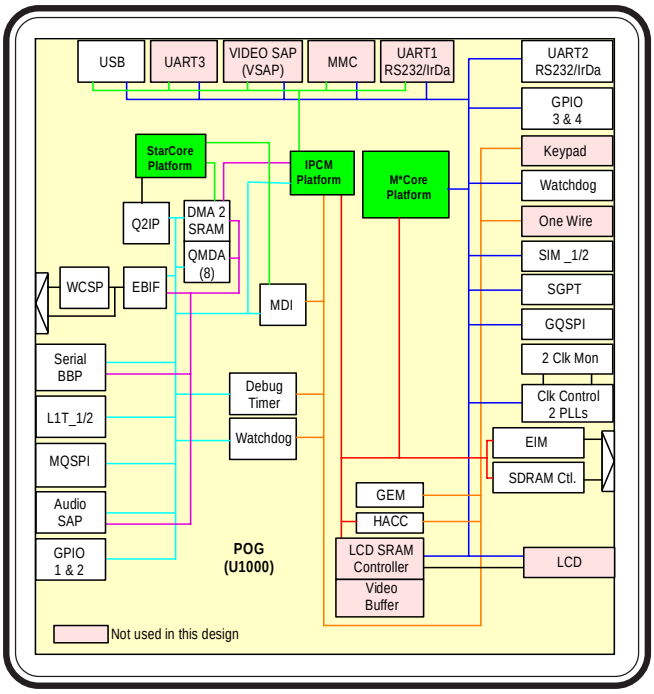
The WCDMA path receive path has a parallel BBP interface to send data to the Base Band processor. The interface is programmed to run at 15.36mhz. An 8-bit parallel interleaved data interface (Parallel BBP) is used to load the TX I and Q chip data from the external host processor (POG) IC into the WCDMA signal path of Harmony.

Baseband Electrical (Digital)

POG (U1000)

POG is the baseband processor IC of the 3G chipset solution. POG is crafted to provide a high performance embedded solution at low power for 3G mobile devices. POG is a TriCore processor IC integrating a powerful DSP core, a 32bit MCU RISC core with unified cache and a custom 32bit RISC engine for data movement across the processing domains.

Figure 3-18. POG Block Diagram



The DSP core is a high performance StarCore with four parallel ALUs, the SC140, with a novel Variable Length Execution Set (VLES) architecture which maximizes the execution of multiple instructions in a single clock cycle. The SC140 is assisted by 3G specific hardware accelerators and timers to optimize performance and power. As part of the 3G support, the Wideband CDMA Signal Processor (WCSP) module implements modem functions required by the CDMA subscriber unit in accordance with the 3GPP specifications.

The 32bit MCU RISC core is the M*Core M341 designed for high performance and low power embedded systems. The M341 embodies an 16K unified cache, integer multiplier and MMU in support of virtual memory management OSes.

Data communication across the cores is handled by a flexible 32bit RISC machine, the Inter Processor Communication Module (IPCM). The IPCM supports flexible data flow between the MCU, DSP and the multimedia peripherals.

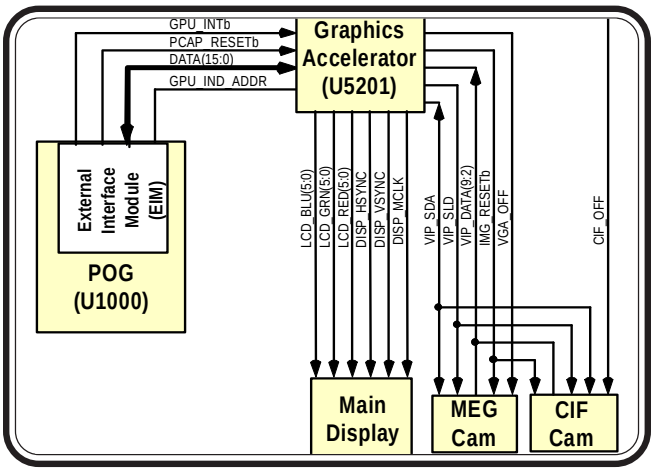
Due to the dual processor architecture design of A1000, some of the POG modules are not used. Functions of these unused modules are controlled by the OMAP application processor. The primary functions of POG will include,

- Colorado RF interface
- PCAP Audio interface
- SIM interface
- GPS GAM interface

Graphics Accelerator

U5201 is a high performance, low power, Graphics/ Media Processor IC (GPU) that supports advanced multimedia applications for W-CDMA, UMTS, and GSM. This IC enables the user to capture, view, and share high quality images and video. A hardware-based MPEG-4 encoder captures video at up to CIF resolution at 30fps. A hardware-based video decoder allows playback of the video recorded, or any other MPEG-4 clip or streaming video. A full hardware codec is utilized for video conferencing – QCIF image size at up to 30fps. Support of VGA (680x480) resolution LCD at

Figure 3-19. GPU Interface

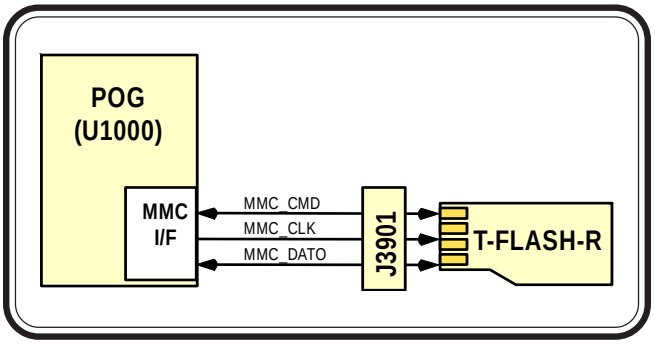


16 and 18-bpp (with dithering) using only an embedded frame buffer and up to 3MP cameras with resolutions up to 2048x1536 image capture with a 10fps preview and 2MP cameras with a 15fps preview. The video processing engine is coupled with a JPEG encoder capable of encoding still images with 3MP resolution and a JPEG decoder capable of playback motion JPEG at up to 30fps at VGA resolution. The host interface bus provides an 8, 16, or 32-bit asynchronous interface that supports both direct and indirect addressing modes.

MMC/SD Flash Interface

The MMC/SD host controller provides an interface between the OMAP and Triflash-R memory card.

Figure 3-20. MMC Interface

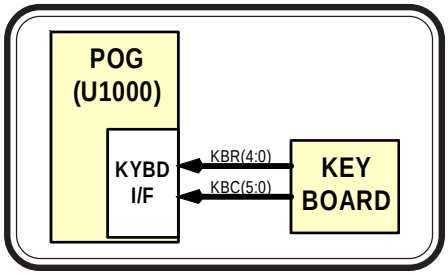


The MMC/SD host controller handles MMC/SD protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for syntactical correctness.

Keypad Interface

The keypad provides the primary physical user interface for the radio. The 5-way NAV joystick has a center keypress in addition to the four primary directions. White LED's will be used for backlighting. The keypad implementation to be used is the 2-contact, 1-pole keypad scanning architecture.

Figure 3-21. Keyboard Interface



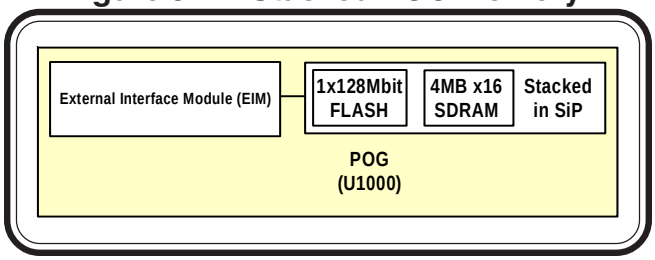
The Keypad Port (KPP) of POG decodes keypad presses. The Keypad Port is a 16-bit peripheral which is used for keypad matrix scanning. Keypad matrix uses 5 rows and 4 columns for key scanning. The KPP on POG can support up to an 8 x 8 row-by-column keypad matrix. The KPP will use a 32.768 KHz clock.

The Power/End key will not be part of the matrix but instead will connect directly to PCAP2.

POG Memory

The POG flash memory uses a 128 (128 Mbit) 1.8 Volt wireless memory which delivers high density flash memory in a single package. Individually erasable memory blocks are optimally sized for code and data storage. Four 16-Kword blocks and seven 64-Kword blocks are located in the parameter partition. The rest of the flash memory is divided into fifteen partitions of eight 64-Kword main blocks. By dividing the flash

Figure 3-22. Stacked POG Memory



memory into partitions, program or erase can take place simultaneously during read operations. The device is available in a 56-ball vfBGA* package with 0.75 mm ball pitch.

The POG SDRAM device is a JEDEC standard SDRAM with 1.8V core supply, 1.8V I/O supply, four banks, and density of 4Mb x 16 (64 Mb). It is low power with special function support including partial array self refresh and temperature compensated refresh. It has a max frequency of 104MHz with CAS latency of three.

Power Supply Architecture

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are illustrated below.

Table 3-1. Power Distribution 1

Physical name	Logical name(s)	Voltage	Supplies
SW1	VLVIO_1.875	1.875	BP Flash cores,
SW2	Not Used	1.725	
SW3	VBOOST_5.5V	5.5	V10, Keypad backlights
V1	V1	1.875	
V2	VA_2.775V	2.775	Audio
V3	Not Used	1.875	
V4	VPOG_VLVIO_1.875V	1.875	Low voltage I/O
V5	VHVIO_2.775	2.775	PCAP internal components
V6	VRF_TX_2.775V	2.775	Harmony, Rattler, RF TX
V7	VBLUETH_1.875	1.875	Bluetooth

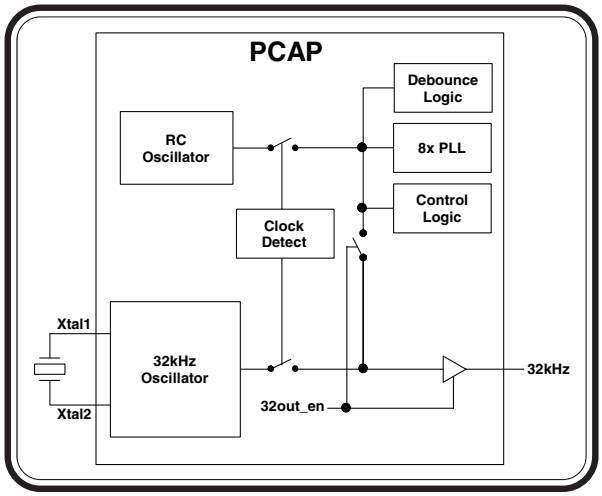
Table 3-2. Power Distribution 2

Physical name	Logical name(s)	Voltage	Supplies
V8	VMMC_2.775	2.775	MMC
V9	VRF_REF_2.475V	2.775	RF Reference
V10	VRF_HV_5V	5	RF HV
VAUX1	VGPS_2.775V	2.775	
VAUX2	VRF_RX_2.775V	2.775	Harmony, Algae, RF RX
VAUX3	VCAM_2.6	2.6	Transflash
VAUX4	Not Used	3	
U3206	VMAIN_1.55V	1.55	POG Core

Clock Generation

PCAP can generate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Rainbow requires for optimal performance, therefore, an external 32.768kHz crystal is used.

Figure 3-24. RTC Clock



The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Audio Circuits

PCAP (U3000)

The PCAP2 IC is an ASIC intended for use in Colorado platform mobile phones. It integrates several functional modules:

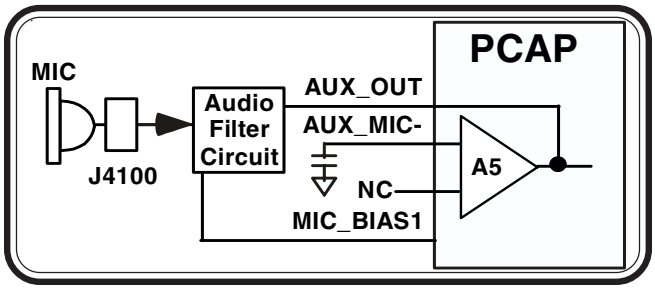
- Voltage regulators of both linear and switching types designed for use in the Colorado power scheme
- Audio codecs and amplifiers
- RS-232 and USB transceivers
- LED controllers for the service light and display/keypad backlights
- Digital interfaces for two controlling processors.

TX Audio

The A1000 supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single-ended with respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

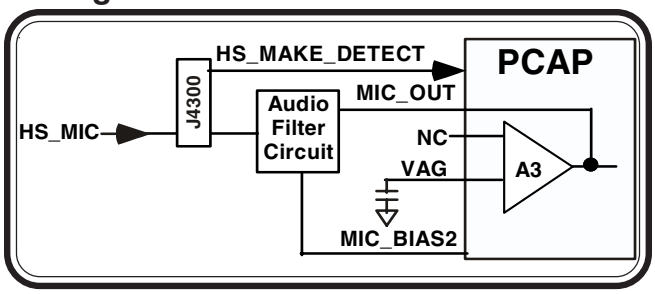
The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 and R4101 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R4102 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

Figure 3-25. Internal Mic Path



The headset microphone path is biased through R4396, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by using R4399 as a pull-up resistor and detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

Figure 3-26. Headset Mic Path



The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight/ALeft Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R34003 and R34002 respectively, and then connected to the transducer. Off the Speaker-path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

Figure 3-28. Handset Speaker Path

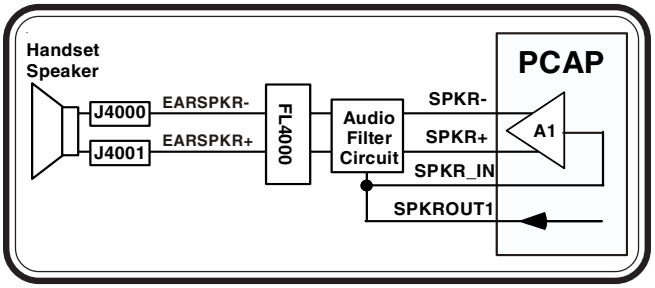
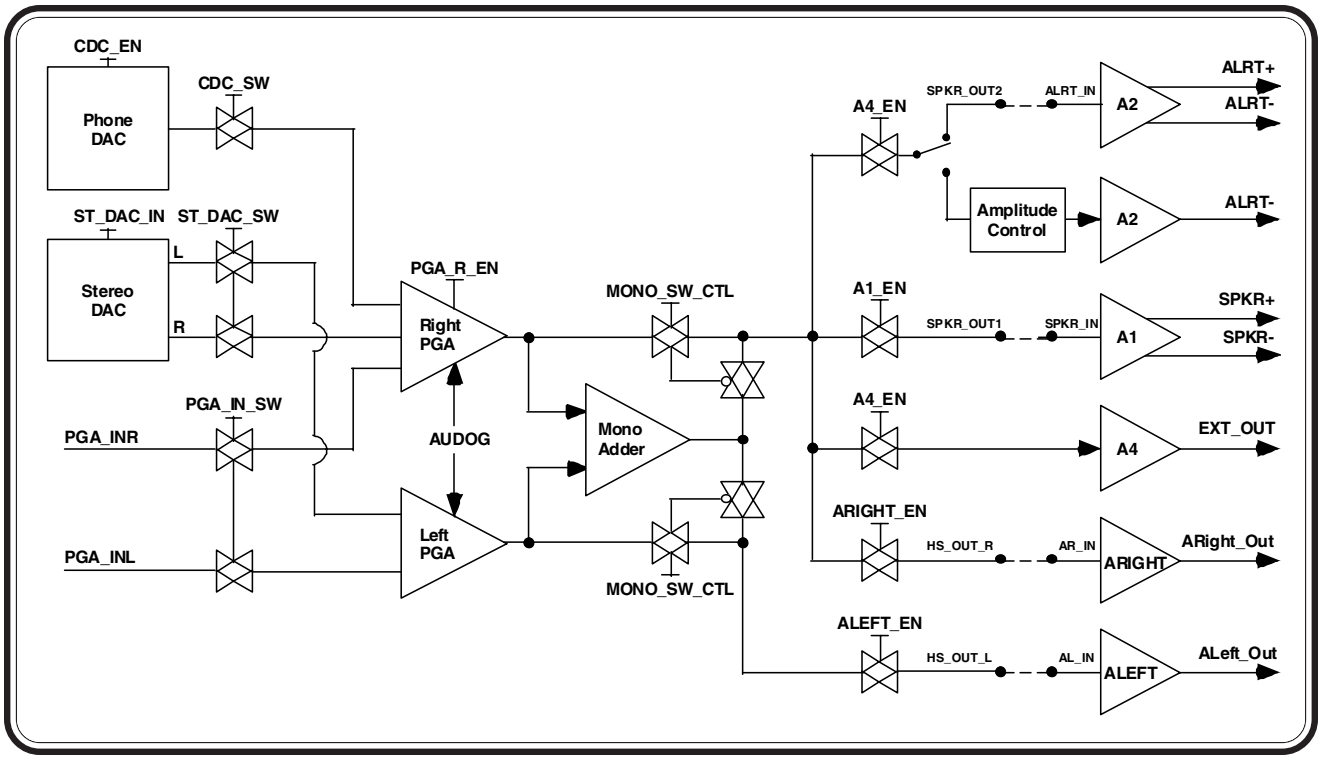
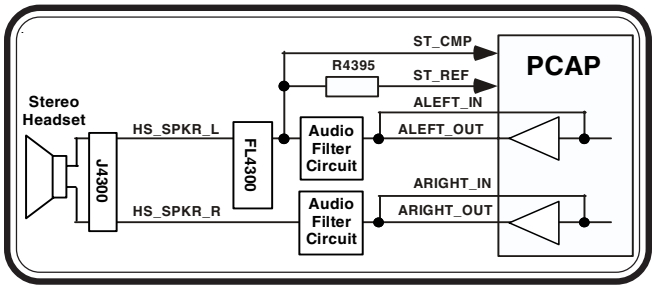


Figure 3-27. RX Audio Block



The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

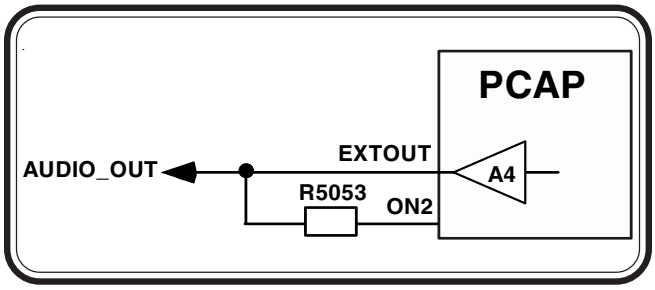
Figure 3-29. Headset Speaker Path



The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R34304 and C4306, R34303 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ARight_Out path, AL_IN is tapped off through C4354 for the inverting input of the audio amp ALEFT.

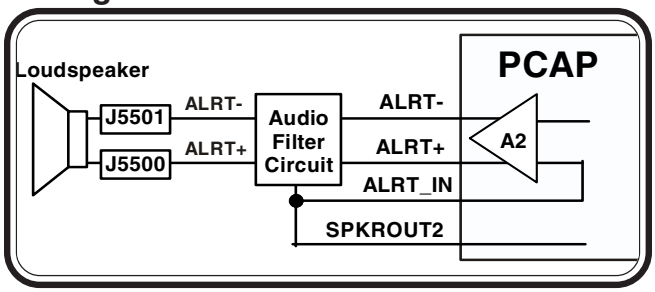
The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

Figure 3-30. External Speaker Path



The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

Figure 3-31. Alert Path



Battery Interface

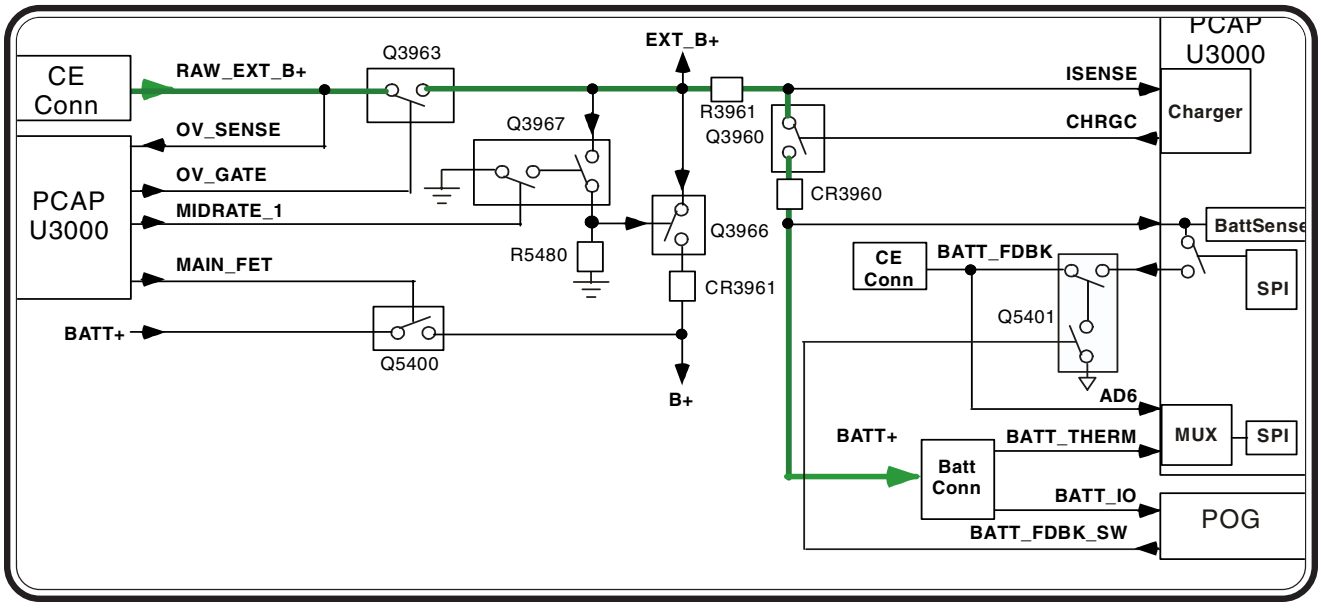
Batteries interface to the main transceiver board via a 4-pin connector (J5400). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q5400 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U3000) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J5000). During full rate charging, Q3966 is turned ON so that current can be supplied from the external source to B+. Q5400 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q3960. A sense resistor (R3961) provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J5000). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 3-32. Battery Interface Block

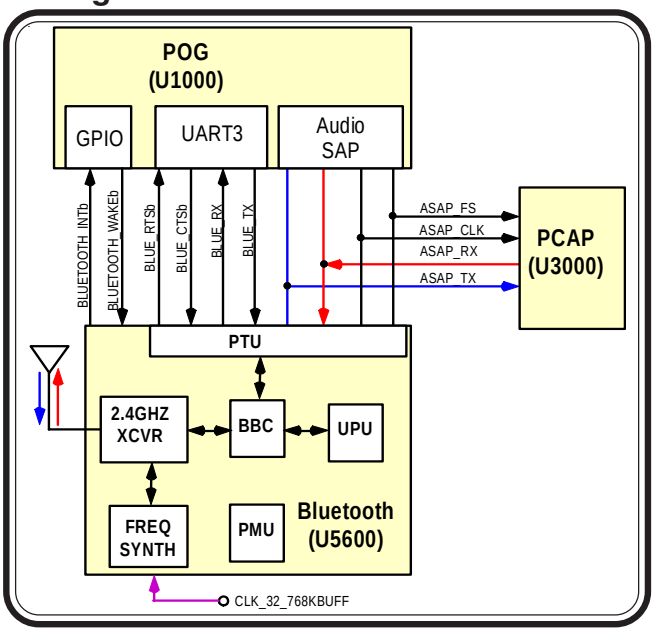


Bluetooth

The Broadcomm 2033 Single Chip Bluetooth solution is being used with the A1000. The BMC2033 is a Bluetooth 1.1 compliant stand alone baseband processor with an integrated 2.4GHz transceiver. The baseband section controls all bluetooth functionality from the physical layers to the HCI layer. The radio section includes PLL, VCO, LNA, PA, upconverter, downconverter, modulator, demodulator, and channel select filtering.

The fractional- N synthesizer can support multiple reference frequencies, including 13MHz and 15.36MHz. The BCM2033 RS232 module interfaces the POG. The ASAP interface communicates between POG, PCAP, and BCM2033.

Figure 3-33. Bluetooth Block



AGPS

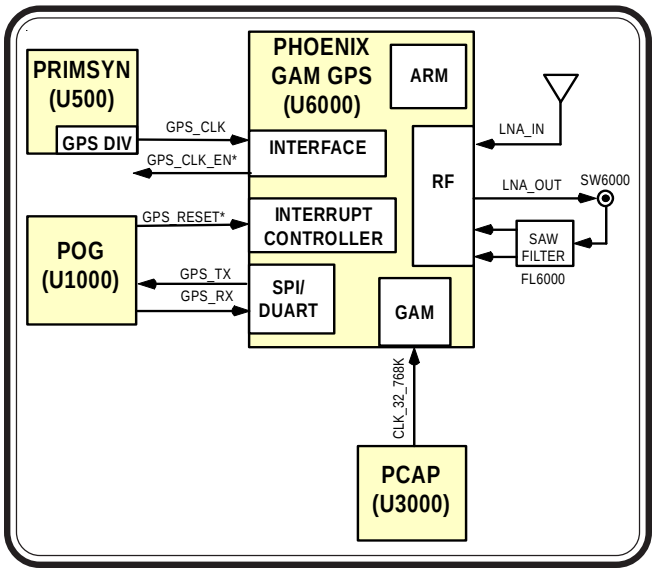
The GPS section is based on the Motorola MG4100 single chip GPS receiver 2M SRAM IC (Phoenix) along with One-Track firmware.

The main blocks of the MG4100 IC consist of the GPS Acquisition Module (GAM), a low IF front-end, an ARM7TDMI microprocessor module, a Boot ROM synthesized in gates, and several processor peripherals.

When Phoenix is configured to OneTrack mode, it will search, acquire, and track satellite signals; decode data without host intervention; calculate position, velocity, and time at a 1Hz rate and perform background data decode. It supports both Oneshot and autonmous (stand alone GPS receiver). In reacquisition mode if more than four satellites with signal strength of more than -140dBm are visible, Phoenix will decode satellite data and autonomously compute a position fix without any assistance. The Tim-To-First-Fix will be greatly reduced comparing to Oneshot.

The GPS external RF connector (SW6000) allows us-

Figure 3-34. GPS Block



ers to attach a pro install car kit or external GPS attenae. It provides power supply through the signal pin at 2.775V and 15mA current max.

The control signals for the Phoenix IC will be transported via the POG (U1000) 2-wire DUART interface (GPS_TX,GPS_RX).

A 26 MHz clock coming from the PrimSyn is used as a dedicated accurate input clock to acquire GPS fix at weak signal environment and faster TTFF. This clock is powered off when GAM does not require the clock. A RTC clock is used for low power operation.

GPS_CLK_EN signal is used to turn off external reference clock when Phoenix IC switches to CPU and low power mode. Conversely, the clock will be turned on when the software switches to full power mode.

Service Manual

Level 3

Draft 1.0

MOTOROLA

DIGITAL WIRELESS TELEPHONE

Model E1000

UMTS 2100MHz/PCS 1900MHz/DCS 1800MHz/GSM 900MHz

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Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the E1000 UMTS/GSM handset.

Table 4-1. Electrical Parts List - B5400 to C404

Reference Number	Part Number	Description
B5400	0988252L01	CONN_J
C001	0662057M01	RES, 0
C005	2113743N38	CAP, 33pF
C007	2113743L41	CAP, .01uF
C008	2113743N26	CAP, 10pF
C002DNP	2113743N02	CAP, 0.75pF
C003DNP	2104801Z10	CAP, 1.5pF
C010	2113743N03	CAP, 1pF
C011	2113743N09	CAP, 2pF
C013	2186463Z07	CAP, 0.3pF
C014	2188884Y01	CAP, 0.7pF
C012DNP	2113743N26	CAP, 10pF
C015DNP	2113743M24	CAP, 0.1uF
C016DNP	2113743N26	CAP, 10pF
C020	2113743N40	CAP, 39pF
C021	2113743N40	CAP, 39pF
C022	2113743N40	CAP, 39pF
C023	2113743N40	CAP, 39pF
C100	2113928P04	CAP, 1.0uF
C101	2113928P04	CAP, 1.0uF
C102	2113928P04	CAP, 1.0uF
C103	2113928P04	CAP, 1.0uF
C104	2113743N38	CAP, 33pF
C105	2113928C04	CAP, 4.7uF
C106	2113928C04	CAP, 4.7uF
C107	2113743N50	CAP, 100pF
C108	2113741A45	CAP, .01uF
C109	2113743L21	CAP, 1500pF
C110	2113741A45	CAP, .01uF
C200	2187906N01	CAP, 4.7uF
C212	2113743L41	CAP, .01uF
C213	2113743L41	CAP, .01uF
C214	2113743L41	CAP, .01uF
C400	2113928A01	CAP, 1.0uF
C401	2113928A01	CAP, 1.0uF
C402	2113928A01	CAP, 1.0uF
C403	2113928A01	CAP, 1.0uF
C404	2113743L41	CAP, .01uF

Table 4-2. Electrical Parts List - C404 to C1019

Reference Number	Part Number	Description
C405	2113743N26	CAP, 10pF
C406	2113928A01	CAP, 1.0uF
C407	2113743N40	CAP, 39pF
C410	2113743L41	CAP, .01uF
C411	2113743L41	CAP, .01uF
C423	2113743N02	CAP, 0.75pF
C500	2113743L41	CAP, .01uF
C501	2113743L41	CAP, .01uF
C801	2113743N40	CAP, 39pF
C802	2113928C04	CAP, 4.7uF
C803	2113928A01	CAP, 1.0uF
C804	2113743N40	CAP, 39pF
C805	2113743N40	CAP, 39pF
C806	2113928A01	CAP, 1.0uF
C807	2113928C12	CAP, 10uF
C808	2113928C12	CAP, 10uF
C809	2113743N50	CAP, 100pF
C810	2113743N26	CAP, 10pF
C811	2113743N03	CAP, 1pF
C814	2113743N26	CAP, 10pF
C821	2113928C04	CAP, 4.7uF
C858	2113743N28	CAP, 12pF
C901	2113928C04	CAP, 4.7uF
C902	2113928C04	CAP, 4.7uF
C903	2113928C04	CAP, 4.7uF
C904	2113928C04	CAP, 4.7uF
C908	2113743M24	CAP, 0.1uF
C909	2113928C04	CAP, 4.7uF
C910	2113928P04	CAP, 1.0uF
C911	2113743N40	CAP, 39pF
C1000	2113743M24	CAP, 0.1uF
C1001	2113743M24	CAP, 0.1uF
C1002	2113743M24	CAP, 0.1uF
C1003	2113743M24	CAP, 0.1uF
C1004	2113743M24	CAP, 0.1uF
C1005	2113947H01	CAP, 0.1uF
C1007	2113947H01	CAP, 0.1uF
C1008	2113947H01	CAP, 0.1uF
C1009	2113947H01	CAP, 0.1uF
C1011	2113947H01	CAP, 0.1uF
C1012	2113947H01	CAP, 0.1uF
C1013	2113947H01	CAP, 0.1uF
C1014	2113743M24	CAP, 0.1uF
C1019	2113743M24	CAP, 0.1uF

Table 4-3. Electrical Parts List - C1020 to C3563

Reference Number	Part Number	Description
C1020	2113743M24	CAP, 0.1uF
C1021	2113743M24	CAP, 0.1uF
C1022	2113743M24	CAP, 0.1uF
C1025	2113947H01	CAP, 0.1uF
C1026	2113947H01	CAP, 0.1uF
C1027	2113743M24	CAP, 0.1uF
C1028	2113947H01	CAP, 0.1uF
C1031	2113947H01	CAP, 0.1uF
C1034	2113947H01	CAP, 0.1uF
C1036	2113743M24	CAP, 0.1uF
C1037	2113947H01	CAP, 0.1uF
C1039	2113743M24	CAP, 0.1uF
C1040	2113743M24	CAP, 0.1uF
C1042	2113743M24	CAP, 0.1uF
C1044	2113743M24	CAP, 0.1uF
C1047	2113947H01	CAP, 0.1uF
C1160	2113743M24	CAP, 0.1uF
C1161	2113743M24	CAP, 0.1uF
C1305	2113743M24	CAP, 0.1uF
C1306	2113743M24	CAP, 0.1uF
C201DNP	2113743N26	CAP, 10pF
C3000	2113928C12	CAP, 10uF
C3001	2113928C12	CAP, 10uF
C3002	2113743M24	CAP, 0.1uF
C3050	2113928P04	CAP, 1.0uF
C3100	2113928C12	CAP, 10uF
C3101	2113928C12	CAP, 10uF
C3102	2113743M24	CAP, 0.1uF
C3150	2113928P04	CAP, 1.0uF
C3151	2113743N38	CAP, 33pF
C3200	2113743N44	CAP, 56pF
C3201	2113928C12	CAP, 10uF
C3202	2113743N54	CAP, 150pF
C3204	2113743M24	CAP, 0.1uF
C3205	2113928C12	CAP, 10uF
C3209	2113928P04	CAP, 1.0uF
C3300	2113928P04	CAP, 1.0uF
C3350	2113928C04	CAP, 4.7uF
C3400	2113928Z11	CAP, 22uF
C3403	2113743M24	CAP, 0.1uF
C3450	2113928P04	CAP, 1.0uF
C3550	2113928P04	CAP, 1.0uF
C3560	2113928Z11	CAP, 22uF
C3563	2113743M24	CAP, 0.1uF

Table 4-4. Electrical Parts List - C3600 to C4211

Reference Number	Part Number	Description
C3600	2113928P04	CAP, 1.0uF
C3651	2113743M24	CAP, 0.1uF
C3654	2113928P04	CAP, 1.0uF
C3700	2113928Z11	CAP, 22uF
C3703	2113743M24	CAP, 0.1uF
C3801	2113928P04	CAP, 1.0uF
C3850	2113928P04	CAP, 1.0uF
C3851	2113928P04	CAP, 1.0uF
C3900	2113743L41	CAP, .01uF
C3901	2113743L41	CAP, .01uF
C3906	2113743N38	CAP, 33pF
C3910	2113743M24	CAP, 0.1uF
C3911DNP	2113928P04	CAP, 1.0uF
C3950	2113928P04	CAP, 1.0uF
C3951	2113928C04	CAP, 4.7uF
C3960	2113928C12	CAP, 10uF
C3961	2113928C12	CAP, 10uF
C3962	2113743M24	CAP, 0.1uF
C3983	2113743N26	CAP, 10pF
C3984	2113743N26	CAP, 10pF
C3985DNP	2113743M24	CAP, 0.1uF
C4000	2113743N38	CAP, 33pF
C4001	2113743L21	CAP, 1500pF
C4002	2113928N01	CAP, 0.1uF
C4003	2113743N38	CAP, 33pF
C4005	2113743N30	CAP, 15pF
C4100	2113928N01	CAP, 0.1uF
C4101	2113743N38	CAP, 33pF
C4102	2113743N38	CAP, 33pF
C4103	2113743N38	CAP, 33pF
C4104	2113743N26	CAP, 10pF
C4105	2113743E07	CAP, .022uF
C4200	2113928N01	CAP, 0.1uF
C4201	2113743N38	CAP, 33pF
C4202	2113743N38	CAP, 33pF
C4203	2113743N38	CAP, 33pF
C4204	2113743N38	CAP, 33pF
C4205	2113928N01	CAP, 0.1uF
C4206	2113743N38	CAP, 33pF
C4207	2113928N01	CAP, 0.1uF
C4208	2113743N38	CAP, 33pF
C4209	2113743N38	CAP, 33pF
C4210	2113928C04	CAP, 4.7uF
C4211	2113743N38	CAP, 33pF

Table 4-5. Electrical Parts List - C4212 to C5222

Reference Number	Part Number	Description
C4212	2113743N30	CAP, 15pF
C4213	2113743N38	CAP, 33pF
C4214	2113743N38	CAP, 33pF
C4215	2113743N38	CAP, 33pF
C4216	2113743N30	CAP, 15pF
C421DNP	2113743N26	CAP, 10pF
C4300	2113743N38	CAP, 33pF
C4301	2113743L41	CAP, .01uF
C4302	2113743L41	CAP, .01uF
C4304	2113928N01	CAP, 0.1uF
C4305	2113743M24	CAP, 0.1uF
C4306	2113928Z11	CAP, 22uF
C4308	2113743N38	CAP, 33pF
C4356	2113928Z11	CAP, 22uF
C4392	2113743N40	CAP, 39pF
C4393	2113743N40	CAP, 39pF
C4400	2113928P04	CAP, 1.0uF
C4401	2113928N01	CAP, 0.1uF
C4402	2113743N38	CAP, 33pF
C4403	2113928P04	CAP, 1.0uF
C4500	2113743N38	CAP, 33pF
C4501	2113928N01	CAP, 0.1uF
C4502	2113928P04	CAP, 1.0uF
C4503	2113928N01	CAP, 0.1uF
C4504	2113743N38	CAP, 33pF
C4550	2113743L33	CAP, 4700pF
C4551	2113928N01	CAP, 0.1uF
C4901	2113928N01	CAP, 0.1uF
C4910	2113928N01	CAP, 0.1uF
C5000	2113743M24	CAP, 0.1uF
C5002	2113947B05	CAP, 33pF
C502DNP	2113743N26	CAP, 10pF
C5150	2113928F07	CAP, 10.0uF
C5151	2113743L01	CAP, 220pF
C5152	2113928C04	CAP, 4.7uF
C5202	2113928N01	CAP, 0.1uF
C5204	2113928P04	CAP, 1.0uF
C5208	2113743M24	CAP, 0.1uF
C5209	2113743M24	CAP, 0.1uF
C5203DNP	2113743N28	CAP, 12pF
C5211	2113947H01	CAP, 0.1uF
C5212	2113947H01	CAP, 0.1uF
C5221	2113947H01	CAP, 0.1uF
C5222	2113743M24	CAP, 0.1uF

Table 4-6. Electrical Parts List - C5223 to C7554

Reference Number	Part Number	Description
C5223	2113743M24	CAP, 0.1uF
C5225	2113743M24	CAP, 0.1uF
C5228	2113947H01	CAP, 0.1uF
C5234	2113947H01	CAP, 0.1uF
C5236	2113947H01	CAP, 0.1uF
C5237	2113928P04	CAP, 1.0uF
C5260	2113928P04	CAP, 1.0uF
C5261	2113743A31	CAP, 1uF
C5295DNP	2113743M24	CAP, 0.1uF
C5296DNP	2113743M24	CAP, 0.1uF
C5400	2113928C04	CAP, 4.7uF
C5402	2113743M24	CAP, 0.1uF
C5403	2113743N30	CAP, 15pF
C5503	2113743N26	CAP, 10pF
C5501DNP	2113743N26	CAP, 10pF
C5502DNP	2113743N26	CAP, 10pF
C5505DNP	2113743N26	CAP, 10pF
C5698	2113743L17	CAP, 1000pF
C5697DNP	2113946D02	CAP, 1.0uF
C6000	2113743L17	CAP, 1000pF
C6001	2113743N28	CAP, 12pF
C6002	2113743L11	CAP, 560pF
C6003	2113743L25	CAP, 2200pF
C6004	2113743N28	CAP, 12pF
C6005	2113743N28	CAP, 12pF
C6006	2113743N32	CAP, 18pF
C6007	2113743N28	CAP, 12pF
C6008	2113743Q03	CAP, 1pF
C6009	2113743E20	CAP, 0.1uF
C6010	2113743L41	CAP, .01uF
C6012	2113743L17	CAP, 1000pF
C6013	2113743L41	CAP, .01uF
C6014	2113743E20	CAP, 0.1uF
C6015	2113743L17	CAP, 1000pF
C6016	2113743L17	CAP, 1000pF
C6017	2113743E20	CAP, 0.1uF
C6018	2113743L41	CAP, .01uF
C6011DNP	2113743E20	CAP, 0.1uF
C6019DNP	2113743E20	CAP, 0.1uF
C6020	2113743N28	CAP, 12pF
C6021	2113743E20	CAP, 0.1uF
C6025	2113743L17	CAP, 1000pF
C6026DNP	2113928N01	CAP, 0.1uF
C7554	2113743N28	CAP, 12pF

Table 4-7. Electrical Parts List - C7556 to D5150

Reference Number	Part Number	Description
C7556DNP	2113928N01	CAP, 0.1uF
C7557DNP	2113928N01	CAP, 0.1uF
C7903	2187893N01	CAP, 1.0uF
C7905	2113743M24	CAP, 0.1uF
C7904DNP	2113946D02	CAP, 1.0uF
C7921	2113743N28	CAP, 12pF
C7925	2113928T01	CAP, 1uF
C7926	2113928N01	CAP, 0.1uF
C7927	2113743L13	CAP, 680pF
C7928	2113743E20	CAP, 0.1uF
C7929	2113947H01	CAP, 0.1uF
C7920DNP	2113743N32	CAP, 18pF
C7922DNP	2113928N01	CAP, 0.1uF
C812DNP	2113743N26	CAP, 10pF
C815DNP	2113743N26	CAP, 10pF
C816DNP	2113743N26	CAP, 10pF
C817DNP	2113743N26	CAP, 10pF
C818DNP	2113743N26	CAP, 10pF
C822DNP	2113743N26	CAP, 10pF
C823DNP	2113743N26	CAP, 10pF
C824DNP	2113743N26	CAP, 10pF
C825DNP	2113743N26	CAP, 10pF
CR3000	4809924D18	RB520S-30
CR3900	4813832M85	NZQA6V8AXV5T1
CR5100	4886193U03	SD15C_TC
CR5101	4886193U03	SD15C_TC
CR5103	4886193U03	SD15C_TC
CR5104	4888112M10	12M10
CR5105	4888112M10	12M10
CR5106	4888112M10	12M10
CR5107	4888112M10	12M10
CR5401	4809948D42	RB751V40
CR5500DNP	4813832M85	NZQA6V8AXV5T1
CR7500	4813832M85	NZQA6V8AXV5T1
CR7501	4813832M85	NZQA6V8AXV5T1
CR7900	4813832M85	NZQA6V8AXV5T1
CR7901	4813832M85	NZQA6V8AXV5T1
CR7902	4813832M85	NZQA6V8AXV5T1
CR7903	4813832M85	NZQA6V8AXV5T1
D001	4809948D37	BA892
D3100	4809924D18	RB520S-30
D3961	4809653F07	MBRM120ET3
D3962	4809653F07	MBRM120ET3
D5150	4809924D24	IR1H40CSP

Table 4-8. Electrical Parts List - E201 to E5253

Reference Number	Part Number	Description
E201	SHORT_RES0201	SHORT
E203	SHORT_RES0201	SHORT
E204	SHORT_RES0201	SHORT
E205	SHORT_RES0201	SHORT
E206	SHORT_RES0201	SHORT
E207	SHORT_RES0201	SHORT
E208	SHORT_RES0201	SHORT
E209	SHORT_RES0201	SHORT
E801	SHORT_RES0201	SHORT
E802	SHORT_RES0201	SHORT
E903	SHORT_RES0201	SHORT
E904	SHORT_RES0201	SHORT
E1010	SHORT_RES0402	SHORT
E1011	SHORT_RES0402	SHORT
E1012	SHORT_RES0402	SHORT
E1013	SHORT_RES0402	SHORT
E1014	SHORT_RES0402	SHORT
E2010	SHORT_RES0201	SHORT
E2011	SHORT_RES0201	SHORT
E2012	SHORT_RES0201	SHORT
E3001	SHORT_RES0402	SHORT
E3100	SHORT_RES0402	SHORT
E3150	SHORT_RES0402	SHORT
E3183	SHORT_RES0402	SHORT
E3201	SHORT_RES0402	SHORT
E3350	SHORT_RES0402	SHORT
E3902	SHORT_RES0402	SHORT
E4008	SHORT_RES0201	SHORT
E4009	SHORT_RES0201	SHORT
E4551	SHORT_RES0201	SHORT
E4552	SHORT_RES0201	SHORT
E5103	SHORT_RES0402	SHORT
E5125	SHORT_RES0402	SHORT
E5128	SHORT_RES0402	SHORT
E5201	SHORT_RES0402	SHORT
E5204	SHORT_RES0402	SHORT
E5205	SHORT_RES0402	SHORT
E5206	SHORT_RES0402	SHORT
E5210	SHORT_RES0402	SHORT
E5211	SHORT_RES0402	SHORT
E5212	SHORT_RES0402	SHORT
E5214	SHORT_RES0402	SHORT
E5251	SHORT_RES0201	SHORT
E5253	SHORT_RES0201	SHORT

Table 4-9. Electrical Parts List - E5406 toL005

Reference Number	Part Number	Description
E5406	SHORT_RES0201	SHORT
E5505	SHORT_RES0402	SHORT
E5605	SHORT_RES0402	SHORT
E5606	SHORT_RES0402	SHORT
E7548	SHORT_RES0201	SHORT
E7549	SHORT_RES0201	SHORT
E7584	SHORT_RES0201	SHORT
E7905	SHORT_RES0402	SHORT
FD1	FIDUCIAL_CE	CE_FIDUCIAL
FD2	FIDUCIAL_CE	CE_FIDUCIAL
FD3	FIDUCIAL_CE	CE_FIDUCIAL
FD4	FIDUCIAL_CE	CE_FIDUCIAL
FL002	9109674L20	S0351
FL003	9109674L21	CF61A5601
FL004	9109674L17	74L17
FL100	9188695K05	CSPRC032AG
FL900	9109239M38	SAFSD2G14
FL4000	4889526L15	CSPEMI201AG
FL4300	4889526L14	CSPEMI202AG
FL5100	4889526L12	CSPEMI306AG
FL5101	4889526L12	CSPEMI306AG
FL6000	9180310L36	SAW_1575_42MHZ
FL6001	9189312N01	B9000
FSH5260	4889615N02	LNJ0F1X7F0MT
J402	3987977Y01	CONTACT
J403	3987977Y01	CONTACT
J3000	TPSM0_50X0_70	TEST_POINT
J3001	TPSM0_50X0_70	TEST_POINT
J3901	3989655N02	CONTACT
J4000	3987495Y02	CONN_P
J4001	3987495Y02	CONN_P
J4200	3988194N04	CONN_J
J4201	3988194N04	CONN_J
J4300	0989675N03	CONN_J
J5000	0987636K08	CONN_J
J5100	0989721N01	CONN_J
J5400	3987697Y02	CONTACT
J5500	3904824R01	CONTACT
J6002	3988194N01	CONN_J
J7500	0988866N01	CONN_J
J7900	0988866N01	CONN_J
L002	2488090Y09	IDCTR, 4.7nH
L003	2488090Y08	IDCTR, 3.9nH
L005	2488090Y06	IDCTR, 2.7nH

Table 4-10. Electrical Parts List - L001 to Q3960

Reference Number	Part Number	Description
L001DNP	2462587V44	IDCTR, 680nH
L013	2487319K01	IDCTR, 1.0nH
L014	2487319K01	IDCTR, 1.0nH
L200	0662057M01	RES, 0
L201	2488090Y24	IDCTR, 82nH
L203	2488090Y19	IDCTR, 33nH
L502	0662057M56	RES, 180
L5600DNP	2488090Y08	IDCTR, 3.9nH
L811	2113743N22	CAP, 6.8pF
L812	2488090Y12	IDCTR, 8.2nH
L3000	2588079Y03	IDCTR, 10uH
L3100	2590031N05	IDCTR, 6.8uH
L3206	2588079Y03	IDCTR, 10uH
L3207	2409377M03	IDCTR, 6.8nH
L4000	2488090Y21	IDCTR, 47nH
L4001	2488090Y21	IDCTR, 47nH
L4203	2409414M42	IDCTR, 48nH
L4204	2409414M42	IDCTR, 48nH
L4205	2409414M42	IDCTR, 48nH
L4206	2409414M42	IDCTR, 48nH
L4399	2409646M13	IDCTR, 39nH
L4400	2409646M13	IDCTR, 39nH
L5150	2590031N05	IDCTR, 6.8uH
L5260	2588079Y07	IDCTR, 15uH
L6000	2488090Y17	IDCTR, 22nH
L6001	2488090Y19	IDCTR, 33nH
L6002	2488090Y07	IDCTR, 3.3nH
L6003	2488090Y19	IDCTR, 33nH
L6004	2488090Y19	IDCTR, 33nH
L6005	2488090Y19	IDCTR, 33nH
L7912	2409154M48	IDCTR, 100nH
L7913	2409154M48	IDCTR, 100nH
L813DNP	2488090Y12	IDCTR, 8.2nH
M100	1188983Y01	1188983Y01
M101	1188983Y01	1188983Y01
M102	1188983Y01	1188983Y01
M103	1188983Y01	1188983Y01
N001	0987378K01	SWITCH
Q3200DNP	4809579E02	2SK1830
Q3403	4804616R01	MBT35200MT1
Q3560	4804616R01	MBT35200MT1
Q3652	4809579E02	2SK1830
Q3703	4804616R01	MBT35200MT1
Q3960	4803558C01	IRF6100

Table 4-11. Electrical Parts List - Q3961 to R1072

Reference Number	Part Number	Description
Q3961	4803558C01	IRF6100
Q3963	4809807C42	SI8405DB
Q3964	4803558C01	IRF6100
Q5001	5109817F58	17F58
Q5100	4813824A17	MMBT3906
Q5401DNP	4809579E58	FDG6332C
R001	0662057C01	RES, 0
R002	0662057M86	RES, 3.3K
R003	0662057M81	RES, 2K
R004	SHORT_RES0402	SHORT
R005	0662057M98	RES, 10K
R015	0662057M98	RES, 10K
R100	SHORT_RES0402	SHORT
R101	SHORT_RES0402	SHORT
R102	SHORT_RES0402	SHORT
R103	SHORT_RES0402	SHORT
R105	0662057M78	RES, 1.5K
R106	0662057M78	RES, 1.5K
R202	0662057M40	RES, 39
R203	SHORT_RES0402	SHORT
R400	0662057M62	RES, 330
R402	0662057M66	RES, 470
R420	2113743N24	CAP, 8.2pF
R502	2113743N38	CAP, 33pF
R801	0662057M01	RES, 0
R802	0662057M01	RES, 0
R804	2113743N17	CAP, 4.3pF
R807	0662057M01	RES, 0
R810	0662057M01	RES, 0
R811	0662057M01	RES, 0
R812	0662057M01	RES, 0
R901	0662057M01	RES, 0
R903	0662057M50	RES, 100
R905	SHORT_RES0402	SHORT
R906	SHORT_RES0402	SHORT
R907	SHORT_RES0402	SHORT
R1015	0662057M01	RES, 0
R1016DNP	0662057M01	RES, 0
R1017DNP	0662057M01	RES, 0
R1018DNP	0662057M01	RES, 0
R1038	0662057M01	RES, 0
R1032DNP	0662057M01	RES, 0
R1071	0662057M01	RES, 0
R1072	0662057M01	RES, 0

Table 4-12. Electrical Parts List - R1075 to R4911

Reference Number	Part Number	Description
R1075	0662057M98	RES, 10K
R3001	0687874L02	RES, 0.1
R3101	0687874L02	RES, 0.1
R3200DNP	0662057N23	RES, 100K
R3205DNP	0662057M01	RES, 0
R3210	0662057V41	RES, 270K
R3211	0662057V29	RES, 120K
R3650	0662057M78	RES, 1.5K
R3651	0662057M34	RES, 22
R3652	0662057M34	RES, 22
R3654	0662057N15	RES, 47K
R3805	SHORT_RES0402	SHORT
R3900	0662057M98	RES, 10K
R3901	0662057N20	RES, 75K
R3903	0662057V11	RES, 22K
R3904	0662057V43	RES, 330K
R3905	0662057V02	RES, 10K
R3906	0662057V17	RES, 39K
R3907	0662057V02	RES, 10K
R3910	0662057M98	RES, 10K
R3911	0662057M98	RES, 10K
R3912	0662057M98	RES, 10K
R3960	0687874L01	RES, 0.24
R3961	0688044N02	RES, 20m
R3962	0662057M92	RES, 5.6K
R3963	0662057N30	RES, 200K
R3965	SHORT_RES0402	SHORT
R4000	0662057N07	RES, 22K
R4100	0662057M90	RES, 4.7K
R410DNP	0662057M01	RES, 0
R412DNP	0662057M01	RES, 0
R4200	0662057N23	RES, 100K
R4202	0662057N23	RES, 100K
R4255	0662057N06	RES, 20K
R4300	0662057N15	RES, 47K
R4301	0662057N15	RES, 47K
R4302	0662057M90	RES, 4.7K
R4400	0662057M50	RES, 100
R4401	0662057M74	RES, 1K
R4550	0662057M92	RES, 5.6K
R4901	0662057N15	RES, 47K
R4902	0662057N33	RES, 270K
R4910	0662057V41	RES, 270K
R4911	0662057V27	RES, 100K

Table 4-13. Electrical Parts List - R5000 to R830

Reference Number	Part Number	Description
R5000	0662057N23	RES, 100K
R5001	0662057N15	RES, 47K
R5100	0662057M98	RES, 10K
R5101	0662057M14	RES, 3.3
R5106	0662057M59	RES, 240
R5108	0662057M59	RES, 240
R5120	0662057M50	RES, 100
R5121	0662057M50	RES, 100
R5122	0662057M50	RES, 100
R5123	0662057M50	RES, 100
R5124	0662057M50	RES, 100
R5126	0662057M50	RES, 100
R5127	0662057M50	RES, 100
R5150	0662057V27	RES, 100K
R5151	0662057V10	RES, 20K
R5204	0662057N23	RES, 100K
R5203DNP	0662057N23	RES, 100K
R5207DNP	0662057M98	RES, 10K
R5208DNP	0662057M98	RES, 10K
R5260	0662057M37	RES, 30
R5262	0662057R19	RES, 100
R5263	0662057R19	RES, 100
R5265	0662057M98	RES, 10K
R5299	0662057V35	RES, 200K
R5401	0662057M90	RES, 4.7K
R5402	0662057M50	RES, 100
R5405DNP	0662057N39	RES, 470K
R5501	0662057M92	RES, 5.6K
R5502	0662057M01	RES, 0
R5503	0662057M01	RES, 0
R5504	0662057M01	RES, 0
R5600	0662057M98	RES, 10K
R5601	0662057M98	RES, 10K
R5603	0662057N23	RES, 100K
R5607	0662057N37	RES, 390K
R6000	0662057U85	RES, 2.2K
R6005	0662057M01	RES, 0
R6006	0662057N23	RES, 100K
R6026	0662057M01	RES, 0
R7904DNP	0662057M01	RES, 0
R7949DNP	0662057M01	RES, 0
R7980DNP	0662057M01	RES, 0
R803DNP	0662057M01	RES, 0
R830DNP	0662057M01	RES, 0

Table 4-14. Electrical Parts List - SH400 to U5260

Reference Number	Part Number	Description
SH400	2688050Y02	SHIELD
SH1000	2687670Y02	SHIELD
SH5600	2688060Y01	SHIELD
SH7901	2688476Y02	SHIELD
SP4300DNP	1009798H02	SOLDER_PELLET
SP4301DNP	1009798H02	SOLDER_PELLET
SW5130	4088591Y01	SWITCH
SW5131	4088591Y01	SWITCH
SW5132	4088591Y01	SWITCH
SW5133	4088591Y01	SWITCH
SW5134	4088591Y01	SWITCH
SW5135	4088591Y01	SWITCH
SW5136	4088591Y01	SWITCH
SW5137	4088591Y01	SWITCH
SW6000	0987378K01	SWITCH
T901	5885949K04	HHM1515
T902	5885949K06	HHM1526
T903	5885949K06	HHM1526
U001	5109944C61	MC13820
U002	4889729N03	FEM3203_ES6D
U003DNP	5113837M44	NL17SZ16
U100	5188450M23	50M23
U1019DNP	5113837M42	NL17SZ32
U1020DNP	5109522E82	NC7SB3157
U200	5188450M21	50M21
U400	5189552N01	MMM5092
U401	5109768D08	LM20
U800	5188220Y02	20Y02
U900	4889717N03	17N03
U1000	5199155K01	DSPIO
U1160	5113837M40	NL17SZ00
U1161	5113837M42	NL17SZ32
U1305	5114007M44	NL17SV08
U1306	5114007M44	NL17SV08
U3000	5185941F02	TWL93010DGZGR
U3650	5164751E01	MC74VHC1GT50
U3651	5109522E90	NC7SP125
U4200	5109731C42	TPA2010D1
U5000	4889526L12	CSPEMI306AG
U5001	4889526L13	CSPEMI307AG
U5150	5102834Y91	LT1930
U5201	5187911Y01	SC4
U5253	5164751E01	MC74VHC1GT50
U5260	5188706Y01	LM3500

Table 4-15. Electrical Parts List - U5600 to Y3982

Reference Number	Part Number	Location
U5600	4889695L14	95L14
U6000	5109841C71	GPS
U6001	5164751E01	MC74VHC1GT50
U9130	5188128Y01	TPS62021
VR3954	4813832M84	SD05T1
VR4300	4809948D49	CSPESD304G
VR4301	4809788E08	UDZS8_2B
VR5000	4813832M84	SD05T1
VR5005	4886193U03	SD15C_TC
VR5102	4809948D49	CSPESD304G
VR5103	4809948D49	CSPESD304G
VR5104	4809948D49	CSPESD304G
VS4200	4809788E06	UDZTE-176.8B
VS4201	4809788E06	UDZTE-176.8B
VS4202	4809788E06	UDZTE-176.8B
VS5001	4886193U03	SD15C_TC
VS5002	4813832M84	SD05T1
VS5400	4809788E06	UDZTE-176.8B
Vs4203	4809788E06	UDZTE-176.8B
Y500	4809718L20	TCO-5871
Y3982	4809995L13	CC5V