NVIDIA

User Guide

SC15

Eval3 Board Kit

PRELIMINARY INFORMATION
RELEASED UNDER NDA ONLY

BD-01996-001_v01

HANDHELD

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Revision History

Date	Revision	Description
09/15/05	Advance v01	First version of document.

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Chapter 1 SC15 Evaluation Kit

1.1 Introduction

The NVIDIA® SC15 Evaluation Board Kit enables SC15-specific development and evaluation. Its modular design supports all SC15 module variants and legacy interfaces.

1.2 Applicable Documentation

To further support use of the SC15 Evaluation Board Kit, use this document along with

- *SC15 Technical Manual and Data Sheet* (NVIDIA document DP-01433-001)

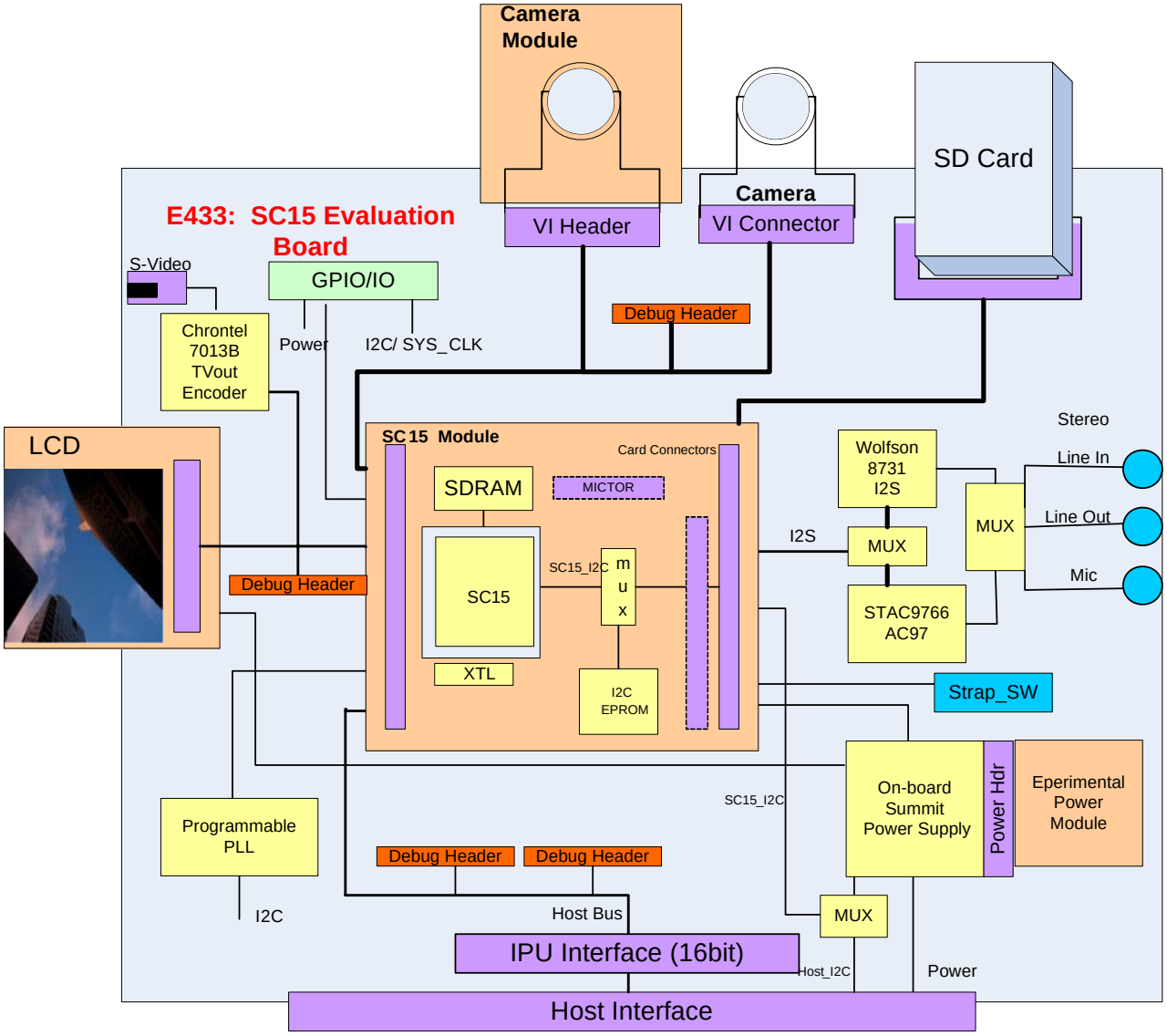
1.3 SC15 Evaluation Board Kit Contents

- SC15 Evaluation Board
- SC15 Module
  - 600-80436-0002-100 PCB Assembly for SC15-NM version
  - 600-80436-0000-100 PCB Assembly for SC15-8ME version
  - 600-80438-001-000: SC15 with 640KB eSRAM and additional, external DDR memory
- NVIDIA LCD Module
  - 600-80431-0000-000 PCB Assembly with Optrex 320 x 240 LCD panel
  - Omnivision OV9650 1.3Mpixel camera
  - PCI32B-BCA5 Standard Windows PC PCI Card

1.4 Evaluation Board Kit Features

Figure 1.1 shows the SC15 Evaluation Board Kit. The main platform is the SC15 Evaluation Board, used with the SC15 module (which contains an SC15.) Because the SC15 is available with different memory configurations, the SC15 module comes with one of the different configurations on it. (Choose the SC15 module corresponding to the version of SC15 chosen for your design.) An LCD module completes the kit. The camera module is optional, as the Evaluation Board comes with a camera already mounted on it.

Figure 1.1: SC15 Evaluation Board Kit Block Diagram



Chapter 2 SC15 Evaluation Board

2.1 Introduction

The NVIDIA® SC15 Evaluation Board Kit has been developed for SC15-specific development and evaluation purposes. Its modular design supports all SC15 module variants and legacy interfaces. Basic features of the E433 follow:

Highly configurable operational modes

- Software programmable through I2C
- Manual mode through Switches and Jumpers

Host configuration support for

- Type A and Type C interfaces
- 32Bit and 16bit interfaces
- Indirect and direct addressing modes
- IPU interface: 16bit, type C

Peripheral devices and interfaces supported

- I^2S Audio using Wolfson WM8731 codec
- AC'97 Audio using SigmaTel CODEC
- SD Socket with insert detect and write protect
- OV 9650 camera module and generic camera interface connector
- LCD Interface Connector
- JTAG, DSP JTAG
- Variable power supply for each rail
- SVideo out using Chrontel CH7013B
- NTSC and PAL outputs

Modules used with the SC15 Evaluation Board, which enable its use as part of a complete kit include the following:

- SC15 Module
  - 600-80436-0002-100 PCB Assembly for SC15-NM version
  - 600-80436-0000-100 PCB Assembly for SC15-8ME version
  - 600-80438-001-000: SC15 with 640KB eSRAM and additional, external DDR memory
- NVIDIA LCD Module
- NVIDIA Camera Module

2.2 SC15 Evaluation Board Features

- Uses PC/PLX PCI card - performance benchmark
- SC15 Module connection to support both rapid design change and different revisions or SKUs of SC15
- SC15 peripheral components:
  - SDRAM/DDR on board (with optional Mictor)
  - XTL clock source
  - External CLK input as primary source (need GFSDK approval)
  - Power measurement Test Points

- Major components
  - LCD panel connector
  - Low profile camera I/F connector
  - Audio CODECs (AC'97/I^2S) with connectors
  - Mictor for host and connector for I2S
  - I2C programmable core & I/O power supplies; and manual control with external card for bring-up
  - SD card
  - SC15 GPIO connector for power control
  - Host Interface connector (PLX I/O PCI card)
  - JTAG
  - I2C PLL OSC as SC15 external clock
  - NTSC encoder for VGA output
  - PAL support
  - Board automation for bus type/width selection

2.3 SC15 Evaluation Board Diagrams

The two figures in this section, Figure 2.1 and Figure 2.2, show the physical layout of the SC15 Evaluation Board from both the top and bottom view, for easy reference.

Figure 2.1: SC15 Evaluation Board Top View

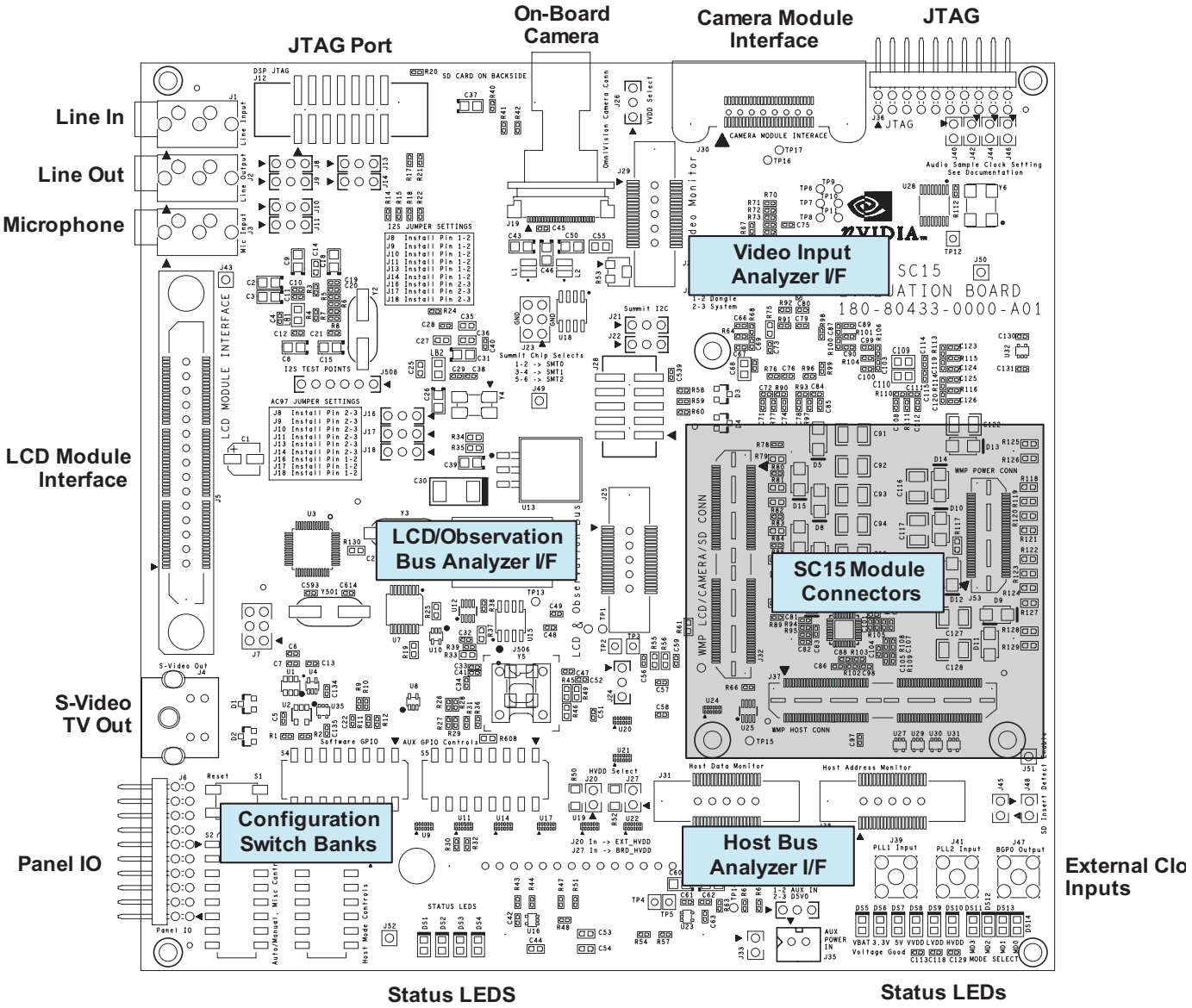
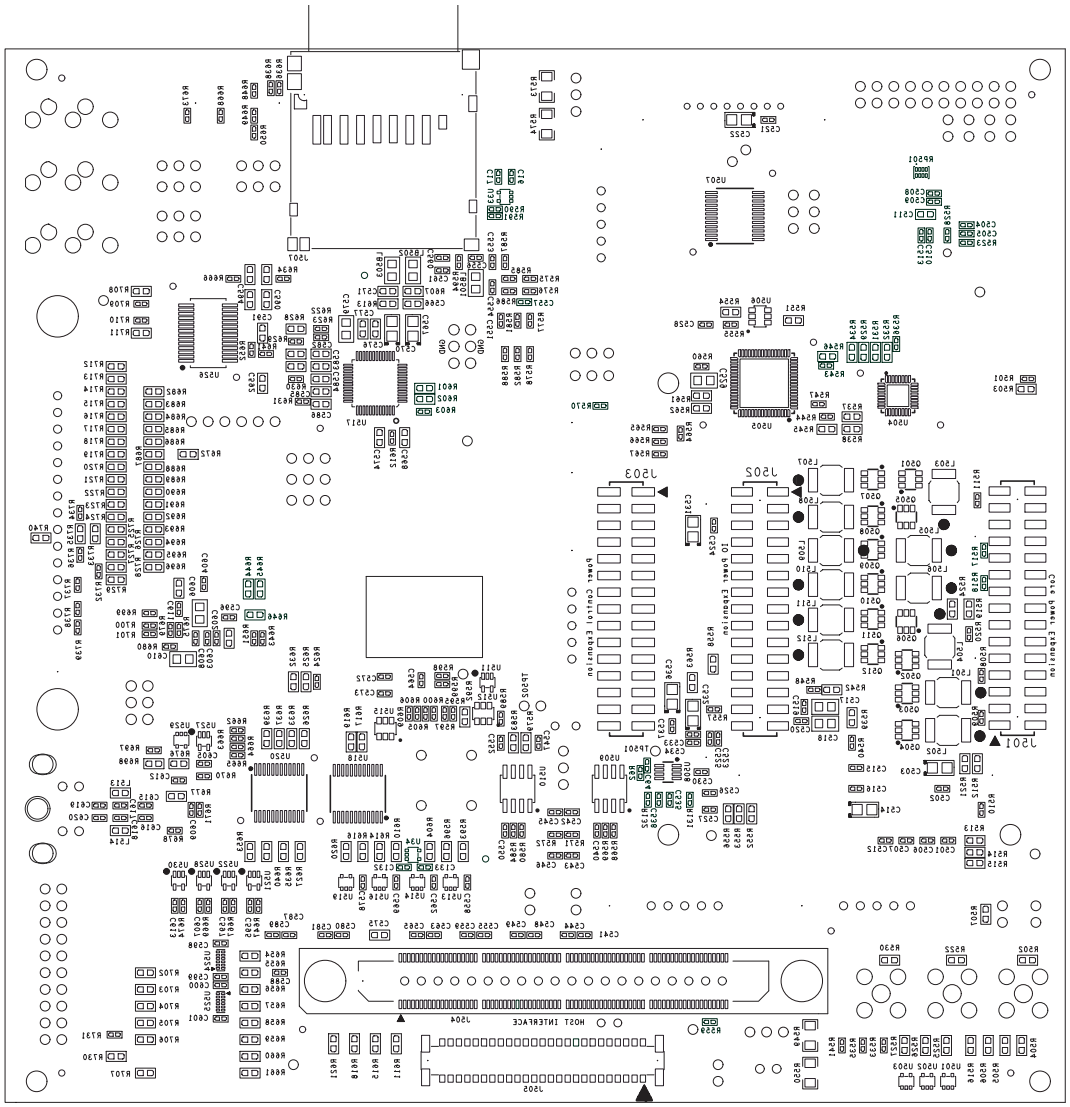


Figure 2.2: SC15 Evaluation Board Bottom View



Chapter 3 Functional Overview

3.1 Feature Overview

- Host interface
- Wireless Media Processor Module Support
- Video input
    - On-board Camera
    - Camera Module Connector

- LCD Display Support
- TVout
- Audio
    - I2C Codec
    - AC97 Coded

I2C Control Bus

- Clocking
- Power
    - Power Management
    - Power module
- Debug support
- JTAG
    - Standard
    - DSP JTAG

3.1.1 Reset

The Maxim 6306UK4.4 is used to generate a 200 ms reset. The reset is triggered three ways:

- Turning on the PCI32B-BCAx
- Depressing the SW1 push button
- Issued by JTAG debugger
- Issued by Host GPIO.

3.1.2 I2C Source

There are two sources for the I2C interface:

- Host I2C
- SC15 I2C

The default is the Host system. The User must configure SW3-7 to use the SC15's I2C.

3.1.3 Power

All power rails of the SC15 are controlled by high-precision voltage regulators (SMB120 or SMB113.)

- The voltage levels can be programmed via I2C
- SMB120 and SMB113 are accurate to +/- 50 mV of the programmed voltage value
- Core voltage regulators are all controlled by the Summit SMB113, at address 0x84h.
- Host and SD card IO voltages are controlled by the SMB120 at address 0x80h
- LCD, camera, audio Codec, and DRAM memory IO voltages are controlled by the SMB113 at address 0x88

3.1.4 SD

Two of SC15's GPIOs are used in the following configuration:

- SD Detect on SGPO0 of SC15
  - True = 1
  - False = 0

- Write Protect SGPO1 of SC15
  - True = 1
  - False = 0

3.1.5 Camera

The SC15 Evaluation Board supports an on-board camera, the Omnivision OV9650 1.3 Mpixel CMOS sensor.

A customer-specific camera board may be installed and tested by using the expansion connector on the SC15 Evaluation Board.

The SC15 controls the I2C for these two modules.

Chapter 4 Power Management

4.1 SC15 Power Rails

This section highlights the SC15 power rails, adjustment of those rails, and software power management of the SC15.

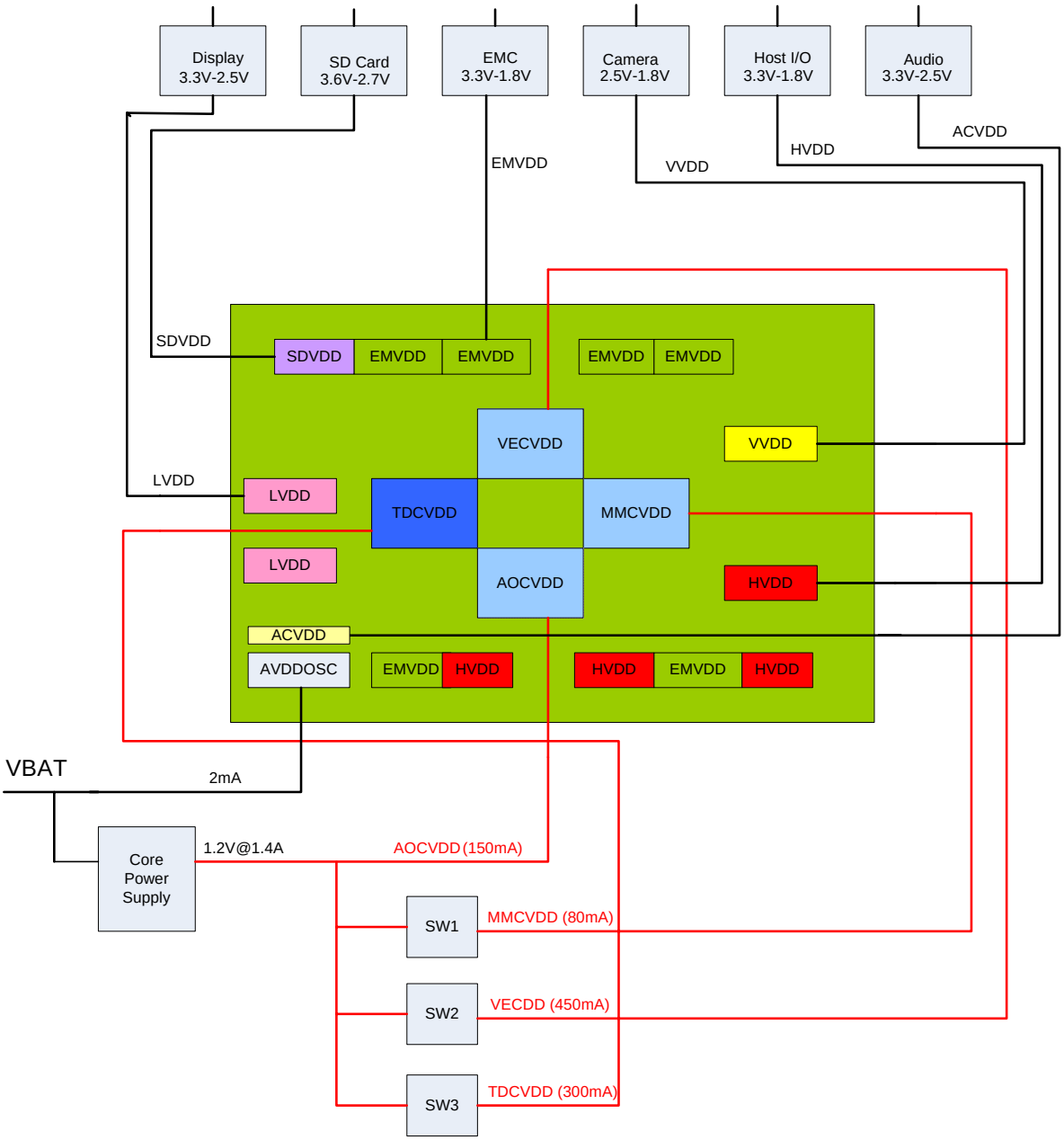
- SC15 Power Requirements
  - AOCVDD 1.2*.15=0.18 W
  - MMCVDD 1.2*.08=0.096 W
  - VECDD 1.2*.45=0.54 W
  - TDCVDD 1.2*.3=0.36 W
  - I/O pads ~ Ave 2.5*.1=0.25 W

    Total Power = 1.4 W

- System
  - CODECS (AC'97)
  - 3.3*0.1=0.33 W + 5.0*0.08=0.26 W
  - SD card =3.3*0.1=0.33 W
  - 100 mW - 400 mW based on camera
  - MDDR (x32) = 1.8*0.08 = 0.15 W (REF mode)
  - Display (0.5-1.5 W) BL "ON"
  - SC15= 1.4 W

    Card Operating Power
    ~ 1.4 W+2.65 W = 4.0 W

Figure 4.1: SC15 Power Rails



4.2 Software Power Management

Table 4.1: Software Power Management Configuration

U30	Control	0	1	Description
IO-0.3	AOCVDD	ON	OFF	Main core voltage On/Off
IO-0.4	VECVDD	ON	OFF	Video core voltage On/Off
IO-0.5	TDVCDD	ON	OFF	3D core voltage On/Off
IO-0.6	MMCVDD	ON	OFF	Embedded memory voltage On/Off
IO-0.7	SDVDD	ON	OFF	SD Interface voltage On/Off
IO-1.0	VVDD	ON	OFF	Camera Interface voltage On/Off
IO-1.1	DPD_	DPD mode	Normal	SC15 DPD mode
IO-1.2	POWER_EN	Plugged	Unplugged	As Input, allows software to read if an SC15 module is plugged onto the Evaluation Board.
IO-1.3	LDVDD	ON	OFF	Display Interface voltage On/Off
IO-1.4	AVDDOSC	ON	OSC	Crystal oscillator voltage On/Off
IO-1.5	AVDDP1	ON	OFF	PLL0 voltage On/Off (May use to control EMCVDD on this bit if PLL voltage control is not required.)
IO-1.6	AVDDP2	ON	OFF	PLL1 voltage On/Off (May use to control EMCVDD on this bit if the PLL voltage control is not required.)
IO-1.7	HVDD	OFF	ON	Host Interface voltage On/Off (should be provided as default by host)

4.3 Software Power Rails Adjustment

Use the I2C to adjust the following supply voltages.

Table 4.2: Software Power Management Configuration

U30	Control	Description
U67	AOCVDD	Main core voltage level control
U66	VECVDD	Video core voltage level control
U69	TDVCDD	3D core voltage level control
U71	MMCVDD	Embedded memory core voltage level control
U40	VVDD	Camera Interface voltage level control
U36	AVDDP1	PLL0 voltage level control
U37	AVDDP2	PLL1 voltage level control

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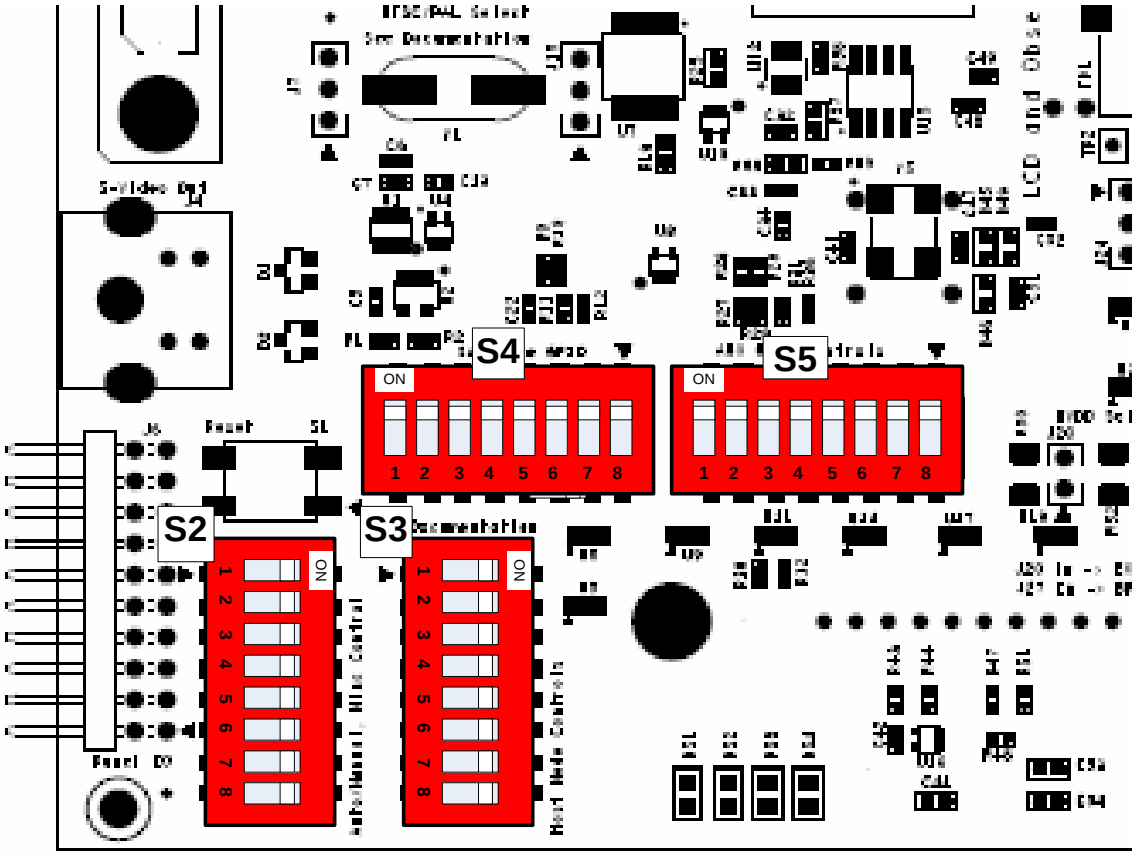
Chapter 5 Evaluation Board Configuration

5.1 Hardware Configuration

Configure the Evaluation Board by switch banks and jumper settings detailed in this chapter. Switch banks S2, S3, S4, and S5 are located as shown in Figure 5.1.

Figure 5.1: SC15 Evaluation Board Switch Banks



5.1.1 Switch Bank Configuration Details

Configure the Evaluation Board using switch banks S1, S2, S3, and S4. Details for doing so follow. In each table, shaded cells indicate default configuration settings.

Table 5.1: Switch Bank S2: Auto and Manual Configuration

	Name	Configuration	Description	Switch Function
1	AUTO / MANUAL OVERRIDE	ON = Normal	All SC15 and board control signals are controlled by switch S3.	Auto Override of board configuration: If this switch is set to OFF, the controls are configured by software only using SPB.
		OFF = Override	All SC15 and board control signals are controlled by SPB GPIO expander. This switch position overrides other switches of S2.	
2	MODE (partial auto mode)	ON = Manual	MOD pins controlled by SW4	SC15 MOD pins HW or SW configuration: This switch has effect only when S2-1 is ON
		OFF = Auto	MOD pins controlled by SPB GPIO expander	
3	BUS WIDTH 16 / 32 (partial auto mode)	ON = Manual	16-bit/32-bit Host I/F controlled by SW4	16bit or 32bit Host I/F HW or SW configuration: This switch has effect only if S2-1 is ON
		OFF = Auto	16-bit/32-bit Host I/F controlled by SPB GPIO expander	
4	BUS TYPE C EMULATION (partial auto mode)	ON = Manual	Type C controlled by SW4	Type C HW or SW configuration This switch has effect only if S2-1 is ON.
		OFF = Auto	Type C controlled by SPB GPIO expander	
5	VARIABLE LATENCY (partial auto mode)	ON = Manual	Variable latency controlled by S3. Only supported in certain Host platforms. Please refer to schematics for more details.	Variable latency HW or SW configuration: This switch has effect only if S2-1 is ON.
		OFF = Auto	Variable latency controlled by SPB GPIO expander	
6	SPARE	ON = GND	N/A	Programmable I/O. Defaults as input pulled low.
		OFF = Pull up	N/A	
7	No Function	N/A	N/A	N/A - No Function
8	INDIRECT ADDRESSING REMAP	ON = LSB	SC15-A[3:2] address bits are controlled by Host A[3:2]	In Indirect mode configuration SC15 address bits A2 and A3 can be shifted to higher bits for easier address and data mapping by the software
		OFF = MSB	SC15-A[3:2] address bits are controlled by Host A[22:21]	

Table 3.2 details the settings of switch bank S3 for setting various host mode control configurations.

Table 5.2: Switch Bank S3: Host Mode Configurations

	Name	Configuration	Description	Switch Function
1	MODE BIT 0	ON = Low	MOD0 = 0	SC15 MOD0 pin HW control *This switch has effect only if S2-1 and S2-2 are ON*
		OFF = High	MOD0 = 1	
2	MODE BIT 1	ON = Low	MOD1 = 0	SC15 MOD1 pin HW control *This switch has effect only if S2-1 and S2-2 are ON*
		OFF = High	MOD1 = 1	
3	MODE BIT 2	ON = Low	MOD2 = 0	SC15 MOD2 pin HW control *This switch has effect only if S2-1 and S2-2 are ON.*
		OFF = High	MOD2 = 1	
4	MODE BIT 3	ON = Low	MOD3 = 0	SC15 MOD3 pin HW control *This switch has effect only if S2-1 and S2-2 are ON.*
		OFF = High	MOD3 = 1	
5	BUS 16/32	ON = 16Bit	MOD4 = 0	SC15 Host I/F bus width configuration. *This switch has effect only if S2-1 and S2-3 are ON*
		OFF = 32Bit	MOD4 = 1	
6	BUS TYPE C Emulation	ON = Type C	Host I/F emulates Type C	SC15 Host I/F type configuration *This switch has effect only if S2-1 and S2-4 are ON.*
		OFF = Type A	Host I/F emulates Type A	
7	VAR LAT WRITE	ON = Dedicated	Dedicated WR2n signal for variable latency	Allows using a dedicated Write signal for variable latency (available only on some platforms). Usually the same WRn signal is used for fixed and variable latency (let switch to OFF). *This switch has effect only if S2-1 and S2-4 are ON*
		OFF = Standard	Single WRn signal for fixed and variable latency	
8	INDIRECT ADDR/DATA CONTROL	ON = A1	Host A1 is the address/data control	SC15-A2 configuration in indirect mode. It can be controlled by Host A1 or A2.
		OFF = A2	Host A2 is the address/data control	

Generic Input states are controlled through switch bank S4, shown in Figure 5.1.

Table 5.3: Switch Bank S4: Generic Switch IOs

	Name	Configuration	Description	Switch Function
1	INPUT SWITCH 1	ON = High	U520 bit 1.4 = 1	General Input Switch HW control *This switch has an effect only if U520-1.4 is configured as an input.*
		OFF = Low	U520 bit 1.4 = 0	
2	INPUT SWITCH 2	ON = High	U520 bit 1.5 = 1	General Input Switch HW control *This switch has an effect only if U520-1.5 is configured as an input.*
		OFF = Low	U520 bit 1.5 = 0	
3	INPUT SWITCH 3	ON = High	U520 bit 1.6 = 1	General Input Switch HW control *This switch has an effect only if U520-1.6 is configured as an input.*
		OFF = Low	U520 bit 1.6 = 0	
4	INPUT SWITCH 4	ON = High	U520 bit 1.7 = 1	General Input Switch HW control *This switch has an effect only if U520-1.7 is configured as an input.*
		OFF = Low	U520 bit 1.7 = 0	
5	NOT USED	N/A		
6	NOT USED	N/A		
7	NOT USED	N/A		
8	NOT USED	N/A		

Use switch bank S5 to configure host bus address mapping, deep power down (DPD_), and voltage control states for HVDD and video.

Table 5.4: Switch Bank S5: Miscellaneous Control

	Name	Configuration	Description	Switch Function
1	ADDR MAP CTRL 0	ON = No Remap	Host A23 remains A23	Used to control address mapping from PCI adapter. *This switch has an effect only if U518 interface 0 is disabled as an output.*
		OFF = Remap	Host Interface A23 is set to 0 and A23 is passed to A25.	
2	ADDR MAP CTRL 1	ON = No Remap	Host A24 remains A24	Used to control address mapping from PCI adapter. *This switch has an effect only if U518 interface 0 is disabled as an output.*
		OFF = Remap	Host Interface A24 is set to 0.	
3	ADDR MAP CTRL 2	ON = No Remap	U520 bit 1.6 = 1	Used to control address mapping from PCI adapter. *This switch has an effect only if U518 interface 0 is disabled as an output.*
		OFF = Remap	U520 bit 1.6 = 0	
4	DPD_ DISABLE	ON = Enabled	N/A	Used to put the chip in Deep Power Down *This switch has an effect only if U518 interface 0 is disabled as an output.*
		OFF = Disabled		
5	CTRL HVDD	ON = Disable PCI Board HVDD power	Turns Host power (from the PCI board) On and Off	*This switch has an effect only if U518 interface 0 is disabled as an output.*
		OFF = Enable PCI Board HVDD power		
6	VIDEO POWER ENABLE	N/A	TBD, Not used yet	*This switch has an effect only if U518 interface 0 is disabled as an output.*
7	NOT USED	N/A		
8	NOT USED	N/A		

5.2 Software Configuration

Software configuration and control of the SC15 Evaluation Board is implemented primarily over the I2C bus.

5.2.1 I2C/SPB Address Map

Table 5.5 gives the I2C Address Mapping. (I2C is sometimes also called SPB in other SC15 documentation.) The following tables give details for specific I2C address locations.

Table 5.5: SPB Address Map

SPB Address	Function	Device	Reference
0x36h	I2S Audio	Wolfson WM8731 CODEC	U526
0x40h	Host modes and LEDs	PCA9555 I2C Expander	U520
0x44h	Video Control and GPIOs	PCA9555 I2C Expander	U507
0x46h	Address Remap and Miscellaneous Power Controls	PCA9555 I2C Expander	U518
0x60h	Onboard camera	Omnivision 9650	J19
0x80h	IO and Auxiliary Power Controller	Summit SMB120	U505
0x84h	Core Power Controller	Summit SMB113	U26
0x88h	IO Power Controller	Summit SMB113	U504
0xA0h	SC15 WMP Module ID EEPROM	Microchip 24LC024	WMP Module
0xA2h	EVAL3 Module ID EEPROM	Microchip 24LC024	U15
0xAEh	LCD Module ID EEPROM	Microchip 24LC024	LCD Module
0xB0h	Sysclk PLL	AMI FS7140	U7
0xEAh	PC to TV Encoder	Chrontel CH7013B	U3
TBD	Generic Camera Module	TBD	TBD

Table 5.6: 0x40h: Host Mode Details

0x40h	Name	Direction	Description	I/O Function
Port 0				
P0-0	MODE BIT 0	Output	Set inverted value of SC15 MD0 pin. This control has effect only if S2-1 and S2-2 are OFF	1 = Active Low Handshake 0 = Active High Handshake
P0-1	MODE BIT 1	Output	Set inverted value of SC15 MD1 pin. This control has effect only if S2-1 and S2-2 are OFF	1 = No Handshake Mode 0 = Handshake Mode
P0-2	MODE BIT 2	Output	Set inverted value of SC15 MD2 pin. This control has effect only if S2-1 and S2-2 are OFF	1 = Direct Addressing 0 = Indirect Addressing
P0-3	MODE BIT 3	Output	Set inverted value of SC15 MD3 pin. This control has effect only if S2-1 and S2-2 are OFF	1 = Asynchronous Mode 0 = Synchronous Mode
P0-4	HOST BUS WIDTH	Output	Set host interface bus controls for appropriate bus width. This control has effect only if S2-1 and S2-2 are OFF	1 = 16Bit Addressing 0 = 32Bit Addressing
P0-5	HOST BUS TYPE	Output	Set host interface bus controls for appropriate bus type. This control has effect only if S2-1 and S2-2 are OFF.	1 = Type C Host Bus 0 = Type A Host Bus
P0-6	WRITE SELECT	Output	Select Write Enable from one of two host interface pins. This control has effect only if S2-1 and S2-2 are OFF.	1 = Set WE_ to Pin 32 of Host interface connector. 0 = Set WE_ to Pin 22 of Host interface connector.
P0-7	SYSTEM RESET	Output	Create a 10 ms system reset. This control has effect only if S2-1 and S2-2 are OFF	1 = Re-arm Reset Trigger 0 = Generate Reset Pulse

Table 5.7: 0x40h: LED Status and Switch Details

0x40h	Name	Direction	Description	I/O Function
Port 1				
P1-0	STATUS LED 0	Output	Control LED DS4	1 = LED Off 0 = LED On
P1-1	STATUS LED 1	Output	Control LED DS3	1 = LED Off 0 = LED On
P1-2	STATUS LED 2	Output	Control LED DS2	1 = LED Off 0 = LED On
P1-3	STATUS LED 3	Output	Control LED DS1	1 = LED Off 0 = LED On
P1-4	INPUT SWITCH 1	Input	Read value of S4-SW1	1 = SW Input On 0 = SW Input Off
P1-5	INPUT SWITCH 2	Input	Read value of S4-SW2	1 = SW Input On 0 = SW Input Off
P1-6	INPUT SWITCH 3	Input	Read value of S4-SW3	1 = SW Input On 0 = SW Input Off
P1-7	INPUT SWITCH 4	Input	Read value of S4-SW4	1 = SW Input On 0 = SW Input Off

Table 5.8: 0x44h: Video GPIO Details

0x44h	Name	Direction	Description	I/O Function
Port 0				
P0-0	VGP0	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-1	VGP1	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-2	VGP2	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-3	VGP3	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-4	VGP4	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-5	VGP5	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-6	VGP6	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low
P0-7	VGP7	Input/Output	User Defined I/O passed to Generic Camera Connector J30	1 = Logical High 0 = Logical Low

Table 5.9: 0x44h: Miscellaneous GPIOs and Video Control Details

0x44h	Name	Direction	Description	I/O Function
Port 1				
P1-0	MGPIO0	Input/Output	User Defined I/O passed to Test point TP9 for miscellaneous control applications.	1 = Logical High 0 = Logical Low
P1-1	MGPIO1	Input/Output	User Defined I/O passed to Test point TP6 for miscellaneous control applications.	1 = Logical High 0 = Logical Low
P1-2	MGPIO2	Input/Output	User Defined I/O passed to Test point TP10 for miscellaneous control applications.	1 = Logical High 0 = Logical Low
P1-3	MGPIO3	Input/Output	User Defined I/O passed to Test point TP7 for miscellaneous control applications.	1 = Logical High 0 = Logical Low
P1-4	MGPIO4	Input/Output	User Defined I/O passed to Test point TP11 for miscellaneous control applications	1 = Logical High 0 = Logical Low
P1-5	MGPIO5	Input/Output	User Defined I/O passed to Test point TP8 for miscellaneous control applications.	1 = Logical High 0 = Logical Low
P1-6	Video Shutter	Output	Shutter control output that is passed to Generic Camera Interface J30.	1 = Logical High 0 = Logical Low
P1-7	Video Reset	Output	Video Reset control output that is passed to Generic Camera Interface J30.	1 = Logical High 0 = Logical Low

Table 5.10: 0x46h: Address Mapping and Miscellaneous Power

0x46h	Name	Direction	Description	I/O Function					
Port 0									
P0-0	ADDR MAP CTRL 0 (AM0)	Output	Remap A23, A24 and A25. This control has effect only if S4-1 is set to OFF	**ADDR CTRL ****					
				AM2	AM1	AM0	A25	A24	A23
P0-1	ADDR MAP CTRL 1 (AM1)	Output	Remap A23, A24 and A25. This control has effect only if S4-2 is set to OFF	0	X	0	0	0	0
				X	X	1	A25	A24	A23
P0-2	ADDR MAP CTRL 2 (AM2)	Output	Remap A23, A24 and A25. This control has effect only if S4-3 is set to OFF	1	X	0	A23	0	0
P0-3	DPD_	Output	Set DPD Mode On or Off This control has effect only if S4-4 is set to OFF	1 = Disables DPD_					
				0 = Enables DPD_					
P0-4	CONTROL HVDD	Output	This control has effect only if S4-5 is set to OFF	1 = Enables PCI board regulator					
				0 = Disables PCI board regulator					
P0-5	VIDEO I/O ENABLE	Output	Enable the Camera Module Video IO voltage This control has effect only if S4-6 is set to OFF	1 = Enables Voltage					
				0 = Disables Voltage					
P0-6	SPARE	Input	Takes input from S5.7	1 = Switch On					
				0 = Switch Off					
P0-7	SPARE	Input	Takes input from S5.7	1 = Switch On					
				0 = Switch Off					

** Default Condition:

- AM2 = 0
- AM1 = X
- AM0 = 1
- A25 = 0
- A24 = 0
- A23 = 0

Table 5.11: 0x46h: Address Mapping and Miscellaneous Power

0x46h	Name	Direction	Description	I/O Function
Port 1				
P1-0	SUMMIT POWER ENABLE 1	Output	Generic Power Enable for Summit Core Voltage	1 = Logical High
				0 = Logical Low
P1-1	SUMMIT POWER ENABLE 2	Output	Generic Power Enable for Summit Core Voltage	1 = Logical High
				0 = Logical Low
P1-2	PWR GPIO 0	Input/Output	User-defined I/O passed to Power Module	1 = Logical High
				0 = Logical Low
P1-3	PWR GPIO 1	Input/Output	User-defined I/O passed to Power Module	1 = Logical High
				0 = Logical Low
P1-4	POWER HEALTHY	Input	Power good indication from the power subsystem.	1 = Power Good
				0 = Power Fault
P1-5	AC'97 AUDIO RESET	Output	Resets the AC97 Audio CODEC.	1 = Normal Operation
				0 = Resets Audio
P1-6	EXT HVDD OFF	Input	Indicates if external HVDD is present.	1 = External HVDD Off
				0 = External HVDD On
P1-7	EFUSE BURN TRIG-GER	Output	Trigger signal passed to SC15 module to trigger EFUSE burn sequence.	1 = Logical High
				0 = Logical Low

Table 5.12: 0x40h: Miscellaneous Control

U27	Name	Configuration	Description	Bit Function
IO-0.0	CRTL_MD0	0	MD0 = 0	SC15 MOD0 pin is under software control Set S2-1 to OFF
		1	MD0 = 1	
IO 0.1	CRTL_MD1	0	MD1 = 0	SC15 MOD1 pin is under software control Set S2-1 to OFF
		1	MD1 = 1	
IO 0/2	CRTL_MD2	0	MD2= 0	SC15 MOD2 pin is under software control Set S2-1 to OFF
		1	MD2 = 1	
IO 0.3	CRTL_MD3	0	MD3 = 0	SC15 MOD3 pin is under software control Set S2-1 to OFF
		1	MD3 = 1	
IO 0.4	CTRL_32_16	0	Host I/F is 16bit mode	SC15 Host I/F bus width configuration Set S2-1 to OFF
		1	Host I/F is 32bit mode	
IO 0.5	CTRL_TYPE_C	0	Host I/F is Type C Emulation	SC15 Host I/F Type configuration Set S2-1 to OFF
		1	Host I/F is Type A Emulation	
IO 0.6	CTRL_WR_LAT	0	Dedicated WR_ signal for variable latency	Allows using a dedicated Write signal for variable latency (available only on some platforms). Usually the same WRn signal is used for fixed and variable latency (let switch to OFF). Set S2-1 to OFF
		1	SIngle WR_ signal for fixed and variable latency	
IO 0.7	I2C_RESET	Falling edge	Create a low pulse reset on SC15	SW Reset of the board

Use specific U30 bits to control the Evaluation board when plugged on to the NVIDIA PCI board (PCI32B-BCA2), which provides only 24 address bits. The address MSB (A23) gets shifted to access the complete SC15 mapping, which requires 26 address bits.

Table 5.13: U30 Bits for Configuration to Old PCI Board

PCI Board	U30			Description
	IO_0.0	IO_0.1	IO_0.2	
"Old" PCI32B-BCA2	0	1	0	A23 from Host is shifted to A25 of SC15, A[24:23] on SC15 are switched to ground
Current PCI32B-BCA5	1	X	1	Complete address mapping is managed by the Host (A[25:0])

5.2.2 Modes Summary

This section summarizes the manual and auto modes.

5.2.2.1 Manual Mode

In manual mode, use the switch positions for SW3 and SW4 shown in Table 5.14 for different host I/F modes.

Table 5.14: U30 Bits for Configuration to Old PCI Board

Latency	Switch	Mode	Position
	SW3-1		On
	SW3-2		On
	SW3-3		On
	SW3-4		On
Fixed	SW4-1		On
	SW4-2		On
Ready Low	SW4-1		On
	SW4-2		Off
Ready High	SW4-1		Off
	SW4-2		Off
	SW4-3	Direct	On
		Indirect	Off
	SW4-4	Asynchronous	On
		Synchronous	Off
	SW4-5	16 Bit	On
		32 Bit	Off
	SW4-6	Type A	Off
		Type C	On

5.2.2.2 Auto Mode

Use the swtich positions of SW3 and outputs of U27 (the GPIO expander) in Table 5.15 for the different host I/F modes when using Auto Mode.

Table 5.15: U30 Bits for Configuration to Old PCI Board

Latency	Switch/Bit	Mode	Position/Output	
	SW3-1		Off	On
	SW3-2		X	Off
	SW3-3		X	Off
	SW3-4		X	Off
Fixed	U27_0.0		0	
	U27_0.1		0	
Ready Low	U27_0.0		0	
	U27_0.1		1	
Ready High	U27_0.0		1	
	U27_0.1		1	
	U27_0.2	Direct	0	
		Indirect	1	
	U27_0.3	Asynchronous	0	
		Synchronous	1	
	U27_0.4	16 Bit	0	
		32 Bit	1	
	U27_0.5	Type A	1	
		Type C	0	

5.3 Jumpers

Table 5.16: Clock Source Selection Jumper Configurations

Jumper	Control	Position	Description
J7	Refclk1 Source	1 - 4	I2C clock generator U29
		2 - 5	Oscillator 13 MHz
		3 - 6	Chrontel pixel clock
J16	SC15 External Clock sources: Sysclk and Refclk0	1 - 2	I2C Clock Generator (U29)
		2 - 3	Oscillator (13 MHz)
		Open (No Jumper)	Use only when a 3.6864 MHz crystal is mounted on the SC15 Module.
J17	Camera Master Clock	1 - 2	SC15 (VSMCLK) generates the camera clock
		2 - 3	Oscillator socket

Table 5.17: I2S/AC'97 Selection Jumper Configurations

Jumper	Control	Position	Description
J14/J15	Line in select	1 - 2	I2C
		2 - 3	AC'97
J10/J11	Microphone select	1 - 2	I2S
		2 - 3	AC'97
J9/8	Line out select	1 - 2	I2S
		2 - 3	AC'97
J16/J17/J18	Codec interface select	1 - 2	I2S
		2 - 3	AC'97

Table 5.18: SRCLOCK Frequency Select

Jumper	Control	Position	Description
J40	SRCLK_GEN	1 - 2	SRCLK_GEN source: S0 of ICS661 (U28)
J42	SRCLK_GEN	1 - 2	SRCLK_GEN source: S1 of ICS661 (U28)
J44	SRCLK_GEN	1 - 2	SRCLK_GEN source: S2 of ICS661 (U28)
J46	SRCLK_GEN	1 - 2	SRCLK_GEN source: S3 of ICS661 (U28)

5.4 Clock Headers

Table 5.19: Clock Headers

Jumper	Control	Position	Description
JP1	REFCLK0	1	Header for oscillator
JP2	NC	1	Header for oscillator
JP3	CLK	1	Header for oscillator
JP4	HGPIO5	1	Header for oscillator
JP5	HGPIO6	1	Header for oscillator

Chapter 6 Software Mapping

6.1 Software Mapping

Table 6.1 gives I^2C addresses for different devices.

Note: Digital potentiometer devices cannot be read back on I^2C.

Table 6.1: I2C Mapping for Different Devices

Device	Type	Reference	I2C Address	Description
PCA9555	GPIO Expander	U520	0100000	Modes, LEDs, Switches
		U518	0100001	Aux Controls, DPDn, Address Remap
		U507	0111000	Spare GPIO for the camera board
FS7140	Clock generator	U7	1011000	SC15 external clock (OSCFO), usually 13 MHz from Baseband J16 must be on 1-2 position to use this clock on SC15
24LC024	EEPROM	U14	1010001	Remote inventory (Board configuration summary)
SMB120	Voltage regulator	TBD	1000000	SC15 IO power
SMB113	Voltage regulator	TBD	1000010	SC15 Core power
		TBD	1000100	SC15 IO power
CH7013	SVideo out	TBD	1110101	Wolfson I2S Codec
24LC024			TBD	SC15 Module EEProm
24IC024			TBD	LCD Module EEProm

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Chapter 7 SC15 Module

7.1 Introduction

The SC15 Module holds the SC15, external components, and headers for routing SC15 signals to the Evaluation Board.

The key components on the module are

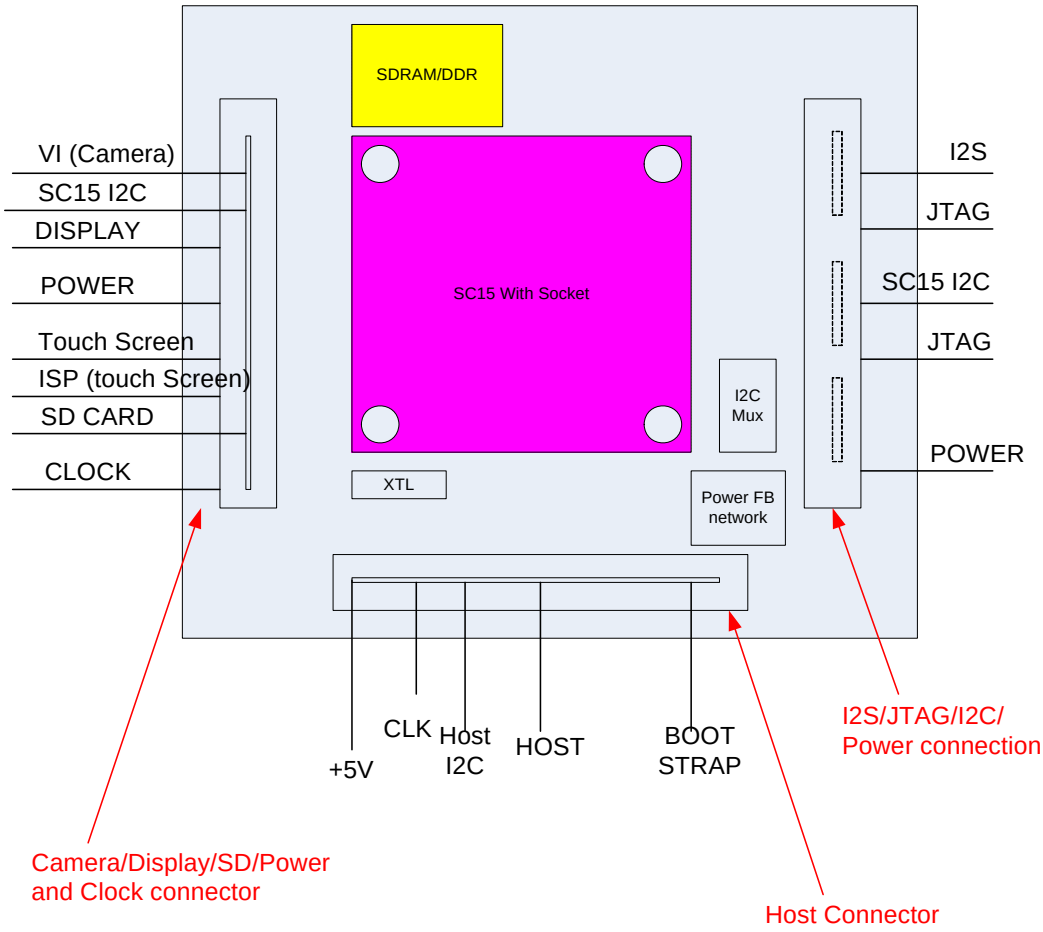
- SC15
  - No additional memory
  - 2MB additional memory
  - 8MB additional memory
- SC15 BGA 0.5mm pitch socket (optional for initial lab/software development)
- Crystal for the SC15 clock.
- Samtec 0.5mm Headers
  - all SC15 I/O signals to applicable boards (such as the Evaluation Board)
  - no signals going through these headers go to the memory interface.
- I2C PROM for module identification, can be interrogated by the Host I2C
- Test Points to monitor rail voltages
- MICTOR on memory I/F for Debug (option for 2MB and 8MB memories configurations)

NVIDIA part numbers

- 600-80436-0002-100 PCB Assembly for SC15-NM Modules
- 600-80436-0000-100 PCB Assembly for SC15-8ME modules
- 600-80438-001-000: SC15 with 640KB eSRAM and additional, external DDR memory

Figure 7.1 depicts the SC15-NM module.

Figure 7.1: SC15-NM Module Block Diagram



7.2 SC15 Module Components

The SC15Wireless Media Processor (WMP) has the following key features:

- Camera interface with support for 8bit ITU-R BT656 YUV or 10/12 bit RAW data format up to 96MHz data rate (3M Pix sensor @ 15fps).
- Host interface
  - direct and indirect interface
  - x16 and x32 bit data bus

- LCD FP interface with support up to 18bit RGB or 1or 2 channel serial interface
- External X32 bit Mobile SDRAM or mobile DDR SDRAM interface
- SD card interface
- Audio I2S or AC'97 interface support
- I2C serial interface used to communicate with camera for adjustments
- GPIOs
- Separate I/O Power and isolated core power

7.3 SC15 Module Interface Details

The module contains the SC15 with all interfaces routed to headers with the exception of the crystal clock pins and SDRAM/DDSDRAM, where appropriate.

Interfaces supported by SC15 family of devices

- Host
  The host interface functional block in the SC15 has the following features
  - Type A or Type C host interfacing with fixed or variable latency
  - 16Bit or 32bit data bus width
  - Asynchronous and synchronous support
  - Direct and Indirect address mapping supported along with
    - fixed cycle
    - ready handshake
    - wait handshake access
  - SC15 reset is supplied by the Eval Board as a system reset
- SDRAM/DDR
  - The modules support either
    - No external memory (Internal RAM only)
    - 2MB External Memory
    - 8MB External Memory
- SD
  - SD and SDIO support
  - The SD detect pin connection TBD and may be routed on the base board to the Host GPIO.
- I2S/AC'97
  - Full-duplex synchronous serial channel interface to an external codec.
  - Support for AC'97 and I2S.
  - Programmable FSYNC and SCLK polarity, stop value, direction
  - FSYNC dividers up to 256
- Video input
  - Interface supports YUV or Bayer
  - Designed to interface to camera modules
  - Maximum clock/data rate (interface): 96 MHz
  - I2C control interface for camera control and configuration:
    If used on the base board to drive I2C and the LCD, may require a voltage translator, depending on design criteria and rail voltages.
- I2C
  - Bus master I2C interface -
  - Used to configure the camera and the I2S codec
  - Additional circuitry may be required on the base boards if I2C is routed to other devices with different rail voltages
- Video Output - LCD Interface
  - Support for VGA and QVGA panels.
  - Backward compatible interface with existing panel modules.
  - Forward compatible interface for new SC15-based panel interface signaling.
- Oscillator
  - On-board crystal or
  - Clock sourced from base board
  - Jumper configuration switches between the two

- Power Supply
  - I/O supply tolerance to be better than +/-10%, respective to rail voltage
  - The regulation tolerance between any of the core power supplies to be better or equal to +/-5%
  - Core power to be adjustable in <20 mV steps particularly for the Eval/bring-up phase
  - Power supply feed back (FB signals) are routed to the headers for tight control of the power tolerance and control on the base board
  - All power supplies on the modules to be de-coupled adequately to minimize impedance, improve transient response and suppress power supply noise.

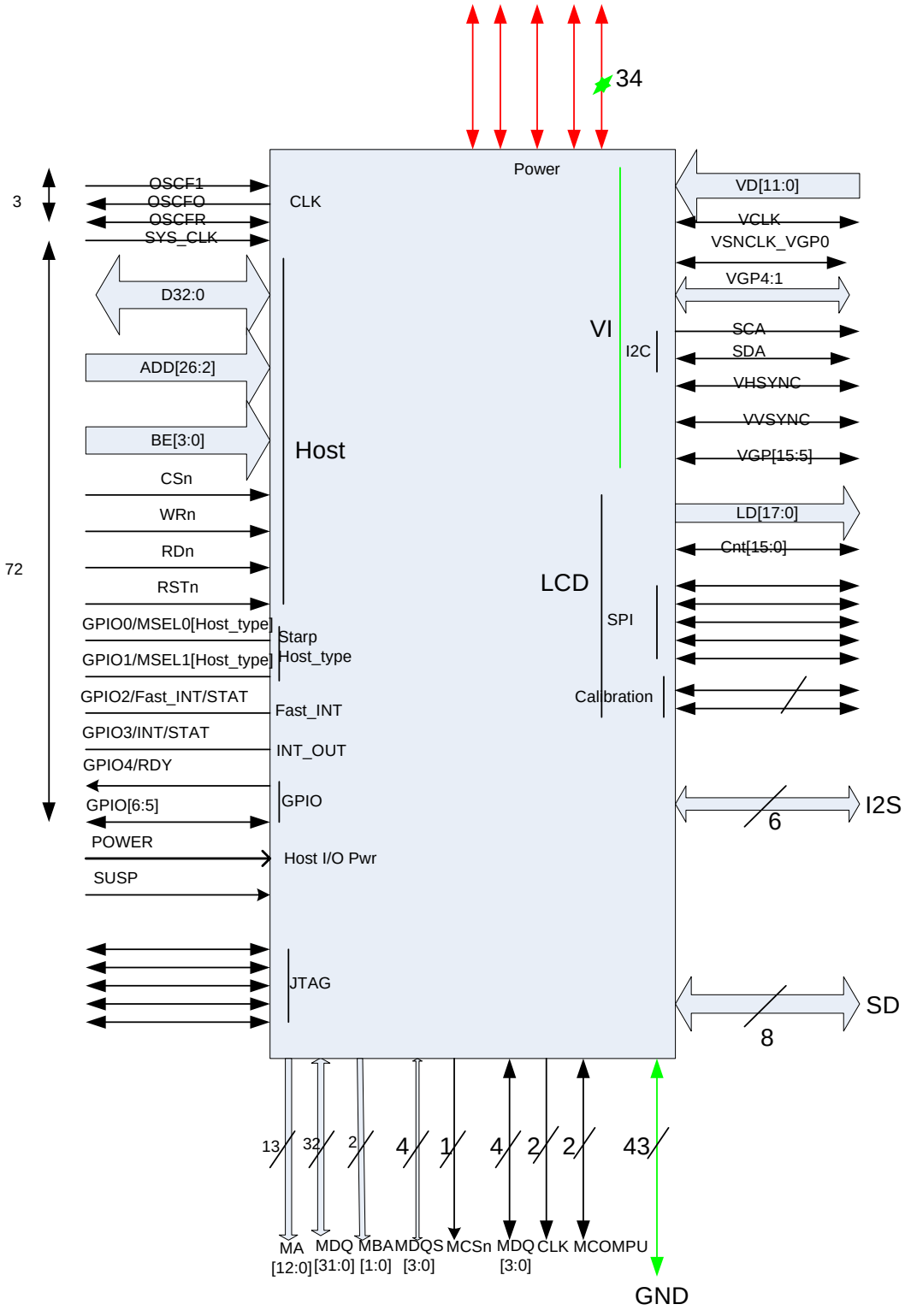
- Boot Strap Pins
  - SC15 Host type select and bus width support select pins routed to the headers. The base board must tie these pins to the appropriate logic level - see SC15 data sheet for option.

- E2PROM
  - E2PROM on the module is connected to the Host I2C to provide module configuration data.

- GPIO
  - Test points on all GPIO pins as well as all GPIOs routed to the header to the base board

Figure 7.2 depicts the SC15 connections to external peripheral devices. All I/O, power, and control (except the memory interface) are routed through the headers to the base card.

Figure 7.2: SC15-NM Module I/Os Block Diagram



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Chapter 8 LCD Module Description

8.1 Introduction

The SC15 LCD Module enables the designer to view 2D and 3D graphics while evaluating the SC15 in design. Figure 8.1 shows the location of the module on the evaluation board; Figure 8.2 gives signal pin-out information.

Figure 8.1: LCD Module on the Evaluation Board

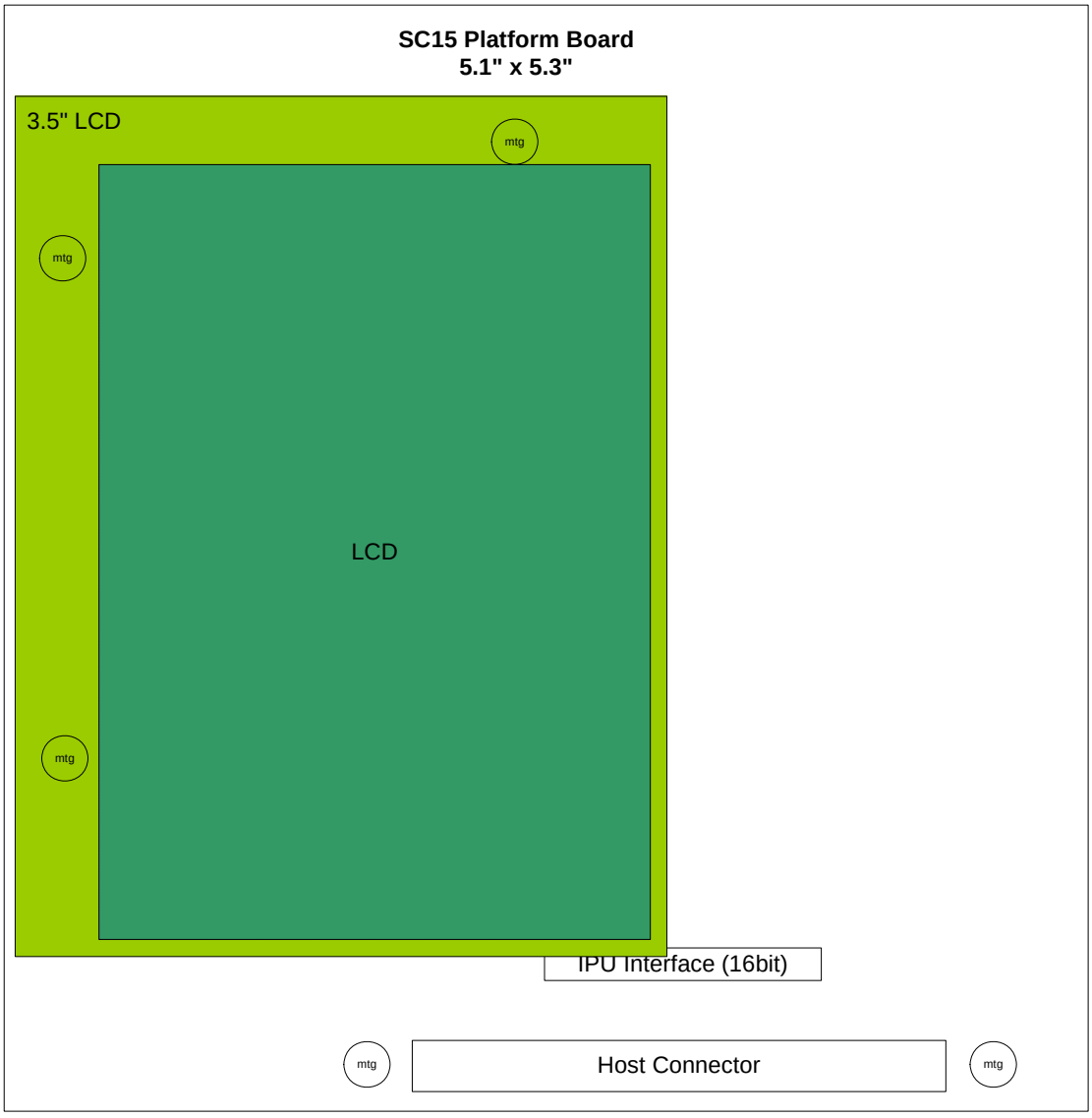


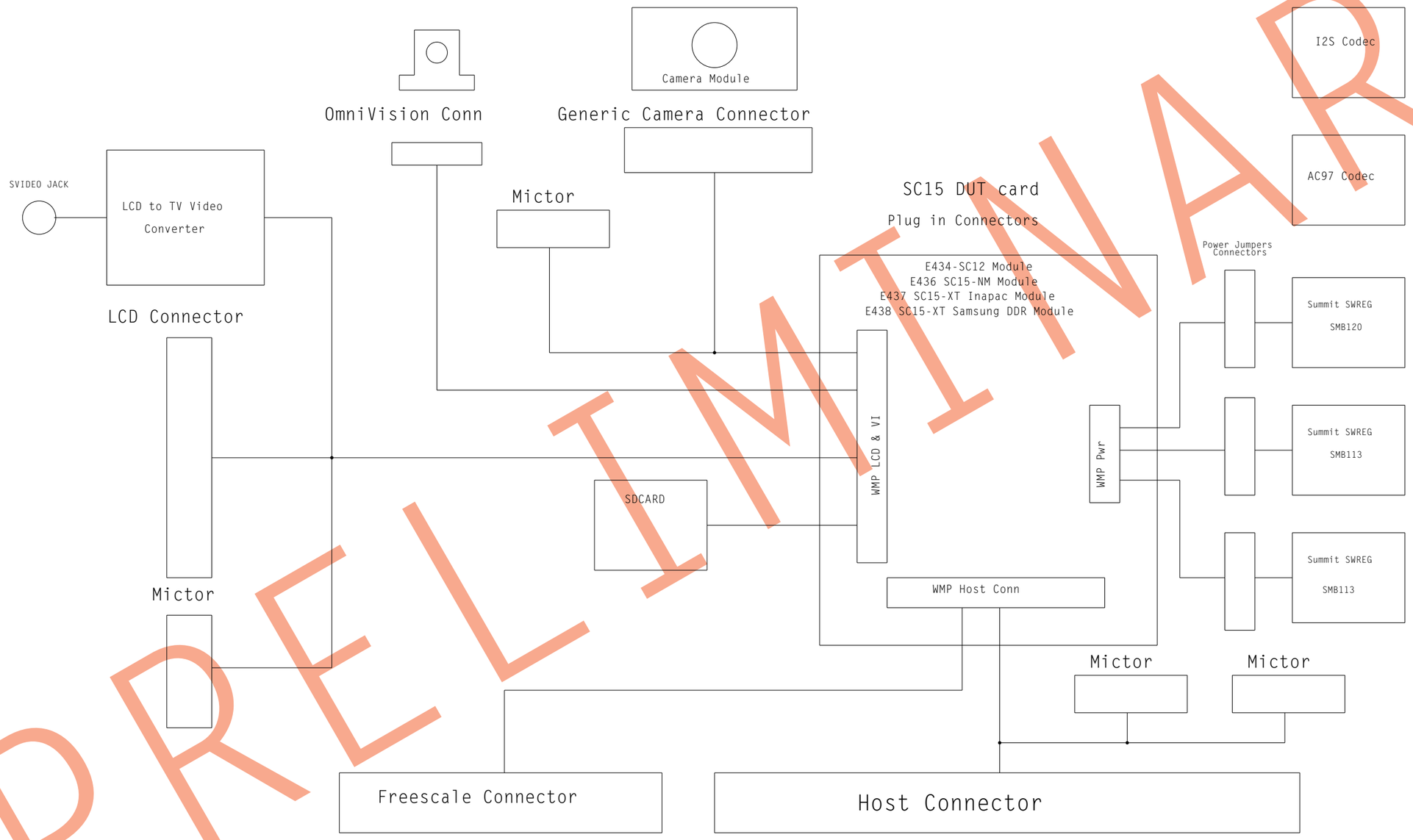
Figure 8.2: LCD Module Connector Pin-to-signal Configuration

Description/notes	SC15 Signal	SC15 I/O Name	New LCD Connector: Conn Pin Name	Pin #	Power Blade	Pin#	Conn Pin Name	SC15 I/O Name	SC15 Signal	Description/Notes
3.3 V from system supply	D3V3	D3V3	D3V3	1		2	SPCK	-	-	
3.3 V from system supply	D3V3	D3V3	D3V3	3	B1-B5	4	SPMOSI	-	-	
3.3 V from system supply	D3V3	D3V3	D3V3	5	GND	6	SPMISO	-	-	
3.3 V from system supply	D3V3	D3V3	D3V3	7	GND	8	SPSSn	-	-	
Serial interface diff clock -	SC*	LD0	**SC***	9	GND	10	**LD18**	LHP1	LD18	LCD Data I/O
Serial interface diff clock +	SC	LD1	**SC**	11	GND	12	**LD19**	LHP2	LD19	LCD Data I/O
Serial interface Data0 -	SD0*	LD2	**SD0***	13	GND	14	**LD0**	LD0	LD0	LCD Data I/O
Serial interface Data0 +	SD0	LD3	**SD0**	15	GND	16	**LD1**	LD1	LD1	LCD Data I/O
Serial interface Data1 -	SD1*	LD4	**SD1***	17	GND	18	**LD2**	LD2	LD2	LCD Data I/O
Serial interface Data1 +	SD1	LD5	**SD1**	19	GND	20	**LD3**	LD3	LD3	LCD Data I/O
Backlight Anode	-	-	**BKLT+**	21	GND	22	**LD4**	LD4	LD4	LCD Data I/O
Panel Control enable	LPW2	LPW2	**LPW2**	23	GND	24	**LD5**	LD5	LD5	LCD Data I/O
Backlight Cathode	-	-	**BKLT-**	25	GND	26	NC26	-	-	
	STH	LD6	**STH**	27	GND	28	**LD20**	LVP1	LD20	LCD Data I/O
Same Dot indication	SDT	LD7	**SDT**	29	GND	30	**LD21**	LM1	LD21	LCD Data I/O
Expansion for panel IO	-	-	**PNLIO0**	31	GND	32	**LD6**	LD6	LD6	LCD Data I/O
	-	-	TSINT	33	GND	34	**LD7**	LD7	LD7	LCD Data I/O
	STP	LD8	**STP**	35	B1-B5	36	**LD8**	LD8	LD8	LCD Data I/O
Serial interface Data2 -	SD2*	LD9	**SD2***	37		38	**LD9**	LD9	LD9	LCD Data I/O
Serial interface Data02 +	SD2	LD10	**SD2**	39	B6-B10	40	**LD10**	LD10	LD10	LCD Data I/O
Panel VDD enable	LPW0	LPW0	**LPW0**	41	FVDD	42	**LD11**	LD11	LD11	LCD Data I/O
Panel VEE enable	LPW1	LPW1	**LPW1**	43	FVDD	44	NC44	-	-	
Main Display Reset	M_RST	LHP2	**M_RST**	45	FVDD	46	**LD22**	LDI	LD22	LCD Data I/O
Display enable	LSC1	LSC1	**LDE**	47	FVDD	48	**LD23**	LPP	LD23	LCD Data I/O
Expansion for panel IO	-	-	**PNLIO1**	49	FVDD	50	**LD12**	LD12	LD12	LCD Data I/O
Horizantal Pulse 0	LHP0	LHP0	**LHP0**	51	FVDD	52	**LD13**	LD13	LD13	LCD Data I/O
Horizantal Pulse 1	LHP1	LHP1	**LHP1**	53	FVDD	54	**LD14**	LD14	LD14	LCD Data I/O
Main panel serial chip select	MSCS	LCS*	**MSCS**	55	FVDD	56	**LD15**	LD15	LD15	LCD Data I/O
Sub panel serial chip select	SSCS	LDI	**SSCS**	57	FVDD	58	**LD16**	LD16	LD16	LCD Data I/O
	LVP1	LVP1	**LVP1**	59	FVDD	60	**LD17**	LD17	LD17	LCD Data I/O
Serial Register Data and Command	SRS_DC	LDC	**SRS_DC**	61	FVDD	62	PWM0	LPW2	PWM0	Sub panel backlight control
Expansion for panel IO	-	-	**PNLIO2**	63	FVDD	64	PWM1	LM1	PWM1	Main panel backlight control
Main panel backlight control (legacy)	PWM0/PWM1	LPW2/LM1	**PWM0/PWM1**	65	FVDD	66	PWM2	LM1	PWM1	Main panel backlight control (legacy)
Expansion for panel IO	-	-	**PNLIO3**	67	FVDD	68	NC68	-	-	
Expansion for panel IO	-	-	**PNLIO4**	69	FVDD	70	CSBO	LHP1	-	Currently Sub Parallel CS. name change?
Expansion for panel IO	-	-	**PNLIO5**	71	FVDD	72	SDAO	LSDA	LSDA	Serial data signal (bidi)
Expansion for panel IO	-	-	**PNLIO6**	73	FVDD	74	SDAI	-	-	
Expansion for panel IO	-	-	**PNLIO7**	75	B6-B10	76	SCLO	LSCK	LSCK	Serial clock
Expansion for panel IO	-	-	**PNLIO8**	77		78	GCS1	LHP2	FGP6	See pin 95 Should be FGP6 or FGP8
PWM clock	LPP	LPP	**LPP**	79	B11-B15	80	GCS2	-	-	
System GPIO	-	-	**SGPIO0**	81	GND	82	**LDI**	LDI	LDI	LCD Data Inversion
Touchscreen X-	-	-	**TSX-**	83	GND	84	**M_RST**	LHP2	M_RST	Main Panel Reset
Touchscreen X+	-	-	**TSX+**	85	GND	86	**SGPIO1**	-	-	System GPIO
Touchscreen Y-	-	-	**TSY-**	87	GND	88	**S_RST**	LVP0	S_RST	Sub Panel Reset
Touchscreen Y+	-	-	**TSY+**	89	GND	90	**SGPIO2**	-	-	System GPIO
General Purpose IO	FGP12	LSPI	LGPIO0	91	GND	92	**LGPIO11**	-	-	Assign an FGP here?
General Purpose IO	FGP10	LPW0	LGPIO1	93	GND	94	**LSC0**	LSC0	LSC0	
General Purpose IO	FGP8	LHP2	LGPIO2	95	GND	96	**LDE**	LSC1	LDE/LSC1	
General Purpose IO	FGP7	LPP	LGPIO3	97	GND	98	**PNLIO_RST**	-	-	Expansion for reset from panel switch
GPIO/Tear Enable	TE	LDC	LGPIO4	99	GND	100	**PNLIO11**	-	-	Expansion for panel IO
GPIO/Parallel Register Data/Command	RS_DC	LVP1	LGPIO5	101	GND	102	**LM0**	LM0	LM0	Main CS for parallel interface. Name change?
Expansion for panel IO	-	-	**PNLIO9**	103	GND	104	**LM1**	LM1	LM1	
Expansion for panel IO	-	-	**PNLIO10**	105	GND	106	**PNLIO12**	-	-	Expansion for panel IO
5 V from system supply	D5V	D5V	D5V	107	GND	108	**LVS**	LVS	LVS	Vertical sync
5 V from system supply	D5V	D5V	D5V	109	GND	110	**LHS**	LHS	LHS	Horizontal Sync
5 V from system supply	D5V	D5V	D5V	111	B11-B15	112	SCL	-	-	
5 V from system supply	D5V	D5V	D5V	113		114	SDA	-	-	

Appendix A Schematics

NOTE: The schematics in this appendix fit pages sized 11" x 17" and can be printed on paper that size for easier viewing.

E433 SC15 Evaluation MainBoard



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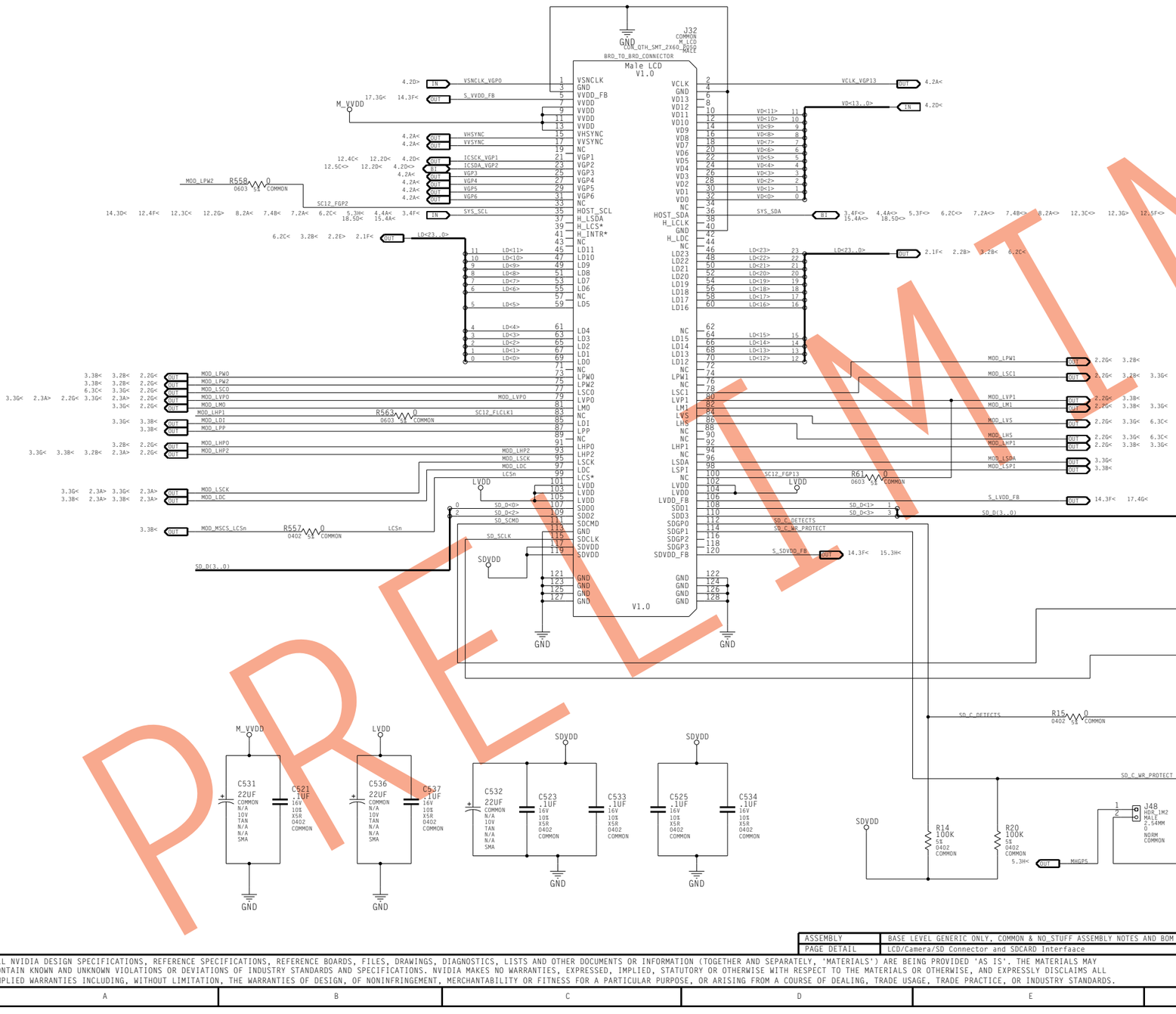
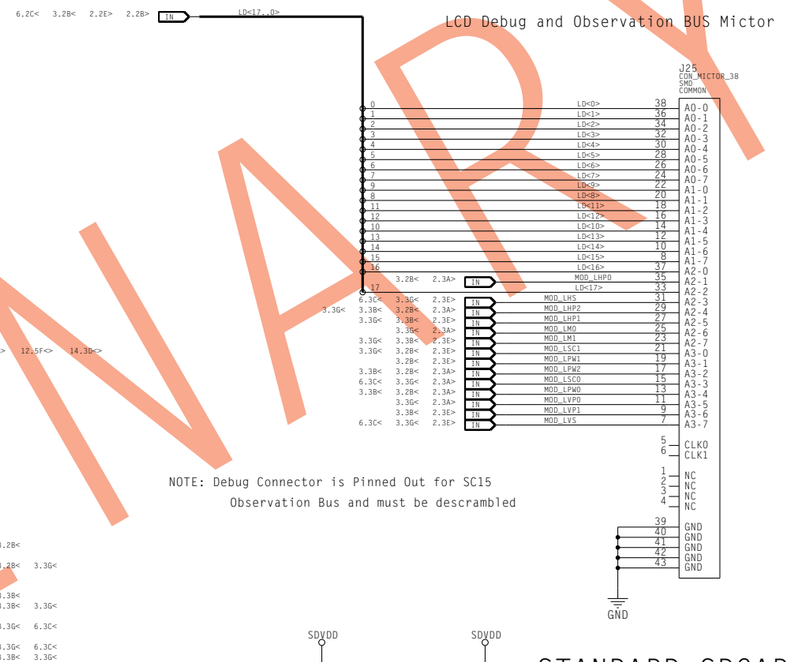
E433 SC15 Evaluation MainBoard

LCD/CAMERA/SD CONNECTOR AND SDCARD INTERFACES

LCD/CAMERA/SD CONNECTOR

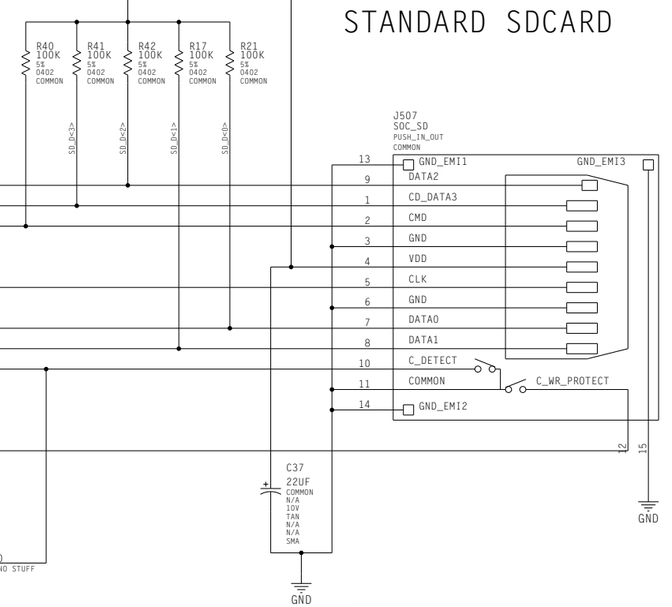


LCD Debug and Observation BUS Mictor



NOTE: Debug Connector is Pinned Out for SC15
Observation Bus and must be descrambled

STANDARD SDCARD



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ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LCD/Camera/SD Connector and SDCARD Interfaace

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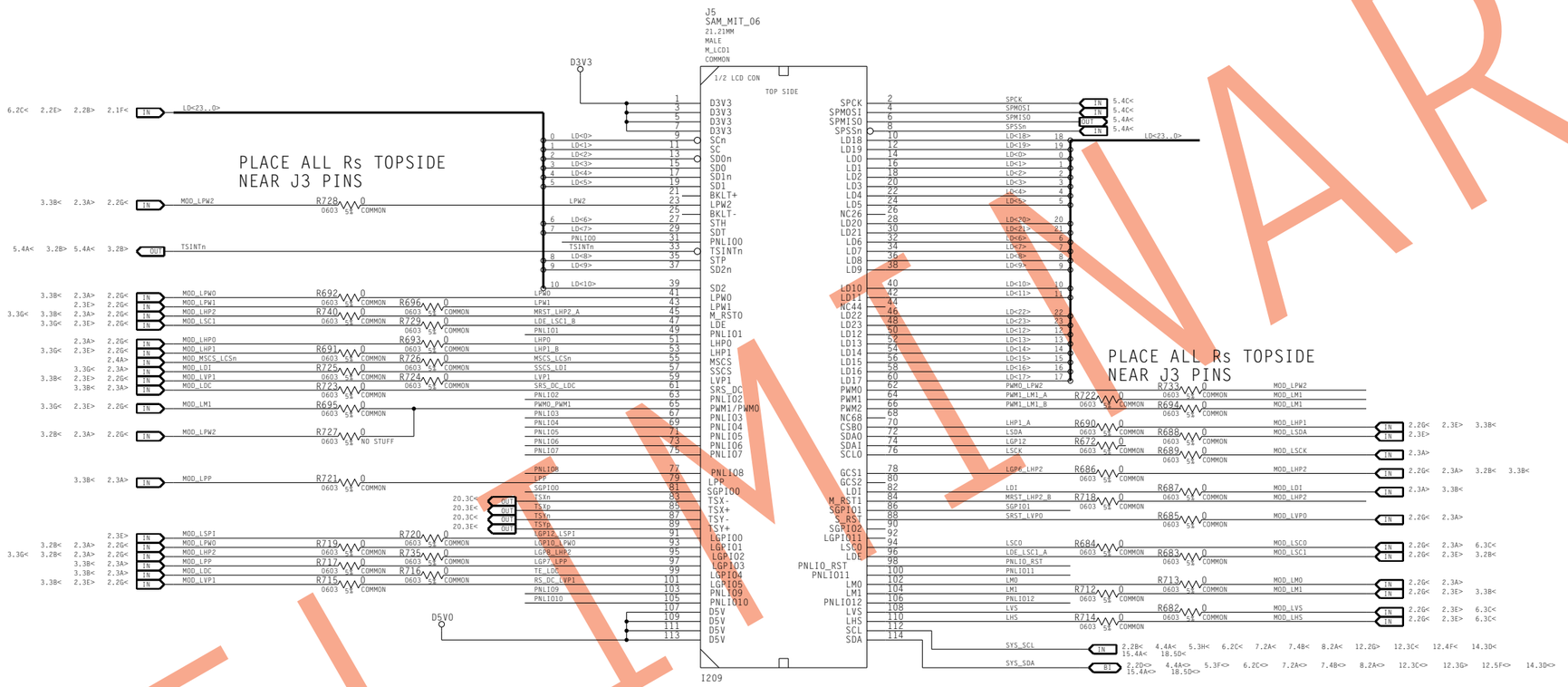
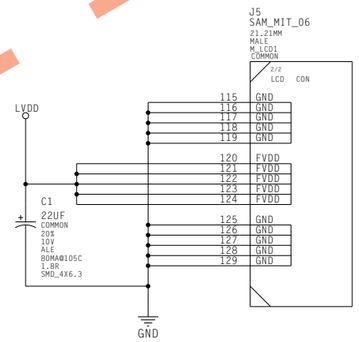
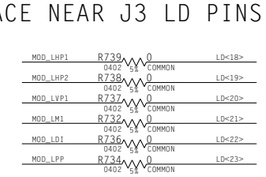
E433 SC15 Evaluation MainBoard

LCD MODULE INTERFACE CONNECTOR







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ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LCD Module Interface Connectors

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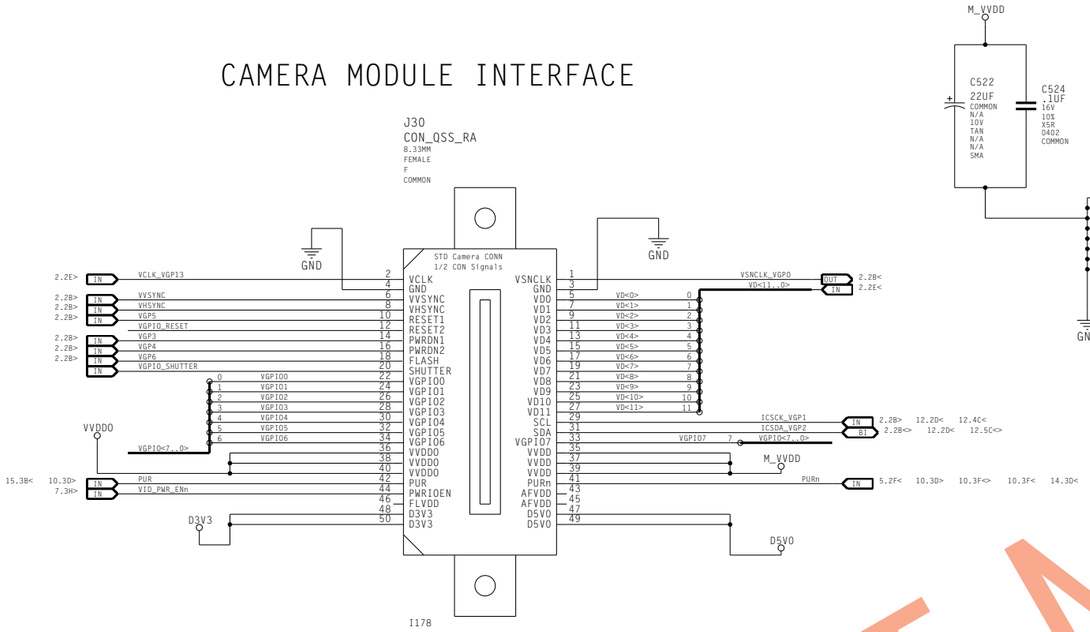
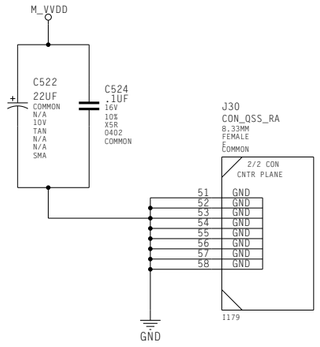
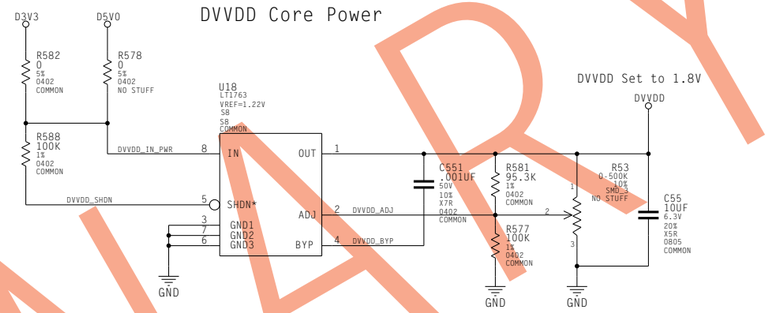
CAMERA CONNECTOR AND MODULE INTERFACE

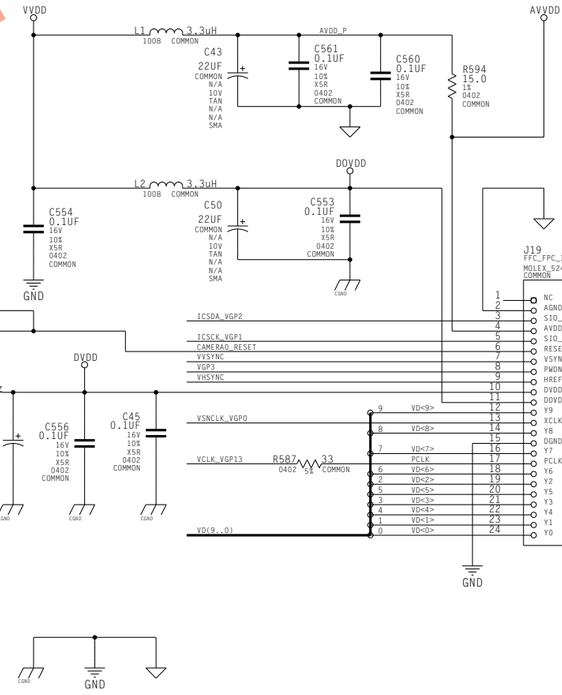
CAMERA MODULE INTERFACE

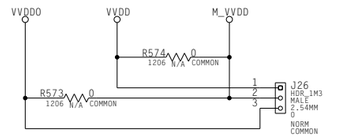


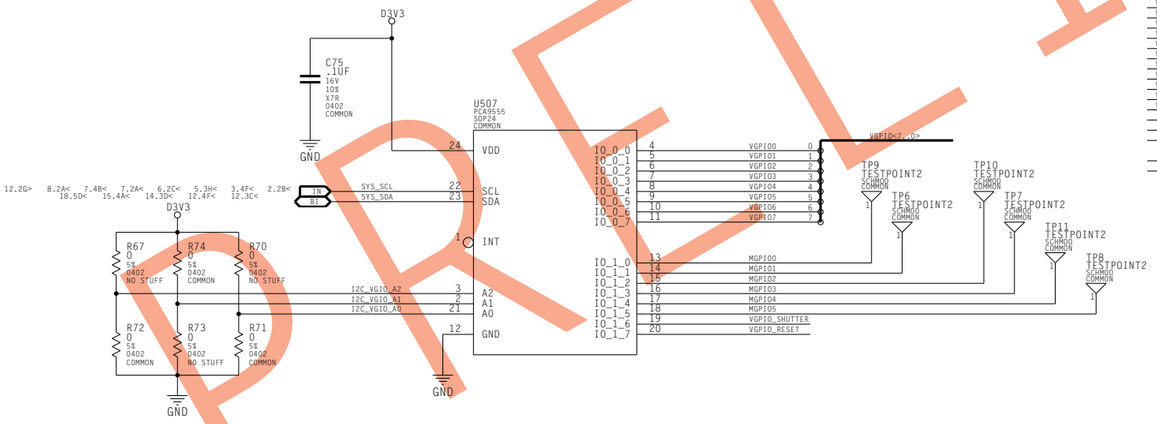


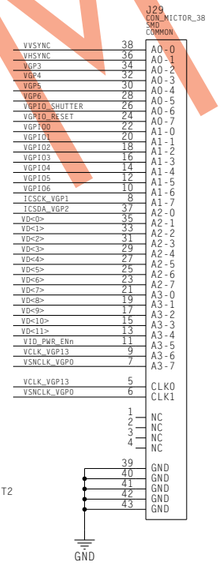


OMNIVISION CAMERA CONNECTOR AND FILTERS









I2C ADDR: 0b0111000

PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Camera Connector and Module Interface

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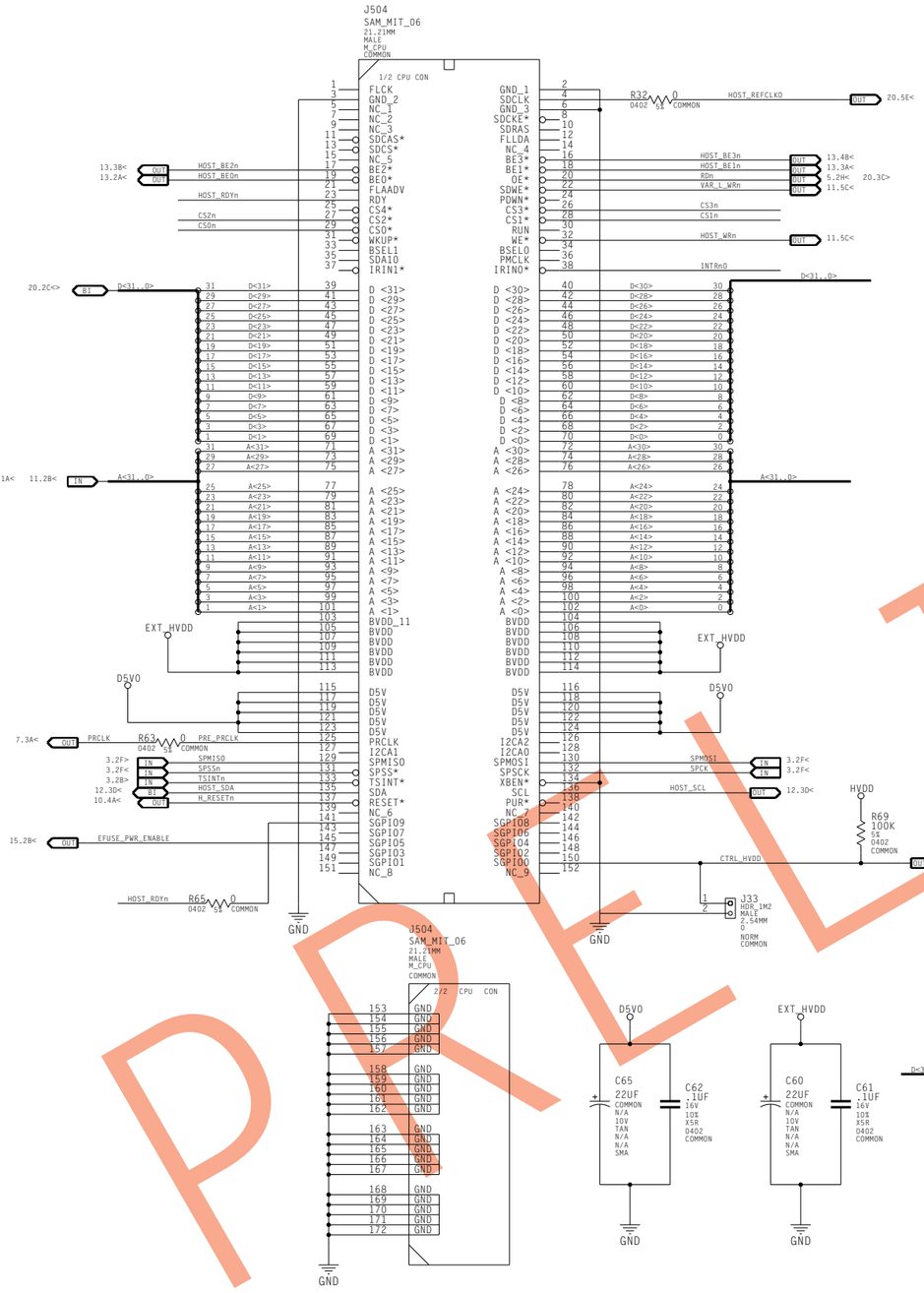
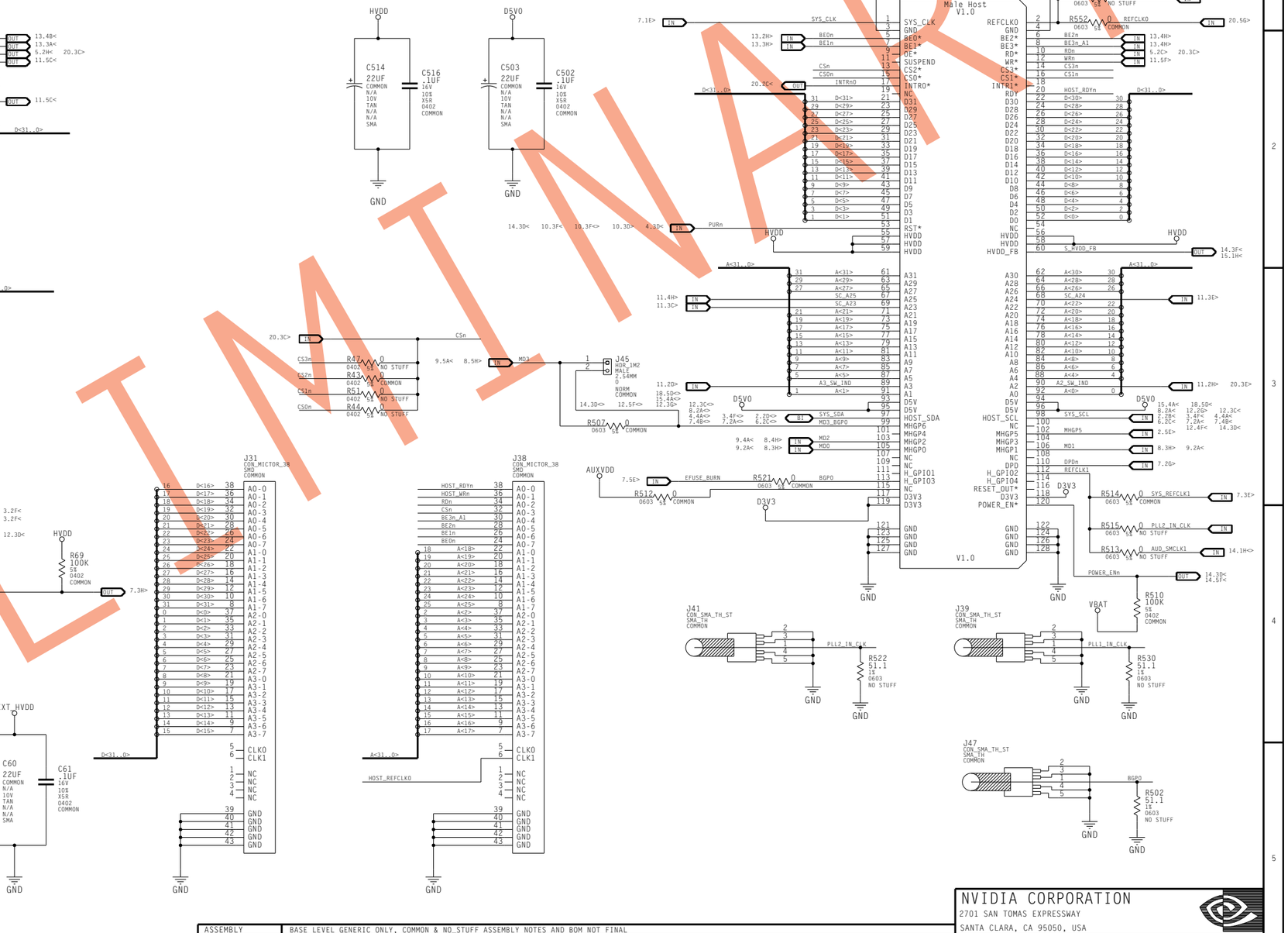
E433 SC15 Evaluation MainBoard

HOST INTERFACE AND CONNECTOR

HOST INTERFACE CONNECTOR



WMP HOST CONNECTOR



PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Host Interface and Connectors

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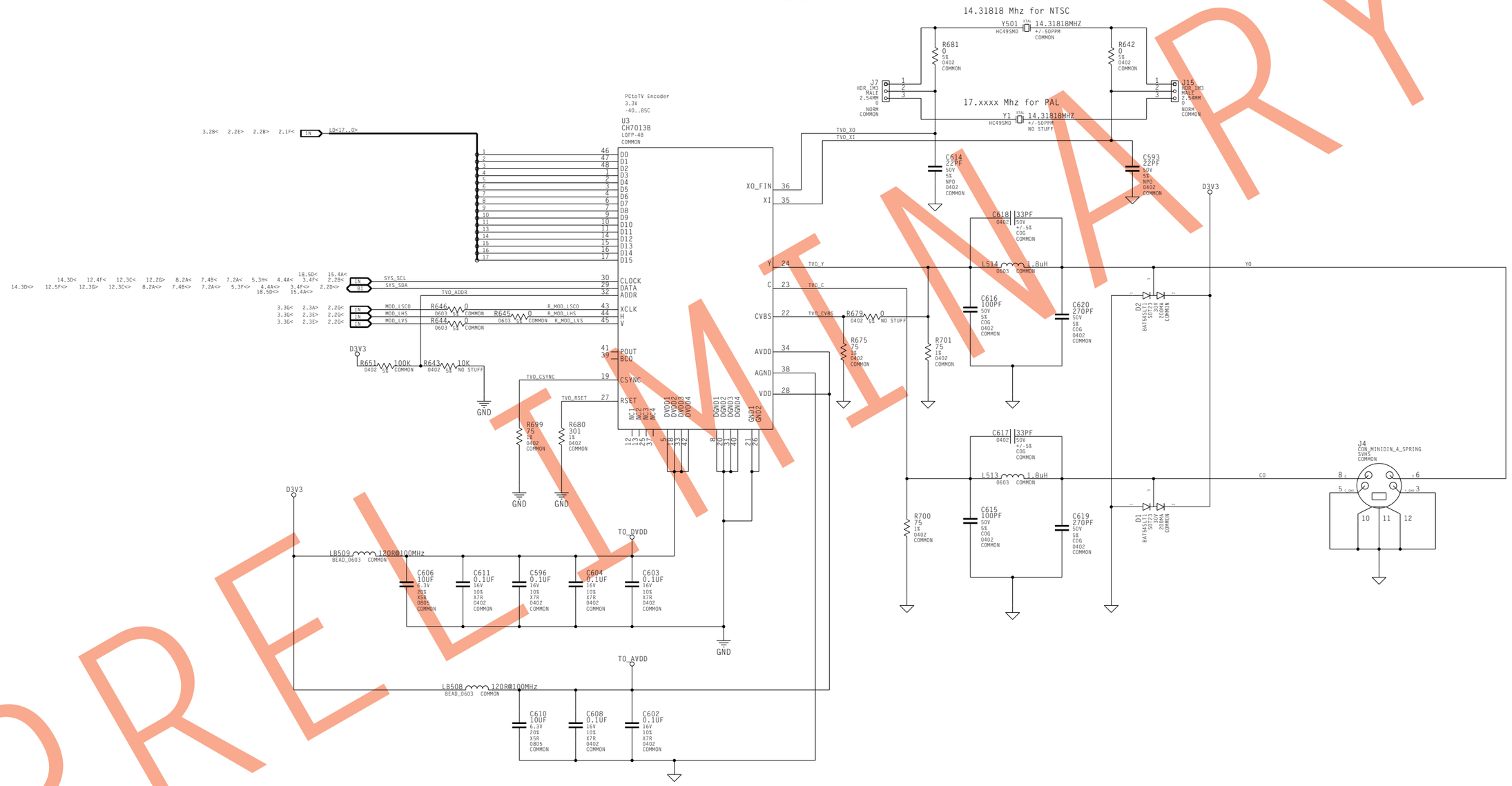
TVOUT ENCODER AND CONNECTOR



PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TV Encoder and Connector

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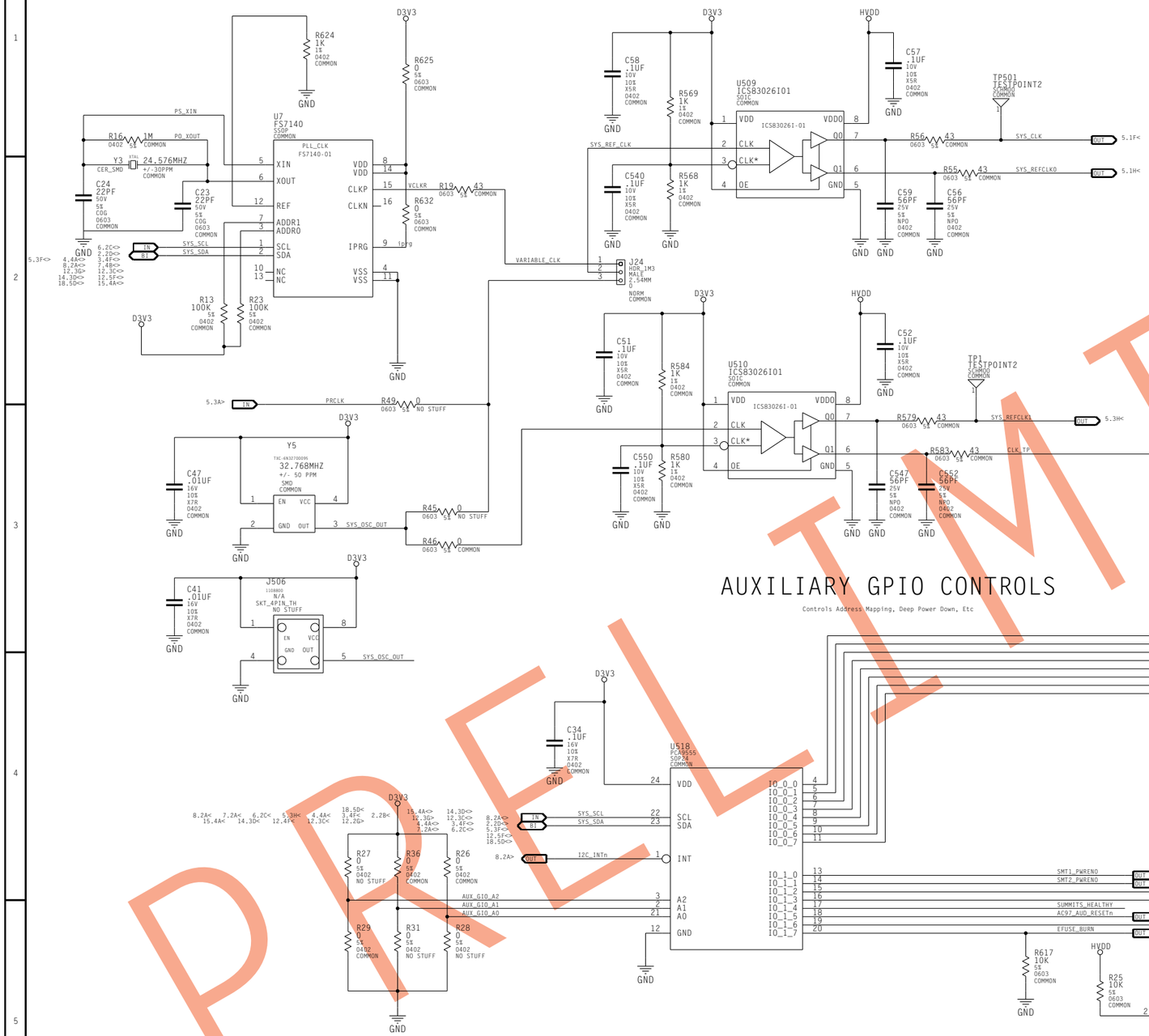
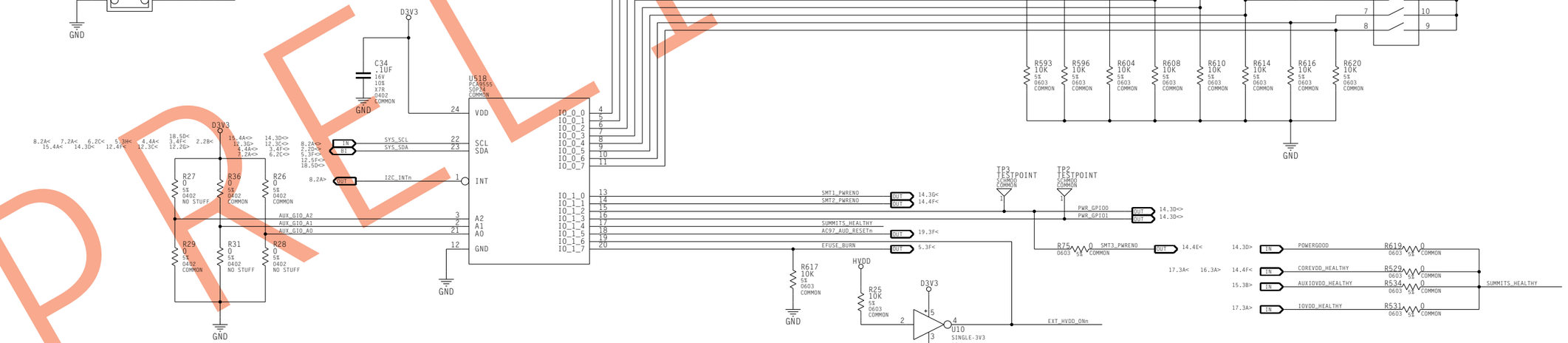
PROGRAMMABLE OSCILLATOR



AUXILIARY GPIO CONTROLS

Controls Address Mapping, Deep Power Down, Etc



PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Programmable Oscillator and Auxillary GPIOs

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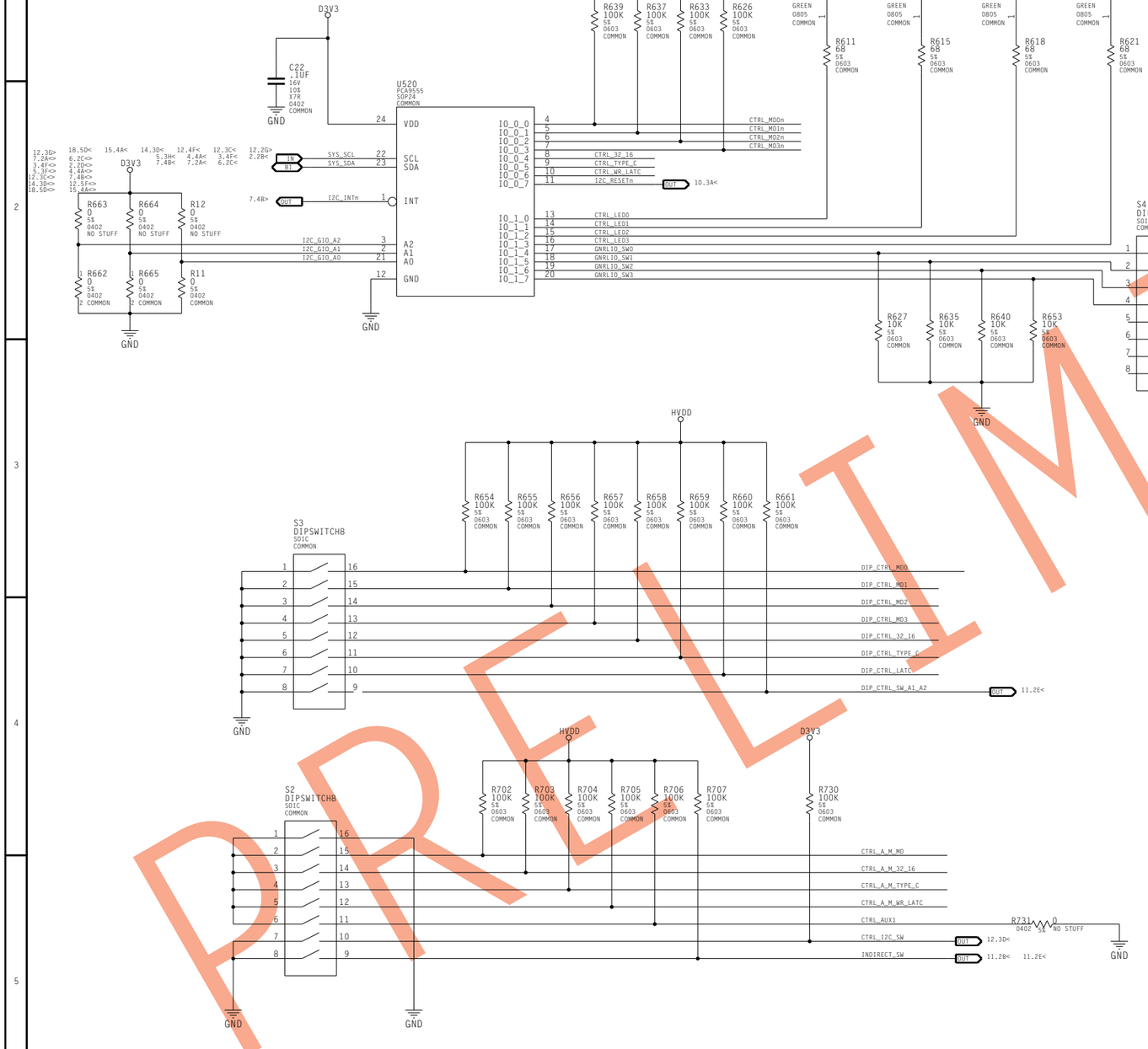
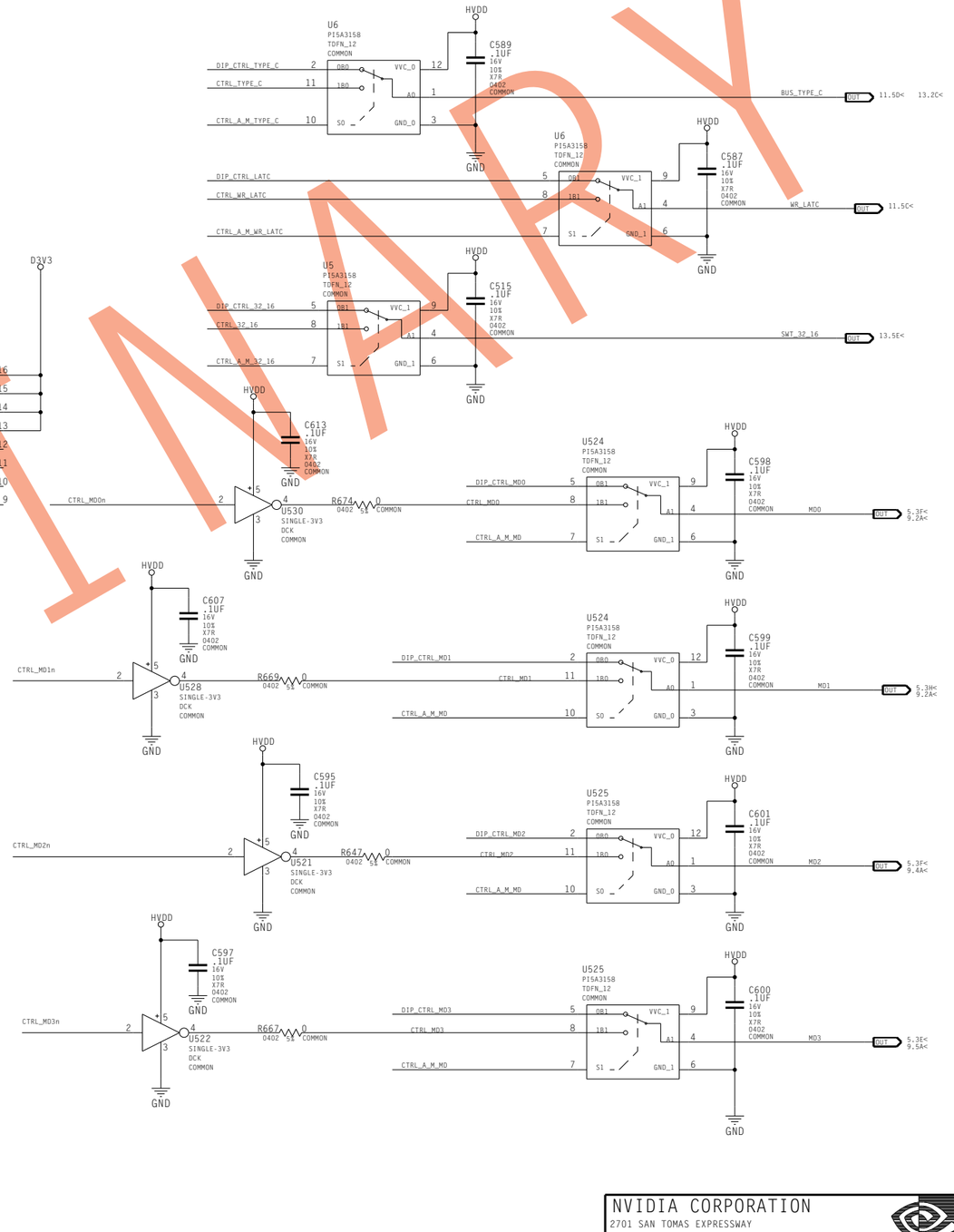
HOST INTERFACE CONTROL LOGIC AND I2C GPIO





PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Host Interface Control and I2C Bus Expansion

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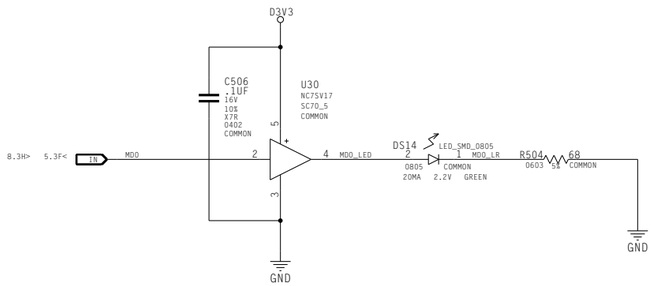
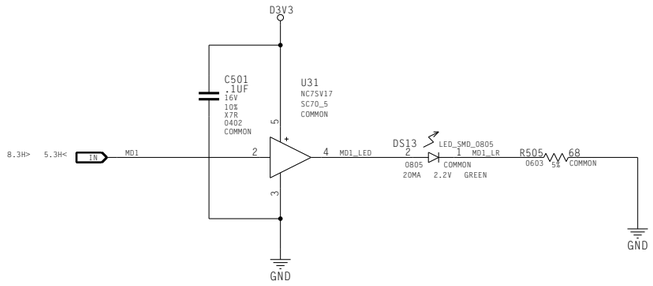
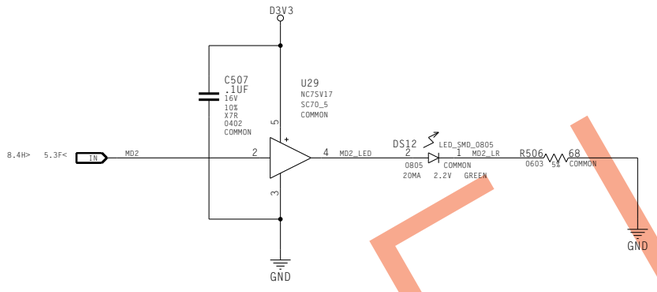
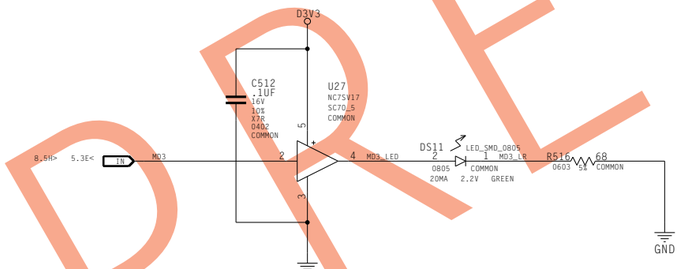
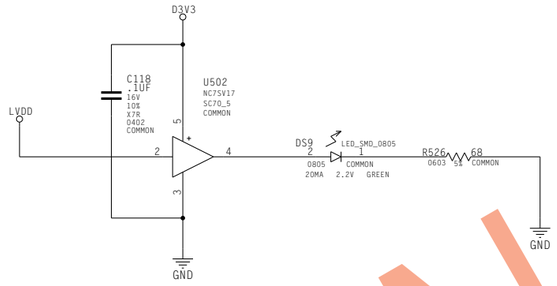
MODE and VOLTAGE LEDS

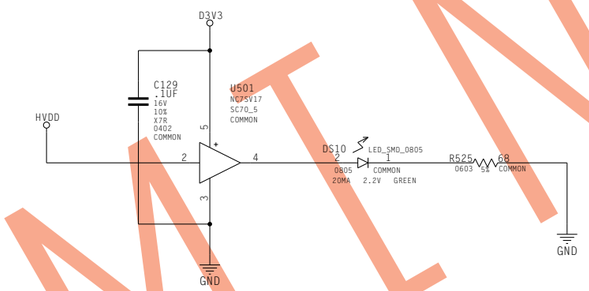


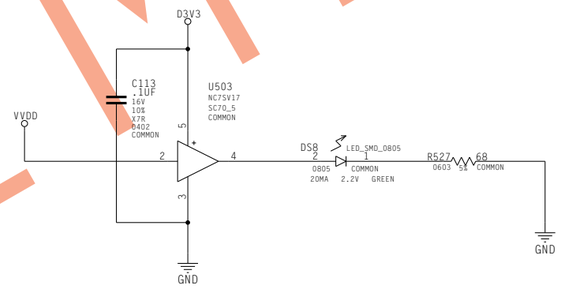


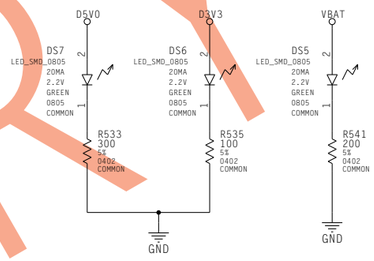












PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Mode and Voltage LEDs

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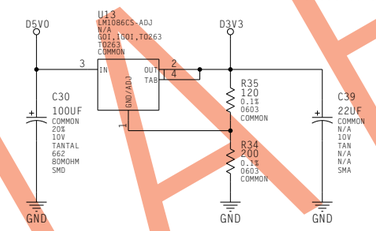
E433 SC15 Evaluation MainBoard

Reset, JTAG and 3.3V Power

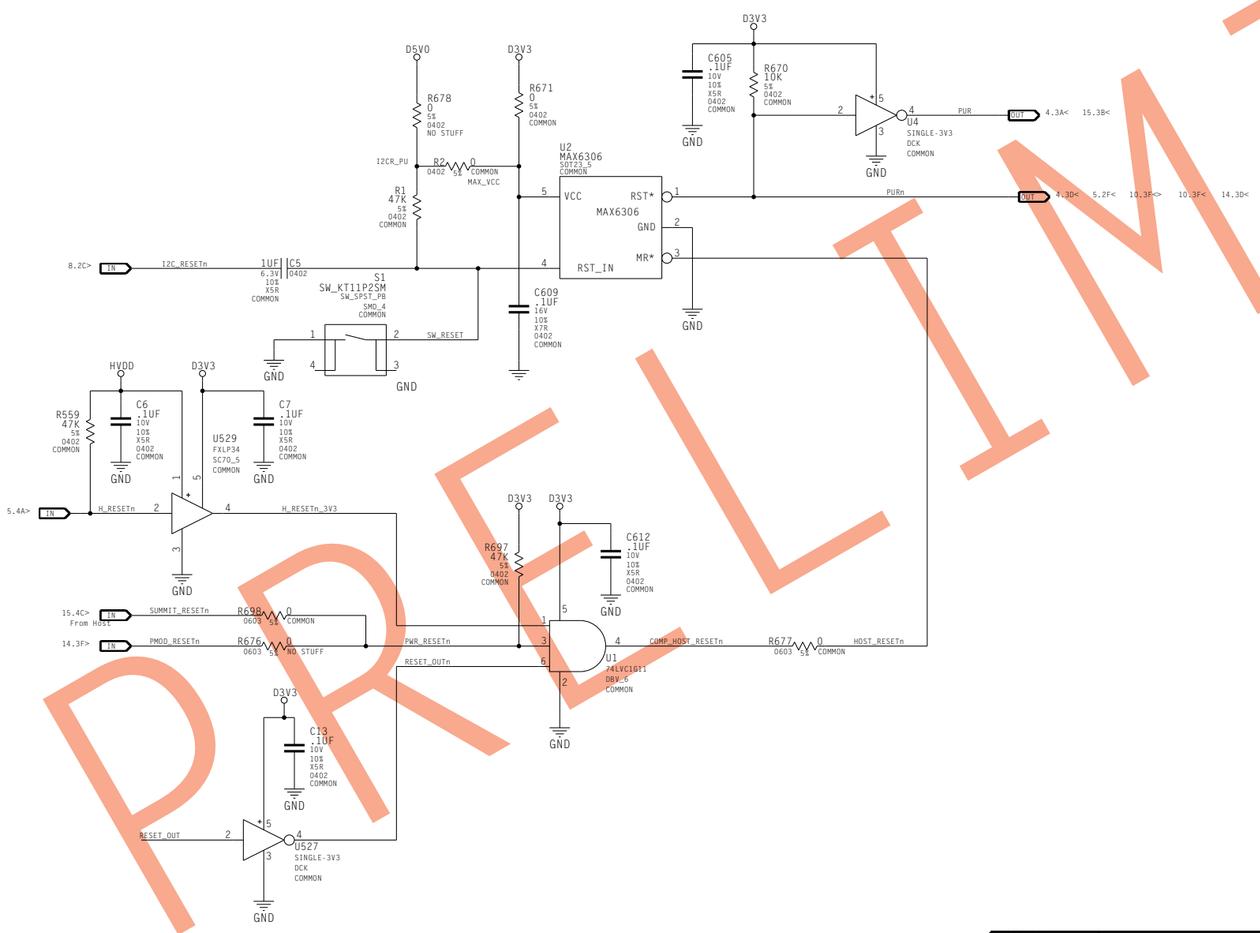
PRELIMINARY

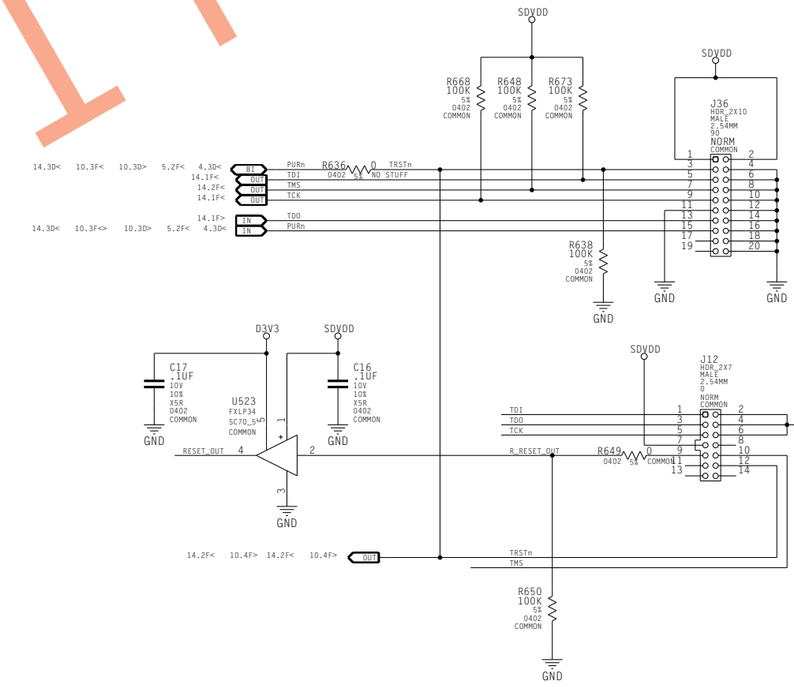
3V Regulator

D3V3 Set to 3.3V @ 500 mA



RESET CIRCUIT





ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	RESET, JTAG and 3V3 Power

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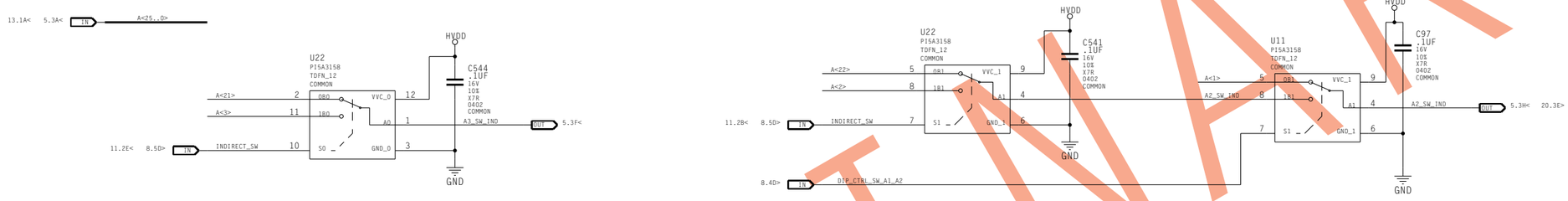
E433 SC15 Evaluation MainBoard

HOST INTERFACE ADDRESS AND CTYPE CONTROLS

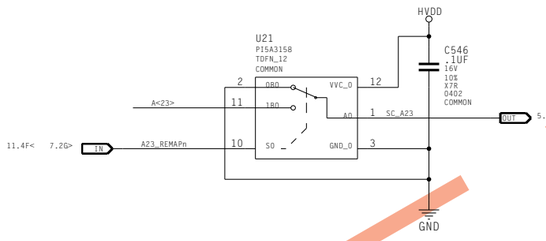
PRELIMINARY

Indirect Addressing Remap

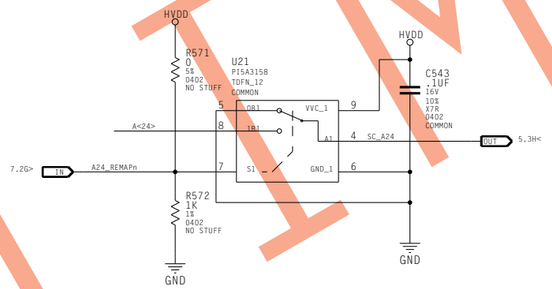
(Remaps to Higher Addr space to support autoincrementing buses)
(Writes to 0xXX40_0000 control A2, Writes to 0xXX20_0000 control A3)



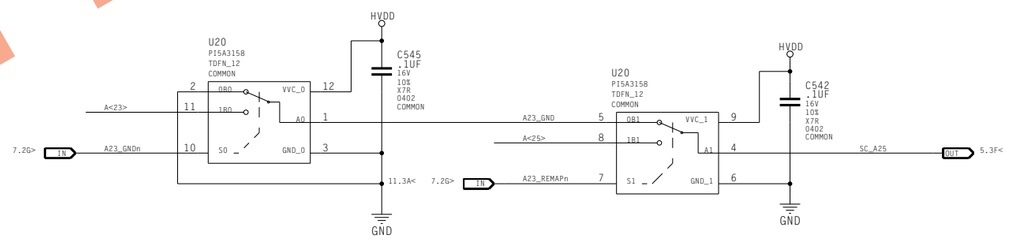
SC15 Address Remap



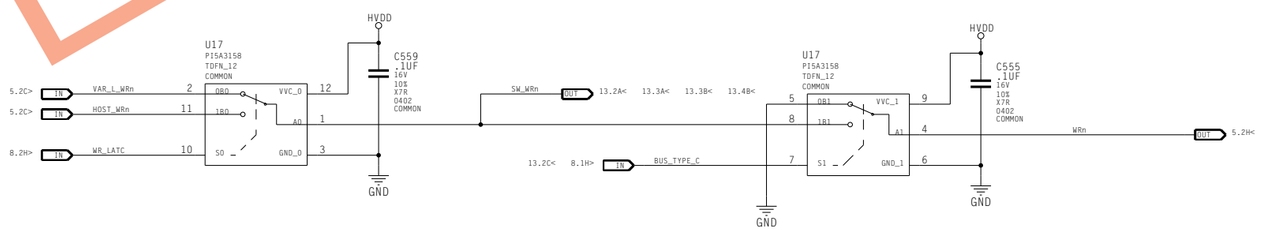
SC15 Address Remap



SC15 Address Remap



TYPE C VARIABLE LATENCY CONTROL



ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Host Interface Address and CType Mode Controls

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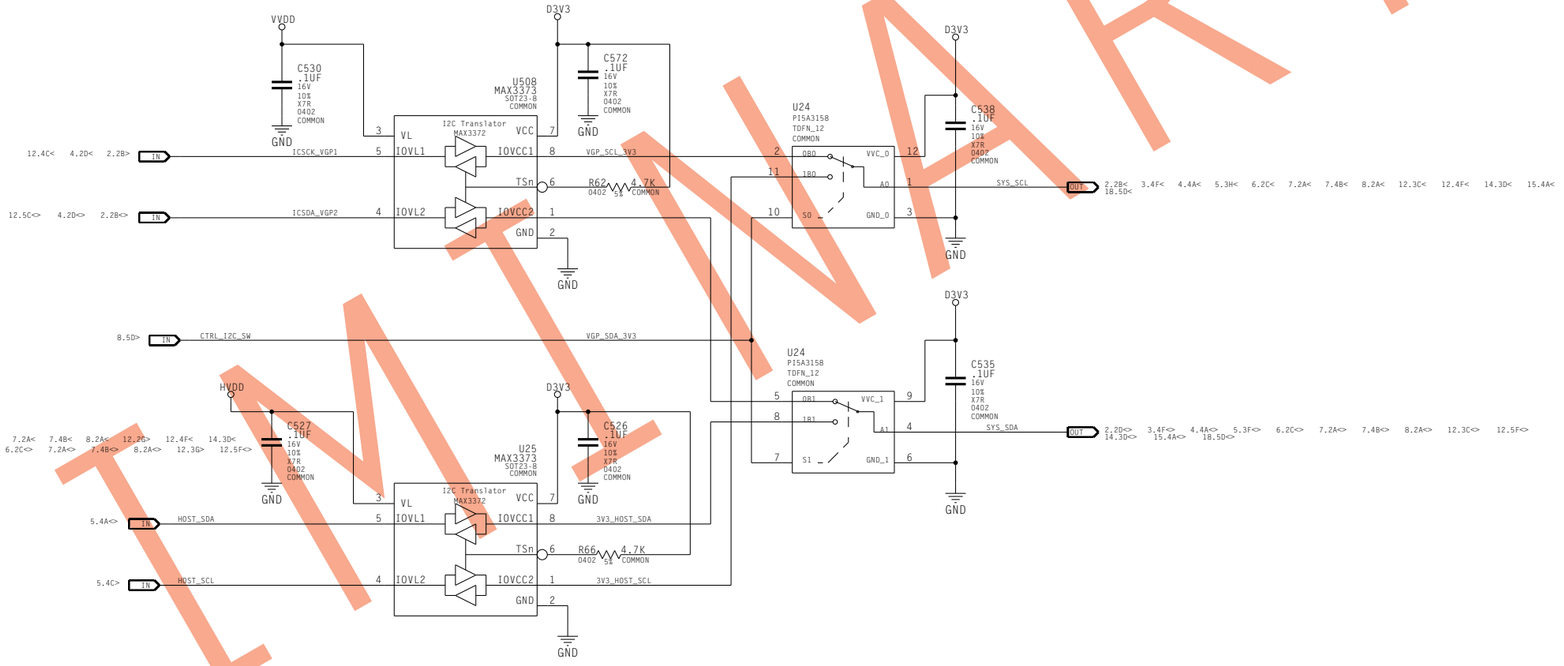
ID	e433	PAGE	11 OF 20
NAME	jcihla	DATE	12-JUL-2004

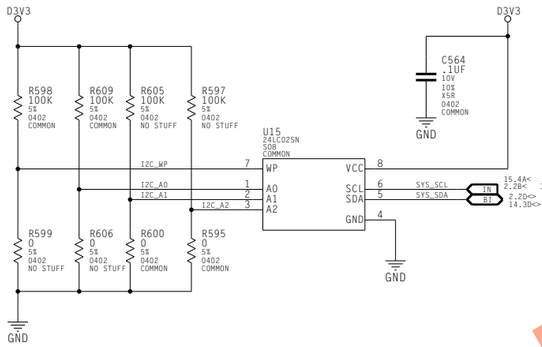
E433 SC15 Evaluation MainBoard

I2C and IDPROM

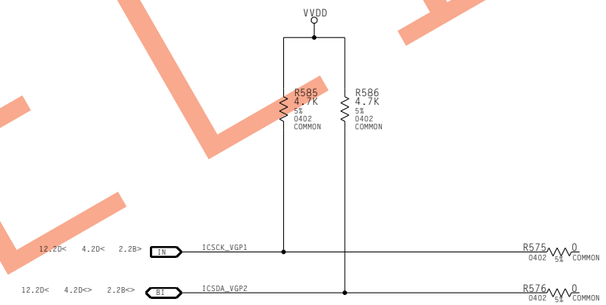
CPU vs GPU I2C Control

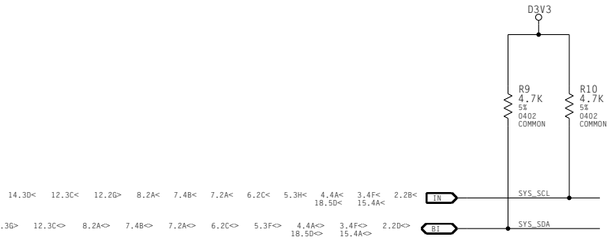


I2C ID Memory



I2C ADDR: 0b1010001





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PAGE DETAIL	IDPROM and I2C Mux Controls

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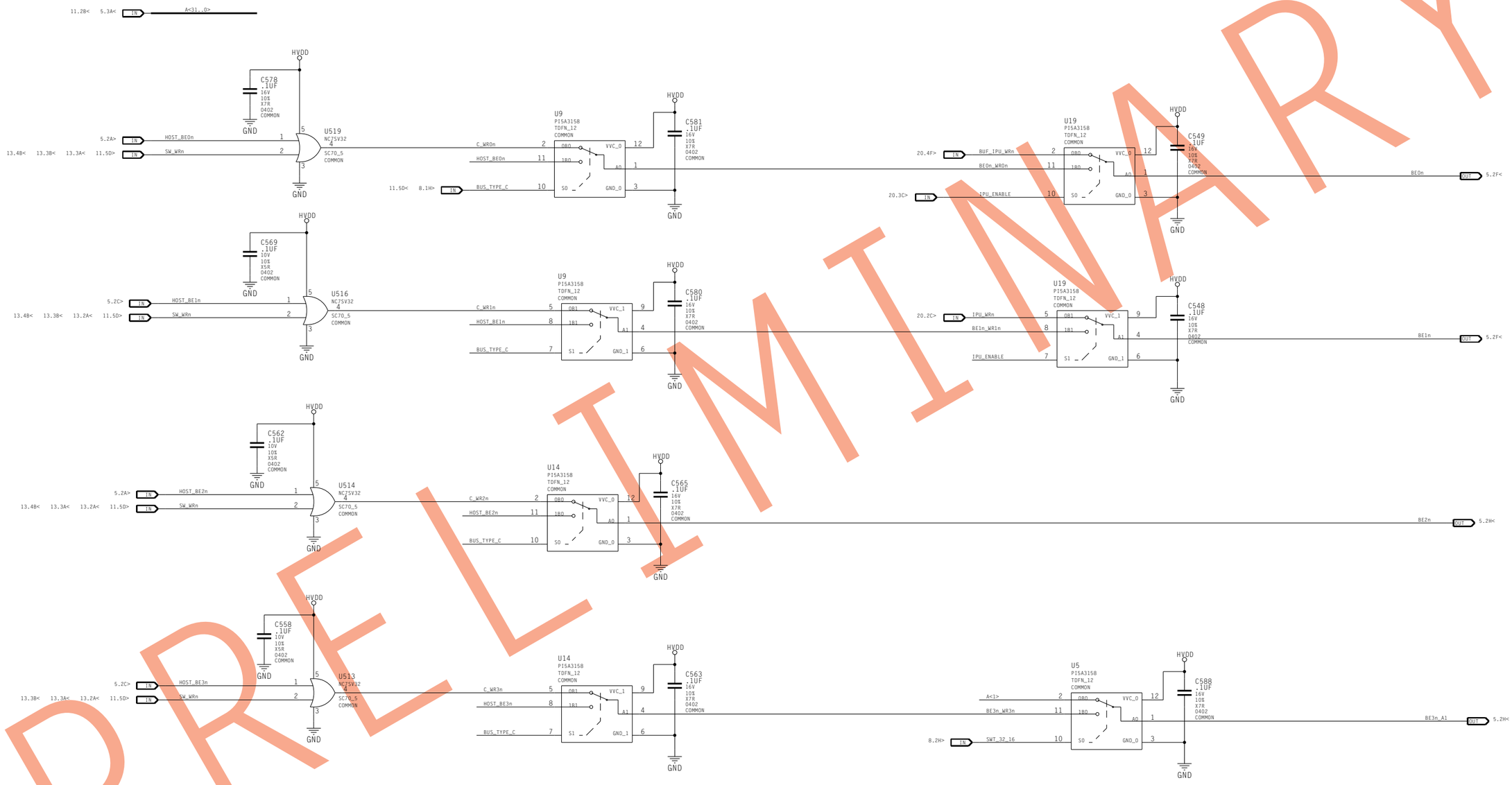
E433 SC15 Evaluation MainBoard

TYPE C BUS MUX CONTROLS



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PAGE DETAIL	Host Bus Mode C Control Logic

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E433 SC15 Evaluation MainBoard

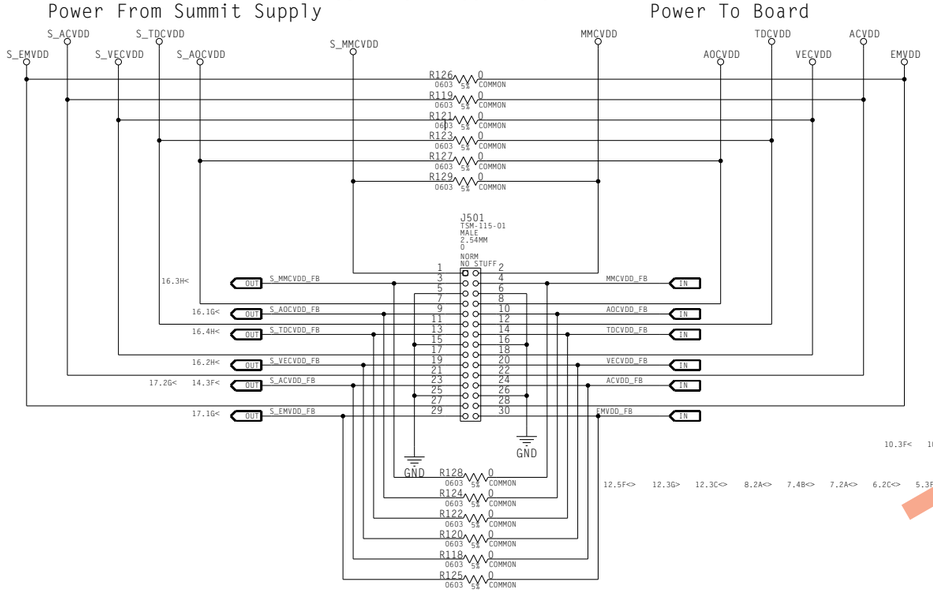
EXPANSION POWER INTERFACE, JTAG, RESET

EXPANSION POWER INTERFACE

CORE POWER CONNECTOR

Power From Summit Supply

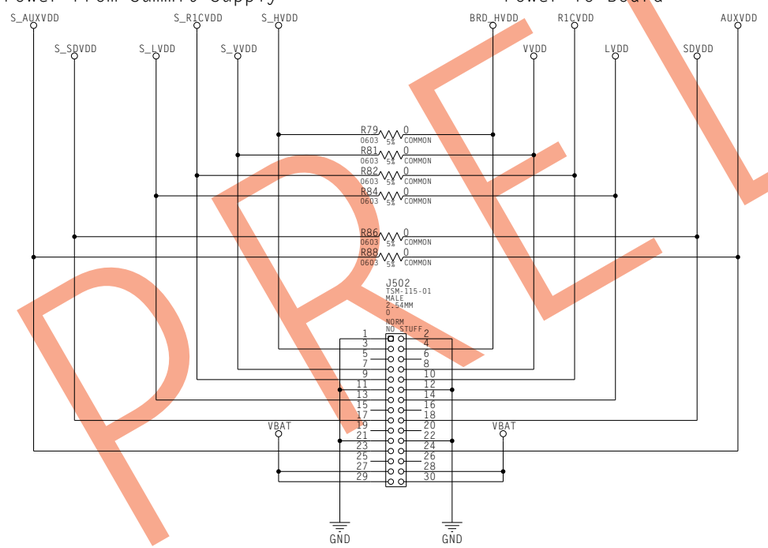
Power To Board



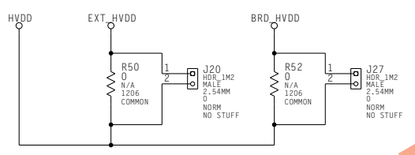
IO POWER CONNECTOR

Power From Summit Supply

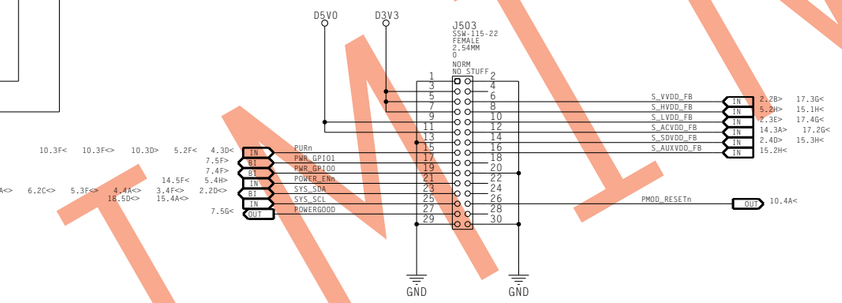
Power To Board



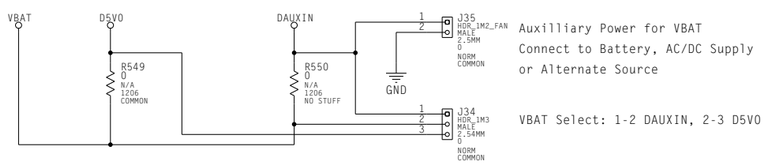
HVDD SELECTION JUMPERS



IO FEEDBACK and MISC CONNECTOR



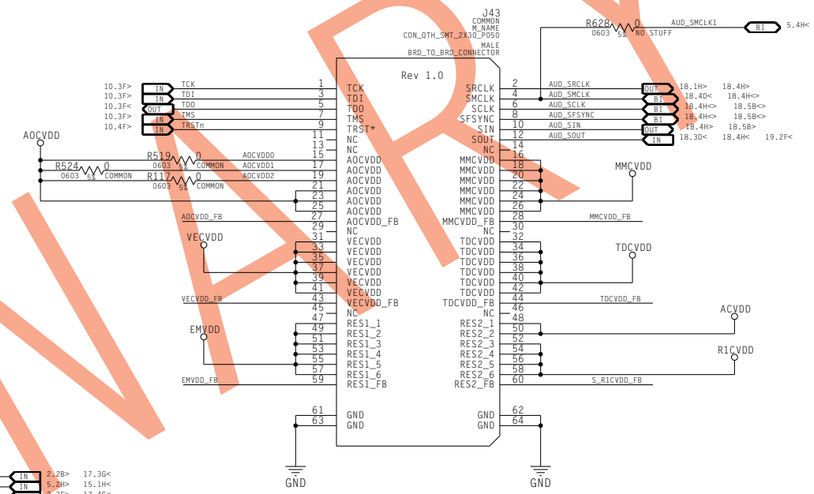
VBAT SELECTION JUMPERS

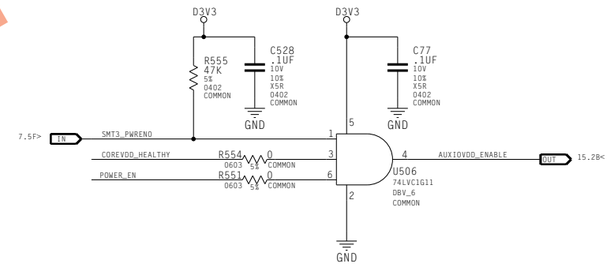


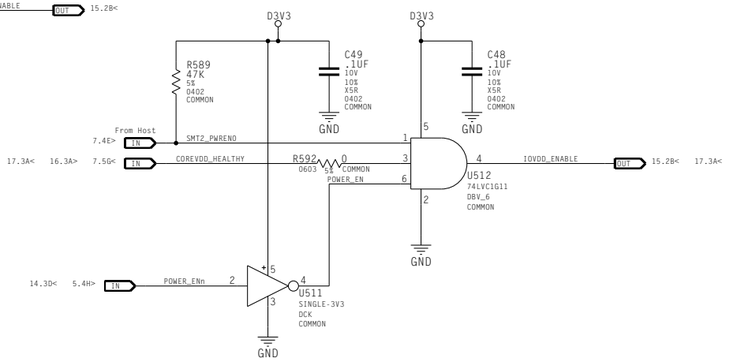
Auxilliary Power for VBAT
Connect to Battery, AC/DC Supply
or Alternate Source

VBAT Select: 1-2 DAUXIN, 2-3 D5V0

MODULE POWER CONNECTOR







PRELIMINARY

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PAGE DETAIL	Expansion Power Interface

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E433 SC15 Evaluation MainBoard

IO AND AUX POWER SUPPLY RAILS

PRELIMINARY

VBAT
SMT_VBAT
D4 1N4148 SOT23 COMMON
C73 .1UF 16V 10% X7R 0402 COMMON
C529 10UF 10V 10% X5R 0805 COMMON
C76 .1UF 16V 10% X7R 0402 COMMON
GND
U505 SMB120N VR_1V QFN QFN COMMON
SMB120
D5V0
D3V3_STDBY
C79 .1UF 16V 10% X7R 0402 COMMON
LDO_OUTPUT
40 LDO_SUPPLY
41 VSTANDBY
INVERTER
25 VBATT
26 VBATT
11 VREF_OUT
10 DOCK_DC
46 DC_IN
12 COMP1_CH0
13 COMP2_CH0
16 LSDRV_CH0
BOOST CHANNELS
59 PCHSEQ_CH1
61 COMP1_CH1
60 COMP2_CH1
64 LSDRV_CH1
43 PCHSEQ_CH2
45 COMP1_CH2
44 COMP2_CH2
48 LSDRV_CH2
27 PCHSEQ_CH3
28 COMP1_CH3
29 COMP2_CH3
32 LSDRV_CH3
BUCK CHANNELS
55 VM_CH4
54 COMP1_CH4
53 COMP2_CH4
51 HSDRV_CH4
49 LSDRV_CH4
50 HVSUP4
39 VM_CH5
38 COMP1_CH5
37 COMP2_CH5
35 HSDRV_CH5
33 LSDRV_CH5
34 HVSUP5
23 VM_CH6
21 COMP1_CH6
22 COMP2_CH6
19 HSDRV_CH6
17 LSDRV_CH6
18 HVSUP6
7 VM_CH7
5 COMP1_CH7
6 COMP2_CH7
3 HSDRV_CH7
1 LSDRV_CH7
2 HVSUP7
15 DRVGND
63 DRVGND
47 DRVGND
31 DRVGND
57 BULK_GND
GND
VBAT
SO_VDDCAP
C68 10UF 10V 10% X5R 0805 COMMON
C70 .1UF 16V 10% X7R 0402 COMMON
24 VDDCAP
SO_VREF
C80 .1UF 16V 10% X7R 0402 COMMON
42 VREF
R543 47K 5% 0402 COMMON
5.4A< IN EFUSE_PWR_ENABLE
14.4F> IN AUXIOVDD_ENABLE
17.3A< 14.4H> IN IOVDD_ENABLE
R546 0 0603 5% NO STUFF
R98 0 0402 5% COMMON
R99 0 0402 5% COMMON
PWREN_CH0
PWREN_CH1
52 PWREN0
62 PWREN1
36 nBATT_FAULT
14 POWER_FAIL
4 HEALTHY
8 SDA
9 SCL
20 HOST_RESET
30 nRESET
TP THERMPAD
56 AGND
58 DGND
SMT_VBAT
R560 47K 5% 0402 COMMON
SUMMIT_RESETn
OUT 10.4A<
SMT_SDA
OUT 16.3B<> 17.3B<>
SMT_VBAT
R91 47K 0402 5% COMMON
R547 47K 0402 5% COMMON
R92 47K 0402 5% COMMON
R76 47K 0402 5% COMMON
R96 47K 0402 5% COMMON
SMT_DONG_D3V3
D3 1N4148 SOT23 COMMON
J28 HTSS-105-01 MALE 2.54MM 0 NORM COMMON
1 SH_SCL
2 SH_SDA
C539 .1UF 16V 10% X7R 0402 COMMON
GND
R564 47K 5% 0402 COMMON
10.3D> 4.3A< IN PUR
R562 0 0603 5% NO STUFF
AUXIOVDD_HEALTHY OUT 7.5G<
R570 0 0402 1% NO STUFF
J22 HDR_1M3 MALE 2.54MM 0 NORM COMMON
12.3C<> 8.2A<> 7.2A<> 14.3D<> 12.5C<> 18.5D<> 7.4B<> 3.4F<> 2.2B<> 6.2C<> 12.3G<>
R1 SYS_SDA
J21 HDR_1M3 MALE 2.54MM 0 NORM COMMON
12.4F< 5.3H< 8.2A< 12.3C< 4.4A< 7.4B< 12.2G< 2.2B< 3.4F< 7.2A< 18.5D< 6.2C< 14.3D<
IN SYS_SCL
SMT_VBAT
R567 47K 5% 0402 COMMON
R566 47K 5% 0402 COMMON
R565 47K 5% 0402 COMMON
J23 HDR_2M3 MALE 2.54MM 0 LVDS COMMON
SMT_SCL
SMT0_SCL
SMT1_SCL OUT 16.3B<
SMT2_SCL OUT 17.3B<
R60 0 0402 5% NO STUFF
R59 0 0402 5% NO STUFF
R58 0 0402 5% NO STUFF

COMP1_CH4
COMP2_CH4
HSDRV_CH4
LSDRV_CH4
22PF C87 0402 50V 5% COG COMMON
R100 1K 0402 1% COMMON
C90 470PF 0402 50V 10% X7R COMMON
C89 470PF 0402 50V 10% X7R COMMON
R101 33.2K 0402 1% COMMON
Q2(P) Q1(N) Q507 FDC6333C_N/F SSOT6 COMMON
L507 6.8uH COMMON SMD_6_6x4_45mm
S_HVDD_FB IN 5.2N> 14.3F<
R78 100 1% 0402 COMMON
S_HVDD
C91 22UF 6.3V 20% X5R 1210 COMMON
GND

COMP1_CH5
COMP2_CH5
HSDRV_CH5
LSDRV_CH5
22PF C69 0402 50V 5% COG COMMON
R68 1K 0402 1% COMMON
C66 470PF 0402 50V 10% X7R COMMON
C67 470PF 0402 50V 10% X7R COMMON
R64 33.2K 0402 1% COMMON
Q2(P) Q1(N) Q512 FDC6333C_N/F SSOT6 COMMON
L512 6.8uH COMMON SMD_6_6x4_45mm
S_AUXVDD_FB IN 14.3F<
R89 100 1% 0402 COMMON
S_AUXVDD
C96 22UF 6.3V 20% X5R 1210 COMMON
GND

COMP1_CH6
COMP2_CH6
HSDRV_CH6
LSDRV_CH6
22PF C72 0402 50V 5% COG COMMON
R90 1K 0402 1% COMMON
C74 470PF 0402 50V 10% X7R COMMON
C71 470PF 0402 50V 10% X7R COMMON
R77 33.2K 0402 1% COMMON
Q2(P) Q1(N) Q511 FDC6333C_N/F SSOT6 COMMON
L511 6.8uH COMMON SMD_6_6x4_45mm
S_SDVDD_FB IN 7.4D> 14.3F<
R87 100 1% 0402 COMMON
S_SDVDD
C95 22UF 6.3V 20% X5R 1210 COMMON
GND

COMP1_CH7
COMP2_CH7
HSDRV_CH7
LSDRV_CH7
22PF C84 0402 50V 5% COG COMMON
R93 1K 0402 1% COMMON
C78 470PF 0402 50V 10% X7R COMMON
C85 470PF 0402 50V 10% X7R COMMON
R97 18.2K 0402 1% COMMON
Q2(P) Q1(N) Q509 FDC6333C_N/F SSOT6 COMMON
L509 6.8uH SMD_6_6x4_45mm COMMON
S_R1CVDD_FB IN
R83 100 1% 0402 COMMON
S_R1CVDD
C93 22UF 6.3V 20% X5R 1210 COMMON
GND

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Summit 120 and IO Power Rails

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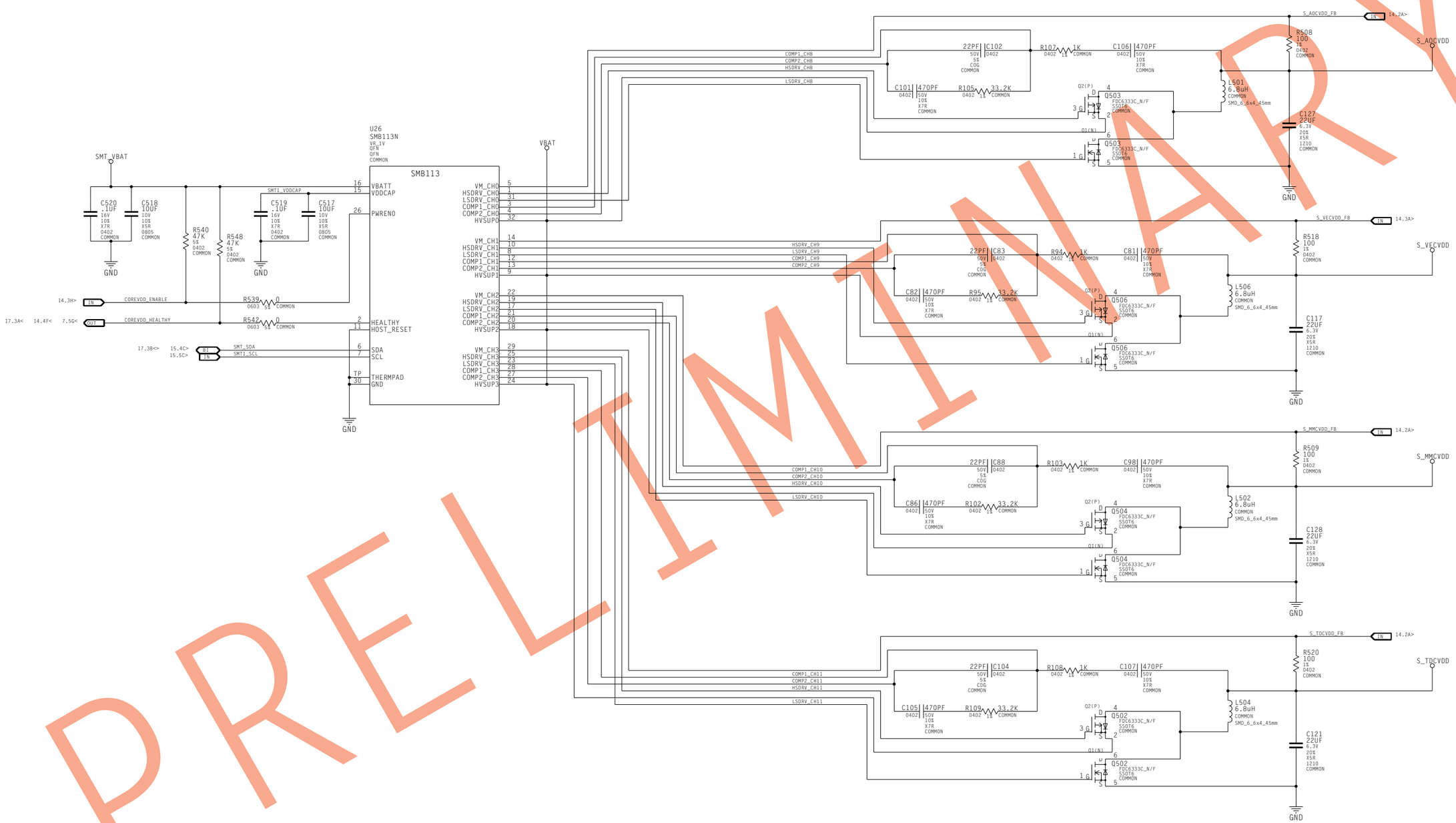
E433 SC15 Evaluation MainBoard

PRIMARY CORE POWER SUPPLY



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PAGE DETAIL	Summit 113 and Primary Core Power Rails

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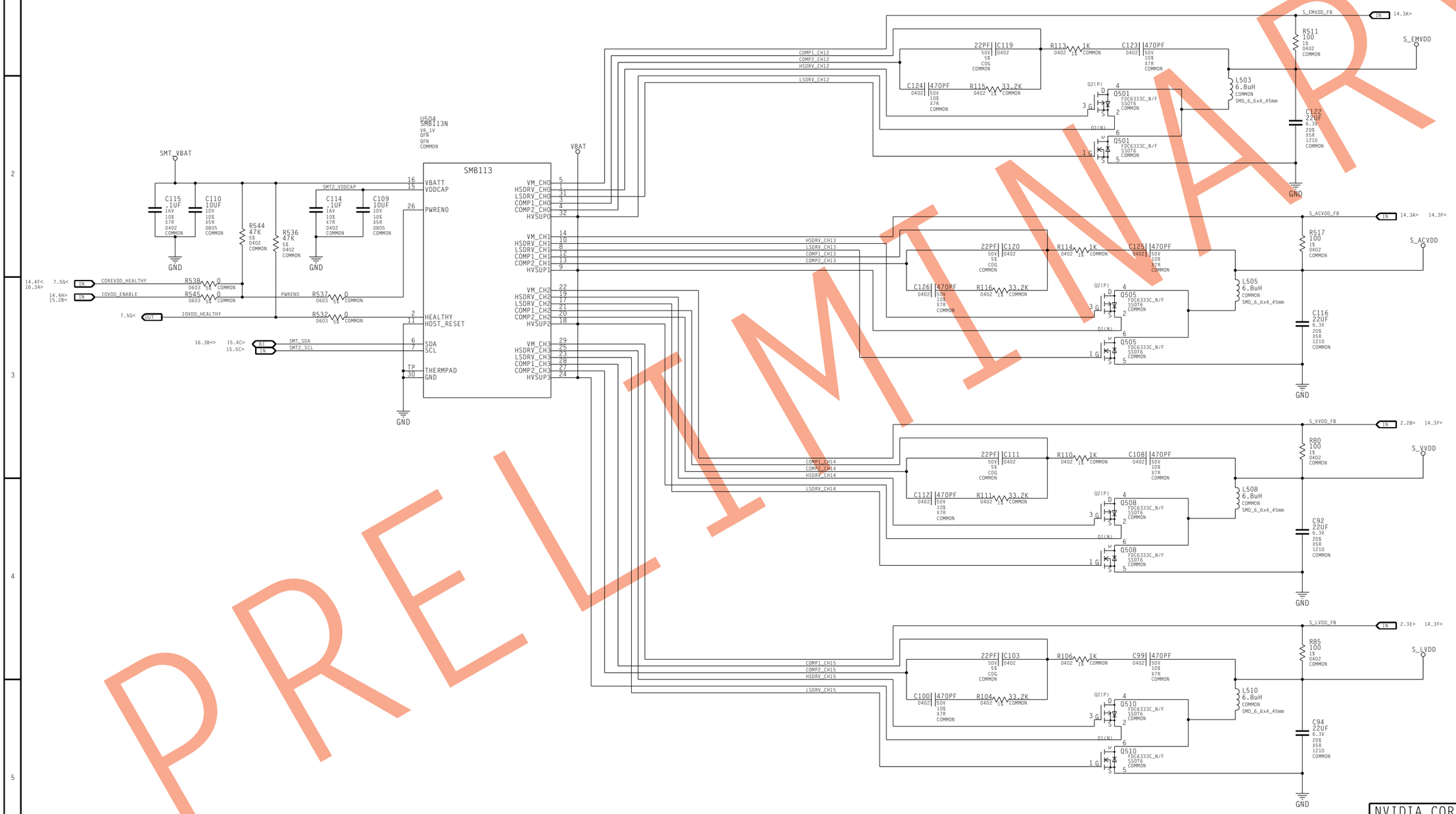
NAME	jcihla	DATE	05-Jun-2005

E433 SC15 Evaluation MainBoard

ADDITIONAL IO POWER SUPPLY RAILS



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ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Additional IO Power Supply Rails

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I2S AUDIO

J20, J10, J9, J8 Audio Sample Clock
0000 - 8.192 Mhz
0001 - 11.2896 Mhz
0010 - 12.288 Mhz
0011 - 24.576 Mhz
0101 - 16.9344 Mhz
0110 - 18.432 Mhz
0111 - 36.384 Mhz
0110 - 18.432 Mhz
1000 - 16.384 Mhz
1001 - 22.5792 Mhz
1011 - 49.152 Mhz
1101 - 33.8688 Mhz
1110 - 36.864 Mhz
1111 - 73.728 Mhz

Line Input

Microphone Input

Line Output

I2S Audio Codec
Wolfson WM8731

Place between Audio Codecs and J11

Audio Jumper Selection
I2S Audio Input/Output
J14 Install Pin 1 - 2 J15 Install Pin 1 - 2 J17 Install Pin 1 - 2 J18 Install Pin 1 - 2
Audio Control
I2C Port on HOST FPGA
J23 Install Pin 1 - 2 J28 Install Pin 1 - 2
I2C Port on HOST Connector
J23 Install Pin 2 - 3 J28 Install Pin 2 - 3
AC97 Audio Input/Output
J14 Install Pin 2 - 3 J15 Install Pin 2 - 3 J17 Install Pin 2 - 3 J18 Install Pin 2 - 3

PRELIMINARY

Analog Audio IO I2S

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Analog Audio IO I2S

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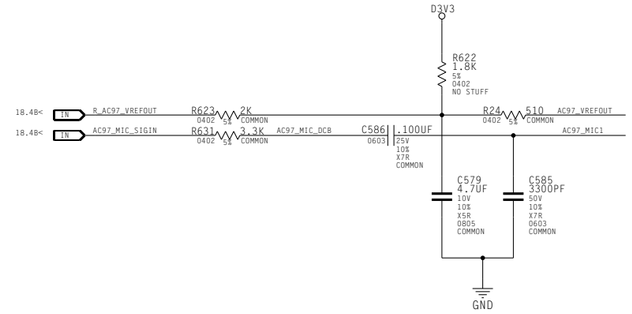
ID	e433	PAGE	18 OF 20
NAME	jcihla	DATE	19-MAY-2005

E433 SC15 Evaluation MainBoard

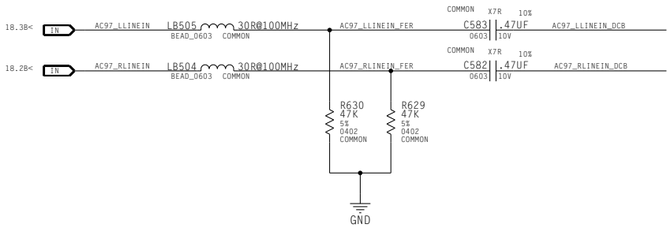
AC97 AUDIO

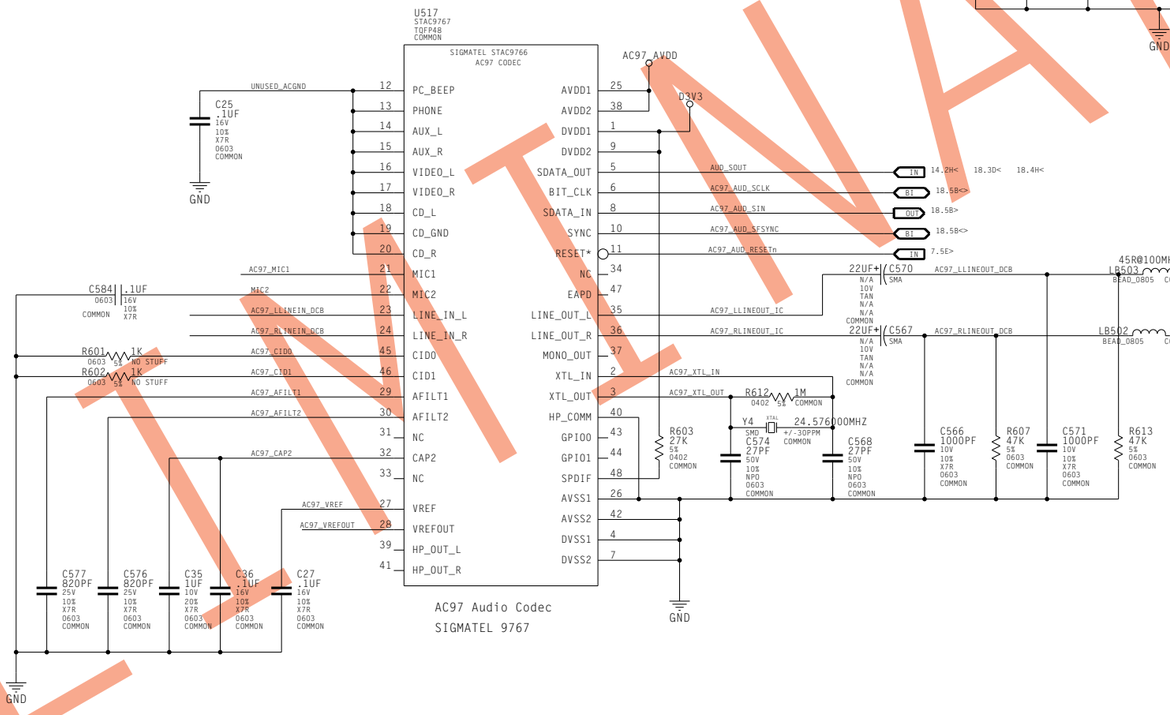
PRELIMINARY

Microphone Network



Line Input Network





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PAGE DETAIL	Analog Audio IO AC97

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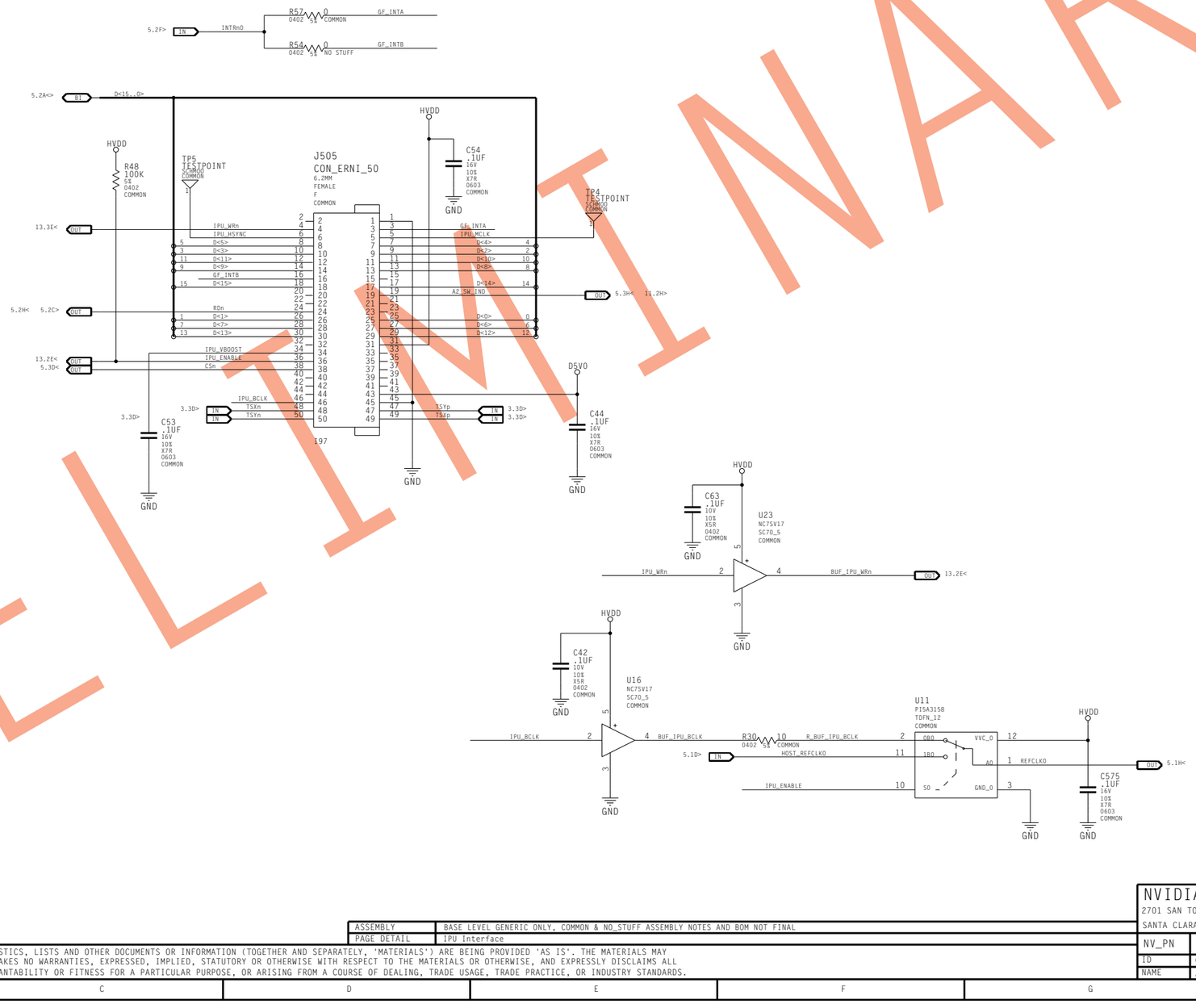
NV_PN	600-80433-0000-000		
ID	e433	PAGE	19 OF 20
NAME	jcihla	DATE	10-Jun-2005

E433 SC15 Evaluation MainBoard
IPU INTERFACE AND MISC CIRCUITS



PRELIMINARY

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IPU Interface

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ID	e433	PAGE	20 OF 20
NAME	jchla	DATE	20-06-05

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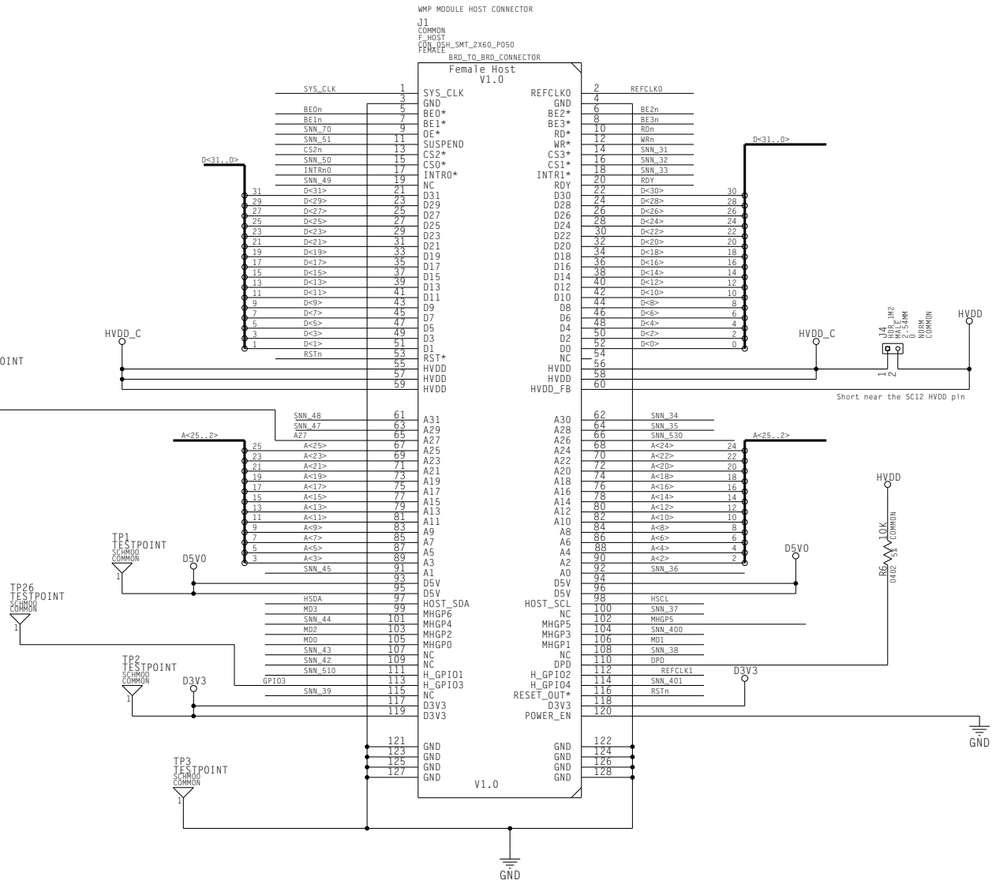
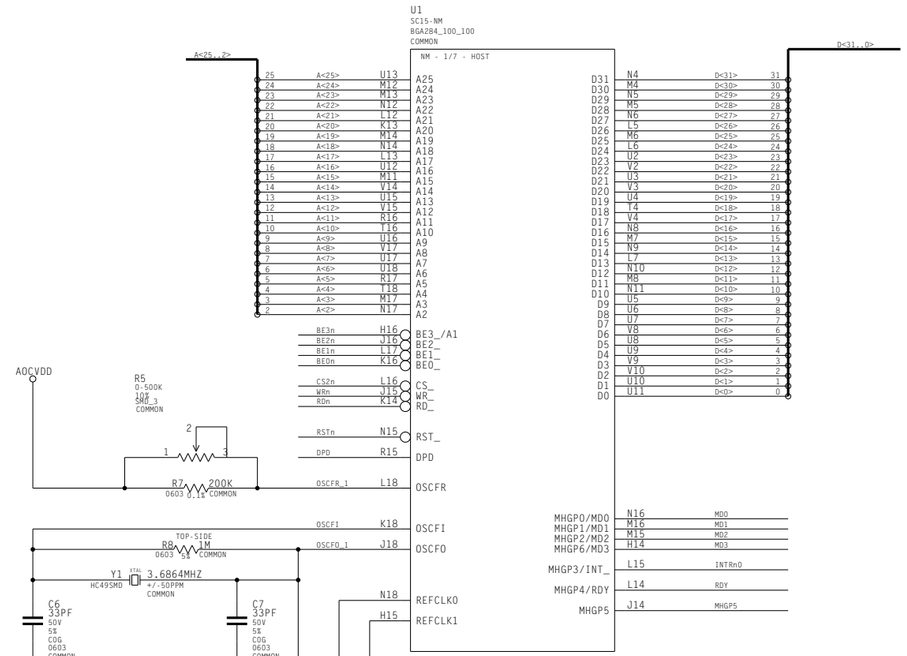
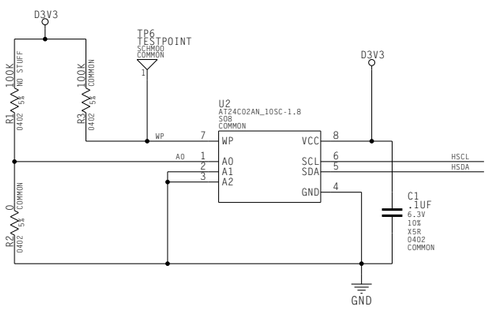
E436 SC15-NM Board

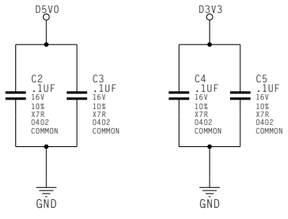
Host Connector and SC15 Host block

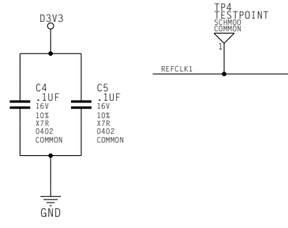


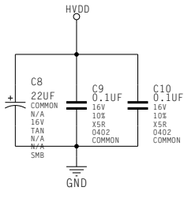


Module E2PROM









ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Host Connector and SC15 Host block

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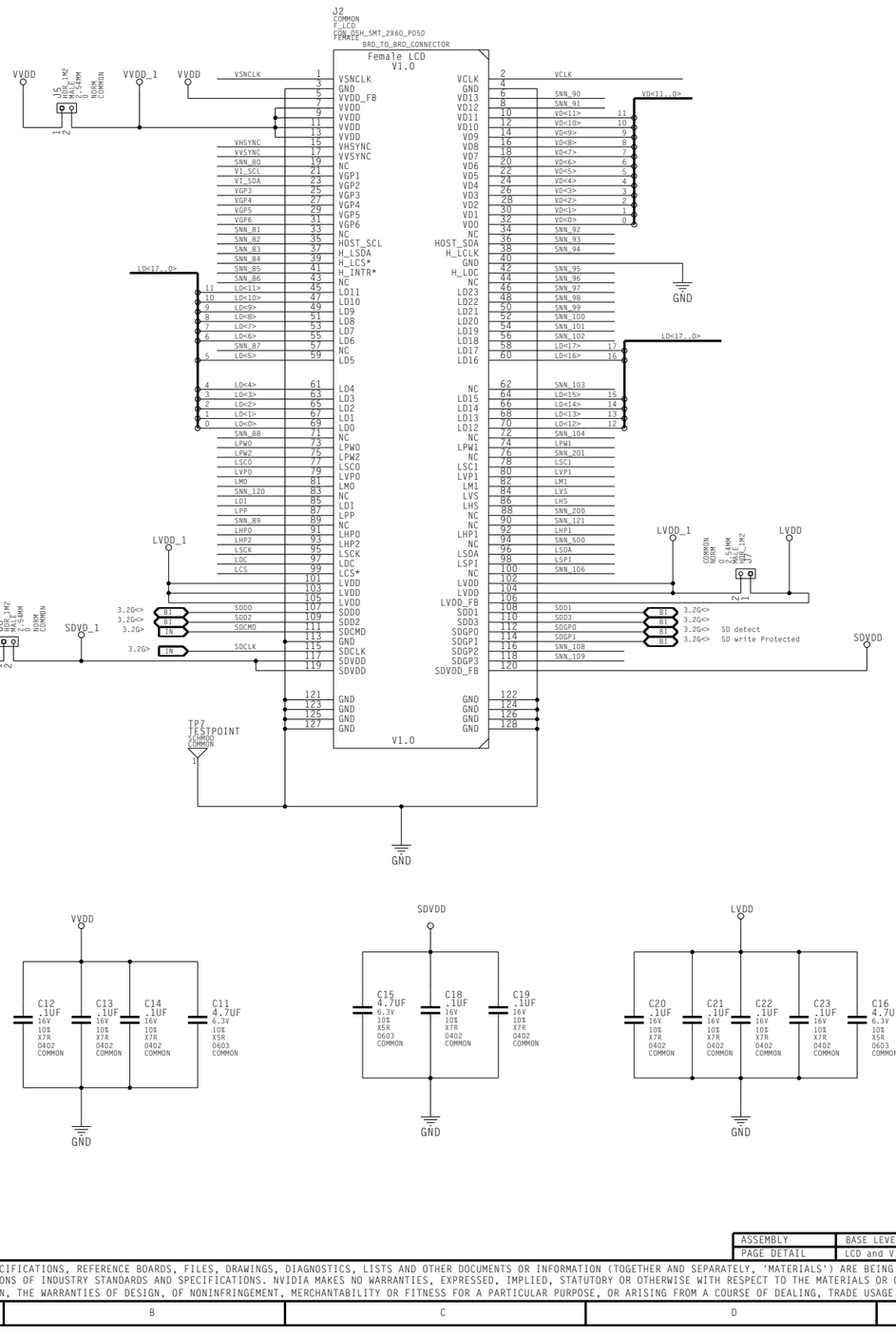
ID	e436	PAGE	1 OF 5
NAME	manoharc	DATE	dd-mon-year

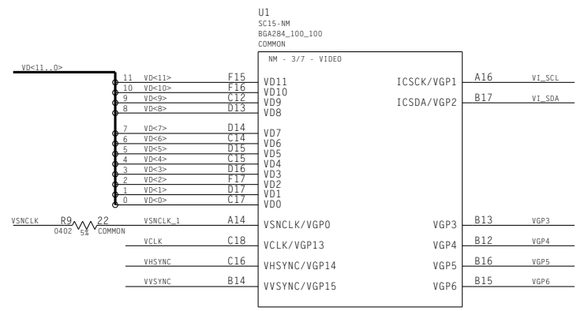
E436 SC15-NM Board

LCD/VI Connector and SC15 blocks

WMP MODULE LCD CONNECTOR



SC15 VI/Camera Interface



SC15 LCD Block

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LCD and VI Camera Interface

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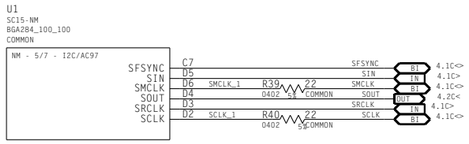
ID	e436	PAGE	2 OF 5
NAME	manoharc	DATE	dd-mon-year

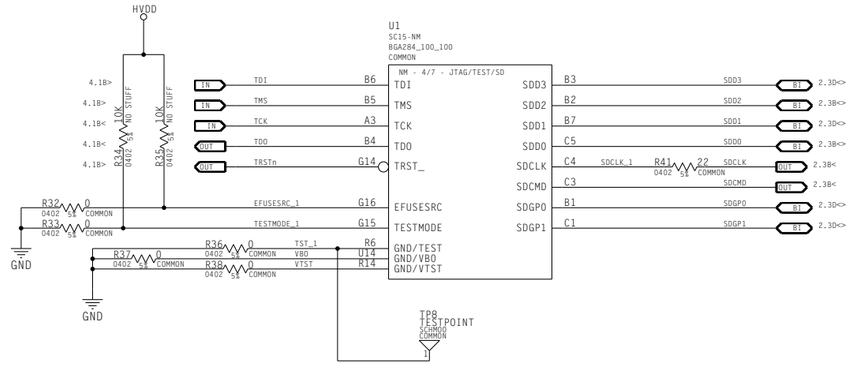
E436 SC15-NM Board

Audio SDCARD & Test Interfaces

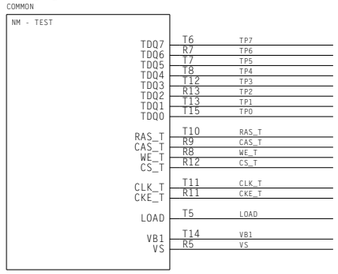
SC15 Audio I2S & AC97

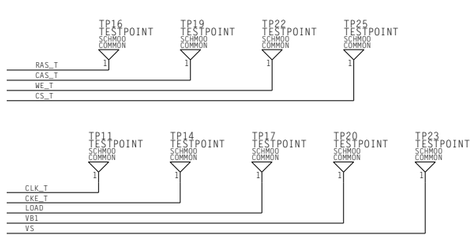


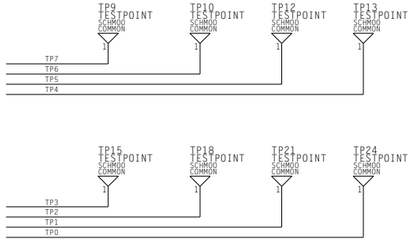
SC15 JTAG & SDCARD



SC15 Stached Chip Test header







ASSEMBLY	BASE LEVEL GENERIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Audio, SDcard & Interfaces

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NV_PN	600-f0ppp-00ss-vvv		
ID	e436	PAGE	3 OF 5
NAME	manoharc	DATE	dd-mon-year

E436 SC15-NM Board

Power Connector & Bypass Caps

WMP MODULE POWER CONNECTOR

J3 COMMON F_NAME CON_QSH_SMT_2X30_P050 FEMALE BRD_TO_BRD_CONNECTOR

Rev 1.0

AVDDOSC AVDDP2 AVDDP1 AOCVDD VECVDD EMVDD MMCVDD TDCVDD ACVDD RESERVE_2 GND

SC15 Power pins

U1 SC15-NM BGA284_100_100 COMMON

NM - 6/7 - POWER

AOCVDD VVDD SDVDD ACVDD AVDDP1 AVDDP2 AVDDOSC EMVDD MMCVDD VECVDD TDCVDD HVDD LVDD EMVREF GND

Alternate Regulator

U3 LT1763 VREF=1.22V S8 S8 NO STUFF

MMCVDD D3V3 RESERVE_1 GND

Core Voltage Bypass Caps

AOCVDD VECVDD EMVDD TDCVDD MMCVDD GND

Place 0.01uF & 0.1uF As Close to the SC15 as possible or under the chip

Place 0.1uF and 0.1uF as close to SC15 as possible

Internal Memory Bypass Caps

EMVDD HVDD GND

IO Bypass Caps

LVDD SDVDD VVDD ACVDD GND

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power supplies and Bypassing

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ID	e436	PAGE	4 OF 5
NAME	manoharc	DATE	dd-mon-year

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

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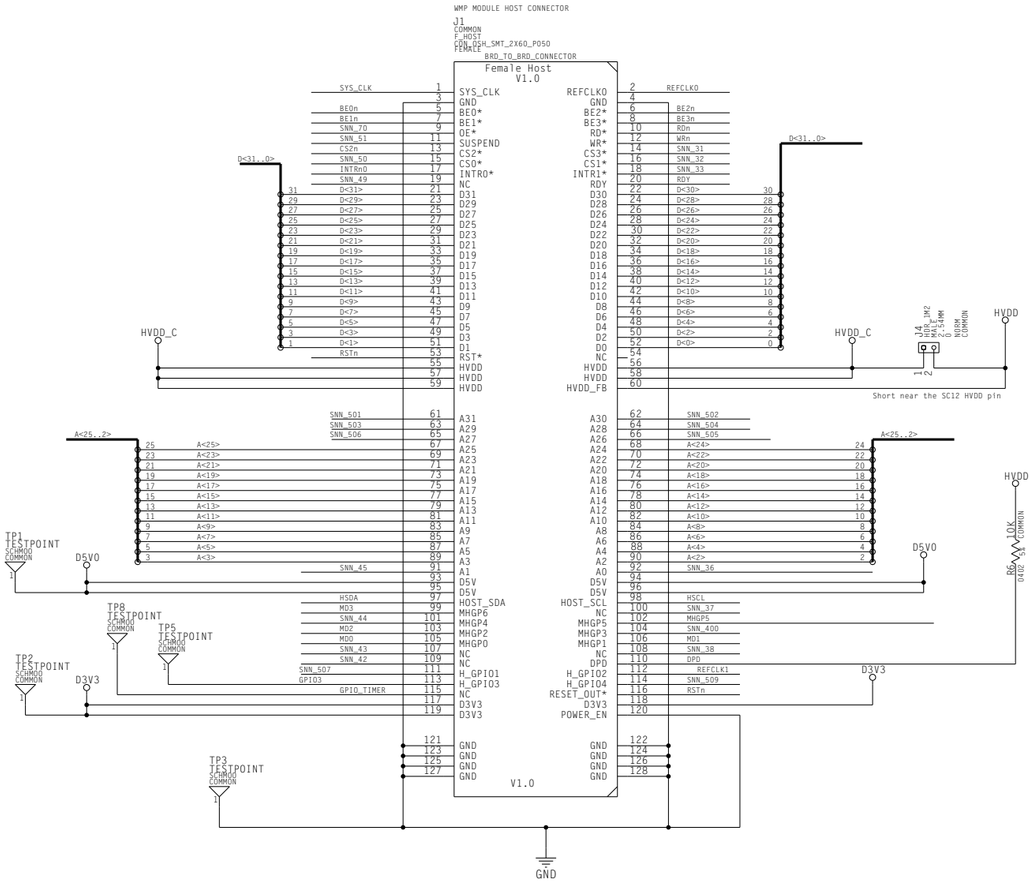
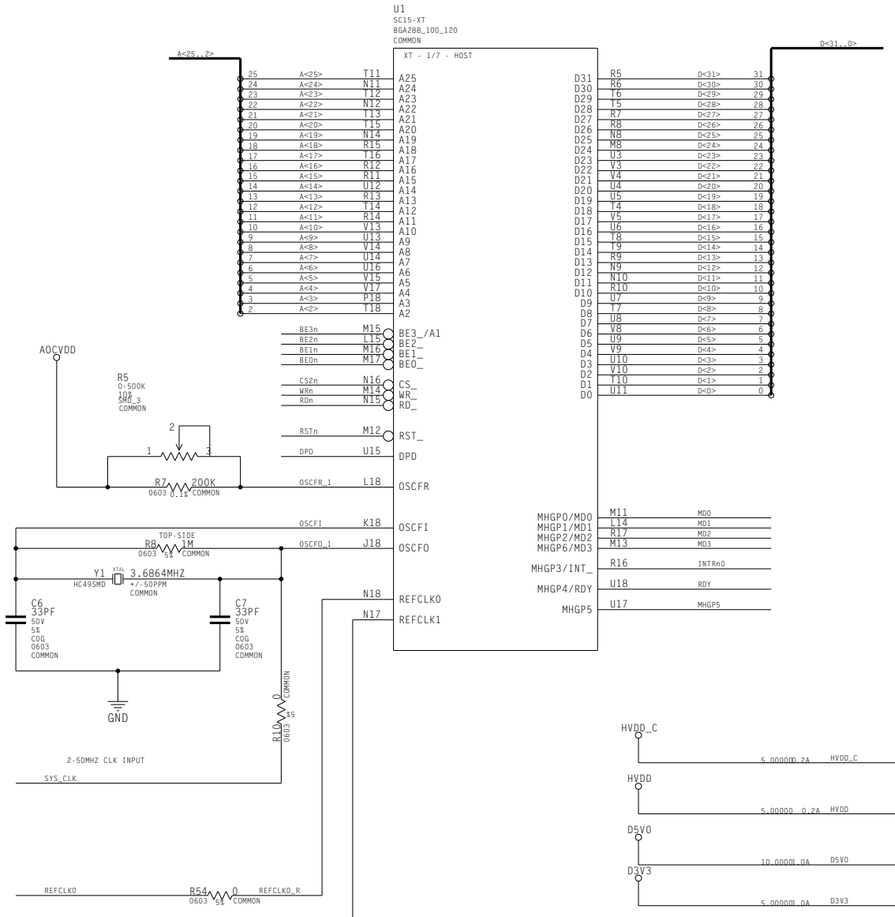
NV_PN	600-f0ppp-00ss-vvv		
ID	e436	PAGE	5 OF 5
NAME	manoharc	DATE	dd-mon-year

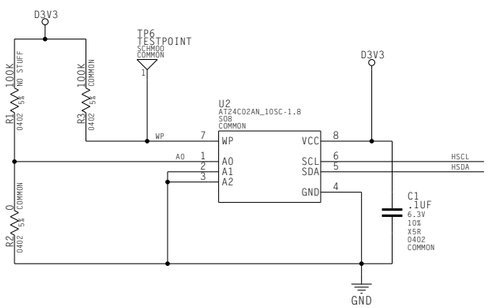
E438 SC15-XT-DDR Board

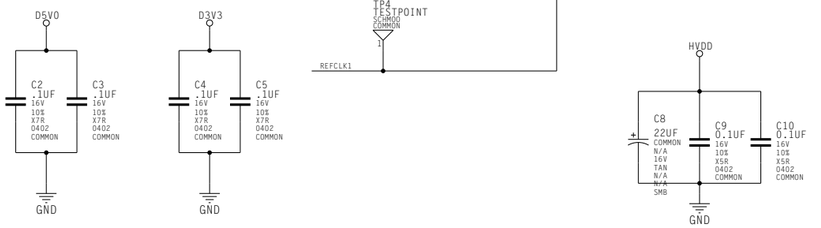
Host Connector and SC15 Host block





Module E2PROM





ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Host Connector and SC15 Host block

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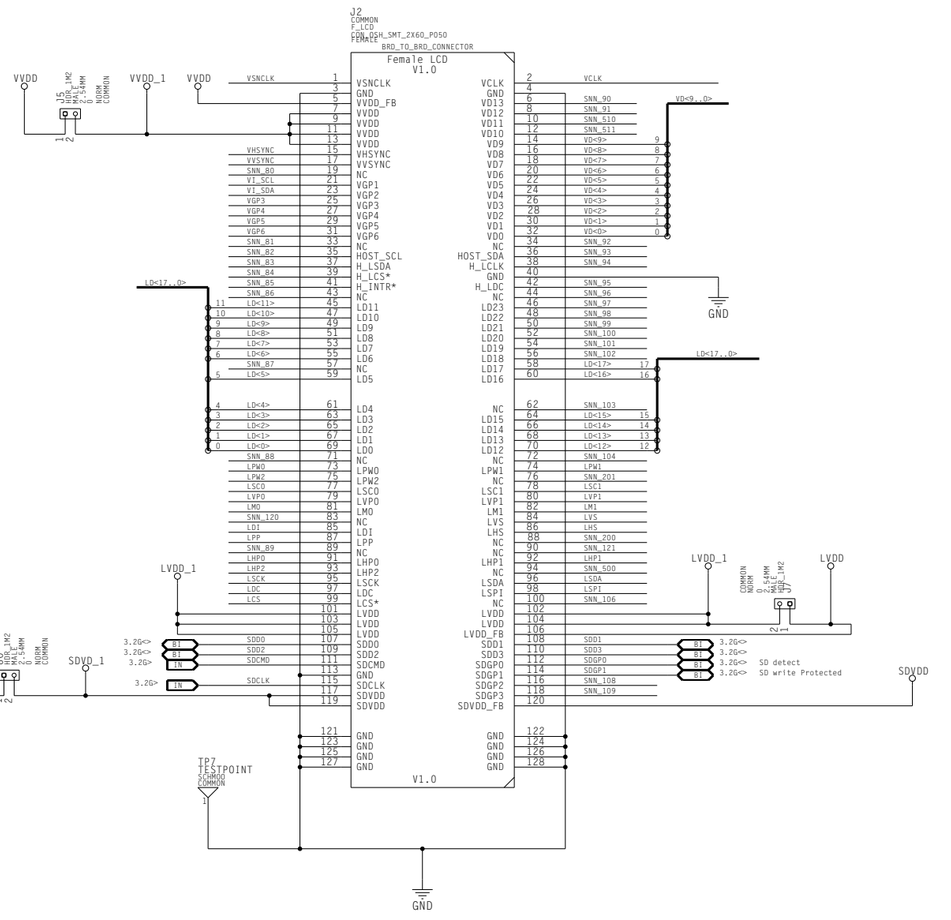
ID	e438	PAGE	1 OF 5
NAME	manoharc	DATE	dd-mon-year

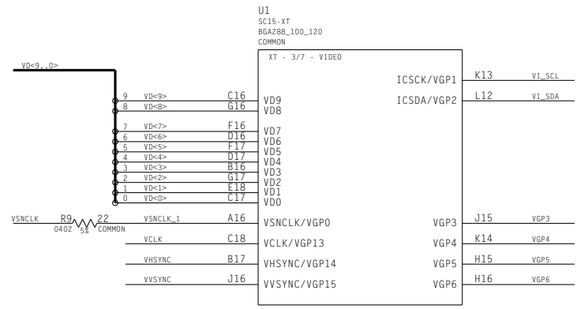
E438 SC15-XT-DDR Board

LCD/VI Connector and SC15 blocks

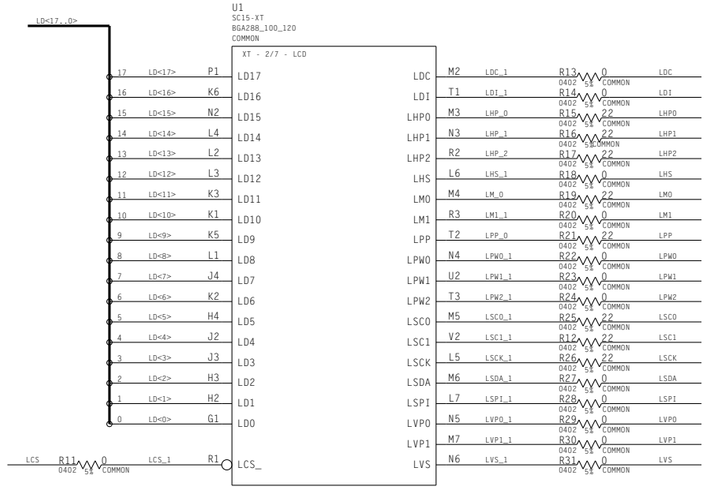
WMP MODULE LCD CONNECTOR

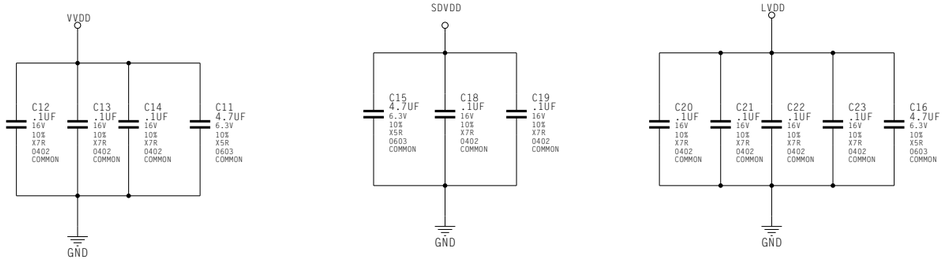


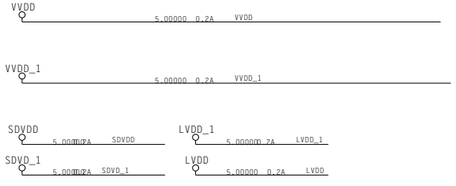
SC15 VI/Camera Interface



SC15 LCD Block







ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LCD and VI Camera Interface

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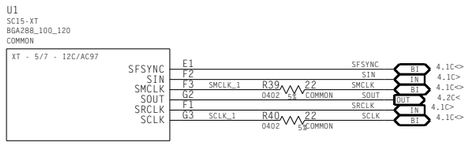
ID	e438	PAGE	2 OF 5
NAME	manoharc	DATE	dd-mon-year

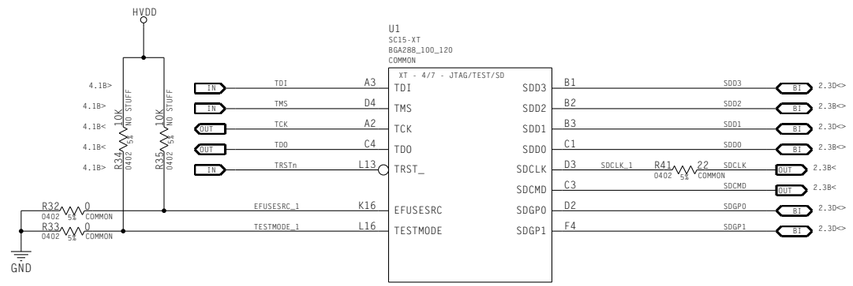
E438 SC15-XT-DDR Board

Audio SDCARD & JTAG Interfaces

SC15 Audio I2S & AC97



SC15 JTAG & SDCARD



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PAGE DETAIL	Audio, SDcard, JTAG Interfaces & SDRAM Debug Logic analyzer

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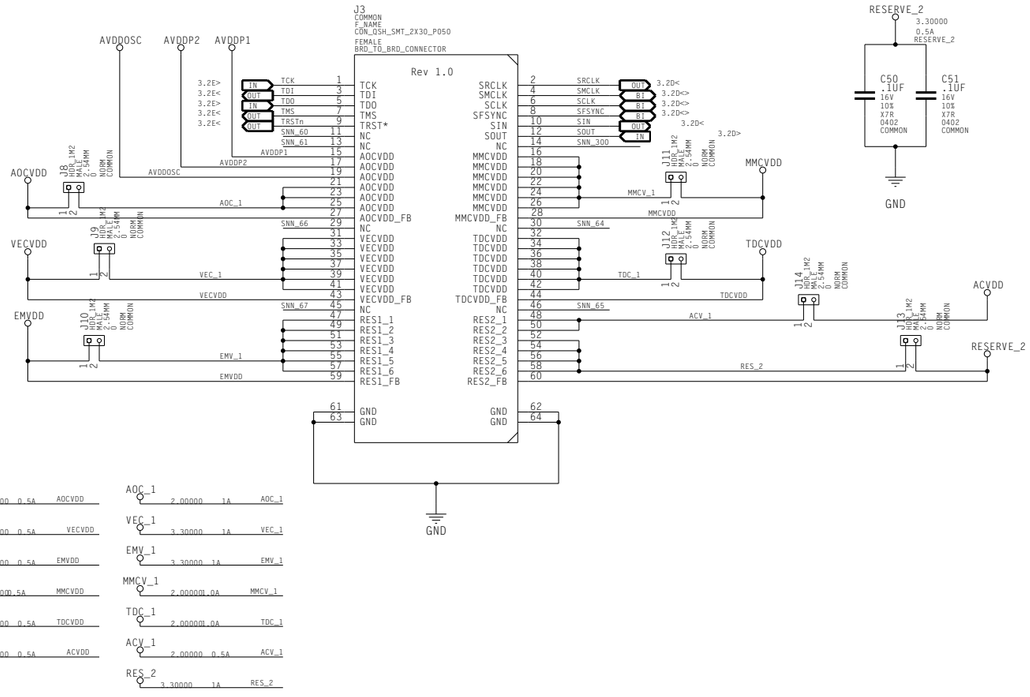
ID	e438	PAGE	3 OF 5
NAME	manoharc	DATE	dd-mon-year

E438 SC15-XT-DDR Board

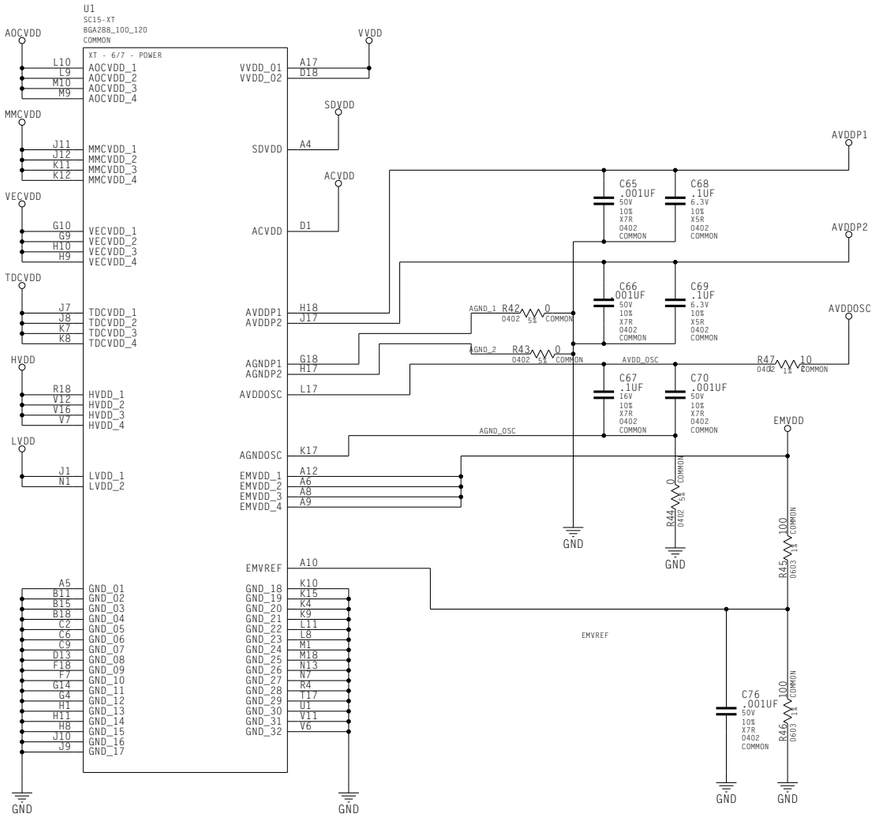
Power Connector & Bypass Caps



NOTE 1

1) All the POWER pins need 0.1 cap to be placed near U1 (SC15)

SC15 Power pins



Core Voltage Bypass Caps

Internal Memory Bypass Caps

IO Bypass Caps

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power supplies and Bypassing

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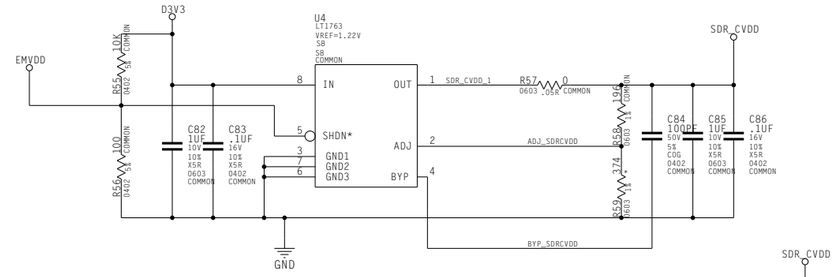
E438 SC15-XT-DDR Board



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