Service Manual

D1000 CARD

6802974C75-0

MOTOROLA
intelligence everywhere™

6802974C75-O

September 2004

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PREFACE

1.1 INTRODUCTION

Motorola® Inc. maintains a worldwide organization that is dedicated to provide responsive, full-service customer support. Motorola products are serviced by an international network of company-operated product care centers as well as authorized independent service firms.

Available on a contract basis, Motorola Inc. offers comprehensive maintenance and installation programs which enable customers to meet requirements for reliable, continuous communications.

To learn more about the wide range of Motorola service programs, contact your local Motorola products representative or the nearest Customer Service Manager.

1.2 PRODUCT IDENTIFICATION

Motorola products are identified by the model number on the housing. Use the entire model number when inquiring about the product. Numbers are also assigned to chassis and kits. Use these numbers when requesting information or ordering replacement parts.

1.3 PRODUCT NAMES

Product names included in Product Family D1000 Cards are listed on the front cover. Product names are subject to change without notice. Some product names, as well as some frequency bands, are available only in certain markets.

1.4 PRODUCT CHANGES

When electrical, mechanical, or production changes are incorporated into Motorola products, a revision letter is assigned to the chassis or kit affected, for example: -A, -B, or -C, and so on.

The chassis or kit number, complete with revision number, is imprinted during production. The revision letter is an integral part of the chassis or kit number and is also listed on schematic diagrams and printed-circuit board layouts.

1.5 COMPUTER PROGRAM COPYRIGHTS

The Motorola products described in this manual may include Motorola computer programs stored in semiconductor memories or other media that are copyrighted with all rights reserved worldwide to Motorola. Laws in the United States and other countries preserve for Motorola, Inc. certain exclusive rights to the copyrighted computer programs, including the exclusive right to copy, reproduce, modify, decompile, disassemble, and reverse-engineer the Motorola computer programs in any manner or form without Motorola's prior written consent. Furthermore, the purchase of Motorola products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license or rights under the copyrights, patents, or patent applications of Motorola, except for a nonexclusive license to use the Motorola product and the Motorola computer programs with the Motorola product.

1.6 ABOUT THIS SERVICE MANUAL

Using this service manual and the suggestions contained in it assures proper installation, operation, and maintenance of D1000 Cards. Refer questions about this manual to the nearest Customer Service Manager.

A product family is the group of products having the same Account Product Code (APC). To locate the APC on a device, refer to "Mechanical Serial Number (MSN)" later in this manual.

1.6.1 Audience

This document aids service personnel in testing and repairing D1000 Cards. Service personnel should be familiar with electronic assembly, testing, and troubleshooting methods, and with the operation and use of associated test equipment.

Use of this document assures proper installation, operation, and maintenance of Motorola products and equipment. It contains all service information required for the equipment described and is current as of the printing date.

1.6.2 Scope

The scope of this document is to provide the reader with basic information relating to D1000 Cards, and also to provide procedures and processes for repairing the cards, including:

- Unit swap out
- Repairing of mechanical faults Basic modular troubleshooting Testing and verification of unit functionality
- Limited PCB component repair

1.6.3 Conventions

Special characters and typefaces, listed and described below, are used in this publication to emphasize certain types of information.

NOTE: Emphasizes additional information pertinent to the subject matter.

CAUTION: Emphasizes information about actions which may result in equipment damage.

WARNING: **Emphasizes information about actions which may result in personal injury.**

Information from a screen is shown in text as similar as possible to what appears in the display. For example, ALERTS.

Information that you need to type is printed in **boldface type**

1.6.4 Revisions

Any changes that occur after manuals are printed are described in Publication Revision Bulletins *(PMRs)*. These bulletins provide change information that can include new parts listing data, schematic diagrams, and printed-circuit board layouts.

1.6.5 Warranty Service Policy

The product will be sold with the standard 18-month warranty terms and conditions. Accidental damage, misuse, and extended warranties offered by retailers are not supported under warranty. Non warranty repairs are available at agreed fixed repair prices.

1.6.5.1 Out-of-Box Failure Policy

The standard out of box failure criteria applies. Customer phones that fail very early on after the date of sale, are to be returned to Manufacturing for root cause analysis, to guard against epidemic criteria. Manufacturing to bear the costs of early life failure.

1.6.5.2 Product Support

Customer's original phones will be repaired but not refurbished as standard. Appointed Motorola Service Hubs will perform warranty and non-warranty field service for level 2 (assemblies) and level 3 (limited PCB component). The Motorola HTC centers will perform level 4 (full component) repairs.

1.6.5.3 Customer Support

Customer support is available through dedicated Call Centers and in-country help desks. Product Service training should be arranged through the local Motorola Support Center.

1.6.5.4 Parts Replacement

When ordering replacement parts or equipment, include the Motorola part number and description used in the service manual or supplement.

When the Motorola part number of a component is not known, use the product model number or other related major assembly along with a description of the related major assembly and of the component in question.

To order parts online, visit:

https://servicelink3.motorola.com.
(contact the EMEA Service Parts Group for the password required)

You can contact the EMEA Service Parts Group at: **+44 131 79 1274**.

2.1 SPESIFICATIONS

The following tables describe the D1000 card specifications.

Table 1. Specifications

General Function	Specification
Frequency Range E GSM	**TX:** 876 - 915 MHz Frequency (MHz) = 890 + (0.2 x n) where: 0 ≤ n ≤ 124 Frequency (MHz) = 890 + (0.2 x (n - 1024)) where: 955 ≤ n ≤ 1023 **RX:** 921 - 960 MHz Frequency (MHz) = 935 + (0.2 x n) where: 0 ≤ n ≤ 124 Frequency (MHz) = 935 + (0.2 x (n - 1024)) where: 955 ≤ n ≤ 1023
Frequency Range DCS	**TX:** 1710 to 1785 MHz Frequency (MHz) = 1710 + (0.2 x (n - 511)) where: 512 ≤ n ≤ 885 **RX:** 1805.2 to 1879.8 MHZ Frequency (MHz) = 1805 + (0.2 x (n - 511)) where: 512 ≤ n ≤ 885
Frequency Range PCS	**TX:** 1850 to 1910 MHz Frequency (MHz) = 1850 + (0.2 x (n - 511)) where: 512 ≤ n ≤ 810 **RX:** 1930 to 1990 MHZ Frequency (MHz) = 1930 + (0.2 x (n - 511)) where: 512 ≤ n ≤ 810
Frequency Range UMTS	**TX:** 1920 to 1980 MHz Frequency (MHz) = UARFCN1 / 5 where: 9612 < UARFCN1 < 9888UARFCN[1] in increments of 25 **RX:** 2110 to 2170 MHz Frequency (MHz) = UARFCN1 / 5, where: 10562 < UARFCN1 <10838UARFCN[1] in increments of 25
Channel Spacing	200 kHz (GSM, DCS, PCS), 5MHz UMTS
Channels	174 EGSM, 374 DCS, 274 PCS carriers with 8 ch. Per carrier, 11UMTS
Duplex Spacing	45 MHz GSM, 95 MHz DCS, 80 MHz PCS, 190 MHz UMTS
Modulation	GMSK AT BT = 0.3 (GSM, DCS, PCS), QPSK (UMTS)
Transmitter Phase Accuracy	5 degrees RMS, 20 degrees peak
Frequency Error	+ 0.1ppm
Input/Output Impedance	50 ohms (nominal)
Nominal Operating Voltage	5.0 Vdc ± 5%
PC Card class	16-bit PC Card
PC Card Type	Extended full-size Type II
Dimensions	133.5 x 54 x 13 (mm)

Table 1. Specifications *(Continued)*

General Function	Specification
Volume	51 cc
Weight	70 g,
Operating Temperature Range	0°C to +55°C
Storage Temperature Range	-20°C to +70°C

[1]UTRA Absolute Radio Frequency Channel Number (UARFCN)

Table 2. GSM System

General Function	Specification
Speech Coding Type	Regular Pulse excitation / linear predictive coding with longterm prediction (RPE LPC with LTP)
Bit Rate	13.0 kbps
RF Power Output	32 dBm nominal GSM, 30 dBm nominal DCS / PCS
Receive Sensitivity	-107 dBm GSM, -105 dBm DCS / PCS
RX Bit Error Rate	< 2%

Table 3. UMTS System

General Function	Specification
Speech Coding Type	Adaptive Multirate (AMR)
RF Power Output	21 dBm nominal WCDMA
Error Vector Magnitude	< 15%
PN9 Bit Error Rate (VER)	0.1% @12.2k, 0.1% @64k, 0.1% @384k
ACLR	0.1% @12.2k, 0.1% @64k, 0.1% @384k

PRODUCT OVERVIEW AND GENERAL OPERATION

3.1 PRODUCT OVERVIEW

The D1000 is a 3G PC Card device. It is an extended Type II PCMCIA card providing high speed data connections via cellular networks. It provides mobile user connection speeds comparable to wired ADSL connections. Additionally, for F3024AA only, the earpiece supplied with the 3G PC card, enables the user to enjoy D1000 voice capabilities.

As a 3G product, the D1000 complies with all key specifications as defined by the 3GPP. Key product features are:

- UMTS: WCDMA 2100, GSM 900/1800 and 1900-MHz Tri-band technology,
- GPRS High speed packet data (1 UL, 4 DL),
- WCDMA High speed packet data (64kbps UL, 384 kbps DL),
- 16MB Integrated Flash Memory,
- Integrated Headset Jack
- External antenna support

NOTE:

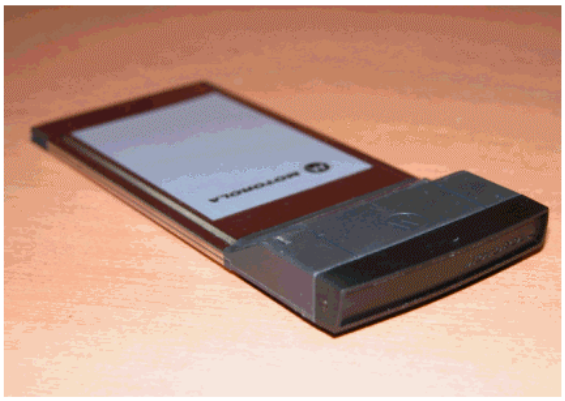
The listed features may be Network, subscription, or service provider dependent. Not available in all areas.

3.2 GENERAL OPERATION

Beside of being a UMTS High data rate PCMCIA card, the D1000 can also perform a regular audio call using earpiece and mPT SW (included).(model F3024AA only).

3.2.1 Introduction and General Description:

3.2.1.1 Antenna Opening



D1000 - Antenna Closed

D1000 - Antenna Open

Figure 1. Antenna Opening

3.2.1.2 D1000 Connectors

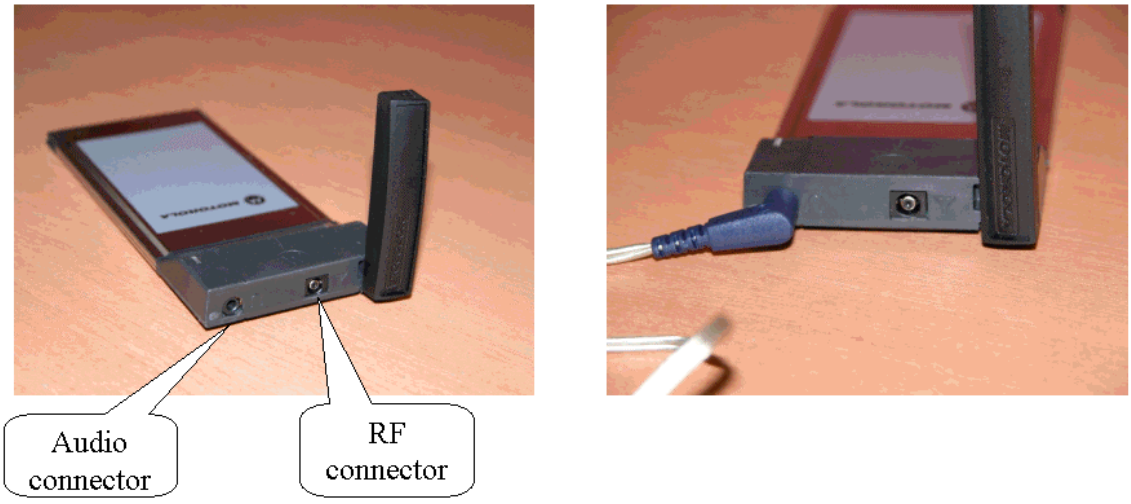


Figure 2. Antenna Connectors

NOTE:

Insert USIM card according to the mark (imprint) on D1000, wrong direction can damage USIM card.

3.2.2 USIM Card Insertion

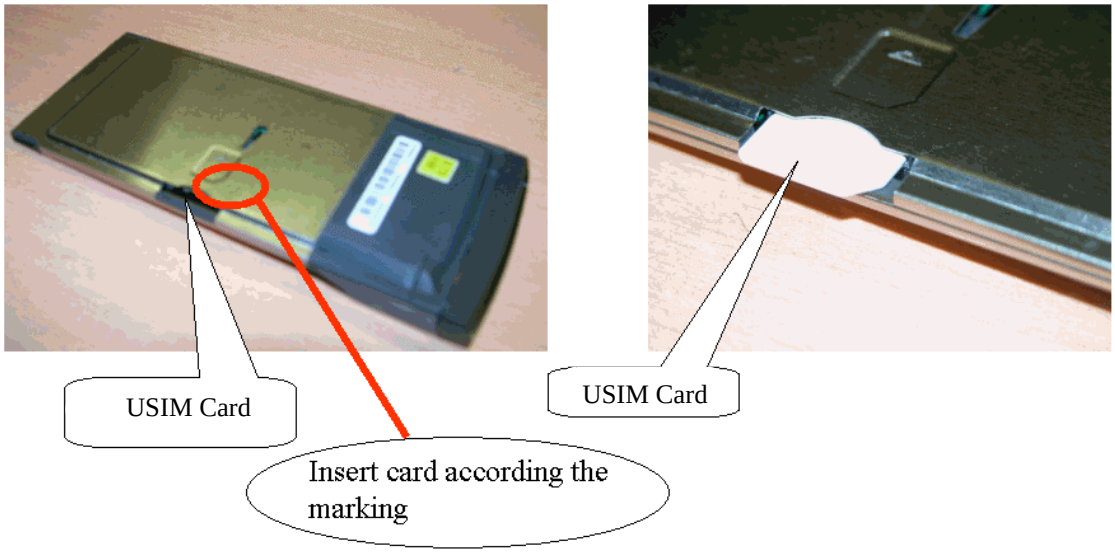


Figure 3. Usim Card Insertion

3.2.3 USIM Card Removal

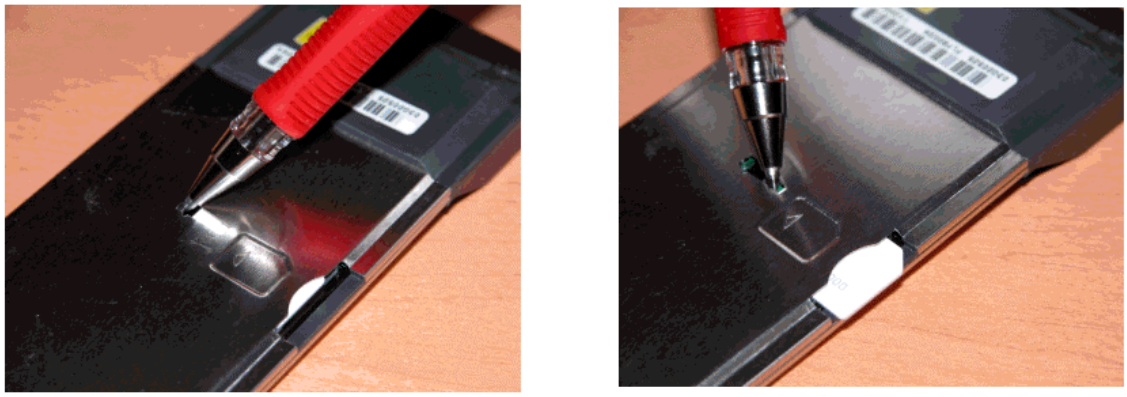


Figure 4. Removing the USIM Card (Using a pen)

3.2.4 Mounting of D1000 Card on a Laptop

1. Insert D1000 card to the appropriate slot on laptop.

2. Open the antenna.

Figure 5. Mounting the D1000 Card

Table 4. Kit contents

Item #	Item Description	Part Number	Quantity
1	D1000 PCMCIA Card	F3024AA (Data and Voice) F3027AA (Data only)	1
2*	Earpiece	SYN8419B (for F3024AA only)	1
3	mPT CD-ROM	9986141U08	1

* If applicable

3.2.5 System Requirements

The mobile Phone Tool (mPT) requires an IBM PC or compatible computer with the following minimum configuration:

Processor:	Pentium® II 233MHz or higher
Memory (RAM):	64 MB
PCMCIA slot:	At least one type II or III available
Free hard disk space for installation:	20 MB
Drive:	CD-ROM
Operating System:	Microsoft Windows® 2000 or XP
Language:	English

3.3 D1000 INSTALLATION

For D1000 Installation, refer to the D1000 Safety and Operation Guide (included in the mPT CD ROM).

TOOLS AND TEST EQUIPMENT

4.1 TOOLS AND TEST AQUIPMENT

This section describes the tools and test equipment needed for the D1000 card operation

Table 5 lists the tools and test equipment used on D1000 cards. Use either the listed items or equivalents.

Table 5. General Test Equipment and Tools

Motorola Part Number	Description	Application
0180386A82	Antistatic Mat Kit (includes 66-80387A95 antistatic mat, 66-80334B36 ground cord, and 42-80385A59 wrist band)	Protects the card from damage caused by electrostatic discharge (ESD)
FCN6475A	Interface Board	Provides an interface for flashing, phasing and testing.
Duel p/n ds8814[1]	Duel p/n ds8814 rework tool	Tool for ultrasonic welded PC Cards disassembly
“Branson 900 plus” and Welding fixture[2]	Ultrasonic welding machine	PC Card housing ultrasonic welding.
	Mini flat-tip screwdriver	Removing and Replacing the Antenna

1. Not available from Motorola. To order, contact:
   Duel systems
   Contact - Michael Chao, Engineering Manager
   Tel 408 436 4931, Fax 408 436 6063
   Michael_chao@duel-systems.com
   1750 Junction Ave., San Jose CA 95112).
2. Not available from Motorola. To order, contact:
   Branson welding machine and welding fixture ordering info:
   Tel (203) 796-0576, fax (203) 796-0574
   partstore@bransonultrasonics.com
   Branson Ultrasonic Corporation,
   Applied Technologies Group,
   41 Eagle Rd., Danbury, CT 06813-1961 USA

4.2 INTERFACE BOARD OVERVIEW

The Interface Board serves as an interface between the D1000 card and the host PCMCIA interface, a USB or a RS232 port of a PC. The interface board is used as a tool for programming and servicing D1000 cards. The D1000 card can be configured to the following modes:

1. **Normal Mode** - D1000 card communicates with the host notebook/PC via PCMCIA interface.
2. **Test Mode (CE Bus Mode)** - PCMCIA interface inside the D1000 card is bypassed, and CE bus signals from within the D1000 card are routed to the high address lines (not used by the D1000) on the 68-pin connector, and from there, to the CE Bus Connector on the interface board. The CE Bus provides USB and RS232 interfaces similar to standard 3G phones. Test mode is used for fleshing, flexing, phasing, etc.

4.3 INTERFACE BOARD ILLUSTRATION

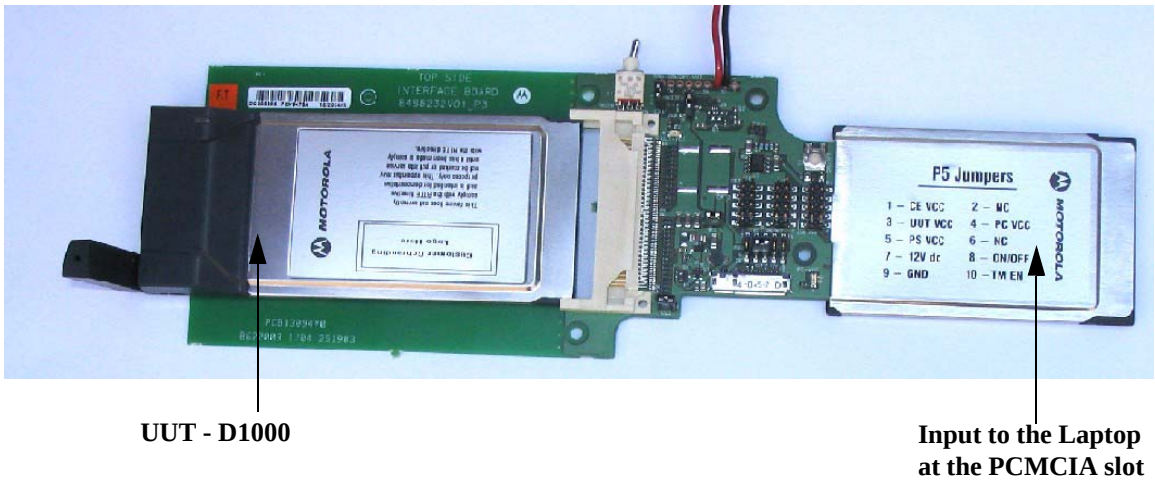


Figure 6. Interface Board Illustration

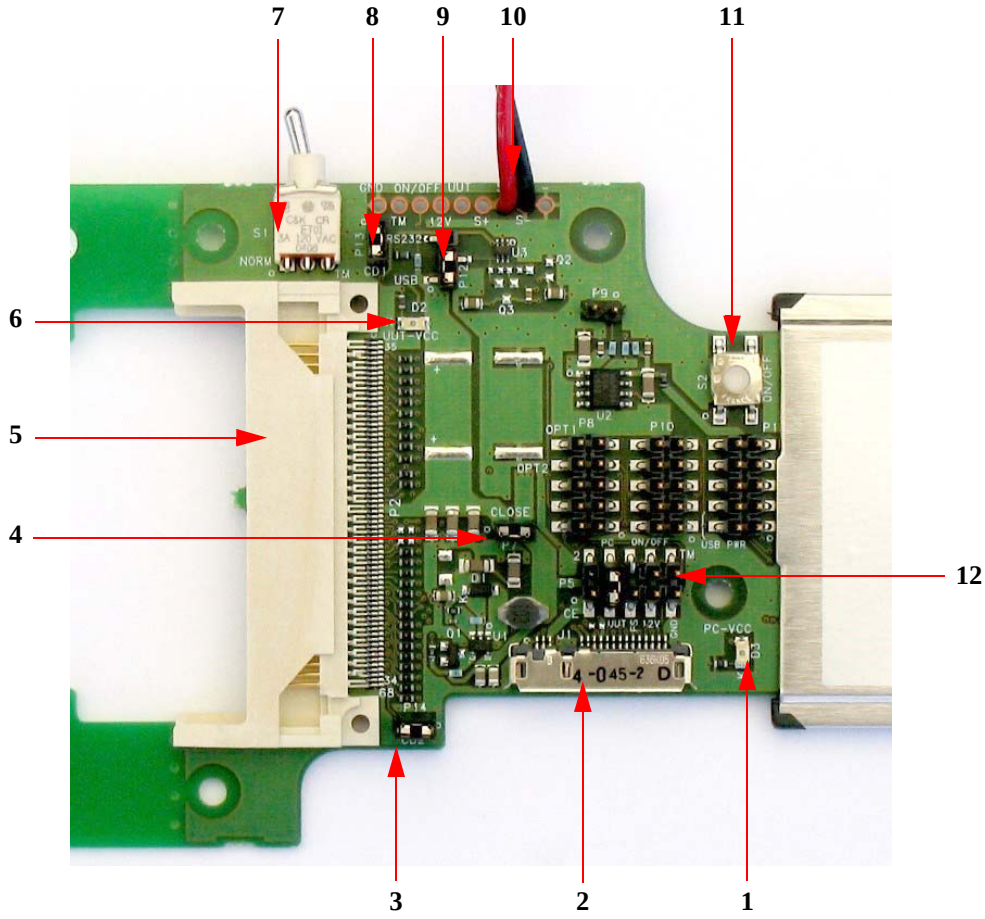


Figure 7. Board Description

1. **PC-VCC LED Indicator**
2. **CE bus Connector (J1)**
3. **CD2** (Card Detect 2) Jumper **P14**
4. UUT VCC Jumper **P7**
5. Connector **P2** - connecting the UUT
6. **UUT-VCC LED Indicator**
7. Switch **S1** - Left: **NORM** (Normal Mode as shown)
   Right: **TM** (Test Mode)
8. **CD1** (Card Detect 1) Jumper **P13**
9. USB/RS232 Setup Jumper **P12 -** use in Test Mode:
   USB: put Jumper Down (as shown).
   RS232: put Jumper up.
10. **Power Supply:** Connect 5.0Vdc to the red (+) and black (-) wires.
11. **ON/OFF** Push Button (active in Test Mode only)
12. **Jumpers P5:**
    To provide Voltage from the PC usually in Normal Mode place jumper on pins 3-4.
    To provide Voltage from the Power Supply usually in Test Mode: place jumper on pins 3-5 (as shown).

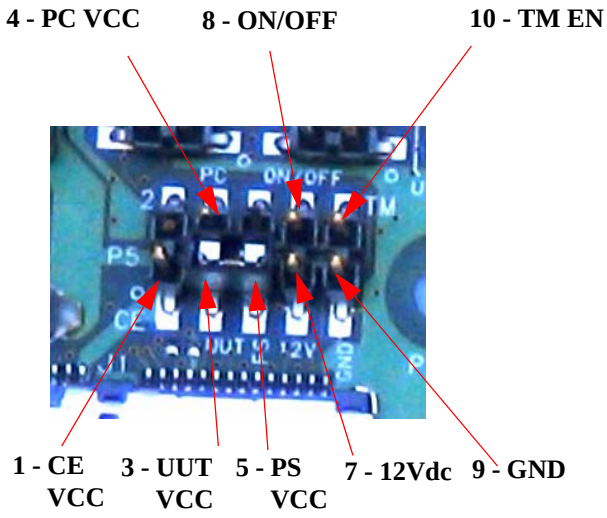


Figure 8. P5 Jumpers

4.4 NORMAL MODE

Setup

1. Insert a jumper on **P13** (Card Detect 1) and **P14** (Card Detect 2) headers.
2. Insert a jumper on **P5** pins 3-4.
3. Insert a jumper on **P7**.
4. Set Switch S1 to NORM (Normal Mode).
5. Insert the D1000 card to P2 (68 pin male connector).
6. Connect the Interface board to the Laptop.

Now the 2 LEDs should be light **ON** and the PC will recognize the D1000 as PCMCIA.

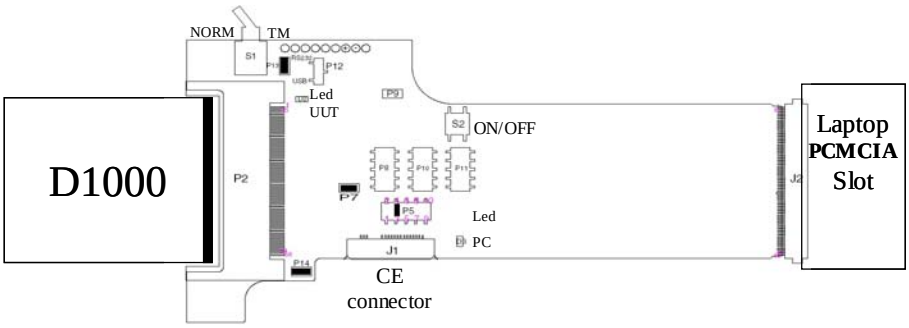


Figure 9. Setup Connections

4.5 TEST MODE

Setup

1. Place a jumper on **P7** header.
2. Place a jumper on **P5** pins 3-5.
3. Switch S1 to TM (Test Mode).
4. Insert the D1000 to P2 (68 pin male connector).
5. Connect the Interface board on J1 to RS232 or USB CE cable.
6. Supply 5Vdc to the red (+) and the GND black (-) wires.
7. Place a jumper on **P12** header for USB or RS232 (USB Mode shown).

Only one LED will light - UUT-VCC should be on.

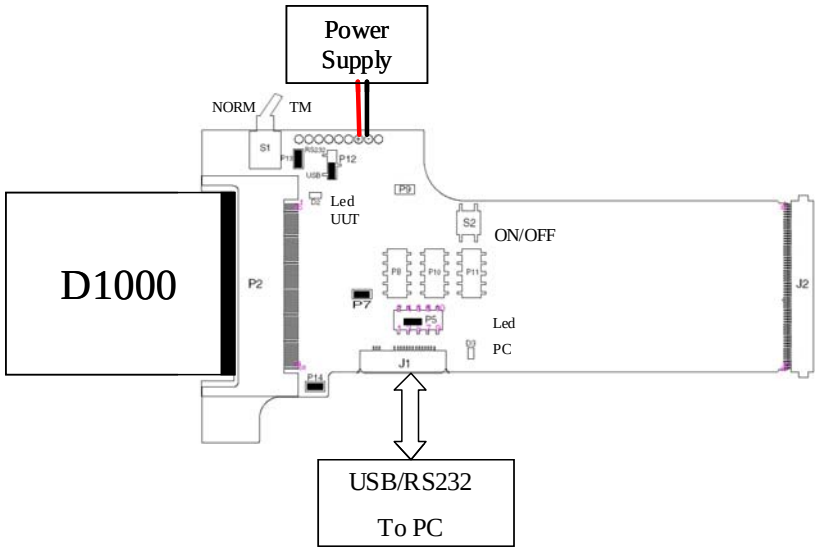


Figure 10. Test Connections

D1000 FLASH/FLEX PROCEDURE

5.1 INTRODUCTION

This document is intended to describe the Flashing (software updates) procedures for D1000 Card and Card Information Structure (CIS) programming or update.

The User should handle the Software updates in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the correct software is programmed.

Software updates allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific conditions, therefore, not all the units will contain identical software.

5.2 HARDWARE REQUIREMENTS

The following hardware is required to properly flash and flex the D1000 card.

5.2.1 Power options

1. Laptop
2. Power supply

5.2.2 Interface Options

1. USB Data Kit(S8951)
   USB Cable (SKN6311B)
2. RS232 Data Kit(S8952)
   RS232 Cable (SKN6315B)
   RS232 to CE converter (SYN0279B)
3. Interface board (FCN6475A)

5.3 SOFTWARE REQUIREMENTS

The Product Support Tool (PST) is used to allow functions such as flashing and memory transfers. Contact your local Motorola service representative to receive download information for the PST and related support files.

For download information on Flash software, contact your local Motorola representative.

5.4 D1000 FLASHING

Prior to performing the flashing procedure, make sure that all hardware connections are secured. Refer to Figure 11 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a non-functional (Bricked) D1000 card.

The D1000 card contains a Flash EPROM with a total memory of 16MB. The memory resides within two 8MB Intel Flash devices connected in parallel.

5.5 POWER SOLUTIONS

There are 2 types of power solutions to perform a flashing procedure.

1. PCMCIA slot.
2. Power supply.

NOTE:

In option 2 it is highly recommended that the interface board will be out of the PC..

5.6 HARDWARE CONNECTION SOLUTIONS

There are two types of hardware solutions to perform a flashing procedure.

1. USB configuration (recommended) via USB cable (SKN 6311B).
2. RS232 configuration via RS232 Cable (SKN6315B).

NOTE:

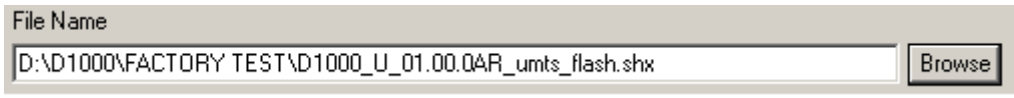
In option 1 and 2 you need to use the interface board.

RS232 configuration should be used only if the PC is running an operating system (OS) that doesn't support the USB interface. USB configuration will provide a faster data rate then RS232. As a result, flash duration will be reduced when using a USB connection.

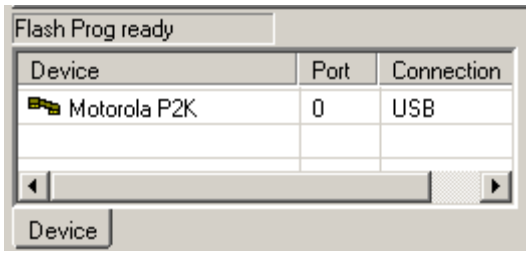
5.7 PST FLASH PROCEDURE

Use the listed procedure to complete the flash procedure for the D1000 card.

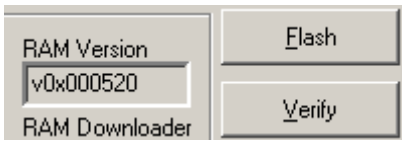
1. Download the desire software into the computer.
2. Connect the desired hardware configuration as illustrated in Figure 11. Make sure to place switch S1 into TM position (test mode), and jumper P12 set to USB (pins 1 and 2 shorted).
3. Power up the D1000 by pressing the ON/OFF switch (S2) for 2 seconds.
4. If the D1000 doesn't power up, refer to "Force Flash Procedure" section 5.8 .
5. Launch the PST application by choosing Start/Programs/Motorola PST/Flash & Test Commands.
6. Click on the Browser button and select the desired flash software.



7. Select the device that will be flashed.



8. Once the D1000 PCMCIA is placed in flash mode, the Flash button is enabled



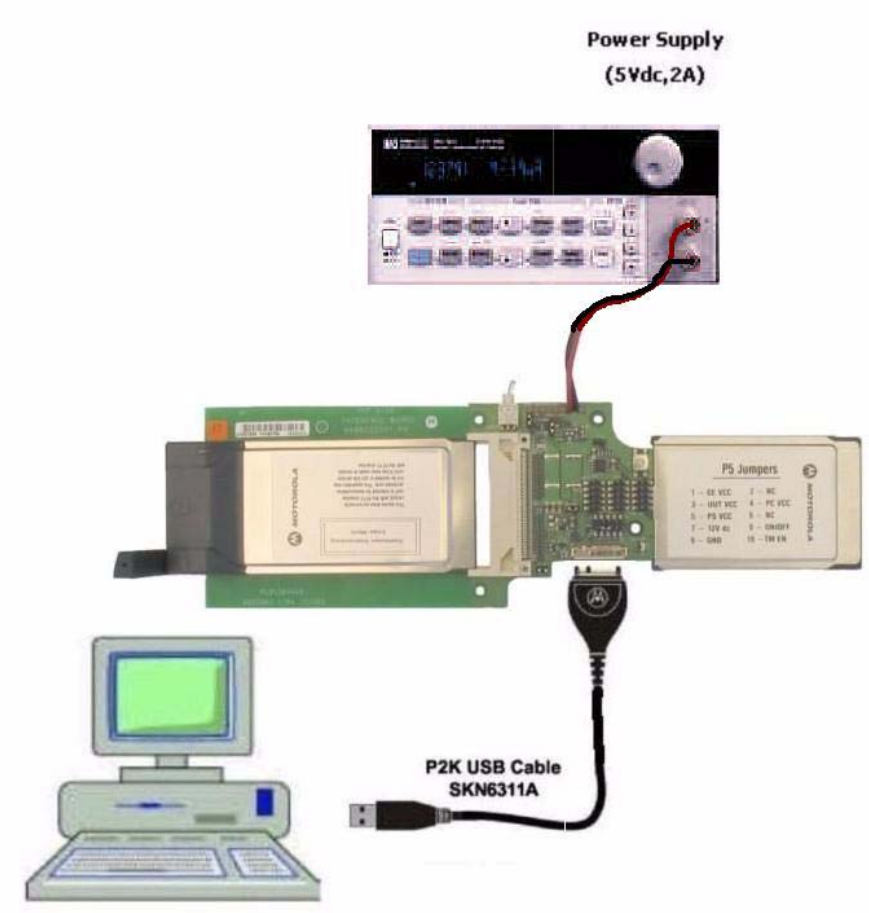


Figure 11. PST Hardware Configuration

9. Click on the Flash button to begin the flashing.

NOTE:

DO NOT interrupt any hardware connections during the flash process. Connection interruptions may cause the flashing process to fail and render the D1000 non-operational.

10. When flashing is complete, a message “Flash another phone?” appears. At this time you may safely disconnect the D1000 card and select the appropriate response.
11. Power up the D1000 card to insure that the flash procedure was successful.

5.8 FORCE FLASH PROCEDURE

The procedure described in this section applies only to situations where the D1000 card doesn’t initiate it’s normal power up sequence, but may recover functionality by a repeat flash procedure.

There are two possible alternatives to place the D1000 in force flash mode.

5.8.1 Option 1 option 2 solution

Step 1. Shorten pin 8 and pin 10 in P8 (look at the Interface board section)

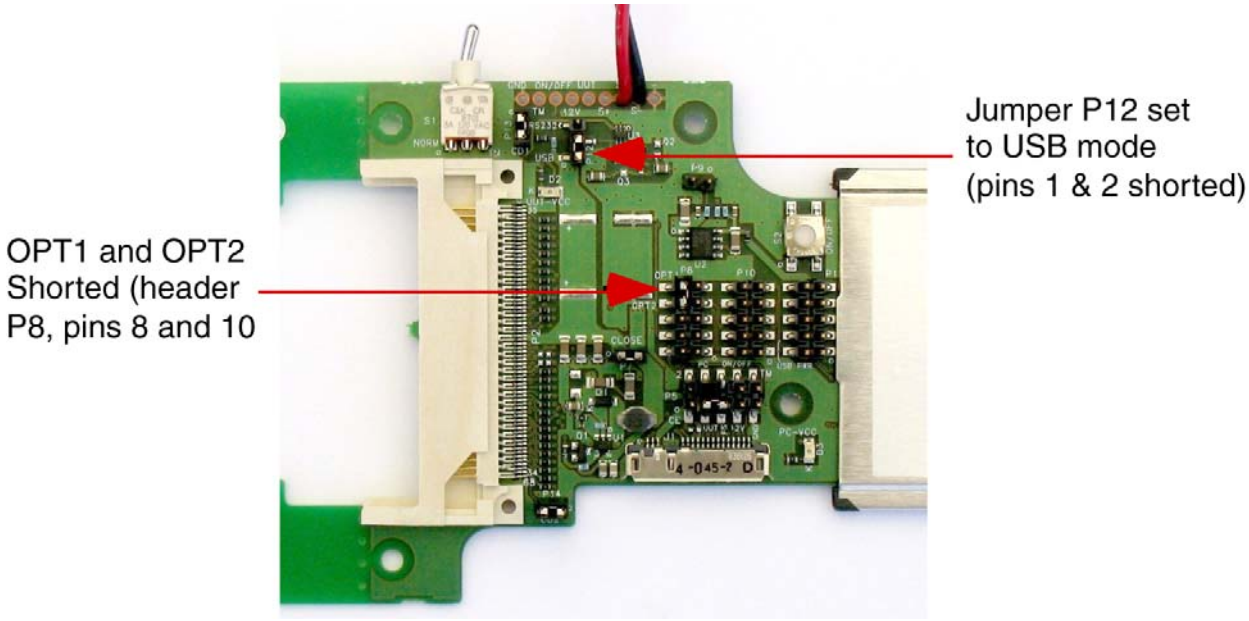


Figure 12. Jumper Settings

Step 2. Connect the USB cable to the interface board.

Step 3. Give power supply to the interface board by connecting it to an external power supply (set to 5.0V dc current limited to 2A).

Step 4. Verify that the PST application detects the D1000.

Step 5. Perform PST Flash Procedure steps 8 through 11.

5.8.1.1 Force Flash USB Cable Solution

Hardware: refer to Figure 11 (USB solution), except, replace USB cable (SKN6311B) with force flash cable (SKN6168A).

Step 1. Connect the force flash cable into the interface board as described in Figure 11.

Step 2. Give power supply to the interface board by connecting it to an external power supply.

Step 3. Verify that the PST application detects the D1000.

Step 4. Perform PST Flash Procedure steps 8 through 11.

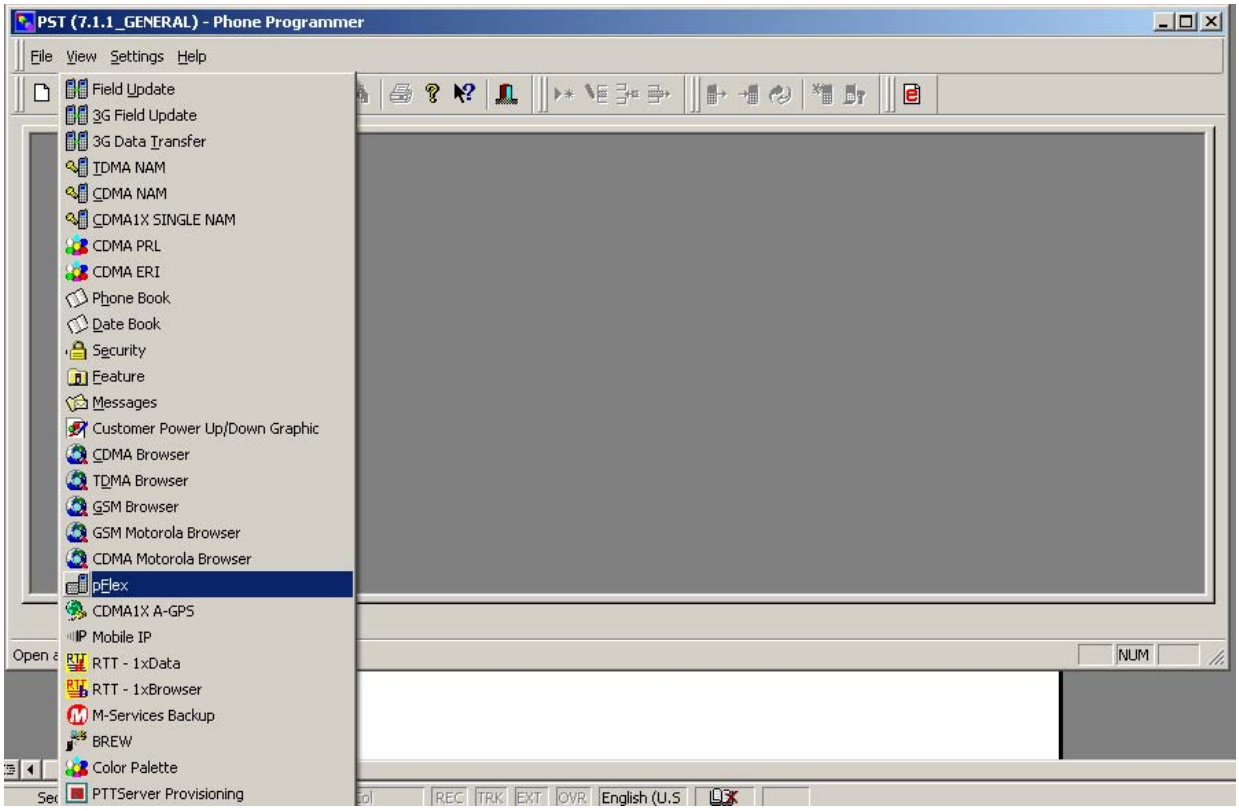
5.8.2 PST flex Procedure

Use the listed procedure to complete the flex procedure for the D1000.

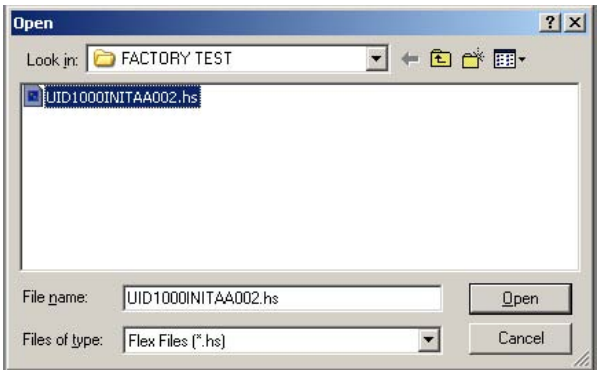
You can use the PST or the RadioComm in order to perform the flex procedure.

5.8.2.1 PST

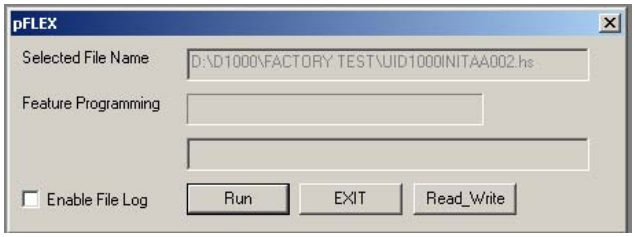
1. Download the desire Flex file into the computer.
2. Connect the desired hardware configuration as illustrated in Figure 11.
3. Power up the D1000.
4. Launch the PST application by choosing Start/Programs/Motorola PST/Phone Programmer.
5. Choose the flex option by choosing File -> open and choosing the pFlex option.



6. Browse to the location of the desired flex file, highlight it and press “Open”.



7. Press on the “Run” button.

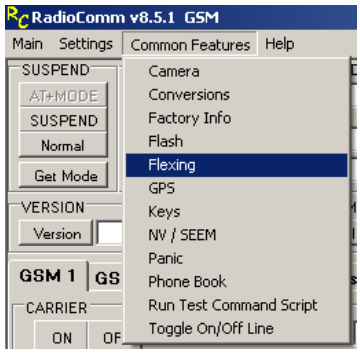


5.8.2.2 RadioComm

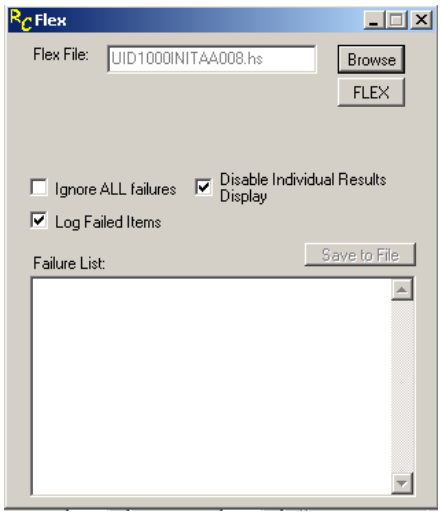
This section refers to the last released RadioComm version for this date (RadioComm V8.5.1).

NOTE:
The flex option is available only with full release of RadioComm.

1. Connect the desired hardware configuration as illustrated in Figure 11.
2. Power up the D1000.
3. Launch the RadioComm application by choosing Start/Programs/RadioComm/RadioComm v8.5.1.
4. Go to Common features menu item and press on the “Flexing”.



5. Browse to desired Flex file highlight it andpress “Open”.



6. Press on the “FLEX” button.

5.8.2.3 Card Information Structure (CIS) Programming

CIS resides in a 256-bit serial E2PROM. To have D1000 card correctly recognized by the host, correct CIS must be programmed in E2PROM. This chapter describes tools and procedures required to correctly program the CIS. Two different tools are described below. Each can be used for E2PROM programming.

5.8.2.4 CIS Programming - Motorola Application

NOTE:

All instruction in this section refer for programming D1000 with blank EEPROM.

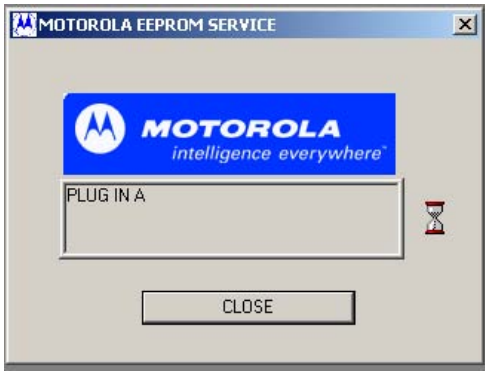
There are three scenarios in which the application operates:

- D1000 modem
- BLANK EEPROM
- Modem in REPAIR mode (refer to “Troubleshooting EEPROM”section 5.8.3)

CIS programming is done with “MEEPROMS.exe” program.

D1000 Scenario

1. Launch the “MEEPROMS.exe” application (Double click ).
2. After initialization, **MOTOROLA EEPROM SERVICE** window appears.



3. Insert D1000 to the PCMCIA driver. After a short pause the **MOTOROLA EEPROM SERVICE USER MODE** screen appears.

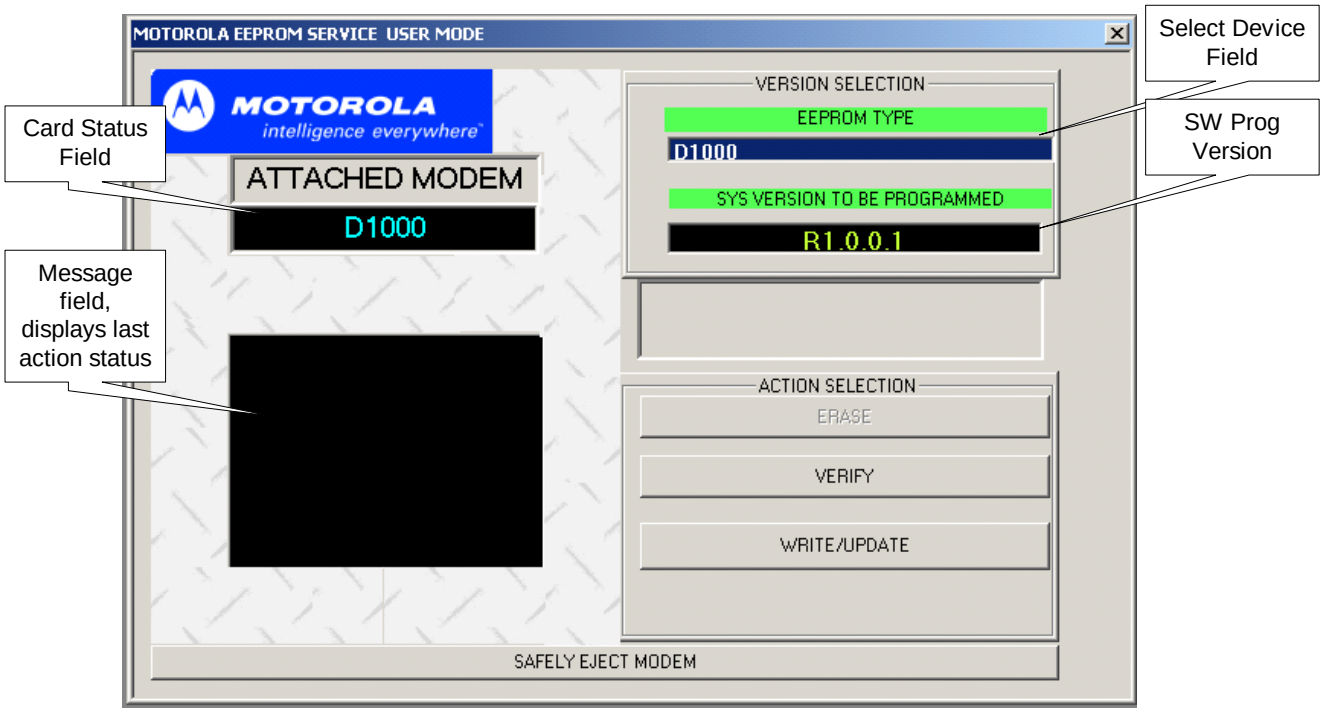


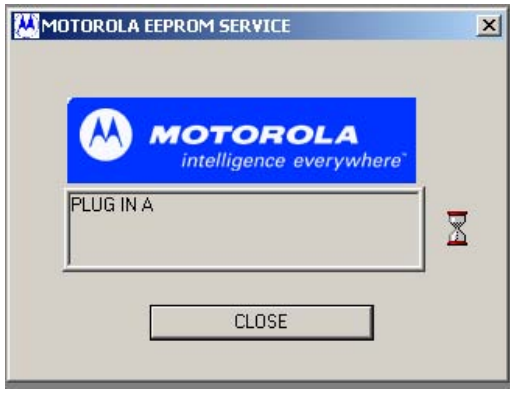
Figure 13. D1000 Scenario Screen

4. In *Card Status* field, "D1000" message appears.
5. In *Select Device* field list box, “D1000” appears. No selection can be made.
6. In *SW prog version* field the latest CIS is displayed.
7. Press *Verify* button (to authenticate modem data compared to last CIS version.) and wait for success / fail message to be displayed in the *Message field*. (Optional step)

8. Press the *Write/Update* button (to update EEPROM), and wait until the writing and the verifieing procedures are done. If If writing is succesfully completed, the program automatically sends a Windows command to eject mode and returns to the step 3. The  icon dsappears. In case of a failuer, a window containing error discriptions appears.
9. Press the *Safely Remove Device* button, and wait until the program returns to step 3. Preform this step if step *Write/Update* was skipped.
10. Remove D1000 from the PCMCIA slot.
11. Enter another modem or press "CLOSE" to exit application.

BLANK EEPROM scenario

1. Launch the “MEEPROMS.exe” application (Double click ).
2. After initialization, **MOTOROLA EEPROM SERVICE** window appears.



3. Insert BLANK EEPROM to the PCMCIA driver. After a short pause the **MOTOROLA EEPROM SERVICE USER MODE** screen appears.

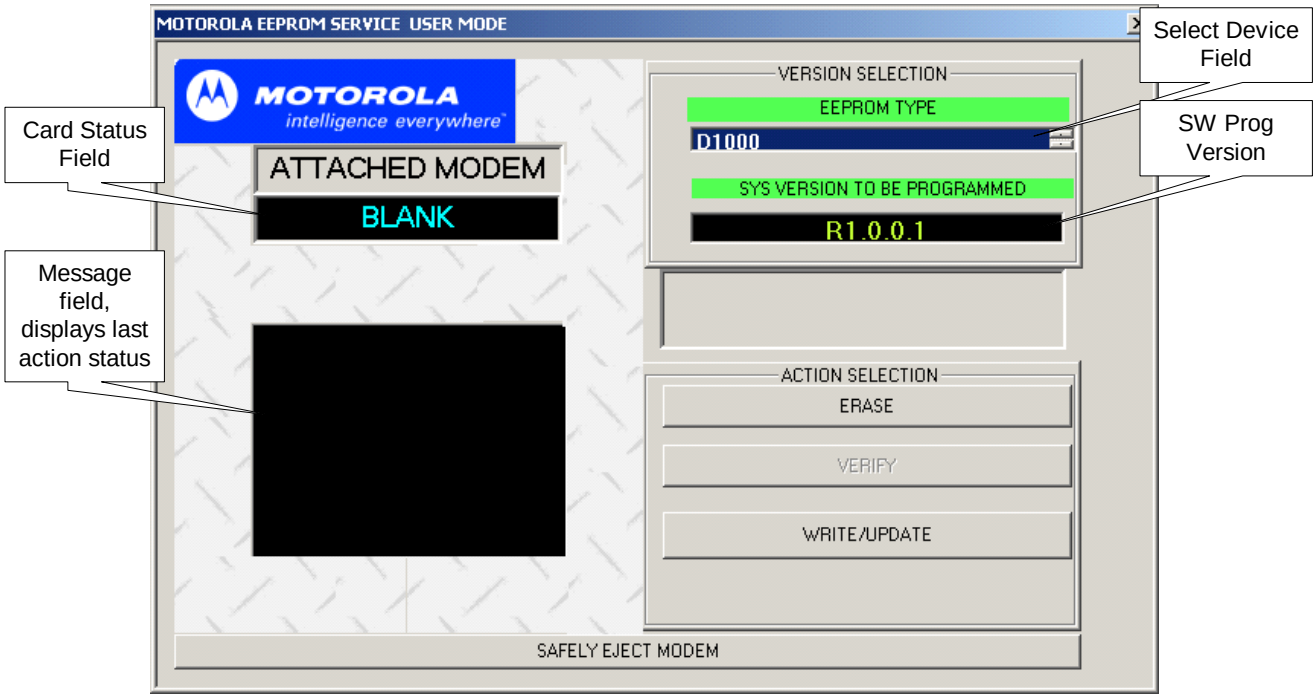


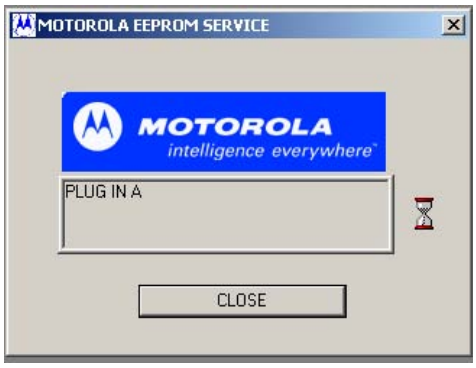
Figure 14. Blank EEPROM Scenario Screen

4. In *Card Status* field, "BLANK" message appears.
5. In *Select Device* field list box, a list of all available modem appears.
6. In *SW prog version* field the latest CIS version is displayed.

7. Press the *Write/Update* button (to program EEPROM), and wait until the writing and the verifieing procedures are done. If If writing is succesfully completed, the program automatically sends a Windows command to eject mode and returns to the step 3. The  icon dsappears. In case of a failuer, a window containing error discriptions appears.
8. Press the *Safely Remove Device* button, and wait until the program returns to step 3. Preform this step if step *Write/Update* was skipped.
9. Remove D1000 from the PCMCIA slot.
10. Enter another modem or press "CLOSE" to exit application.

REPAIR mode scenario

1. Launch the “MEEPROMS.exe” application (Double click ).
2. After initialization, **MOTOROLA EEPROM SERVICE** window appears.



3. Insert modem in REPAIR mode to the PCMCIA driver. After a short pause the **MOTOROLA EEPROM SERVICE USER MODE** screen appears.

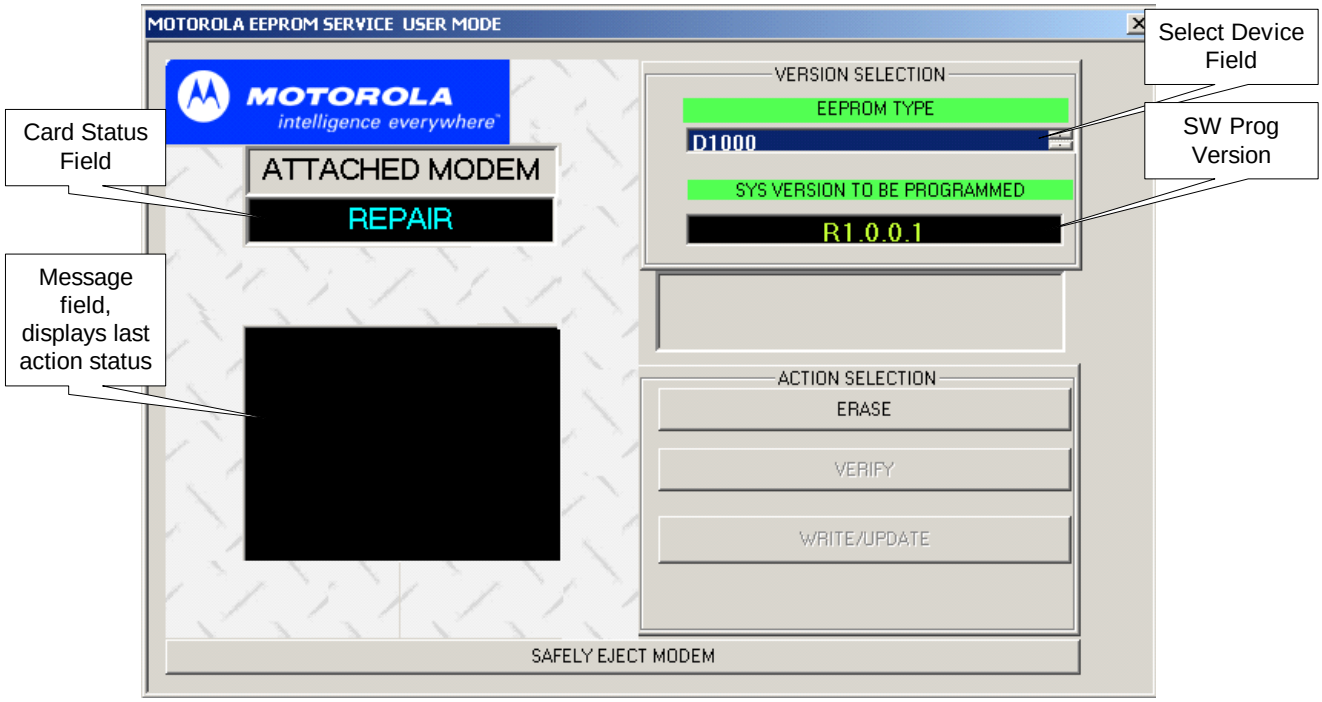


Figure 15. Repair Mode Scenario Screen

4. In *Card Status* field, "REPAIR" message appears.
5. In *Select Device* field list box, a list of all available modem appears.
6. In *SW prog version* field the latest CIS version is displayed.

7. Press *Erase* button and wait for the erasing to complete, if erasing is successfully completed, the program automatically sends a Windows command to eject mode and returns to the step 3. The  icon disappears. In case of a failure, a window containing error descriptions appears.
8. Press the *Safely Remove Device* button, and wait until the program returns to step 3.
9. Remove the modem from the PCMCIA slot.
10. Enter another modem or press "CLOSE" to exit application.

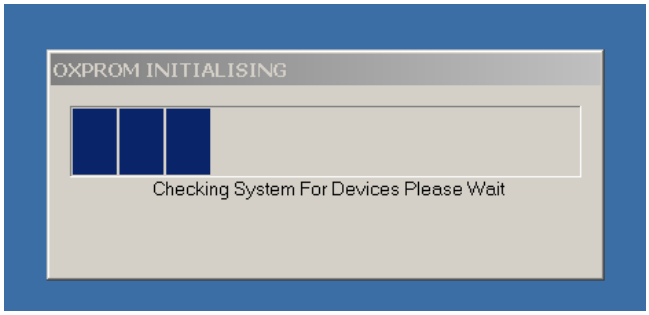
5.8.2.5 CIS Programming - Oxford Application

NOTE:

All instruction in this section refer for programming D1000 with blank EEPROM.

CIS programming is done with “OXPROM_r.exe” program, and uses a “*.dat” file.

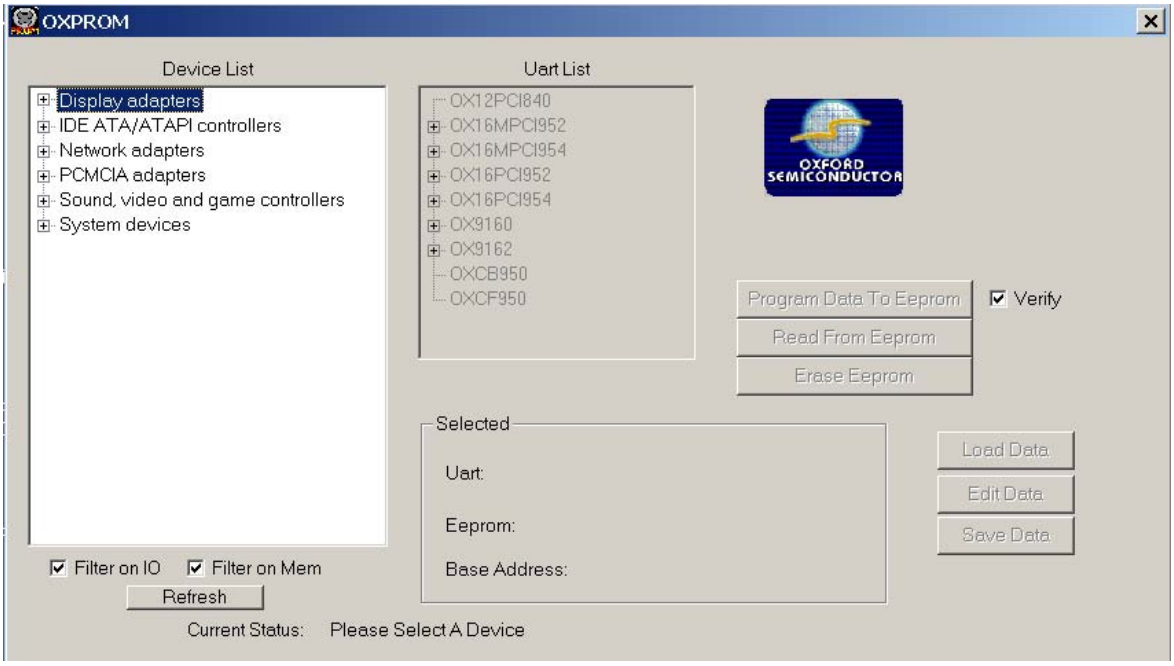
1. Download the desire “*.dat” file into the computer.
2. Insert D1000 to the laptop.
3. Launch the “OXPROM_r.exe” application (Double click ).
4. Initialization screen appears, and program initialization is performed.



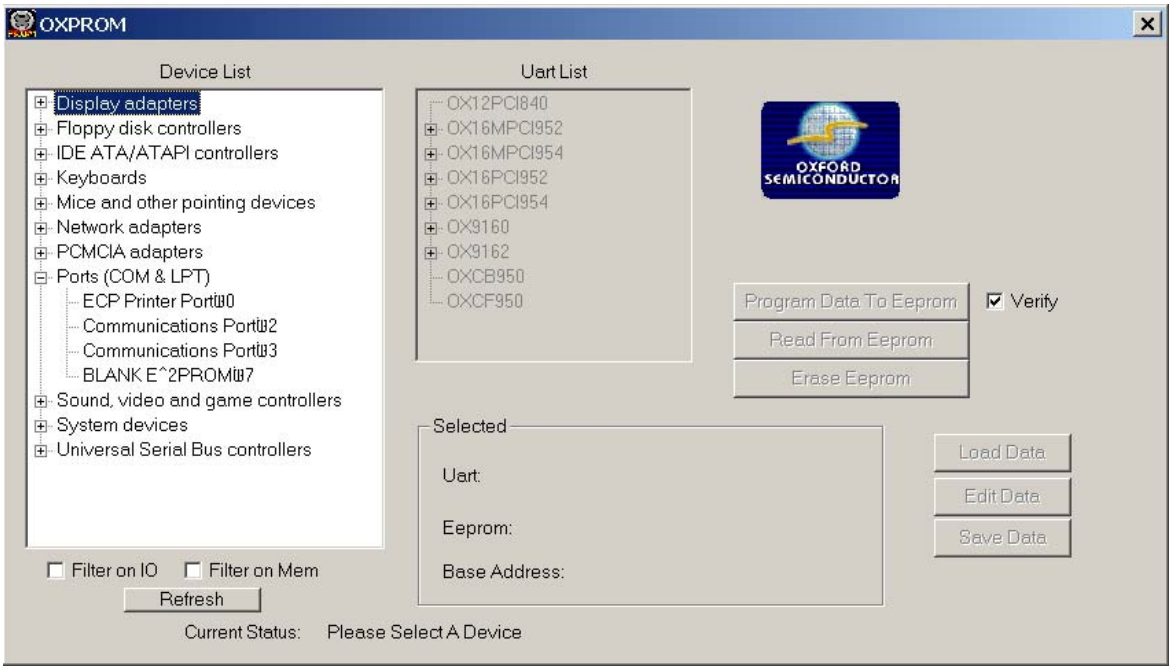
NOTE:

In the initialization process, more then one error massages may pop. Ignore massages by pressing the “OK” button on each massage.

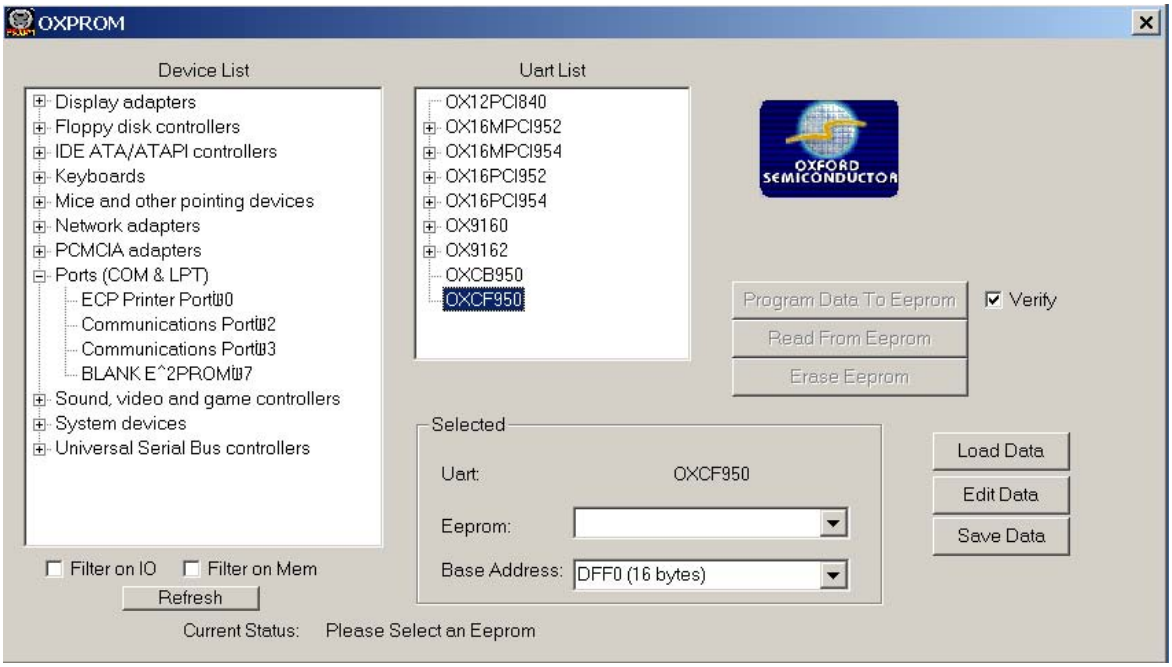
5. After initialization is complete, the program's main screen appears.



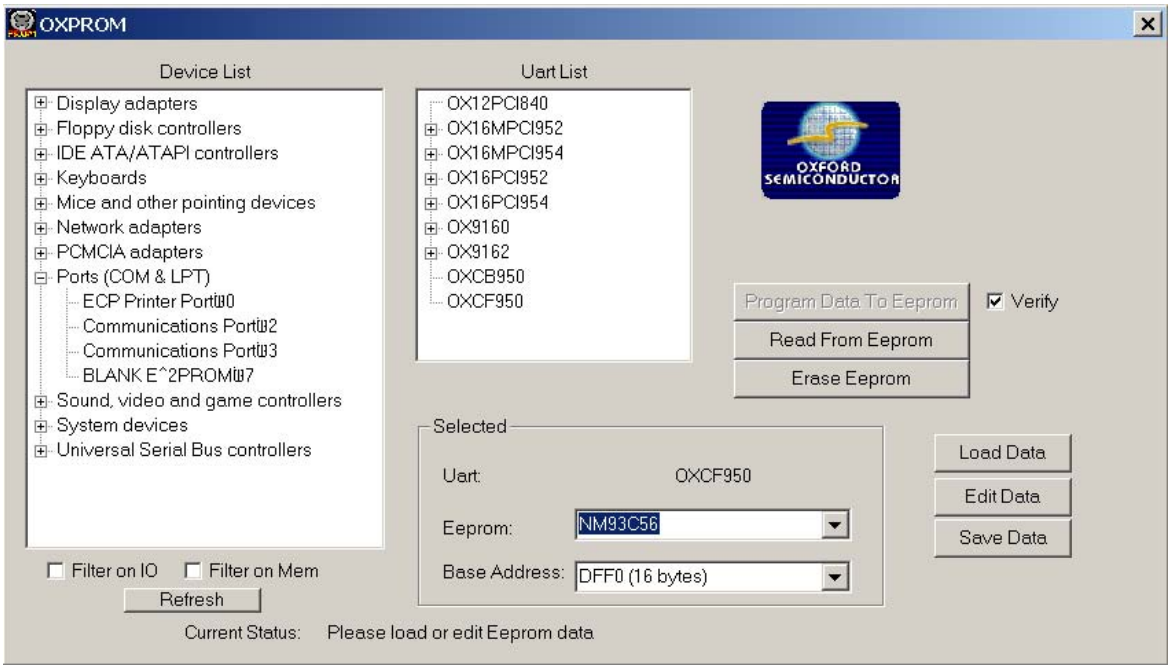
6. Unmark "Filter on IO" and "Filter on Mem" field on the bottom left, and press the "Refresh" button. In the Device list, device "Ports (COM & LPT)" appears.



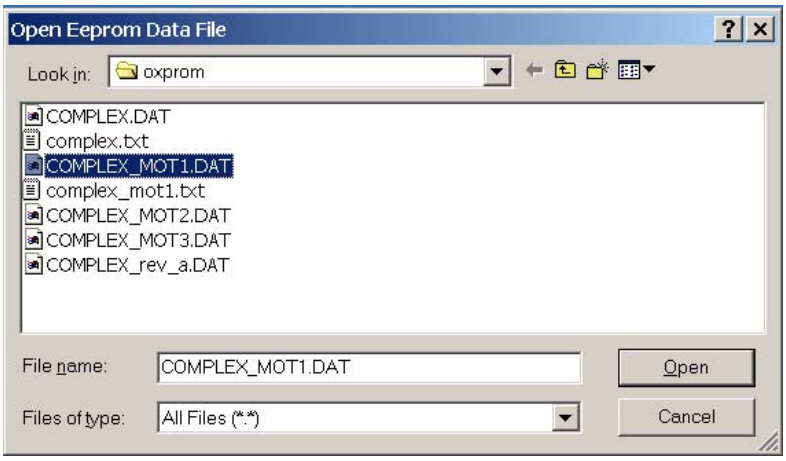
7. In the “Device List” double click Ports/BLANK EEPROM. In the “Selected” field (bottom center), the “Base Address” field appears. Mark the base address (This address is generated by the laptop). The “Uart List” is enabled.



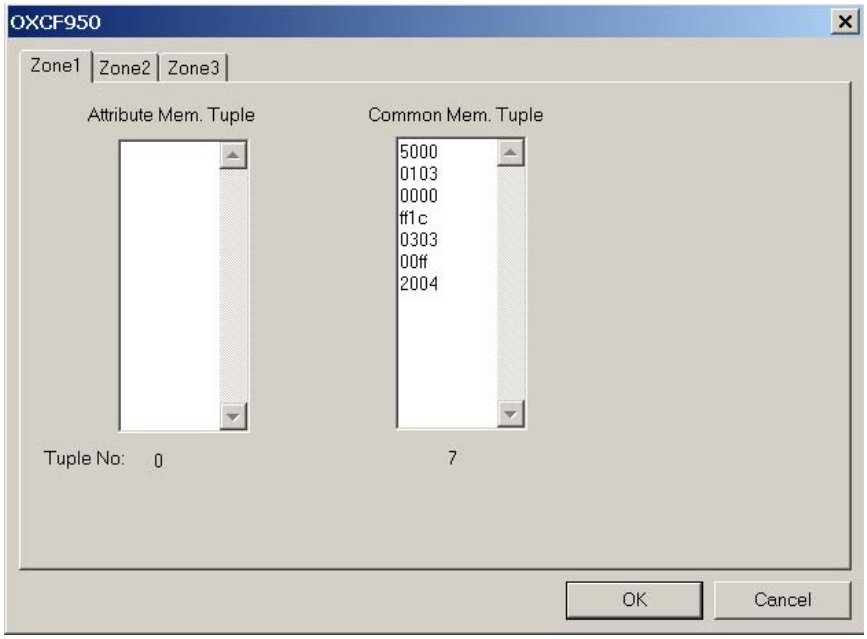
8. In the “Uart List” double click “OXCF950”, the “Eeprom” field appears. Select “NM93C56”.



9. Load a valid CIS file (this file ends with *.dat) by pressing the “Load Data” button at bottom right, “Open Eeprom Data File” window appears. Choose the desired dat file, and press “Open”.



10. The “OXCF950” window opens, press the **“**Cancel**”** button. The file is now loaded and ready for programming.



11. Press “Program data to Eeprom” button and wait a few second. Programe **completed** box appears.

12. Press “OK”.
13. Exit application.

5.8.3 Troubleshooting EEPROM

When the following problems occur:

- “Found New Hardware” wizard is reappearing.
- CIS programming fails.
- D1000 can not be recognized by the laptop.

perform the following steps:

1. Remove R6013 resistor (will be used later).
2. Redo steps 1 to 4 at CIS programming.
3. Press *Erase* (upper right) button, and wait a few second for the eeprom to be erased.
4. Press the *Safely Remove Device* (bottom left) button, and wait for finish OK massage in the *Massages Field* (center left).
5. Remove D1000 from laptop.
6. Place R6013 resistor back.
7. Perform steps 1 to 11. See “CIS Programming - Motorola Application”, section 5.8.2.4.

MANUAL TEST PROCEDURES

6.1 INTRODUCTION

The PC Card allows computer controlled testing of various digital test parameters.

This chapter describes the computer functions and recommended equipment setup to be used when testing a PC Card manually.

6.1.1 Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform an automatic call-processing tests. Automatic call processing tests can be performed when the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

NOTE:

The D1000 needs to be flexed with factory flex before the call processing tests. After the tests are done, the D1000 needs to be flexed with the customer flex.

6.1.2 Non-Signaling Test Measurements

When the PC Card causes RF failures that prevent call processing, the service technician may need to perform some non-signaling tests. These tests will provide information regarding which stage of the PC Card is failing prior to opening the card for troubleshooting. The following tests are described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The digital phasing parameters are stored in Flash devices. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted to the GPGate System. Checking and adjusting calibration parameters is also useful as a troubleshooting / diagnostic tool to isolate defective sections.

6.2 GSM/DCS/PCS CALL PROCESSING

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

6.2.1 Hardware Requirements

6.2.1.1 Power Options

Full-Rate Power Supply (PSM5049A)

6.2.1.2 Control Interface Options (PCS Only)

- USB Cable (SKN6311A)
- Serial Cable (SKN6315A) with CE converter (SYN0279B)

6.2.1.3 RF Interface (Everything listed is required)

- SMA/N-type Adaptor (0-00-00-40042)*
- SMA Cable 0.5m (0-00-00-40047)*
- USIM (0-00-00-40810)*
- RF Cable (02-0677, Description: MS-151-C(LP) TO SMA / F / B /RG316-MO)**
- *Contact AMS Software and Elektronik GmbH for ordering.
- ** Contact Astragal Ltd. for ordering, contact person:

  Moshe Hai

  e-mail: mosheh@astragal.co.il

  Tel : 972-3-5591660

  Mobile : 972-51-559672

  Fax : 972-3-5592340

  3 Hashikma St. Azur 58190, P.O.B. 99

  Israel

6.2.2 Software Requirements

The user should send a test command to the PC Card before performing the test. The command can be initiated through computer test commands.

6.2.2.1 Computer Test Command

RadioComm (latest release).

6.2.3 Call Origination (GSM and DCS only)

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adapted to any other test box that will be used to perform call processing.

To perform call processing:

1. Install the test USIM in the card.
2. Connect hardware as shown Figure 16.

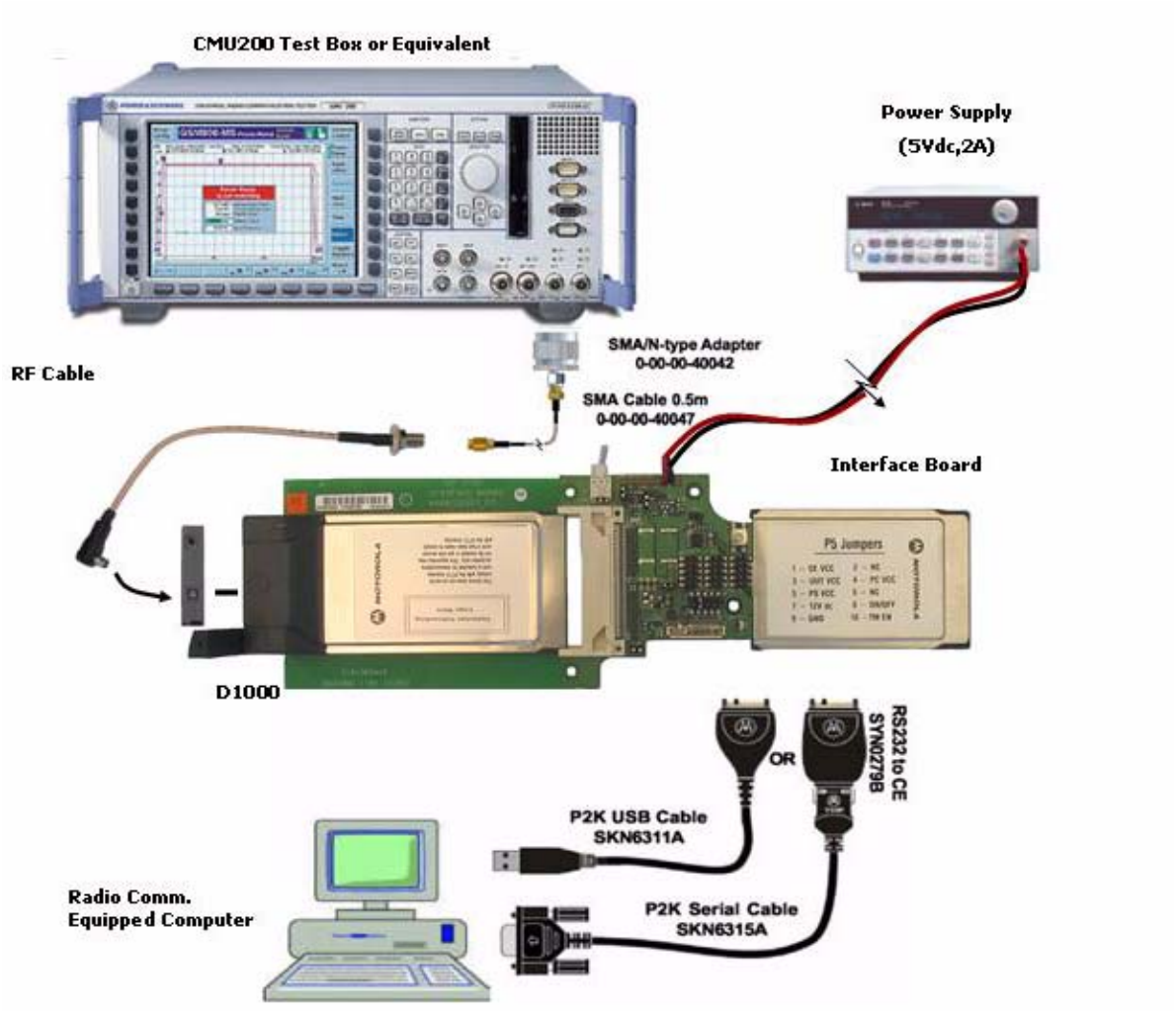


Figure 16. D1000 Manual Test Hardware Configuration

3. Setup up the test box for GSM or DCS Signaling.

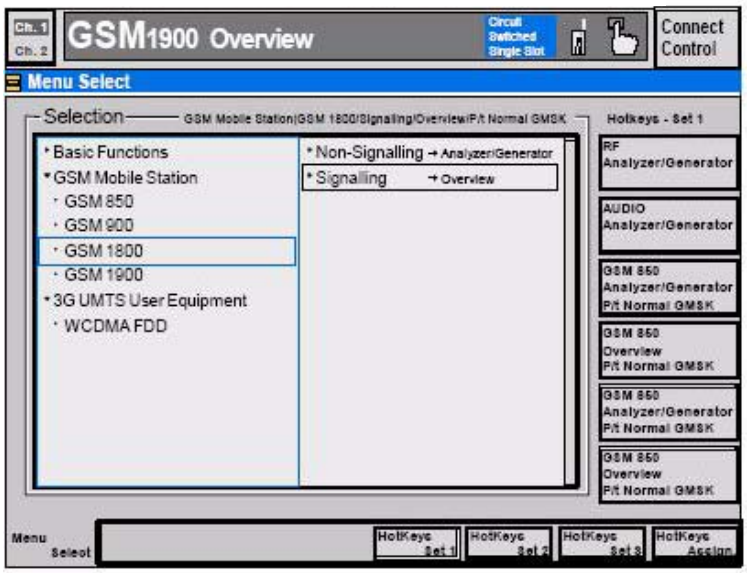


Figure 17. GSM Signalling Setup

4. Set Broadcast Channel (BCH) to 120 (GSM) or 700 (DCS).
5. Set Broadcast channel level to -85dBm.
6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS).
7. Set Traffic channel level to -85dBm.

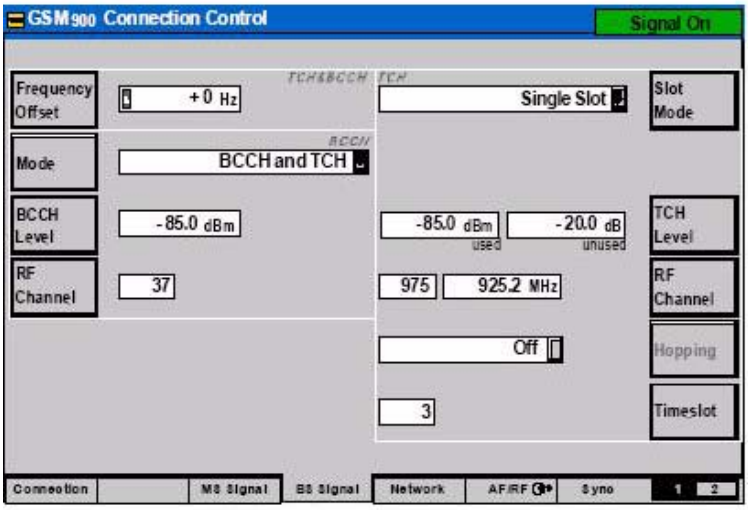
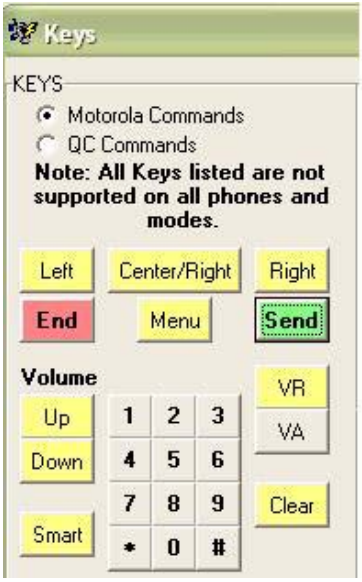


Figure 18. GSM Connection Control

8. Wait until the PC Card's Green LED starts flashing.
9. Dial a number using the RadioComm and press "send".



10. The PC Card is now connected.

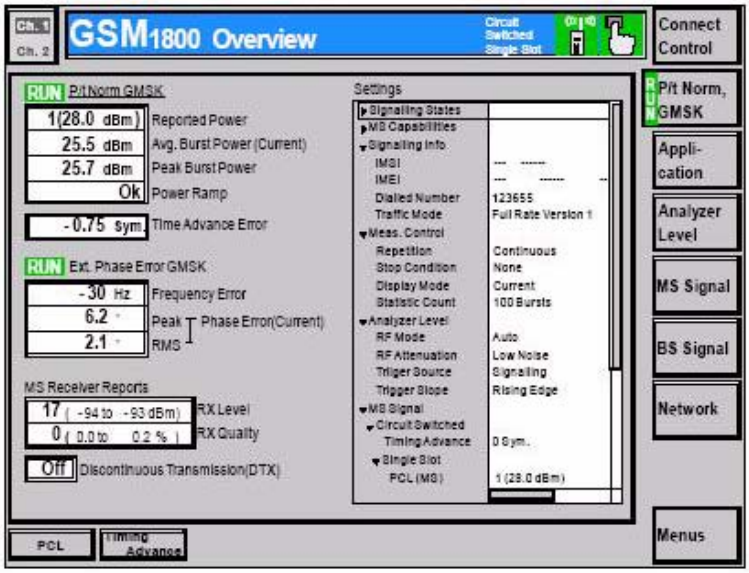


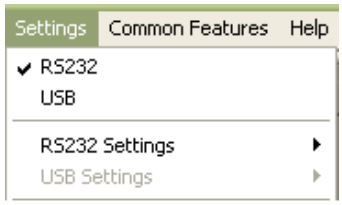
Figure 19. GSM Call Connected

6.2.4 Call Origination (PCS Only)

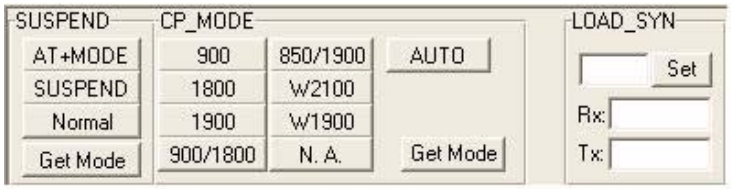
To perform Call Origination change the transceiver's mode to PCS.

6.2.4.1 Radio Comm Test Command

1. Connect as shown in Figure 16.
2. Power up the PC Card.
3. Start Radio Comm application.
4. Correctly select Settings option for USB or serial.



5. Click on AT+/mode, suspend, CP_Mode 1900, respectfully.



6. Power cycle PC Card

Repeat steps 1 through 10 in the, “Call Origination (GSM and DCS only),” section with the following modifications,

- Set PCS Signaling
- BCH = 661
- TCH = 512

Once the PCS call processing is complete, return the card to its original state by performing the following procedures:

6.2.4.2 Computer Test Command (Radio Comm) procedures:

1. Click on AT+/mode, Suspend, CP_Mode 900/1800, respectfully.
2. Power cycle PC Card.

6.2.5 Call Test Parameters (GSM/DCS/PCS)

When the PC Card under test is in an active call, the parameters for each band should be verified as described in Table 6.

Table 6. GSM Call Parameters

Parameter	LowLimit	HighLimit	Unit
Burst Avg Power Out[1]	31	33	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1] Power Level = 5

[2] Set BS TCH level to -105 dBm

[3] Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 7. DCS Call Parameters

Parameter	LowLimit	HighLimit	Unit
Burst Avg Power Out[1]	28.2	30	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

[1] Power Level = 0

[2] Set BS TCH level to -103 dBm

[3] Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 8. PCS Call Parameters

Parameter	LowLimit	HighLimit	Unit
Burst Avg Power Out[1]	28.2	30	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1] Power Level = 0

[2] Set BS TCH level to -104 dBm

[3] Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Burst Output Shape should fall within the standard limits of the Power Ramp.

BER measurements is only required if RX Quality reads a value of 4 or higher.

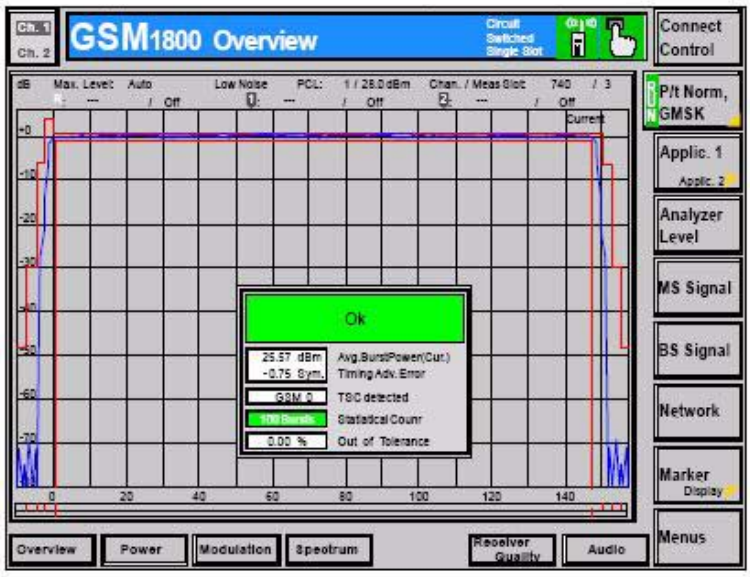


Figure 20. Burst Output Shape

It is recommended that handover procedures will be performed as shown in the following table.

Table 9. GSM/DCS/PCS Handover

Band	From		To	
	TrafficChannel	Pow e rControl	TrafficChannel	Pow e rControl
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

6.3 WCDMA CALL PROCESSING

In order to successfully complete a WCDMA call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through WCDMA base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

6.3.1 Hardware Requirements

Refer to “Hardware Requirements” section 6.2.1. Also Refer to Figure 16.

6.3.2 Software Requirements

Refer to “Hardware Requirements” section 6.2.1. Also Refer to Figure 16

6.3.3 Call Origination (WCDMA)

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signaling options installed. These procedures can be adopted to any other test box that will be used to perform call processing.

1. Install the test USIM in the card.
2. Connect hardware as illustrated in Figure 16.

3. Set up the test box for WCDMA FDD Signaling.

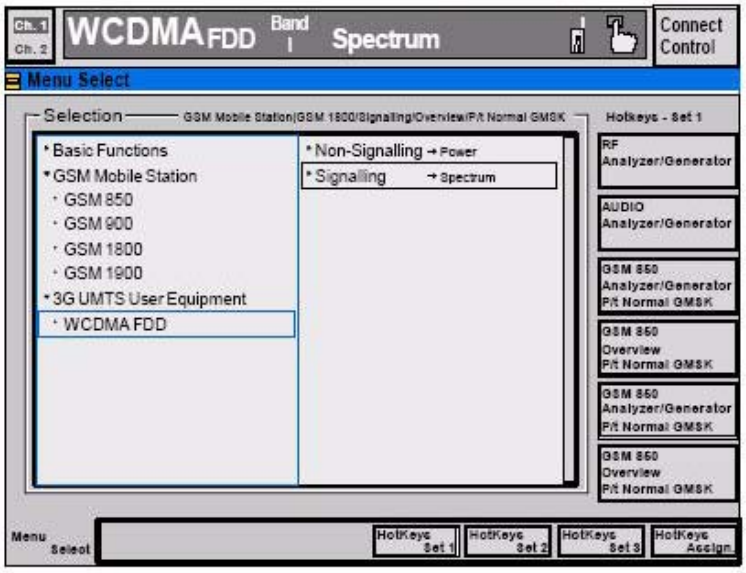


Figure 21. WCDMA Signalling Setup

4. Set UE Signal, RF Channel Uplink to 9750.

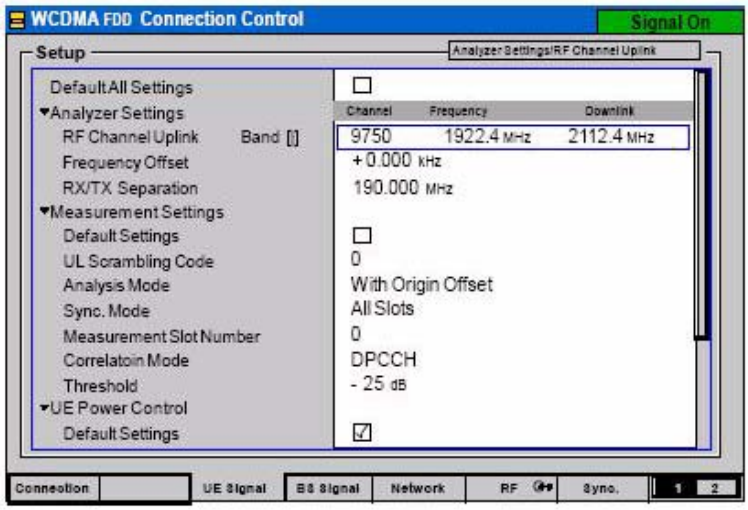


Figure 22. Channel Uplink(UE Signal)

5. Set TPC Pattern type to A11 1

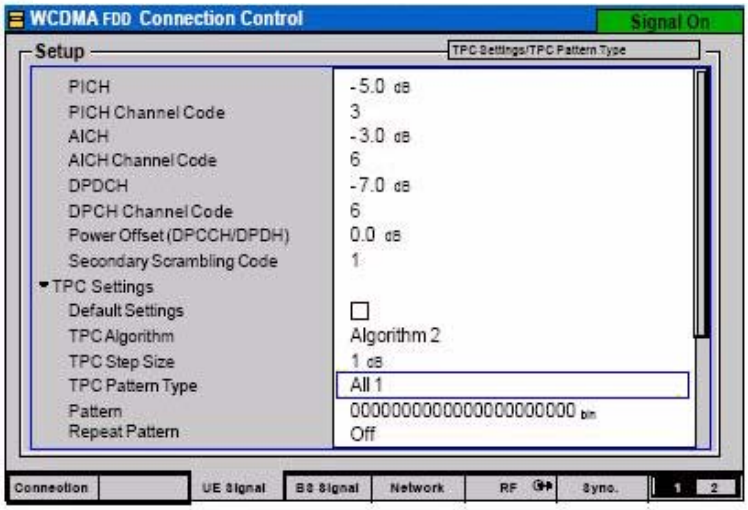


Figure 23. TPC Pattern Type(UE Signal)

6. Wait until the PC Card's Green LED starts flashing
7. Dial a number using the Radio Comm and press send.
8. The PC Card is now connected.

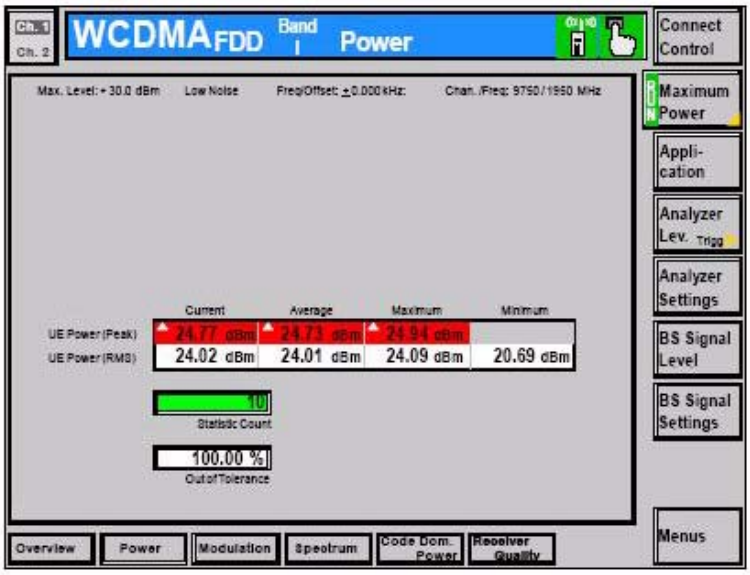


Figure 24. WCDMA Call Connected

6.3.4 WCDMA Call Test parameters

When the PC Card under test is in an active call, the parameters for each band should be verified as described in Table 10.

Table 10. WCDMA Call Parameters

Parameter	Low limit	High limit	Unit
Avg. RMS Power Out[1]	20	22	DBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[3]	0	13.5	%
Avg. RMS ACLR -2	-100	-43	dB
Avg. RMS ACLR -1	-100	-33	dB
Avg. RMS ACLR +1	-100	-33	dB
Avg. RMS ACLR +2	-100	-43	dB

[1]See Figure 26.

[2]See Figure 26.

[3]See Figure 26.

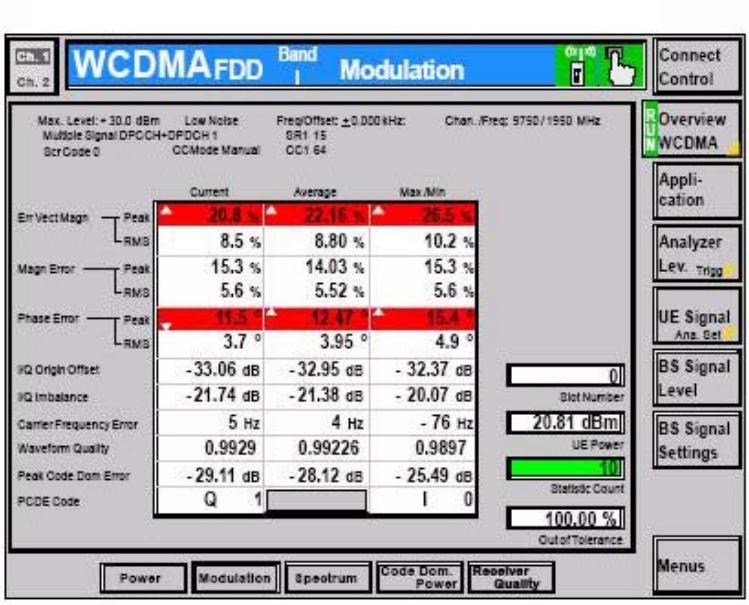


Figure 25. WCDMA Modulation

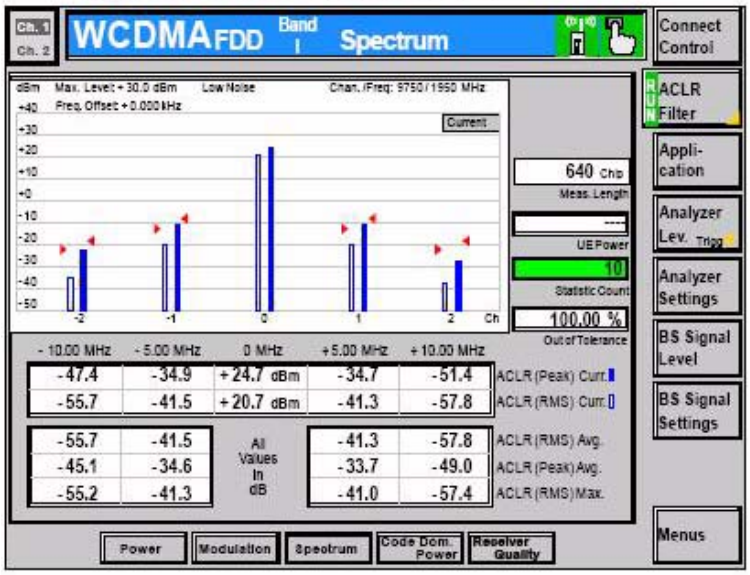


Figure 26. ACLR Screen

6.4 NON-SIGNALING TEST PROCEDURES

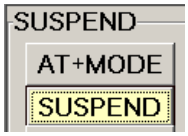
6.4.1 (GSM/DCS/PCS)

To perform non-signaling test procedures, the user should be familiar with sending test commands to the PC Card under test. The test commands can be sent through a computer.

In order to successfully send test commands to the PC Card under test, the PC Card should be in a suspend mode.

Follow the following procedure to place the PC Card in suspend mode.

6.4.1.1 RadioComm Test Commands

1. Click AT+MODE then SUSPEND (Serial Only).
2. Click PST Initialize.
3. Click 

when initialization is complete (USB Only).

6.4.2 Hardware Requirements

Refer to “Hardware Requirements” section 6.2.1 for a list of hardware. Refer to Figure 16 for a configuration description.

6.4.3 Software Requirements

6.4.3.1 Computer Test Command

- RadioComm (latest release)

6.4.4 Verify TX Power Output (GSM/DCS/PCS)

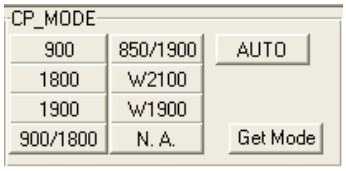
Verify the TX Power output by initiating the commands in this section. Verify that the results are within the limits described in Table 11.

Table 11. TX Power Limits

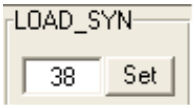
Parameter	LowLimit	HighLimit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28.2	30	dBm
PCS TX Power Out	28.2	30	dBm

6.4.4.1 RadioComm Test Commands

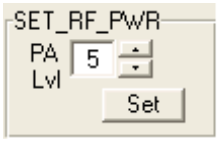
1. Click on 900/1800 (GSM/DCS) or 1900 (PCS).



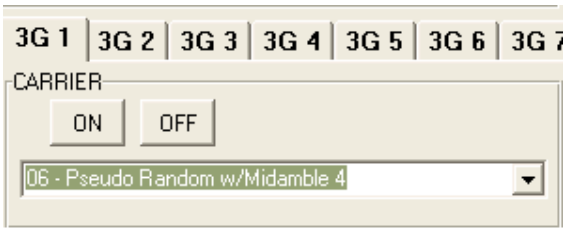
2. Enter 38 (GSM), 700 (DCS), or 661 (PCS) and click Set.



3. Enter 5 (GSM) or 0 (DCS/PCS) and then Set.



4. Select 06 and click ON.



6.5 GSM RSSI

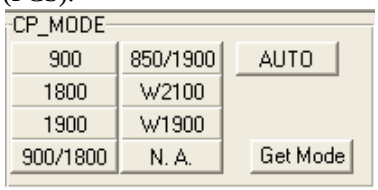
Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user should set the RF generator to the following parameters.

Broadcast Channel (BCH): 20

Broadcast Channel (BCH) Level: -105 dBm

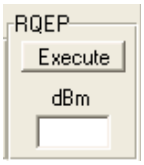
6.5.1 RadioComm Test Commands

1. Click on 900/1800 (GSM/DCS) or 1900 (PCS).



2. Enter Channel 20 Click INIT.

3. Click Execute.



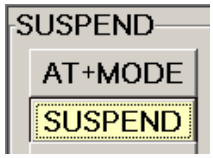
4. Verify return data is approximately -105 dBm.

6.6 NON-SIGNALING TEST PROCEDURES (WCDMA)

To perform non-signaling test procedures, the user should be familiar with sending test commands to the phone under test. The test commands can be sent through a computer. Refer to section 6.2.2.1 “Computer Test Commands,” for details on how to send test commands through the computer.

In order to successfully send test commands to the phone under test, the phone should be in suspend mode. Follow the the next section procedure to place the phone in suspend mode.

6.6.1 RadioComm Test Commands

1. Click AT+MODE then SUSPEND (Serial Only).
2. Click PST Initialize and click 

when initialization is complete (USB Only).

6.6.2 Hardware Requirements

Refer to section 6.2.1 for a list of Hardware. Refer to Figure 16 for a configuration description.

6.6.2.1 Computer Test Command

- Radio Comm (latest release) Verify TX Power Output

6.6.2.2 (WCDMA)

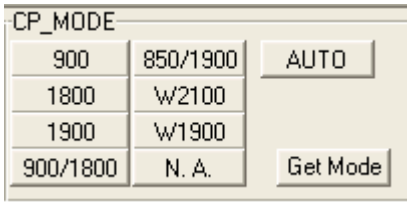
Verify the TX Power output by initiating the commands in this section. Verify that the results are as described in Table 12 .

Table 12. WCDMA TX Power Output

Parameter	LowLimit	HighLimit	Unit
WCDMA Power Out	20	22	dBm

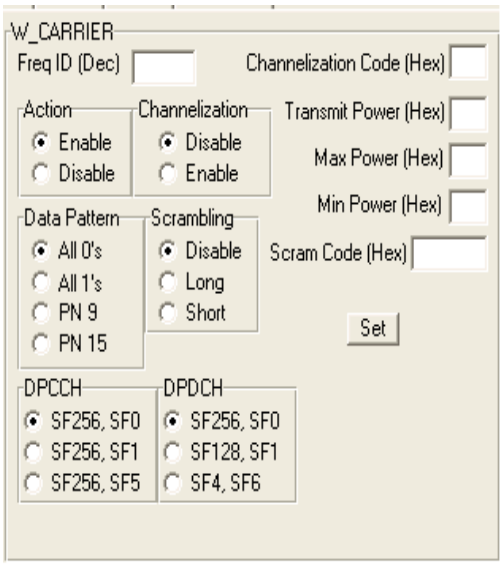
6.6.2.3 RadioComm Test Commands

- Click on W2100



For W_CARRIER assign these actions to each field

Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256,
DPDCH	SF256,
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00



[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)

6.7 HEADSET TEST PROCEDURES

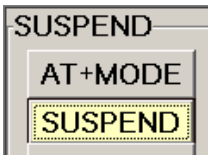
NOTE:

If applicable.

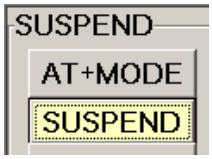
This section describes how to use test commands to verify headset interface.

In order to successfully send test commands to the phone under test, the card shuold be in suspend mode. Perform the listed procedure to place the card in suspend mode.

6.7.1 RadioComm Test Commands

1. Click AT+MODE.
2. Click SUSPEND 

(Serial Only).
3. Click PST Initialize 

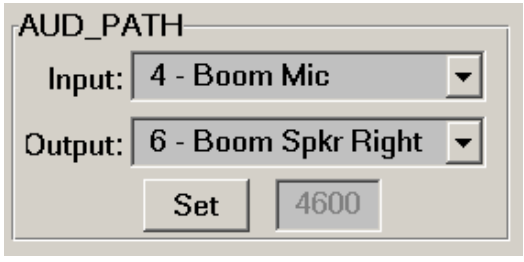
.
4. Click 

when initialization is complete (USB Only).

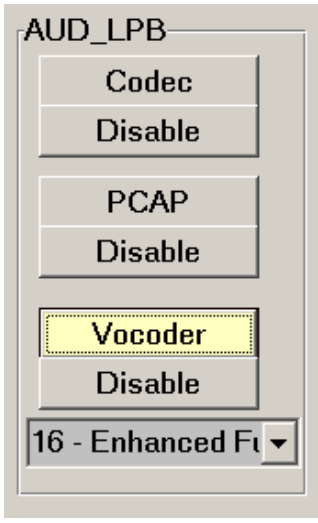
6.7.2 Headset Mic/Speaker test

6.7.2.1 RadioComm Test Commands

1. Enable headset mic and headset speaker.



2. Enable Vocoder loopback at Enhanced Full Rate.



6.7.2.2 Verification:

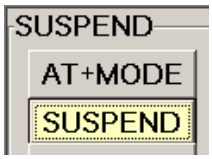
Speak into the headset mic and listen for undistorted speech in the headset speaker.

6.8 SOFTWARE VERSION CHECK

Use the following procedures to retrieve software information. Software information can also be retrieved from the card's customer User Interface (mPT). Refer to the card's user manual for details.

In order to successfully send test commands to the card under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands

6.8.1 RadioComm Test Commands

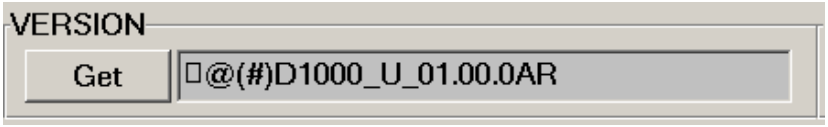
1. Click AT+MODE (Serial Only) 

.

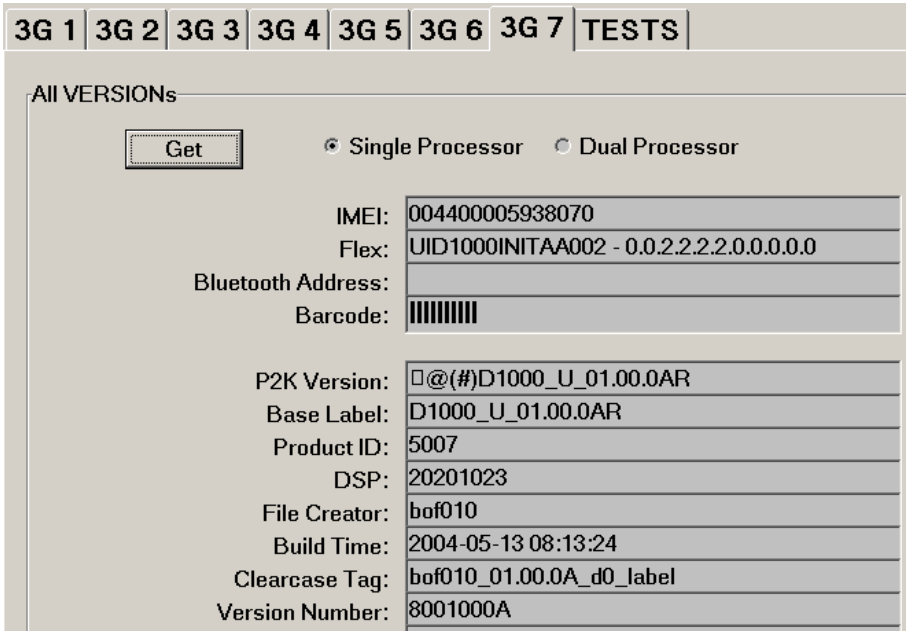
2. Click PST Initialize (USB Only) 

.

3. Click "Get" to retrieve software version.



Select Build Time and click “Get” to retrieve Build Date

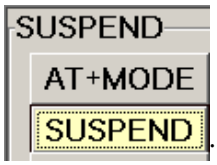


6.8.2 LEDS Test

Use the following procedures to verify status LEDs.

In order to successfully send test commands to the phone under test, the phone doesn’t need to be in suspend mode. Follow the listed procedure to configure the card to accept test commands.

6.8.2.1 RadioComm Test Commands

1. Click AT+MODE (Serial Only) 

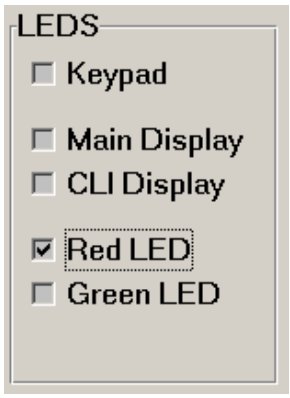
.
2. Click PST Initialize (USB Only) 

.

6.9 STATUS LEDS

6.9.1 RadioComm Test Commands

- Select Red LED or Green LED to enable. Deselect Red LED or Green LED to disable.



6.9.2 Verification

- Verify that the Red and Green status LEDS activate.

DISASSEMBLING AND REASSEMBLING THE D1000 UNIT

Mechanical checks and self-tests should be performed in a basic level of service. To perform testing in a field level, it is sometimes necessary to disassemble the unit. The next section describes the procedures for disassembling and reassembling the D1000 unit.

NOTE:

Read each procedure thoroughly before performing the actual task.

7.1 REMOVING AND REPLACING THE ANTENNA

Recommended tools: mini flat-tip screwdriver.

7.1.1 To remove the Antenna

1. Carefully insert a mini flat-tip screwdriver into the opening on the bottom side of the D1000. Avoid damaging the outer surface of the housing.

2. Push in and up to release the cover (P/N 1587508V30).

3. Carefully insert a mini flat-tip screwdriver into the groove as shown.

4. Push in and up to release the antenna holder (P/N 1587538V67).

5. Remove the antenna (P/N 8586381J09) from the housing.

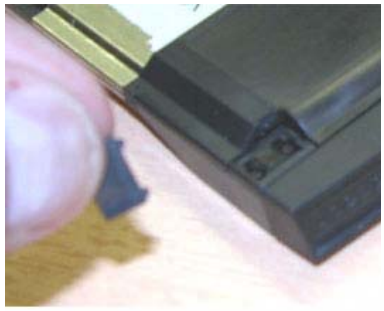
7.1.2 To reassemble the Antenna

1. Insert the antenna (P/N 8586381J09) into the housing.

2. Lubricate Antenna axis using lubricant P/N 1102383L49 according to process described in drawing no. 0102710K32.

3. Insert a new holder (P/N 1587538V67) into the slot. .

4. Insert the tabs of the cover (P/N 1587508V30) into the housing.



5. Press the cover carefully until the snap is on place.

7.2 HOUSING DISASSEMBLY

Recommended tools: Duel p/n ds8814 rework tool.

1. Follow the procedures to remove the:

   •USIM Card

   •Antenna

2. Place the D1000 card on ultra sonic disassembly tool (Duel p/n ds8814):

3. Slide the handle until the D1000 card reaches the end of the tool trajectory.

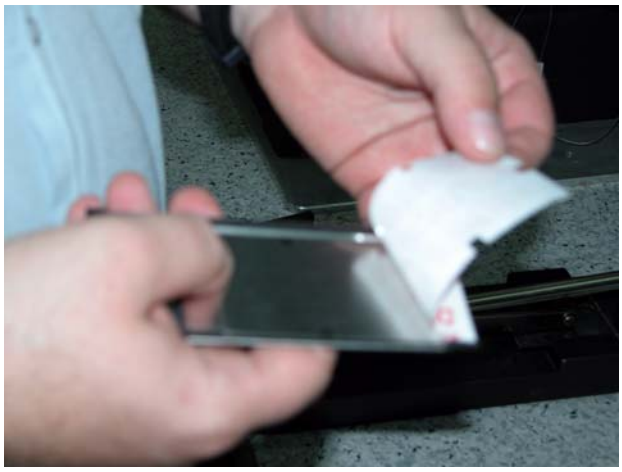
4. Separate the two housing parts from PC Board.

7.3 HOUSING ASSEMBLY

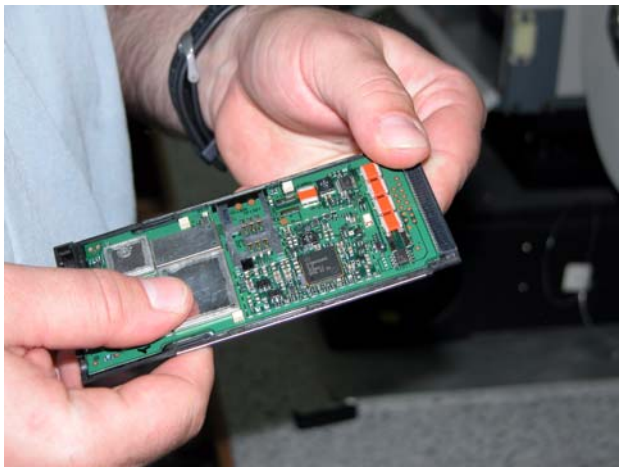
Recommended tools: welding fixture and “Branson 900 plus” machine.

(Or other machine approved by Motorola.)

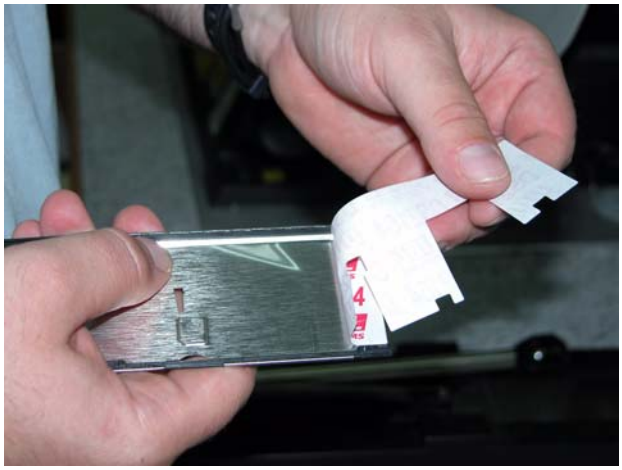
1. Remove the liner from a new top housing (P/N 1588068U06).



2. Put the pc board in place and gently press against the adhesive.



3. Peel off the liner from a new bottom housing (P/N 1588068U05) and put in place over the pc board.



4. Put the assembly inside the ultra sonic welding tool cavity.

5. Operate the machine on the parameters mentioned in drawing 0102710K31, section 1.6.

6. Insert the assembled module into the P/N TGC0193AT 68-pin connector fastening machine. The green led will turn on.
7. Wait until the green led is turn off and take out the module from the machine.

7.4 EXPLODED VIEW DIAGRAM

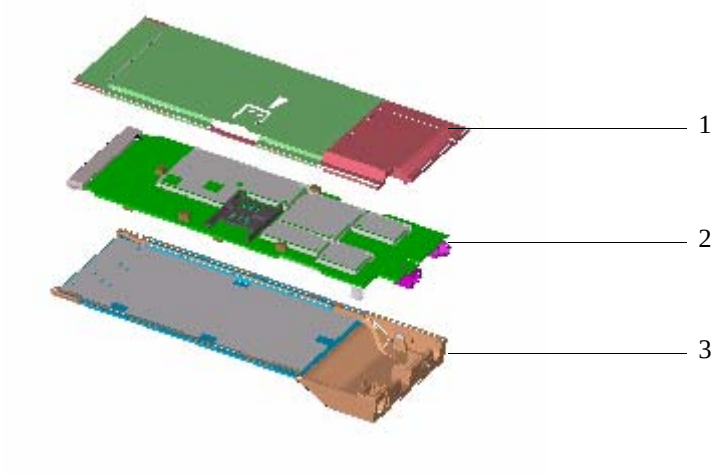


Figure 27. Exploded View Diagram

Table 13. Housing Part Numbers

D1000 Housing Assembly Description - Part Number 0102710K31		
Item	**Description**	**Part Number**
1	Bottom Housing	1588068U05
2	PCB	8488185V01
3	Top Housing	1588068U06

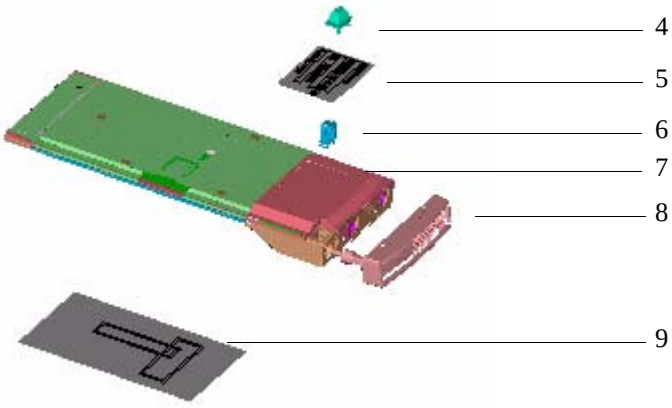


Figure 28. Exploded View Diagram - Main Assembly

Table 14. Main Assembly Part Numbers

D1000 Main Assembly Description - Part Number 0102710K32		
Item	**Description**	**Part Number**
4	Antenna holder cover	1587508V30
5	Regulation Label	5487503V73
6	Antenna holder	1587538V67
7	D1000 Housing Assembly	0102710K31
8	Antenna Assembly	8586381J09
9	Branding Label	5487503V72

UMTS SUBSCRIBER IDENTITY MODULE (USIM) IDENTIFICATION LABEL

8.1 USIM

A USIM is required to access an existing local GSM ,WCDMA network and a remote networks when traveling (when a roaming agreement exists with the provider).

The USIM card contains:

- All the data necessary to access GSM or WCDMA services
- The ability to store user information such as phone numbers

All information required by the network provider to provide access to the network

Each Motorola 3G PC Card is labeled with a variety of identifying numbers. The following section describes the current identifying labels.

8.1.1 Mechanical Serial Number (MSN)

The MSN is an individual unit identity number and remains with the unit throughout its life.

The MSN can be used to log and track a phone on Motorola's Service Center Database.

The MSN is divided into 4 sections as shown in Figure 29.

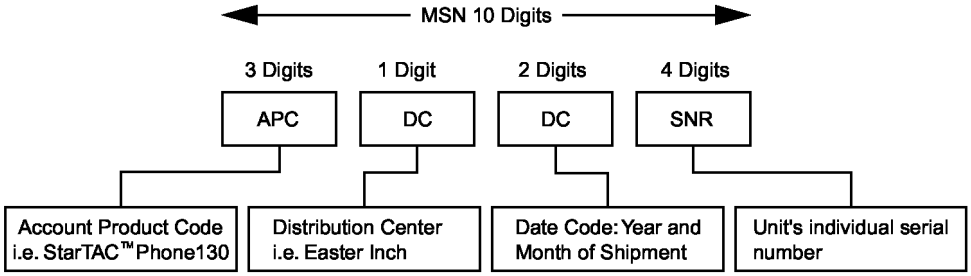


Figure 29. MSN Label Breakdown

8.1.2 International Mobile Station Equipment Identity (IMEI)

The International Mobile station Equipment Identity (IMEI) number is an individual number unique to the PCB and is stored within the unit's memory.

The IMEI uniquely identifies an individual mobile station and thereby provides a means for controlling access to GSM or UMTS networks based on mobile station types or individual units. The full IMEI structure is listed in Table 15

Table 15. IMEI Number Breakdown

Type Allocation Code (TAC)	Serial Number	Check Digit
NNXXXXYY	ZZZZZZ	A

Where:

NN Reporting body identifier

XXXX Type Identifier

YY YY is set to 00 from 01/01/2003 until 31/03/2004

ZZZZZZ Individual unit serial number

A Phase 1 = 0.

Phase 2 and 2+ = check digit defined as a function of all other IMEI digits

3GPP system = check digit and is defined as a function of all other IMEI digits

Other label number configurations present are:

- **MODEL NUMBER:** Identifies the product model.
- **TRANSCEIVER NUMBER:** Identifies the product type. Normally the SWF number. (i.e. D1000).
- **PACKAGE NUMBER:** Identifies the equipment type, mode, and language in which the product is shipped.

SERVICE DIAGRAMS

9.1 INTRODUCTION

This section provides contact information for any possible queries that may arise, such as the following:

The service diagrams were carefully prepared to allow a Motorola certified technician to easily troubleshoot PC Card failures. Our professional staff provided directional labels, color coded traces, measurement values and other guidelines to help a technician troubleshoot a PC Card with speed and accuracy.

We worked hard in trying to provide the best service diagrams, therefore, to avoid cluttered diagrams, we may exclude some components from the service diagrams. Our professional staff carefully selected to excluded components that are unlikely to fail.

9.2 TEST POINT MEASUREMENTS

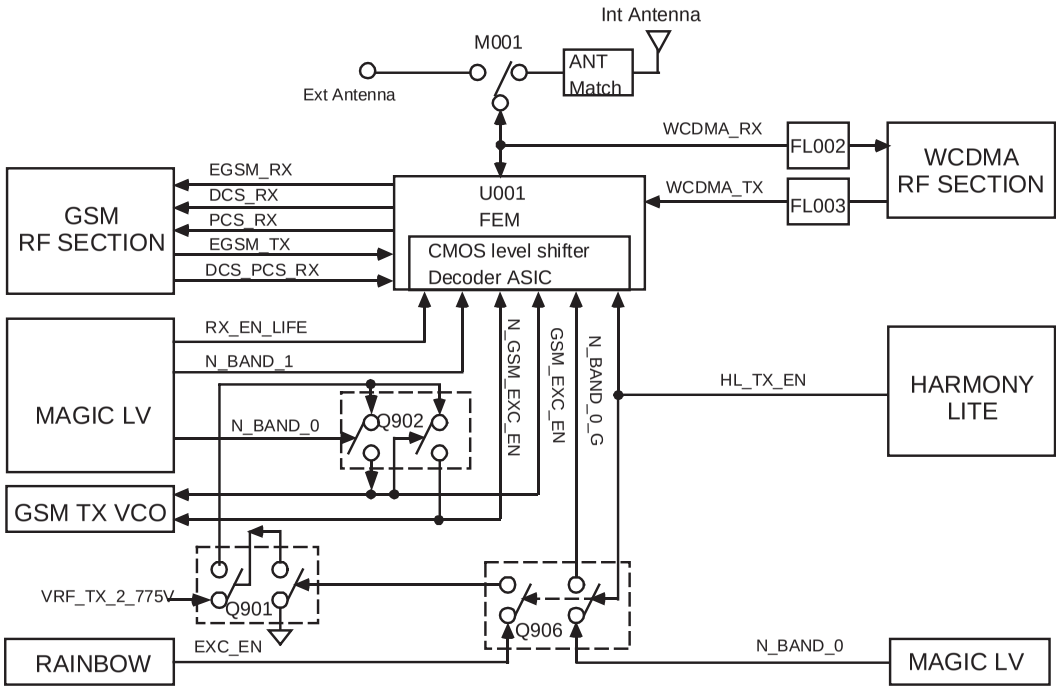
The measurements labeled on the service diagrams are approximate values and may vary slightly. These measurements are dependent on the accuracy of the test equipment.

It is strongly recommended that the test equipment calibration schedule be followed as stated by the manufacturer. RF probes should be calibrated for each frequency in which tests are going to be performed.

The types of probes used will also affect measurement values. Test probes and cables should be tested for RF losses and loose connections.

Due to the sensitivity of RF, measured readings will be greatly affected if they are taken in certain locations. To get the most accurate readings, take measurements nearest to the labeled measurement on the service diagram.

D1000: ANTENNA CIRCUIT



DESCRIPTION

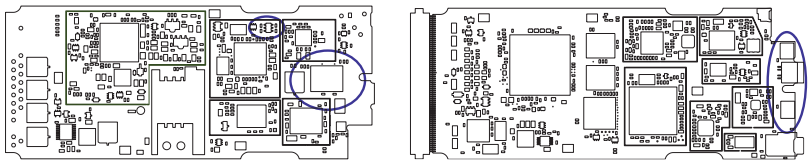
All cellular receive bands are fed into either the internal antenna or external antenna. M001 is a mechanical switch which has the internal antenna path connected when a no insertion condition exists. The RF path will switch to external antenna upon insertion of a male SMA connector to M001. The internal antenna path is fed to the FEM(Front End Module) through antenna matching components. The FEM provides band selection and filtering between the EGSM, DCS, PCS and WCDMA receive and transmit bands to a single antenna port. GSM band selection is done by control lines N_BAND_1 and N_BAND_0_G. Mode selection is done by control lines HL_TX_EN, RX_EN_LIFE, N_GSM_EXC_EN, and GSM_EXC_EN. The diplexing arrangement permits reception of WCDMA signals in any FEM switch position. This allows the phone, while in a GSM call in any band, to detect signals from a WCDMA base station. The decision may then be made to hand over to the WCDMA system. Similarly, EGSM base station signals can be detected while the phone is in a WCDMA call to permit a handover decision from WCDMA to EGSM (This is not possible for base station signals in the DCS and PCS bands.).

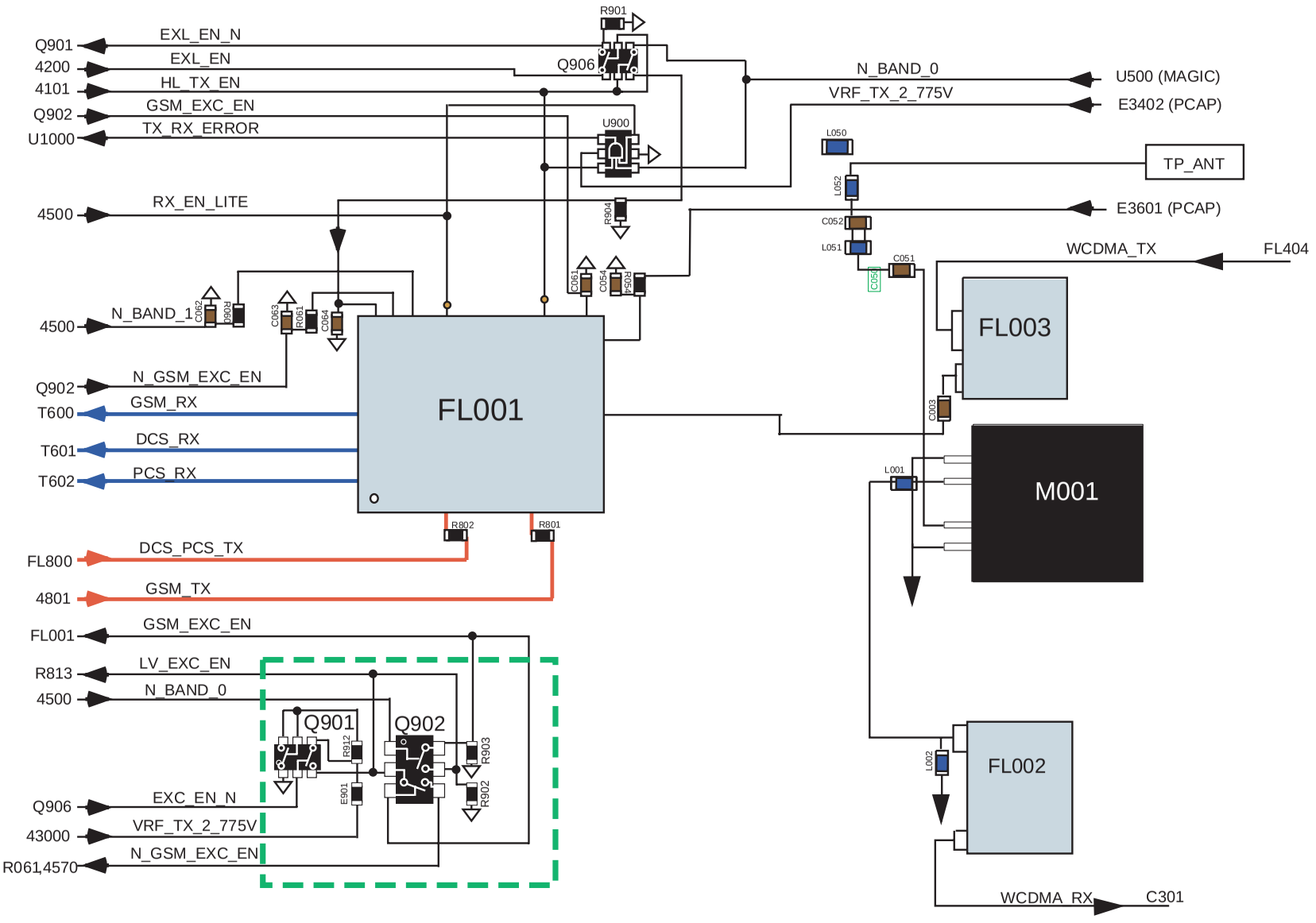
Signals received at the antenna between 2110 - 2170MHz will See the RF switch as an open circuit at any position. Consequently WCDMA Rx signals will go through FL2 to the WCDMA receiver. FL2 should have a maximum insertion loss of ~0.5dB. Outside of the WCDMA Rx band, FL2 behaves as an open circuit, preventing outof-band signals from reaching the WCDMA receiver.

GSM, DCS, and PCS receive signals from the antenna port through the FEM should have a maximum insertion loss of -4.4dB. The FEM EGSM transmit path should have a maximum insertion loss of -2.5dB. The FEM DCS transmit path should have a maximum insertion loss of -3.1dB. The FEM PCS transmit path should have a maximum insertion loss of -3.7dB

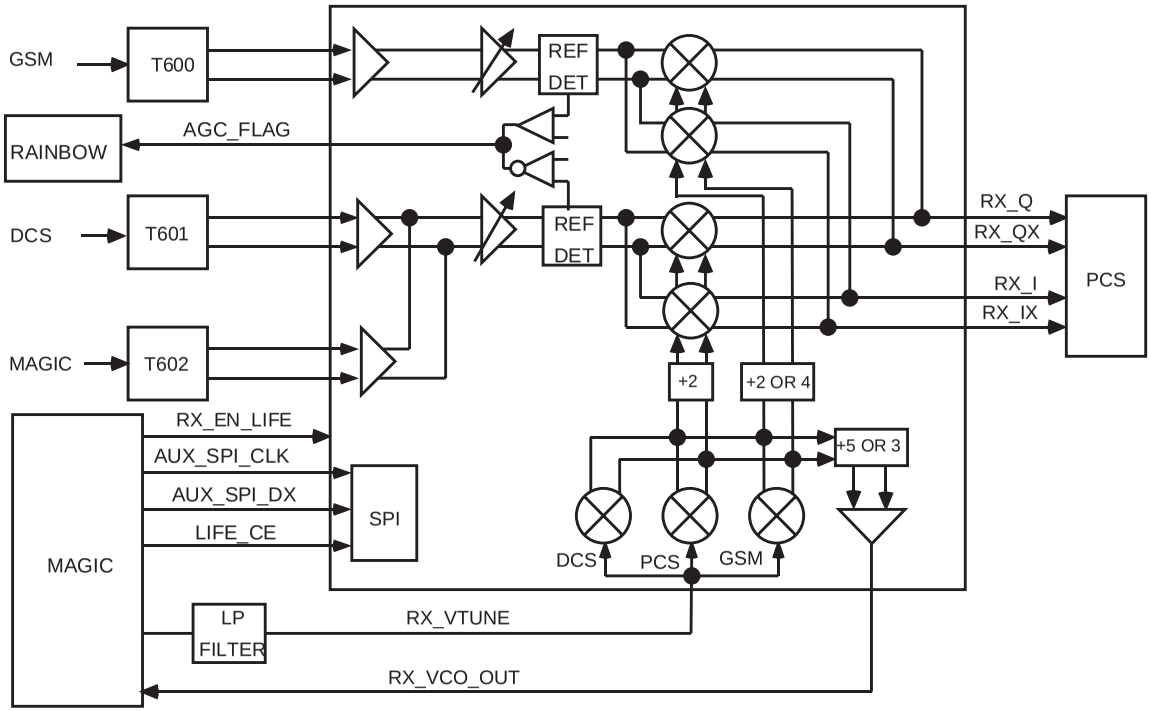
Q902 is a dual FET package that's being used to multiplex function of the N_BAND_0 control signal coming from the Magic LV. With the use of Q902, N_GSM_EXC_EN will follow N_BAND_0. GSM_EXC_EN will be the inverted level of N_BAND_0. Q906 is another dual FET package that's used to prevent simultaneous GSM and WCDMA transmission conditions. During WCDMA transmission conditions, HL_TX_EN will be in a high state. This will open both FETs in Q906, thus, disabling any signal functions from control lines EXC_EN and N_BAND_0. Q901 is used to invert the control signal coming from Q906.

D1000: ANTENNA CIRCUIT





D1000: GSM RX Front End



DESCRIPTION

The EGSM, PCS and DCS signals must first pass through baluns before reaching the LIFE IC. Since the LIFE expects differential inputs, the baluns will provide this. Baluns provide the change from an unbalanced to a balanced line condition. By directly connecting to lines together, a possibility might arise where one line might ground a signal and impair the operation of a circuit. This situation is solved through the use of an un-balanced to balanced transformer, a balun. Expected nominal losses is ~.5 - 1.0dB.

The first IC in the EGSM, DCS, and PCS RX line up is U625 (LIFE), which is an LNA, VCO, and down converter mixer. The RX frequency is mixed down to a Very Low Intermediate Frequency (VLIF) of ~ 100KHz. This design is utilized to improve LO leakage causing RF self-mixing, DC offsets, and noise performance. The LIFE IC operates from the MAGIC_LV (tracking regulator), MAGIC_RF_V2_475. and MAGIC_SF (isolated supply for the VCO). LIFE is comprised of four low noise amplifiers (three of which are used) with two quadrature mixer paths for use in receive GSM 900 (925- 960MHz), DCS (18051880MHz), and PCS (1930-1990MHz) frequency bands, all SPI programmable. The RX_VCO_OUT signal is fed back to the MAGIC_LV prescaler input. Although the frequency will be dependent of the channel selected, the amplitude signal is ~30dBm.

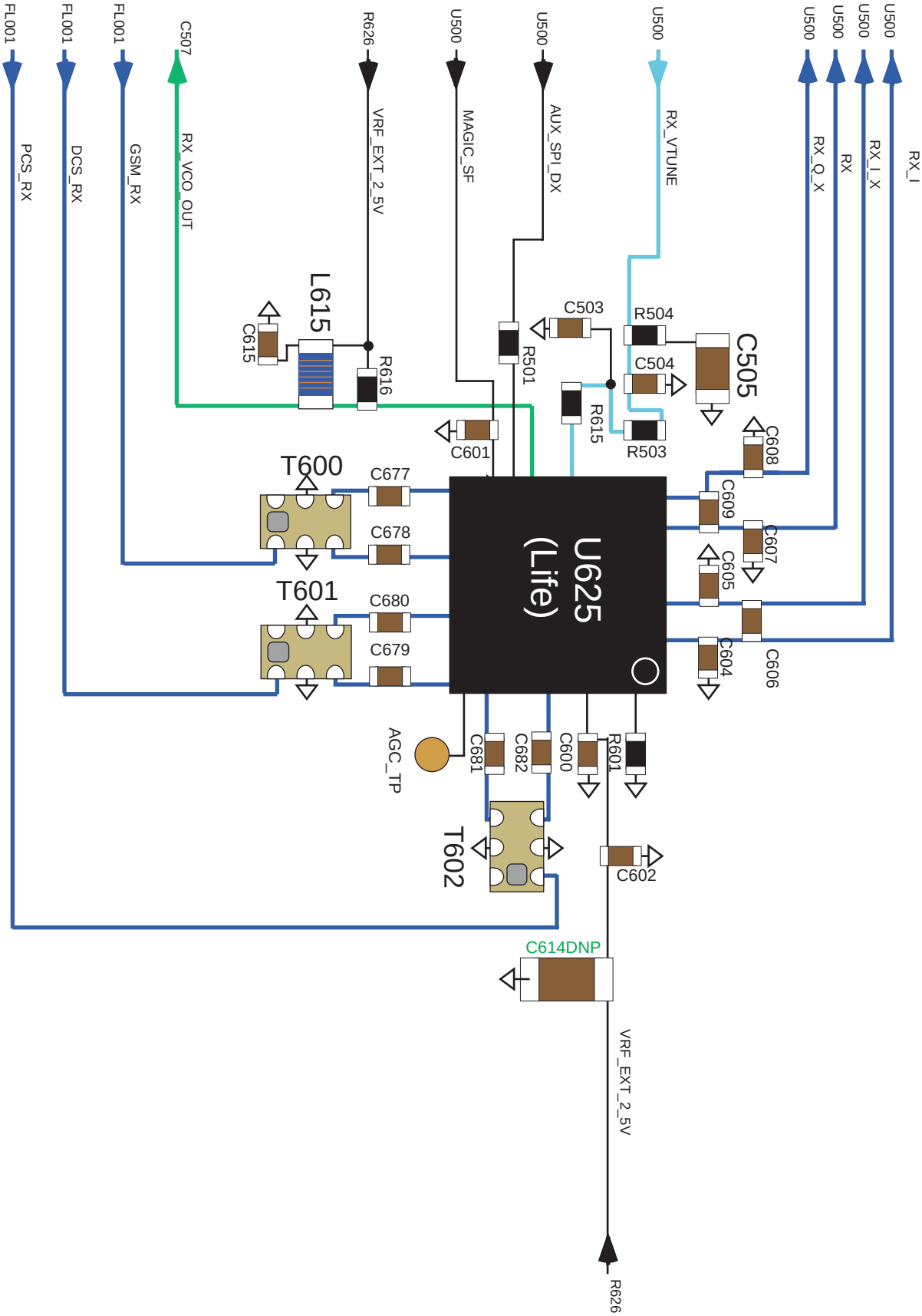
LIFE contains three fully contained VCOs which operate at ~4GHz. These VCOs are internally divided to provide precise quadrature down conversion for the three frequency bands. The input signal RX_VTUNE from the RX backend processor (MAGIC_LV) selects the VCO frequency to operate at. The tune range is .5 - 4.5V. The VCO frequencies for the three technologies are: DCS 3610 - 31759MHz, EGSM 3700 - 3838MHz, and PCS 3859 - 3980MHz.

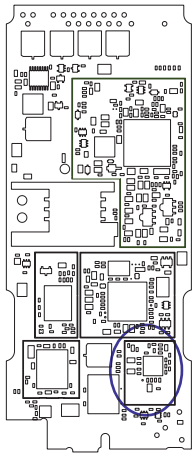
The AGC is provided by a common amplifier section, which is shared by all four LNAs. The AGC amplifier gain control is controlled by the voltage on the AGC pin, utilizing the internal 6-bit D/A to set the AGC via the SPI lines (SPIDATA, SPI_CLK, and SPI_CE). LIFE has an internal RF detector at the input of the AGC amplifier. The detected

DC output level will be compared against a reference, which corresponds to the maximum safe input level to the mixer. This reference is SPI selectable so that the threshold can be set to 0dB, 3dB, 6dB, or 9dB below the level, which results in the mixer malfunction. If the detected level is above the reference then AGC_FLAG will go high. The MAGIC_LV will receive this signal as an interrupt and will reprogram the AGC until the level drops below the safe mixer input level as signified by AGC_FLAG returning low.

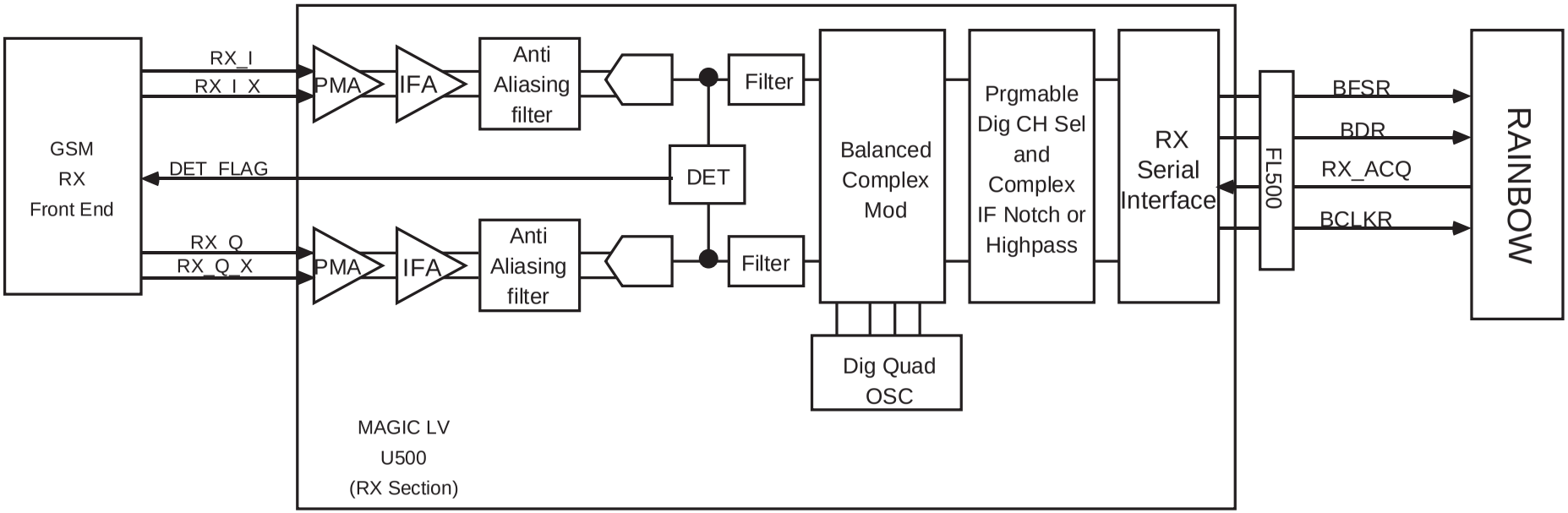
The output signals I / IX and Q / QX are @ ~100KHz IF value for the Very Low IF. The input pin, RX_EN_LIFE controls the on / off state of the receiver and the PLL circuits. For input amplitude at the antenna of -50 to -40dBm the expected nominal output should be an AC rms peak-to-peak voltage of ~4.5 - 14mV

D1000: GSM Front End





D1000: Magic LV (RX Section)



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DESCRIPTION

The MAGIC_LV (U500) handles the backend processing for the EGSM,DCS and PCS (VLIF:RX_I,RX_I_X,RX_Q,and RX_Q_X) signal lines from LIFE. Simply, the MAGIC_LV performs an analog to digital conversion of I/Q and sends it to the data to the board processor (RAINBOW) via the SSI (serial synchronous interface). The MAGIC_LV also has a programmable and phase - able digital IF to improve image rejection.

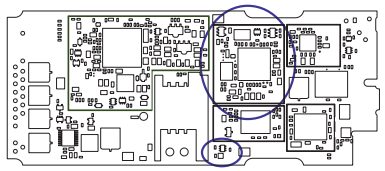
In MAGIC_LV, each channel is comprised of a Post Mixer Amplifier (PMA), an integrated passive two pole filter, a gain stage (AMP1) followed by an active programmable 2 pole anti-aliasing filter (mainly required to meet the blocking specs). This is following by a lowpass sigma-delta ADC with a programmable oversampling clock OVSCLK (derived from the reference oscillator) equal to 13MHz for 200KHz channel spacing (13bits).

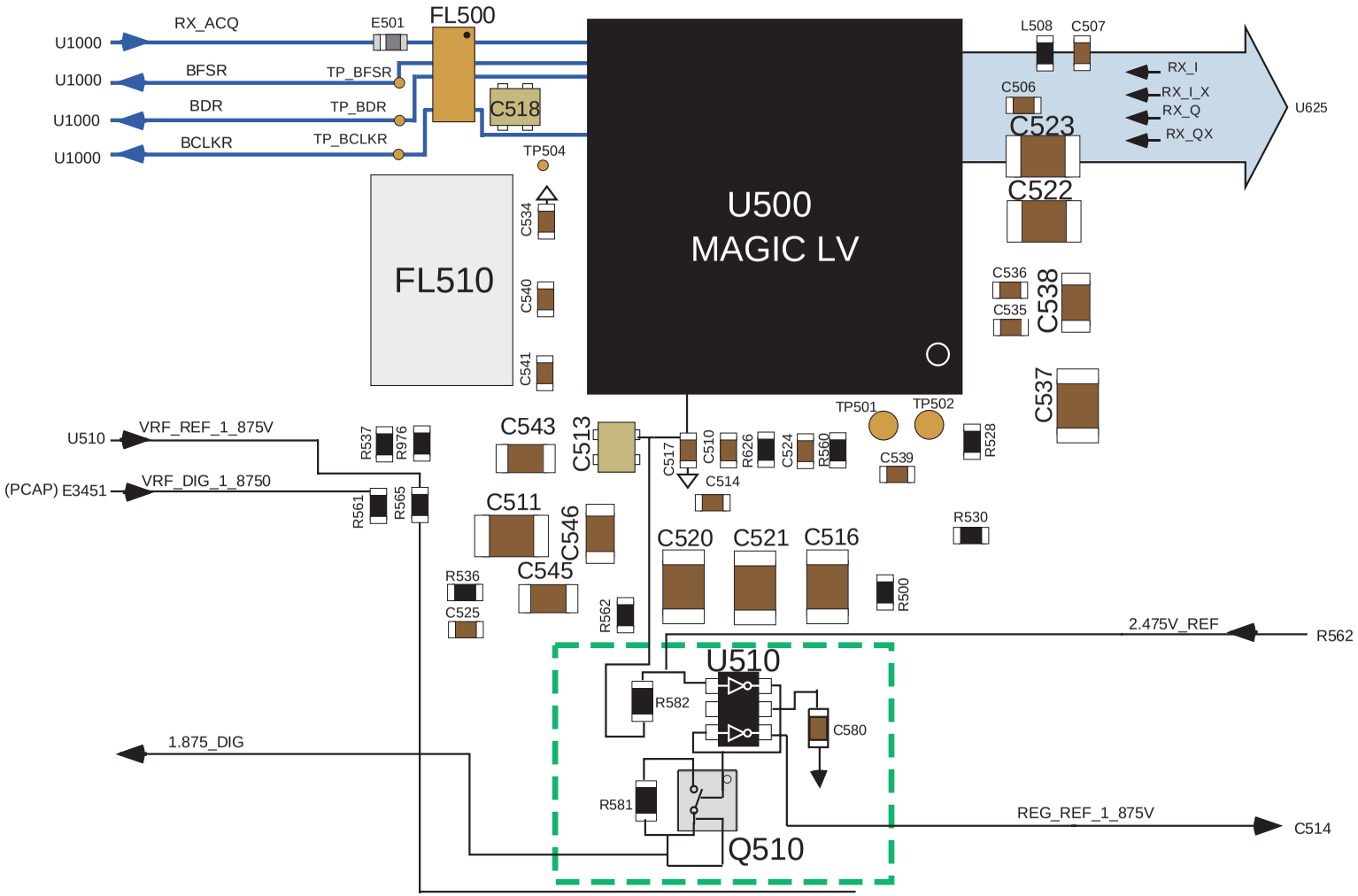
Digital detector circuits are placed on each channel at the output of the sigma delta converters. The outputs of these detectors are compared against a level defined by DET_LVL. If either of the detected levels exceeds the programmed threshold then the pin DET_FLAG is set high. This indicates that the signal level is excessively high for the sigma delta modulator. DET_FLAG is read by the processor, which will respond by re-programming one of the AGC settings to a lower gain until DET_FLAG returns low.

The outputs of the sigma-delta modulators are digitally processed through a noise cancellation circuit, comb and decimation filters. A second programmable digital LO based on a look up ROM generates digital quadrature oscillators with programmable gain/phase correction (called balanced complex multiplier) to digitally downconvert the I/Q signals to baseband (digital zero IF) through four quadrature mixers that provide image rejection of adjacent/alternate channels. Gain/ Phase correction at a single baseband frequency is performed on the Digital Quadrature Oscillator to compensate the analog gain/phase mismatch of the quadrature I and Q paths. After baseband downconversion and image reduction, the quadrature I and Q signals are further processed by digital filters that perform channel selectivity and out of band noise rejection.

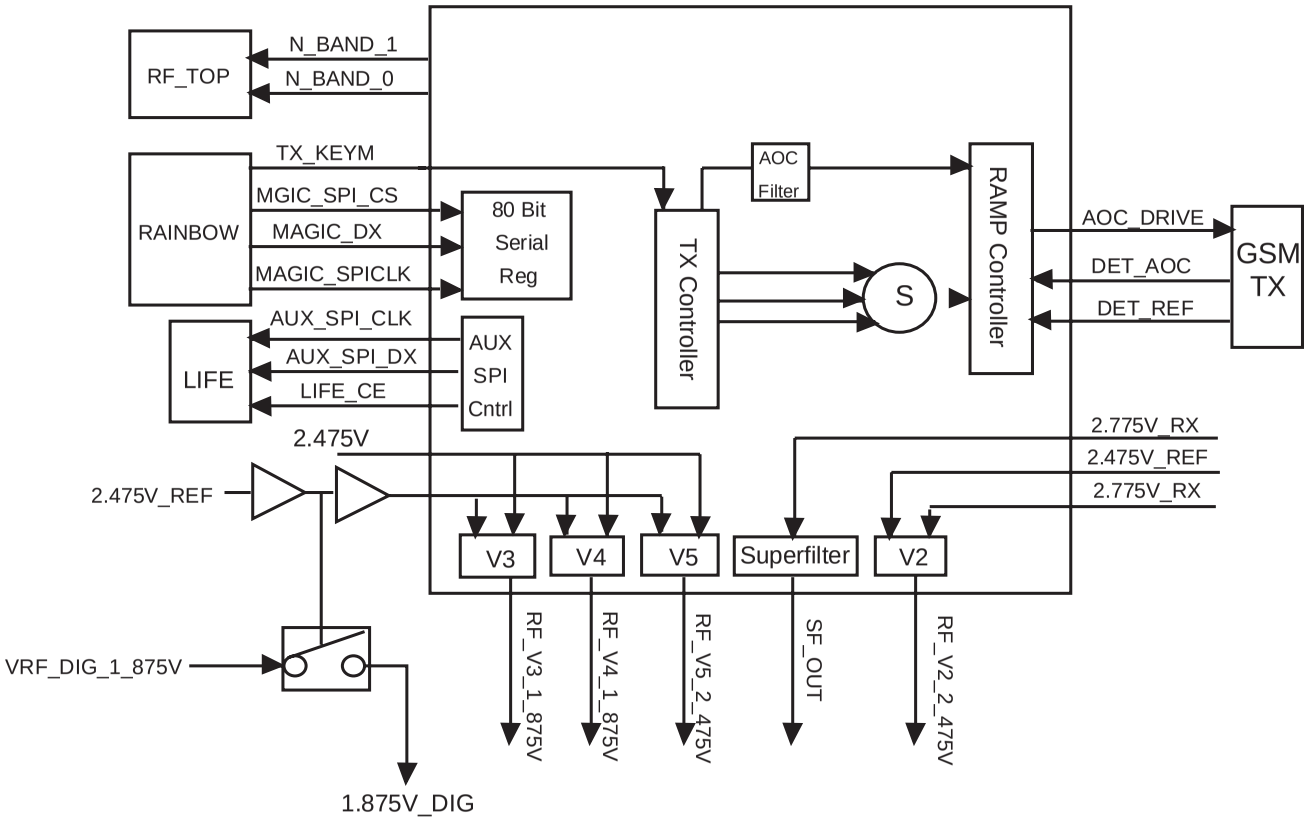
A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data in 2's complement format. BDR and BFSR are outputs from MAGIC LV. BFSR is a framing signal which marks the beginning of an I,Q transfer. BDR is the serial data. The clock used for the serial transfer is BCLKR. When RX_ACQ goes high MAGIC LV will activate the SSI interface in the digital receiver section. The data transmission over the serial bus will begin at the next normal occurrence of valid I and Q data, as defined internally to

D1000: Magic LV (RX Section)





D1000: Magic LV Control Functions



DESCRIPTION

The MAGIC LV contains 4 tracking regulators and one superfilter, which will generate the supplies for most of the IC as well as the front end and the main VCO. The tracking regulators derive their internal power from the REG_REF pins. The reference voltages are filtered and buffered for use on the IC. The buffered voltages should track the references within +/-1.5%. A raw supply voltage is provided to the tracking regulators which is higher than REG_REF as specified below for each regulator. A superfilter is needed for the external VCO power supply. This superfilter, cascaded with an external regulator and any filtering in front of the IC, will need to provide 80dB of rejection to a 0.1V step occurring at a 217Hz rate with a risetime of 20us on the raw supply (battery) and a duty cycle of 0.125. The superfilter will use an internal pass transistor that is capable of driving a 30 mA load with a voltage drop of less than 0.4V relative to SF_SPLY from the SF_OUT pin. An external 1uf cap is required on SF_OUT. As the superfilter will track SF_SPLY it will need to sense the power on reset and turn off even though its supply may remain active. All supplies within the IC must be within 5% of their final values after 5msec from the start of POR_LB. The power on reset circuit contained within the crystal reference oscillator is used to aid this functionality.

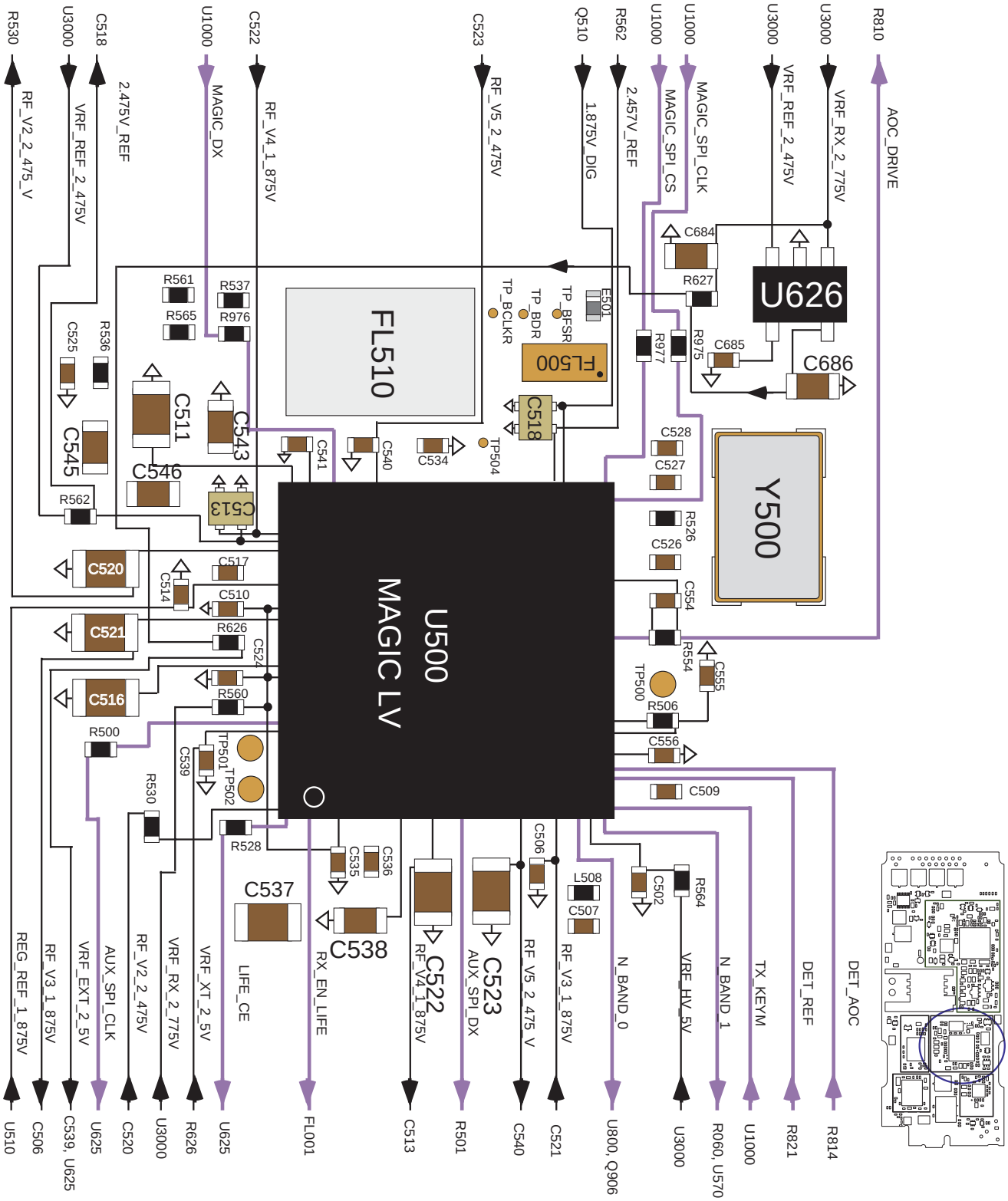
The MAGIC_LV has two sets of SPI interfaces; one set is for handling the control interface for the LIFE IC (AUXSPI lines) and ones for interfacing with RAINBOW (SPI lines). AUX_SPI_DX is the serial data input line. AUX_SPI_CLK is the clock input line, where data shifting occurs at the rising edge of this signal. LIFE_CE is the clock enable line, active high, for the LIFE IC.

MAGIC_LV will integrate a system of D/As and control logic to generate the power amplifier control ramps. In addition, MAGIC_LV will integrate the op-amps and comparators which receive the detected output of the power amplifier and create the necessary control voltage to drive the power amplifier control port based on the control ramps. When TX_KEYM goes high, the ramp controller receives an positive input.

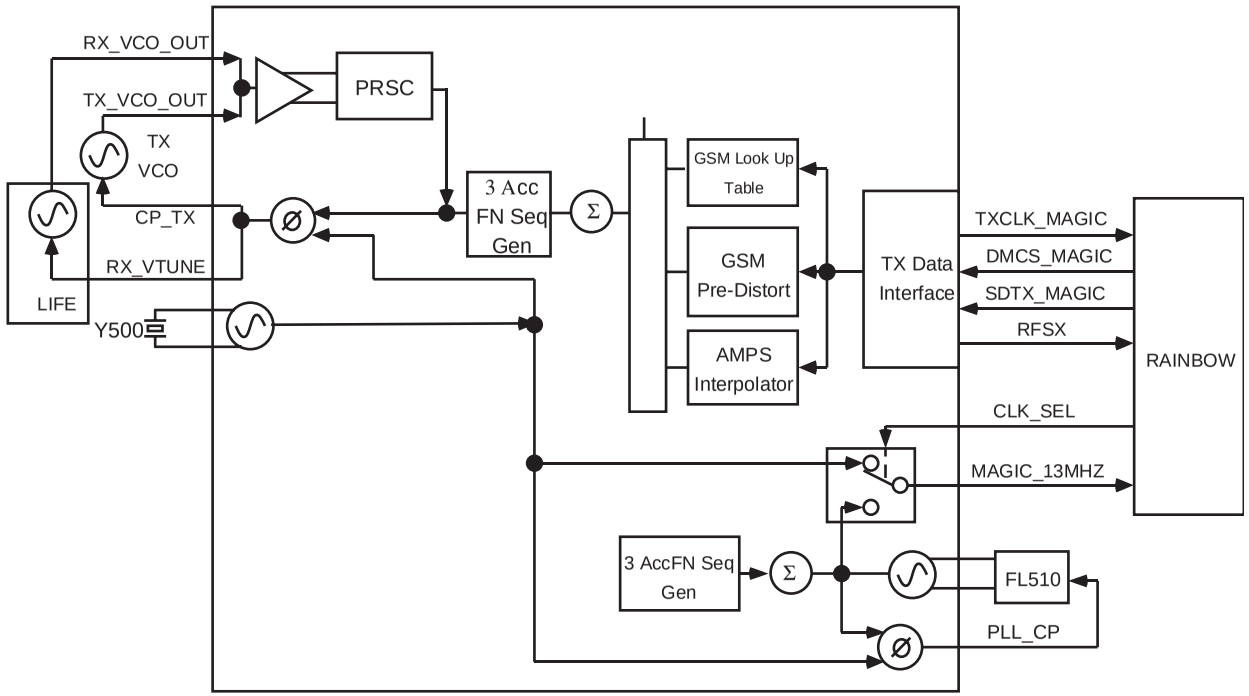
This will cause the AOC_DRIVE pin to linearly rise which in turn will cause the PA output power to rise. The rising PA output power will cause DET_AOC to begin to rise until the DC level on DET_AOC exceeds the DC level on DET_REF by the intentional offset of the RF detector versus it's reference. At this point the "Active Detect" comparator will go low and break the input voltage to the integrator with the ramp controller. This will cause the PA power to stop rising and hold the present power level as determined by the 8 bit offset value fed to the ramp controller. The PA control loop is now at a minimal power needed to keep the control system in a closed loop for a controlled ramp up of the power.

The MAGIC uses two SPI driven GPO lines which are used to control the operating bands of the GSM RF circuits. They are N_BAND_0 and N_BAND_1.When the MAGIC LV is set to battery save mode it will shutdown the receiver analog sectioins (via RX_EN_LIFE), the AOC, the main synthesizer and the superfilter.

D1000: Magic LV Control Functions



D1000: MAGIC LV (Synthesizers/Transmitter)



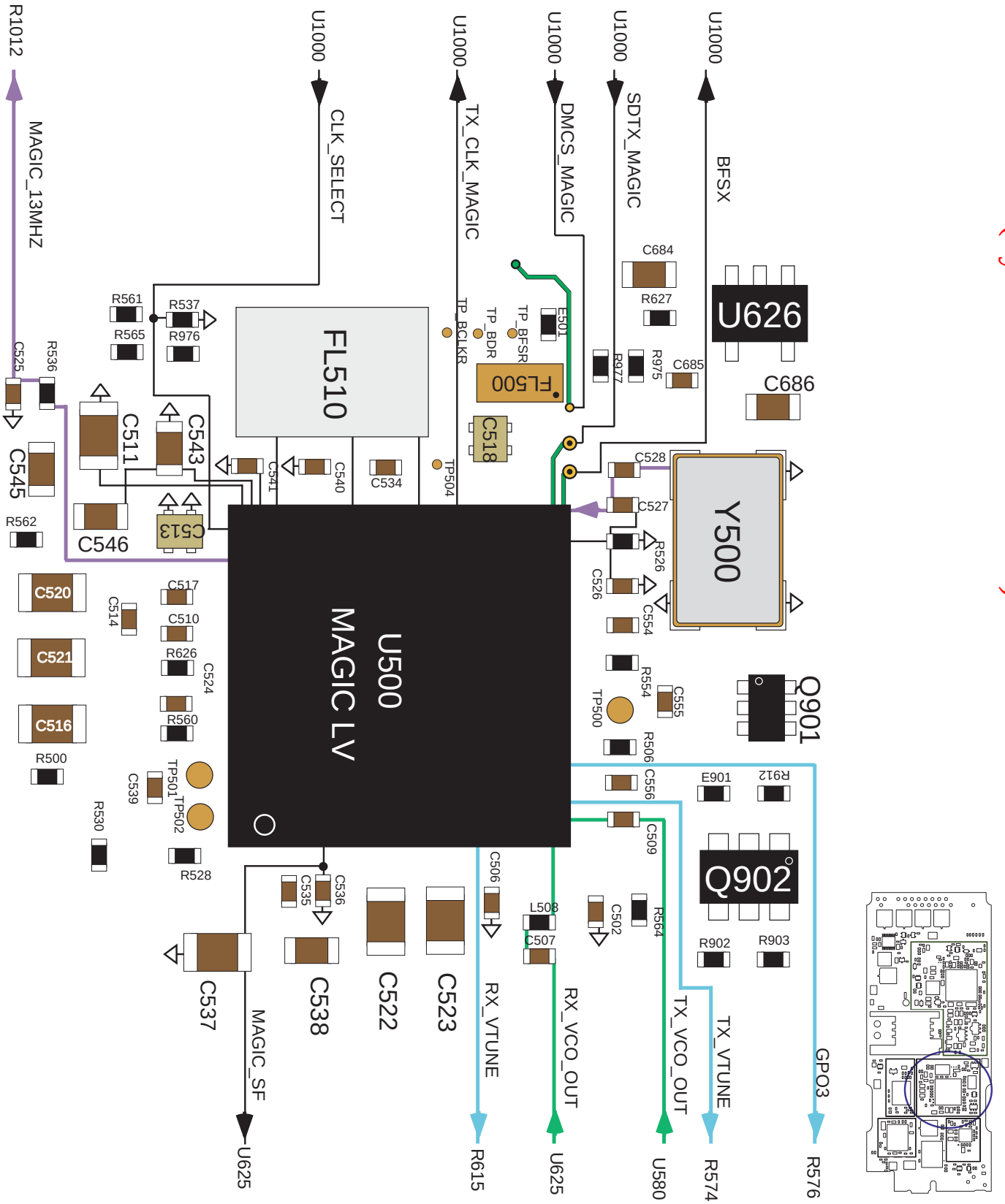
DESCRIPTION

The MAGIC_LV receives SSI Tx data at DMCS (digital input to start Tx modulation), TXCLK (clock for serial transfer) and SDTX (serial Tx data) from RAINBOW. The present serial data bit and the three previous data bits are used to set up one of 16 possible waveforms based on the sum of Gaussian pulses stored in a look up ROM. The resulting signal will then be clocked out at a 16x over-sampling rate. This data pattern input to three-accumumalator fractional N synthesizer with a 24-bit resolution. The VCO control lines must have compliance over an output voltage range of 0.3VDC to Vcc-0.3V. The charge pumps will have their own supply pin. The voltage on this pin is expected to be 2.775V typically to obtain sufficient compliance. This will drive external loop filters, which will in turn drive external VCOs. A dual port modulation mode is obtained with a 9 bit D/A which follows the modulation look up table output waveform is output on the GPO3 pin.This signal is then coupled into the loop filter to add in the higher frequency components of the modulation which may have been attenuated in the main PLL path. This will allow the use of a lower bandwidth main PLL to improve the spectral purity of the transmit signal.For EGSM the synthesizer output is 880 - 915MHz, DCS is 1710 - 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

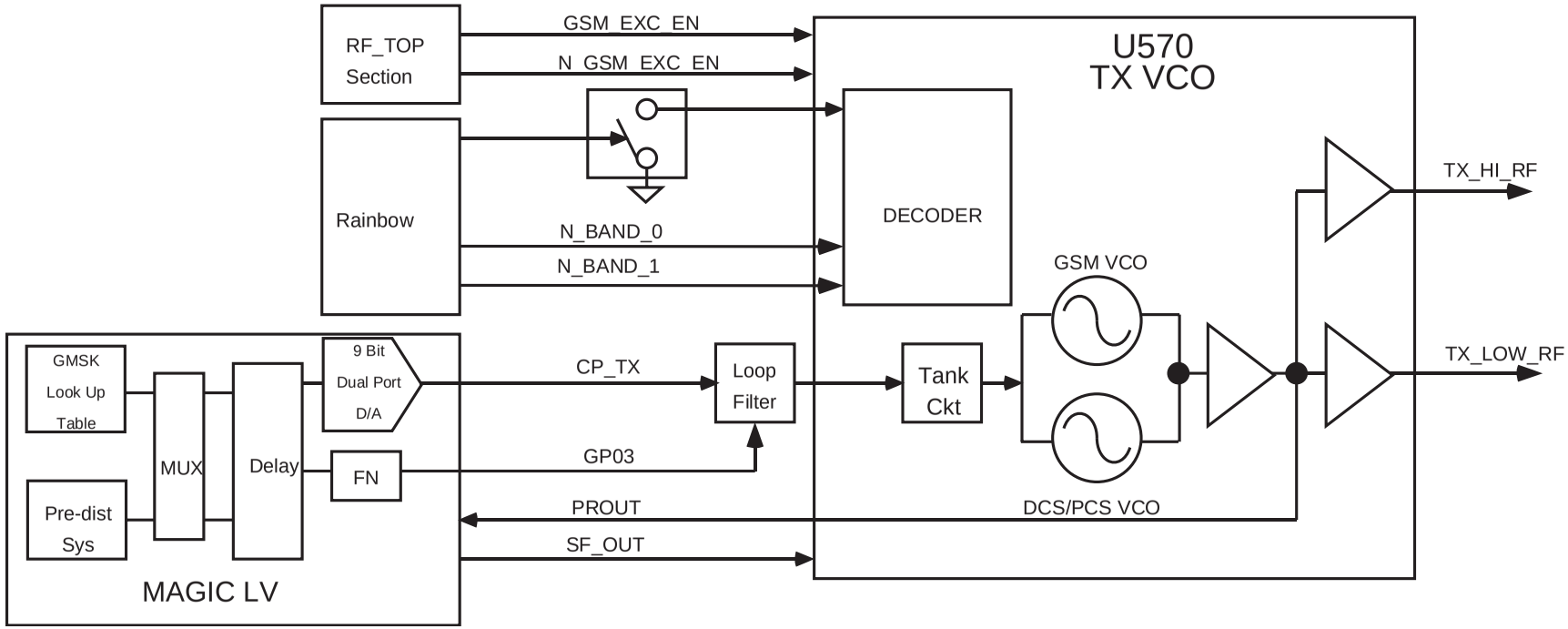
The prescaler for the main LO is able to accept input frequencies as high as 2.0GHz. The level of this signal shall be between -20dbm and -10dbm. There are two prescaler inputs to this point each has a 100? resistor in series between the pin and the actual prescaler input.

The reference oscillator is a free running 26MHz crystal. AFC is provided through the SPI bus as a programming offset to the fractional N division system. Since the 26MHz crystal is not locked to the AFC, a second fractional divider system is necessary to derive an accurate 200KHz system reference. This reference is then multiplied in a PLL to 13MHz for use as an accurate clock to the logic sections of the transceiver.

D1000: MAGIC LV (Synthesizers/Transmitter)



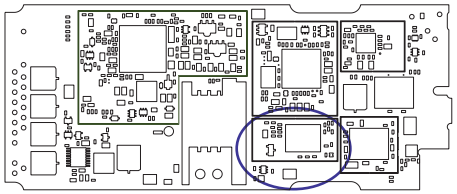
D1000: GSM TX VCO



DESCRIPTION

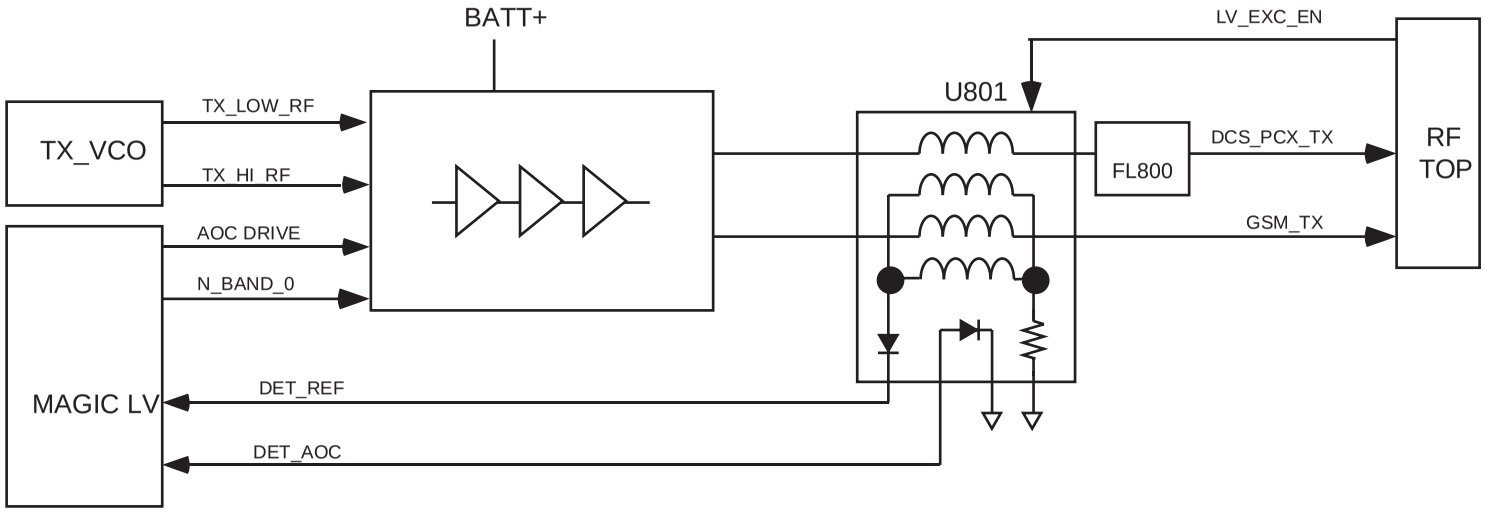
The VCO frequencies are 897-1880MHz, handling the three technology bands. The technology bands are controlled by MAGIC_LV via the data lines: N_BAND_0and N_BAND_1. CP_TX and GPO3 provides a dual port modulation mode for the TXVCO.N_BAND_0 and N_BAND_1 will select which VCO band will be activated. GSM_EXC_EN and N_GSM_EXC_EN will enable the buffer stage of U570. TX_EN is activated prior to enabling the buffer and PA. PROUT is fed back to the MAGIC_LV for proper PLL operation. The output frequency for GSM is TX_LOW_RF and PCS/DCS is TX_LOW_RF. The charge pump output (CPTX) from MAGIC_LV is the input (VT) for the VCO.

D1000: GSM TX VCO



U500
U500
U1000
R575
C572
R576
L574
R577
C576
R574
C571
C573
Q500
U570
GSM Tx VCO
C570
L571
N_BAND_0
U500
N_GSM_EXC_EN
Q902
N_BAND_1
U500
C581
C578
TX_HI_RF
U800
C579
L579
R583
R570
C575
TX_LO_RF
U800
TX_VCO_OUT
C509
U580
MAGIC_SF
C537

D1000: GSM PA



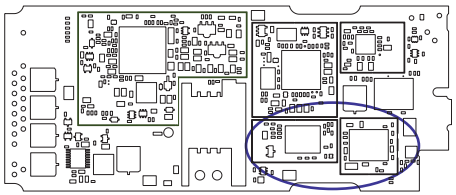
DESCRIPTION

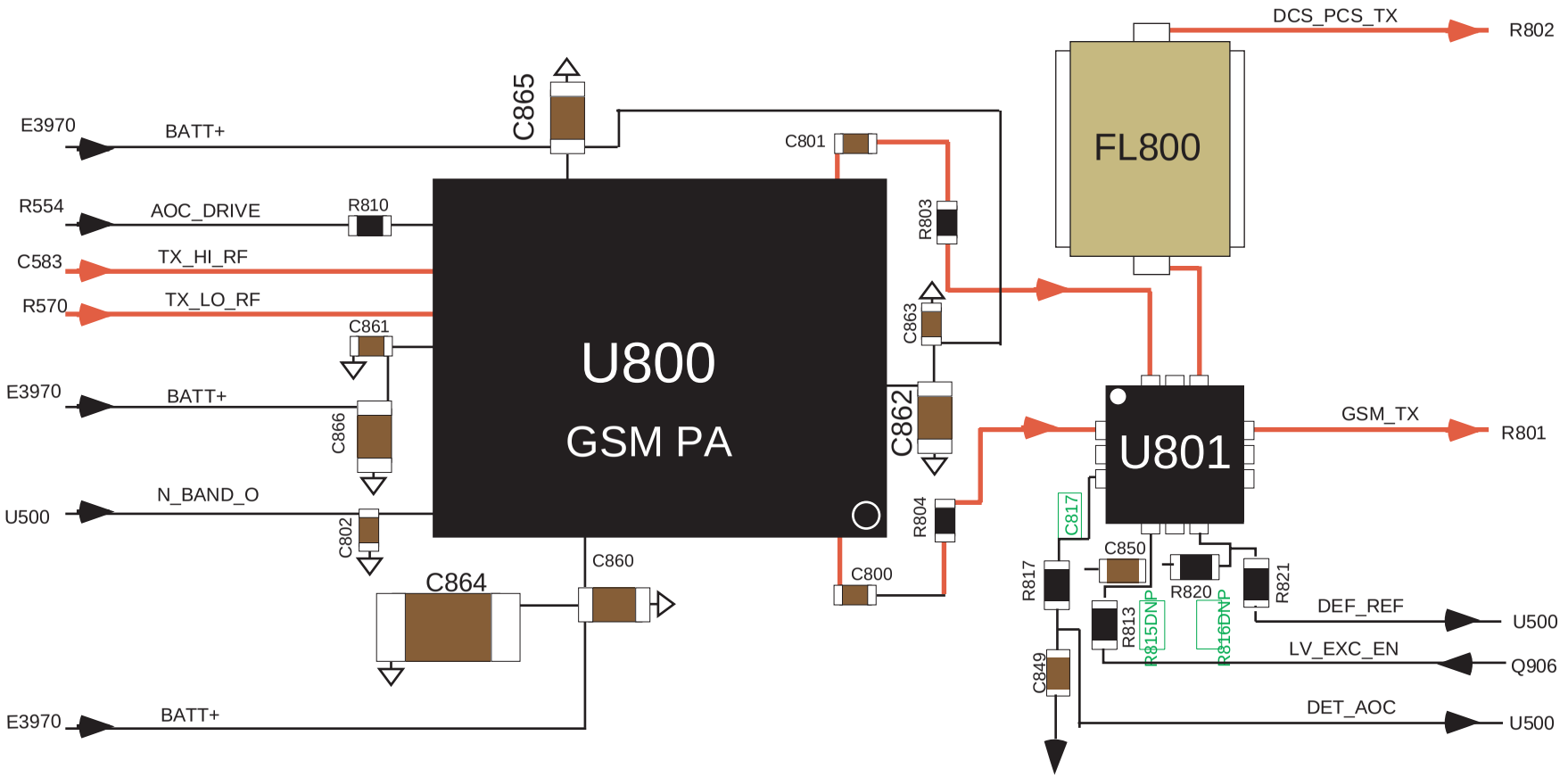
U800 is a tri-band PA module that operates in EGSM, DCS and PCS bands. The nominal expected maximum gain is ~30dB. .

The AOC_DRIVE input from MAGIC_LV controls the PA output. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases. N_BAND_0 is used to select the operating band. LV_EXC_EN will enable PA operation.

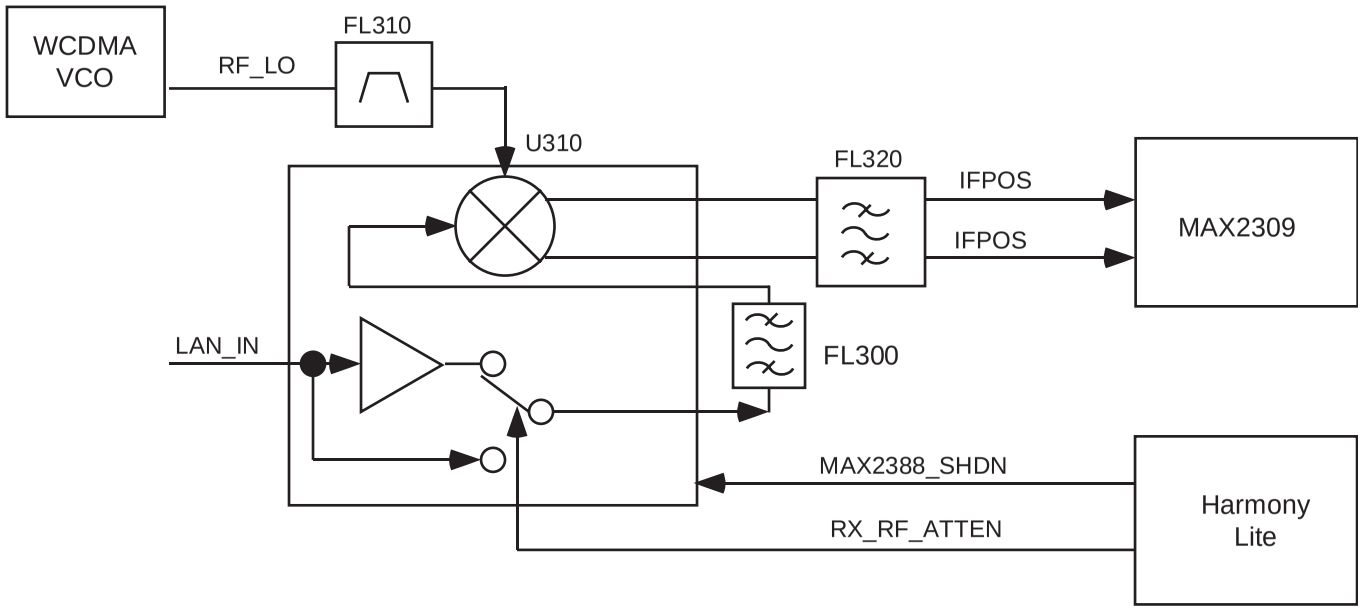
The power detector receives the amplified GSM signal at #1 (EGSM_IN), PCS and DCS at pin #12 (DCS_PCS_IN) from the U800. U801 is a dual combination directional coupler and temperature compensated power detector output. The power detector couples the Tx power input and feedbacks an output DET_AOC to MAGIC_LV. A comparator within the MAGIC LV will sample DET_AOC and based on the power amplifier ramps will provide any necessary control voltage adjustments to AOC_DRIVE The DET_RE F is a reference voltage to MAGIC_LV. Expected nominal loss is <. 3dB.

D1000: GSM PA




E3970
BATT+
C865
C801
DCS_PCS_TX
R802
FL800
R554
AOC_DRIVE
R810
R803
C583
TX_HI_RF
R570
TX_LO_RF
C861
C863
U800
GSM PA
E3970
BATT+
C862
U801
GSM_TX
R801
C866
U500
N_BAND_O
C802
R804
C817
C850
R817
R820
R821
C860
C864
C800
R813
R815DNP
R816DNP
DEF_REF
U500
LV_EXC_EN
Q906
C849
DET_AOC
U500
E3970
BATT+

D1000: WCDMA RX Downconverter (MAX2388)



DESCRIPTION

The first IC in the WCDMA Rx line up is U310 (MAX2388), which is an LNA and down converter mixer combination. The RX frequency will be mixed down to an IF frequency of 190MHz. The MAX2388 also has a shutdown mode to power down the IC, via MAX2388_SHDN*, during the front-end receiver's idling period to conserve battery life. U310 operates from the PCAP supply voltage RC_VCCA (derived from VRF_RX_2_775V). The nominal gain expect is ~15dB.

U310 operates in high gain mode selectable from RX_RF_ATTEN by the HARMONY_LITE . The nominal gain expected while in this mode is 15dB. During high input signal levels the LNA will be off.

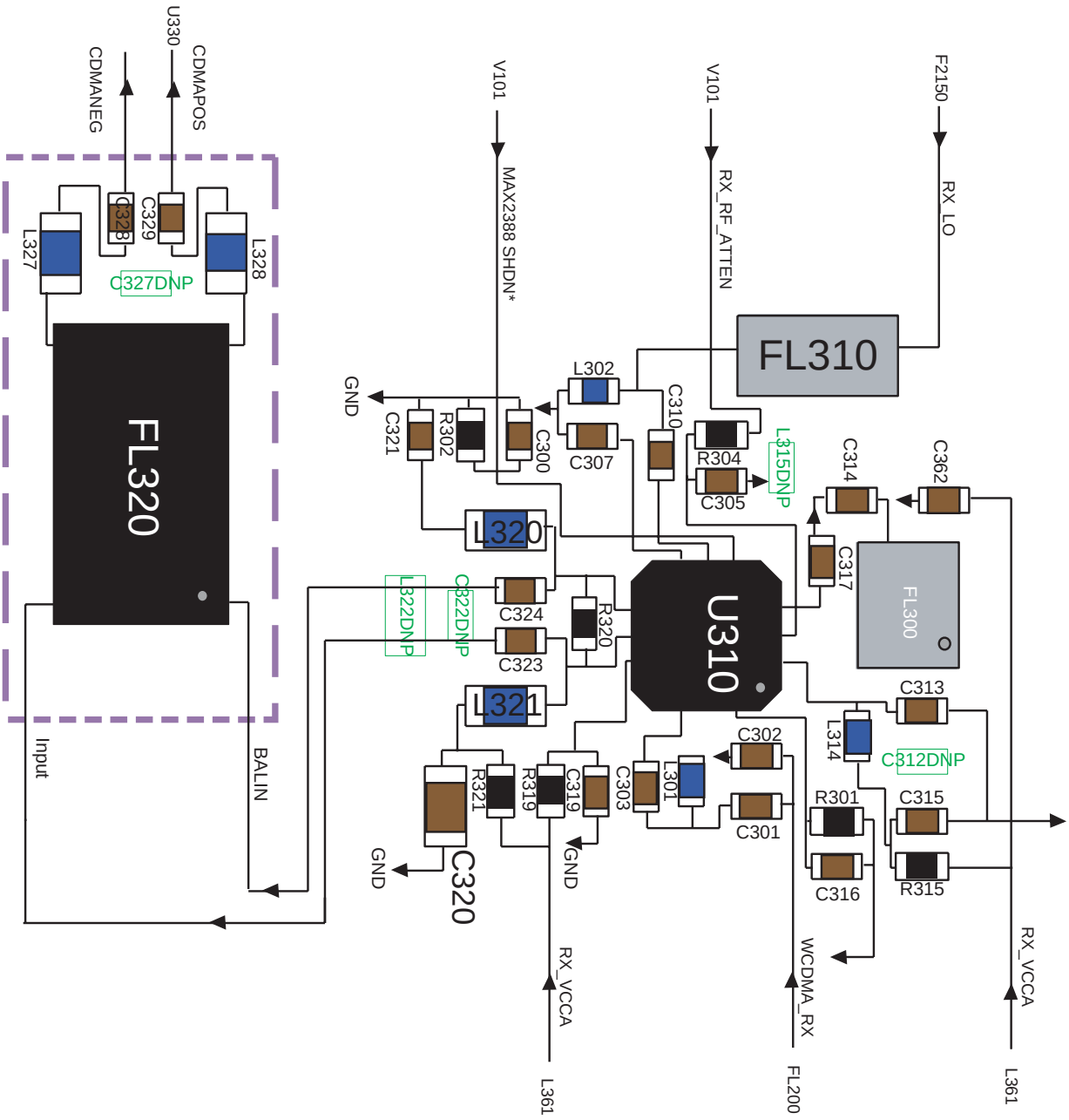
The receive mixer is a wideband, single-balanced design. The input RF_LO (pin #5) receives the VCO frequency (2330 - 2360MHz) through FL310 from U140 (VCO). The RF input (LNA_IN, pin #10) receives the RX frequency (2110 - 2170MHz) from FL002.

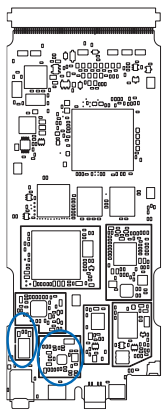
The MIX_IN (pin #3) input is connected to LNAOUT (pin #1) through FL300. The function of FL300 is to provide image rejection and out-of-band interferers filtering. The frequency conversion process performed by the mixer / oscillator combination sometimes will allow a frequency other than desired frequency to be fed into the IF and subsequently amplified.

The IF mixer output (190MHz) appears on the differential IFPOS (pin #8) and IFNEG (pin #7). These open-collector outputs require an external inductor (L320 & L321) to VCC for DC biasing.

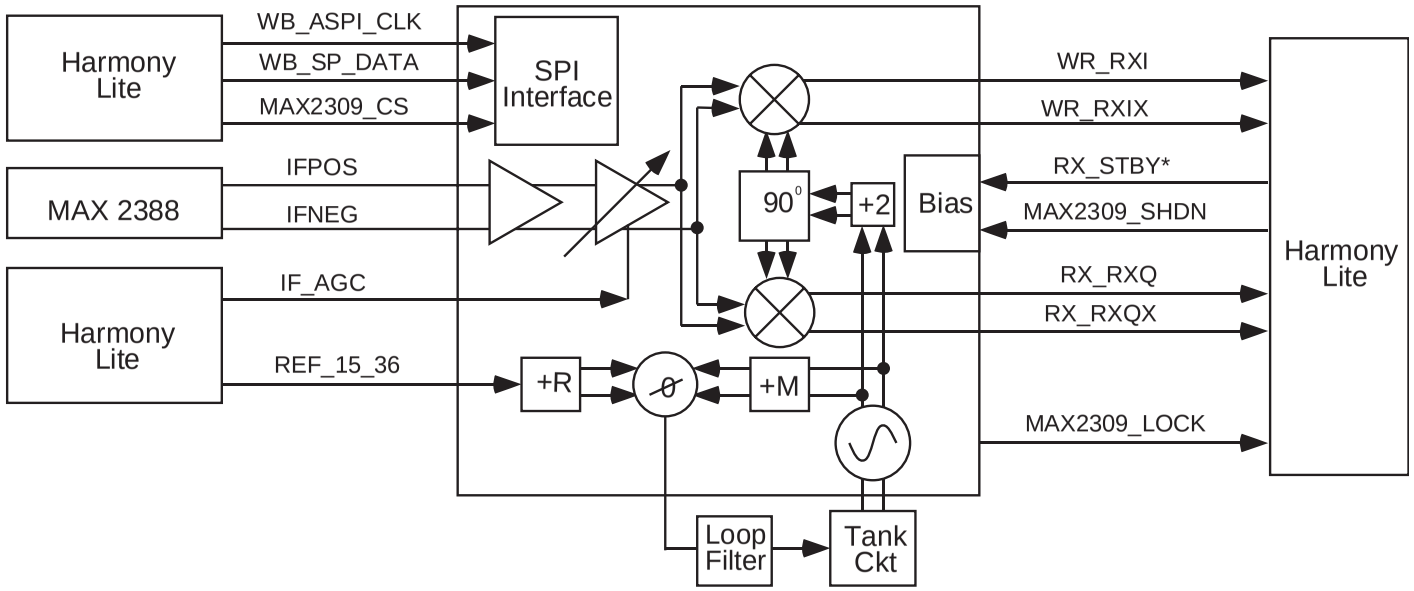
The 190MHz IF frequency passes through FL320. The IF SAW filter has a nominal center frequency of 190MHz and a bandwidth of 3.84MHz. Between the input match (C323, C324 & L322), output match (L327, L328, C328, C329, & C325) and the filter (FL320)- the expected nominal losses is ~10dB.

D1000: WCDMA RX Downconverter (MAX2388)





D1000: WCDMA RX Demodulator (MAX2309)



DESCRIPTION

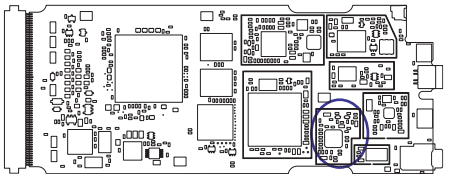
The MAX2309 is an IF quadrature demodulator with the signal paths consisting of a variable-gain amplifier (VGA) and an I/Q demodulator. The IF LO synthesizer's reference and RF dividers are fully programmable through the 3-wire serial bus (WB_ASPI_CLK, WB_SPI_DATA, MAX2309_CS). The 190MHz IF is demodulated to BaseBand differential in phase (I+ / I-) and quadrature (Q+ / Q-) signals to be passed through to the receiver's backend IC, HARMONY LITE. The IC operates from a pair of supply voltages RX_VCCD & RX_VCCA derived from VRF_RX_2_775V.

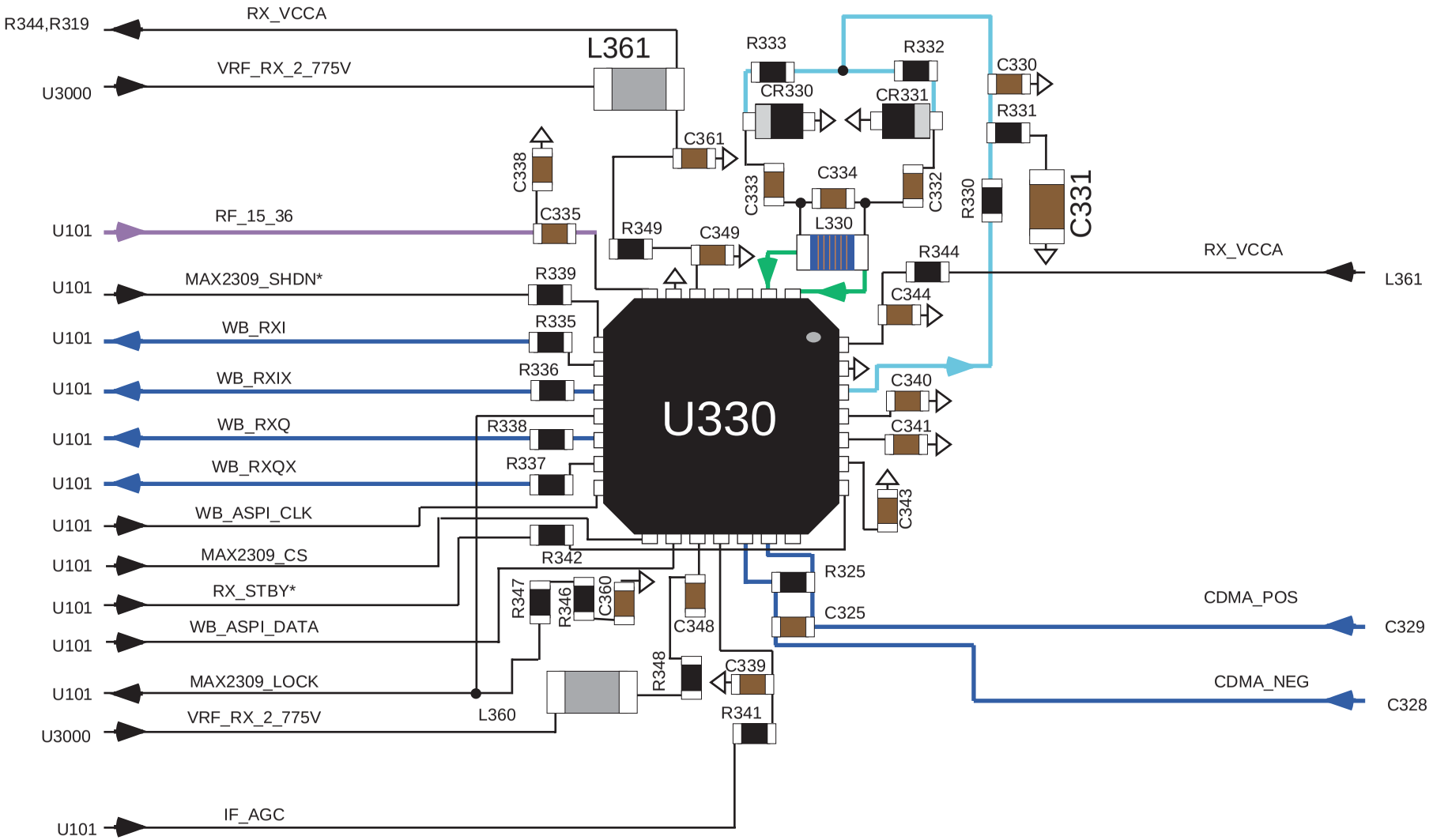
The MAX2309 VCO output frequency is controlled by an internal phase lock loop (PLL) synthesizer. The external loop filter consists of the components connected to pins #1 and #2 (& pin #26). The VCO output frequency (Tank+ / Tank-) at pins #1and pin #2 are divided down internally, to a desired comparison frequency. The reference signal at pin #7 (REF_15.36MHz) is also divided down to the same comparison frequency. The two divided signals are compared with a three state digital phase detector. The internal phase detector drives the charge pump as well as the lock-detect logic. The charge pump output at pin #26(CP_OUT) is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency (380MHz) and closing the loop.

The AGC ensures that the I/Q inputs to HARMONY LITE are at constant signal level. The IF_AGC line is controlled by HARMONY_LITE with a DC control range of 1.2V to 2.1V.

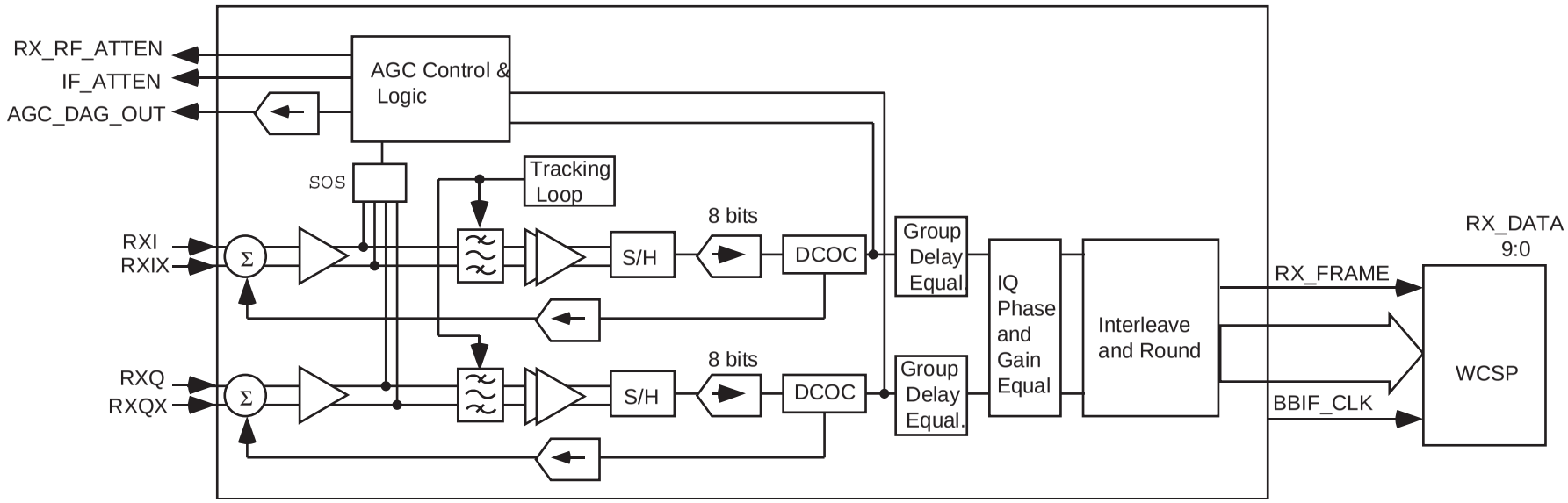
The MAX2309 has a shutdown mode to power down the IC, via MAX2309_SHDN*, during the front-end receiver's idling period to conserve battery life. RX_STBY* is used to shut down VGA and demodulator while maintaining the VCO, PLL, and serial interface active.

D1000: WCDMA RX Demodulator (MAX2309)





D1000: HARMONY Lite Recieve Section



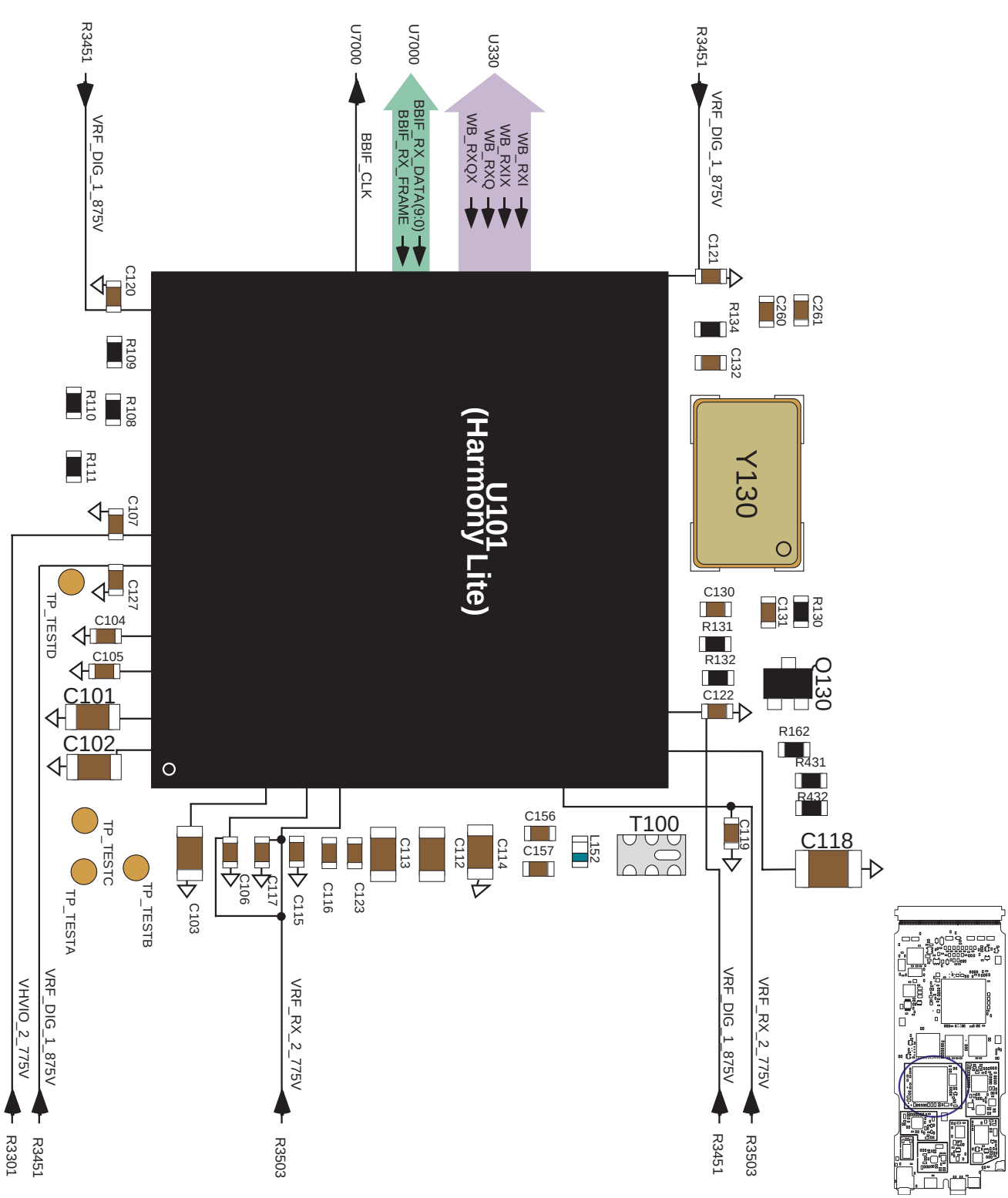
DESCRIPTION

The HAMONY LITE (U101) handles the backend processing of the WCDMA in phase (WB_RXI, WB_RXIX) and quadrature (WB_RXQ, WB_RXQX) signals from the demodulator. The HARMONY LITE performs an analog to digital conversion of gain, phase and DC offset correction of the RX data and sends it to the WCSP (U7000) via data lines RX_DATA(9:0).

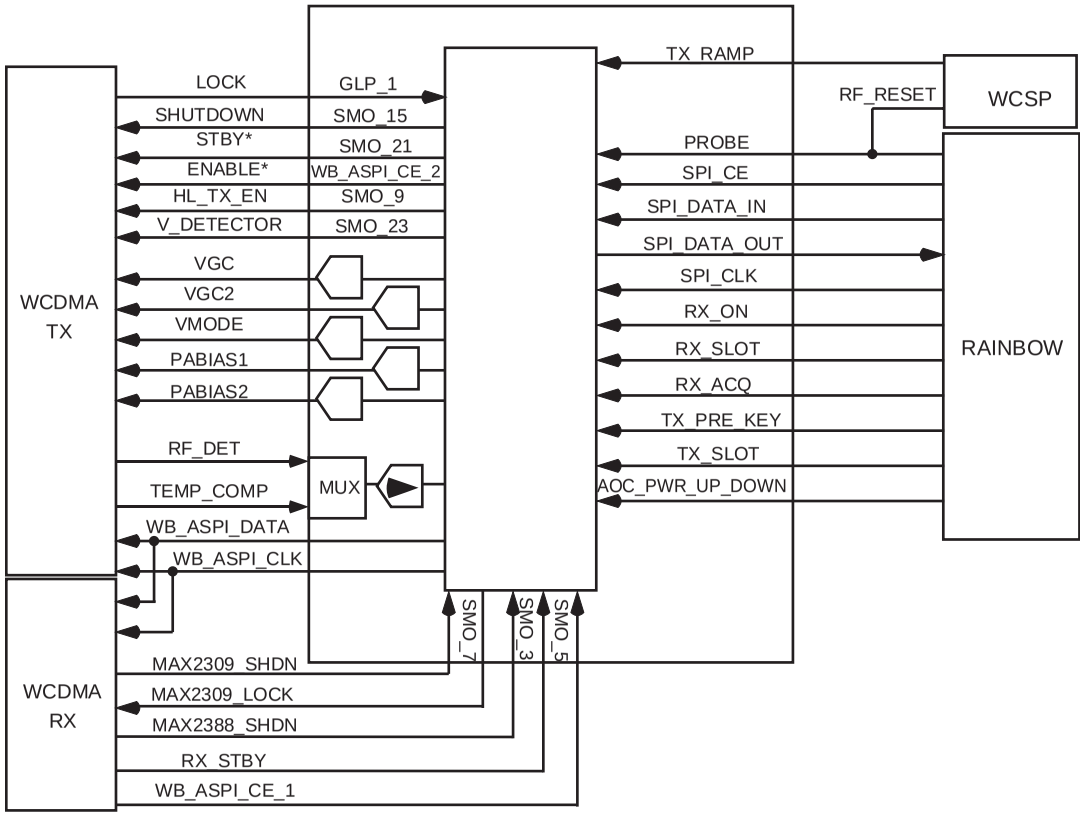
The analog I and Q signals are applied to the Harmony Lite IC, which processes the analog baseband portion of the radio. The SOS detector is used as an off-channel detector to detect the level of undesired interfering signals. It monitors the voltage swing at the input to the baseband filters, and provides a logic level output to the AGC/RSSI controller to indicate if the level is greater than a threshold specified by SPI bits, which then sets the appropriate gain setting in the front-end and IF stages.The AGC system provides overload protection for both the strong on-channel signal and the off-channel portion of the signal (interferers) that is present in the RF receive band. Signal levels are detected at the baseband filter inputs of the Harmony Lite (off-channel detector) as well as after the channel filtering and analog-to-digital conversion (on-channel detector).The digital AGC/RSSI block controls the bypass mode of the LNA and the IF variable gain amplifier. A digital representation of the desired received signal strength is sent to the Rainbow via the SPI.

Low pass filtering is performed on the complex I and Q signals, and then applied to the associated 8-bit ADCs and sampled at a rate of 4 times per symbol. A DC offset correction loop corrects for any DC offsets at the I and Q ADC inputs. A group delay equalizer is employed in the receive signal path following the baseband SRRC filter to minimize performance loss from the analog active order SRRC channel filter. Gain and phase mismatches between the I and Q channels can affect the detectability of a WCDMA signal in static and multipath fading conditions due to distortion caused in the QPSK signal constellation map. Thus, I/Q magnitude and phase imbalance correction circuits are used. At the output of the Magnitude Equalizer, the I and Q values are rounded from 8 bits to 6 bits and then multiplexed and routed to the digital signal processing circuitry located on the Rainbow IC.

D1000: HARMONY Life Recieve Section



D1000: HARMONY Life (Control Section)



DESCRIPTION

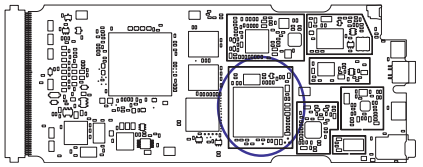
There are several functions that the sequence manager is controlling.

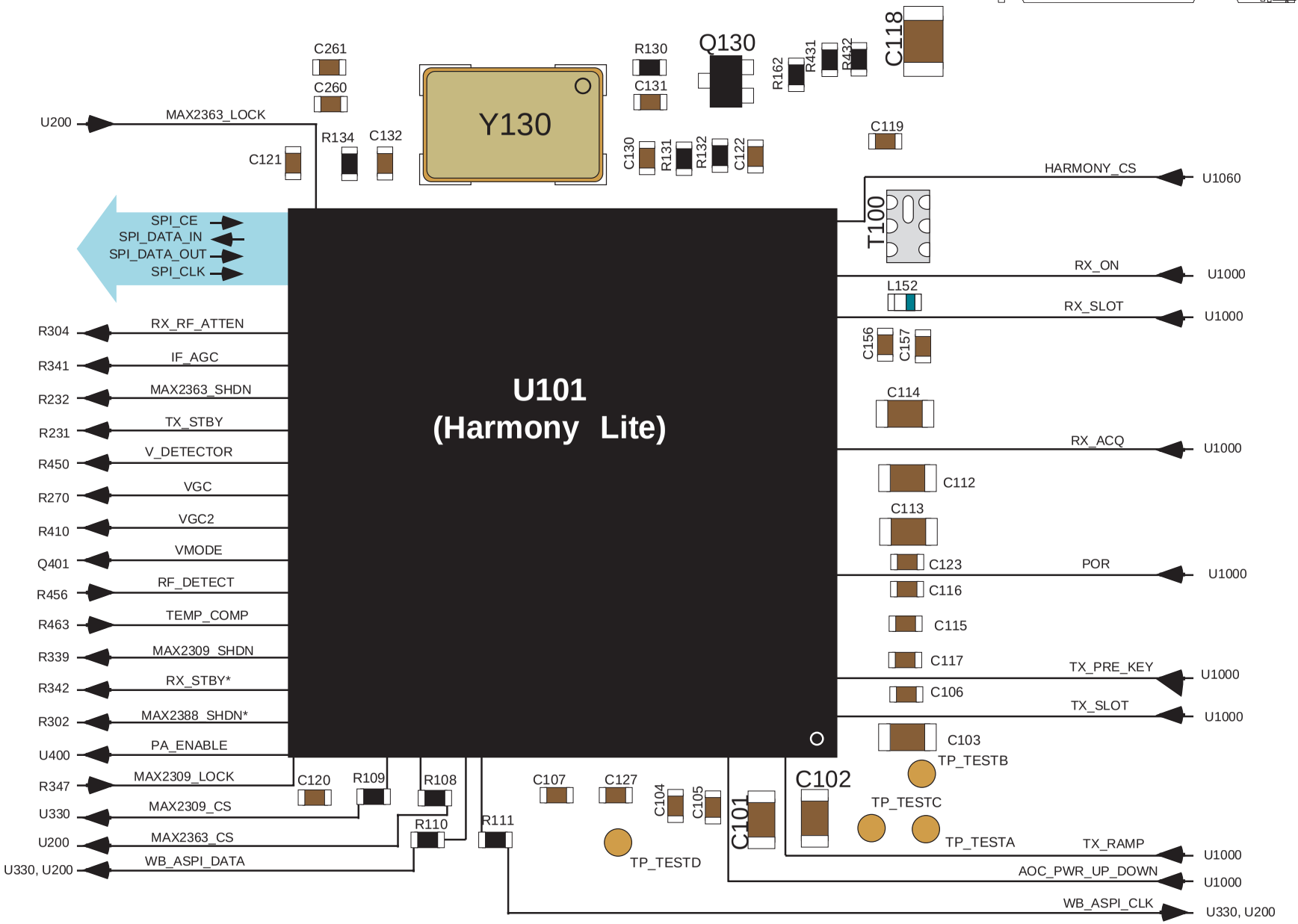
1. Sequence manager outputs to external devices
2. On/Off control of clocks, battery save signals etc…
3. Clock frequency selection for correction paths
4. DCOC register selection coarse, medium and fine modes

The HARMONY LITE has two sets of SPI interfaces; one set is for handling the control interface for the transceiver (AUXSPI lines) and ones for interfacing with RAINBOW (SPI lines). Further, all SPI interface is generated from RAINBOW and written to HARMONY_LITE or parsed through to the MAXIM (U200 & U310) parts.

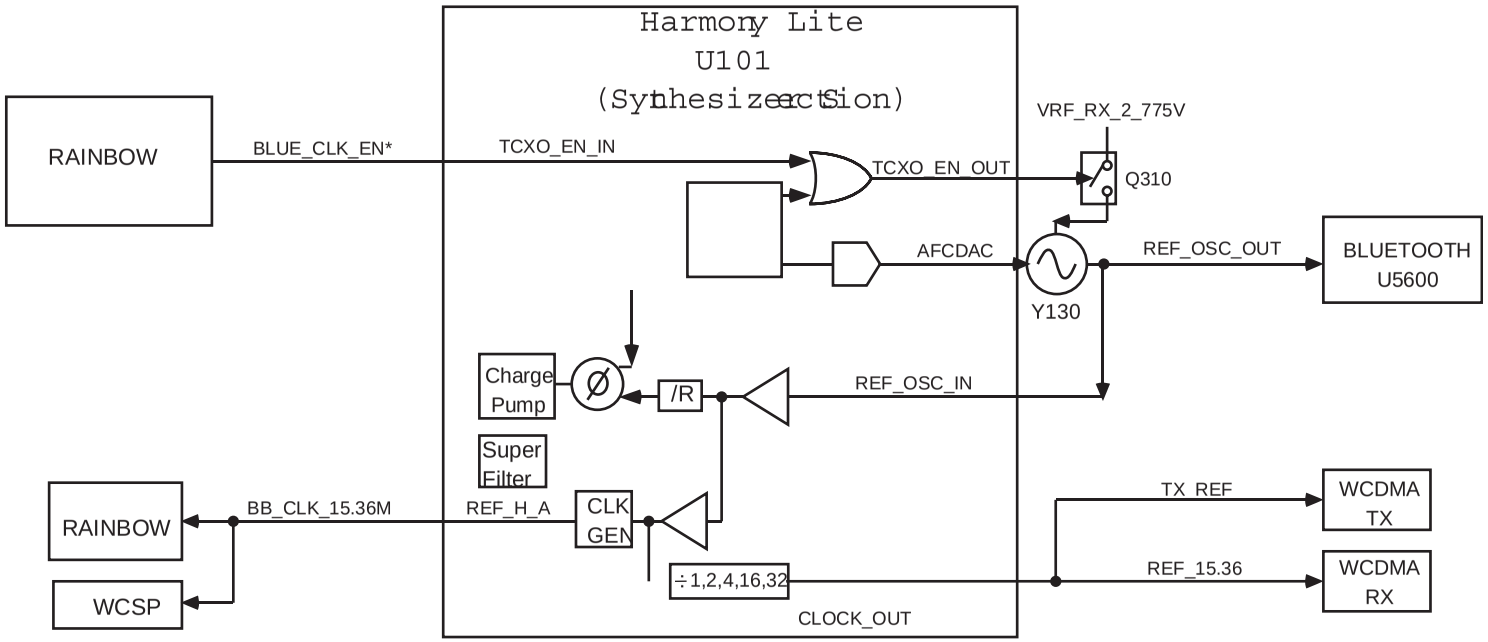
Layer one timing signals control the functionality of the RF section of the transceiver relative to the air interface. There are three signals defined on each transmit and receive section of the transceiver. TX_PRE_KEY and RX_ON are asserted before the need to receive or transmit in order to launch the necessary sequence of events to warm up the required functional blocks. TX_RAMP and RX_AQUIRE are asserted when actual transmission and reception are to begin. RX_SLOT and TX_SLOT are used during continuous transmission and reception to trigger events that must be aligned with slot boundaries. It's important to reiterate, the TX_RAMP directly corresponds to the PA turning on and RX_AQUIRE corresponds to data being sent to the WCSP.

D1000: HARMONY Lite (Control)





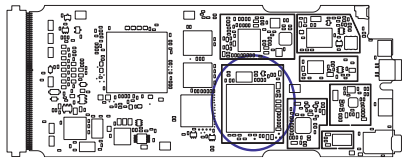
D1000: HARMONY Life (Synthesizer Section)

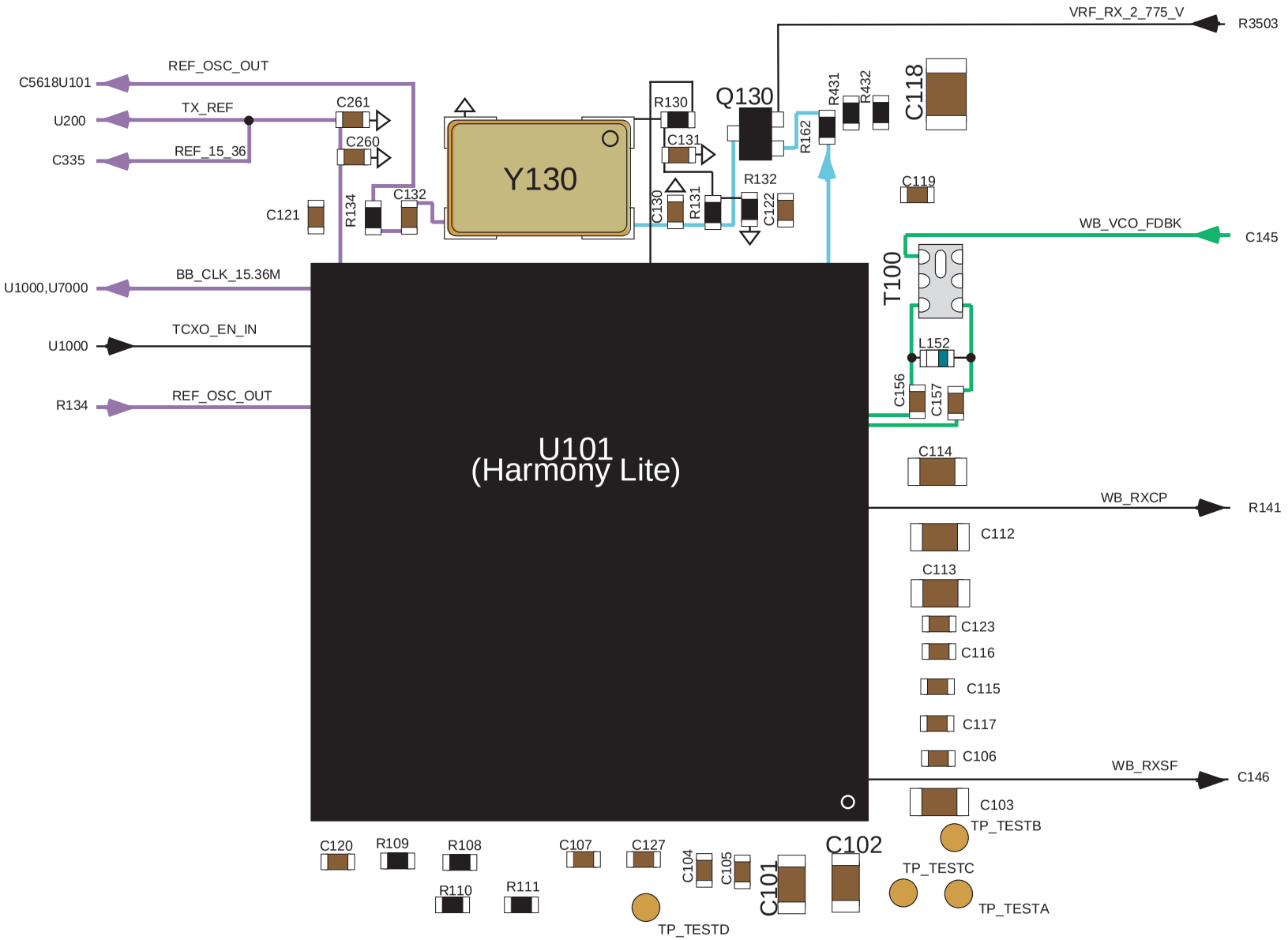


DESCRIPTION

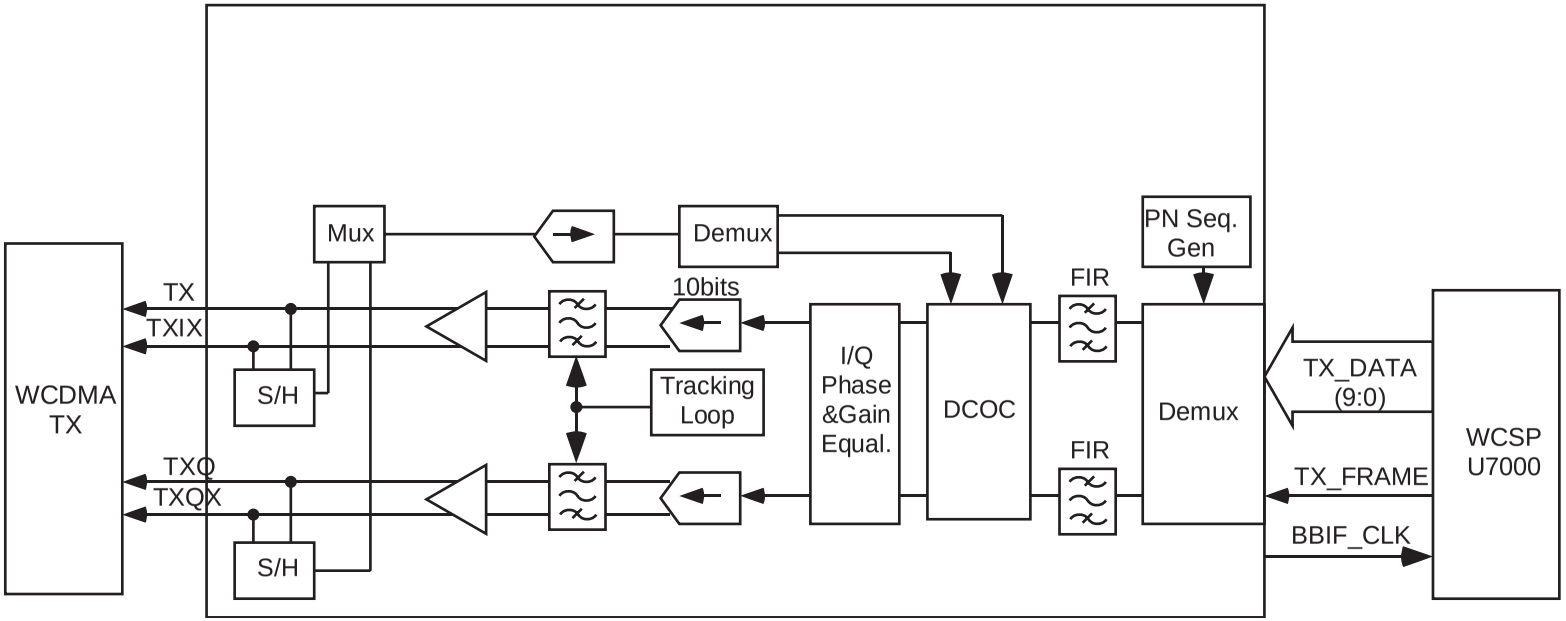
The clock source for the Harmony Lite (HLite) is a 15.36Mhz oscillator (TCXO). Y130 is used to generated the 15.36MHz clock source. AFC for Y130 is controlled by the Harmony Lite sequence manager via the AFCDAC line. The 15.36MHz clock source is enabled by an internal SPI bit and external control signal coming from RAINBOW(BLUE_CLK_EN*). The 15.36MHz clock source provides clocks to all A/Ds, DACs, external references and internal digital circuits of the Harmony Lite. In addition, clock references are generated for the RAINBOW, WCSP, RX and TX RF circuits.

D1000: HARMONY Lite (Synthesizers)





D1000: HARMONY Lite (TX Section)

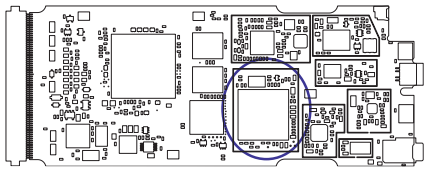


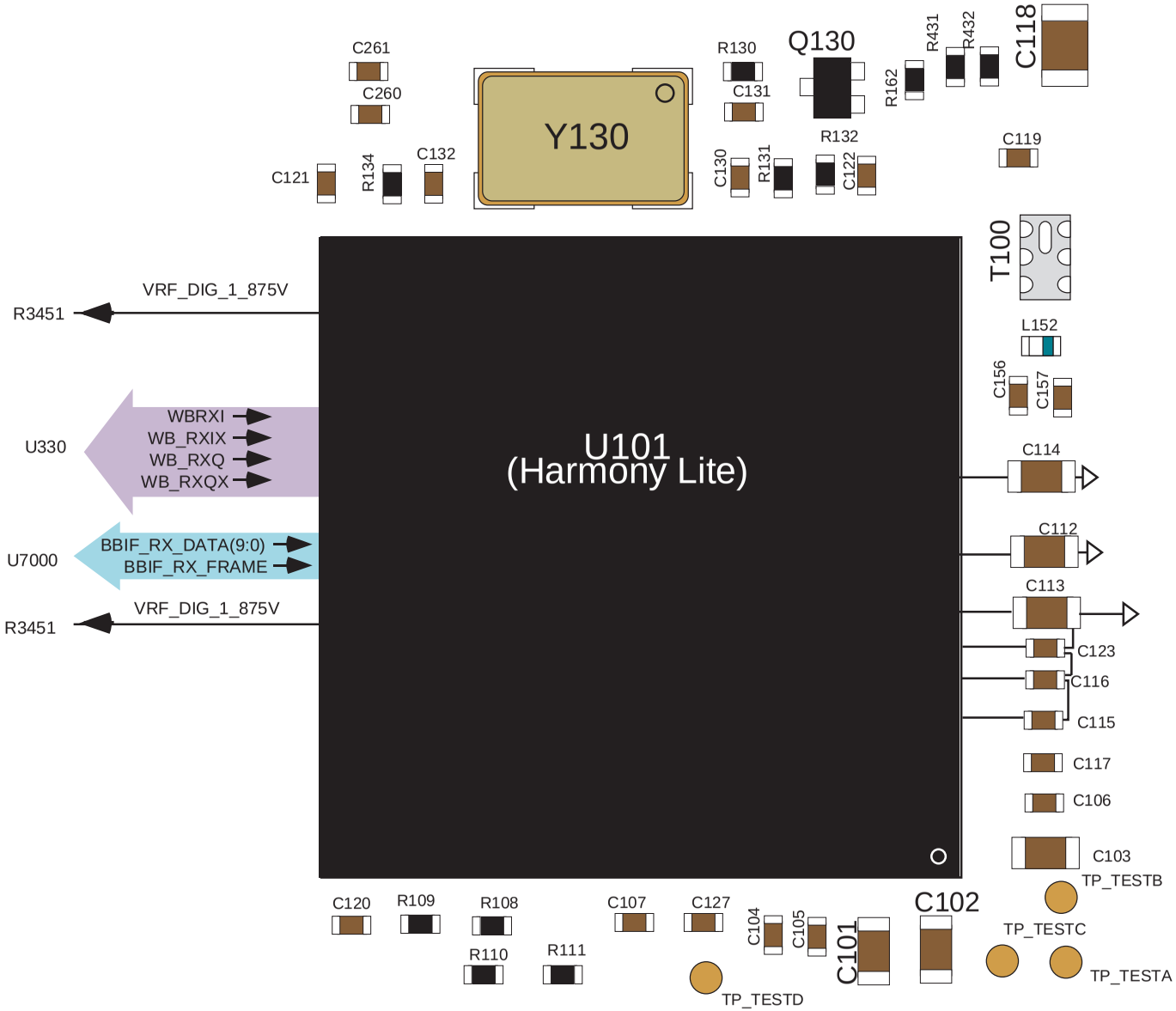
DESCRIPTION

The BBIF(TX_DATA) is the transmit data path for transferring digitally sampled I / Q data from the WCSP. The demultiplexing unit performs the I/Q deinterleaving function to supply separate I and Q channel data into the transmit FIR filters. The FIR filter design is used to meet 3GPP spec requirements of simultaneous transmission of a pilot channel and of multiple data channels each requiring a different spreading code and each requiring separate power control. The PN sequence generator provides I/Q interleaved 8-bit PN data into the demultiplexing section. The DC correction(DCOC) block is able to correct for DC offsets due to the D/A's, anti-aliasing filters, and transmit FIR filters in a feedback control loop. A mixed mode control loop located at the output of the transmit FIR filter is employed to correct DC offsets and I/Q gain imbalances, i.e. DCOC and I/Q Phase and Gain equalizer. The outputs of the I/Q gain equalization unit is fed into 10-bit I and Q DAC's. The programmable gain antialiasing filters, or TX smoothing filters, accepts differential I/Q signals of DC to 1.92MHz frequency components from the D/A Converters to attenuate the unwanted clock signals of 15.36MHz and to smooth the signals for the TX modulator(MAX2363). The output of the TX smoothing filters are then fed into a multiplexed 6-bit A/D with sample/hold scheme. This gives the information of the amplitude and the DC common mode voltage from the I / Q Tx filter outputs by a single Analog-to-Digital Converter (ADC) as the part of digital correction loop.

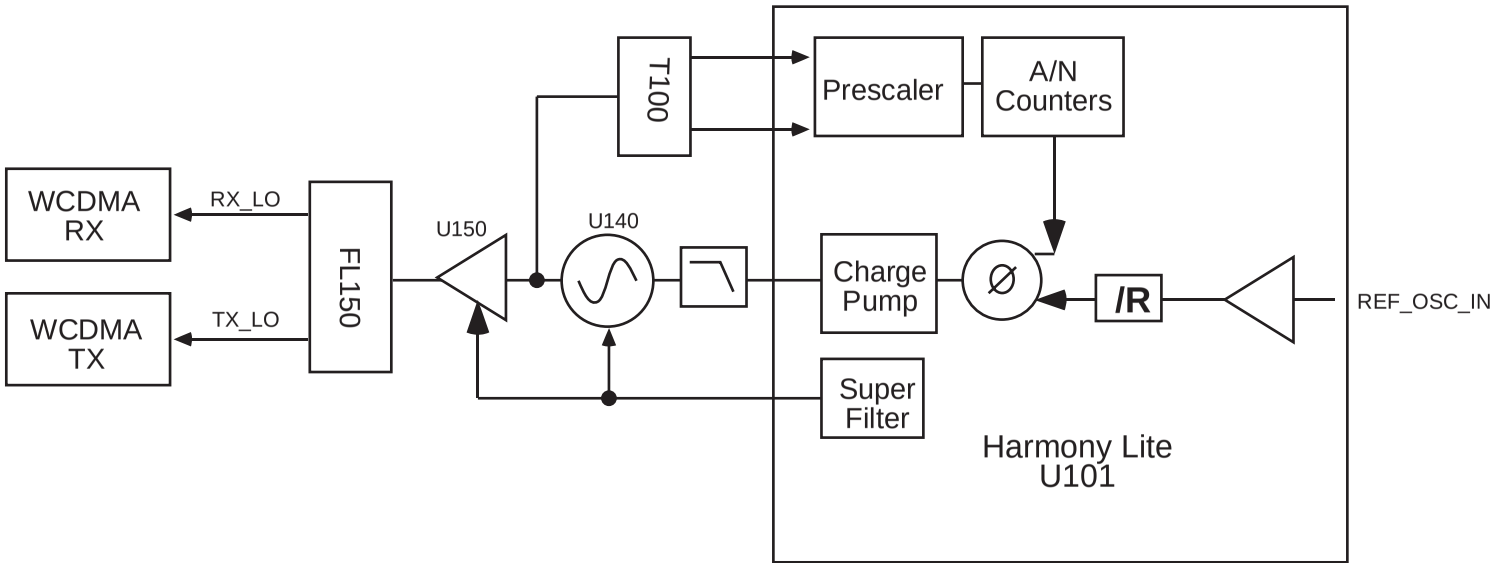
The differential TX I and TX Q signal are finally fed into the TX modulator(MAX2363).

D1000: HARMONY Lite (Transmit Section)





D1000: WCDMA VCO

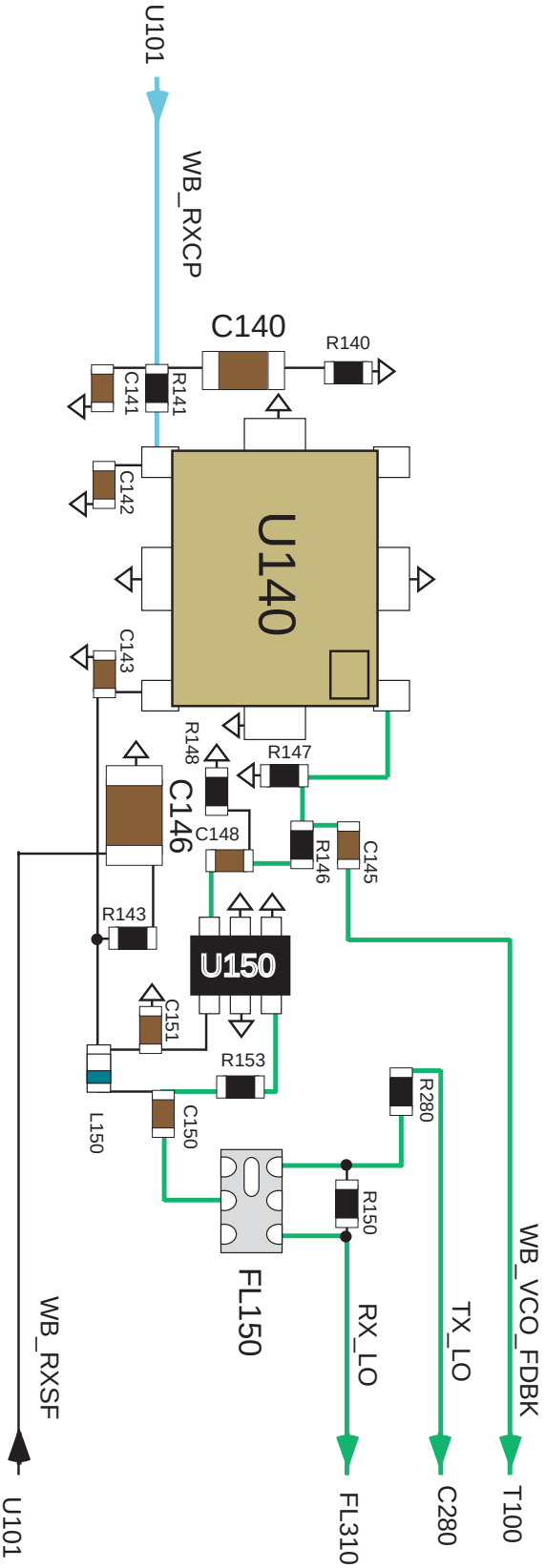


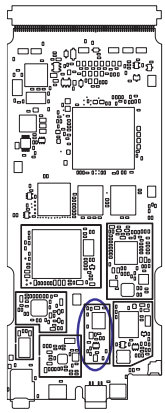
DESCRIPTION

The WCDMA VCO(U140) has a frequency range of 2.3G thru 2.36GHz, supplying both the receiver and transmitter with an LO. The control range is controlled by HARMONY_LITE with a control range between 0.5 - 2.5V, with an output power @ ~-3 - 3dBm. The WCDMA VCO output frequency is controlled by an internal phase lock loop (PLL) synthesizer. The phase locked loops use a fractional loop divider to permit fast lock times and low phase noise on their output signals. The VCO output frequency is fed into a prescalar and devided down into a desired comparison frequency. The 15.36MHz reference frequency is also divided down into a comparison frequency. The two divided frequencies are then compared with a phase detector. The phase detector will then drive the charge pump. The charge pump output is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency and closing the loop.

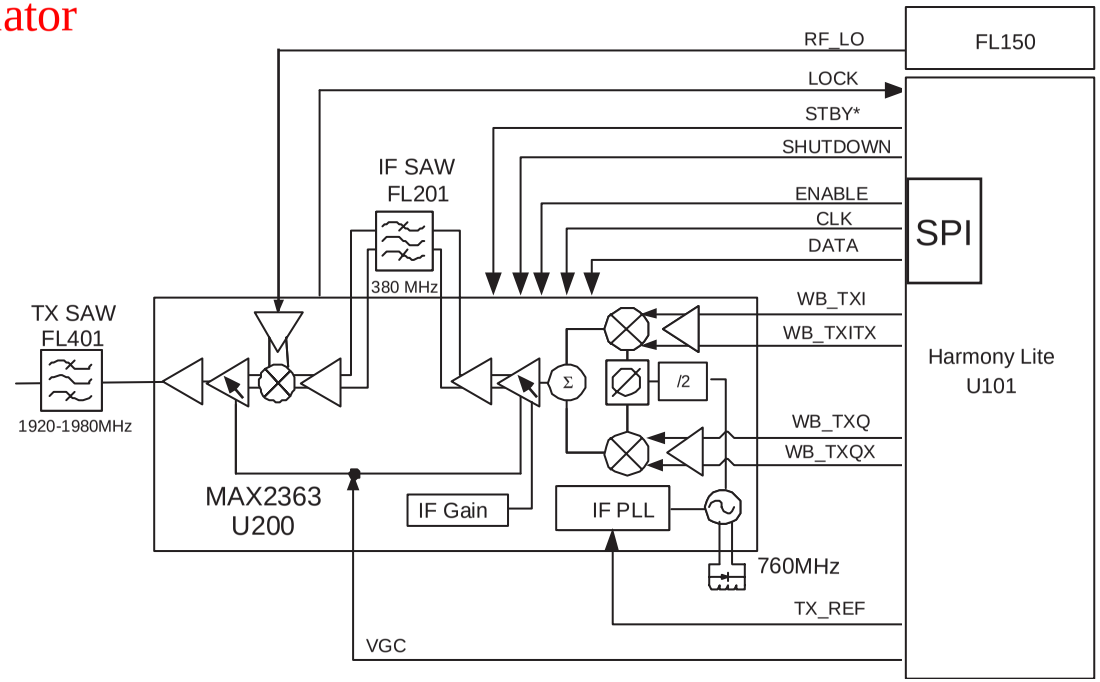
The superfilter block is used to provide a filtered supply voltage to the WCDMA VCO.

D1000: WCDMA VCO





D1000: TX Modulator (MAX2363)



DESCRIPTION

The in phase (I) and quadrature phase (Q) inputs are received at pins #23 (Q+), #24(Q-), #25(I+), & #26(I-) of U200. The expected DC bias levels are 1.30V - 1.40V with a minimum 300mVpp signal upon the DC level.

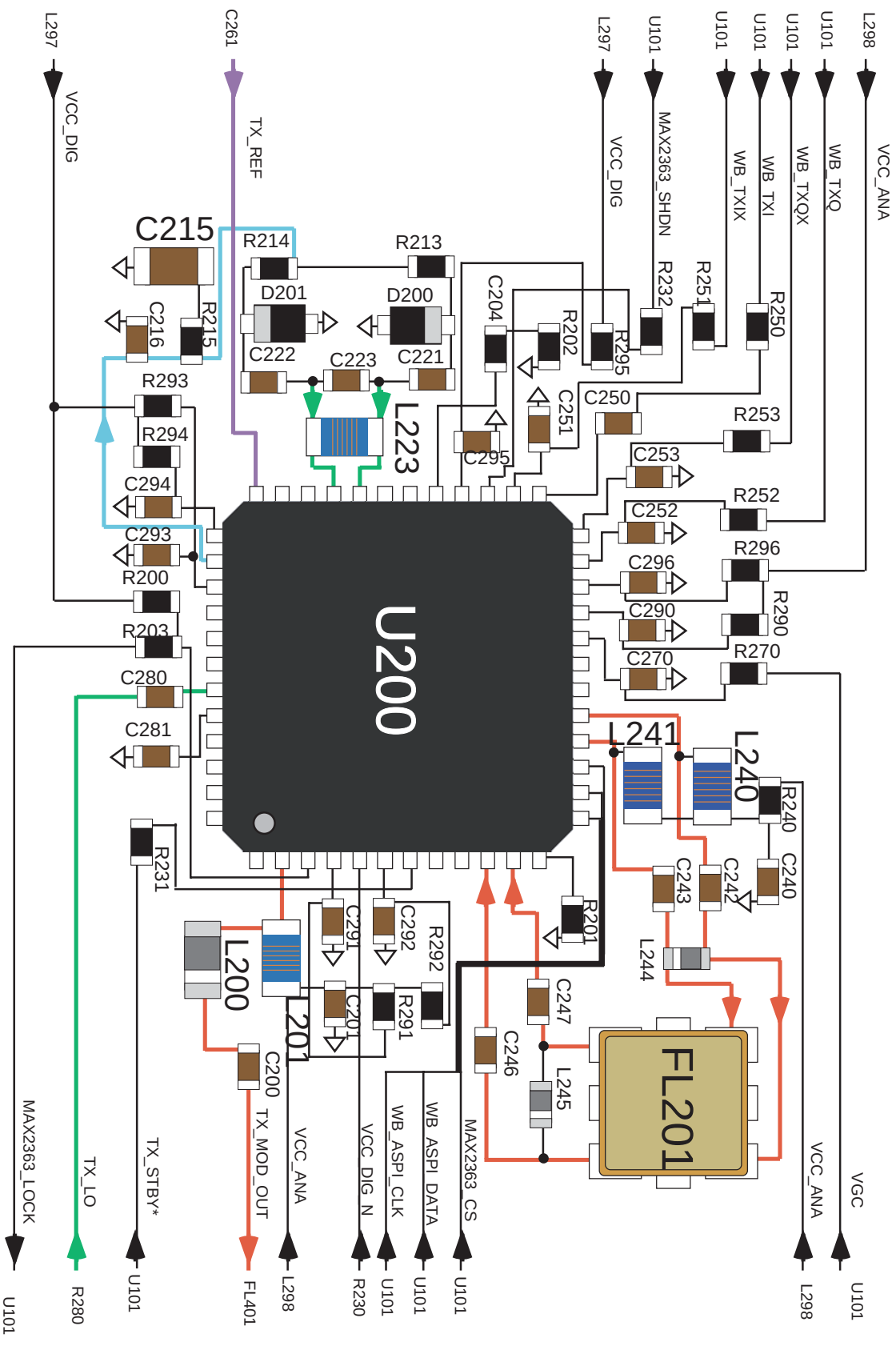
The MAX2363 receives the differential I/Q BaseBand input and converts it up to the IF frequency of 380MHz through a quadrature modulator and IF variable gain amplifier (VGA). The IFINH+ (pin #10) and IFINH- (pin #11) input are connected through off-chip FL201 from IFOUT+ (pin #17) and IFOUT- (pin #16), respectively. The function of FL201 is to provide image rejection and out-of-band interferers filtering. The frequency conversion process performed by the mixer / oscillator combination sometimes will allow a frequency other than desired frequency to be fed into the IF and subsequently amplified. The SAW filter (FL201) has a nominal center frequency of 380MHz and an insertion loss of ~ 3.5dB with a total bandwidth of 5MHz

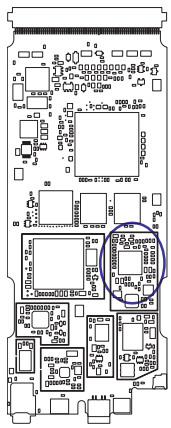
The IF and RF VGA (VGC) are common and allow for varying the IF / RF output level . HARMONY_LITE controls the VGC signal with a range of ~1.3 - 2.6V and provides gain a control range of ~75dB.

The MAX2363 VCO output frequency is controlled by an internal phase lock loop (PLL) synthesizer. The external loop filter consists of the components connected to pins #33 and #32 (& pin #38). The VCO output frequency (TankH+ / TankH-) at pin #33and pin #32 are divided down internally, to a desired comparison frequency. The reference signal at pin #36 (TX_REF) is also divided down to the same comparison frequency. The two divided signals are then compared with a three state digital phase detector. The internal phase detector drives the charge pump as well as the lock-detect logic(LOCK). The charge pump output (IFCP, pin # 38) is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency (760MHz) and closing the loop.

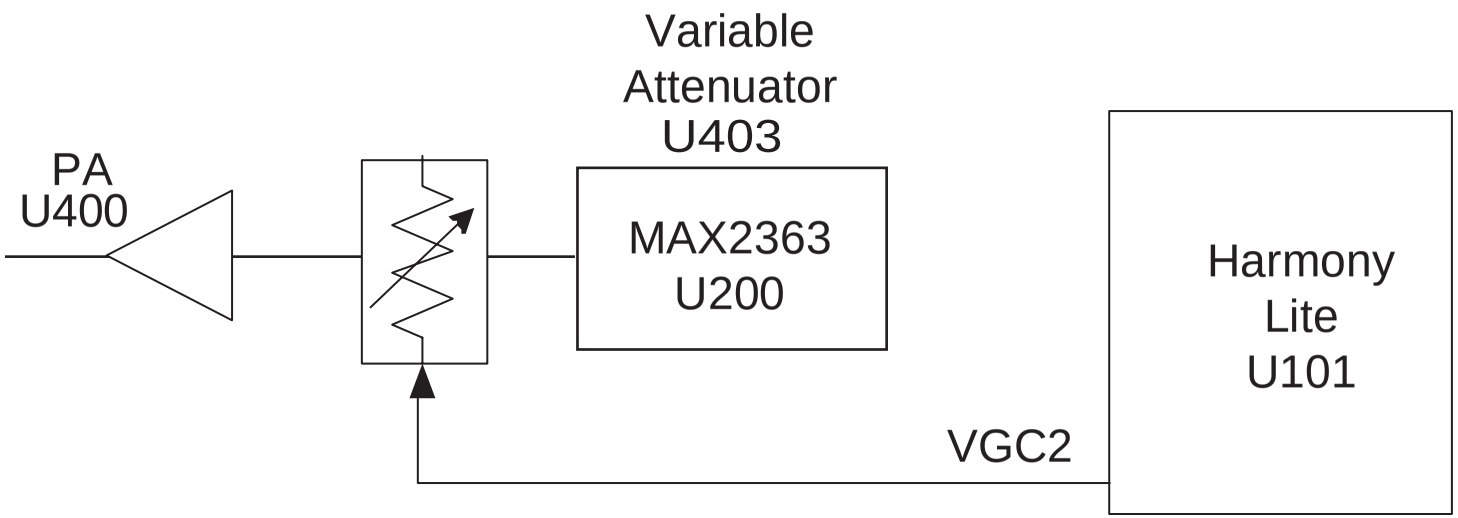
The differential IF output at pins #17 & #16 (IFOUTH+ / IFOUTH-) support high IF operation of frequency of 380MHz. The signal is routed to an off-chip IF SAW filter (FL201) and up-mixed to RF through an image reject mixer and RF VGA. The signal is further amplified with an on-chip PA driver. The RF signal is then routed to an interstage RF SAW filter (FL401).The IF synthesizer (760 MHz VCO) and local oscillator (RF_LO) buffer are both programmable through the 3-wire bus. The sequence manager from HARMONY_LITE programs standby mode(STBY*) and shutdown mode(SHUTDOWN). This IC operates from a pair of supply voltages VCC_DIG (isolated supply for IF_CP and 760 VCO) & VCC_ANA derived from VRF_TX_2_775V.

D1000: WCDMA TX Modulator





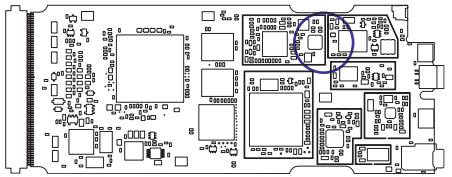
D1000: WCDMA TX Attenuator

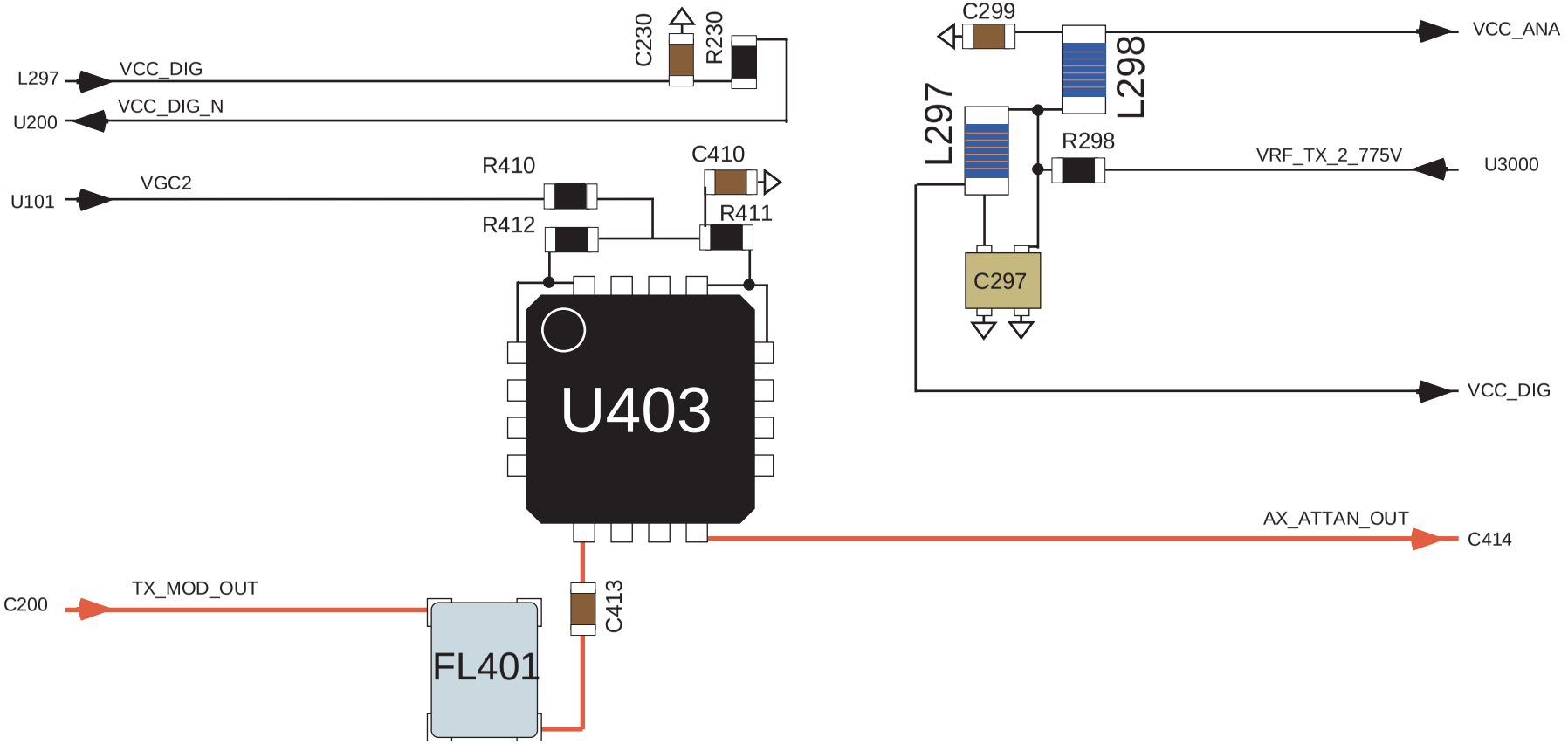


DESCRIPTION

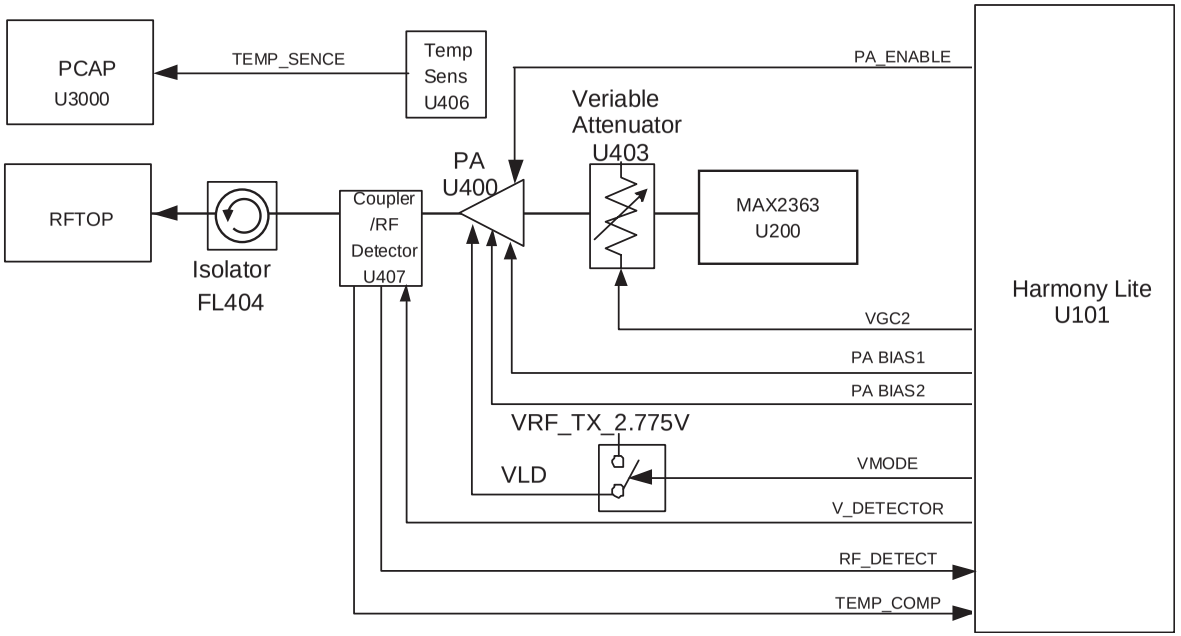
The U403 provides necessary attenuation of the TX carrier before reaching the PA so that it doesn't exceed the maximum allowable input of 1dBm of the PA and to control the overall power output of the transceiver. The U403 has a 16-18 dB of attenuation depending on the control voltage VGC2 applied at HYBOUT1 and HYBOUT2, which is controlled by Harmony Lite.

D1000: WCDMA TX Attenuator





D1000: WCDMA PA



DESCRIPTION

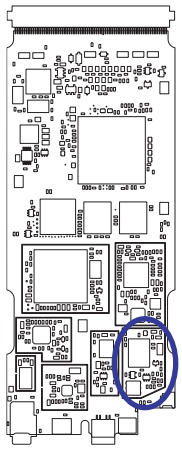
The U403 provides necessary attenuation of the TX carrier before reaching the PA so that it doesn't exceed the maximum allowable input of 1dBm of the PA and to control the overall power output of the transceiver. The U403 has a 16-18 dB of attenuation depending on the control voltage VGC2 applied at HYBOUT1 and HYBOUT2, which is controlled by Harmony Lite.

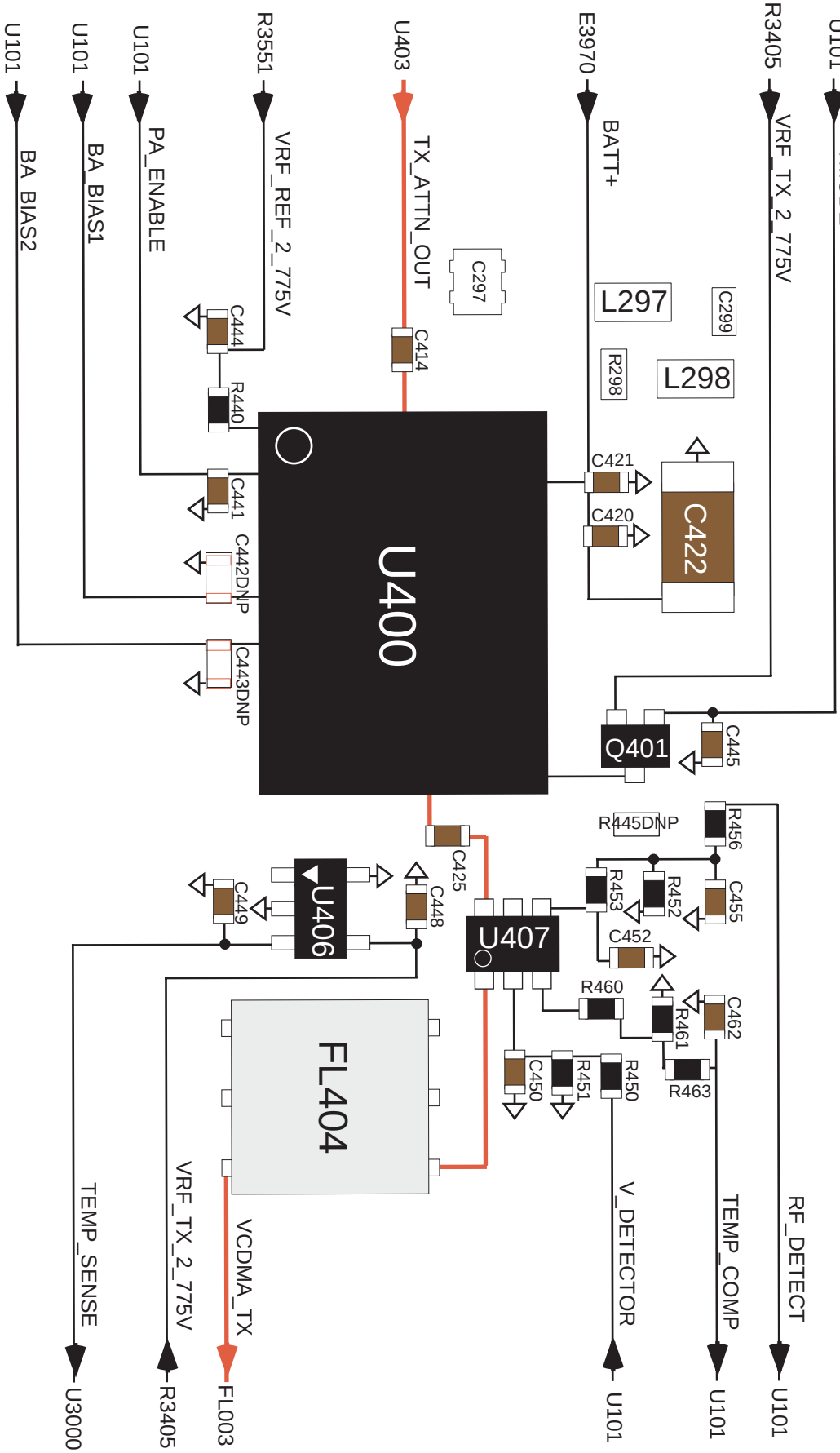
U400 is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 - 1980MHz. The nominal expected maximum gain is ~30dB. HARMONY_LITE controls the RF biasing of the amplifier at pins #4 (PA_BIAS1) and #5 (PA_BIAS2) with a control range of 0 - 2.5v. HARMONY_LITE also controls pin #12 (VLD) for PA load switching. Although not implemented, the theory of PA load switching in WCDMA is vitally important to conserve battery life and to avoid unnecessary radio interference with base stations. When VLD is at a low state (0v), the transmitter is in high power mode, consuming higher current but with overall better PA performance. When VLD is at a high state, the transmitter is in low power mode, consuming less current with overall poor PA performance. In theory, as the Tx power level increases or decreases beyond a certain power threshold, VLD is enabled or disabled. As Tx power decreases (as requested from a base station) down to ~14.5dBm, VLD will switch high. If Tx power is requested to increase beyond ~19dBm, VLD is switched low.

The power detector receives the amplified WCDMA RF signal at RF_IN (pin #6) from the PA. U407 is a combination directional coupler and temperature compensated power detector with a differential output. The power detector couples the TX power input and feedbacks an output RF_DETECT to HARMONY LITE. The TEMP_COMP also obtains the coupled power but removes the RF signal content, leaving a DC level. The DC level is feedback to HARMONY LITE. Expected nominal loss is <. 3dB.

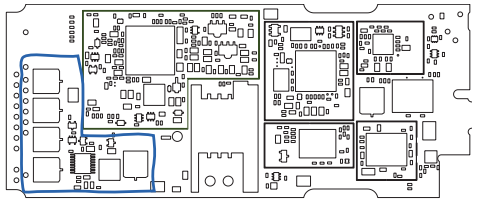
The isolator provides isolation between Front-End Module (FEM) and transmitter path. Nominal insertion loss is ~ 0. 55dB

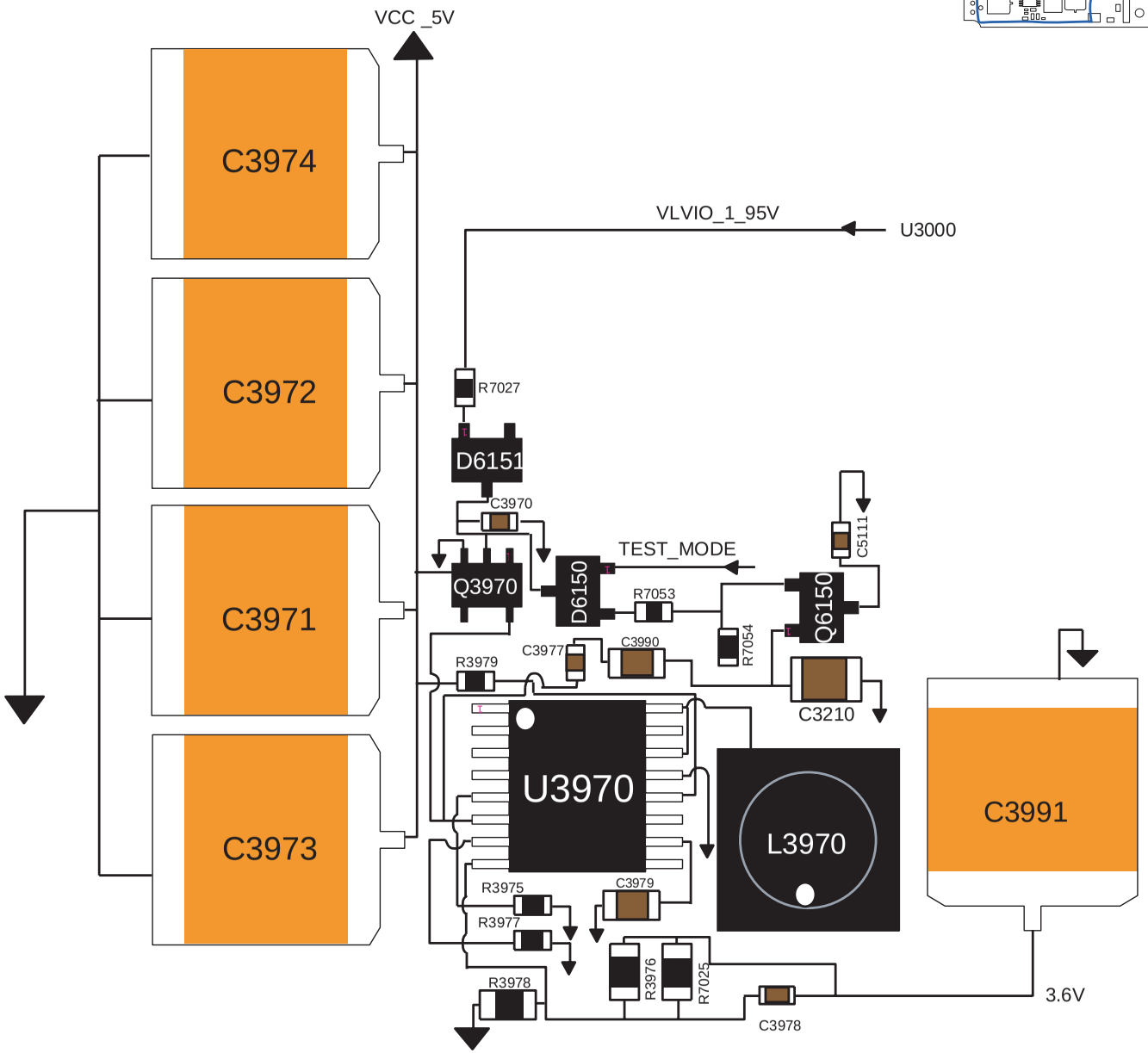
D1000: WCDMA PA



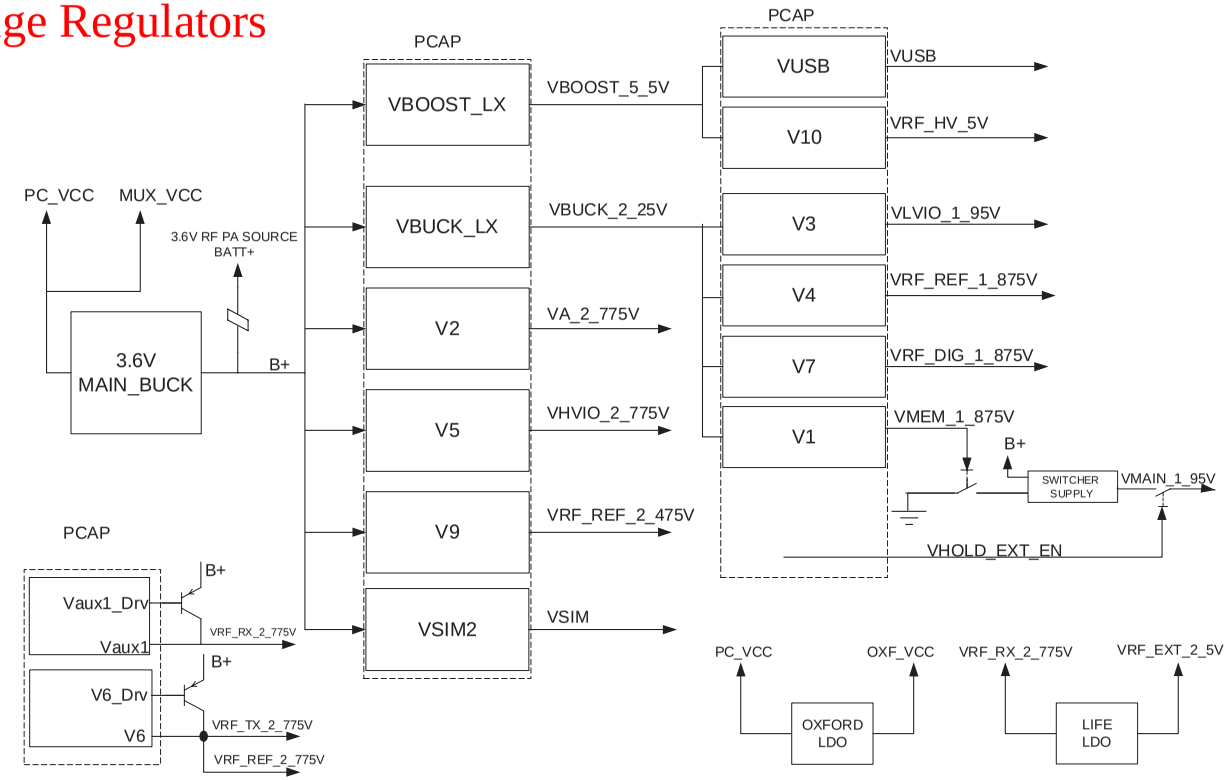


D1000: Main Buck Regulators





D1000: Voltage Regulators



DESCRIPTION

Voltage regulation is provided by the PCAP IC (U3000). Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry.

The regulators and their load circuitry are described below:

· VBOOST_LX (VBOOST_5_5V) - VUSB and V10 input voltage regulator

· VBUCK_LX (VBUCK_2_25V) - V1, V3, V4, V7, and V8 input voltage regulator

· Vsim2 (VSIM) - SIM card interface

· Vaux1 (VRF_RX_2_775V) - RF RX circuits

· VUSB - USB interface

· V1 (VMEM_1_875V) - Flash Core

· V2 (VA_2_775V) - Audio, ADC/DACs and Baseband Processor Peripherals.

· V3 (VLVIO_1_95V) - Rainbow I/O, and Flash I/O

· V4 (VRF_REF_1_875V) - Magic LV reference

V6 (VRF_TX_2_775V) - RF TX circuits

· V7 (VRF_DIG_1_875V) - Magic LV, and Harmony Lite

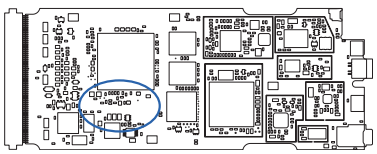
· V9 (VRF_REF_2_475V) - WCDMA PA Reference

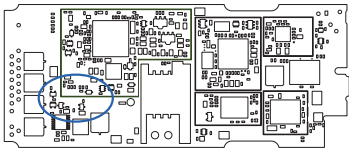
· V10 (VRF_HV_5V) - Magic LV and FEM

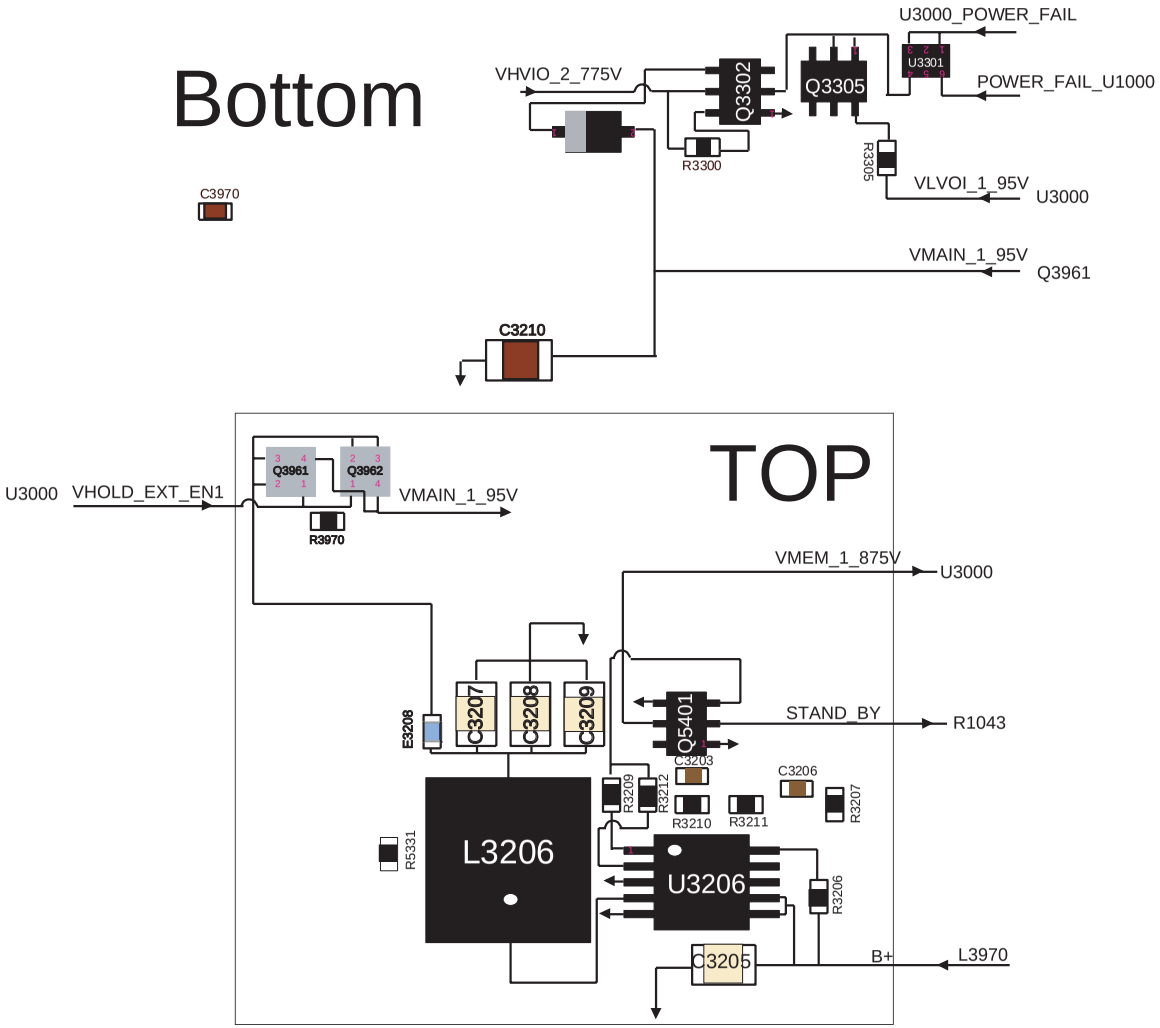
· OXFORD_LDO (OXF_VCC)- Oxford, EEPROM and Oxford Peripherals.

· LIFE_LDO (VRF_EXT_2_5V) - LIFE IC.

·3.6 MAIN_BUCK (B+) - MUX and PCAP



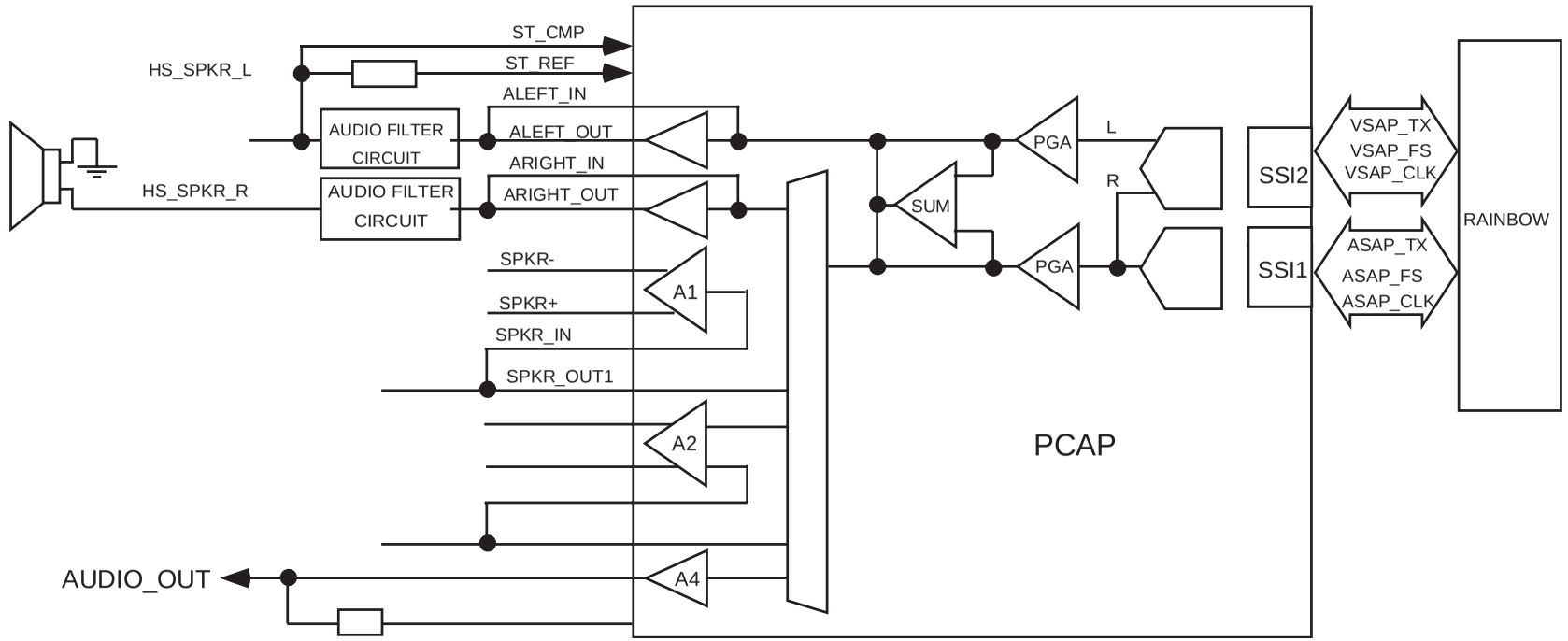




The VMAIN buck regulator U3206 provides Rainbow core voltage. It converts the 3.6V dc, provided by the Main Buck Regulator (U3970), into 2.2V dc.

D1000: RX AUDIO*

*If Applicable



DESCRIPTION

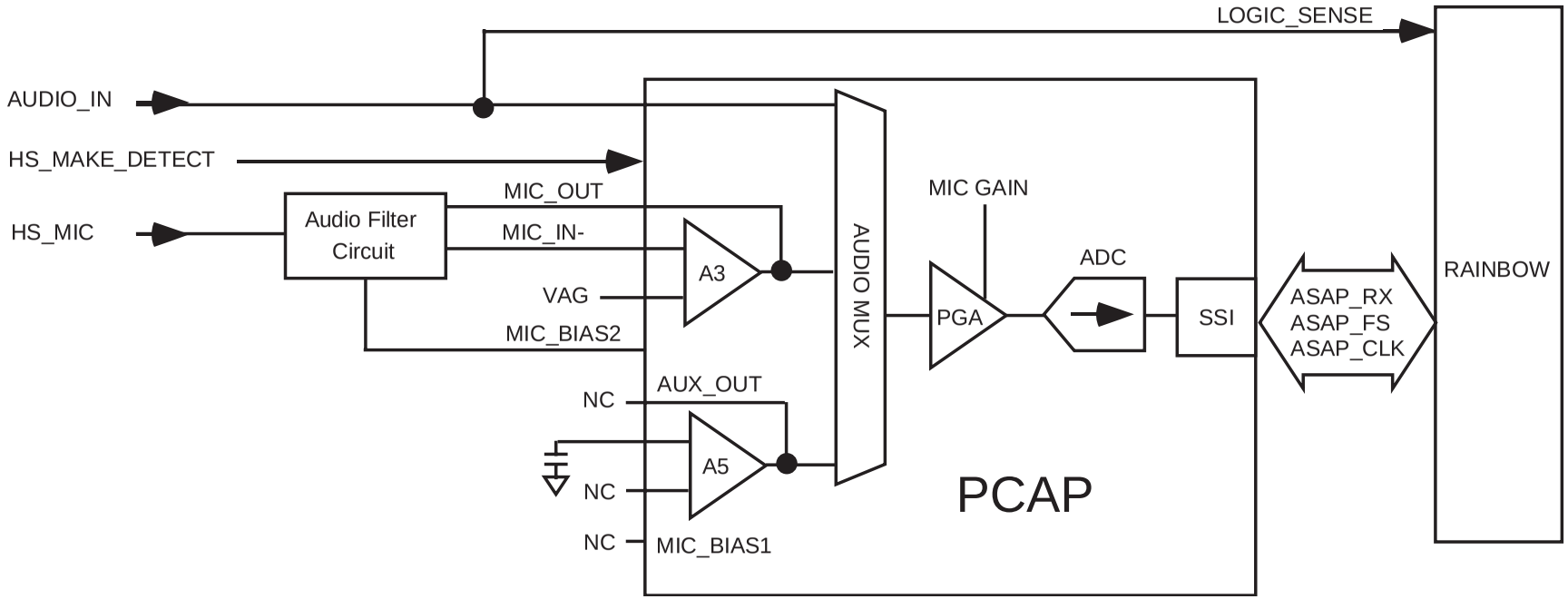
Receive audio data is transferred from the Rainbow to the PCAP through the ASAP interface. The data is then converted into an analog form through a 13-bit phone DAC. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons. In D1000, only headset interface is used.

The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

The Headset Speaker is driven by PCAP's internal Right amplifier. Following the speaker path from the PCAP pin ARight_Out, it is routed through C4356, R4352, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. The DC level of Audio_Out signal is used to externally command the phone module to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

D1000:TX AUDIO*

*If Applicable



DESCRIPTION

The headset microphone path (HS_MIC) is biased through R4396 and R4392, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier.

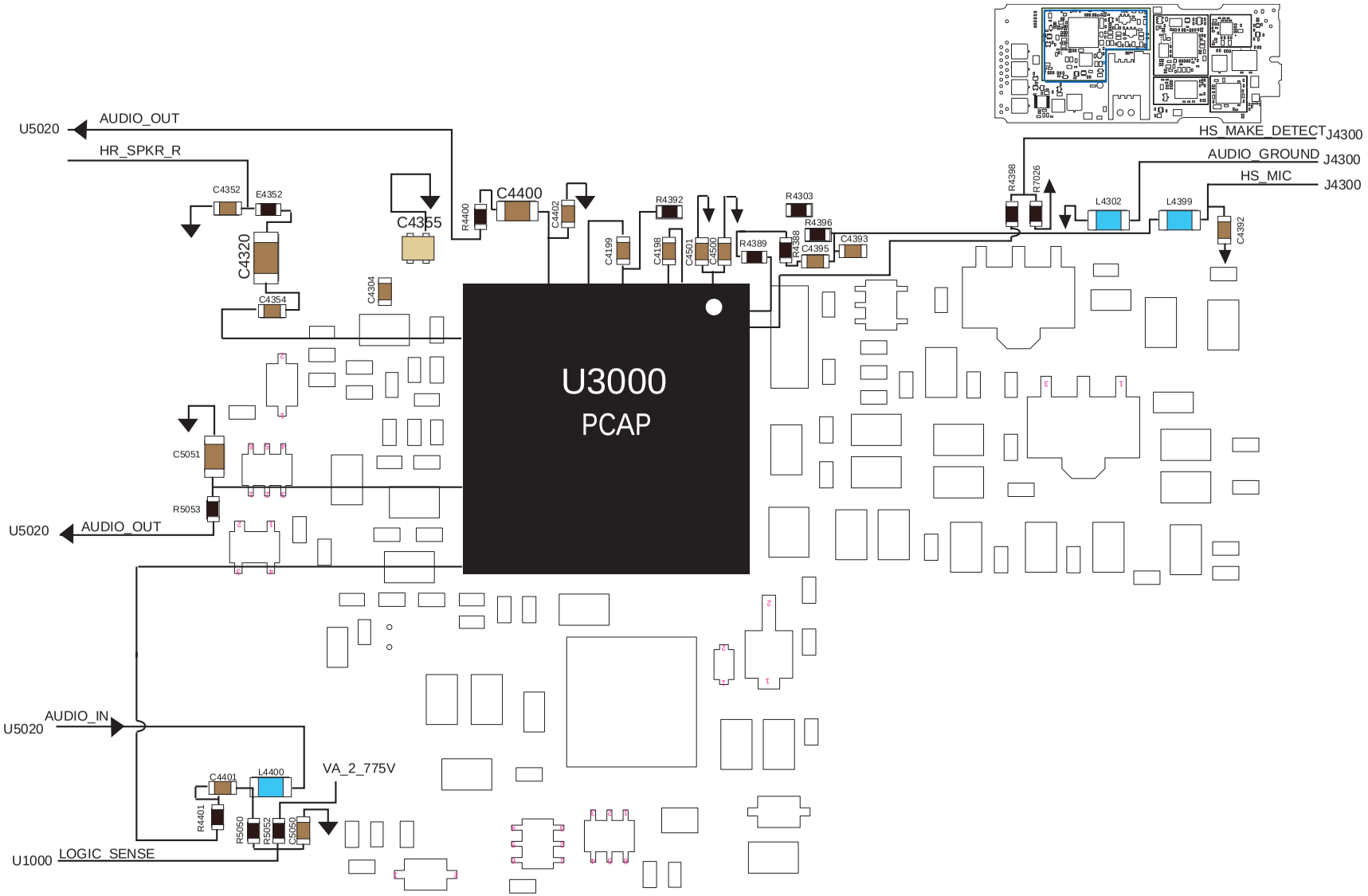
The HS_MAKE_DET line monitors the presence of a headset by detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

The External Microphone input (AUDIO_IN) is connected to the accessory connector for the mobile phone. The path is routed through L4400, C4401 and R4401 to the E XT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage. In addition to audio signals, AUDIO_IN supports detection of accessory devices. The accessory attached to the CE bus shall have an output impedance that will load LOGIC_SENSE to a predetermined level. The RAINBOW will read the input level of LOGIC_SENSE and configure the audio accordingly.

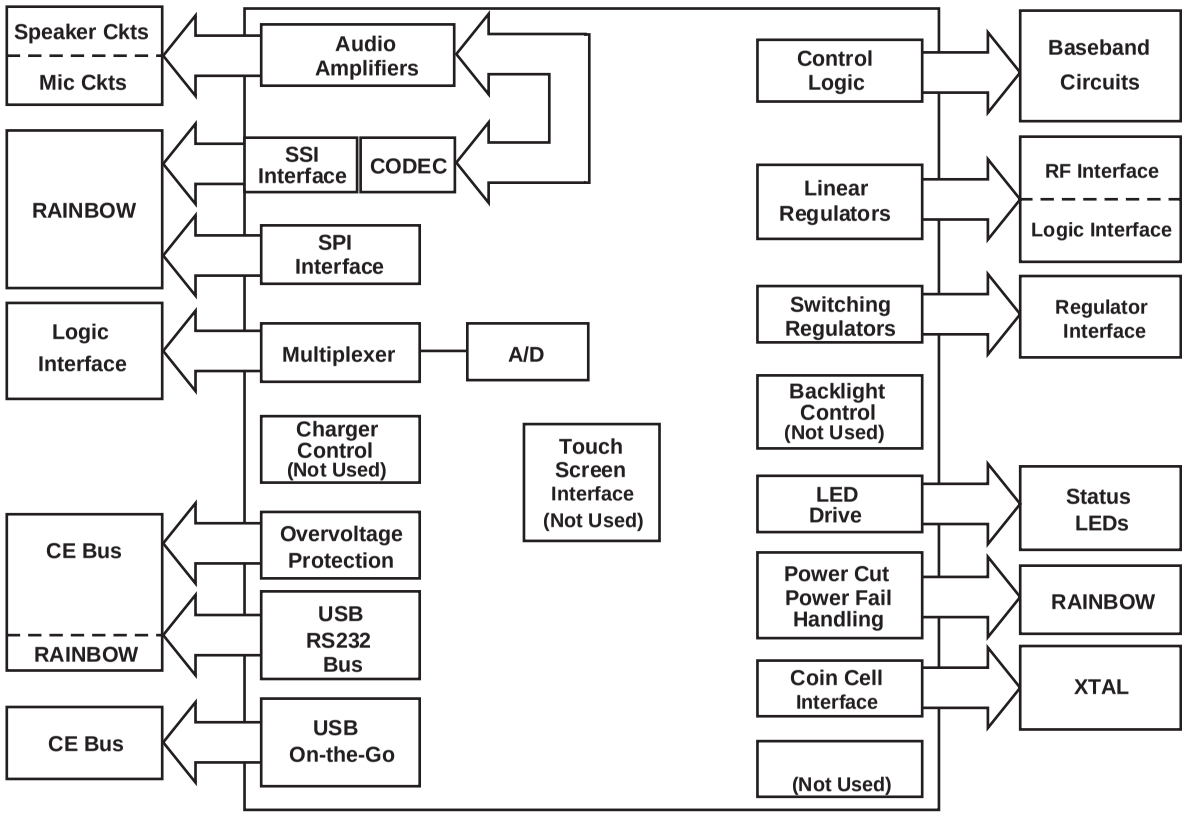
The proper Microphone path is selected by the AUD MUX controller and path gain is programmable at the PGA. The A/D converter willl convert incoming analog signals into 13-bit, 2's compliment, linear PCM words. The digital audio signals are then transferred to the Rainbow DSP through a four wire serial interface (ASAP).

D1000: AUDIO*

*If applicable



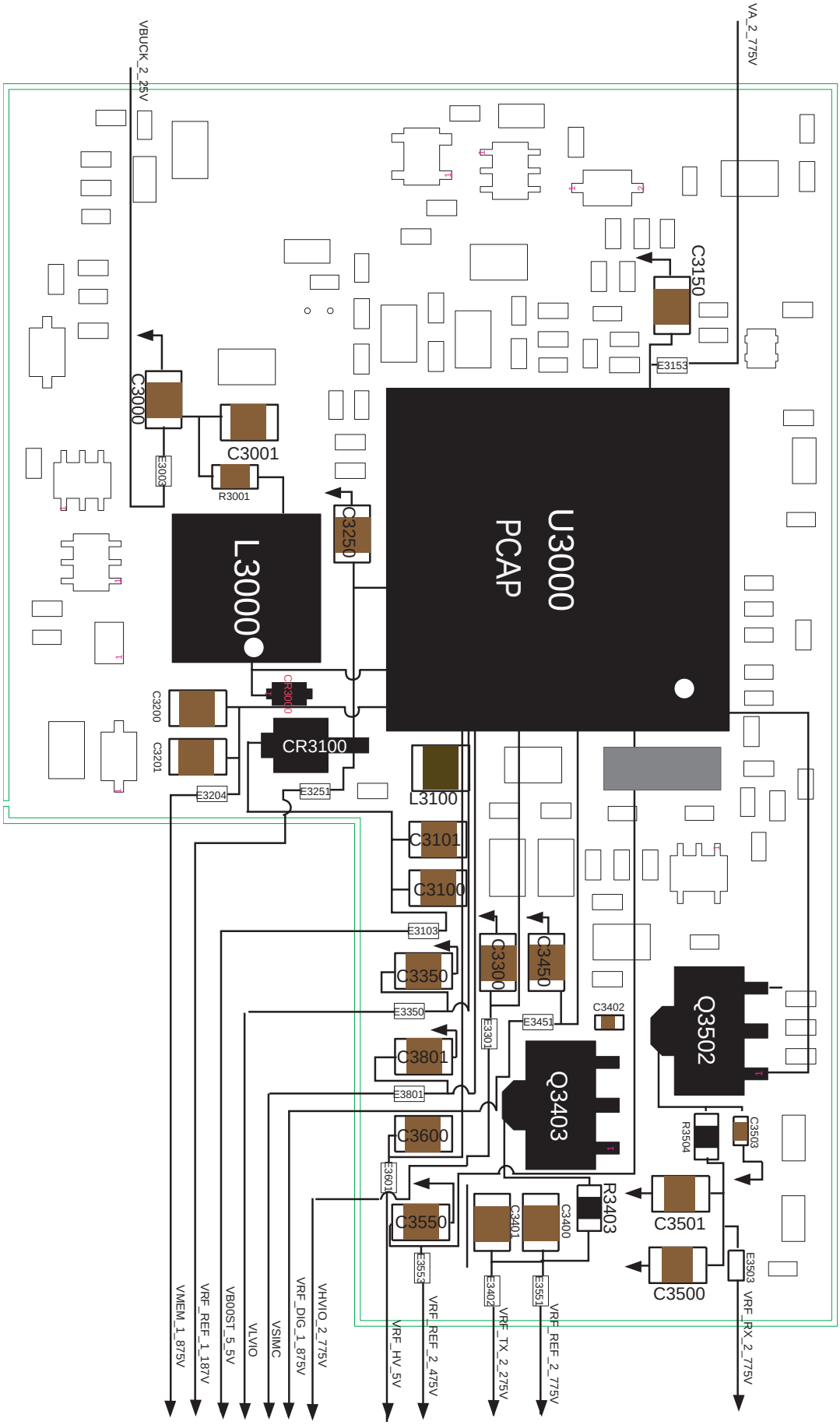
D1000: PCAP

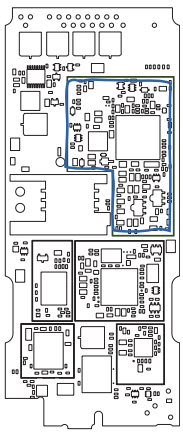


DESCRIPTION

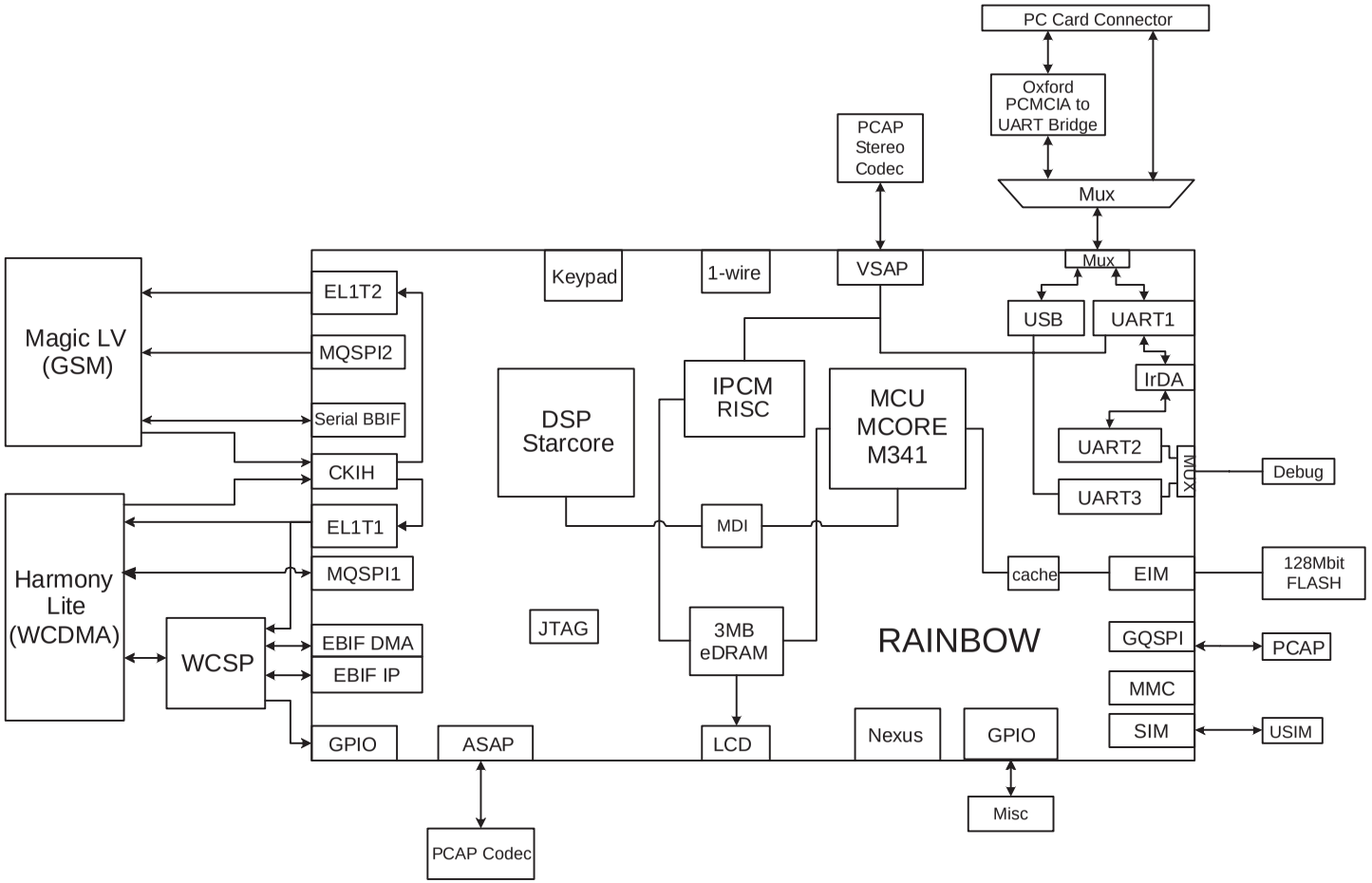
The Platform Control Audio Power IC (PCAP), U3000, is a mixed signal IC that contains the following features:

- Audio input/output amplification and filtering
- Audio path selection
- Voltage regulation
- Real time clock
- RS-232/USB drivers
- Status LED control
- Multiplexed DAC inputs for temperature and voltage monitoring
- Dual SPI control interface to allow access from two independent baseband processors
- Back-light control
- Ringer/vibrator control
- Stereo DAC
- Battery charging control
- Overvoltage protection
- The PCAP IC is controlled and configured by the Rainbow Baseband Processor IC through a four-wire SPI interface. The Baseband Processor has read/write access to the PCAP IC. Audio data is transmitted/received via the Baseband Processor through a four-wire SSI interface.


VBUCK_2_25V
VA_2_775V
C3150
E3153
C3000
C3001
R3001
E3003
L3000
C3250
U3000
PCAP
C3200
C3201
CR3100
E3204
E3251
L3100
C3101
C3100
E3103
C3350
E3350
C3300
C3450
E3301
E3451
C3402
Q3502
C3801
E3801
Q3403
C3600
E3601
C3550
R3504
C3503
C3501
C3500
R3403
C3401
C3400
E3553
E3402
E3551
E3503
VMEM_1_875V
VRF_REF_1_187V
VB0OST_5_5V
VLVIO
VSIMC
VRF_DIG_1_875V
VHVIO_2_775V
VRF_HV_5V
VRF_REF_2_475V
VRF_TX_2_275V
VRF_REF_2_775V
VRF_RX_2_775V



D1000: RAINBOW



The logic architecture is built around the Rainbow multi-core processor and the PCAP power management IC. The PCAP integrates several linear and switching voltage regulators, audio codecs and amplifiers, serial and USB transceivers, backlight and service-light LED controllers and digital interfaces to the Rainbow cores.

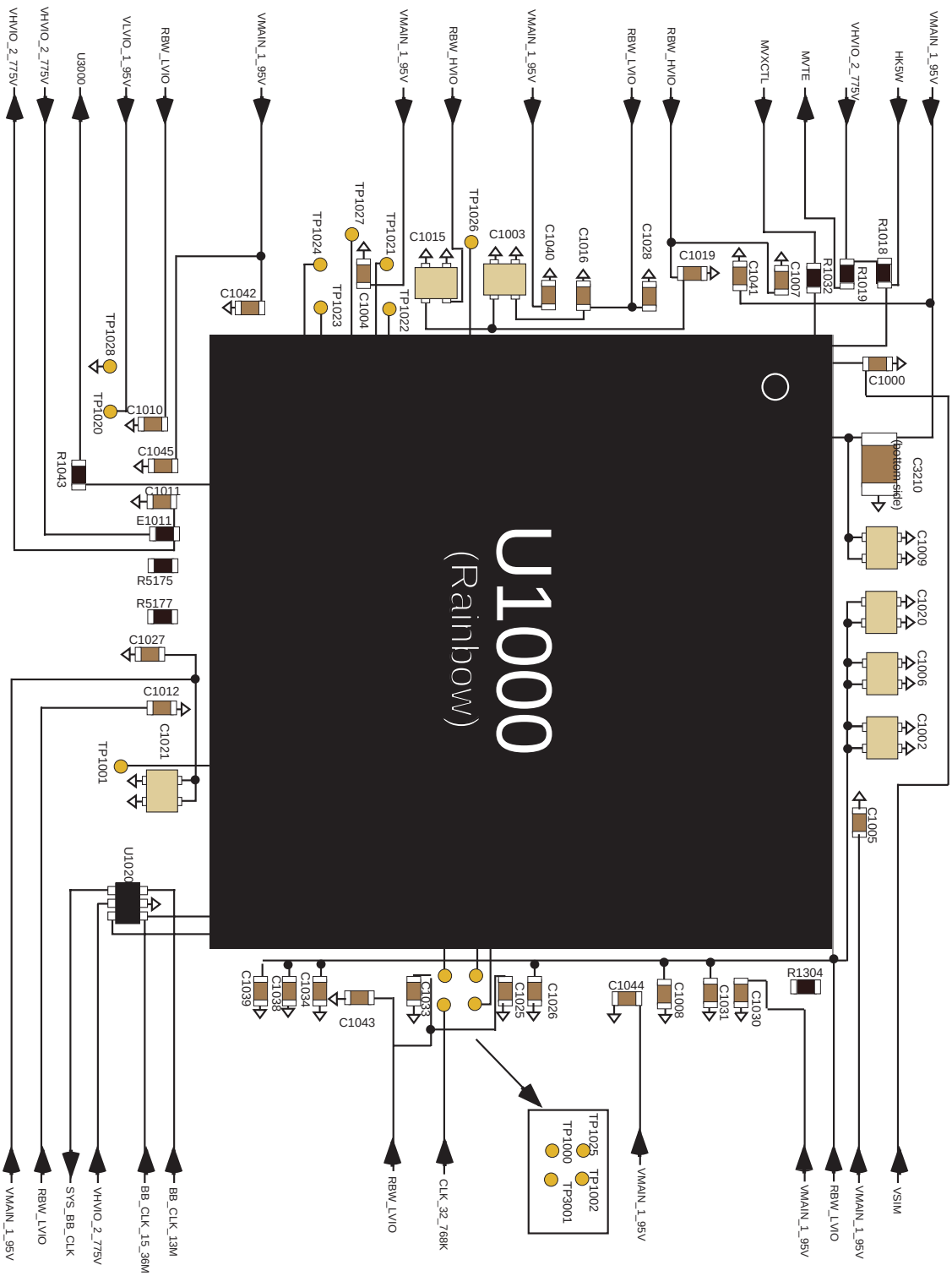
The Rainbow integrates a 32-bit RISC Communications Engine (MCU), a 32-bit DSP Core and an Interprocessor Communications Module (IPCM) along with associated peripherals and co-processors. The following provides a brief description of the cores and associated peripherals.

- MCU - Micro Controller
- DSP for GSM Signal processing
- EIM(external interface module) interfaces to FLASH and DRAM
- USB/Serial Communications
- GPIO - For A/Ds, LED, backlight, and vibrator control

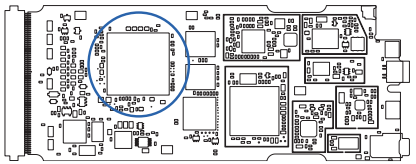
- IPCM which provides a multichannel DMA between the Mcore, DSP and peripherals.
- WCSP Interface
- GQSPI - PCAP Interface
- EBIF(External Bus Interface) DMA - WCDMA Data Transportation
- MQSPI1(Qued Serial Peripheral Interface) - WCDMA Control Signals
- EL1T1(Enhance Layer Timer) - WCDMA Event timer
- CLIH - WCDMA 15.36MHz clock
- 1 wire Communication for Battery EPROM
- Keypad Interface
- Display Interface
- USIM interface
- IrDA interface
- MMC interface
- ASAP interface for PCAP and Bluetooth audio interface
- VSAP interface for PCAP stereo Codec
- Serial BBIF(Baseband Interface) - GSM Data Transportation
- MQSPI2(Qued Serial Peripheral Interface) - GSM Control Signals
- EL1T2(Enhance Layer Timer) - GSM Event timer
- CLIH - GSM 13MHz clock "

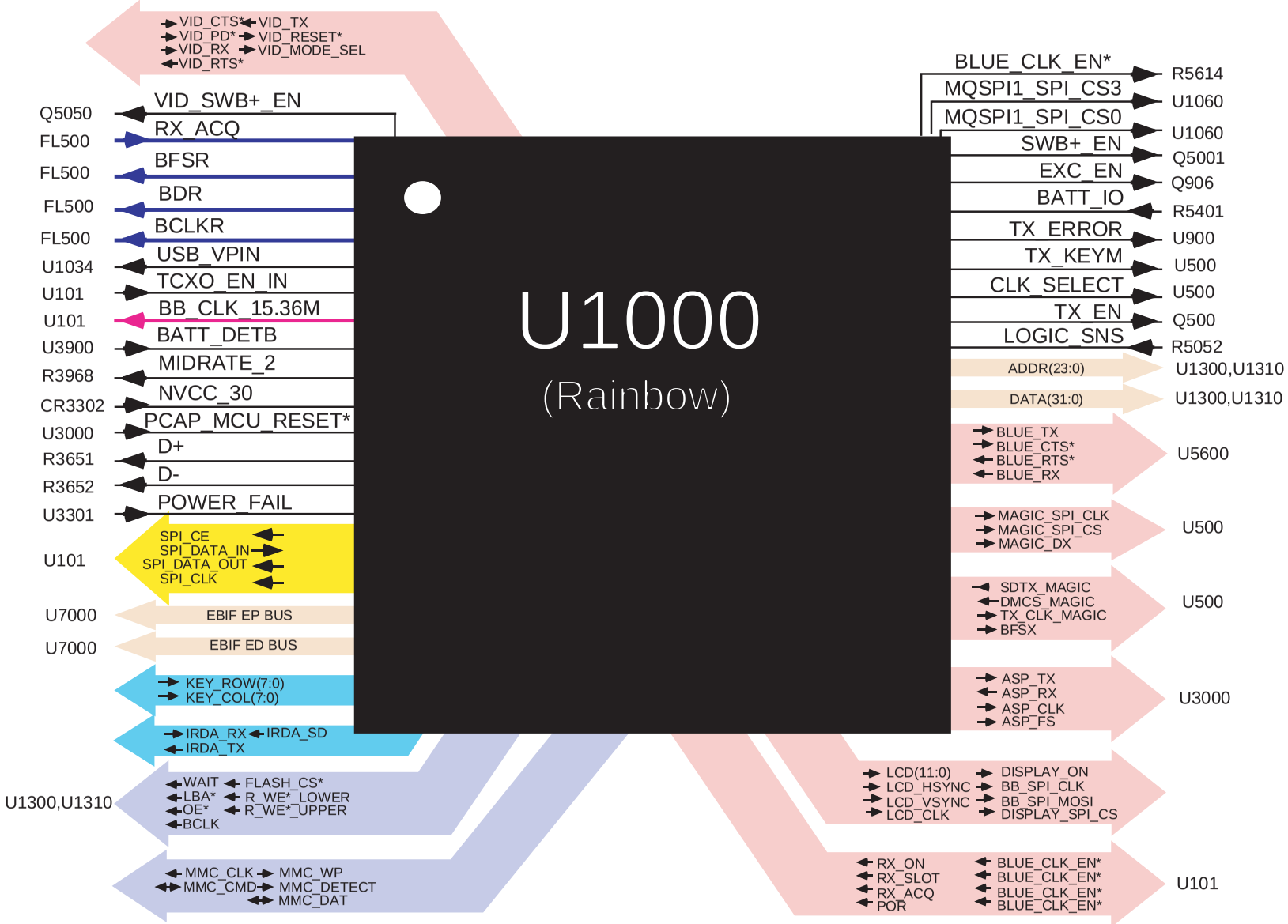
In addition to Rainbow's internal memory system, the architecture provides 128Mbits (16M byte) of external flash memory via two Intel Whitecliffe 64M bit parts. The memory bus is 23 address bits and 32 data bits. The flash memory runs at 50MHz.

D1000: RAINBOW

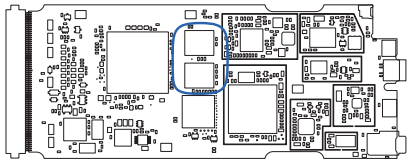


D1000: RAINBOW (continued)





D1000: Memory



R1305 FLASH_12V
V_FLASH1
C1303
C1309

E1303 V_FLASH1_IO

U1300
(Lower F lash)

VCCQ1 V_FLASH1_IO E1303
C1305
C1308
VCC1,VCC2 V_FLASH1 E1300
ADDR(23:0) U1000
DATA(15:0) U1000

U1000 LBA*
U1000 OE*
U1000 BCLK
U1000 R_WE*_LOWER

RESET
VCCQ2
E1303
E1300
C1300
TP3000
RESET

V_FLASH1_IO
VLVIO_1_95V E3350
V_FLASH1
VMEM_1_875V E3204
PCAP_RESET* U3000
MAGIC_13M R536
BB_CLK_13M U1020
V_FLASH2_IO E1301
V_FLASH2 E1302
ADDR(23:0) U1000
VLVIO_1_95V
WCSP_1_95V
DATA(31:16) U1000

U1310
(Upper F lash)

U1000 R_WE*_UPPER

VCCQ1,VCCQ2
VCC1
VCC2
E1012
C1302
C1306
E7000

E1302 V_FLASH2

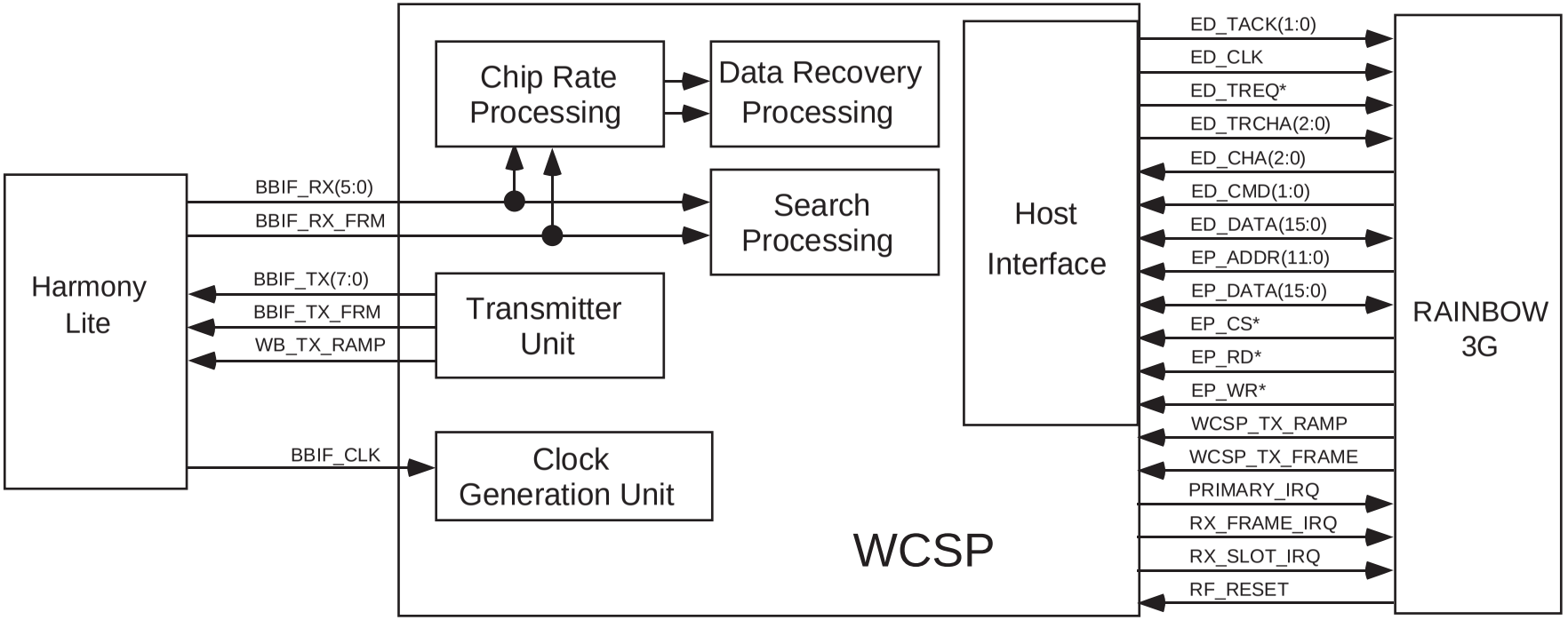
VPP
WP

E1301 V_FLASH2_IO
R1305 VFLASH_12V
V_FLASH2

E1302
C1304
C1307
C7004
C1310
E1301
R1305
C7003

V_FLASH2_IO
FLASH_12V
WCSP_1_95V
VLVIO_1_95V E3350
VMEM_1_875V E3204

D1000: WCSP



6802974C75-0

DESCRIPTION

The WCSP consists of five distinct functional units: the Transmitter Processing Unit, the Chip Rate Processing Unit, the Data Recovery Processing Unit, the Search Processing Unit, and the Host Interface Unit. Within Rainbow, the WCSP will interface to the DSP Peripheral and DMA buses using the existing EBIF interface. A Turbo Decoder Unit has also been developed for an FPGA implementation. When integrated within Rainbow, the Turbo Decoder engine will be implemented as a peripheral on the DSP Peripheral Bus. The Turbo memory, however, will be integrated within the DSP SRAM.

The Transmitter Unit implements the chip-rate processing functions of the reverse link defined in the 3GPP specifications.The framed data, which has been assembled within the DSP, is stored within an input buffer, spread by an OVSF channelizaton sequence, and spread in quadrature by the I and Q scrambling code PN sequences. The gating of the transmit power amplifier is controlled via the output pin PA_ENABLE.

The Chip Rate Processing Unit is responsible for the front-end reception of the forward link waveform defined in 3GPP specifications. The unit accepts 6-bit I and Q samples (RXI and RXQ) from the baseband interface at a rate of four times the chip rate of 3.84 MHz. The Chip Rate Processor then despreads and correlates the

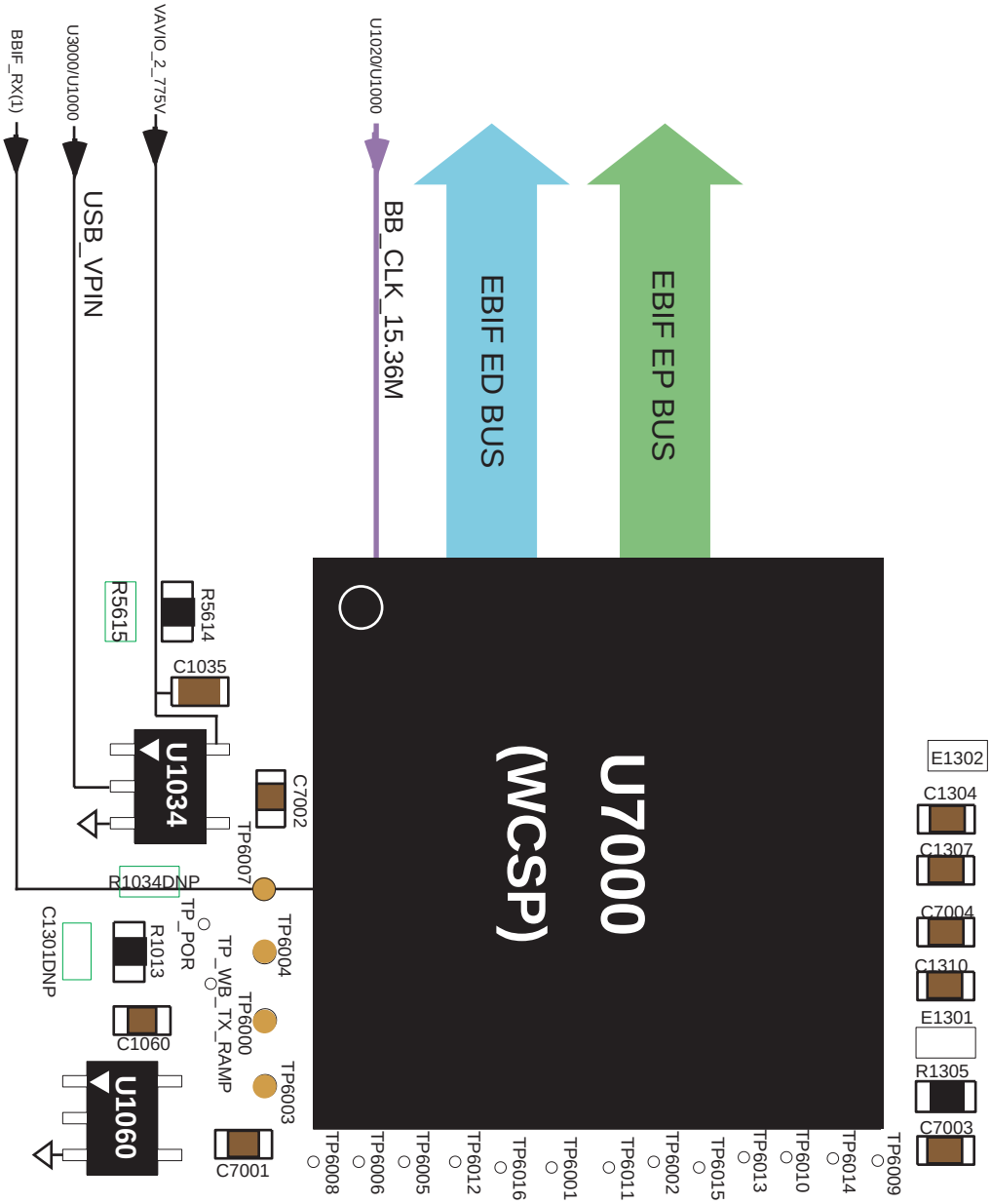
received signal (i.e., removes the scrambling and channelization PN codes) using eight independent rake branches.

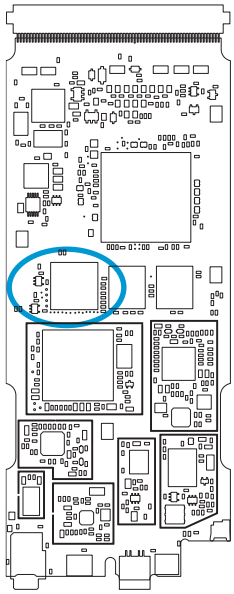
The Data Recovery Processing Unit performs coherent demodulation of the forward link signal. Within the unit, a channel estimate is generated for each rake receiver branch using FIR filtering methods. By multiplying this interally generated estimate by the correlated data, which is produced by the Chip Rate Processing Unit, coherently demodulated data can be generated. From the eight branhes, the data streams are then deskewed, combined, stored in an output buffer. The combined data symbols may be accessed by the DSP through one of the EBIF DMA channels.

The Search Processor Unit attempts to locate received signal paths having sufficient energy for demodulation. These high energy paths are detected when the receiver PN code sequences are time-aligned with the sequences applied at the base transmitter.

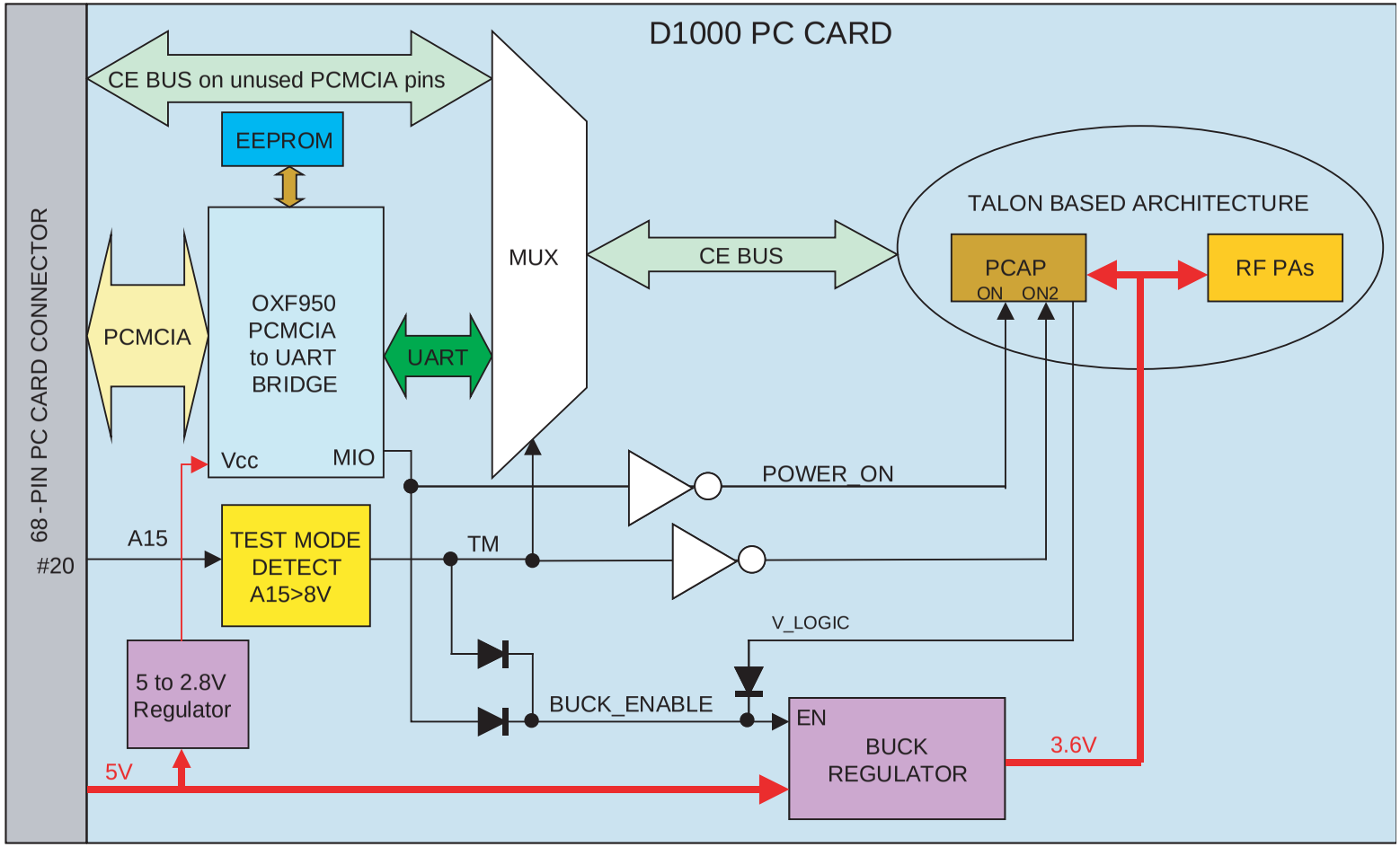
The Host Interface Unit provides the WCSP's interface to the EBIF peripheral and DMA buses. On the peripheral interface, this block converts the data, address, and control signals into the format required by the WCSP's internal registers.

D1000: WCSP


U7000
(WCSP)
EBIF EP BUS
EBIF ED BUS
BB_CLK_15.36M
U1020/U1000
VAVIO_2_775V
U3000/U1000
USB_VPIN
BBIF_RX(1)
U1034
U1060
R5614
R5615
C1035
C7002
TP6007
R1034DNP
TP_POR
R1013
C1301DNP
C1060
TP6004
TP6000
TP6003
TP_WB_TX_RAMP
C7001
E1302
C1304
C1307
C7004
C1310
E1301
R1305
C7003
TP6009
TP6014
TP6010
TP6013
TP6015
TP6002
TP6011
TP6001
TP6016
TP6012
TP6005
TP6006
TP6008



D1000: PC Card Intergface



DESCRIPTION

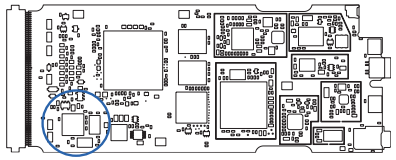
D1000 has two operating mode options: Normal Mode and Test Mode.

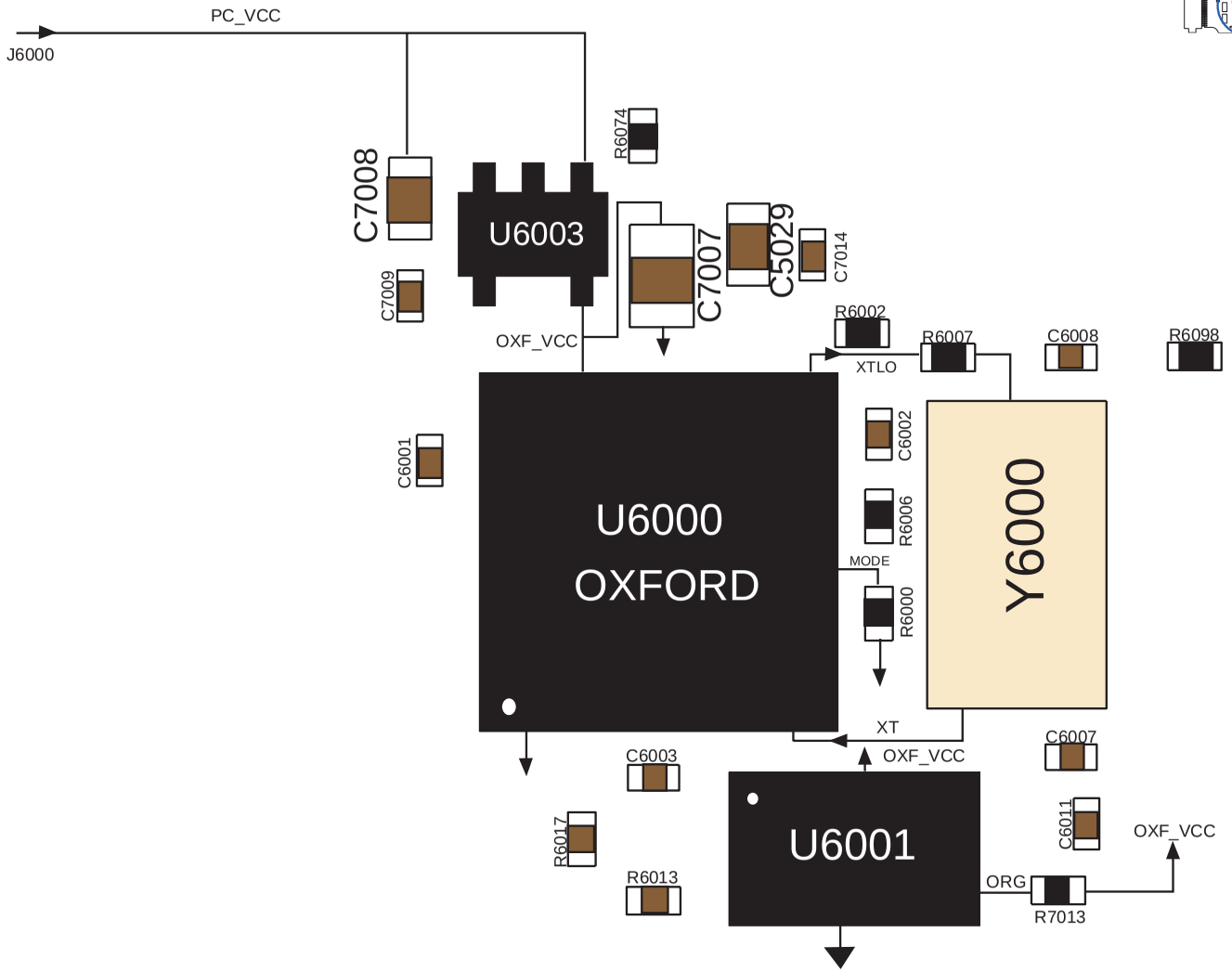
Normal Mode is the default mode when D1000 is inserted to PCMCIA slot of a host computer, and shall be the only mode that a customer uses, while Test Mode is used for maintenances using an "Extender board".

In Normal Mode D1000 main processor (Rainbow) communicate with the host computer via a "PC card <-> RS232 converter (OXFORD)<-> Rainbow", but the Rainbow can also support CE Bus, that is why for maintenance operation (such as flashing, flexing using an "Extender Board), Test Mode is used. In Test Mode the OXFORD is bypassed, and communication path is "Extender CE Bus" <-> Rainbow".

Communication path switching is done with 2X1 analog multiplexers, which are controlled with "Test Mode" signal. "Test Mode" is possible only if "12V" signal is injected to J6000 pin 20, then 12V is divided, and compared to 1.5V. The comparator output is the multiplexers control signal ("?5V" for in Test Mode or "0V" for Normal Mode). In Test Mode, Buck Regulator is also enabled, while in Normal Mode, Buck Regulator is enabled only when OXFORD turn on D1000.

D1000: PC Card Interface (Oxford)

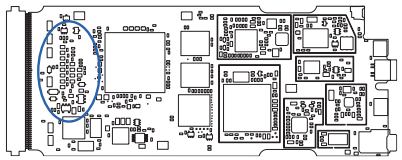


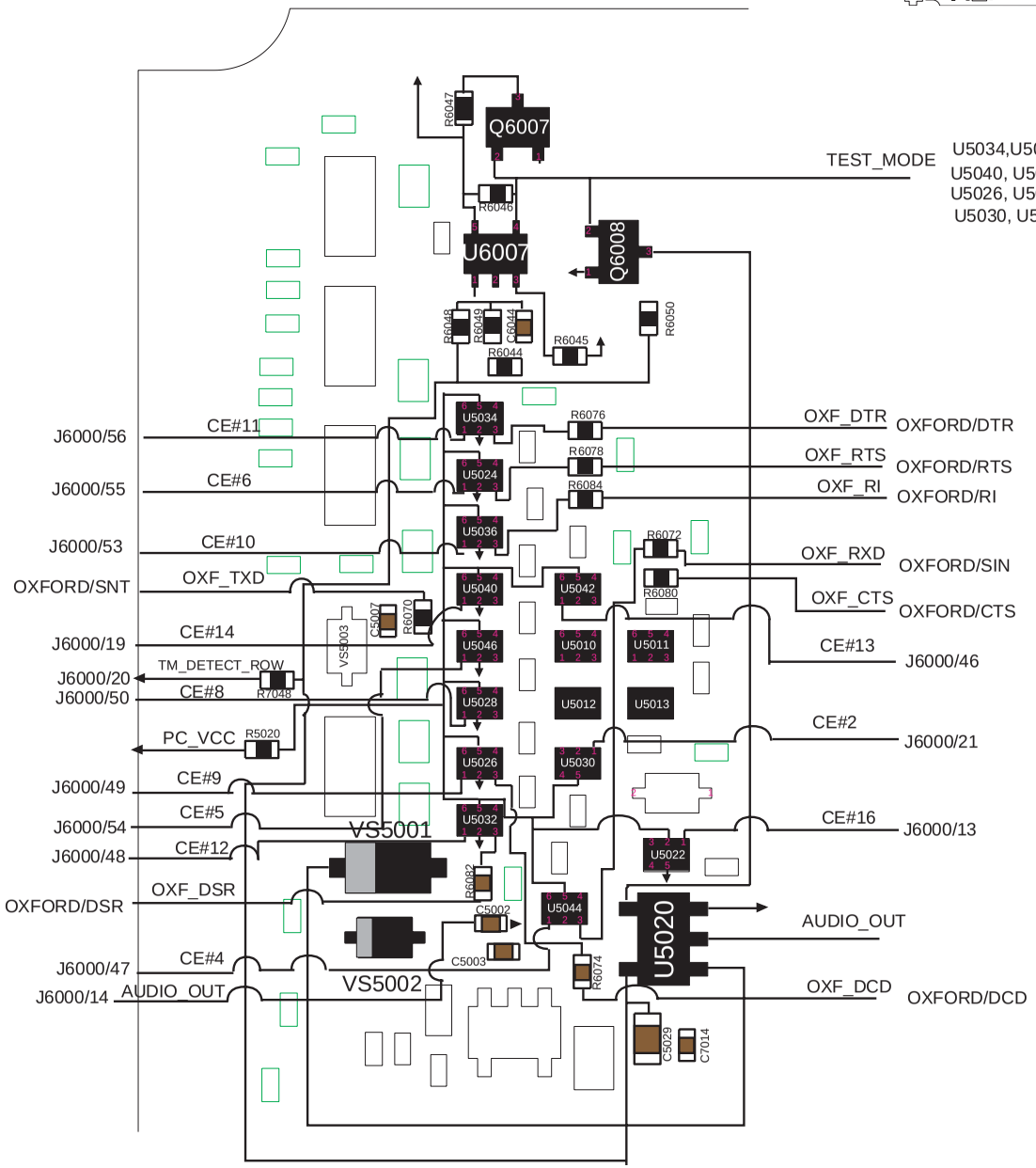


D1000: PC Card Interface (Connector Pinout)

68	-----	GND
34	-----	GND
67	-----	CD2#
33	-----	WP/IOIS16#
66	-----	NC
32	-----	PC_DATA2
65	-----	NC_
31	-----	PC_DATA1
64	-----	NC_
30	-----	PC_DATA0
63	-----	NC_
29	-----	PC_A0
62	-----	NC_
28	-----	PC_A1
61	-----	PC_CARD_REG#
27	-----	PC_A2
60	-----	NC_
26	-----	PC_A3
59	-----	NC_
25	-----	PC_A4
58	-----	OX_RESET
24	-----	PC_A5
57	-----	NC_
23	-----	PC_A6
56	-----	CE_BUS11
22	-----	PC_A7
55	-----	CE_BUS6
21	-----	CE_BUS2
54	-----	CE_BUS5
20	-----	TM_DETECT_RAW
53	-----	CE_BUS10
19	-----	CE_BUS14
52	-----	NC_
18	-----	NC
51	-----	PC_VCC
17	-----	PC_VCC
50	-----	CE_BUS8
16	-----	READY/IREQ#
49	-----	CE_BUS9
15	-----	WE#
48	-----	CE_BUS12
14	-----	CE_BUS15
47	-----	CE_BUS4
13	-----	CE_BUS16
46	-----	CE_BUS13
12	-----	NC_
45	-----	IOWR#
11	-----	NC
44	-----	IORD#
10	-----	NC
43	-----	VS1#
9	-----	OE#
42	-----	CE2#
8	-----	NC
41	-----	NC
7	-----	CE1#
40	-----	NC
6	-----	PC_DATA7
39	-----	NC_
5	-----	PC_DATA6
38	-----	NC_
4	-----	PC_DATA5
37	-----	NC_
3	-----	PC_DATA4
36	-----	CD1#
2	-----	PC_DATA3
35	-----	GND
1	-----	GND

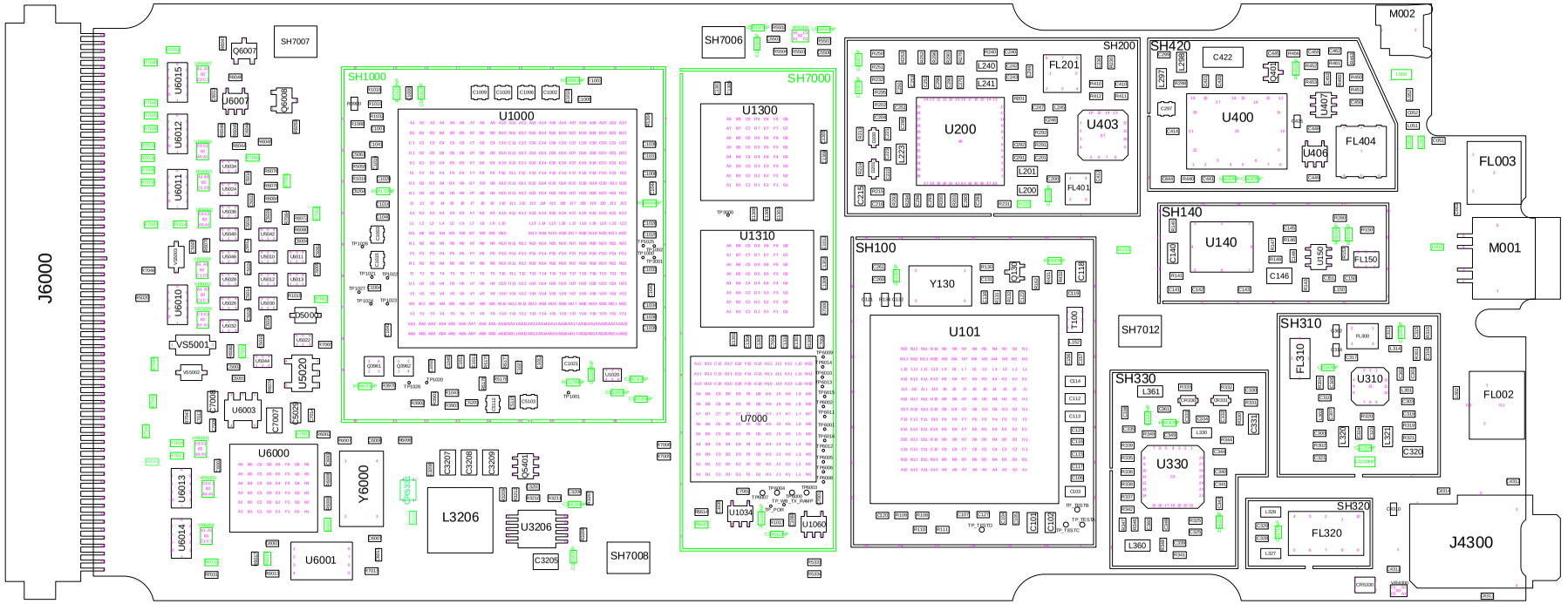
D1000: Normal / Test Mode Mux



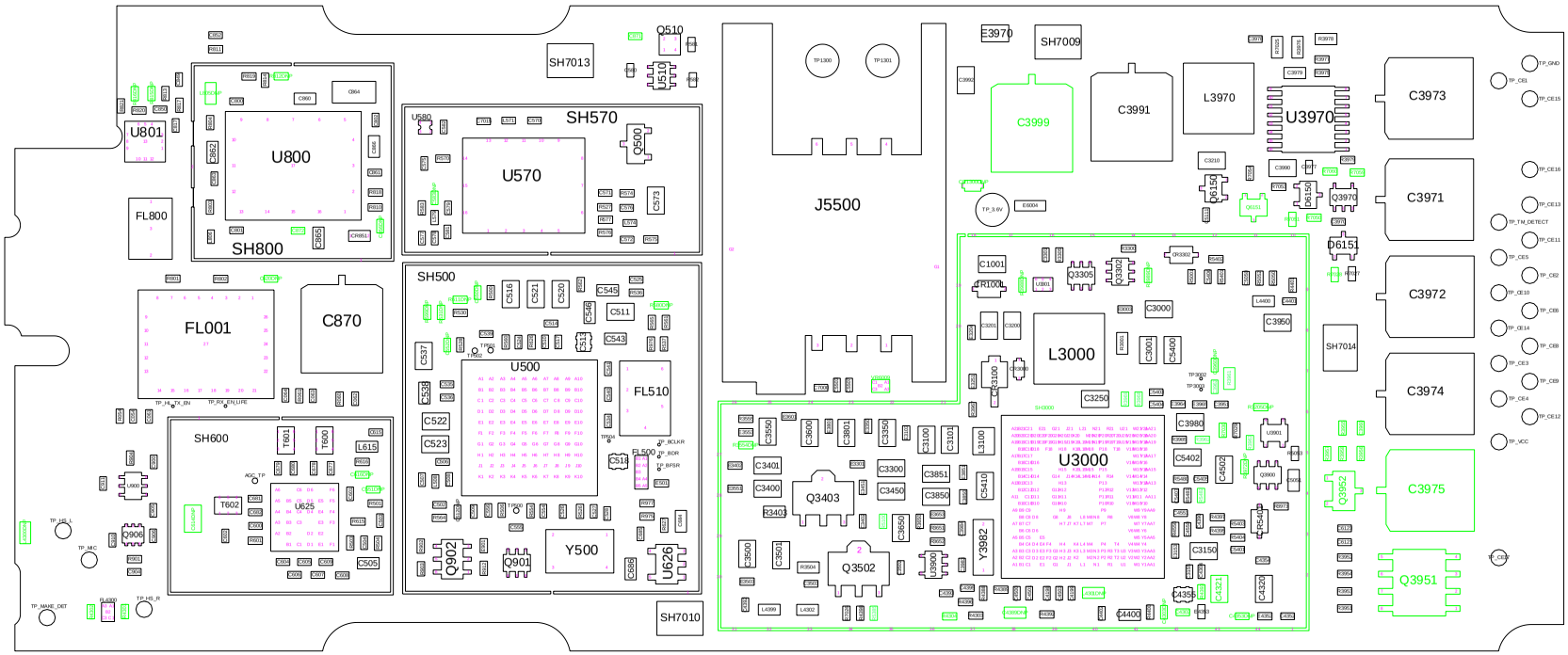


U5024/4	USB_PWR	PCAP
U5044/4	D+	PCAP
U5046/4	D-	PCAP
U5026/4	MUTE	RAINBOW
U5010/1	HKSW	RAINBOW
U5042/4	OPT2	RAINBOW
U5040/1	OPT1	RAINBOW
U5012/1	DSEL0	RAINBOW
U5034/4	DSEL1	RAINBOW
U5013/1	DSEL2	RAINBOW
U5022/4	AUDIO_IN	RAINBOW

D1000: Side 1 Layout



D1000: Side 2 Layout



ELECTRICAL PARTS LIST

The following tables list the electronic parts and accessories of the D1000 card.

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C003	2113743N09	CAP, 2pF
C051	0662057M01	RES, 0
C052	0662057M01	RES, 0
C054	2113743N50	CAP, 100pF
C061	2113743N34	CAP, 22pF
C062	2113743N26	CAP, 10pF
C063	2113743N26	CAP, 10pF
C064	2113743N26	CAP, 10pF
C101	2113928P04	CAP, 1uF
C102	2113928P04	CAP, 1uF
C103	2113928P04	CAP, 1uF
C104	2113743L17	CAP, 1nF
C105	2113743L17	CAP, 1nF
C106	2113928N01	CAP, 100nF
C107	2113928N01	CAP, 100nF
C112	2113928P04	CAP, 1uF
C113	2113928P04	CAP, 1uF
C114	2113928P04	CAP, 1uF
C115	2113743L17	CAP, 1nF
C116	2113928N01	CAP, 100nF
C117	2113928N01	CAP, 100nF
C118	2187906N01	CAP, 4.7uF
C119	2113928N01	CAP, 100nF
C120	2113928N01	CAP, 100nF
C121	2113928N01	CAP, 100nF
C122	2113928N01	CAP, 100nF
C123	2113928N01	CAP, 100nF
C127	2113928N01	CAP, 100nF
C130	2113928N01	CAP, 100nF
C131	2113743L41	CAP, 10nF
C132	2113743L41	CAP, 10nF
C140	2113743E07	CAP, 22nF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C141	2113743L25	CAP, 1200pF
C142	2113743N46	CAP, 68pF
C143	2113743L41	CAP, 10nF
C145	2113743N01	CAP, 0.5pF
C146	2113928C04	CAP, 4.7uF
C148	2113743N28	CAP, 12pF
C150	2113743N03	CAP, 1pF
C151	2113743N21	CAP, 6.2pF
C156	2113743N03	CAP, 1pF
C157	2113743N03	CAP, 1pF
C200	2113743N38	CAP, 33pF
C201	2113743N50	CAP, 100pF
C204	2113743L17	CAP, 1nF
C215	2113743E07	CAP, 22nF
C216	2113743L29	CAP, 3.3nF
C221	2113743N30	CAP, 15pF
C222	2113743N30	CAP, 15pF
C223	2104801Z08	CAP, 1.2pF
C230	2113743L17	CAP, 1nF
C240	2113743L17	CAP, 1nF
C242	2113743L17	CAP, 1nF
C243	2113743L17	CAP, 1nF
C246	2113743L05	CAP, 330pF
C247	2113743L05	CAP, 330pF
C250	2113743N26	CAP, 10pF
C251	2113743N26	CAP, 10pF
C252	2113743N26	CAP, 10pF
C253	2113743N26	CAP, 10pF
C260	2113743N28	CAP, 12pF
C261	2113743N16	CAP, 3.9pF
C270	2113743N50	CAP, 100pF
C280	2113743N50	CAP, 100pF
C281	2113743N22	CAP, 6.8pF
C290	2113743L17	CAP, 1nF
C291	2113743L17	CAP, 1nF
C292	2113743L17	CAP, 1nF
C293	2113743L17	CAP, 1nF
C294	2113743L17	CAP, 1nF
C295	2113743L17	CAP, 1nF
C296	2113743L17	CAP, 1nF
C297	2113947E01	CAP, 0.01uF
C299	2113743L41	CAP, 10nF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C300	2113743N26	CAP, 10pF
C301	2113743L41	CAP, 10nF
C303	2113743L09	CAP, 470pF
C305	2113743N26	CAP, 10pF
C307	2113743N50	CAP, 100pF
C310	2113743N26	CAP, 10pF
C313	2113743N02	CAP, 0.75pF
C314	2113743N26	CAP, 10pF
C315	2113743L41	CAP, 10nF
C316	2113743N26	CAP, 10pF
C317	2113743L37	CAP, 6.8nF
C319	2113743L41	CAP, 10nF
C320	2113743K16	CAP, 220nF
C321	2113743M24	CAP, 100nF
C323	2113743N26	CAP, 10pF
C324	2113743N26	CAP, 10pF
C325	2113743N24	CAP, 8.2pF
C328	2113743L41	CAP, 10nF
C329	2113743L41	CAP, 10nF
C330	2113743L29	CAP, 3.3nF
C331	2113743E07	CAP, 22nF
C332	2113743N28	CAP, 12pF
C333	2113743N28	CAP, 12pF
C334	2113743N18	CAP, 4.7pF
C335	2113743N16	CAP, 3.9pF
C338	2113743N24	CAP, 8.2pF
C339	2113743L05	CAP, 330pF
C340	2113743L17	CAP, 1nF
C341	2113743L17	CAP, 1nF
C343	2113743N50	CAP, 100pF
C344	2113743L05	CAP, 330pF
C348	2113743L41	CAP, 10nF
C349	2113743L41	CAP, 10nF
C360	2113743L41	CAP, 10nF
C361	2113743L41	CAP, 10nF
C362	2113743N26	CAP, 10pF
C410	2113743L01	CAP, 220pF
C413	2113743N28	CAP, 12pF
C414	2113743N28	CAP, 12pF
C420	2113743N30	CAP, 15pF
C421	2113743L41	CAP, 10nF
C422	2113743G26	CAP, 4.7uF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C425	2113743N28	CAP, 12pF
C441	2113743L41	CAP, 10nF
C444	2113743L41	CAP, 10nF
C445	2113743N50	CAP, 100pF
C448	2113743N26	CAP, 10pF
C449	2113743L41	CAP, 10nF
C450	2113743N30	CAP, 15pF
C452	2113743N30	CAP, 15pF
C455	2113743L17	CAP, 1nF
C462	2113743N30	CAP, 15pF
C502	2113743M24	CAP, 100nF
C503	2113743L01	CAP, 220pF
C504	2113743L13	CAP, 680pF
C505	2113741F45	CAP, 6.8nF
C506	2113743L41	CAP, 10nF
C507	2113743N50	CAP, 100pF
C508	2113743N03	CAP, 1pF
C509	2113743N50	CAP, 100pF
C510	2113743M24	CAP, 100nF
C511	2113928C03	CAP, 1uF
C513	2113947E01	CAP, 0.01uF
C514	2113743L41	CAP, 10nF
C516	2113928C03	CAP, 1uF
C517	2113743L17	CAP, 1nF
C518	2113947E01	CAP, 0.01uF
C520	2113928C04	CAP, 4.7uF
C521	2113928C04	CAP, 4.7uF
C522	2113928C04	CAP, 4.7uF
C523	2113928C04	CAP, 4.7uF
C524	2113743N34	CAP, 22pF
C525	2113743N28	CAP, 12pF
C526	2113743N32	CAP, 18pF
C527	2113743N32	CAP, 18pF
C528	2113743N40	CAP, 39pF
C534	2113743N34	CAP, 22pF
C535	2113743L17	CAP, 1nF
C536	2113743L41	CAP, 10nF
C537	2113928C04	CAP, 4.7uF
C538	2113928A01	CAP, 1uF
C539	2113743L41	CAP, 10nF
C540	2113743L41	CAP, 10nF
C541	2113743L41	CAP, 10nF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C543	2113928P04	CAP, 1uF
C545	2113928P04	CAP, 1uF
C546	2113928P04	CAP, 1uF
C554	2113743L01	CAP, 220pF
C555	2113743L07	CAP, 390pF
C556	2113743L05	CAP, 330pF
C570	2113743M24	CAP, 100nF
C571	2113743L03	CAP, 270pF
C572	2113743L19	CAP, 1.2nF
C573	0888600M19	CAP, 3.3nF
C575	2113743N14	CAP, 3.3pF
C576	2113743L05	CAP, 330pF
C577	2113743N28	CAP, 12pF
C578	2113743N28	CAP, 12pF
C579	2113743N03	CAP, 1pF
C580	2113743M24	CAP, 100nF
C581	2113743N28	CAP, 12pF
C582	2113743N12	CAP, 2.7pF
C600	2113743N34	CAP, 22pF
C601	2113743N02	CAP, 0.75pF
C602	2113743L41	CAP, 10nF
C604	2113743L05	CAP, 330pF
C605	2113743L05	CAP, 330pF
C606	2113743N54	CAP, 150pF
C607	2113743L05	CAP, 330pF
C608	2113743L05	CAP, 330pF
C609	2113743N54	CAP, 150pF
C614DNP	2113928C04	CAP, 4.7uF
C615	2113743N36	CAP, 27pF
C677	2113743N36	CAP, 27pF
C678	2113743N36	CAP, 27pF
C679	2113743N36	CAP, 27pF
C680	2113743N36	CAP, 27pF
C681	2113743N36	CAP, 27pF
C682	2113743N36	CAP, 27pF
C684	2113928A01	CAP, 1uF
C685	2113743L41	CAP, 10nF
C686	2113928A01	CAP, 1uF
C800	2113743N36	CAP, 27pF
C801	2113743N28	CAP, 12pF
C802	2113743N37	CAP, 30pF
C817	2113743N13	CAP, 3pF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C849	2113743N28	CAP, 12pF
C850	2113743N28	CAP, 12pF
C852	2113743N38	CAP, 33pF
C860	2113743E20	CAP, 100nF
C861	2113743N26	CAP, 10pF
C862	2113743E20	CAP, 100nF
C863	2113743N26	CAP, 10pF
C864	2113743G26	CAP, 4.7uF
C865	2113743E20	CAP, 100nF
C866	2113743E20	CAP, 100nF
C870	2388094U03	CAP, 330uF
C900	2113743N28	CAP, 12pF
C904	2113743N28	CAP, 12pF
C905	2113743N28	CAP, 12pF
C906	2113743N28	CAP, 12pF
C910	2113743N28	CAP, 12pF
C911	2113743N28	CAP, 12pF
C1000	2113743M24	CAP, 100nF
C1001	2113928C13	CAP, 10uF
C1002	2113947B05	CAP, 33pF
C1003	2113947H01	CAP, 100nF
C1004	2113743M24	CAP, 100nF
C1005	2113743M24	CAP, 100nF
C1006	2113947H01	CAP, 100nF
C1007	2113743M24	CAP, 100nF
C1008	2113743M24	CAP, 100nF
C1009	2113947H01	CAP, 100nF
C1010	2113743M24	CAP, 100nF
C1011	2113743M24	CAP, 100nF
C1012	2113743M24	CAP, 100nF
C1015	2113947H01	CAP, 100nF
C1016	2113743M24	CAP, 100nF
C1019	2113743M24	CAP, 100nF
C1020	2113947H01	CAP, 100nF
C1021	2113947H01	CAP, 100nF
C1025	2113743M24	CAP, 100nF
C1026	2113743M24	CAP, 100nF
C1027	2113743M24	CAP, 100nF
C1028	2113743M24	CAP, 100nF
C1030	2113743M24	CAP, 100nF
C1031	2113743M24	CAP, 100nF
C1033	2113743M24	CAP, 100nF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C1034	2113743M24	CAP, 100nF
C1035	2113743M24	CAP, 100nF
C1038	2113743M24	CAP, 100nF
C1039	2113743M24	CAP, 100nF
C1040	2113743M24	CAP, 100nF
C1041	2113743M24	CAP, 100nF
C1042	2113743M24	CAP, 100nF
C1053	2113743M24	CAP, 100nF
C1044	2113743M24	CAP, 100nF
C1045	2113743M24	CAP, 100nF
C1060	2113743M24	CAP, 100nF
C1300	2113743M24	CAP, 100nF
C1302	2113743M24	CAP, 100nF
C1303	2113743M24	CAP, 100nF
C1304	2113743M24	CAP, 100nF
C1305	2113743M24	CAP, 100nF
C1306	2113743M24	CAP, 100nF
C1307	2113743M24	CAP, 100nF
C1308	2113743M24	CAP, 100nF
C1309	2113743M24	CAP, 100nF
C1310	2113743M24	CAP, 100nF
C3000	2113928C13	CAP, 10uF
C3001	2113928C13	CAP, 10uF
C3100	2113928C13	CAP, 10uF
C3101	2113928C13	CAP, 10uF
C3150	2113928C04	CAP, 4.7uF
C3155	2113743N38	CAP, 33pF
C3200	2113928C13	CAP, 10uF
C3201	2113928C13	CAP, 10uF
C3203	2113743N35	CAP, 24pF
C3205	2113928C13	CAP, 10uF
C3206	2113743L17	CAP, 1nF
C3207	2113928C13	CAP, 10uF
C3208	2113928C13	CAP, 10uF
C3209	2113928C13	CAP, 10uF
C32010	2113928C13	CAP, 10uF
C3250	2113928C04	CAP, 4.7uF
C3300	2113928C04	CAP, 4.7uF
C3301	2113743M24	CAP, 100nF
C3350	2113928C13	CAP, 10uF
C3400	2113928C13	CAP, 10uF
C3401	2113928C13	CAP, 10uF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C3402	2113743M24	CAP, 100nF
C3450	2113928C04	CAP, 4.7uF
C3500	2113928C13	CAP, 10uF
C3501	2113928C13	CAP, 10uF
C3502	2113743M24	CAP, 100nF
C3503	2113743N36	CAP, 27pF
C3550	2113928C04	CAP, 4.7uF
C3600	2113928C04	CAP, 4.7uF
C3650	2113928C04	CAP, 4.7uF
C3801	2113928C04	CAP, 4.7uF
C3850	2113928C04	CAP, 4.7uF
C3851	2113928C04	CAP, 4.7uF
C3950	2113928C04	CAP, 4.7uF
C3951	2113743M24	CAP, 100nF
C3970	2113743L13	CAP, 680pF
C3971	2388094U03	CAP, 330uF
C3972	2388094U03	CAP, 330uF
C3973	2388094U03	CAP, 330uF
C3974	2388094U03	CAP, 330uF
C3977	2113743L09	CAP, 470pF
C3978	2113743N42	CAP, 47pF
C3979	2113928P04	CAP, 1uF
C3980	2113928C03	CAP, 1uF
C3983	2113743N30	CAP, 15pF
C3984	2113743N30	CAP, 15pF
C3990	2113928C04	CAP, 4.7uF
C3991	2388094U03	CAP, 330uF
C3992	2113928C13	CAP, 10uF
C4198	2113743M24	CAP, 100nF
C4199	2113743M24	CAP, 100nF
C4304	2113743L41	CAP, 10nF
C4310	2113743N38	CAP, 33pF
C4311	2113743N38	CAP, 33pF
C4312	2113743N38	CAP, 33pF
C4313	2113743N38	CAP, 33pF
C4314	2113743N38	CAP, 33pF
C4320	2113928C13	CAP, 10uF
C4352	2113743N38	CAP, 33pF
C4354	2113743L41	CAP, 10nF
C4355	2113947B05	CAP, 33pF
C4390	2113743M24	CAP, 100nF
C4392	2113743N40	CAP, 39pF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C4393	2113743N40	CAP, 39pF
C4395	2113743M24	CAP, 100nF
C4400	2113928A01	CAP, 1uF
C4401	2113743M24	CAP, 100nF
C4402	2113743N26	CAP, 10pF
C4500	2113743M24	CAP, 100nF
C4501	2113743N38	CAP, 33pF
C4502	2113928C04	CAP, 4.7uF
C4503	2113743M24	CAP, 100nF
C4550	2113743L25	CAP, 1200pF
C4551	2113743L41	CAP, 10nF
C5002	2113743N38	CAP, 33pF
C5003	2113743N38	CAP, 33pF
C5004	2113743M24	CAP, 100nF
C5005	2113743M24	CAP, 100nF
C5007	2113743N34	CAP, 22pF
C5010	2113743N38	CAP, 33pF
C5012	2113743N38	CAP, 33pF
C5014	2113743N38	CAP, 33pF
C5016	2113743N38	CAP, 33pF
C5018	2113743N38	CAP, 33pF
C5020	2113743N38	CAP, 33pF
C5022	2113743N38	CAP, 33pF
C5024	2113743N38	CAP, 33pF
C5026	2113743N38	CAP, 33pF
C5028	2113743N38	CAP, 33pF
C5029	2113743E20	CAP, 100nF
C5050	2113743M24	CAP, 100nF
C5051	2113928A01	CAP, 1uF
C5061	2113743N36	CAP, 27pF
C5062	2113743L17	CAP, 1nF
C5103	2113947B05	CAP, 33pF
C5111	2113743N38	CAP, 33pF
C5112	2113947B05	CAP, 33pF
C5115	2113743N38	CAP, 33pF
C5203	2113743N38	CAP, 33pF
C5204	2113743N38	CAP, 33pF
C5400	2113928C13	CAP, 10uF
C5401	2113743L41	CAP, 10nF
C5402	2113928C13	CAP, 10uF
C5403	2113743M24	CAP, 100nF
C5404	2113743N34	CAP, 22pF

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
C5405	2113743N34	CAP, 22pF
C5406	2113743N34	CAP, 22pF
C5407	2113743L41	CAP, 10nF
C5410	2113928C13	CAP, 10uF
C5501	2113743N34	CAP, 22pF
C5503	2113743M24	CAP, 100nF
C5506	2113743N34	CAP, 22pF
C5507	2113743N34	CAP, 22pF
C6001	2113743M24	CAP, 100nF
C6002	2113743M24	CAP, 100nF
C6003	2113743M24	CAP, 100nF
C6007	2113743N34	CAP, 22pF
C6008	2113743N34	CAP, 22pF
C6011	2113743M24	CAP, 100nF
C6013	2113743M24	CAP, 100nF
C6044	2113743M24	CAP, 100nF
C6121	2113743N38	CAP, 33pF
C6123	2113743M24	CAP, 100nF
C7000	2113743M24	CAP, 100nF
C7001	2113743M24	CAP, 100nF
C7002	2113743M24	CAP, 100nF
C7003	2113743M24	CAP, 100nF
C7004	2113743M24	CAP, 100nF
C7007	2113928C04	CAP, 4.7uF
C7008	2113928A01	CAP, 1uF
C7009	2113743L41	CAP, 10nF
C7013	2113743N34	CAP, 22pF
C7014	2113743N34	CAP, 22pF
C7015	2113743N28	CAP, 12pF
C512DNP	2113743N16	CAP, 3.9pF
CR330	4809877C32	SMV1763 Varactor Diode
CR331	4809877C32	SMV1763 Varactor Diode
CR851	4809496B11	QSMG-H799 led
CR1001	4809948D42	RB751V40 Schottky diode
CR3000	4809924D18	RB520S-30 Schottky diode
CR3100	4809653F02	MBRM120T3 Schottky Rectifier
CR3302	4809948D42	RB751V40 Schottky diode
CR5330	4809118D02	LNJ115 Two color led
CR5401	4809948D42	RB751V40 Schottky diode
D200	4809877C32	SMV1763 Varactor Diode
D201	4809877C32	SMV1763 Varactor Diode
D5000	4809948D42	RB751V40 Schottky diode

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
D6150	4809606E08	RB715F Two Schottky diode
D6151	4809606E08	RB715F Two Schottky diode
E3208	0662057M01	RES, 0
E3970	2480675U01	IDCTR, Ferrite Bead
FL001	4889695L12	ASM3201B Filter
FL002	9109674L20	9109674L20 Filter
FL003	9109674L18	S0350 Filter
FL150	5885949K03	LDD15A Filter
FL201	9109405J17	SAFCD380 Filter
FL300	9109239M28	SAF2G14KB0 Filter
FL310	9109674L14	LFSG20N25 Filter
FL320	9109405J16	FLTR Filter
FL401	9109239M16	SAF1G95KB0 Filter
FL404	5888234M01	34M01 Filter
FL500	9188695K04	95K04 Filter
FL510	4889767N01	4889767nF01 Filter
FL800	9109674L17	74L17 Filter
FL4300	4889526L04	FLTR Filter
J4300	0985885K01	Audio connector
J5500	0986632U05	USIM connector
J6000	0988247V01	PCMCIA connector
L002	2409154M09	IDCTR, 4.7nH
L051	0662057M01	RES, 0
L052	2409154M07	IDCTR, 3.3nH
L150	2409154M07	IDCTR, 3.3nH
L152	2409154M06	IDCTR, 2.7nH
L200	2409646M16	IDCTR, 2.2nH
L201	2485793G04	IDCTR, 10nH
L223	2485793G04	IDCTR, 10nH
L240	2409377M16	IDCTR, 82nH
L241	2409377M16	IDCTR, 82nH
L244	2488289M25	IDCTR, 100nH
L245	2488289M26	IDCTR, 125nH
L297	2409377M16	IDCTR, 82nH
L298	2409377M16	IDCTR, 82nH
L301	2409154M07	IDCTR, 3.3nH
L302	2409154M07	IDCTR, 3.3nH
L314	2409154M04	IDCTR, 1.8nH
L320	2485793G14	IDCTR, 68nH
L321	2485793G14	IDCTR, 68nH
L327	2485793G15	IDCTR, 82nH
L328	2485793G15	IDCTR, 82nH

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
L330	2409377M08	IDCTR, 22nH
L360	2462587Q39	IDCTR, 220nH
L361	2462587Q39	IDCTR, 220nH
L508	2409154M10	IDCTR, 5.6nH
L571	2409154M66	IDCTR, 18nH
L574	2409154M43	IDCTR, 39nH
L579	0662057M01	RES, 0
L615	2409377M03	IDCTR, 6.8nH
L806	2409154M12	IDCTR, 8.2nH
L3000	2588866L14	IDCTR, 47uH
L3100	2487659M11	IDCTR, 47uH
L3206	2488214V01	IDCTR, 2.2uH
L3970	2588866L05	IDCTR, 2.2uH
L4302	2409646M13	IDCTR, 39nH
L4399	2409646M13	IDCTR, 39nH
L4400	2409646M13	IDCTR, 39nH
M001	0986428Z01	Ext Antenna connector
M002	3987997U05	Int Antenna contact
Q130	4809579E24	2SJ347
Q401	4809608E03	DTA114YE
Q500	4809579E16	TN0200T
Q510	4862830F01	SI8401DB
Q901	4809579E58	FDG6332C
Q902	4809579E48	FDC6306P
Q906	4809939C34	EMB10
Q3302	4809579E58	FDG6332C
Q3305	4809579E58	FDG6332C
Q3403	4809607E04	2SB1132
Q3502	4809607E04	2SB1132
Q3900	4809579E58	FDG6332C
Q3961	4862830F01	SI8401DB
Q3962	4862830F01	SI8401DB
Q3970	4809939C05	UMC5nFTL
Q5401	4809579E43	FDG6303nF
Q6007	4802393L55	2SK3018T106
Q6008	4802393L55	2SK3018T106
Q6150	4802393L55	2SK3018T106
R060	0662057M01	RES, 0
R061	0662057M01	RES, 0
R130	0662057M74	RES, 1K
R131	0662057N09	RES, 27K
R132	0662057N09	RES, 27K

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
R134	0662057M01	RES, 0
R140	0662057M70	RES, 680
R141	0662057M94	RES, 6.8K
R146	0662057U44	RES, 51 1%
R147	0662057M52	RES, 120
R148	0662057M52	RES, 120
R150	0662057M50	RES, 100
R153	0662057M01	RES, 0
R200	0662057N15	RES, 47K
R201	0662057M98	RES, 10K
R202	0662057U44	RES, 51 1%
R213	0662057M98	RES, 10K
R214	0662057M98	RES, 10K
R215	0662057V02	RES, 10K 1%
R230	0662057N15	RES, 47K
R231	0662057M01	RES, 0
R240	0662057M26	RES, 10
R250	0662057M78	RES, 1.5K
R251	0662057M78	RES, 1.5K
R252	0662057M78	RES, 1.5K
R253	0662057M78	RES, 1.5K
R251	0662057M78	RES, 1.5K
R252	0662057M78	RES, 1.5K
R253	0662057M78	RES, 1.5K
R270	0662057M50	RES, 100
R280	0662057M01	RES, 0
R290	0662057M01	RES, 0
R291	0662057M01	RES, 0
R292	0662057M01	RES, 0
R293	0662057M01	RES, 0
R294	0662057M01	RES, 0
R295	0662057M01	RES, 0
R296	0662057M01	RES, 0
R301	0662057N05	RES, 18K
R315	0662057M26	RES, 10
R319	0662057M26	RES, 10
R320	0662057M98	RES, 10K
R321	0662057M26	RES, 10
R325	0662057M70	RES, 680
R331	0662057M98	RES, 10K
R332	0662057M98	RES, 10K
R333	0662057M98	RES, 10K

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
R341	0662057M50	RES, 100
R344	0662057M74	RES, 1K
R346	0662057N15	RES, 47K
R348	0662057M26	RES, 10
R349	0662057M26	RES, 10
R410	0662057M90	RES, 4.7K
R411	0662057M70	RES, 680
R412	0662057M70	RES, 680
R431	0662057M01	RES, 0
R432	0662057M01	RES, 0
R440	0662057M01	RES, 0
R450	0662057M95	RES, 7.5K
R451	0662057M90	RES, 4.7K
R452	0662057N20	RES, 75K
R453	0662057M98	RES, 10K
R456	0662057M01	RES, 0
R460	0662057M90	RES, 4.7K
R461	0662057N11	RES, 33K
R463	0662057M01	RES, 0
R500	0662057M01	RES, 0
R501	0662057M01	RES, 0
R503	0662057M83	RES, 2.4K
R504	0662057M74	RES, 1K
R506	0662057N21	RES, 82K
R526	0662057N03	RES, 15K
R527	0662057M01	RES, 0
R528	0662057M01	RES, 0
R530	0662057M01	RES, 0
R537	0662057N01	RES, 12K
R554	0662057N07	RES, 22K
R570	0662057M01	RES, 0
R574	0662057M56	RES, 180
R575	0662057M72	RES, 820
R576	0662057N11	RES, 33K
R577	0662057M96	RES, 8.2K
R581	0662057N21	RES, 82K
R582	0662057M01	RES, 0
R583	0662057M19	RES, 5.1
R616	0662057M58	RES, 220
R626	0662057M01	RES, 0
R627	0662057N30	RES, 200K
R801	0662057M01	RES, 0

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
R802	0662057M01	RES, 0
R803	0662057M01	RES, 0
R804	0662057M01	RES, 0
R810	0662057M64	RES, 390
R811	0662057U44	RES, 51 1%
R813	0662057V02	RES, 10K 1%
R814	0662057V02	RES, 10K 1%
R817	0662057M01	RES, 0
R818	0662057M80	RES, 1.8K
R819	0662057M89	RES, 4.3K
R820	0613952L47	RES, 301 1%
R821	0662057M01	RES, 0
R901	0662057M98	RES, 10K
R902	0662057M98	RES, 10K
R903	0662057N15	RES, 47K
R904	0662057M98	RES, 10K
R912	0662057N15	RES, 47K
R1013	0662057N23	RES, 100K
R1015	0662057N23	RES, 100K
R1016	0662057M98	RES, 10K
R1018	0662057M98	RES, 10K
R1019	0662057M74	RES, 1K
R1032	0662057M01	RES, 0
R1043	0662057M01	RES, 0
R1088	0662057N23	RES, 100K
R1304	0662057M98	RES, 10K
R1305	0662057M86	RES, 3.3K
R1309DNP	2113743N38	CAP, 33pF
R3001	0687874L02	RES, 0.1
R3206	0662057N23	RES, 100K
R3207	0662057N01	RES, 12K
R3209	0662057N35	RES, 330K
R3210	0613952P60	RES, 412K 1%
R3211	0662057V39	RES, 220K 1%
R3212	0662057N47	RES, 1M
R3300	0662057M14	RES, 3.3
R3305	0662057M14	RES, 3.3
R3403	0687874L02	RES, 0.1
R3504	0687874L02	RES, 0.1
R3555	0662057M50	RES, 100
R3650	0662057M78	RES, 1.5K
R3651	0662057M30	RES, 15

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
R3652	0662057M30	RES, 15
R3900	0662057M98	RES, 10K
R3901	0662057N20	RES, 75K
R3902	0662057N23	RES, 100K
R3903	0662057N23	RES, 100K
R3951	0662057M01	RES, 0
R3952	0662057M01	RES, 0
R3954	0662057M01	RES, 0
R3967	0662057M98	RES, 10K
R3970	0662057M01	RES, 0
R3973	0662057N39	RES, 470K
R3975	0662057N23	RES, 100K
R3976	0662057A96	RES, 91K
R3977	0662057N13	RES, 39K
R3978	0613952E30	RES, 20K 1%
R3979	0662057M26	RES, 10
R3985	0662057M01	RES, 0
R4303	0662057M01	RES, 0
R4388	0662057M91	RES, 5.1K
R4389	0662057N21	RES, 82K
R4392	0662057M68	RES, 560
R4395	0662057M98	RES, 10K
R4396	0662057M90	RES, 4.7K
R4397	0662057N39	RES, 470K
R4398	0662057N15	RES, 47K
R4400	0662057M50	RES, 100
R4401	0662057M74	RES, 1K
R4550	0662057N06	RES, 20K
R5001	0662057N15	RES, 47K
R5020	0662057M01	RES, 0
R5050	0662057N15	RES, 47K
R5052	0662057N33	RES, 270K
R5053	0662057M86	RES, 3.3K
R5055	0662057N15	RES, 47K
R5175	0662057N23	RES, 100K
R5176	0662057N23	RES, 100K
R5177	0662057N23	RES, 100K
R5178	0662057N23	RES, 100K
R5333	0662057M34	RES, 22
R5334	0662057M34	RES, 22
R5401	0662057M90	RES, 4.7K
R5402	0662057M50	RES, 100

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
R5403	0662057N13	RES, 39K
R5404	0662057M98	RES, 10K
R5480	0662057V02	RES, 10K 1%
R5481	0662057M01	RES, 0
R5501	0662057M91	RES, 5.1K
R5502	0662057M50	RES, 100
R5503	0662057M50	RES, 100
R5504	0662057M50	RES, 100
R5614	0662057N15	RES, 47K
R6000	0662057M98	RES, 10K
R6002	0662057M98	RES, 10K
R6006	0662057N31	RES, 220K
R6007	0662057M64	RES, 390
R6013	0662057M01	RES, 0
R6017	0662057M98	RES, 10K
R6044	0662057M98	RES, 10K
R6045	0662057M98	RES, 10K
R6046	0662057M98	RES, 10K
R6047	0662057M98	RES, 10K
R6048	0662057N15	RES, 47K
R6049	0662057M95	RES, 7.5K
R6050	0662057M98	RES, 10K
R6070	0662057M64	RES, 390
R6072	0662057M01	RES, 0
R6074	0662057M01	RES, 0
R6076	0662057M64	RES, 390
R6078	0662057M64	RES, 390
R6080	0662057M01	RES, 0
R6082	0662057M01	RES, 0
R6084	0662057M01	RES, 0
R6098	0662057M01	RES, 0
R7005	0662057M01	RES, 0
R7006	0662057M01	RES, 0
R7013	0662057M01	RES, 0
R7025	0662057A96	RES, 91K
R7026	0662057N15	RES, 47K
R7027	0662057M01	RES, 0
R7029	0662057M01	RES, 0
R7031	0662057M01	RES, 0
R7047	0662057M34	RES, 22
R7048	0662057M34	RES, 22
R7053	0662057M98	RES, 10K

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
R7054	0662057N23	RES, 100K
R7064	0662057M01	RES, 0
SH100	2687523V77	Harmony SHIELD
SH140	2687523V72	CDMA VCO SHIELD
SH200	2687523V76	CDMA IQ SHIELD
SH310	2687523V75	CDMA Mixer SHIELD
SH320	2687523V78	CDMA IF SHIELD
SH330	2687523V74	CDMA BE SHIELD
SH420	2687523V73	CDMA PA SHIELD
SH500	2687523V65	Magic SHIELD
SH570	2687523V64	GSM VCO SHIELD
SH600	2687523V66	Life SHIELD
SH800	2687523V67	GSM PA SHIELD
SH7006	0989668N01	EMI GASKET
SH7007	0989668N01	EMI GASKET
SH7008	0989668N01	EMI GASKET
SH7009	0989668N01	EMI GASKET
SH70010	0989668N01	EMI GASKET
SH7012	0989668N01	EMI GASKET
SH7013	0989668N01	EMI GASKET
SH7014	0989668N01	EMI GASKET
T100	5887510M01	HHM1520 Multiplayer Balun
T600	5885949K08	HHM1409 Multiplayer Balun
T601	5885949K09	HHM1410 Multiplayer Balun
T602	5885949K05	HHM1525 Multiplayer Balun
U101	5188450M07	Harmony Lite 50M07
U140	4809283D73	MQL304 2300MHz VCO
U150	5109940K32	UPC8151TB Current Amplifier
U200	5109817F71	MAX2363 Dual-Band Transmitters
U310	5109944C46	MAX2388 WCDMA LNA
U330	5109817F69	MAX2309 WCDMA Demodulators
U400	5109908K55	PA2001_5W RF PA
U403	5187970L05	AV122 Attenuator
U406	5109768D08	LM20 Temperature Sensor
U407	5187970L13	DD02-92 Power detector
U500	5188450M05	50M05 Magic LV
U510	5109522E63	NC7WZ04 dual inverters
U570	4809283D97	83D97 880-1910MHz GSM VCO
U580	5887694L17	EXB24ATE Attenuator
U625	5109940K41	LIFE
U626	5109512F47	LP3985IM5X 2.5V LDO
U800	5109908K90	08K90 GSM PA

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
U801	5885811G11	DD05-EN722 Dual Coupler Power Detector
U900	5109522E83	NC7SZ11 3-Input AND gate
U1000	5199133J01	RAINBOW 3G 2.3
U1020	5109522E82	NC7SB3157 2X1 Analog switch
U1034	5164751E01	MC74VHC1GT50 buffer
U1060	5109522E24	TC7SH32 2-input OR gate
U1300	5199146J01	28F640W18 64M Flash Memory
U1310	5199146J01	28F640W18 64M Flash Memory
U3000	5188450M06	PCAP 50M06
U3206	5187324N01	LTC3411 2.2V buck regulator
U3301	5109522E84	NC7WZ17 dual Schmitt Trigger buffer
U3900	5164751E01	MC74VHC1GT50 buffer
U3901	5113815A55	NCP304 Voltage Detector
U3970	5185956E52	MAX1830 BUCK Regulator
U5010	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5011	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5012	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5013	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5020	5105750U28	TC4S66F Bilateral Analog Switch
U5022	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5024	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5026	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5028	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5030	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5032	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5034	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5036	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5040	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5042	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5044	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U5046	5109522E82	NC7SB3157 2X1 ANALOG SWITCH
U6000	5102870C25	OXCF950-TB-B PCMCIA to UART Interface
U6001	5189233U51	2K bit EEPROM AT93C56AY1-10YL-2_7
U6003	5185130C22	LP2985 3V LDO
U6007	5109817F30	LMV331 Comparator
U6010	9185003D11	EZADT RC Filter
U6011	9185003D11	EZADT RC Filter
U6012	9185003D11	EZADT RC Filter
U6013	9185003D11	EZADT RC Filter
U6014	9185003D11	EZADT RC Filter
U6015	9185003D11	EZADT RC Filter
U7000	5109962C28	AT57460 WCDMA processor

Table 16. Electrical Parts List

ReferenceNumber	PartNumber	Description
VR4300	4809948D44	CSPESD304 quad ESD diode array
VR5000	4809948D44	CSPESD304 quad ESD diode array
VR5002	4809948D44	CSPESD304 quad ESD diode array
VR5004	4809948D44	CSPESD304 quad ESD diode array
VR6001	4809948D44	CSPESD304 quad ESD diode array
VR6002	4809948D44	CSPESD304 quad ESD diode array
VR6003	4809948D44	CSPESD304 quad ESD diode array
VR6004	4809948D44	CSPESD304 quad ESD diode array
VR6005	4809948D44	CSPESD304 quad ESD diode array
VR6006	4809948D44	CSPESD304 quad ESD diode array
VR6007	4809948D44	CSPESD304 quad ESD diode array
VR6008	4809948D44	CSPESD304 quad ESD diode array
VR6009	4809948D44	CSPESD304 quad ESD diode array
VS5001	4813830C29	MMSZ5246B Zener Diode
VS5002	4809788E06	UDZTE-176.8B Zener Diode
VS5003	4809788E06	UDZTE-176.8B Zener Diode
Y130	4809718L14	NT5032SA 15.36MHz crystal
Y500	4809612J43	Magic LV 26MHz crystal
Y3982	4809995L13	HzCC5V 32.768K crystal
Y6000	4802582S60	TSX-5-14 14.7456MHZ crystal

Accessories

Table 17.

Description	Part Number
Mono Headset with Send/End*	SYN8419B
External Antenna	

*If applicable