Service Manual

Level 3

Draft 1.0

MOTOROLA

DIGITAL WIRELESS TELEPHONE

Model C975/C980

UMTS 2100MHz/PCS 1900MHz/DCS 1800MHz/GSM 900MHz

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3G Flash Procedures

Introduction

This document is intended to describe the flashing (firmware upgrade) procedures for 3G terminals. The 3G terminal described in this document will be limited to the V975, V980, C975, and C980.

Firmware upgrades need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the firmware upgrade application database is up-to-date.

Firmware upgrades allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific circumstances, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the 3G terminal.

Power Hardware

1. Fully Charged battery (SNN5743A or equivalent)

2. Full-rate Charger (SPN5049 or equivalent)

Interface Options

1. USB Data Kit (S8951)
   USB Cable (SKN6311A)
   Data Software CD

Software Requirements

The RSD (Remote Software Download) General Release is used to allow functions such as firmware upgrade, Phone Swap, and Multi-refurbish. Contact your local Motorola service representative to receive download information for the RSD and related support files. Also insure that the RSD database has the latest update.

Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1-1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a nonfunctional (Bricked) 3G terminal.

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery
2. Full-Rate Charger w/battery (recommended)

If the user decides on using the battery only solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the flash process. This action may cause unrecoverable failures to the 3G terminal.

RSD Firmware Upgrade Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal.

1. Launch the RSD General application
2. Connect the unit as illustrated in figure 1-1.
3. Power up the 3G terminal
4. If the 3G terminal doesn't power up, refer to the Force Flash section.
5. Once the phone is fully powered up, the Radio Information Panel will be updated.
7. In the Utilities Panel, select Firmware Upgrade.
8. In the Main information Panel, select desired restore and logging options
9. In the Main information Panel, click on the Start button to begin Firmware upgrade.

NOTE: DO NOT interrupt any hardware connections during the flash process. Connection interruptions may cause the flashing process to fail and render the 3G terminal non-operational.

10. When the process is complete, the Main Information Panel will indicate whether the process was successful. At this time you may safely disconnect the 3G terminal.
11. Power up the 3G terminal to insure that the flash procedure was successful.

Figure 1-1. RSD Hardware Configuration

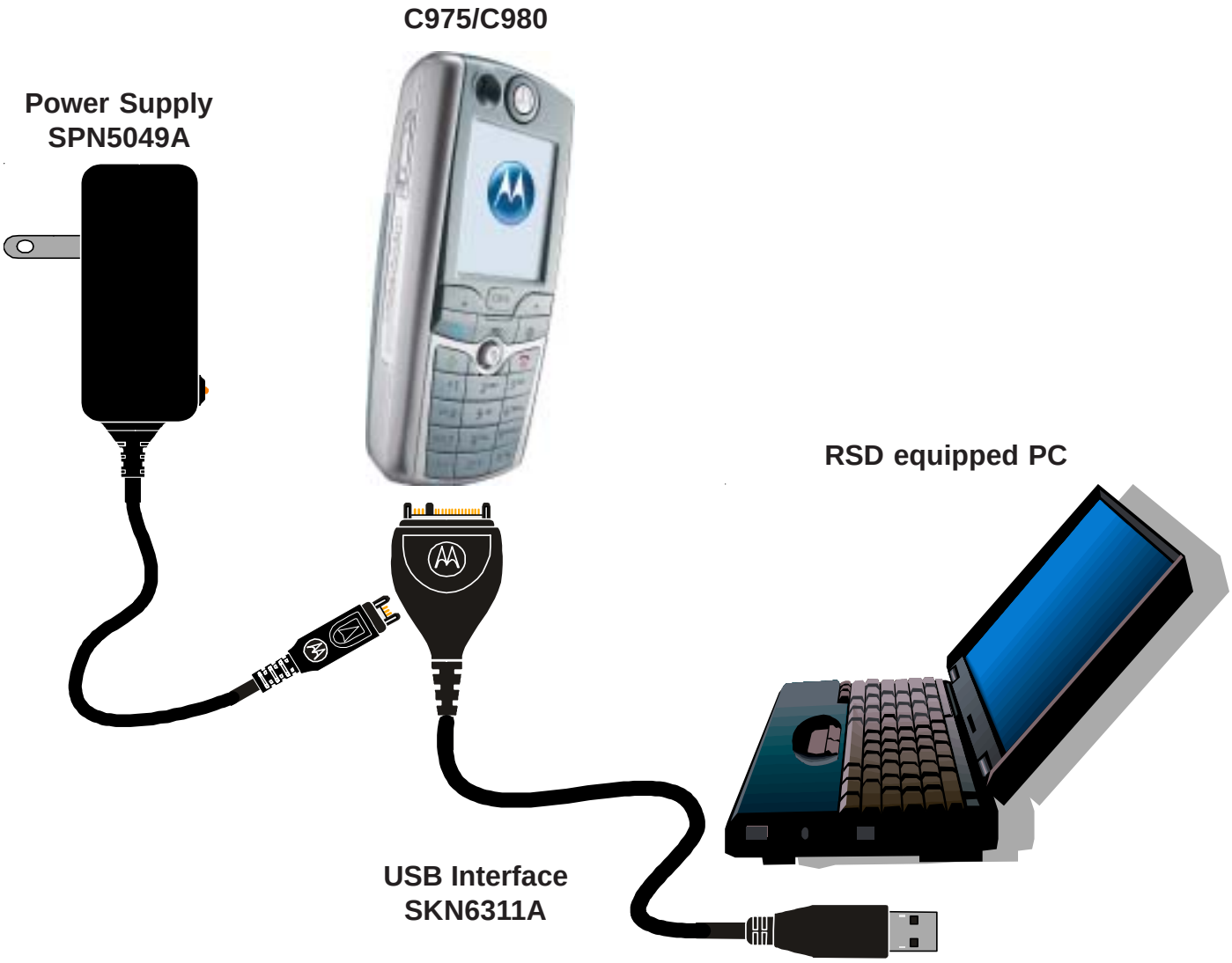


Figure 1-2. RSD General Release GUI

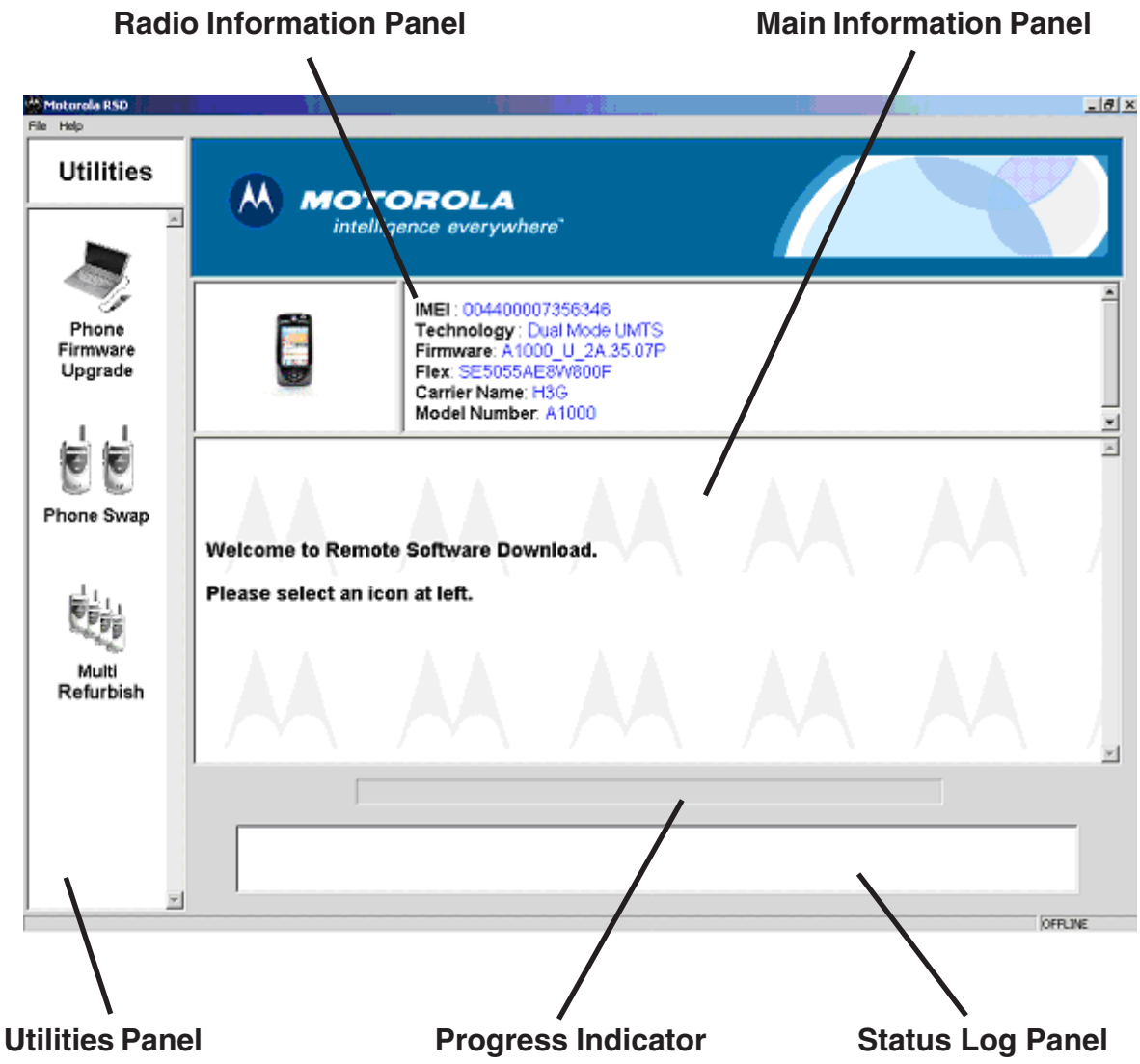
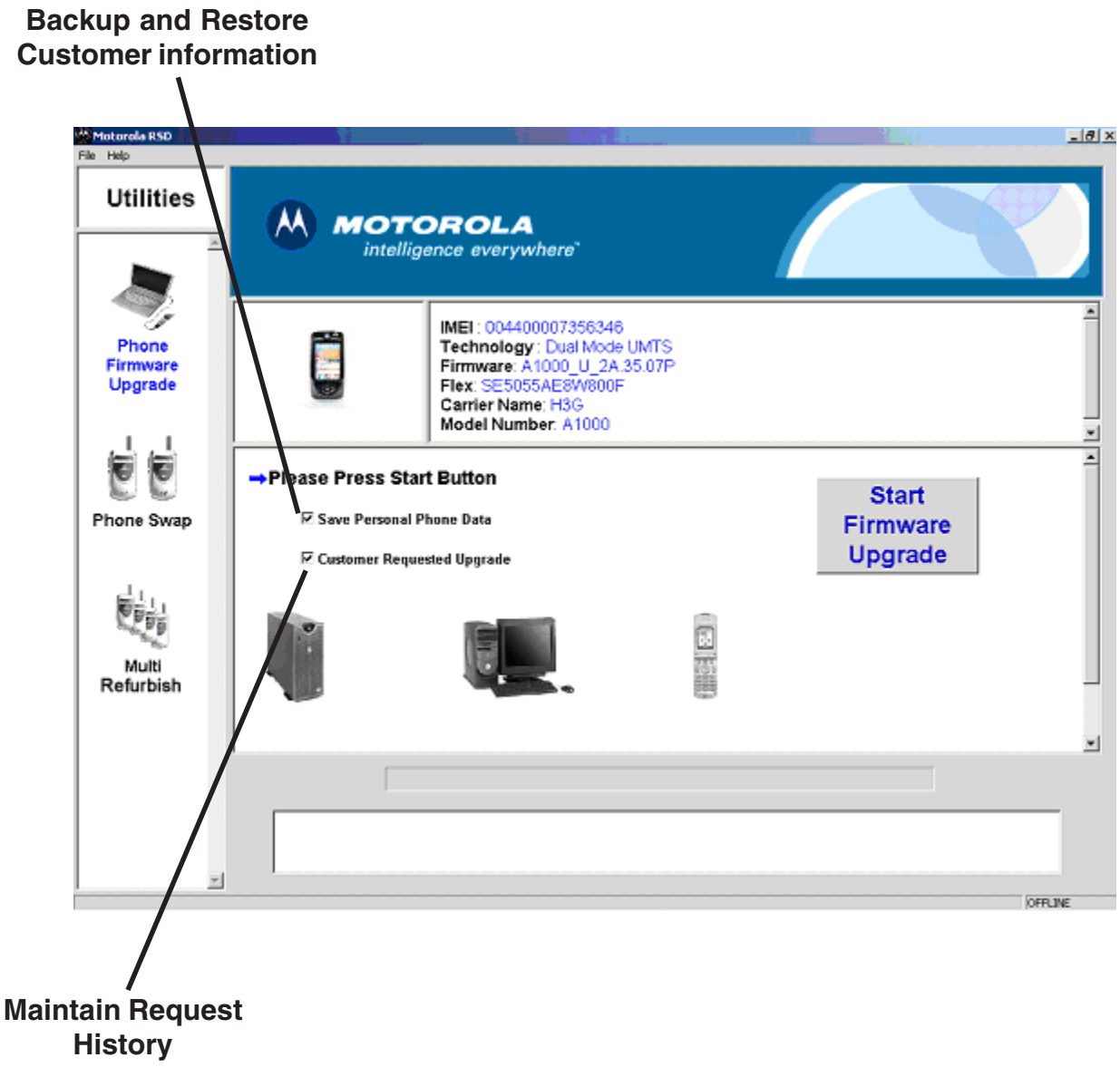


Figure 1-3. Firmware Upgrade



Force Flash Procedures

The procedures described in this section apply only to situations where the 3G terminal will not initiate it's normal power up sequence, but may recover functionality by a repeat flash procedure.

There are two possible alternatives to place the 3G terminal in force flash mode.

Key Hold Solution

Hardware: Refer to Figure 1 (USB solution)

Step 1. Remove the battery from the 3G terminal

Step 2. Prior to connecting the USB cable, press and hold "#" and "*" keys from the 3G terminal

Step 3. Attach the USB cable

Step 4. Verify that the RSD application detects the 3G terminal, if it's not detected, press and hold the gaming keys once again.

Force Flash USB Cable Solution

Hardware: Refer to Figure 1-1 (USB solution), except, replace USB cable (SKN6311A) with force flash cable (SKN6168A)

Step 1. Connect the force flash cable in the same manner described in Figure 1-1.

Step 2. The 3G terminal will automatically be placed in force flash mode. There's no need to press the power key. The RSD application will now detect the 3G terminal

Manual Test Procedures

Introduction

The phone allows computer controlled testing of various test parameters.

This chapter includes the computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

Non-Signaling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signaling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The phasing parameters are stored in an EPROM in the transceiver board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted (phased) with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5743A[1] or equivalent)
- Full-Rate Power Supply (SPN5049A[1])
- Battery Eliminator (5-00-3Y-12000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

RF Interface

- RF Adapter (2-00-4E-10000[2])
- SMA/N type Adapter (0-00-00-40042)
- SMA Cable 0.5m (0-00-00-40047[2])
- USIM (0-00-00-40810[2])

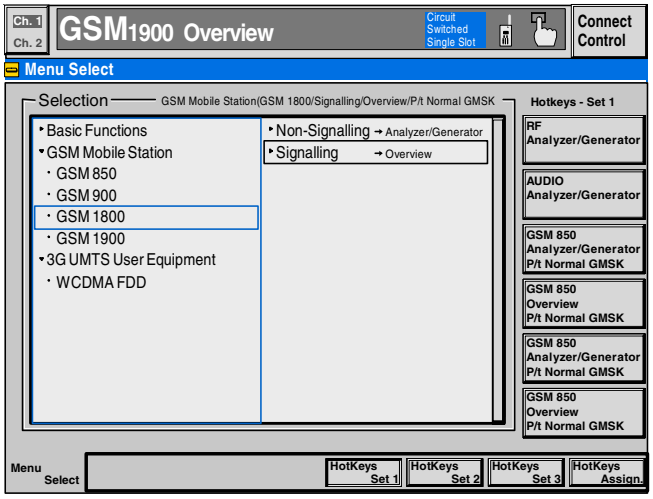
[2]Contact AMS Software and Elektronik GmbH for ordering

Call Origination

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

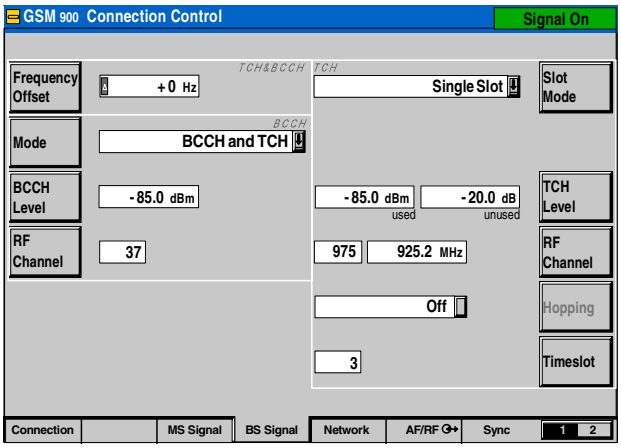
1. Install the test USIM in phone.
2. Connect hardware as illustrated in figure 2-5.

Figure 2-1. GSM Signaling Setup



3. Setup up the test box for GSM, DCS, or PCS Signaling
4. Set Broadcast Channel (BCH) to 120 (GSM), 700 (DCS), or 661 (PCS)
5. Set Broadcast channel level to -85dBm
6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS/PCS)
7. Set Traffic channel level to -85dBm
8. Wait until the phone indicates a receive signal

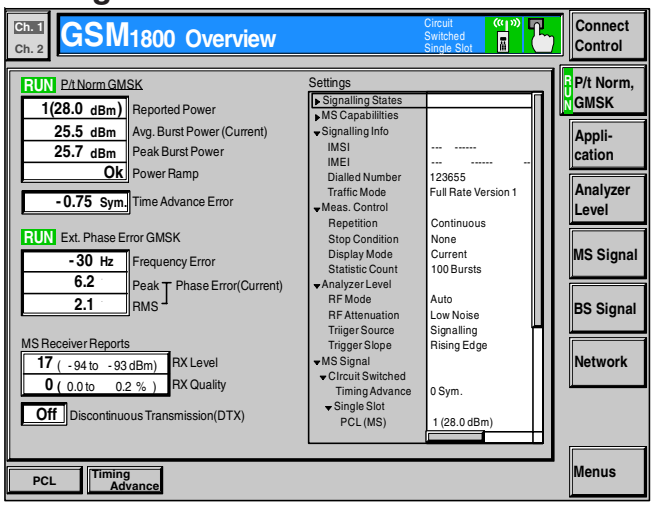
Figure 2-2. GSM Connection Control



9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 2-3. GSM Call Connected



Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-1. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	27	31	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 2-2. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

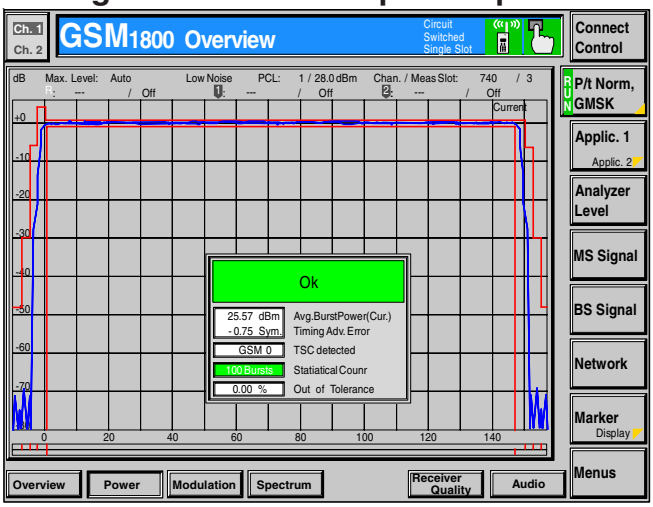
[1]Power Level = 15
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 2-3. PCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 15
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Figure 2-4. Burst Output Shape



Burst Output Shape should fall within the standard limits of the Power Ramp.

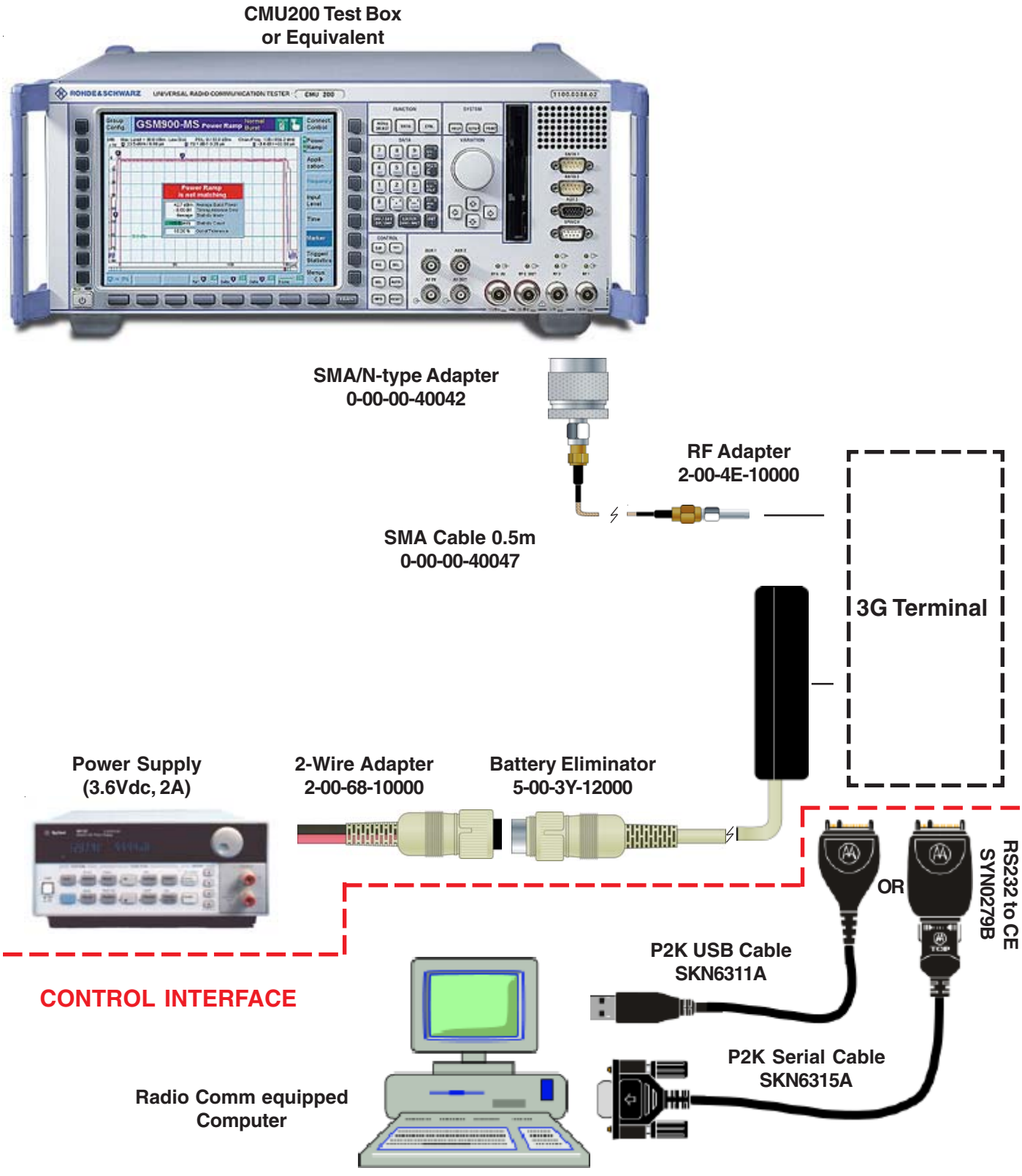
BER measurements is only required if RX Quality reads a value of 4 or greater.

It is recommended that handover procedures be performed as shown in the following table.

Table 2-4. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

Figure 2-5. Manual Test Hardware Configuration



WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 2-5.

Software Requirements

None.

Call Origination (WCDMA)

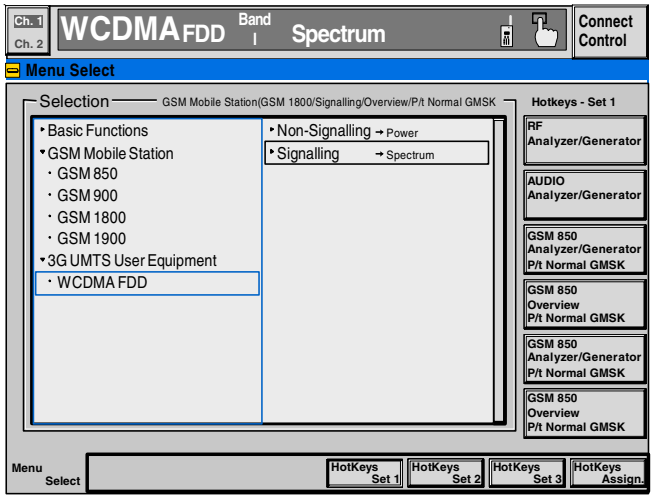
Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signaling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

Figure 2-6. WCDMA Signalling Setup

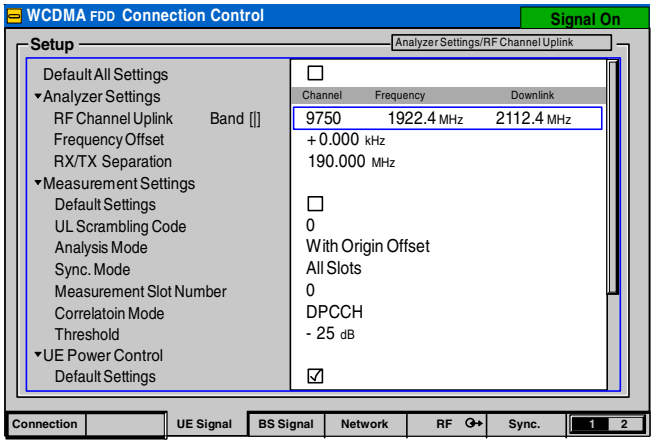


3. Setup up the test box for WCDMA FDD Signaling

4. Set UE Signal, RF Channel Uplink to 9400

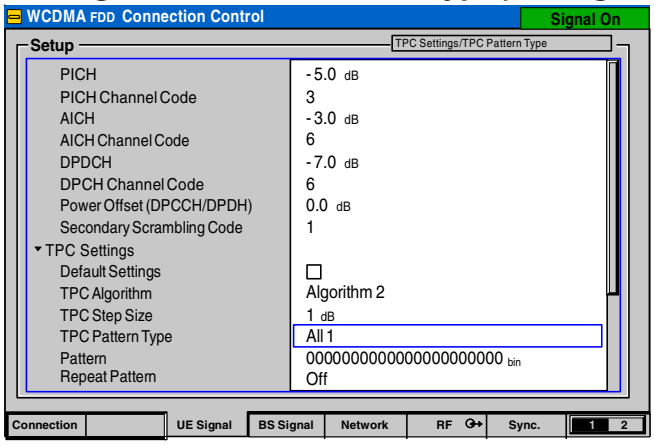
5. Set UE Signal, RF Channel Downlink to 9800

Figure 2-7. Channel Uplink(UE Signal)



6. Set TPC Pattern Type to All 1

Figure 2-8. TPC Pattern Type(UE Signal)

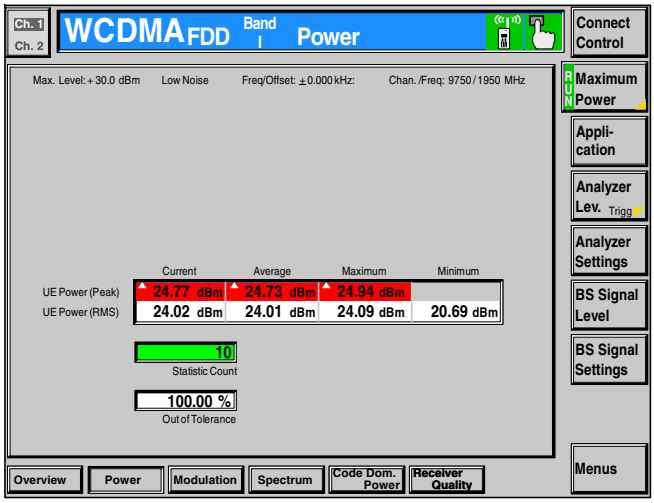


7. Wait until the phone indicates a signal

8. Dial a number from the phone and press the send button.

9. The phone is now connected.

Figure 2-9. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-5. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 2-10. WCDMA Modulation

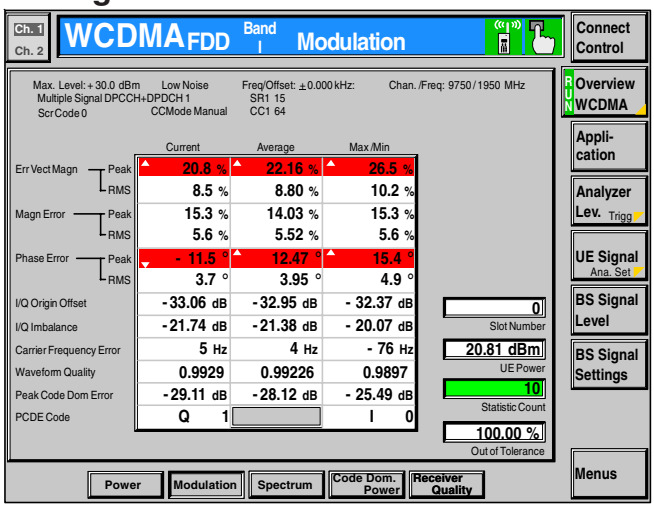
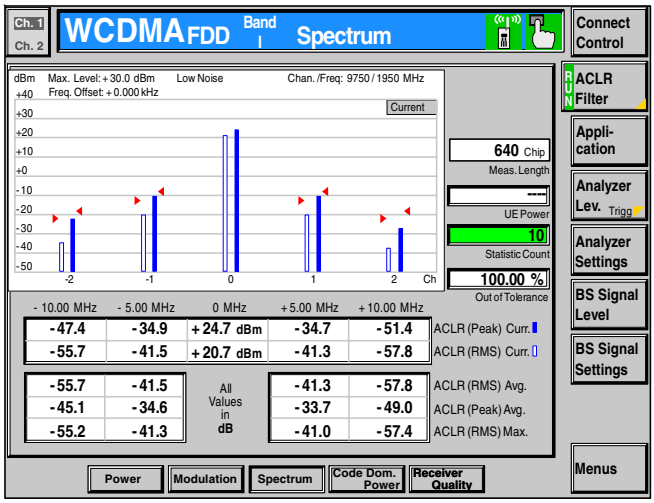


Figure 2-11. ACLR Screen

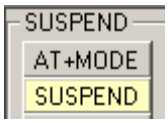


Non-Signaling Test Procedures (GSM/DCS/PCS)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands are sent using a computer.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)



Click SUSPEND (USB Only)

Hardware Requirements

Control Interface Options

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

[1]Contact your local Motorola dealer for ordering

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

Verify TX Power Output (GSM/DCS/PCS)

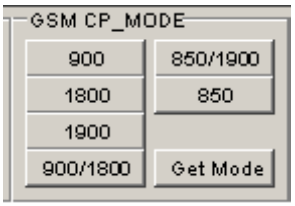
Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-6. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28.2	30	dBm
PCS TX Power Out	28.2	30	dBm

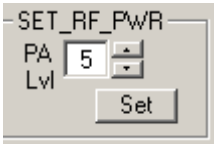
[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

Click on 900/1800 (GSM/DCS) or 1900 (PCS)

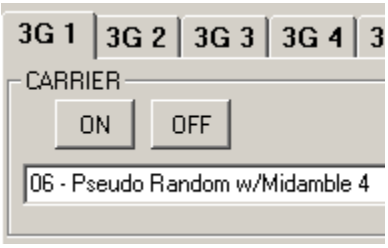


Enter 38 (GSM), 700 (DCS), or 661 (PCS) and then click Set

Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



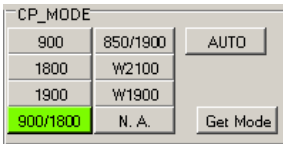
NOTE: Set Training Sequence to 4 on the test equipment.

GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

Broadcast Channel (BCH): 38
Broadcast Channel (BCH) Level: -105 dBm

Click on 850/1900 (GSM/DCS) or 1800 (DCS)



Enter Channel 38
Click INIT

Click Execute

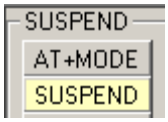
Verify return data is approximately -105 dBm

Non-signaling Test Procedures (WCDMA)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Hardware Requirements

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

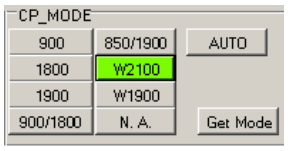
Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-7. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	19.5	22	dBm

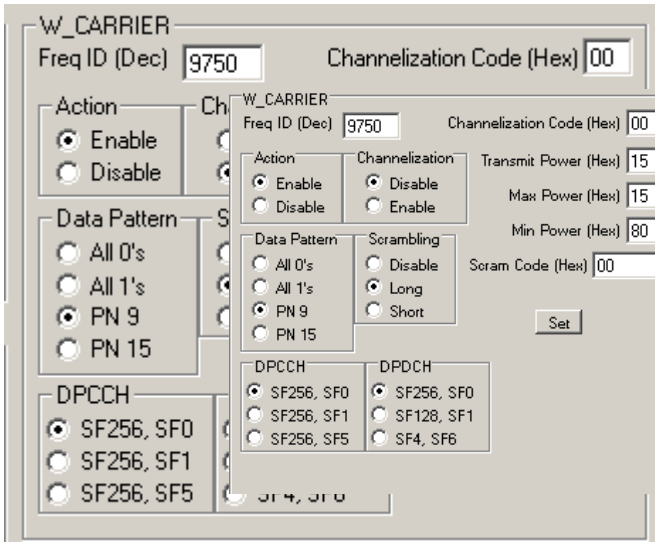
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)

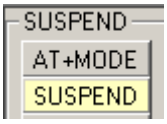


Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

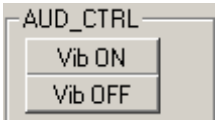
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Vibrator Test

Enable or Disable Vibrator



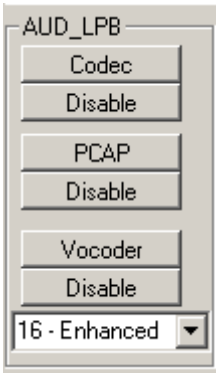
Verification

Verfiy vibration function when enabled.

Handset Mic/Speaker test

Set as illustrated.
Click Set

Select Enhanced Full Rate and click Vocoder



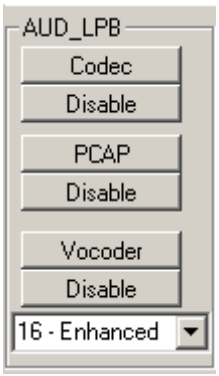
Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

Mono Headset Mic/Speaker test

Set as illustrated
Click Set

Select Enhanced Full Rate and click Vocoder

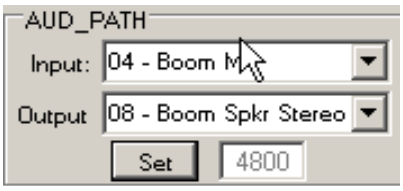


Verification

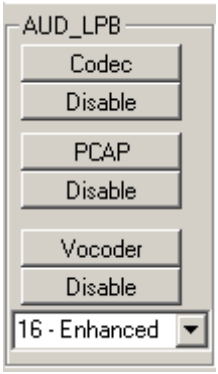
Speak into the headset mic and listen for undistorted speech in the headset speaker.

Stereo Headset Mic/Speaker test

Set as illustrated
Click Set



Select Enhanced Full Rate and click Vocoder



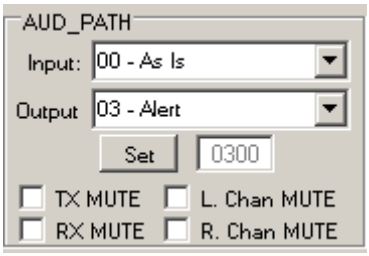
Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

Set AUD_TN_GEN as illustrated and click Start Tones

Set AUD_PATH as ilustrated and Click Set



Verification

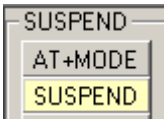
Listen for undistorted audio on the Alert.

Display Test Procedures

This section will describe the proper test procedures to determine the functionality of the color display.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Display Backlight Test

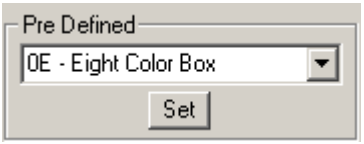
Click "FL Off" to disable backlight
Click "FL On-Full" to enable backlight

Verification

Verify that the backlights respond for each issued command.

Display Color Test

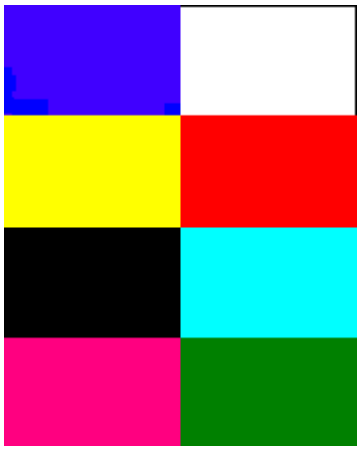
Select Eight Color Box and click "Set"



Verification

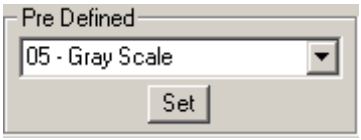
Verify that the color pattern on the phone's display matches the color box in figure 23. Also verify edges (uniform/smooth).

Figure 20. Eight Color Box Pattern



Display Linearity Test

Select Grey Scale and click “Set”



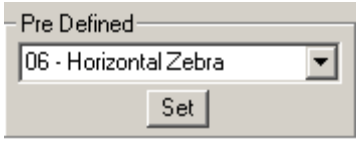
Verification

Verify that the Grey scale block on the phone’s display matches the Grey scale block in figure 14. This test can also be used to confirm that the color intensity is linear.

Figure 21. Grey Scale Block

Display Flicker Test

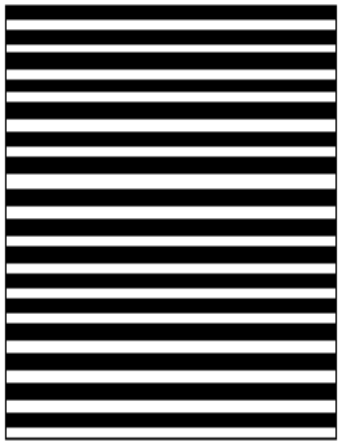
Select Horizontal Zebra and click “Set”



Verification

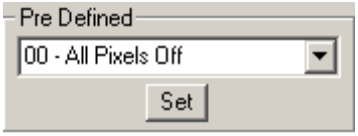
Verify that no noticable flicker exists.

Figure 22. Zebra Pattern



Display Pixel Defect (Bright)

Select All Pixels Off and click “Set”

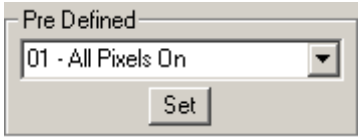


Verification

Verify that no greater than two pixels are off.

Display Pixel Defect (Dark)

Select All Pixels On and click “Set”



Verification

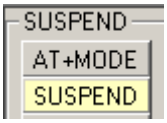
Verify that no greater than two pixels are on.

LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

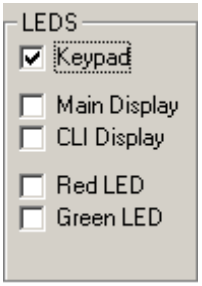
In order to successfully send test commands to the phone under test, the phone doesn’t need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Click AT+MODE (Serial Only)



Keypad Backlight

Select Keypad to enable. Deselect Keypad to disable.



Verification

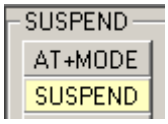
Verify that all keypad backlight LEDs activate.

Camera Testing

This section is intended to describe the procedures that will determine whether the camera function of a Motorola terminal is under normal operating conditions.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

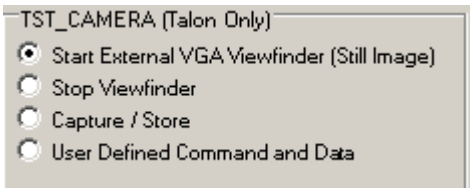
Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



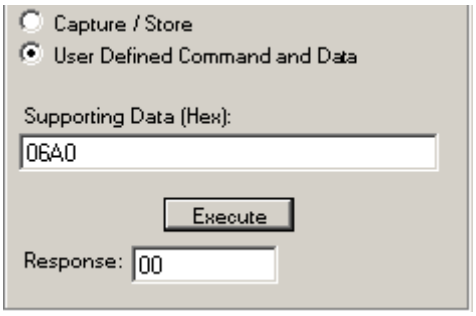
Data Line Integrity Check

When performing this test, RadioComm needs to be switched to GSM for proper responses. Go to the Menu bar and select Main>MA>GSM.

Select Start External Viewfinder



Select User Defined Command, enter 06A0 for data, and click Execute

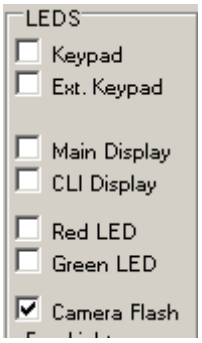


Verification

Verify that the response data returned 00.

Camera Flash Check

Select Camera Flash to enable. De-select Camera Flash to disable.



Verification

Verify that Camera Flash LED activates.

Theory of Operation

C975/C980 Overview

Motorola C975 and C980 telephones deliver 3G features in a smaller and lightweight package. These global system for mobile communications (GSM) general packet radio service (GPRS) wireless application protocol (WAP)-enabled mobile phones incorporate an icon based interface (UI) for easier operation, allows short message service (SMS) text messaging, and includes personal information manager (PIM) functionality. The C975 and C980 are tri band phones that allow roaming within the GSM 900 MHz, (DCS) 1800 MHz digital cellular system, and PCS 1900 MHz bands, in addition to the UMTS WCDMA 2100 MHz band.

C975 and C980 telephones support GPRS and SMS in addition to traditional circuit switched transport technologies.

C975 and C980 telephones feature a 65k TFT color display. The housing contains the keypad, transceiver printed circuit board (PCB), microphone, flex connection, external accessory connector, smart button, volume buttons, and voice button. The standard 820 mAh Lithium Ion (Li Ion) battery fits behind a removable back cover.

The phone accepts both 3V subscriber identity module (SIM) cards which fit into the SIM holder underneath the battery. The antenna is internally mounted within the housing. Inexpensive direct connection to a computer or handheld device via USB for data and fax calls, and for synchronizing phonebook entries with mobile Phone Tools software, can be accomplished by using the optional data cable and soft modem.

C975 and C980 telephones use advanced, self-contained, sealed, custom integrated circuits to perform the complex functions required for GSM/WCDMA communication. Features available in this family of telephones include:

- WCDMA 2100 MHz, GSM/GPRS 900/1800/1900 MHz
- 2-Way Video Call
- Audio/video streaming, capture, download and playback
- Advanced Messaging (MMS, E-Mail, IM with

Figure 3-1. C975 Transceiver

Presence)
- Synchronization (via Over-The-Air and PC)
- Built in Speaker phone
- Speaker Dependant Voice Activation and Voice Note Recording
- 1.9" TFT display, 176x220, 65K color
- VGA camera with 4x zoom, CIF camera for video call
- Java™ MIDP 2.0
- Enhanced WAP 2.0 and Motorola Internet Browser
- Multimedia: MPEG4, WMV, WMA, MP3, AAC, MIDI, XMF
- 16mm Polyphonic Speaker (24 voice polyphony, 16 channels)
- Supports removable TransFlash external memory card

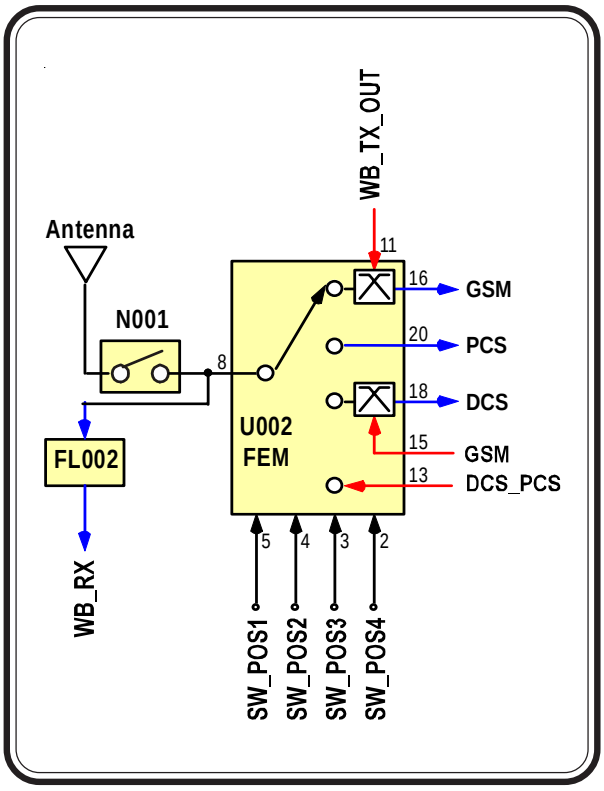
Voice tags can be used for voice dialing up to 20 phone numbers in the phone book and for creating up to 5 voice shortcuts for menu items. The phone must be "trained" by the voice tag being read into the phone's memory twice before it is recognized.

You can add voice tags to the phone's memory using the usual name addition
methods (i.e., via the phone book menu structure or with the shortcut editor).

Front End Module

GSM receive signals from the antenna are fed into the FEM (Front End Module) through an antenna matching network and RF connector (N001). The WCDMA receive signal is directly tapped into the antenna matching network. This WCDMA receive configuration allows the mobile transceiver to receive WCDMA and GSM signals simultaneously, facilitating the ability to handover from a GSM network to UMTS network and vise-versa.

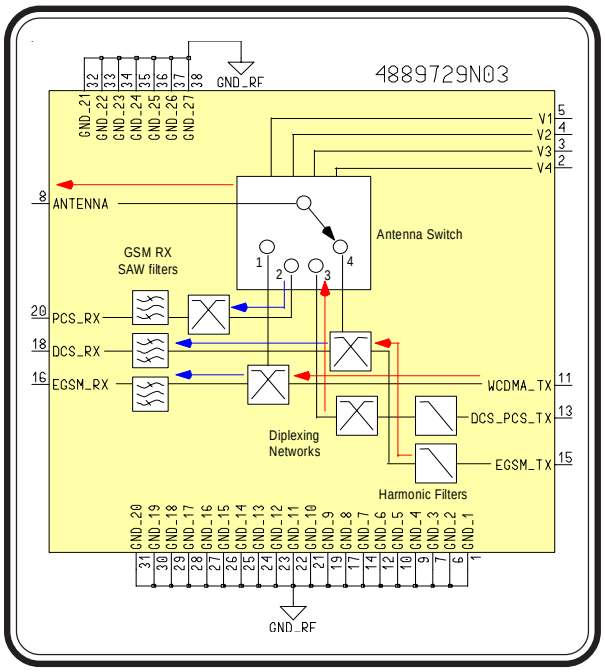
Figure 3-2. RF Top



WCDMA and GSM (all bands) transmit signals are passed through the FEM and fed into the antenna for transmission. If N001 is used, all WCDMA and GSM signals are fed into N001. Also, the internal antenna path will be in an open state when N001 is used.

The FEM integrates a 4-position GaAs antenna switch, diplexers, transmit harmonic filters, SAW filters and matching components on a multilayer low-temperature cofired ceramic (LTCC) module. The module provides band selection and filtering between the EGSM, DCS, PCS, and WCDMA (UMTS) receive and transmit bands in the 3G terminal.

Figure 3-3. FEM Module (U002)



There is a network on each port of the antenna switch that serves several functions. The primary function is to make each switch path behave as an open circuit to incoming signals in the WCDMA receive band (2110 – 2170 MHz). Signals in the WCDMA Rx band are thereby reflected back to the WCDMA receiver. Received signals in the EGSM, DCS or PCS bands are allowed to pass through the switch and undergo some pre-filtering, then pass through SAW filters before leaving the module.

Signals from the WCDMA transmitter are diplexed with EGSM Rx, sharing switch position 1. Similarly, signals from the EGSM transmitter are diplexed with DCS Rx, sharing switch position 4. Switch position 3 is used solely by the DCS/PCS transmitter, and switch position 2 is used only by PCS Rx.

Band Selection in the Front End Module follows the Truth Table shown in table 3-1.

Table 3-1. FEM Truth Table

Band Selected	V1	V2	V3	V4
WCDMA Rx	x	x	x	x
WCDMA Tx, EGSM Rx	1	0	0	0
PCS Rx	0	1	0	0
DCS/PCS Tx	0	0	1	0
EGSM Tx, DCS Rx	0	0	0	1

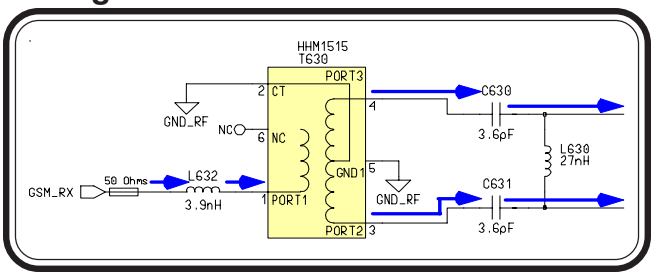
WCDMA Rx is available in any switch position.
Logic “1” is defined as 2.5 volts minimum.
Logic “0” is defined as 0 volts.

RF GSM Receiver

BALUN

From the FEM, the GSM singled-end, unbalanced received signals are fed into the Algae MB section of the Blue Module (900). Since the Algae MB expects a balanced differential receive input signal, the EGSM, PCS, and DCS signals must first pass through a differential conversion. Balun transformers provide the conversions from an unbalanced to a balanced line condition.

Figure 3-4. Balun Transformer

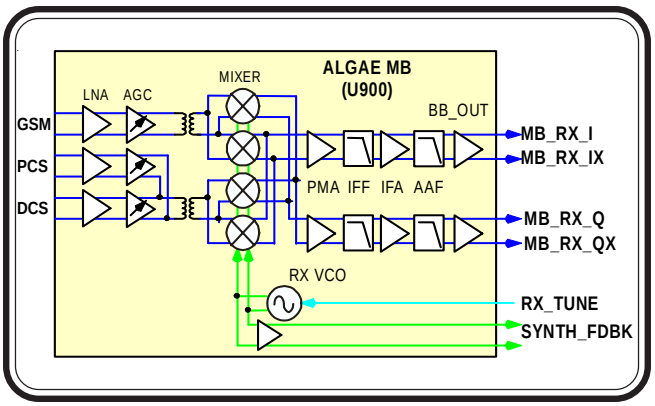


Each GSM band will contain a Balun transformer for differential conversions. The expected insertion loss for the Balun transformer is approximately 0.6 dBm.

BLUE MODULE IC (ALGAE)

Three LNAs are used for each receiver frequency band. Two hi-band LNAs are used for DCS and PCS frequencies and one low-band LNA is used for EGSM. Both hi-band LNAs are grouped together to share the same impedance matching transformer at the output. The low-band EGSM LNAs uses a separate impedance matching transformer at the the output.

Figure 3-5. ALGAE MB (Receiver)



Automatic gain control is provided by an AGC current steering differential pair. This current steering stage diverts current from the LNA load to supply in order to reduce the gain. The current steering differential pair alone would not have the desired transfer function, therefore an AGC linearizer is needed to provide a response that is linear in dB/V.

The LNAs drive AGC current steering stages that feed integrated transformer matching networks. The transformer drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q.

The downmixer converts the RF signal to baseband so that the signal can pass through a low-pass antialiasing filter and be converted to a digital format.

The output of the mixer connects directly to the post-

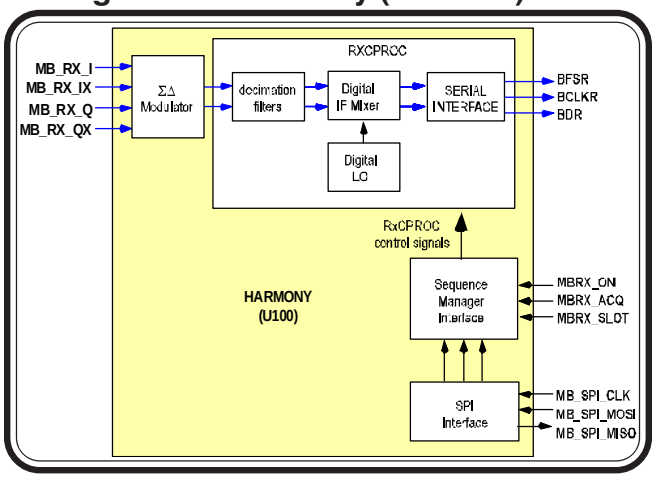
mixer amplifier. Large integrated capacitors are used to provide a low-frequency, low-pass corner at the output of the mixer. The signal then passes through baseband amplification and anti-aliasing filtering. The output of ALGAE MB will be balanced RXI and RXQ signal. It will have a 100kHz Very Low Intermediate Frequency (VLIF) signal that will be sent to the Harmony for Analog to digital conversion.

The LO signal is provided by a fully integrated VCO that drives either a divide-by-two or divide-by-four quadrature generator. In addition, a divide-by-3or5 circuit is used to feed back the LO signal to the synthesizer. The divide-by-3or5 circuit drives a differential output stage that provides the appropriate power level to the synthesizer. This output stage is shared with the TX path and provides the synthesizer feedback signal in both transmit and receive.

HARMONY GSM_RX (U100)

The RXI and RXQ VLIF signal entering the Harmony is sent to the Sigma-Delta modulator which transforms the slow moving analog signal into a high speed digital output. The Sigma-Delta modulator is set as an Analog-to-Digital Converter (ADC). The output of the Sigma-Delta modulator is then fed into the Receive Coprocessor (RxCPROC).

Figure 3-6. Harmony (GSM RX)



The RxCPROC includes the digital signal processing hardware required for the receive transceiver (Rx) after the initial conversion done by the sigma-delta modulator. It's configured to be used in the very low intermediate frequency mode (VLIF). The RxCPROC supports the GSM and EDGE standards.

The RxCPROC is represented by blocks listed as "decimation filters", "digital IF mixer", "digital LO" and "serial interface". The RxCPROC decimates and filters the I and Q quadrature input signals and converts them to baseband. Processed signals are sent serially to the Base Band Port (BBP) to be further handled by the DSP and VIAC.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data to the BBP module in the POG. SDFS is a framing signal which marks the beginning of an I,Q transfer. SDRX is the serial data. The clock used for the serial transfer is SCLK.

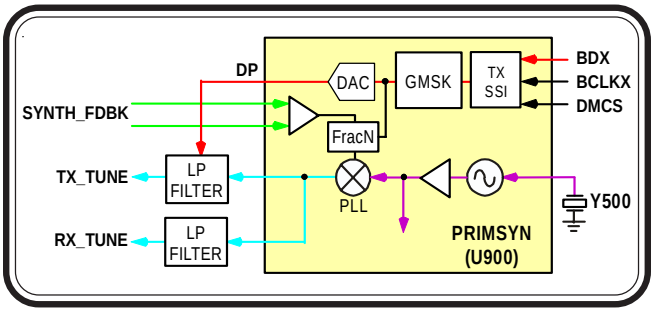
The RxCPROC is controlled via the SEQUENCE MANGER or SPI. Each control line of the Seq. Manager can be overridden by a corresponding line from the SPI (MB_SPI_CLK, MB_SPI_MOSI). Layer One timer signals (MB_RX_ON, MBRX_ACQ, MBRX_SLOT) from POG control the start of major sequences of events.

RF GSM Transmitter

BLUE MODULE IC (PRIMSYN GSM_TX)

The PRIMSYN receives SSI TX data at *DMCS* (digital input to start Tx modulation), *TXCLK* (clock for serial transfer) and *SDTX* (serial Tx data) from POG. This data pattern input to a fractional N synthesizer with a 24-bit resolution. For EGSM the synthesizer output is 880 – 915MHz, DCS is 1710 – 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

Figure 3-7. PRIMSYN (GSM TX)

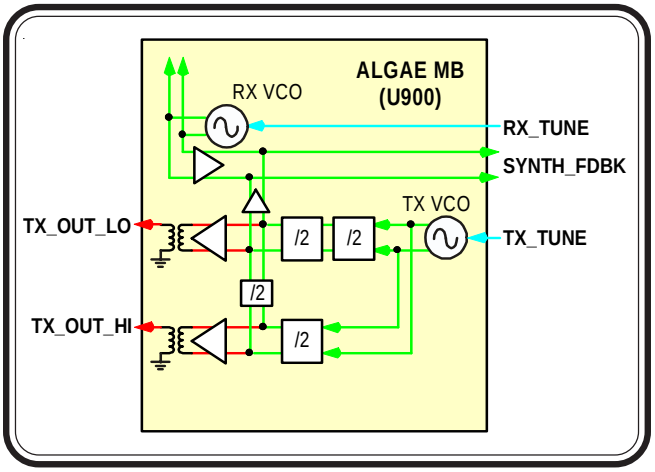


BLUE MODULE (ALGAE)

TRANSMIT SECTION

An integrated VCO is used for the transmit path. A single VCO is used for transmit. A low noise floor divide-by-2 stage drives the high band output. The low band output is driven by a divide-by-4 stage.

Figure 3-8. ALGAE MB (Transceiver)



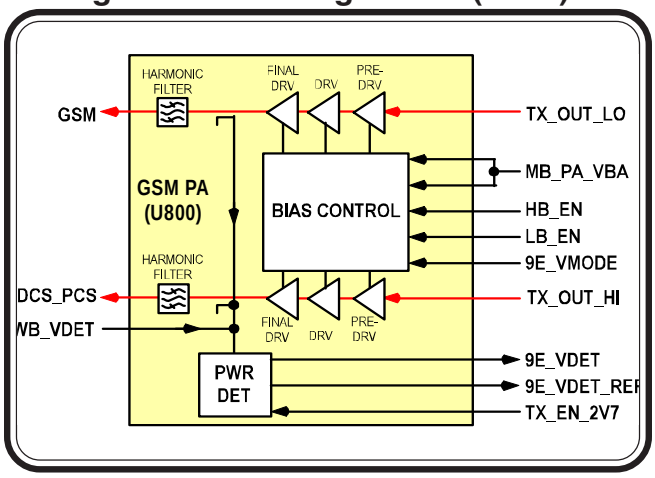
Two transmit output stages are provided. Both stages have integrated output matches in order to reduce the required number of discrete components. The integrated matches are implemented as differential to single-ended transformers.

The transmit signal is fed back to the synthesizer through a differential output stage that is shared with the receiver.

GSM PA (U800)

The TX VCO output signal from the ALGAE MB is injected in the Durango 9E3G via the TX_OUT_LO (Low Band) and TX_OUT_HI (Hi Band). Durango

Figure 3-9. Durango 9E3G (U800)



9E3G is a quad band PA Module for GSM applications in 3G phones. The module uses a dual amplifier lineup which operates in the three separate EGSM, DCS1800, and PCS1900 bands. It is compatible with GSM/GPRS operating modes. The integrated module incorporates coupler/detector for power control, Low pass filtering for harmonic rejection, and is internally input and output matched to 50 ohms.

This Transmit module is to be used as the final amplification stages in the A1000 for the EGSM (900 MHz), DCS (1800 MHz) and PCS (1900 MHz).

The nominal expected maximum gain is ~30dB.

The *VDET* (output) is the RF feedback along the DC reference *V_REF_DET* (output) are used in backend PA Control (PAC) processing by the HARMONY.

VBA_1 and VBA_2 are inputs from HARMONY that controls the PA output level. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases.

The power detector is internal to the PA and is shared among all GSM bands as well as WCDMA. WB_VDET connects WCDMA TX to the power detector

HB_EN enables the high band (DCS/PCS) amplifier lineup. LB_EN enables the low band (EGSM) amplifier lineup. TX_EN_2V7 enables the detector.

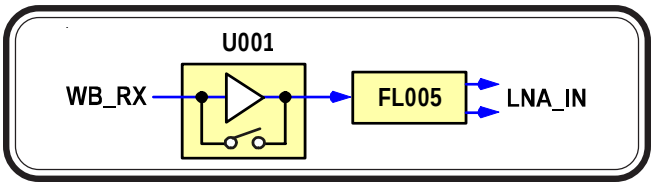
9E_VMODE sets the operating mode of the PA. GMSK and EDGE modes are supported, but only GMSK mode is used in this design. 9E_VMODE is set high during GMSK TX mode. 9E-VMODE is set low when the transmitter is in standby mode. This line is also enabled in WCDMA mode to allow proper WCDMA power detection.

RF WCDMA Receiver

MC13820 (U001)

The first IC in the WCDMA Rx line up is U001 (MC13820), which is a Low Noise Amplifier. The RX frequency will be amplified and passed on to OneLife WB through FL005. The LNA is controlled by Harmony (U100) through two enable lines. MBC_EN1 enables gain for the LNA while MBC_EN2 enables the IC. Both lines can be probed at testpoints located near Harmony (TP120 and TP121).

Figure 3-10. WCDMA LNA

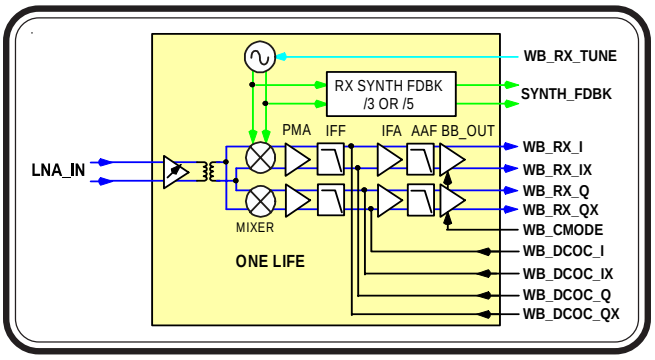


BLUE MODULE (ONELife)

ONELife is a full custom mixed signal BiCMOS IC with the SiGe option with electroplated copper inductors. This IC is a fully differential direct-conversion front-end IC and is comprised of a multiband RF section and a single path baseband section. The RF section is comprised of three Low Noise Amplifiers, two sets of quadrature mixers and an integrated 4GHz VCO with a divided prescaler output. Only one LNA is used in this design to cover the WCDMA/UMTS band (2110-1710). The LNA has two gain states; a high gain state and a bypass state with no reverse isolation. The LNA drives the quadrature mixers, via an integrated transformer matching network, that convert the RF signal to baseband, quadrature I and Q. The LO signal is provided by fully integrated VCOs that drives a divide-by-two quadrature generator. In addition, a divide-by-three/five circuit is used to feed back the LO signal to the synthesizer via an open collector output stage.

The baseband section is comprised of two separate I and Q paths each containing a PMA, an anti-aliasing filter made up of an IFA with an active pole and DCOC, two bi-quad sections, and an output buffer. The baseband signal path has six poles of baseband filtering distributed between mixer pole, the active IFA pole, and the two bi-quad blocks. The PMA has pseudo-continuous gain capability and is part of the AGC system along with the LNAs. The PMA AGC is controlled through five dedicated IC pins. At the output of the PMA stage, a baseband detector circuit provides broadband, strong signal information to the baseband part. DC Offset correction is provided through external differential pins to provide offset corrections to the internal IFA stage. The output buffer receives an input voltage via feedback from the Harmony WB_CMODE line so that OneLifeWB's output signal drives the A/D with the correct common mode voltage.

Figure 3-11. ONELife



Control and programming are done through a SPI interface from Harmony. Two supplies are required to power the IC, VRF_DIG_1.875V for SPI lines and VRF_2.775V for RF portions.

Harmony WCDMA_RX (U100)

The RX I an Q baseband signals are fed into the Sigma-Delta modulator of the Harmony. The Sigma-Delta modulator is an A/D converter that converts the I and Q baseband inputs to noise shaped 6-bit digital outputs. These outputs are then next decimated by a ratio of 3 using 3-stage cascaded comb type filters to a sampling rate of 15.36 MHz.

DC offset correction is performed next immediately to minimize the amount of delay in this mixed mode control loop to achieve rapid DC acquisition during *normal mode warmup sequences*. The DC offset correction unit has feedback to the OneLife-WB IC to be able to correct for DC offsets at the inputs to IF amplifier stage.

The matched selectivity filter is designed such that it provides the desired selectivity to meet adjacent channel and blocker specifications in the 2100 and 1800 MHz frequency bands.

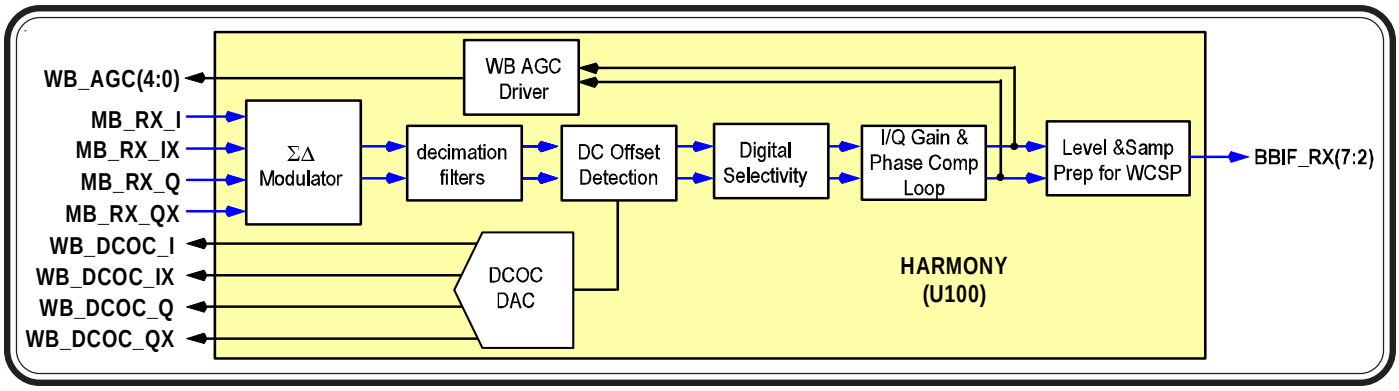
I/Q gain and phase imbalance equalization units located next in the lineup is used to correct for I/Q mismatches due to both the base station transmitter as well as the mobile device.

Next, the outputs of the I/Q gain equalization unit feed into the RF/IF AGC as well as the digital gain compensation control units. These outputs from the I/Q gain equalizer are used by the AGC unit for on-channel power detection. In addition, the AGC unit also receives off-channel power indication from a 2-bit SOS detector data bus from OneLife-WB IC. The on-channel and off-channel power levels are used by the RF/IF AGC unit to control internal and external LNA step attenuator stages as well as the variable gain PMA stage in OneLife-WB IC.

Two bit control lines are used to control each of the external LNA step attenuator stages. Alternately, a 1-bit control line is employed to control the internal LNA in the OneLife IC. In addition, a 5-bit parallel digital bus is employed to control the PMA variable gain control stage in OneLife-WB IC. The AGC unit also supplies the detected RSSI level to the external host device (e.g. POG IC) based upon the current RF, IF, and digital baseband gain control settings as well as the on-channel RSSI detected.

Following the I/Q gain equalization stage, a digital gain compensation unit is located next. The purpose of this gain compensation unit is to provide a 6-bit gain compensated output signal to the WCSP unit given that the input signal's dynamic range is 13 bits. The 15.36 MHz rate I and Q outputs are then interleaved in the BBIF (baseband interface) unit to generate the output I/Q data at a 30.72 MHz rate on a single 6-bit data bus to the external host device.

Figure 3-12. Harmony WCDMA RX (U300)



RF WCDMA Transmitter

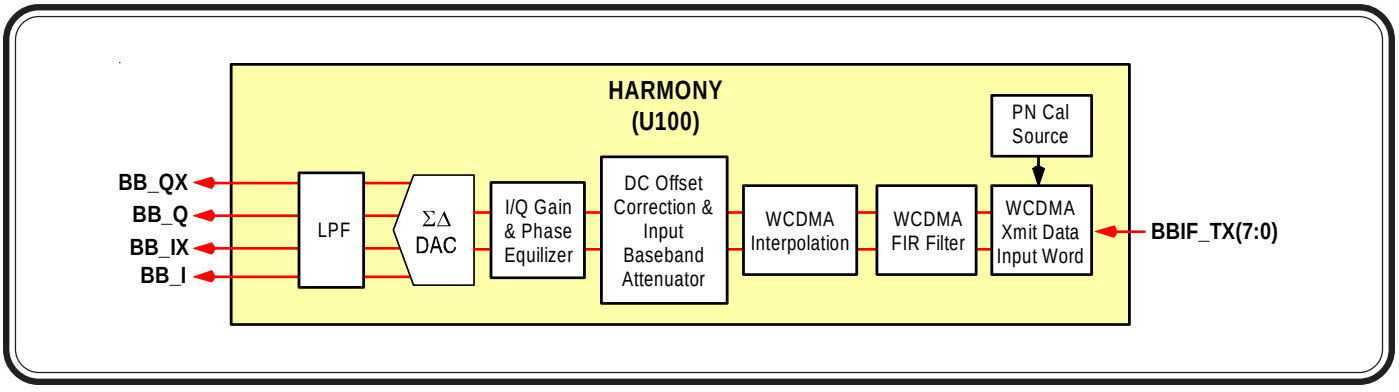
Harmony WCDMA TX (U100)

The Harmony provides pulse shaping and modulation of the 8-bit interleaved TX data coming from the POG. RF carrier suppression and baseband DC offset, I/Q gain and phase equilization will be then be performed. Finally, the I/Q signal is passed through a DAC and fed into the Rattler IC.

An 8-bit parallel interleaved data interface (BBIF_TX) is used to load the I and Q chip data from POG into the WCDMA signal path. Alternately, a PN calibration signal may also be loaded into this signal path for correction of baseband DC offsets and I/Q imbalances during transmitter warmup sequences. The parallel I and Q data from POG is first pulse shaped at a 7.68 MHz sampling rate using 31-tap SRRC FIR filters for the I and Q channels. These filters' outputs are then interpolated to a 30.72 MHz sampling rate using two stages of halfband interpolation filters.

The 12-bit outputs from the baseband pulse shaping and modulation system are fed into this DC and I/Q correction system. The specified 12 bit inputs first pass through the DC offset, I/Q phase and gain equalization blocks. The output samples from the gain equalizer are then fed into the sigma delta DACs at a higher sampling rate to minimize anti-aliasing filtering requirements. Following the DACs, there is an analog gain stage with 5 attenuation settings available for the baseband gain control system. Following this stage, a 2-pole passive filter and a 4th order Butterworth filter is employed in the quadrature signal path to eliminate the shaped noise from the sigma delta D/A's. The outputs of these reconstruction filters feed into the RF modulator IC (Rattler).

Figure 3-13. Harmony WCDMA TX (U300)



MC13786 (U401)

The MC13786 is an integrated I/Q modulator, IF and RF variable gain amplifier, UHF frequency synthesizer with a fully integrated VCO, image-reject upconverter mixer, and linear PA driver.

The synthesizer or phase locked loop (PLL) consists of a buffer amplifier, multi-modulus prescaler (divide by 4, 5, 6, and 7), a sixbit programmable post divider, reference divider, phase detector, and charge pump. The PLL uses a reference frequency of 15.36 MHz. One frequency synthesizer/VCO provides both the main and offset LO functions. The VCO operates over a frequency range of 2114 MHz to 2263 MHz and is fully integrated.

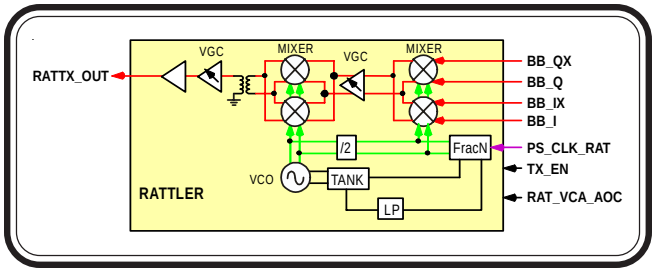
The I/Q Modulator consists of a quadrature generator and two Gilbert Cell active mixers. Using the offset LO and quadrature generator, the active mixers modulate the differential baseband I/Q signals onto a TXIF signal. Depending on the channel selection, the TXIF frequency will range from 274 MHz to 283 MHz.

From the active mixers, the TXIF signal is fed into a IF Variable Gain Amplified (IF VGA). The IF VGA has 70 dB of total typical gain control range and is controlled by the VGC line. The output of the VGA shall have a single pole bandpass tank circuit to provide attenuation to far-out noise.

The upconverter has an image-reject configuration so that the unwanted sideband is rejected to decrease the linearity requirements of the VGA stage. An input polyphase filter shall provide the necessary phase shift for the IR mixer. The TXIF signal is upconverted to a TX carrier frequency ranging from 1920MHz to 1980MHz. An on-chip copper balun shall provide the differential to single ended conversion necessary for the following stages.

The VGA provides a reduction in gain and current to optimize the TX lineup for lower output power levels. The PA driver amplifies the signal to provide sufficient drive for the radio power amplifier.

Figure 3-14. Rattler (U401)

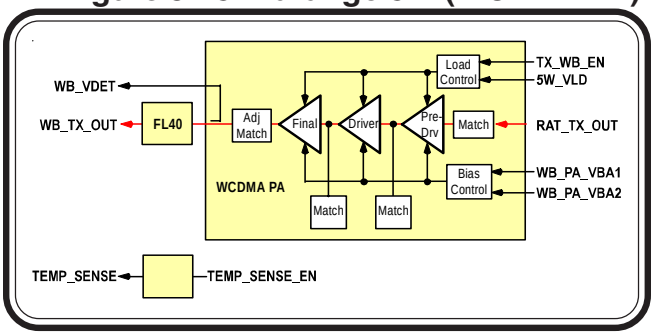


WCDMA PA (U850)

Durango5W is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 – 1980MHz. The nominal expected maximum gain is ~30dB.

A Motorola proprietary high power / low power efficiency enhancement load switch (5W_VLD) is included in the output match. VLD adjusts the output load for optimum efficiency from low power to high power out.

Figure 3-15. Durango 5W (WCDMA PA)



In conjunction with VLD, bias control (WB_PA_VBA1/WB_PA_VBA2) is performed between high and low power ranges.

The amplified WCDMA carrier is fed into a RF coupler device which has an integrated RF detector. An RF detect will pass through the Durango 9E3G (GSM PA) before being fed to the Harmony for power detection.

U880 is used to measure temperature. Its linear output is a voltage signal that corresponds to its physical device temperature. TEMP_SENSE is measured by PCAP and the MCU (POG) retreives the temperature readings every 5 seconds and passes it to the DSP (POG) so that the temperature compensation tables are updated.

The isolator provides a stable 50 ohm PA load. It also protects the PA from interfering with other frequency bands. Finally, it guards against IM products being produced by the transmitter and affecting receiver circuits.

RF Interface

Harmony

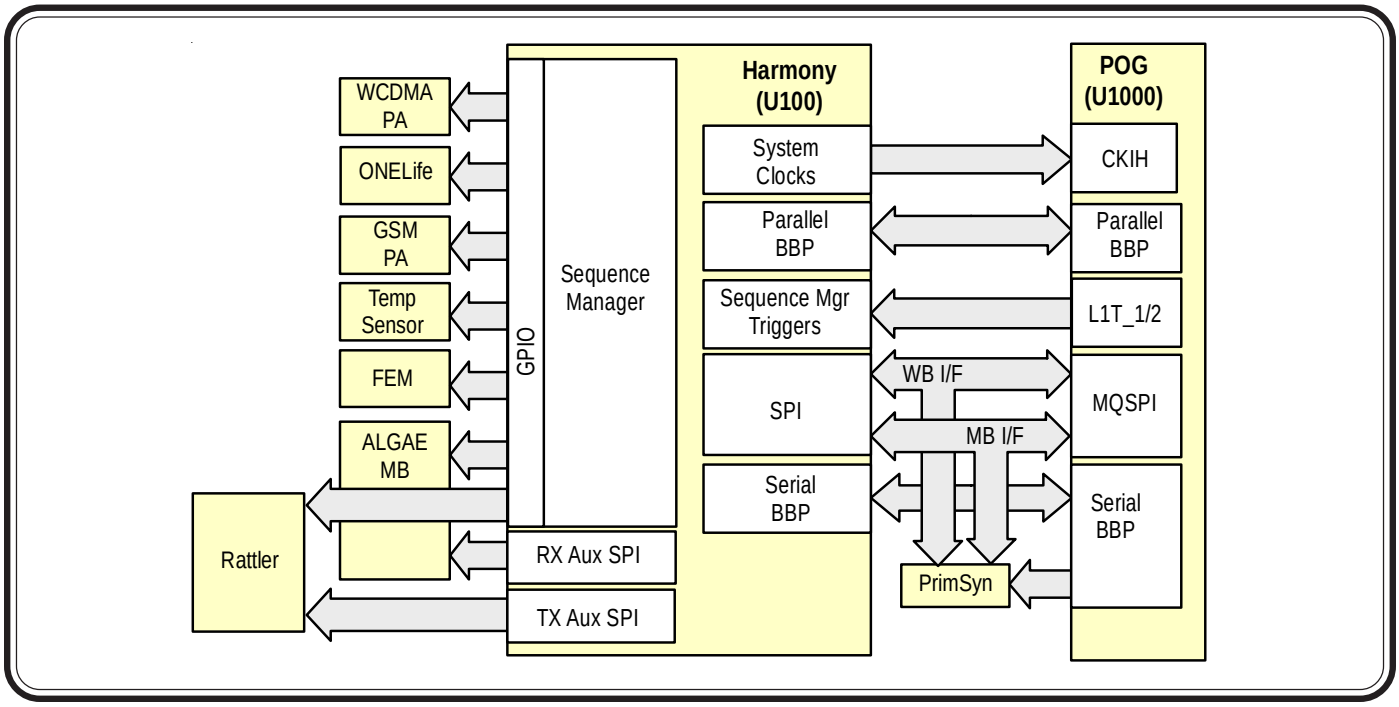
The Harmony IC is a mixed-signal transceiver backend IC intended to support GSM, EDGE and WCDMA services. It includes 2 receive paths: a medium-band path and a wideband path. The medium-band path is intended for GSM and EDGE and is configured to support VLIF receiver architecture. The wideband path is intended for WCDMA and is designed to operate in a direct conversion receiver architecture. Both of these receive signal paths are optimized for non-compressed mode. The transmitter path is designed to operate in a direct-launch transmitter architecture. The IC also includes dual clock synthesizers, as well as general support circuit such as sequence manager and SPI.

The Harmony IC and Base-Band (POG) IC interface consists of two independent sets of SPI lines (WB I/F, MB I/F); 2 chip-enable inputs, 2 clock inputs, 2 data inputs, and 2 data outputs. Harmony interfaces to the Base-band IC as a slave IC, however, it is also a master to two auxiliary ICs (Algae MB and Rattler) using two independent sets of SPI lines (TX AUX, RX AUX). The two auxiliary ICs are programmed by the Base-Band via Harmony.

In order to decrease the overall area required for controlling the sequences, a sequential access strategy was developed. The sequence manager would consist of controllers that would access an SRAM device sequentially. These controllers run of a set of programs that are pre loaded in to an SRAM memory device. In order to eliminate the need for a stack and interrupts each controller is dedicated to a single task. In the sequence manager there exists a controller per task, where the number of maximum tasks would be equivalent to the number of input TIMER lines.

A serial bus consisting of SDFS and SDRX will transmit the GSM RXI and RXQ data in 2's complement format to the Serial BBP module. The RXI and RXQ data will then be handled by the DSP integrated in the

Figure 3-16. RF Interface Block Diagram



POG. The Serial BBP module for TX is not used in this design.

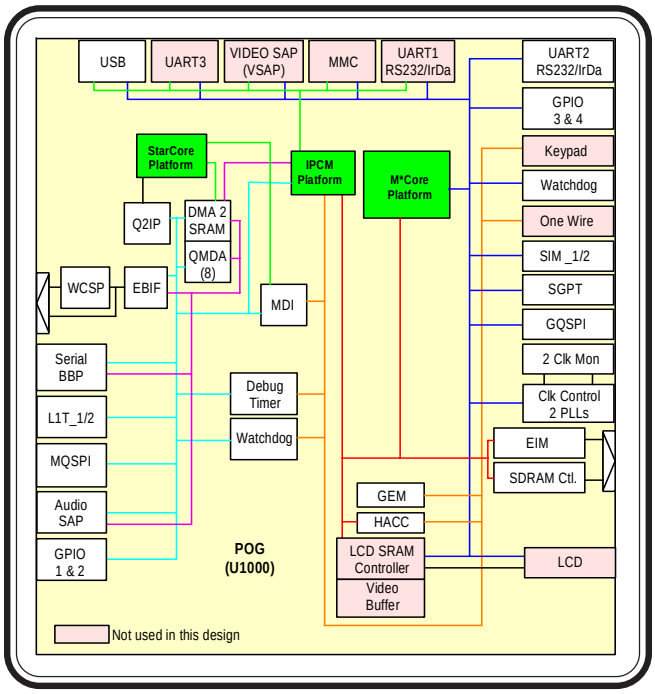
The WCDMA path receive path has a parallel BBP interface to send data to the Base Band processor. The interface is programmed to run at 15.36mhz. An 8-bit parallel interleaved data interface (Parallel BBP) is used to load the TX I and Q chip data from the external host processor (POG) IC into the WCDMA signal path of Harmony.

Baseband Electrical (Digital)

POG (U1000)

POG is the baseband processor IC of the 3G chipset solution. POG is crafted to provide a high performance embedded solution at low power for 3G mobile devices. POG is a TriCore processor IC integrating a powerful DSP core, a 32bit MCU RISC core with unified cache and a custom 32bit RISC engine for data movement across the processing domains.

Figure 3-18. POG Block Diagram



The DSP core is a high performance StarCore with four parallel ALUs, the SC140, with a novel Variable Length Execution Set (VLES) architecture which maximizes the execution of multiple instructions in a single clock cycle. The SC140 is assisted by 3G specific hardware accelerators and timers to optimize performance and power. As part of the 3G support, the Wideband CDMA Signal Processor (WCSP) module implements modem functions required by the CDMA subscriber unit in accordance with the 3GPP specifications.

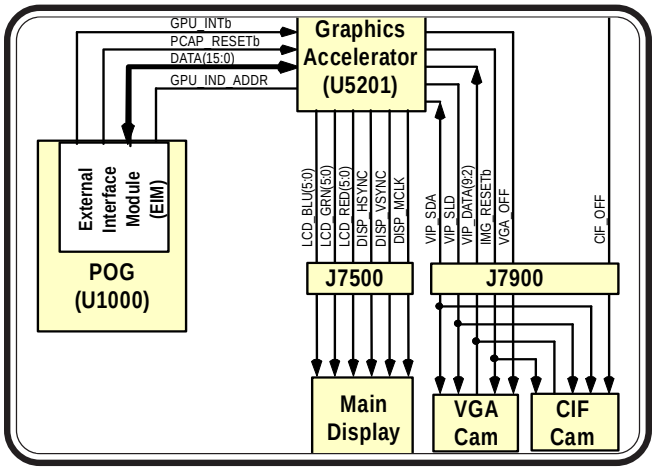
The 32bit MCU RISC core is the M*Core M341 designed for high performance and low power embedded systems. The M341 embodies an 16K unified cache, integer multiplier and MMU in support of virtual memory management OSes.

Data communication across the cores is handled by a flexible 32bit RISC machine, the Inter Processor Communication Module (IPCM). The IPCM supports flexible data flow between the MCU, DSP and the multimedia peripherals.

Graphics Accelerator

U5201 is a high performance, low power, Graphics/ Media Processor IC (GPU) that supports advanced multimedia applications for W-CDMA, UMTS, and GSM. This IC enables the user to capture, view, and share high quality images and video. A hardware-based

Figure 3-19. GPU Interface



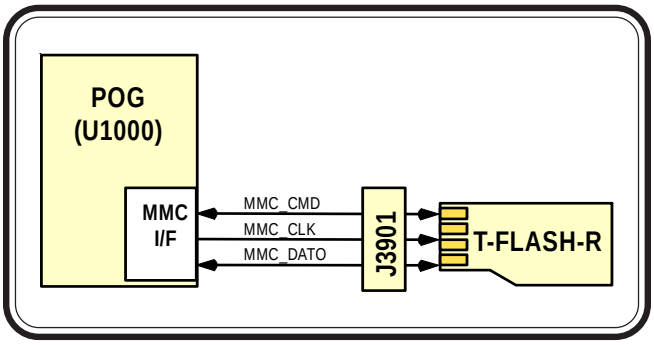
MPEG-4 encoder captures video at up to CIF resolution at 30fps. A hardware-based video decoder allows playback of the video recorded, or any other MPEG-4 clip or streaming video. A full hardware codec is uti-

lized for video conferencing – QCIF image size at up to 30fps. Support of VGA (680x480) resolution LCD at 16 and 18-bpp (with dithering) using only an embedded frame buffer and up to 3MP cameras with resolutions up to 2048x1536 image capture with a 10fps preview and 2MP cameras with a 15fps preview. The video processing engine is coupled with a JPEG encoder capable of encoding still images with 3MP resolution and a JPEG decoder capable of playback motion JPEG at up to 30fps at VGA resolution. The host interface bus provides an 8, 16, or 32-bit asynchronous interface that supports both direct and indirect addressing modes.

MMC/SD Flash Interface

The MMC/SD host controller provides an interface between the POG and Triflash-R memory card.

Figure 3-20. MMC Interface

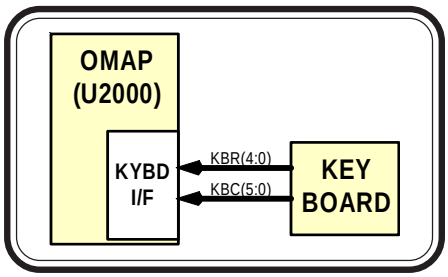


The MMC/SD host controller handles MMC/SD protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for syntactical correctness.

Keypad Interface

The keypad provides the primary physical user interface for the radio. The 5-way NAV joystick has a center keypress in addition to the four primary directions. White LED's will be used for backlighting. The keypad implementation to be used is the 2-contact, 1-pole keypad scanning architecture.

Figure 3-21. Keyboard Interface



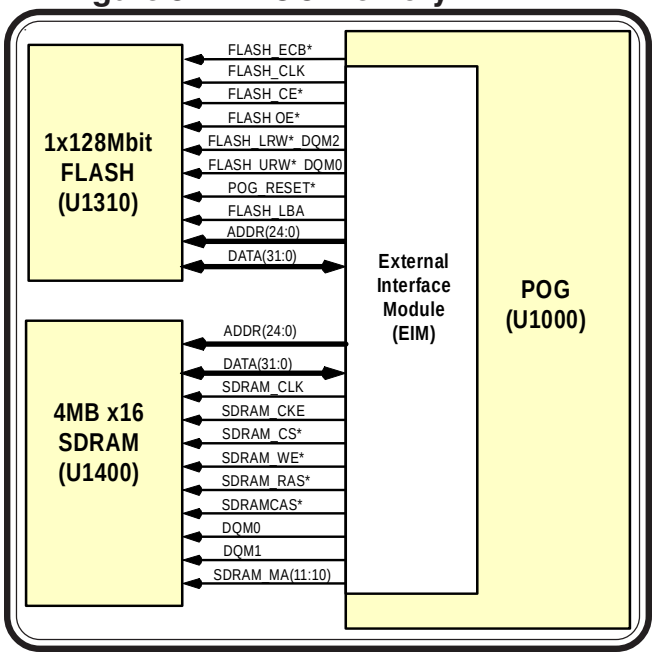
The Keypad Port (KPP) of POG decodes keypad presses. The Keypad Port is a 16-bit peripheral which is used for keypad matrix scanning. Keypad matrix uses 5 rows and 4 columns for key scanning. The KPP on POG can support up to an 8 x 8 row-by-column keypad matrix. The KPP will use a 32.768 KHz clock.

The Power/End key will not be part of the matrix but instead will connect directly to PCAP2.

POG Memory

The POG flash memory uses a 128 (128 Mbit) 1.8 Volt wireless memory which delivers high density flash memory in a single package. Individually erasable memory blocks are optimally sized for code and data storage. Four 16-Kword blocks and seven 64-Kword blocks are located in the parameter partition. The rest of the flash memory is divided into fifteen partitions of eight 64-Kword main blocks. By dividing the flash memory into partitions, program or erase can take place simultaneously during read operations. The device is available in a 56-ball vfBGA* package with 0.75 mm ball pitch.

Figure 3-22. POG Memory



The POG SDRAM device is a JEDEC standard SDRAM with 1.8V core supply, 1.8V I/O supply, four banks, and density of 4Mb x 16 (64 Mb). It is low power with special function support including partial array self refresh and temperature compensated refresh. It has a max frequency of 104MHz with CAS latency of three.

Power Supply Architecture

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are illustrated below.

Table 3-1. Power Distribution 1

Physical name	Logical name(s)	Voltage	Supplies
SW1	VLVIO_1.875	1.875	AP/BP Flash cores, AP flash I/O
SW2	Not Used	1.725	
SW3	VBOOST_5.5V	5.5	V10, Keypad backlights
V1	V1	1.875	Camera processors
V2	VA_2.775V	2.775	Audio
V3	Not Used	1.875	
V4	VPOG_VLVIO_1.875V	1.875	Low voltage I/O
V5	VHVIO_2.775	2.775	PCAP internal components
V6	VRF_TX_2.775V	2.775	Harmony, Rattler, RF TX
V7	Not Used	2.775	

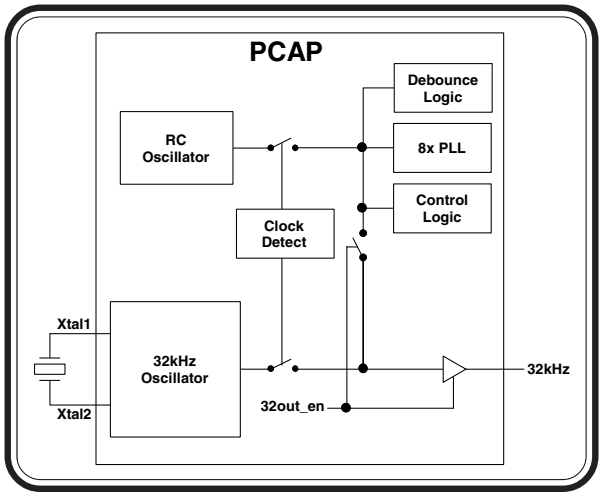
Table 3-2. Power Distribution 2

Physical name	Logical name(s)	Voltage	Supplies
V8	VMMC_2.775	2.775	MMC
V9	VRF_REF_2.475V	2.775	RF Reference
V10	VRF_HV_5V	5	RF HV
VAUX1	Not Used	2.775	
VAUX2	VRF_RX_2.775V	2.775	Harmony, Algae, RF RX
VAUX3	VCAM_2.6	2.6	Transflash
VAUX4	Not Used	3	
U3206	VMAIN_1.55V	1.55	POG Core

Clock Generation

PCAP can generate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Rainbow requires for optimal performance, therefore, an external 32.768kHz crystal is used.

Figure 3-24. RTC Clock



The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Audio Circuits

PCAP (U3000)

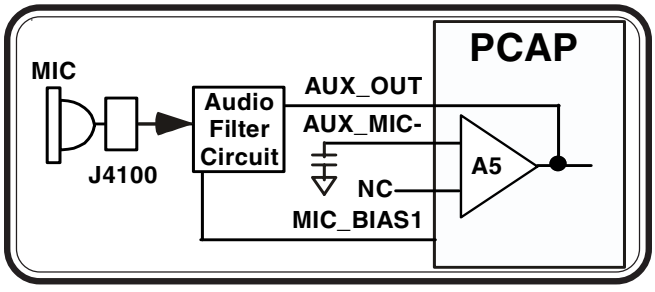
The PCAP2 IC is an ASIC intended for use in Colorado platform mobile phones. It integrates several functional modules:

- Voltage regulators of both linear and switching types designed for use in the Colorado power scheme
- Audio codecs and amplifiers
- RS-232 and USB transceivers
- LED controllers for the service light and display/keypad backlights
- Digital interfaces for two controlling processors.

TX Audio

The 3G termianl supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single-ended with respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

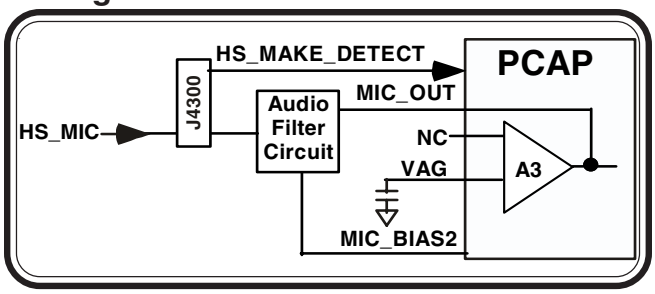
Figure 3-25. Internal Mic Path



The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 and R4101 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R4102 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

The headset microphone path is biased through R4396, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by using R4399 as a pull-up resistor and detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

Figure 3-26. Headset Mic Path



The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight/ALeft Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R34003 and R34002 respectively, and then connected to the transducer. Off the Speaker-path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

Figure 3-28. Handset Speaker Path

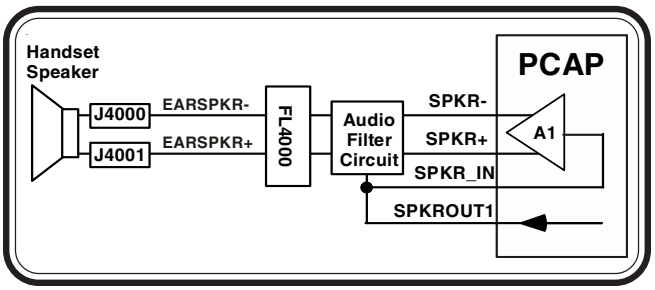
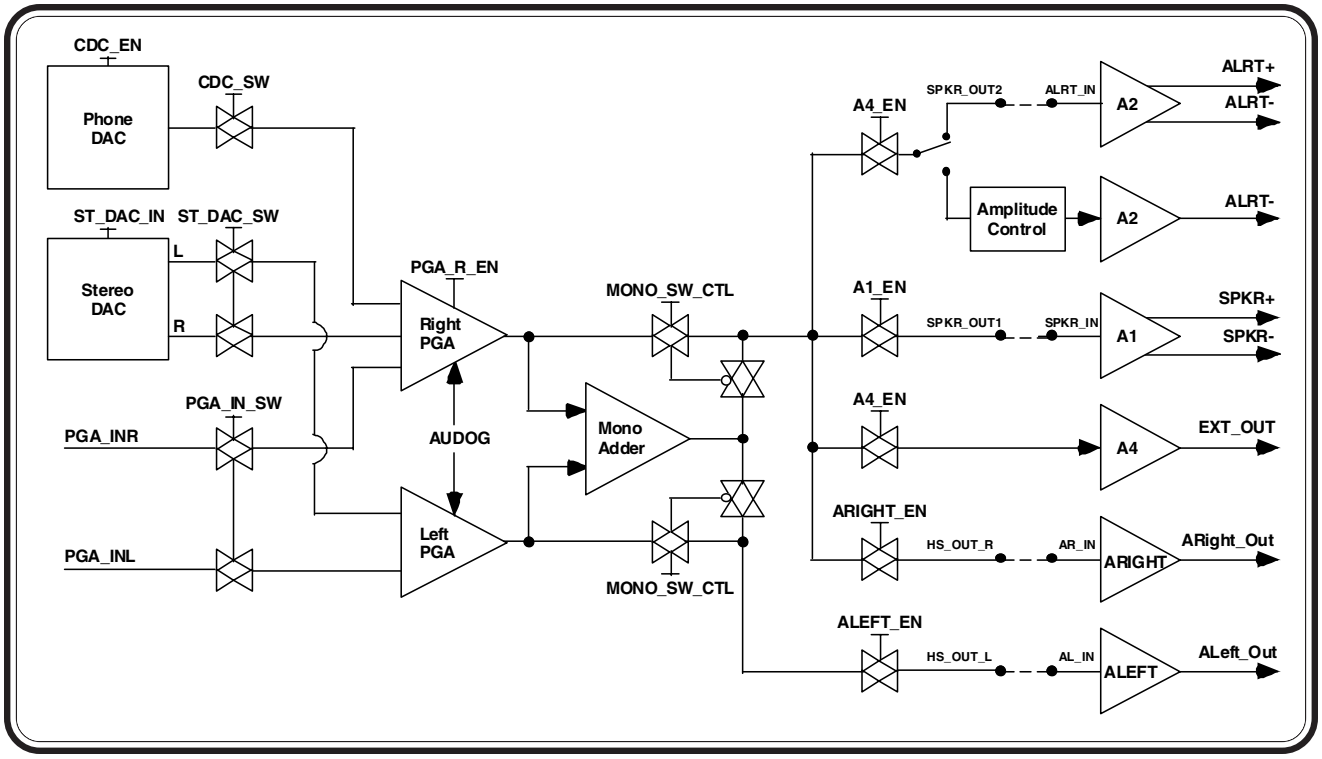
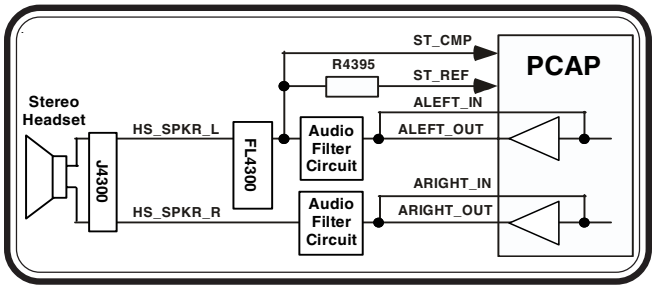


Figure 3-27. RX Audio Block



The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

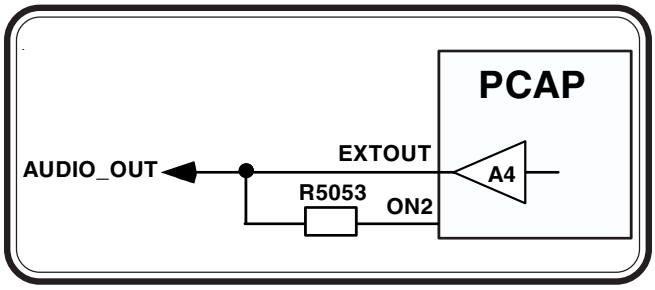
Figure 3-29. Headset Speaker Path



The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R34304 and C4306, R34303 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ARight_Out path, AL_IN is tapped off through C4354 for the inverting input of the audio amp ALEFT.

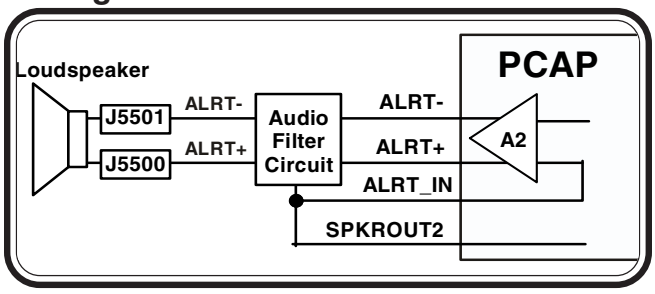
The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

Figure 3-30. External Speaker Path



The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

Figure 3-31. Alert Path



Battery Interface

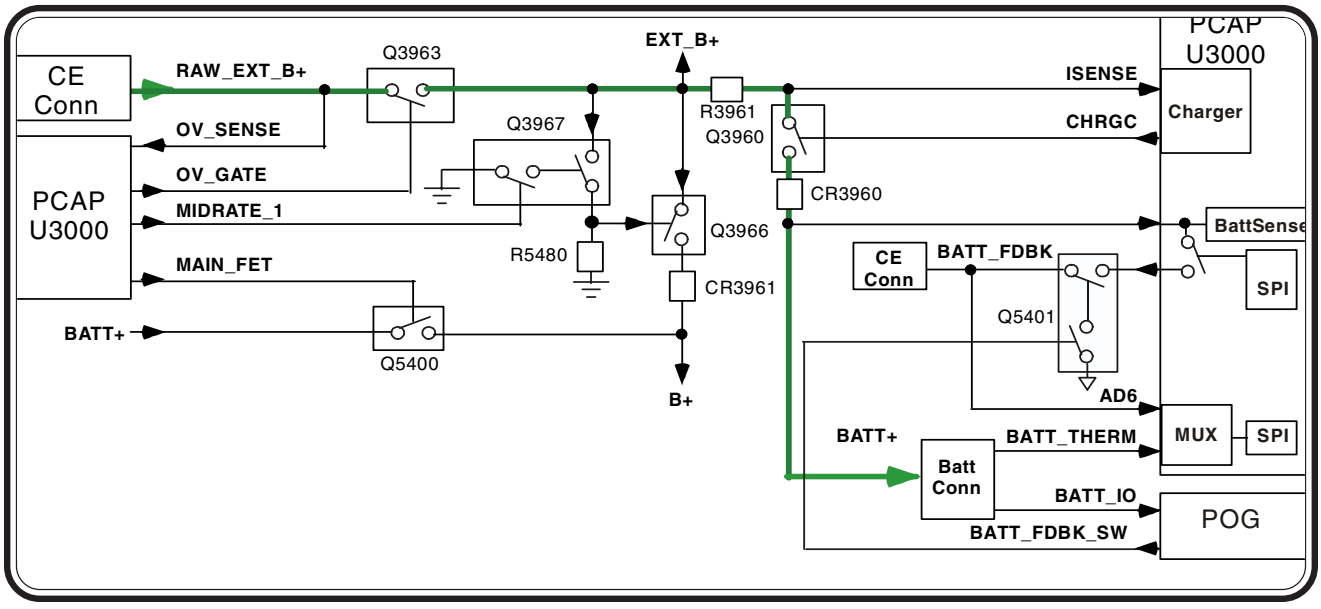
Batteries interface to the main transceiver board via a 4-pin connector (J5400). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q5400 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U3000) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J5000). During full rate charging, Q3966 is turned ON so that current can be supplied from the external source to B+. Q5400 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q3960. A sense resistor (R3961) provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J5000). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 3-32. Battery Interface Block



Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the A1000 UMTS/GSM handset.

Table 4-1. Electrical Parts List - B5400 to C1024

Reference Number	Part Number	Description
B5400	‘0988252L01	
C001	‘2113740A29	
C002	‘NOTPLACED	
C005	‘2113944A31	
C006	‘NOTPLACED	
C007	‘2113945B02	
C008	‘2113944A25	
C009	‘NOTPLACED	
C010	‘2113743N03	
C011	‘NOTPLACED	
C012	‘NOTPLACED	
C013	‘NOTPLACED	
C014	‘2186463Z07	
C015	‘2113743N40	
C016	‘2113743N40	
C017	‘2113743N40	
C018	‘2113743N40	
C019	‘2113743N40	
C100	‘2113945B02	
C1002	‘2113946K02	
C1003	‘2113946K02	
C1006	‘2113946K02	
C1007	‘2113946K02	
C101	‘2113945B02	
C1010	‘2113946K02	
C1011	‘2113946K02	
C1012	‘2113946K02	
C1013	‘2113946K02	
C1014	‘2113946K02	
C1015	‘2113946K02	
C1016	‘2113946K02	
C1017	‘2113946K02	
C1018	‘2113946K02	
C1020	‘2113946K02	
C1021	‘2113946K02	
C1022	‘2113946K02	
C1023	‘2113946K02	
C1024	‘2113946K02	

Table 4-2. Electrical Parts List - C1025 to C3201

Reference Number	Part Number	Description
C1025	‘2113946K02	
C1026	‘2113946K02	
C1027	‘2113946K02	
C1028	‘2113946K02	
C1029	‘2113946K02	
C1030	‘2113946K02	
C1031	‘2113946K02	
C1032	‘2113946K02	
C1033	‘2113946K02	
C1034	‘2113946K02	
C1035	‘2113946K02	
C1036	‘2113946K02	
C1037	‘2113946K02	
C1038	‘2113946K02	
C1039	‘2113946K02	
C1049	‘2113946K02	
C1050	‘2113946K02	
C1161	‘NOTPLACED	
C1301	‘2113946K02	
C1303	‘2113946K02	
C1304	‘2113946K02	
C1306	‘2113946K02	
C1307	‘2113946K02	
C1308	‘2113946K02	
C1402	‘2113946B04	
C1403	‘2113946K02	
C1404	‘2113946B04	
C1405	‘2113946K02	
C1406	‘2113946K02	
C1407	‘2113946B04	
C1408	‘2113946B04	
C1409	‘NOTPLACED	
C3000	‘2113928C12	
C3001	‘2113928C12	
C3002	‘2113946K02	
C3003	‘NOTPLACED	
C3050	‘2113946D02	
C3100	‘2113928C12	
C3101	‘2113928C12	
C3102	‘2113946K02	
C3150	‘2113946D02	
C3151	‘2113944A31	
C3200	‘2113743N44	
C3201	‘2113928C12	

Table 4-3. Electrical Parts List - C3202 to C4105

Reference Number	Part Number	Description
C3202	‘2113743N54	
C3204	‘2113946K02	
C3205	‘2113928C12	
C3209	‘2113946D02	
C3300	‘2113946D02	
C3350	‘2113928C04	
C3400	‘2113928Z11	
C3403	‘NOTPLACED	
C3450	‘2113946D02	
C3550	‘2113946D02	
C3560	‘2113928Z11	
C3563	‘NOTPLACED	
C3600	‘2113946D02	
C3651	‘2113946K02	
C3654	‘2113946D02	
C3801	‘2113946D02	
C3850	‘2113946D02	
C3851	‘2113946D02	
C3900	‘2113945B02	
C3901	‘2113945B02	
C3906	‘2113944A31	
C3910	‘2113946K02	
C3911	‘NOTPLACED	
C3951	‘2113928C04	
C3960	‘2113928C12	
C3961	‘2113928C12	
C3962	‘2113946K02	
C3963	‘2113743N16	
C3964	‘2113743N16	
C3965	‘2113743N16	
C3983	‘2113944A25	
C3984	‘2113944A25	
C4000	‘2113743N40	
C4001	‘2113743L21	
C4002	‘2113946B04	
C4003	‘2113743N40	
C401	‘2187906N01	
C402	‘NOTPLACED	
C4100	‘2113946B04	
C4101	‘NOTPLACED	
C4102	‘NOTPLACED	
C4103	‘2113944A31	
C4104	‘2113944A25	
C4105	‘2113946D02	

Table 4-4. Electrical Parts List - C4203 to C514

Reference Number	Part Number	Description
C4203	‘2113944A31	
C4204	‘2113944A31	
C4205	‘2113944A25	
C4206	‘2113944A25	
C4208	‘2113944A31	
C4209	‘2113944A31	
C4210	‘2113928C04	
C4211	‘2113944A31	
C4212	‘2113743L13	
C4213	‘2113946B04	
C4214	‘2113944A27	
C4215	‘2113944A31	
C4300	‘2113944A31	
C4301	‘2113945B02	
C4302	‘2113945B02	
C4304	‘2113946B04	
C4305	‘2113946K02	
C4306	‘2113928Z11	
C4308	‘2113944A31	
C4356	‘2113928Z11	
C4392	‘2113743N40	
C4393	‘2113743N40	
C4400	‘2113946D02	
C4401	‘2113946B04	
C4402	‘2113944A31	
C4403	‘2113946D02	
C4500	‘NOTPLACED	
C4501	‘2113946B04	
C4502	‘2113946D02	
C4503	‘2113946B04	
C4504	‘NOTPLACED	
C4550	‘2113743L33	
C4551	‘2113743E20	
C4901	‘2113946B04	
C4910	‘2113946K02	
C5000	‘2113946K02	
C5002	‘2113947B05	
C506	‘2113928C04	
C507	‘2113928C04	
C510	‘2113741A45	
C511	‘2113741A45	
C512	‘2113743L21	
C513	‘2113743L21	
C514	‘2113944A31	

Table 4-5. Electrical Parts List - C515 to C7907

Reference Number	Part Number	Description
C515	‘2113946D02	
C516	‘2113743N40	
C518	‘2113946D02	
C520	‘2113743N40	
C5200	‘2113944A25	
C5201	‘2113944A25	
C5202	‘2113946B04	
C5203	‘2113946D02	
C5204	‘2113946D02	
C5208	‘2113946K02	
C5209	‘2113946K02	
C521	‘2113743N40	
C5210	‘2113946K02	
C5211	‘2113946K02	
C5212	‘2113946K02	
C5213	‘2113946K02	
C5214	‘2113946K02	
C5221	‘2113946K02	
C5222	‘2113946K02	
C5223	‘2113946K02	
C5225	‘2113946K02	
C5226	‘2113946K02	
C5228	‘2113946K02	
C5234	‘2113946K02	
C5235	‘2113946K02	
C5236	‘2113946K02	
C5237	‘2113946K02	
C5239	‘2113946K02	
C5240	‘2113946K02	
C5254	‘2113946K02	
C5255	‘2113946K02	
C5295	‘NOTPLACED	
C5296	‘NOTPLACED	
C5400	‘2113928C04	
C5402	‘2113946K02	
C5501	‘NOTPLACED	
C5502	‘NOTPLACED	
C5503	‘2113944A25	
C5505	‘NOTPLACED	
C7554	‘2113944A26	
C7903	‘2187893N01	
C7904	‘NOTPLACED	
C7906	‘NOTPLACED	
C7907	‘NOTPLACED	

Table 4-6. Electrical Parts List - C7916 to C859

Reference Number	Part Number	Description
C7916	‘2113743L37	
C7917	‘NOTPLACED	
C7920	‘NOTPLACED	
C7921	‘NOTPLACED	
C7923	‘2113946K02	
C7924	‘2113946K02	
C7925	‘2113946K02	
C7926	‘2113946K02	
C7927	‘2113946K02	
C7928	‘2113944A25	
C7929	‘2187893N01	
C7930	‘2113928A01	
C7931	‘2113928A01	
C7932	‘2113928A01	
C7933	‘2113928A01	
C7934	‘2113743N15	
C800	‘2187906N01	
C801	‘2113743N40	
C802	‘2187906N01	
C803	‘2113928A01	
C804	‘2113743N40	
C805	‘2113743N40	
C806	‘2113928A01	
C807	‘NOTPLACED	
C808	‘NOTPLACED	
C809	‘2113944A25	
C810	‘2113944A25	
C812	‘2113928C12	
C813	‘NOTPLACED	
C814	‘2113944A25	
C815	‘NOTPLACED	
C816	‘NOTPLACED	
C817	‘2113743N03	
C818	‘2113743N03	
C850	‘2113928C04	
C851	‘2113946D02	
C852	‘2113946D02	
C853	‘2113946D02	
C854	‘2113743N40	
C855	‘NOTPLACED	
C856	‘2113945B02	
C857	‘2113944A25	
C858	‘2113944A26	
C859	‘NOTPLACED	

Table 4-7. Electrical Parts List - C881 to E401

Reference Number	Part Number	Description
C881	‘2113945B02	
C882	‘2113945B02	
C901	‘2113928C04	
C902	‘2113928C04	
C903	‘2113928C04	
C904	‘2113928C04	
C9117	‘2113946K02	
C9118	‘2113946K02	
C9119	‘2113947B05	
C9120	‘2113947B05	
C9121	‘2113947B05	
C9125	‘2113945B02	
C9126	‘2113945B02	
C9127	‘2113945B02	
C9128	‘2113743N40	
C9129	‘2113944A31	
C9130	‘2113944A25	
C9131	‘2113944A25	
C9132	‘2113945B02	
C9133	‘NOTPLACED	
C9134	‘2113945B02	
C9135	‘2113945B02	
C9136	‘2113945B02	
C9137	‘2113945B02	
C9138	‘2113928C12	
C9139	‘2113743N40	
CR3000	‘4809924D18	
CR3900	‘4813832M85	
CR5401	‘4809948D42	
CR5500	‘4813832M85	
D3100	‘4809653F07	
D3961	‘4809653F07	
D3962	‘4809653F07	
D5000	‘NOTPLACED	
D7500	‘NOTPLACED	
D7501	‘NOTPLACED	
D7900	‘4813832M85	
D7901	‘4813832M85	
D7902	‘4813832M85	
D7903	‘4813832M85	
D7904	‘4889615N02	
D7905	‘4809948D37	
E400	‘SHORT_RES0201	
E401	‘SHORT_RES0201	

Table 4-8. Electrical Parts List - E402 to L3000

Reference Number	Part Number	Description
E402	‘SHORT_RES0201	
E403	‘2409154M99	
E405	‘SHORT_RES0201	
E406	‘SHORT_RES0201	
E407	‘SHORT_RES0201	
E408	‘SHORT_RES0201	
E409	‘SHORT_RES0201	
E412	‘SHORT_RES0201	
E801	‘SHORT_RES0201	
E900	‘SHORT_RES0201	
E901	‘SHORT_RES0201	
E9128	‘SHORT_RES0201	
FL002	‘9109674L20	
FL003	‘9109674L21	
FL004	‘9109674L17	
FL005	‘9109239M38	
FL4000	‘4889526L03	
FL4300	‘4889526L04	
FL4301	‘4889526L01	
FL4302	‘4889526L01	
FL500	‘9188695K05	
J3000	‘TPSM0_50X0_70	
J3001	‘TPSM0_50X0_70	
J3901	‘3989655N02	
J4000	‘TPSM0_50X0_40	
J4001	‘TPSM0_50X0_40	
J402	‘3989625N01	
J403	‘3989625N01	
J4100	‘NOTPLACED	
J4201	‘3988194N01	
J4300	‘0989675N03	
J5000	‘0987636K06	
J5100	‘0987817K06	
J5400	‘3987697Y02	
J5500	‘3904824R01	
J7500	‘0988866N01	
J7900	‘0988866N01	
L001	‘NOTPLACED	
L002	‘2488090Y09	
L003	‘2488090Y09	
L005	‘2488090Y06	
L009	‘NOTPLACED	
L014	‘2487319K01	
L3000	‘2588079Y03	

Table 4-9. Electrical Parts List - L3100 to R1101

Reference Number	Part Number	Description
L3100	‘2485063F02	
L3206	‘2588079Y03	
L3207	‘2409377M03	
L401	‘2409154M99	
L4399	‘2409646M13	
L4400	‘2409646M13	
L5201	‘2409377M17	
L7925	‘2488090Y19	
L811	‘2409154M07	
M7900	‘3903537C01	
M7901	‘3903537C01	
MC1300	‘2113946K02	
MC1302	‘2113946K02	
MC1305	‘2113946K02	
MC1310	‘2113946K02	
MR1010	‘0613952R66	
MR1011	‘0613952R66	
MR1300	‘0613952R66	
MR1303	‘0613952R66	
N001	‘0987378K01	
Q3200	‘NOTPLACED	
Q3403	‘4804616R01	
Q3560	‘4804616R01	
Q3652	‘4809579E02	
Q3960	‘4862830F01	
Q3961	‘4862830F01	
Q3963	‘4862830F01	
Q3964	‘4862830F01	
Q5001	‘5109817F58	
Q5100	‘4813824A17	
Q5401	‘NOTPLACED	
R002	‘0662057M86	
R003	‘0613952Q80	
R004	‘0613952R66	
R006	‘0613952R66	
R007	‘0613952R66	
R008	‘0613952R66	
R015	‘0613952R01	
R1032	‘0613952R66	
R1038	‘NOTPLACED	
R1061	‘0613952R66	
R1062	‘0613952R66	
R1064	‘0613952R66	
R1101	‘0613952R01	

Table 4-10. Electrical Parts List - R1160 to R411

Reference Number	Part Number	Description
R1160	‘0613952R66	
R1167	‘0613952R66	
R1400	‘NOTPLACED	
R1401	‘0613952R66	
R1402	‘NOTPLACED	
R1403	‘0613952R66	
R1404	‘0613952R66	
R1405	‘0613952R66	
R3001	‘0687874L02	
R3100	‘0613952R66	
R3101	‘0687874L02	
R3150	‘0613952R66	
R3179	‘NOTPLACED	
R3180	‘0613952R66	
R3200	‘NOTPLACED	
R3201	‘0613952R66	
R3205	‘NOTPLACED	
R3210	‘0662057V41	
R3211	‘0662057V29	
R3650	‘0613952Q77	
R3651	‘0613952Q33	
R3652	‘0613952Q33	
R3654	‘0613952R66	
R3900	‘0613952R01	
R3901	‘0613952R22	
R3902	‘0613952R66	
R3903	‘0613952R01	
R3904	‘0613952R01	
R3905	‘0613952R01	
R3906	‘0662057V17	
R3907	‘0613952N01	
R3960	‘0687874L01	
R3961	‘0688044N02	
R3962	‘0613952Q91	
R3963	‘0613952R32	
R3965	‘0613952R66	
R4000	‘0613952R09	
R4008	‘0613952R66	
R4009	‘0613952R66	
R402	‘0613952R66	
R403	‘0613952R66	
R404	‘0613952Q39	
R4100	‘0613952Q89	
R411	‘0613952R66	

Table 4-11. Electrical Parts List - R4300 to R5501

Reference Number	Part Number	Description
R4300	‘0613952R17	
R4301	‘0613952R17	
R4302	‘0613952Q89	
R4400	‘0613952Q49	
R4401	‘0613952Q73	
R4402	‘0662057N06	
R4550	‘0613952Q91	
R4551	‘0613952R66	
R4552	‘0613952R66	
R4901	‘0613952R17	
R4902	‘0613952R35	
R4910	‘0662057V41	
R4911	‘0662057V27	
R500	‘0613952Q77	
R5000	‘0613952R25	
R5001	‘0613952R17	
R501	‘0613952Q77	
R502	‘0613952R66	
R503	‘0613952R66	
R504	‘0613952R66	
R505	‘0613952R66	
R5100	‘0613952R01	
R5101	‘0662057M03	
R5102	‘0613952R66	
R5103	‘NOTPLACED	
R5200	‘0613952Q33	
R5203	‘0613952R25	
R5204	‘0613952R66	
R5205	‘0613952R66	
R5206	‘0613952R66	
R5207	‘0613952Q80	
R5208	‘NOTPLACED	
R5210	‘0613952R25	
R5211	‘0613952R25	
R5212	‘0613952R25	
R5213	‘0613952R25	
R5214	‘0613952R25	
R5216	‘NOTPLACED	
R5299	‘0613952P30	
R5401	‘0613952Q89	
R5402	‘0613952Q49	
R5405	‘NOTPLACED	
R5406	‘0613952R66	
R5501	‘0613952Q91	

Table 4-12. Electrical Parts List - R5502 to R910

Reference Number	Part Number	Description
R5502	‘0613952R66	
R5503	‘0613952R66	
R5504	‘0613952R66	
R5505	‘0613952R66	
R7902	‘0613952R66	
R7903	‘0613952R66	
R7904	‘0613952R66	
R7912	‘0613952Q25	
R7915	‘0613952R01	
R7920	‘0613952B92	
R7921	‘0613952B92	
R7922	‘0613952N01	
R7923	‘0613952R01	
R7924	‘0613952R25	
R7925	‘0613952R66	
R7926	‘0613952R25	
R7927	‘0613952R66	
R7928	‘0662057V11	
R7929	‘0662057V43	
R7930	‘0613952N01	
R801	‘0613952R66	
R802	‘0613952R66	
R803	‘NOTPLACED	
R805	‘0662057M43	
R810	‘0613952Q49	
R812	‘0613952R66	
R818	‘0613952R66	
R819	‘0662057M52	
R820	‘0613952R66	
R821	‘0662057M52	
R830	‘NOTPLACED	
R851	‘0613952R66	
R855	‘0613952R66	
R858	‘NOTPLACED	
R859	‘NOTPLACED	
R882	‘0613952Q65	
R901	‘0613952R66	
R903	‘0613952R66	
R904	‘0613952R66	
R906	‘0613952R66	
R907	‘0613952R66	
R908	‘0613952R66	
R909	‘NOTPLACED	
R910	‘0613952R66	

Table 4-13. Electrical Parts List -R911 to VR4301

Reference Number	Part Number	Description
R911	'NOTPLACED	
R912	'0613952R66	
S1	'4087635K01	
S2	'4087635K01	
SH1	'2603523B01	
SH2	'2603524B01	
SH3	'2603525B01	
SH4	'2603526B01	
SH5	'2603527B01	
SH6	'2603528B01	
SH7	'2603529B01	
SW5130	'4087635K01	
T1	'5885949K04	
T2	'5885949K06	
T3	'5885949K06	
U001	'5109944C61	
U002	'4889729N03	
U1000	'5199154K05	
U1019	'5109522E14	
U1020	'5109522E82	
U1161	'NOTPLACED	
U1300	'5199171J01	
U1310	'5199171J01	
U1400	'5109509A67	
U3000	'5185941F02	
U3200	'5188128Y01	
U3650	'5164751E01	
U3651	'NOTPLACED	
U401	'5188450M21	
U500	'5188450M23	
U5000	'4889526L01	
U5001	'4889526L02	
U5201	'5187911Y01	
U5253	'5164751E01	
U5254	'5164751E01	
U5255	'5164751E01	
U800	'5188220Y01	
U850	'5189552N01	
U880	'5109768D08	
U900	'4889717N03	
U9129	'TPSM0_508	
U9130	'5103670B03	
VR4300	'4809948D44	
VR4301	'4809788E08	

Table 4-14. Electrical Parts List - VR4302 to Y3982

Reference Number	Part Number	Description
VR4302	‘4809788E08	
VR5000	‘4813832M85	
VR5001	‘4809948D44	
VR5002	‘4809948D44	
VR5003	‘4813830C29	
VS4200	‘4809788E06	
VS4201	‘4809788E06	
VS5001	‘4886193U03	
VS5002	‘4813832M84	
VS5400	‘4809788E06	
Y100	‘4809718L24	
Y3982	‘4809995L20	