GSM Service Support
Training - Documentation - Engineering

C115

Level 3
Circuit Description
07 / 30 / 04
V1.0

Index

C115 Level 3 Circuit Description

1 Receive

1.1 Band selection

The received signal is received through the antenna. Received GSM RF signal enters the unit at the antenna. C144, C145, and C146 components provide antenna matching. The RF signal then enters mechanical 50-ohm RF connector JP1. This RF connector is used for phasing, testing. From A1 the RF signal enters U17 (TX/RX antenna switch) on **Pin 3** (**ANT**), where through control voltages the RX path is isolated from the TX path. The following voltages control the RF Switch:

VC1 put low and **VC2** put high, these signals put the phone into TX GSM900/850 Mode (from U7 **Pin K13 and K14**).

VC1 put high and **VC2** put low, these signals put the phone into TX DCS1800/PCS1900 Mode.

VC1 and VC2, these signals put the phone into RX Mode when both Low.

The low band RX output from U17 (**Pin 11**) is connected to the SAW filter F2. The high band RX output from U17 (**Pin 1**) is connected to the SAW filter F3. The RF signal of the selected frequency band is then sent to single ended input to differential output to the front end IC U15 (Rita).

1.2 Frontend

The receiver block diagram in the Rita IC U15 is shown in **Figure 1**. Three LNAs are provided to support the receiver frequency bands. The LNAs drive an AGC current steering stages that feed integrated transformer matching network. The transformer drives the quadrature mixers that convert the RF signal to baseband, DCR(Direct Conversion Receiver), quadrature I and Q signals. The signal then passes through the baseband amplification and 3-cascaded low pass filters into an analog to digital converter in the Iota IC.

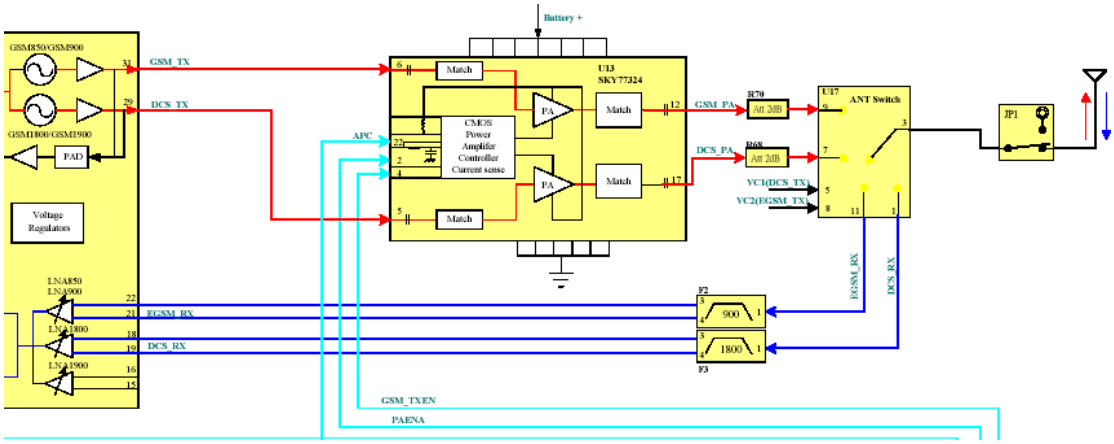


Figure 1 Receiver Path

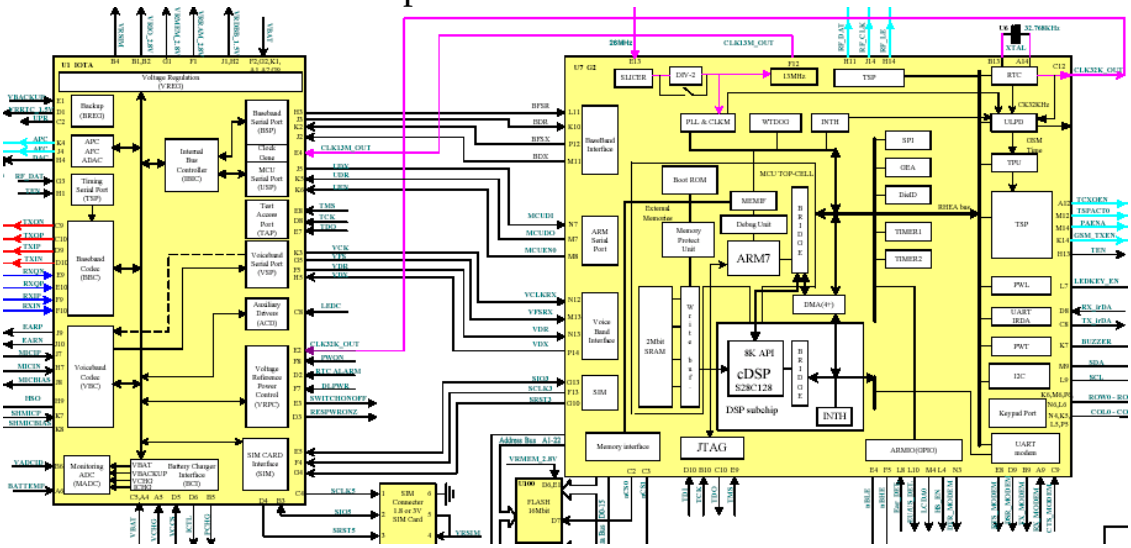


Figure 2 Iota and CalpysoLite_G2 IC

1.3 Demodulation

The **RXI** and **RXQ** signals are feed in the ΣΔ. Dual ADC stage on Iota IC U1 (**Pin F9, F10, E9 and E10)**. The baseband codec (BBC) is composed of a baseband uplink path (BUL) and a baseband downlink path (BDL).

The BDL path includes two identical circuits for processing the analog baseband I and Q components generated by the RF circuits. The first stage of the BDL path is a continuous second-order antialiasing filter that prevents aliasing of out-of-band frequency components due to sampling in the ADC. This filter serves also as an adaptation stage between external and on-chip circuitry.

The antialiasing filter is followed by a fourth-order ΣΔ modulator that performs analog-to-digital conversion at a sampling rate of 6.5 MHz. The ADC provides 2-bit words to a digital filter that performs the decimation by a ratio of 24 to lower the sampling rate to 270.833 kHz. The ADC also provides channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM specification.

The BDL path includes an offset register, in which the value representing the channel dc offset is stored. This value is subtracted from the output of the digital filter before transmitting the digital samples to the CalpysoLite_G2 IC U7 (DSP) via the BSP. Upon reset, the offset register is loaded with 0s; its content is updated during the calibration process.

The typical sequence of burst reception consists of:

1. Power up the BDL path
2. Perform an offset calibration
3. Convert and filter the I and Q components and transmit digital samples

Timing of this sequence is controlled via the TSP, which receives serial real-time control signals from the TPU of the CalpysoLite_G2 IC U7 (DSP) device. Three real-time signals control the transmission of a burst: **BDLON**, **BDLCAL**, and **BDLENA**. Each signal corresponds to a time window.

BDLON high sets the BDL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. **BDLCAL** enables the offset calibration window. Two offset calibration modes are possible and are selected by the state of bit 9 (**EXTCAL**) of the baseband codec control register. When **EXTCAL** is 0, the analog inputs are disconnected from the external world and internally shorted. The result of conversion done in this state is stored in the

offset register. When **EXTCAL** is 1, the analog input remains connected to external circuitry, and the result of conversion, including in this case internal offset plus external circuitry offset, is stored in the offset register. The duration of the calibration window depends mainly on the settling time of the digital filter.

Data conversion starts with the rising edge of the **BDLENA** signal; however, the first eight I and Q samples are not transmitted to the CalpysoLite_G2 IC U7 (DSP), since they are meaningless due to the group delay of the digital filter. The rising edge of **BDLENA** is also used by the IBIC to affect the transmit path of the BSP to the BUL path during the entire reception window. At the falling edge of **BDLENA**, the conversion in progress is completed and samples are transmitted before stopping the conversion process. Finally, **BDLON** low sets the BDL path in power-down mode.

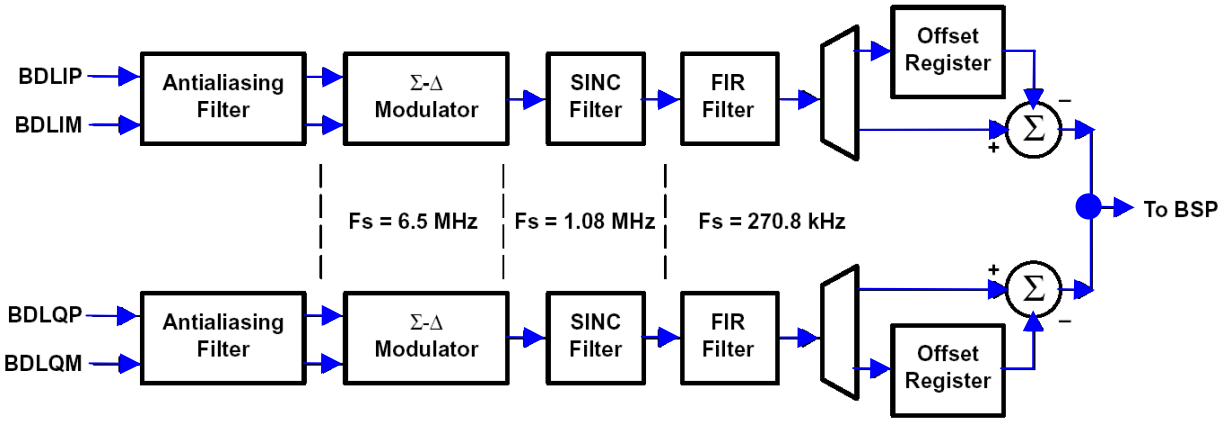


Figure 3 Baseband Downlink Block Diagram

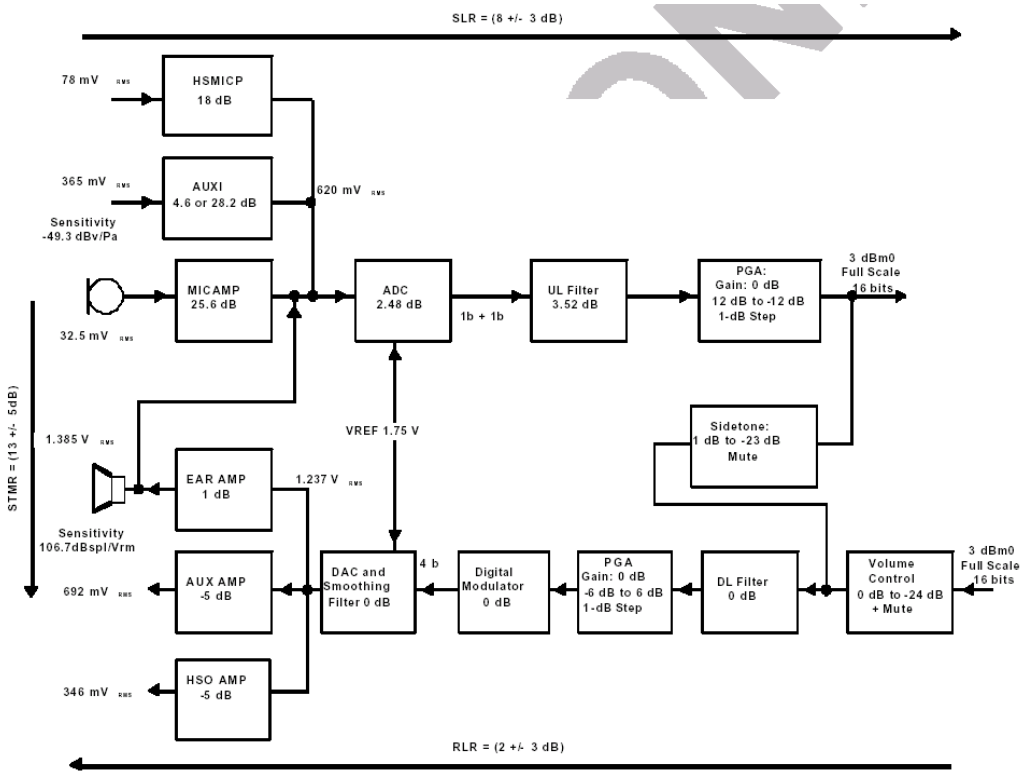


Figure 4 Voice Codec Block Diagram

1.4 Audio

The voice codec circuitry processes analog audio components in the uplink path and applies this signal to the voice signal interface for eventual baseband modulation. In the downlink path, the codec circuitry changes voice component data received from the voice serial interface into analog audio. The following paragraphs describe these uplink/downlink functions in more details.

1.4.1 Voice Downlink Patch

The VDL path receives speech samples at the rate of 8 kHz from the CalpysoLite_G2 IC U7 (DSP) via the VSP and converts them to analog signals to drive the external speech transducer.

The digital speech coming from the CalpysoLite_G2 IC U7 (DSP) is first fed to a speech digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate from 8 kHz up to 40 kHz to allow the digital-to-analog conversion to be performed by an oversampling digital modulator. The second function is to band-limit the speech signal with both low-pass and high-pass transfer functions. The filter, the PGA gain, and the volume gain can be bypassed by programming bit 9 (**VFBYP**) in the voiceband control register 1.

The interpolated and band-limited signal is fed to a second order ΣΔ digital modulator sampled at 1 MHz to generate a 4-bit (9 levels) oversampled signal. This signal is then passed through a dynamic element-matching block and then to a 4-bit digital-to-analog converter (DAC).
The volume control and the programmable gain are performed in the voiceband digital filter. Volume control is performed in steps of 6 dB from 0 dB to –24 dB. In mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from –6 dB to +6 dB in 1-dB steps to calibrate the system depending on the earphone characteristics. This configuration is programmed with the voiceband downlink control register. The VDL path can be powered down by bit 1 (VDLON) of the power down register.

and a headset output amplifier provides a single-ended signal on the HSO Iota Pin H9 terminal.

1.5 Earpiece Receiver

The Receiver LS1 is connected to BL1 and BL1 connected to R1. Following the Receiver path from the R1 pins EARP U1 Pin J9 and EARN U1 **Pin J10**. The earphone amplifier provides a full differential signal on the EARP Iota Pin J9 and EARN Iota Pin J10 terminals.

1.6 Headset

The headset uses a standard 2.5mm phone jack. The headset circuit contains a analog switch(U11), which is normally switched to headset after power on. When system turn on, the signal HS_EN(U7 Pin L4) is applied. When earphone plug in, the phone will detect this action and make an appropriate response to answer a call while incoming call occur. The interrupt for the headphones is detected on the EAR_DETECT line from Pin 2 of Headset Jack J5. This signal will be pulled to high when the headset is connected.

1.7 Download Receive Path

The External download cable is connected to the Earphone Jack J5 **Pin 4** ,the headset connector for the mobile phone. The download path is routed from J5 **Pin 4** through EF2 Pin 1 and Pin 5 and U11 Pin 4 and Pin 3. The **RX_Modem** signal connects to CalpysoLite_G2 IC U7 **Pin A9** to provide this capability. When software is set to download mode, the signal **HS_EN** is applied low from CalpysoLite_G2 IC U7 **Pin L4**, the phone will toggle it's download state.

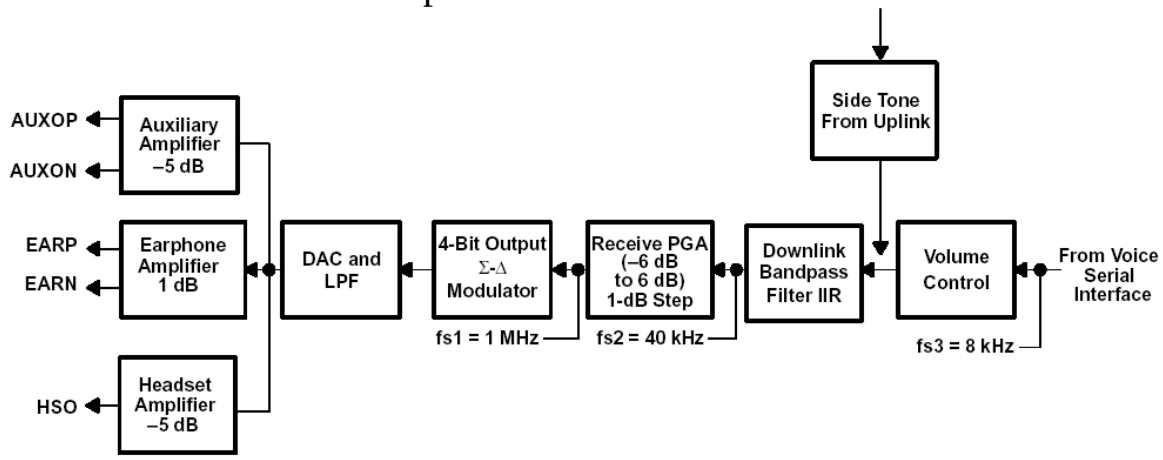


Figure 5 Voice Codec Downlink Patch

1.8 26MHz System Clock

The CalpysoLite_G2 IC U7 contains the **26 MHz** system clock with external Crystal U14.
The system clock will synchronize all time depending devices. It will be converted down with variable divider to a usable smaller internal reference clock.

1.9 Tracking Oscillator

The Tracking Oscillator isolates the CalpysoLite_G2 system clock to synchronize the digital filters in the frontend section of the RITA IC. The responsible signal is the 26Mhz **26MHZ** clock.

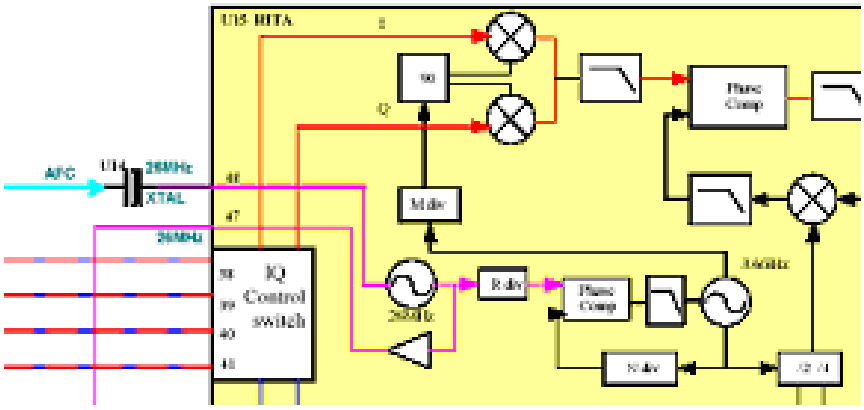


Figure 6 Rita 26MHz clock circuit

2 TRANSMIT

2.1 Audio (Voice uplink Patch)

The VUL path includes two input stages. The first stage is a microphone amplifier, compatible with electric microphones containing a FET buffer with open drain output. The microphone amplifier has a gain of typically 25.6 dB (±1 dB) and provides an external voltage of 2.0V or 2.5V to bias the microphone (**MICBIAS** Iota **Pin J8**). The Transmit audio **HSMICIP** from the Headset Connector J5 **Pin 4** is input to the EF2 **Pin 1 to Pin 5** through **U11 Pin 4** and **Pin 1** and **C98.** This signal is fed to the internal multiplexer, amplified and then passed to the Voice/Audio Codec.

The auxiliary audio input can be used as an alternative source for higher-level speech signals. This stage performs single-ended-to-differential conversion and provides a programmable gain of 4.6 dB or 28.2 dB; currently this stage is not used. The third stage is a headset microphone amplifier, compatible with electric microphones. The headset microphone amplifier has a gain of typically 18 dB and provides an external voltage of 2.0V or 2.5V to bias the headset microphone (**HSMICBIAS** Iota **Pin K8**). When one of the input stages (**MICI**, **HSMICP**) is in use, the other input stages are disabled and powered down.

The resulting fully differential signal is fed to the analog-to-digital converter (ADC). The ADC conversion slope depends on the value of the internal voltage reference.

Analog-to-digital conversion is performed by a third-order ΣΔ modulator with a sampling rate of 1 MHz. Output of the ADC is fed to a speech digital filter, which performs the decimation down to 8 kHz and band-limits the signal with both low-pass and high-pass transfer functions. Programmable gain can be set digitally from –12 dB to +12 dB in 1-dB steps and is programmed with bits 4–0 (VULPG (4:0)) of the voiceband uplink register. The speech samples are then transmitted to the DSP via the VSP at a rate of 8 kHz. There are 15 meaningful output bits.

Programmable functions of the VUL path, power-up, input selection, and gain are controlled by the Baseband serial port (BSP) or the MCU serial port (USP) via the serial interfaces. The VUL path can be powered down by bit 0 (**VULON**) of the power down register.

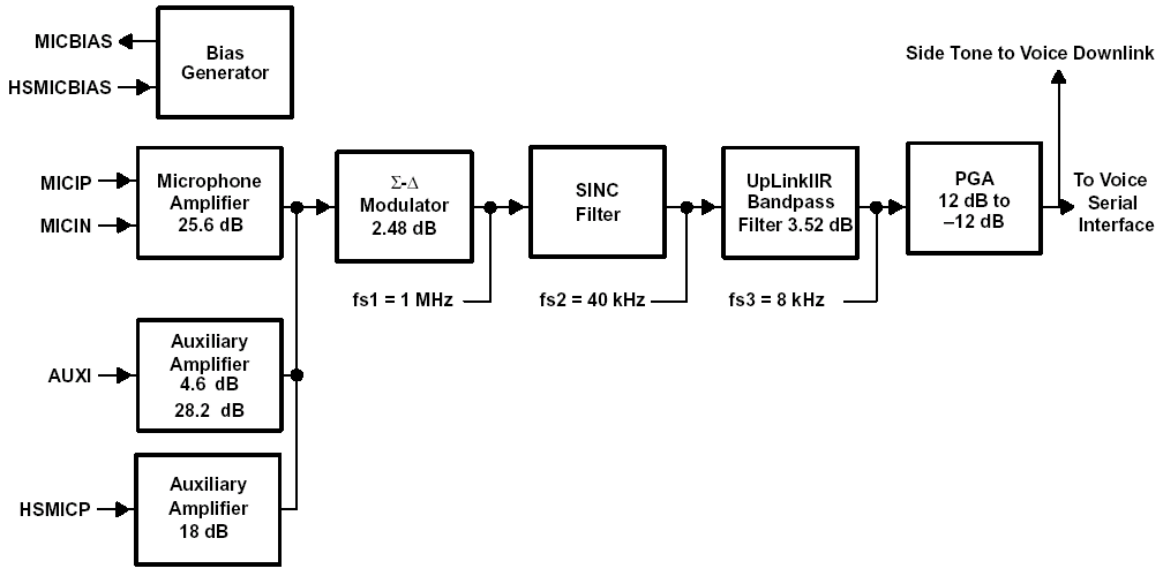


Figure 7 Voice Uplink Path

2.2 Download Transmit Path

The External download cable is connected to the Earphone Jack J5 **Pin 3** ,the headset connector for the mobile phone. The download path is routed from J5 **Pin 3** through EF2 Pin 3 and Pin 4 and U12 Pin 4 and Pin 3. The **TX_Modem** signal connects to CalpysoLite_G2 IC U7 **Pin B9** to provide this capability. When software is set to download mode, the signal **HS_EN** is applied low from CalpysoLite_G2 IC U7 **Pin L4**, the phone will toggle it's download state.

2.3 Modulation

The modulator circuit in the BUL path performs the Gaussian minimum shift keying (GMSK) in accordance with the GSM specification 5.04. The data to be modulated flows from the DSP radio interface (RIF) through the baseband serial port (BSP).

The GMSK modulator is implemented digitally, the Gaussian filter computed on 4 bits of the input data stream being encoded in the sine/cosine look-up tables in ROM, and it generates the in-phase (I) and quadrature (Q) digital samples with an interpolation ratio of 16.

These digital I and Q signals are sampled at 4.33 MHz and applied to the inputs of a pair of 10-bit DACs. The analog outputs are then passed through third-order Bessel filters to reduce out-of-band noise and image frequency and to obtain a modulated output spectrum consistent with GSM specification 05.05.

Fully differential signals are available at the **TXIP** Iota **Pin D9 (**BULIP**)**, **TXIN** Iota **Pin D10 (**BULIM**)**, **TXQP** Iota **Pin C10 (**BULQP**)**, and **TXQN** Iota **Pin C9 (**BULQM**)** terminals.

To minimize phase trajectory error, the dc offset of the I and Q channels can be minimized using offset calibration capability. During offset calibration, input words of the 10-bit DACs are set to zero code and a 6-bit sub-DAC is used to minimize the dc offset at analog outputs.

The entire content of a burst, including guard bits, tail bits, and data bits, is stored in one of two 160-bit burst buffers before starting the transmission. The presence of two burst buffers is dictated by the need to support multislot transmission: one buffer is loaded with new data while the content of the second buffer is pushed into the GMSK modulator for transmission.

Single-slot or multislot mode is selected by bit 5 (**MSLOT**) of the baseband codec control register. When single-slot mode is selected, only the content of burst buffer 1 is used for modulation. Output level can be selected with bits 8–6 (OUTLEV [2:0]) of the baseband codec control register.

The typical sequence of burst transmission consists of:

1. Power up the BUL path
2. Perform an offset calibration (not mandatory)
3. Modulate the content of the burst buffer

Timing of this sequence is controlled via the timing serial port (TSP), which receives serial real-time control signals from the TPU of CalpysoLite_G2 IC U7 (DSP) device. Three real-time signals control the transmission of a burst: **BULON**, **BULCAL**, and **BULENA**. Each signal corresponds to a time window.

BULON high sets the BUL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. **BULCAL** enables the offset calibration window. During **BULCAL**, inputs of 10-bit DACs are forced to code zero and a low-offset comparator senses the dc level at the **TXIP** Iota **Pin D9 (**BULIP**)/TXIN** Iota **Pin D10 (**BULIM**)** and **TXQP** Iota **Pin C10 (**BULQP**)/ TXQN** Iota **Pin C9 (**BULQM**)** terminals. The result of the comparison modifies the content of the offset registers, which drives the 6-bit sub-DACs to minimize the offset error. The duration of the calibration phase depends on the time needed to sweep the sub-

DAC dynamic range. Modulation starts with the rising edge of **BULENA** and ends 32 one-quarter bits after the falling edge of **BULENA**. At the end of modulation, the modulator is reinitialized by setting the pointers of burst buffers and the filter ROM to the base address. The I vector is set to its maximum value, while the Q vector is set to 0.

The output common mode voltage of the **TXIP** Iota **Pin D9 (**BULIP**)**, **TXIN** Iota **Pin D10 (**BULIM**)**, **TXQP** Iota **Pin C10 (**BULQP**)**, and **TXQN** Iota **Pin C9 (**BULQM**)** terminals can be set to several values by bits 2–0 (SELVMID [2:0]) of the baseband codec control register.

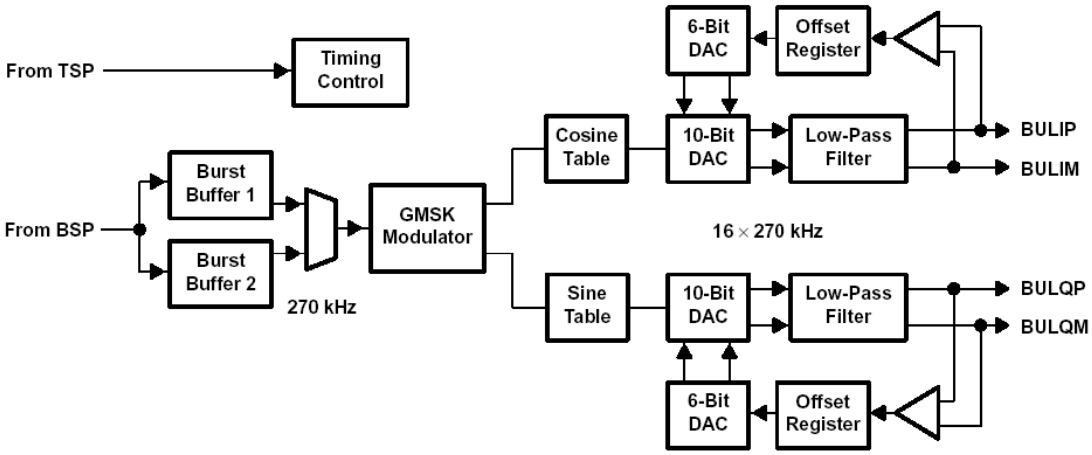


Figure 8 Baseband Uplink Block Diagram

2.4 Transceiver

The RITA is a quadruple band transceiver IC suitable for GSM 850, GSM 900, DCS 1800 and PCS 1900 GPRS class 12 applications. The chip integrates the receiver based on direct conversion architecture, the transmitter based on the modulation loop architecture, the frequency synthesis including a 26MHz VCXO, a MAIN N- integer synthesizer, 2 MAIN VCOs, a programmable MAIN loop filter, 2 TX VCOs, a TX loop filter, the voltage regulators to supply on chip. Please

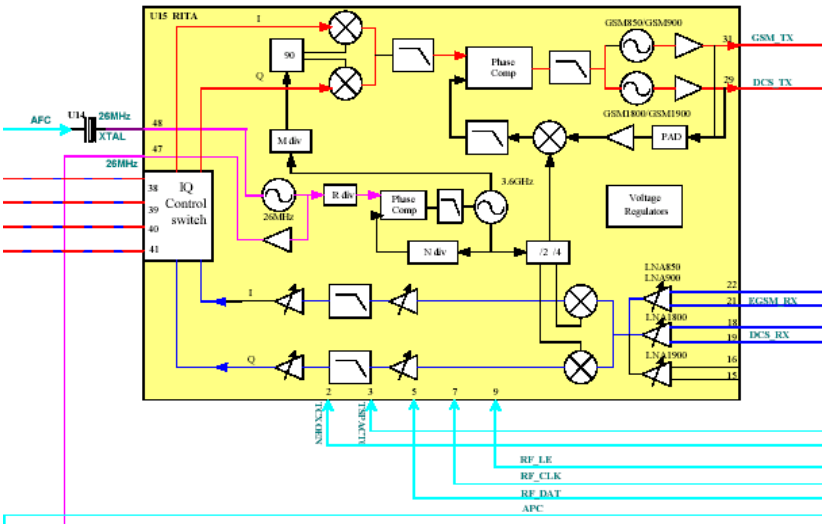


Figure 9 Rita IC

2.5 TX PA

The TX signal outputs at **GSM_TX** Rita **Pin 31** (low-band) and **DCS_TX/ PCS_TX** Rita **Pin 29** (high-band). The high-band signal passes through C113, and the low-band signal passes through L4 and C112. The SKY77324 PA IC, U13, has two independent paths (one for the high-band signal and one for the low-band signal). A 2-stage linear power amplifier amplifies the signal in each path. The SKY77324 U13 also contains band-select switch circuitry to select GSM (logic0) or DCS/PCS (logic1) as determined from the **GSM_TXEN Pin 4** signal. The module consists of separate GSM850/900 PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50Ω input and output impedances, and a Power Amplifier Control (**PAC** SKY77324 **Pin 22**) block with an internal current-sense resistor.

The CX77324 is in closed loop PAC mode when the **PAENA Pin 2** signal remains high.

The amplified RF output signal feeds out of SKY77324 from **Pin 17** for high-band and **Pin 12** for low-band. The high-band signal enters the Antenna Switch at **Pin 7**, and the low-band signal enters the Antenna Switch at **Pin 9**. The Antenna Switch provides isolation between the various receiver and transmitter paths as they connect to the antenna port, **Pin 3**. For Antenna Switch settings, see **Section 1.1: Band Selection**.

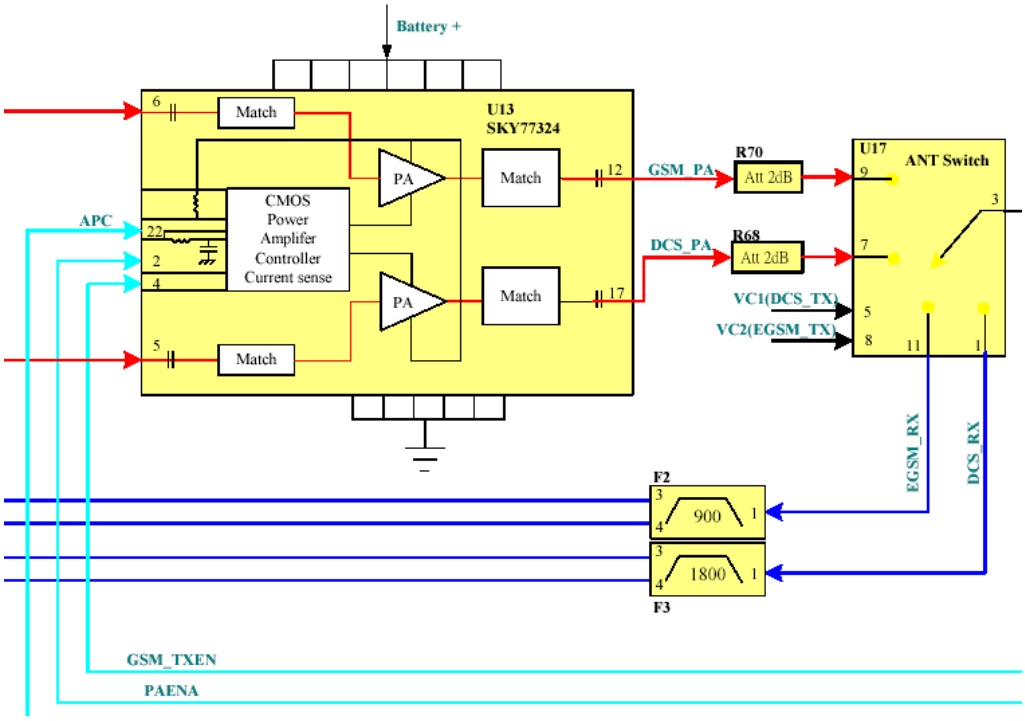


Figure 10 Power Amplifier and Antenna Switch

2.6 TX PA Power Control in SKY77324 U17

Figure 10 shows the Integrated Power Amplifier Control (iPAC) function along with SKY77324 proven quad-band PA architecture and CMOS current buffering bias scheme. The iPAC circuitry generally operates independently of other device subcircuits and serves to make the RF output power a predictable function of the **APC** SKY77324 **Pin 22** (V_{APC}) control voltage over variations in supply, temperature, and process. Top-level performance specifications, with exception of those directly associated with power control (or the range of **APC** control voltage), are not altered by placing the device into internal closed loop operation with the **PAENA (**PAC Enable**)** signal. Thus, the iPAC function of the SKY77324 can be analyzed separately from the general power amplifier performance.

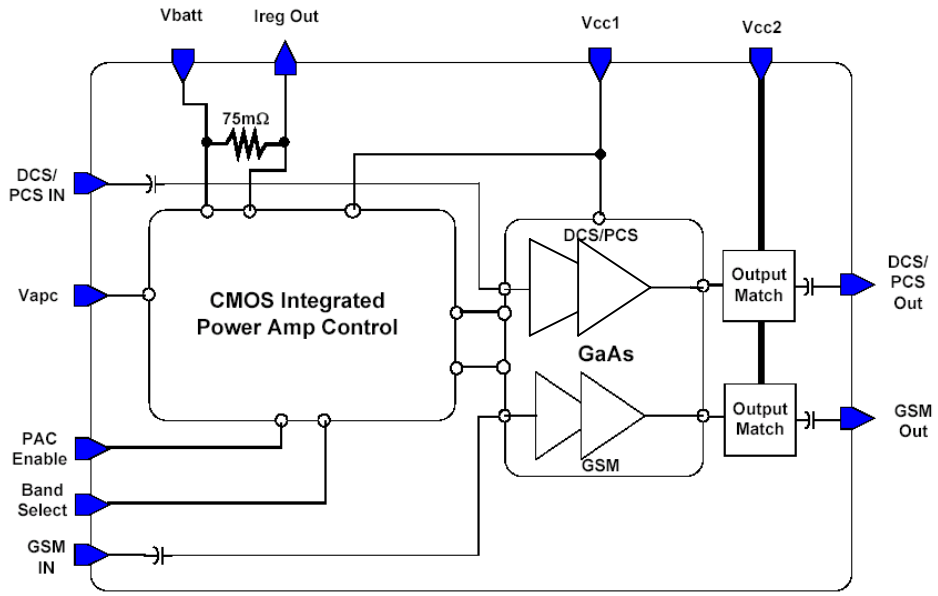


Figure 11 Top Level View of SKT77324 PAM

A more detailed view of the CMOS circuitry in Figure 11 shows two main functional blocks that are added to the typical CMOS buffering circuitry providing a high impedance voltage interface for transistor amplifier bias control. The **APC** SKY77324 **Pin 22** input is normally tied directly to the Iota **Pin K4** output.

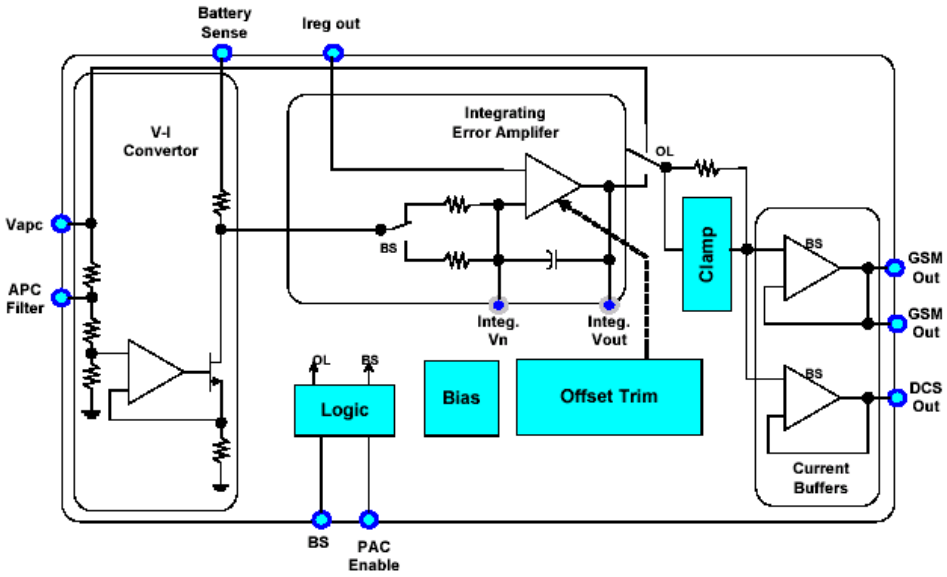


Figure 12 Top Level View of SKT77324 PAM

A key function of the iPAC circuitry is to adjust the voltage across the current sense resistor to match what it was during the initial phone level calibration at a corresponding **APC** voltage. The V-I Converter creates the stabile current source reference that sets the collector currents. The Integrating Error Amplifier supports compliant design performance with DAC ramp profiles.

The **Ireg out** sources current, which is routed back to the last stage linear power amplifier Vcc input for closed loop operation. This routing is internal to the PA, which can be sensitive to any

rectified RF voltage signals. Also, because resistance to temperature variation is one of the primary goals of the iPAC circuitry, the die floor plan and package IO designations have been carefully chosen to keep the iPAC functions away from the transistor finals where most of the heat is generated during the power burst. The GSM RF input has been located so as to minimize any RF isolation issues with the sense resistor.

3 Iota Monitoring ADC

The monitoring section includes a 10-bit ADC and 10-bit/15-word RAM. The ADC monitors:

- Four internal analog values:
  – Battery voltage (**VBAT**)
  – Battery charger voltage (**VCHG1**)
  – Current charger (current-to-voltage (I-to-V) converter) (**ICHG)**
  – Backup battery voltage (**VBACKUP**)
- Four external analog values:
  – **VADCID** Rita **Pin B6** for test point
  – **BATTEMP** Rita **Pin A6** for monitor the battery temperature
  – ADIN3: not used
  – **TEMP_SEN** Rita **Pin C6** for temperature sense(currently SW not support)

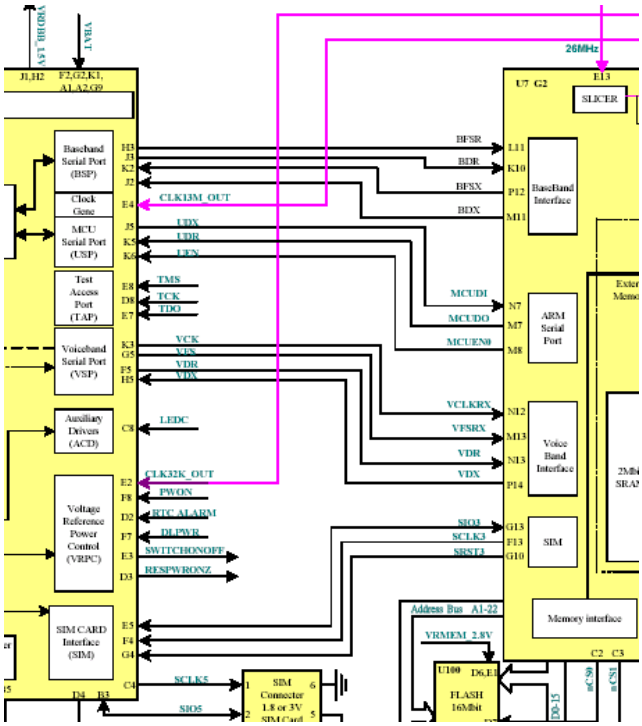


Figure 13 Baseband interface

4 Baseband Serial Port(BSP)

The baseband serial port (BSP) is a bidirectional (transmit/receive) serial port. Both receive and transmit operations are double-buffered and permit a continuous communication stream. Format is a 16-bit data packet with frame synchronization.

The CK13M master clock is used as a clock for both transmit and receive.
The BSP allows read and write access of all internal registers under the arbitration of the internal bus controller. But its transmit path is allocated to the BDL path during burst reception for I and Q data transmissions.

5 Microcontroller Serial Port(USP)

The microcontroller serial port (USP) is a synchronous serial port. It consists of three terminals: data transmit (**MCUDI** Rita **Pin J5**), data receive (**MCUDO** Rita **Pin K5**), and port enable (**MCUEN0** Rita **Pin K6**). The clock signal is the CK13M master clock.

Transfers are initiated by the external microcontroller, which pushes data into the USP via the **MCUDO**, while synchronous data contained in the transmit buffer of the USP is pushed out via the **MCUDI**. The USP allows read and write access of all internal registers under the arbitration of the internal bus controller.

6 Pulse Width Tones (PWT)

This module generates a modulated frequency signal for the external buzzer via **BUZZER** CalypsoLite_G2 **Pin K7**. Frequency is programmable between 349Hz and 5276Hz with 12 half tone frequencies per octave. The volume is also programmable.

7 Pulse Width Light (PWL)

This module allows the control of the backlight of LCD and keypad by employing a 4096bit random sequence via **LEDKEY_EN** CalypsoLite_G2 **Pin L7**. This voltage level control technique decreases the spectral power at the modulator harmonic frequencies. The block uses a switching clock of 32kHz.

8 General purposes I/O (GPIO)

CalypsoLite_G2 provides 16 GPIOs in read or write mode by internal registers.

GPIO Pin	Used As.	Description
IO0/TPU_WAIT	**DTR_MODEM Pin N3**	Data Terminal Ready
IO1/TPU_IDLE	IO1	None
IO2/IRQ4	**HS_EN Pin L4**	Control UART or HS trace
IO3/SIM_RnW	**LCDA0 Pin M4**	LCD driver detect
IO4/TSPDI	IO4	None
IO5/SIM_PWCTRL	**S_PWCT Pin F4**	For SIM Card
IO6/BCLKX	IO6	None
IO7/NRESET_OUT	**nRESET Pin N2**	Reset LCD
IO8/MCUEN1	IO8	None
IO9/MCSI_TXD	IO9	850/1900 or 900/1800 band detect
IO10/MCSI_RXD	**MCSI_RXD Pin M10**	DAI interface
IO11/MCSI_CLK	**MCSI_CLK Pin N10**	DAI interface
IO12/MCSI_FSYNCH	**MCSI_FSYNCH Pin K9**	DAI interface
IO13/MCUEN2	**EAR_DETECT Pin L8**	Ear Phone detect
IO14/NbhE	**nBHE Pin E5**	SRAM U24 Hi byte select
I015/NblE	**nBLE Pin E4**	SRAM U24 Low byte select

9 Mono Display

The mono display LCD display is controlled using the **LCDA0** CalpysoLite_G2 **Pin M4, SDA**

CalpysoLite_G2 **Pin M9, SCL** CalpysoLite_G2 **Pin L9, nRESET** CalpysoLite_G2 **Pin N2,** and **VRIO_2.8V** Rita **Pin B1**

LCDA0, an LCD driver is detected.

SDA is I2C interface serial bidirectional data for LCD.

SCL is I2C interface master serial clock for LCD.

nRESET resets LCD.

VRIO_2.8V provides LCD power supply**.**

9.1 Display Backlights

The Display backlights are provided by the control signals **LEDC** Rita **Pin C8** and **LEDKEY_EN** CalpysoLite_G2 **Pin L7**.

LEDC is a pre-charging indication. The maximum current is 10mA. During charging and when battery voltage is under 3.2V, the backlights are illuminated

LEDKEY_EN controls keypad lights and backlights are illuminated when this signal goes high.

10 32KHz RTC

The Real-time Clock Interface is part of the CalpysoLite_G2 U7 in use with the crystal U6.
The clock signal is running on 32KHz as reference for the Clock module and as deep sleep Clock.

.

11 SIM Circuit

To allow the use of both 1.8V and 3V SIM card types, a SIM level-shifter module in the Iota U1 device. The SIM card digital interface ensures the translation of logic levels between the Iota U1 device and the SIM card for the transmission of three different signals:

VRSIM –this is an LDO voltage regulator providing the power supply to the SIM card driver of the Iota device.

SIO5 – Data Communications path between SIM CON1 **Pin 2** and Iota **Pin C4**

SCLK5 – SIM data Clock

SRST5 – SIM Reset from Iota **Pin D4**

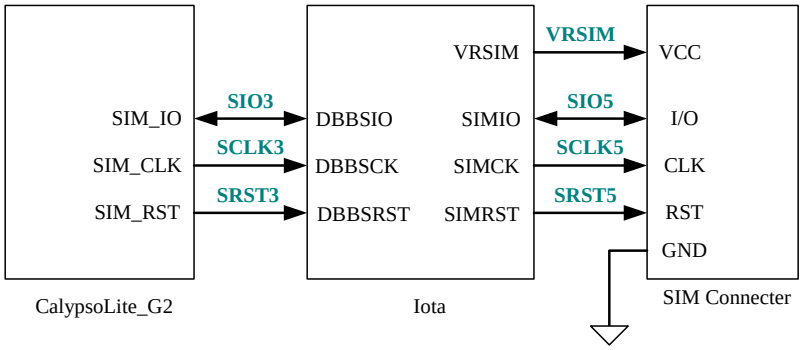


Figure 14 SIM interface

11.1 SIM Card Supply Voltage Generation

To accommodate the 1.8V or 3V SIM cards, the Iota includes an LDO voltage regulator that

delivers supply voltage **VRSIM Pin B4** to the SIM module.

The LDO voltage regulator is configured to generate the 1.8V or 2.9V (**VRSIM Pin B4**) supply. The **VRSIM Pin B4** terminal is decoupled by a capacitor (C15).

The SIM Card Supply Voltage Generation is controlled by the following setoff control bits:

- Bit 0 (SIMSEL) of the SIM Card control register selects the **VRSIM** output voltage (1.8V or 2.9V).
- Bit 1 (RSIMEN) of the SIM Card control register enables the 1.8V/2.9V series regulator.
- Bit 2 (SIMRSU) of the SIM Card control register is the **VRSIM** regulator status.
- Bit 3 (SIMLEN) of the SIM Card control register enables the SIM interface level shifter (on the SIMCK, SIMRST, and SIMIO terminals).

12 Keypad

The keyboard is connected to the chip using:

ROW0-ROW4(KBR 4:0) input pins for row lines

COL0-COL3(KBC 4:0) output pins for column lines

If a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted.

To allow key press detection, all input pins (**KBR**) are pulled up to VCC and all output pins (**KBC**) are driving a low level. Any action on a button will generate an interrupt to the microcontroller which will, as answer, scan the column lines with the sequence describe below.

This sequence is written to allow detection of simultaneous press actions on several key buttons.

	RESET	IDLE	KEYBOARD SCANNING						IDLE
KBC(0)	1	0	1	0	1	1	1	1	0
KBC(1)	1	0	1	1	0	1	1	1	0
KBC(2)	1	0	1	1	1	0	1	1	0
KBC(3)	1	0	1	1	1	1	0	1	0
KBC(4)	1	0	1	1	1	1	1	0	0

Figure 15 Keyboard scanning sequence

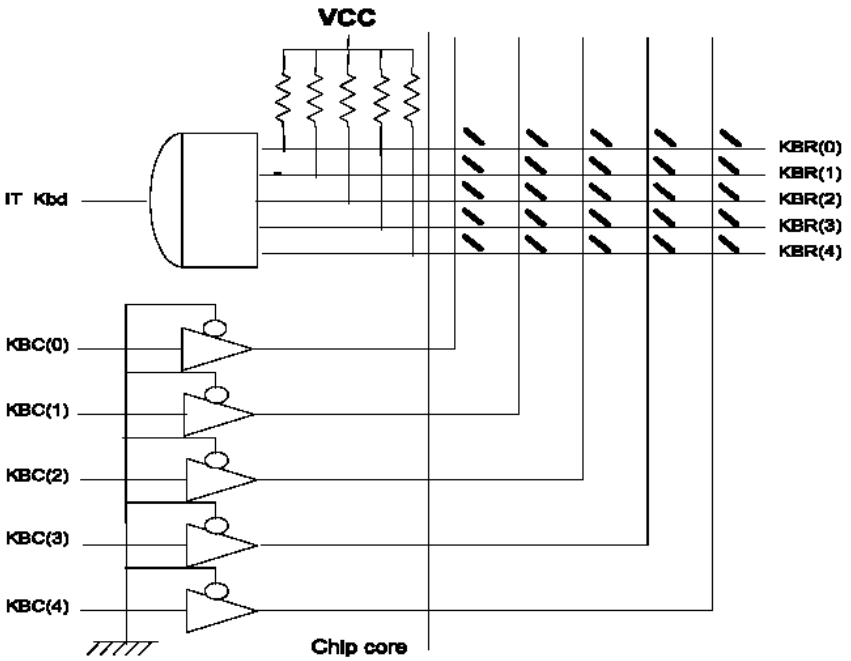


Figure 16 Keyboard connection

12.1 Keypad Matrix

The keypad matrix is as follow:

Function	key	Col 0	Col 1	Col 2	Col 3	Row 0	Row1	Row 2	Row 3	Row 4
No/PWR	S1									0
MEDIR	S2				0					0
*	S3				0				0	
7	S4				0			0		
4	S5				0		0			
1	S6				0	0				
MENU	S7			0						0
0	S8			0					0	
8	S9			0				0		
5	S10			0			0			
2	S11			0		0				
STYLE	S12		0							0
#	S13		0						0	
9	S14		0					0		
6	S15		0				0			
3	S16		0			0				
RIGHT	S17	0								0
LEFT	S18	0							0	
DOWN	S19	0						0		
UP	S20	0					0			
SEND	S21	0				0				

13 Vibrater circuit

DAC Iota **Pin H4** is used to control the vibrational level. D1 is used to protection the vibrater. In the 3.8V, the **DAC** output voltage is 2V and drain current is around 80mA .

14 Memory

The C115 portable will be using two memory parts, U100 and U24. The Flash memory U100 has 16Mbit size and the SRAM memory U24 has 2Mbit size.

A [1..22] – Address Bus for Flash U100 and SRAM U24 memory.

D [0..15] – Data Bus for Flash U100 and SRAM U24 memory.

VRMEM_2.8V – This is provided Flash memory power supply.

RnW – Read and Write allows information to be written or read from the memory devices.

nFOE – Flash and SRAM output Enable (Active Low).

FDP – The Flash reset/deep power-down mode control.

nCS0 – This is used as Chip Enable for the Flash Memory.

nCS1 – This is used as Chip Enable for the SRAM Memory.

nBHE – Enable to address High Byte Information.

nBLE – Enable to address Low Byte Information.

VRRAM _2.8V – This provides SRAM memory power supply

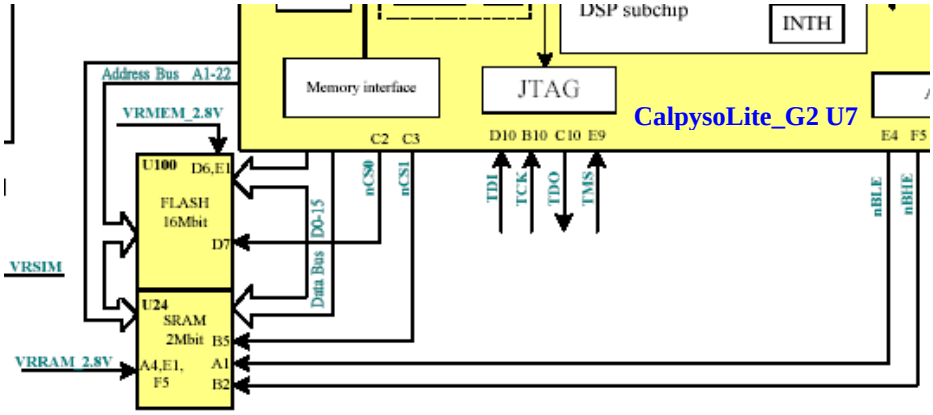


Figure 17 Memory interface

15 Power

15.1 Low-Dropout Voltage Regulators

The voltage regulation block consists of seven subblocks.

Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators supply power to internal analog and digital circuits, to the CalpysoLite_G2 IC U7 (DSP) processor, and to external memory.

The first LDO (**VRDBB_1.5V** Iota **Pin J1 and H2**) is a programmable regulator that generates the supply voltages 1.5 V for CalpysoLite_G2 IC U7 (DSP). During all modes, the main battery directly supplies **VRDBB**.

The second LDO (**VRIO_2.8V** Iota **Pin B1 and B2**) generates the supply voltage (2.8 V) for

the CALPYSOLITE_G2 IC U7 (DSP), LCM backlight, U11/U12 (analog switch) and Rita U15. During all modes, the main battery directly supplies **VRIO**.

The third LDO (**VRMEM_2.8V** Iota **Pin G1**) is a programmable regulator that generates the supply voltages 2.8 V for flash memory U100 and CalpysoLite_G2 IC U7 (DSP) memory interface I/Os. During all modes, the main battery directly supplies **VRMEM**.

The fourth LDO (**VRRAM_2.8V** Iota **Pin F1**) is a programmable regulator that generates the supply voltages 2.8 V for external memories (SRAM memories). The main battery directly supplies **VRRAM**.

The fifth LDO (**VRABB_2.8V**) generates the supply voltage (2.8 V) for the analog functions of the Iota U1 device. During all modes, the main battery directly supplies **VRABB**.

The sixth LDO (**VRSIM** Iota **Pin B4**) is a programmable regulator that generates the supply voltages (2.9 V and 1.8 V) for SIM card and SIM card drivers. During all modes, the main battery directly supplies **VRSIM**.

The Iota U1 allows three operating modes for each of these voltage regulators:

1. ACTIVE mode during which the regulator is able to deliver its full power.
2. SLEEP mode during which the output voltage is maintained with very low power consumption but with a low current capability.
3. OFF mode during which the output voltage is not maintained and the power consumption is null.

The regulators rise up in ACTIVE mode only and each of them has a regulation ready signal RSU. In switched-off and backup states of the mobile phone, the voltage regulators will be set to a SLEEP or OFF mode depending on the system requirements. The regulator voltages are decoupled by a low ESR capacitor (C14 ~C19) connected across the corresponding VCC and ground terminals. Besides its voltage filtering function, this capacitor also has a voltage storage function that could give a delay for data protection purposes when the main battery is unplugged.

The seventh LDO (**VRRTC_1.5V** Iota **Pin D1**) is a programmable regulator that generates the supply voltages 1.5 V for the real-time clock and the 32-kHz oscillator located in the CalpysoLite_G2 IC U7 (DSP) device during all modes. The main or backup battery supplies **VRTC**.

15.2 Radio Power Down Methods

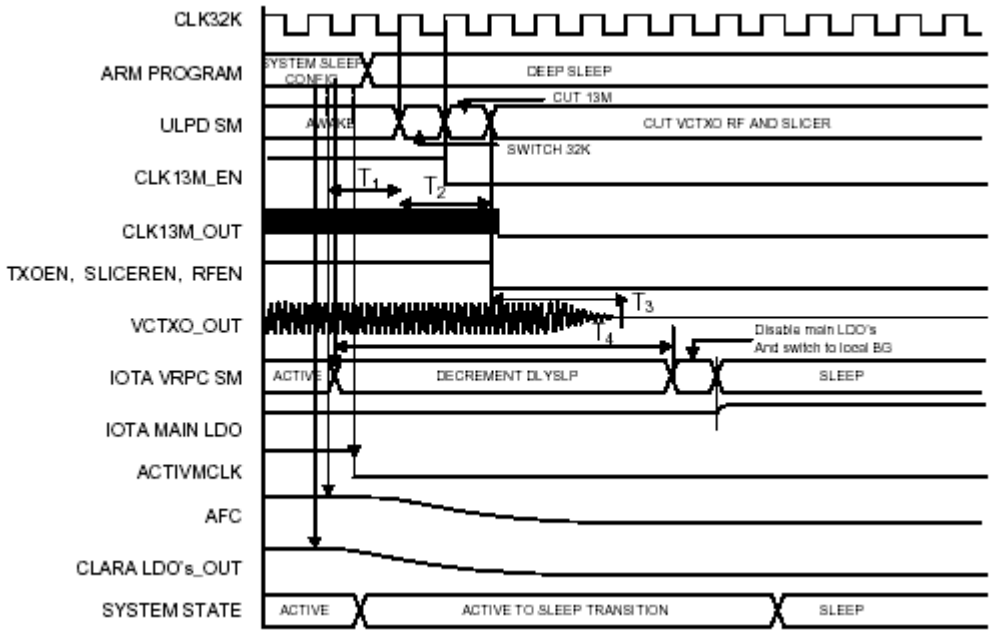
The phone is disabled by one of the following conditions:

1. Software-initiated power down.
   When the user requests to turn the phone off by pressing the ON/OFF key, or put **DLPWR** **TP27** to GND, or when a low battery voltage is detected by software through **VBATS** Iota **Pin C5**(typical value is 3.5V) measurement and therefore the phone turns off.
2. Hardware-initiated power down.
   When the RFEN voltage drops below the Threshold voltage +3.2V, system will trigger an interrupt to program LDO to stay in SLEEP mode.

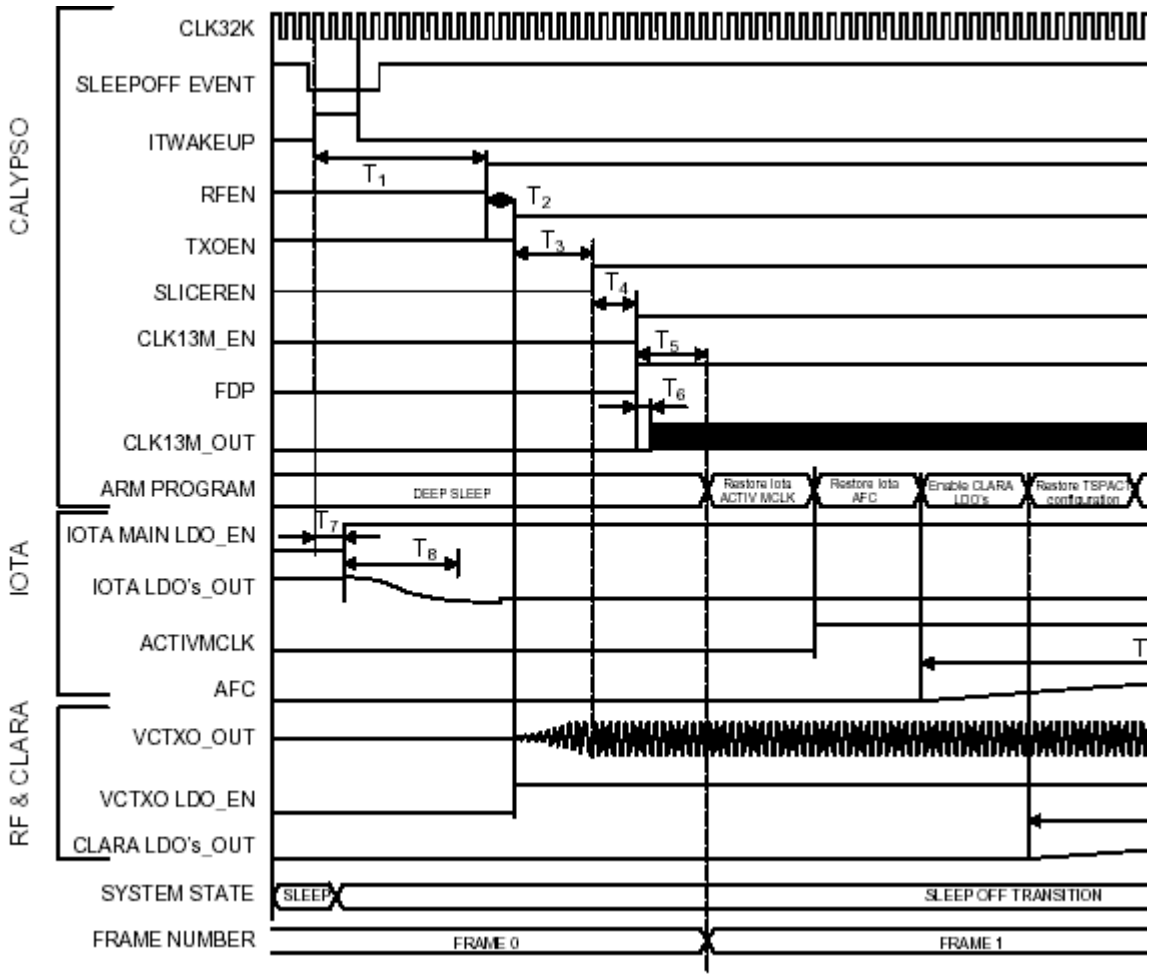
16 Sleep Module

The Sleep Module allowed for optimal power savings in idle modes. Rita internal LDOs (VRDBB, VRIO, VRRAM, VRMEM, VRSIM, VRABB) have very low current consumption and can provide 1mA current.

16.1 Sleep Up Sequence



16.2 Sleep off Sequence



17 Power Tree

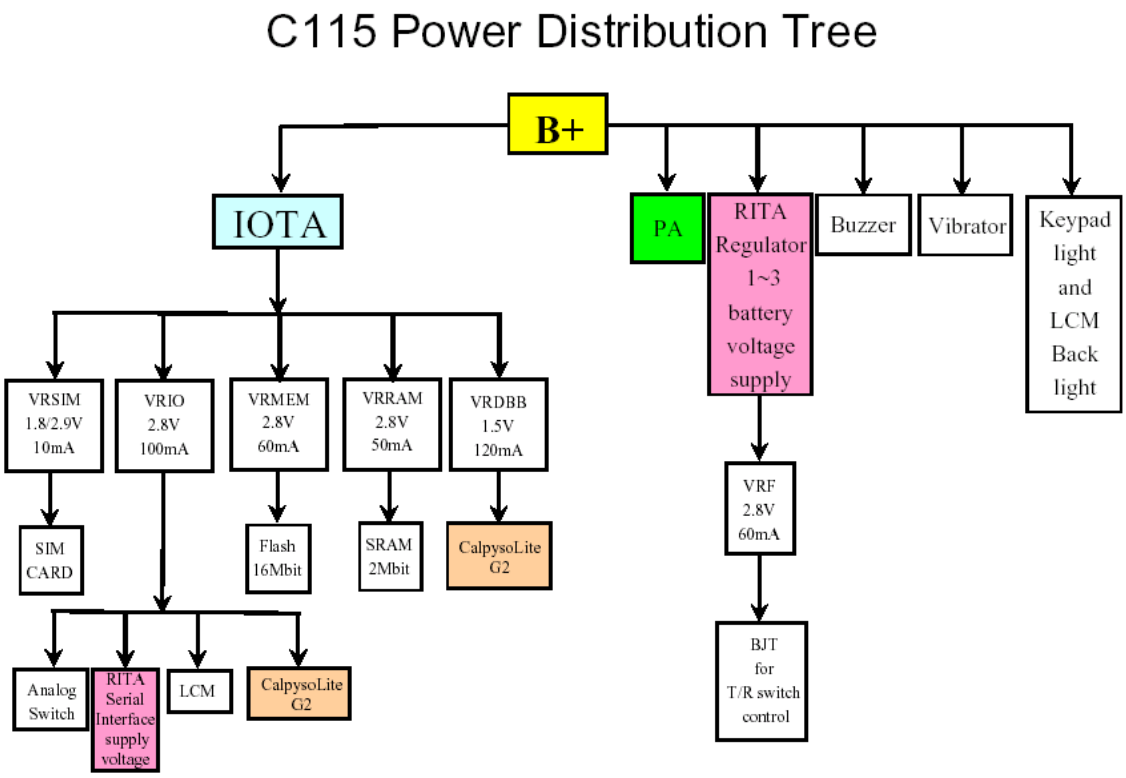


Figure 178Power Distribution Tree

18 Charging Circuit and External Power

We can obtain power from battery, and an external charger. Power source via the accessory connector are not supported.

18.1 Battery support

The Battery Block J1 is made up of 3 contacts, these are

- Pin 1– **VBAT**
- Pin 2–**BATTEMP** –Used to measure the Battery temperature during charging, fed from the battery connector to Iota U1 **PinA6**
- Pin 3– **BATTGND**

18.2 Charger support

When a charger is plugged in, U5(NCP345) will enable U4(P-MOSFET) to start charging process if **VCHG1** Iota **PinA5** is less than 6.85V. The process starts at pre-charge state until **VBAT** is higher than 3.2V. Pre-charge current is about 40mA, depending on the voltage of **VBAT**. When **VBAT** is higher than 3.2V the Battery Charge Interface(BCI) turns to normal charge. The normal charge will start as constant current mode (MAX current is 330mA), and followed by constant voltage mode (MAX voltage is less than 4.3V).
When **ICHG** is larger than 1A, the PT1 will be opened (OCP). When the battery voltage is higher than 4.35V, U104 will stop charging.