AURA R1
Theory of Operation

Version 2008.08.20.1

Table of Contents

1) VERSION HISTORY

Version	Notes
2008.07.07.1	Initial Draft
2008.08.14.1	Initial Release
2008.08.14.1	Updated Bluetooth

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2) INTRODUCTION

The Motorola AURA R1 mobile phone is a small and lightweight Global System for Mobile communications (GSM) mobile phone. It incorporates a Java / Linux software platform, allows short message service (SMS) text messaging, and includes personal information manager (PIM) functionality. The supported GSM bands for AURA R1 are GSM 850/900/1800/1900 MHz; operating frequencies are shown in Table 1. AURA R1 also supports Bluetooth™ Version 2.0 EDR, GPRS and EDGE (Class 12).

Band	GSM900	DCS1800	PCS1900	GSM850
Transmit	880-915 MHz	1710-1785 MHz	1850-1910 MHz	824-849 MHz
Receive	925-960 MHz	1805-1880 MHz	1930-1990 MHz	869-894 MHz

Table 1: Operating Frequencies

The AURA R1 mobile phone has a rotator form factor. Key features include 1.55” round (480 pixel diameter) TFT display, 2 Megapixel camera, Bluetooth streaming stereo (A2DP), MPEG4 video capture/playback, and USB 2.0 for high speed data transfers to and from a computer. The standard 810 mAH Lithium Ion (Li-Ion) battery fits behind a removable back cover. The phone accept both 3V and 1.8V mini subscriber identity module (SIM) cards which fit into the SIM holder underneath the battery. AURA R1 also features 2GB of embedded user memory. The antenna is a fixed internal type antenna.

3) ANTENNA SWITCHING AND CONTROL CIRCUIT

The integrated antenna switch and power amplifier module block diagram is shown in Figure 1. The module supports quad-band, dual-mode (GMSK/8PSK (EDGE)) operation, and consists of a dual line-up power amplifier, harmonic filter, and antenna switch. The antenna contact connects the antenna to any one of four receiver ports or either low band power amplifier output or high band power amplifier output.

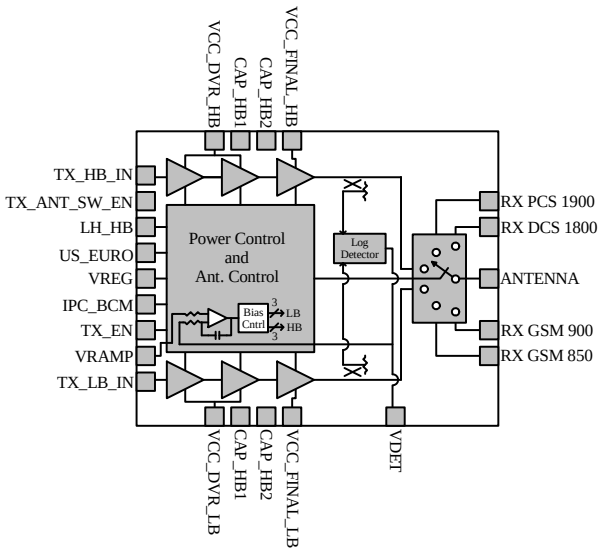


Figure 1: Power Amplifier and Antenna Switch Control

Table 2 shows the truth table for the antenna switch. The antenna switch routes the appropriate band transmit or receive signal between the antenna and respective IC. The switch is controlled by a sequence control unit inside the TransAAM. The outputs of the TransAAM are TX_ANT_SW_EN, LB_HB, and US_EURO.

Primary Logic Table: Use Primary sequencer code			
Inputs			**Output**
TX_ANT_SW_EN	**LB_HB**	**US_EURO**	**Antenna Port Connection**
1	0	X	TX_LB
1	1	X	TX_HB
0	0	0	RX_CEL (Pin 1)
0	0	1	RX_EGSM (Pin2)
0	1	0	RX_ PCS (Pin 4)
0	1	1	RX_DCS (Pin 3)

Table 2: Antenna Switch Truth Table

In addition, in order to provide increased antenna bandwidth under multiple conditions, an additional switch is employed to switch in an antenna matching element, as shown in Figure 2, depending on the band of operation and the position of the rotator (open or closed).

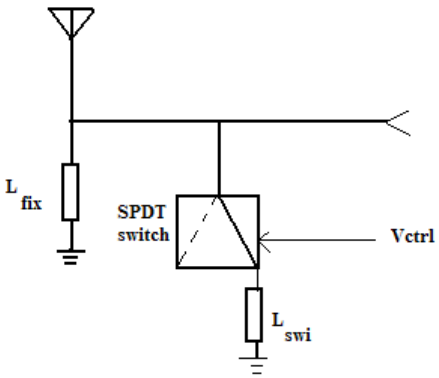
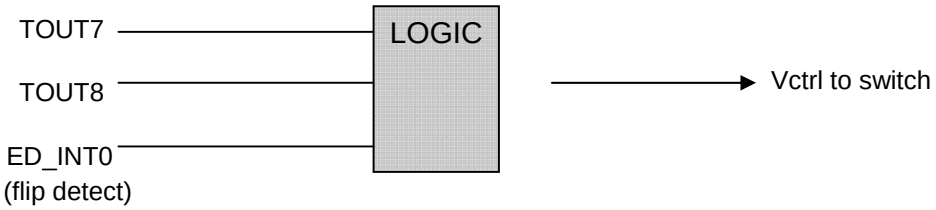


Figure 2: Antenna Match Switching

Depending on both the band and rotator position, the Lswi will be switched in or out based on the state of Vctrl, thereby changing the tuning of the antenna response for either the 850 or 900 MHz bands. When switch is in off state, the response is tuned for 850 MHz band and when the switch is in on state it is tuned for 900 MHz band. The control signals and truth table are shown in Figure 3.



Truth Table

FLIP	TOUT7	TOUT8	ED_INT0	VCTRL
open	0	0	0	0
open	0	1	0	1
open	1	0	0	0
open	1	1	0	1
closed	0	0	1	0
closed	1	0	1	1
closed	0	1	1	0
closed	1	1	1	1

Figure 3: Antenna Match Switching Logic and Truth Table

TOUT7 and TOUT8 are programmed in permanent data storage (SEEM_ANTENNA_SWITCH) and can be set according to transmit and receive frequencies in each operating band.

4) RECEIVER THEORY OF OPERATION

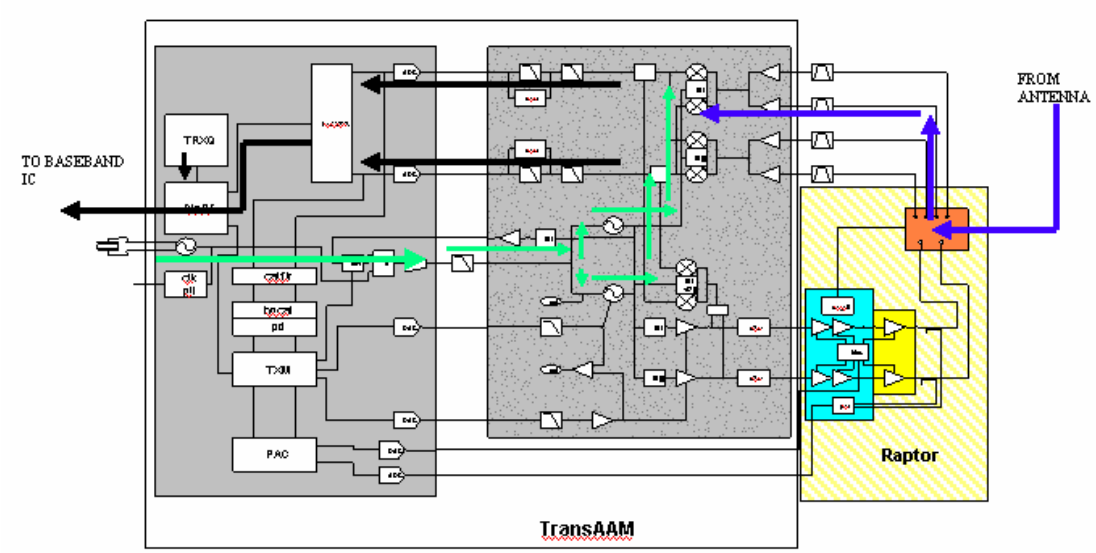


Figure 4: TransAAM Functional Block

The TransAAM receiver is a quad band receiver, built around a Superheterodyne-infradyne architecture. A simplified block diagram for the receive path is depicted in Figure 4. The receive signal is down-converted to a VLIF of 122.7 kHz, after the LNA and is then passed through a polyphase filter in order to suppress the image frequency. The VLIF signal is then digitally converted to baseband and passed through a digital filter with a bandwidth of 90 kHz. The filter selected is suitable for the feature DARP (2X, 14th order). On TransAAM, POR programming sets up the necessary registers so as to meet the receiver topology architecture, the digital mixer, as well as the digital VLIF requirements as previously described. The values are directly derived from permanent data storage (SEEM_RF_DEFAULT_SPI).

The receiver has multiple gain setting blocks, of which two need adjustment for automatic gain control: the low-noise amplifier (LNA) and the intermediate frequency amplifier (IFA) gain. The other two blocks have fixed gain or attenuation.

The AGC is programmed on a receive activation basis. The AGC strategy is based on a range approach where the headroom varies as a function of the antenna power.

The ability of on-chip matching results in little need to characterize the IFA gain. The LNA absolute gain, however, has the potential to vary from die to die in production. Therefore only the LNA requires factory calibration, and the Layer 1 stack expects knowledge of the accurate gain of the front end for each permissible setup, encompassing all static contributions from the antenna to the LNA. The front end gain, for up to 8 AGC settings, is stored in the SEEM_AGC_TABLE. 2 bytes per setting is allocated and a 2 compliment value having a resolution of 1/256 dB. Across the band frequency compensation of the receiver lineup is catered for by a set of seven first order interpolation chords. Correction terms and first order interpolation models are directly derived from permanent data storage (SEEM_AGC_TABLE).

Stack software derives antenna power for any given receive activation using normalized baseband power, and the associated receiver lineup gain. The receiver lineup gain is obtained by accumulating each contributor of the lineup.

The receive coprocessor latency covers the following filters: noise cancellation, sinc, droop, 1st and 2nd alias, 38th FIR and selectivity (DARP). That latency amounts to approximately 98us.

TransAAM is always set for EDGE filter line-up, even in GSM mode, therefore the latency remains constant independent of mode. If the selectivity filter is not used then the latency value needs to be reduced by approx 30us. Once the antenna data path is turned off, the filters clocked at 13 MHz will start to corrupt the slower clocked filters quicker with bad data due to multi-rate clocking, therefore it is not possible to flush the full latency of the Receive coprocessor, and data will only remains valid for 54us. Latency from antenna to DigRF Interface is approximately 102us (2us for analog, 98us for receive coprocessor and 2us for DigRF). The total receive time from Strobe to first baseband sample is approximately 230us.

The VLIF is set to 122.7 kHz. The complex quadrature mixer in ACE operates at a frequency based on the ARFCN to be received, which introduces some phase imbalance between I-and-Q paths. Provision is made for factory phased Imbalance correction coefficients to minimize imbalance and therefore to maximize image rejection of the receiver. This is particularly important for adjacent channel rejection in VLIF mode. This is done on a receive activation basis based on the ARFCN, with paired values of PHASEADJAx and PHASEADJBx for phase, and paired values of GAINADxA and GAINADxB for gain.

VLIF (DIF) is defaulted at POR, and the digital mixer topology (SIGN) is fixed to infradyne. When “IF toggling” is enabled, the Engine Stack shall keep track of the last IF topology used on a radio block basis. That mechanism shall be implemented for (E)GPRS as well as on the SACCH for voice calls. Apart from the calibration of the phase imbalance, and the monitoring windows, the “IF toggling” is active on every receive activation type. The reasons for those exceptions respectively come from the averaging the Layer 1 performs on phase errors responses during the RQPI operation (which would otherwise cancel out the measures), and the fact that monitoring and traffic channels can share the same ARFCN (which would otherwise prevent effective IF toggling on the serviced timeslot). The actual toggling is activated when the perceived SNR falls below the threshold listed in the SEEM_IQ_BALANCE table.

5) TRANSMITTER THEORY OF OPERATION

The TransAAM transmitter architecture is shown in Figure 5. It consists of the EDGE/GMSK TX modulator, Time/Scale Alignment circuit, TX synthesizer as part of a dual port modulated PLL, a TX VCO, an AM modulator, step attenuators, TRXQ, Digital Power control system, a 3 stage power amplifier, and a single pole six through RF antenna switch.

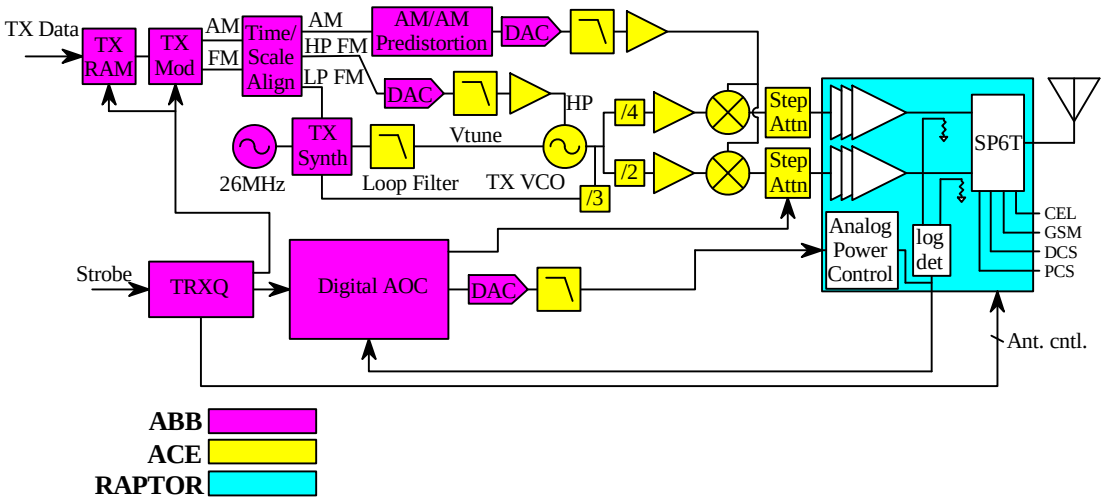


Figure 5: Transmitter Block Diagram

TransAAM uses polar modulation for EDGE mode. TransAAM performs all of the necessary pulse shaping, and maps the data bits into amplitude and phase components for the required modulation. The AM component is corrected to AM to AM distortion. No correction is required for AM/PM distortion since the AM modulator does not produce significant AM/PM distortion.

On TransAAM, POR programming sets up the registers listed in the POR section of this document. The values are directly derived from permanent data storage (SEEM_RF_DEFAULT_SPI).

The EDGE/GMSK Digital Transmit Module (TXM) supports two modulation schemes (GMSK and 8-PSK) and supports the Amplitude/Frequency polar modulator. This is done by having two different modulators, a digital CORDIC algorithm and a phase derivative block. The modulator supports GMSK and 8-PSK modulation per GSM specification 05.04. The output drivers can support AM/FM and AM/PM polar transmission. The symbols enter the modulator at a rate of ~270.8333 kHz (13 Hz/48). Each GMSK symbol contains 1 bit of information and each 8-PSK symbol contains 3 bits of information. For GMSK modulation, the initial state of the modulator and the final state of the modulator is assumed to consist of an infinite series of logic “1” data bits. For 8-PSK modulation, the initial and final state of the modulator is an infinite series of logic “111” symbols/data bits (This is marked ‘not defined’ in the GSM specification). The first 3 and last 3 symbols within a burst are called “tail bits”. These 3 symbols are always “0” for GMSK and “7”, i.e. 1,1,1), for 8-PSK. The start of the burst is defined as the center of the first symbol and the end of the burst is defined as the center of the 148th symbol. The useful part of the burst is therefore 147 symbol periods, even though 148 symbols are sent to the modulator.

TransAAM supports both GMSK and 8PSK modulations. The modulator is accessed by SCMA11 through the digital interface shown in Figure 6.

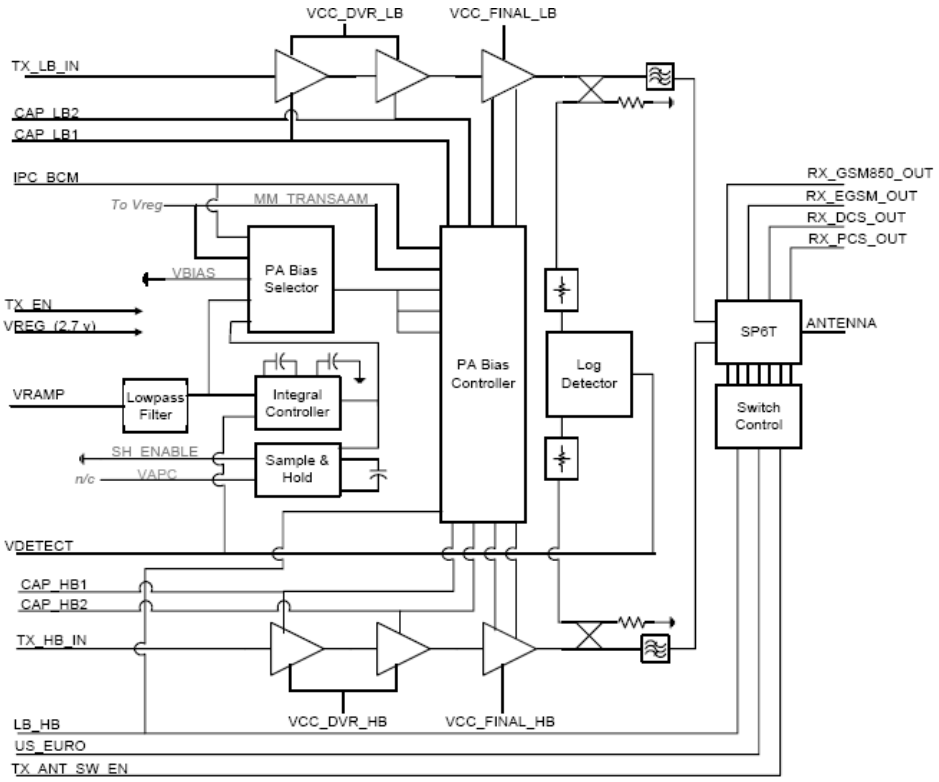


Figure 6: Digital Modulator Interface

6) RF-BASEBAND INTERFACE

Figure 7 describes interface between RAPTOR, TransAAm and SCM-A11. The connections include RF, analog and digital signals.

- RX signals flow from the antenna to TransAAM through RF switch inside the RAPTOR. These signals are filtered, amplified, mixed, converted to IQ and digitized before sending to the Base Band IC. The transmitter IQ is modulated directly into the TxVCO's, buffered then sent to RAPTOR for amplification.
- Vramp from TransAAM is used to control PA output power. This signal includes the amplitudes and timings of ramping up, final power level and ramping down of the TX burst. DAC values are programmed through SPI interface in the registers inside TransAAM. Vdetect from RAPTOR to SCM-A11 is used to monitor the power out of the PA.
- TXRXEN and TXRXDATA from SCM-A11 to TransAAM are serial digital TX modulation, and TX modulation enable signals. TXRXEN, and DBG_FRAME from TransAAM to SCM-A11 are digital serial RX data and RX data enable signals. SysClk from TransAAM to SCM-A11 is a digital clock. It is used as system clock of the radio as well as the TX and RX data transfer clock. SPI from SCM-A11 to TransAAM is used to program the TransAAM. Strobe is the timing control for both TX and RX modes.

The industry standard "DigRF" digital BB/RF interface requires 8 pins to be connected between Baseband IC and RF IC to support GSM/GPRS/EDGE. DigRF interface consists of 3 interfaces:
a) Rx/Tx Data Interface b) Control Interface c) Master Clock Interface

MQSPI provides DigRF control interface. This is a 3 wire interface (CtrlClk, CtrlData & CtrlEn lines) with MQSPI as master.

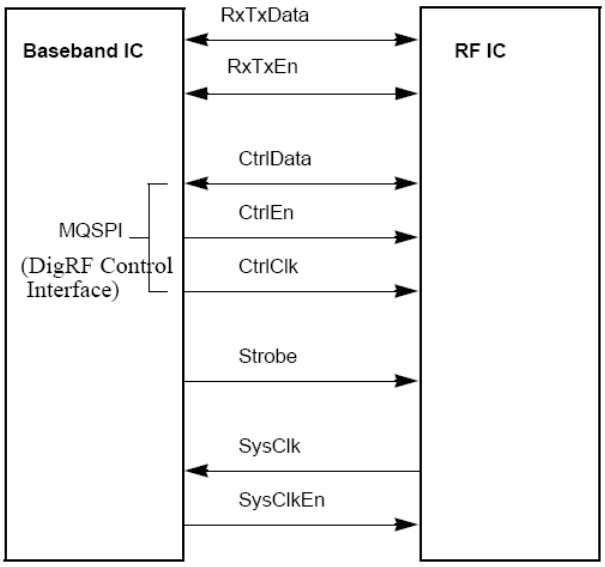


Figure 7: RF-Baseband Interface

7) POWER DISTRIBUTION

The majority of phone power is supplied by linear or switching regulators on the Atlas power management IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and other noisy circuitry. The regulators and their respective loads are listed in Table 3.

VMAIN, 1.2V	SCM-A11 DVDD for AP/BP Core
VDIG_1.8V, 1.8V	SCM-A11 logic, Atlas SPI bus, Imager core and IO, NAND Flash, SDRAM, Bluetooth IO, Serializer & Deserializer, Display, Hall Effect, USB HS IO VCC, Antenna Logic
VBOOST, 5.0V	Display backlights, Keypad backlights, BT LED, USB High Speed, VFUSE, VINBUS,
VIOLO, 1.8V	Atlas logic
VIOHI, 2.775V	SCM-A11 UART3 and USB, Atlas USB, Main LCD driver, Batt_Data Pull up, Serializer & Deserializer, Antenna Logic
VRF1, 2.775V	TransAM VDD_ACE, TransAM VDD_CP
VRF2, 2.775V	TransAAM TXRX, TransAAM LVDD, Raptor VREG
VRFDIG 1.875V	TransAAM QVDD and JVDD, SCM-A11 VDD_BBP, VDD_L1T.
VRFCP, 2.775V	TransAAM VDDA, SCM-A11 QVDD
VAUDIO, 2.775V +/- 3%	Atlas audio circuitry
VCAM, 2.8V	Imager analog
VSIM, 1.8V	SIM circuitry, SCM-A11 VDD_SIM.
VUSB, 2.775V	USB transceiver inside Atlas
VTFLASH, 2.9V	Bluetooth PA, 2GB Memory, SCM-A11 VDD_SDIO
VATLAS, 2.775V	Atlas core circuitry
VVIB, 1.3V	Vibrator motor

Table 3: Voltage Regulators

8) CLOCK GENERATION

ATLAS provides a 32 kHz clock used for power savings and real-time clock (RTC) operations. The clock frequency comes from either an internal RC Oscillator or an external 32.768 kHz crystal. The RC oscillator will be used to run the de-bounce logic, PLL, and internal control logic. The 32 kHz oscillator is powered at all times when a valid voltage source is applied to either battery, USB power or the coin cell battery for RTC maintenance. The square wave output of the oscillator is also used to put the unit into low power operation. This system is shown in Figure 8.

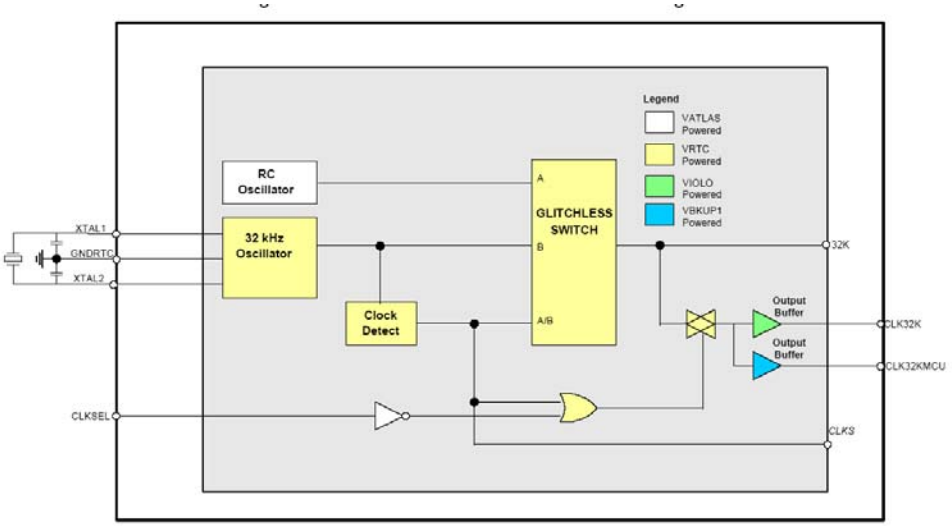


Figure 8: Atlas 32 kHz Clock Generation

9) ATLAS TRANSMIT AUDIO

The mobile phone supports an internal and external microphone. The input path is identified and selected by the MUX controller and path gain is programmable at the PGA. The internal microphone is an active, single ended surface mount part. The internal mic is biased by MC1RB (MIC BIAS 1 of Figure 9) of Atlas. The MC1RIN (MIC_INM of figure 8) signal is routed to the A3 amplifier. The external mic complies with the CEA-936-A spec and is connected through the EMU (mini USB) connector, and muxed on the USB D+ line.

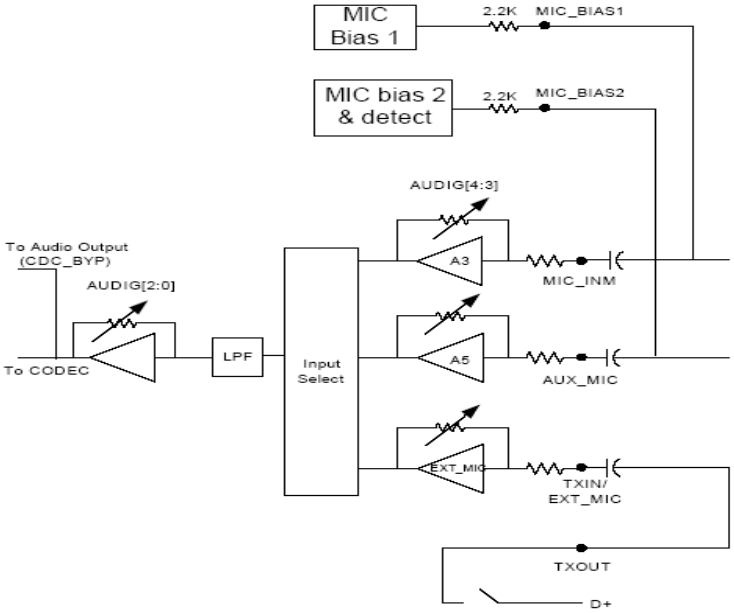


Figure 9: Atlas Transmit Audio

10) ATLAS RECEIVE AUDIO

The mobile phone supports three audio output paths. The output of Atlas's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the three supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (handset earpiece speaker), the ALERT amplifier (handset loudspeaker/alert speaker), and the CEA-936-A output for external speaker (headset speaker). All outputs use the same D/A converter so only one output can be active at one time. There are certain use cases that require a headset and loudspeaker to output the same signal. In this scenario, the headset PGA gain will be used for both outputs. Output gain is adjusted via volume control buttons.

The handset speaker is driven by Atlas's internal SPKR differential amplifier. Following the speaker path, the pins SPM (speaker minus) and SPP (speaker plus) are connected to the transducer.

The headset uses a standard micro-USB connector. The headset may contain a momentary switch, which is normally open and connected to the USB ID line. When the momentary switch is pressed, the ID line is shorted to ground. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number. The headset speaker is driven by Atlas's internal USBAMP.

The alert transducer is driven by Atlas's single LSPL signal via a Class-D amplifier with differential output ALRT+/-. The alert path from the class-D pins ALRT- and ALRT+ are routed directly to the alert transducer. ALERT+/- drives a 4 ohm speaker for a 1 watt output.

11) BATTERY CHARGING SYSTEM

The AURA R1 Dual Path Charging system is designed to supported removable Lithium Ion & Lithium Polymer batteries and to be compatible with existing P2K05 (USB Bus) charging accessories.

During power up, the SCMA_11 will check the EPROM located inside the battery package through One-wire bus (batt_I/O) to determine battery validity and characteristics that impact phone and charging operations. Internal thermistor element in the battery provides temperature feedback.

Figure 10 shows how the current flows to the battery within a phone using ATLAS IC.

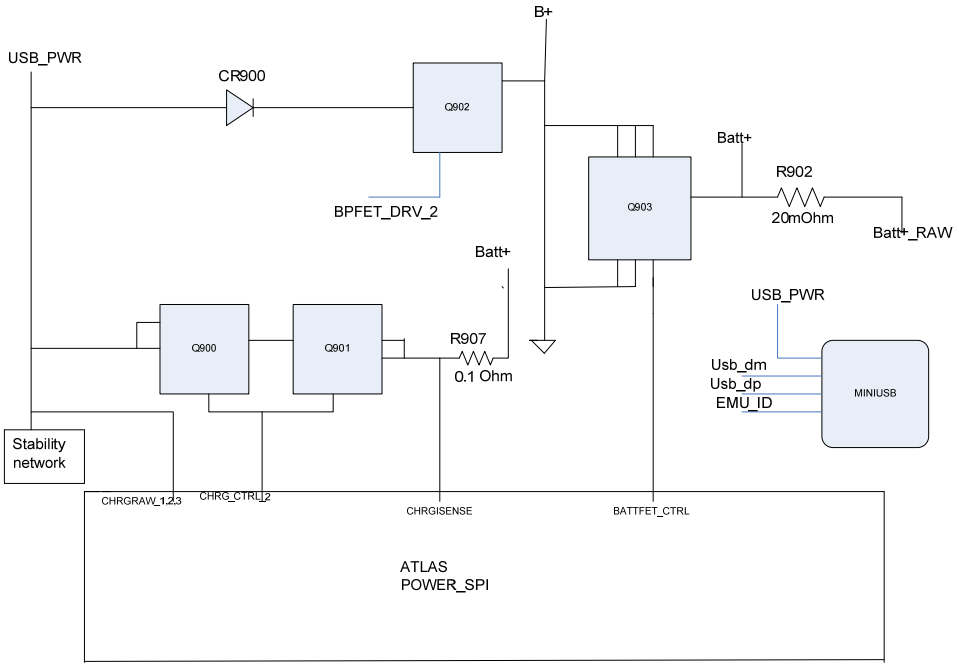


Figure 10: Charger Block Diagram

The purpose of the internal charger is to provide constant current and voltage regulation to supply current to the battery in order to reach full charge. Battery charging is enabling (via software) by turning on the P-Ch MOSEFET (Q900, Q901). These FET'S control the voltage going into battery and limits the maximum current from charger input to battery. They are used as combine pass device and have programmable output set by the VCHRG [2:0] bits and programmable current limit set by the ICHRG [3:0] bits. Also a 0.1 ohm external resistor (R907) is used as the current sense element, where the voltage drop is measured between the CHRGISENSE and Batt+ nodes by the ATLAS. Using the value of Res = 0.1 ohm, Ibatt = (Vchrgisense – Vbatt+) / 0.1 ohm. CHRG_CTRL is the dc signal which controls the gate of Q900 & Q901.

The charge regulators allow a maximum charge rate of 1000mA during normal charging condition, where charge current will ramp down when Vbatt+ equals 4.2 Volt. Charging will stop when current goes below 50mA defined in the battery EPROM data.

The BP regulator (Q902) operates as a voltage regulator and limits the voltage going to B+ from the charger/USB input to between 4.1 and 4.5 volts. The main FET (Q903) is a switch used to selectively connect the battery (Batt+) to B+. A Schottky diode CR900 is used to prevent reverse leakage current from the battery to USB_PWR pin on MINIUSB bus. The stability network is required when charging battery with long charger cables. The network consists of capacitors and resistors to decouple the inductance from long charger cable which causes unstable current regulation during charging.

The over voltage protection function protects the ATLAS from an over voltage condition by shutting off the charge path regulator by opening Q900 & Q901 and for dual path, shutting off the B+ regulator by opening Q902. When OV condition is detected, an interrupt CHOVI is generated and software will disable all regulators.

AURA R1 supports two types of charging operations:

- Charge Only Mode Operation: When the phone is off (with or without a battery attached), the phone will go into charge only mode when external wall charger is attached. In this condition, the phone stays off and “charging battery “state is indicated on the display.
- Normal Charging Operation: The states of all FETs in normal operating mode are shown in Table 4.

Event	Q900	Q901	Q902	Q903	Comments
Battery Present (no charger)	OFF	OFF	OFF	ON	Phone turns on
Mid-Full rate Charger Present	ON	ON	ON	OFF	Software detects battery validation and configures the charging regulators .
PC USB Cable attached	ON	ON	ON	OFF	Software detects battery validation, pc usb cable and configures the charging regulators .

Table 4: Charging FET States

12) SCM-A11

The SCM-A11 is a baseband and application processor for the 2.75G GSM market. A block diagram is shown in Figure 11.

Baseband Core:
The Baseband Processor (BP) modem core is the V3 version of the SC140. The SC140 core is a flexible programmable DSP core which enables the emergence of computational intensive communication applications by providing exceptional performance, low power consumption, efficient, compilability and compact code density. The SC140 core efficiently deploys a variable-length execution set (VLES) execution model which utilizes maximum parallelism by allowing multiple address generation and data arithmetic logic units to execute multiple instructions in a single clock cycle. Departing from commonly used dual Core based BP modem where the DSP does Layer 1 processing and MCU takes over Layer 2 and Layer 3 processing, Starcore can perform the entire layer 1, 2 and 3 processing for Baseband IC.

ARM Core:
The ARM1136 Platform consists of the ARM1136JF-S processor, the ETM real-time debug modules, three AHB Nexus modules along with NPC/NCG, a 6x5 Multi-Layer AHB crossbar switch, and a "primary AHB" complex. The instruction and data read/write buses (I_AHB,DR_AHB,DW_AHB) of the ARM1136 processor are connected to the slave ports S0, S1, and S2 of the L2CC. The L2CC master ports M0 and M1 are connected to the crossbar master ports M0 and M1 respectively. The P_AHB ports is connected to the master port M2 via a PAHBMUX. All other AP bus masters (the alternative bus masters) are connected to master ports M3, M4, and M5 of the crossbar switch.
The five slave ports of the crossbar are AHB-Lite compliant buses. Slave port S0 and S1 are connected to the shared external memory system and slave port M2 is connected to the Image Processing Unit. S3 and S4, the remaining two slave ports, are connected to AIPS-A and AIPS-B which provide interfaces between the AHB-Lite 2.v6 bus and the IP Skyblue interface (IP-Bus). The platform supports realtime trace through three AHB Nexus modules and ETM, JTAG-based debug.

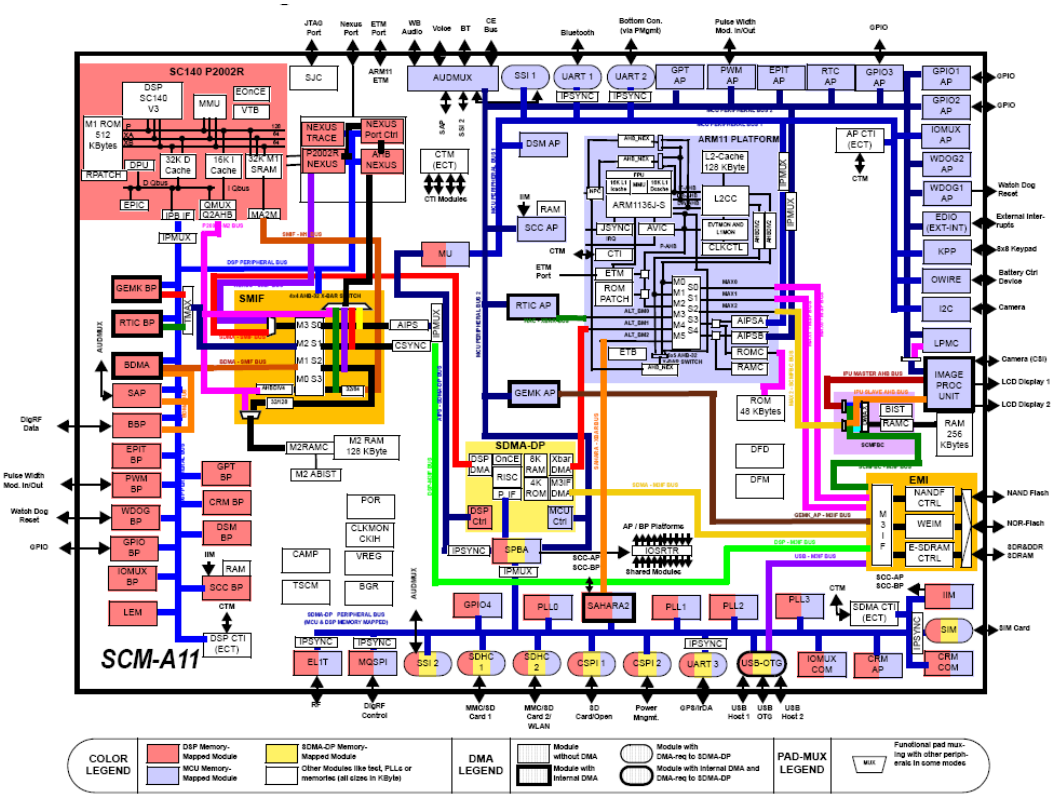


Figure 11: SCM-A11 Block Diagram

13) MEMORY INTERFACE

The EMI is the External Memory Interface, i.e. EMI controls all IC external memory accesses (read/write/erase/program) from all the masters in the system, through port interfaces (MPG, AHB 32 bit) toward different external memories. All accesses are arbitrated by the Multi Master Memory Interface (M3IF) and controlled by the respective memory controller. The EMI encloses the Multi Master Memory Interface (M3IF) and different external memory controllers in order to support several memory devices;

- M3IF - Multi Master Memory Interface.
- ESDCTL/MDDRC - Enhanced SDRAM/MDDR memory controller.
- NFC - NandFlash memory controller.
- WEIM - SRAM/PSRAM/FLASH memory controller.

The M3IF - ESDCTL/MDDRC interface is optimized and designed to reduce access latency by generating multiple accesses through the dedicated ESDCTL/MDDRC arbitration (MAB) module, which controls the access towards/from the Enhanced SDRAM/MDDR memory controller.
For the other memory interfaces, the M3IF only arbitrates and forwards the masters requests received through the Master Port Gasket (MPG) interface (and M3IF arbitration) toward the respective memory controller. When a master request a memory access, the access will immediately be taken by the M3IF if no other access is in progress. The M3IF forward the access toward the respective memory controller (slave), and depending on the respective memory controller state a command to the memory will be generated. If the access can't be started due to a previous active access, the master request pends ("HREADY" held negated) until it will be

executed by the memory controller. When the access execution is completed the HREADY will be asserted and a new request can be processed.

The EMI includes these distinctive features:

- Multi Master Memory Interface (M3IF)
  - Supports multiple requests from 7 masters through input ports interfaces;
- Master Port Gasket (MPG) - ARM11 AMBA AHB lite bus protocol.
  - Supports memory "snooping", i.e., monitor a region (from 2KB up to 16MB) in external memory for write accesses.
  - Supports memory watermark protection for up to 8 different chip selects for preselected (by hardware) masters.
  - Enables AHB accesses to three different memory controllers (that share some of their I/O pads, through the EMI AHB MUX and EMI I/O MUX)
- Enhanced SDRAM Controller (ESDCTL) or MDDR Controller (MDDRC)
  - Up to 2 chip selects (due to PADS sharing all 2 chip selects are supported only in case that WEIM CS2 and CS3 are not is use).
  - Support 32 bit (only by using the stacked die pads) SDR SDRAM (up to 2Gb @133 MHz)
  - Support 32 bit (only by using the stacked die pads) MDDR SDRAM (up to 2Gb @ 266 MHz)
- NandFlash Controller - (NFC)
  - 8/16 bit NANDFLASH (up to 2GB address space)
  - 2K RAM Internal Buffer
- Wireless External Interface Memory Controller - (WEIM)
  - Up to 6 chip selects (due to PADS sharing all 6 chip selects are supported only in case that both ESDCTL/MDDRC chip selects are not is use).
  - Support 16 bit SRAM memories.
  - Support 16 bit PSRAM (up to 133 MHz) memories.
  - Support 16 bit (NOR) FLASH memories

14) KEYPAD INTERFACE

The Keypad Port is a 16-bit peripheral, used generally for keypad matrix scanning, or as a GPIO port up to 16 bits wide. The keypad matrix can be configured up to 8 rows by 8 columns, with unused pins as GPIO's. For this phone, the keys were remapped in order to optimize the number of signals going to the Slide module. All rows shall be set as inputs at all times. Columns shall be set as outputs driven low when there are no key presses detected. Pressing a key will short a row to a column driving the row low and generating an interrupt to the SCMA11 processor. At this point, all columns will be set as inputs and progressively scanned low (set as an output driven low in a sequential fashion with only one column driven low at any point in time) to determine the key that is pressed.

15) SIM INTERFACE

The SIM interface block is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards. The card itself stores important information including the subscriber telephone number, phone numbers, the users' PIN, and other information to be able to complete a phone call. The card holds all this information for the user and therefore must be protected from electro-static discharge that could destroy the card. We prevent this event by also requiring the user to attach a battery. Batteries on some Motorola products are arranged in such a way to fully cover or block the SIM block. The SIM block has two ports that can be used to interface with the various cards. The interface with the MCU is a 16-bit connection via the AIPI Controller and the IP-Bus Interface. Figure 13.1 shows the signals and direction of propagation between the different device modules.

ATLAS can supply the SIM block with either 1.875 V or 3.0 V. The bit VSIM_0 determines the voltage. This is bit number 18 in the AUX_VREG register (location 07). The 5 V SIM cards are not supported with this architecture. The VSIM regulators on and off state will be controlled by one SPI bit (VSIM_EN) and one external pin (SIMEN). SIM1_SVEN is a pin on SCMA-11 that connects to the VSIM_EN pin of ATLAS. The SIM regulator will be on only when the SIM_VCCEN pin and the VSIM_EN SPI bit are logic high. The voltage supply to the card must be shut down before the SIM card is removed and the card loses contact with the radio. Because of the nature of the removable SIM card the SIM regulator must be able to withstand a short circuit at its output without sustaining any damage. The SIM module contains a block designed specifically for generating the clocks used internal to the SIM module, and the clocks provided to the SIM cards. There are no interrupt sources generated by the SIM clock generator block. The SIM Transmitter block contains a transmit state machine, transmit shift register, and a transmit FIFO. The SIM Receiver block contains a receive state machine, receive FIFO, and control logic. On power up, the phone checks for connected accessories and for the validity of battery voltage. If the battery voltage is valid then the SIM Card is secure and the phone attempts to read data from the SIM on the SIM_I/O line. If no data is read then that indicates that a card is not present and S/W should write “CHECK CARD” to the display. The SIMPD input allows for detection of the insertion or removal of a SIM card. A mask-able interrupt can be generated when a SIMPD event occurs. An internal 69k pull-up is present on the SIMPD pin for SCMA-11. This will provide for a high to low transition on the SIMPD pin when a SIM card is removed. The SIM port control block contains hardware that provides the correct sequence to power down a SIM card. The software must perform the power-up sequence:

- RST transitions from high to low
- CLK is turned off to a low
- I/O transitions from tri-state to low
- SIM Vcc is turned off

The SIM module is capable of forcing a SIM card power down. It is similar to the auto power down feature, except that it is not dependent upon either the state of the SIM card auto power down enable bit, or triggering of a presence detect event.

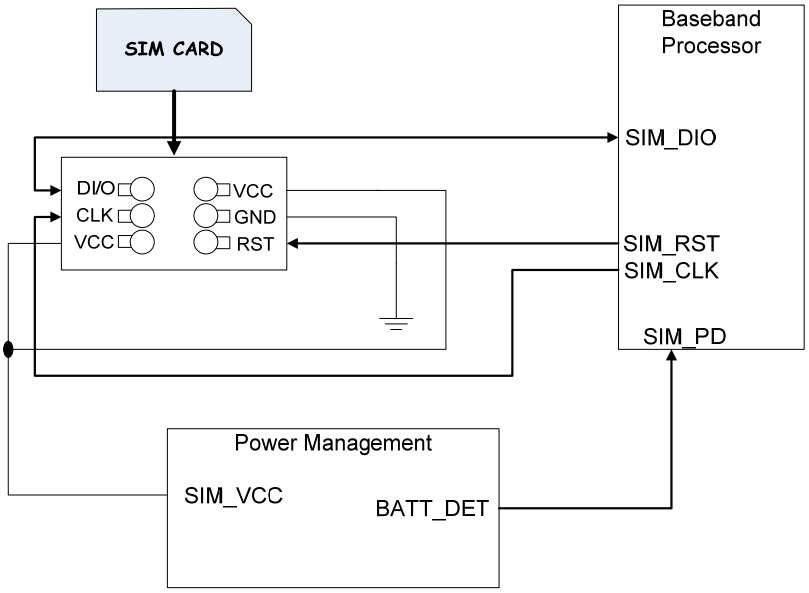


Figure 12: SIM Interface

16) USB 2.0 INTERFACE

The USB High Speed interface is designed to allow fast downloads to the storage device of a mobile phone from a desktop computer. It is required that the path between the computer and phone's storage device be optimized for efficient transfer of data in both directions.

The FX2LP USB-HS controller can be accessed by the phone's microprocessor as a memory mapped device and be used as a USB-HS controller. It is possible to make the phone appear as a mass-storage device, MTP device, high-speed modem etc to a desktop computer using FX2LP. All data to/from the desktop computer will be transferred to/from FX2LP to the microprocessor.

FX2LP contains an 8051 processor embedded within it. As FX2LP does not contain any ROM code firmware for 8051 needs to be loaded into its internal RAM before the part can be initialized and USB functions accessed. This firmware is loaded into FX2LP using its I2C interface in "Master" mode. The FX2LP's firmware resides in system FLASH (approximately 16KB).

A USB switch will be used to switch between FX2LP and Atlas to EMU connector. The default position of the switch will be in Atlas position to allow backward capability with existing USB full speed (FS). Accessory detection will take place through Atlas and EMU interface without any changes. In case the phone is in an OFF state and a charger jack or mini-USB jack from a computer cable is inserted into EMU connector the USB switch will default to the position connecting D+/D- of EMU connector to Atlas. Existing USB-FS interface using the full-speed USB transceiver in Atlas and USB-FS host/device controller in microprocessor is still supported on the hardware level.

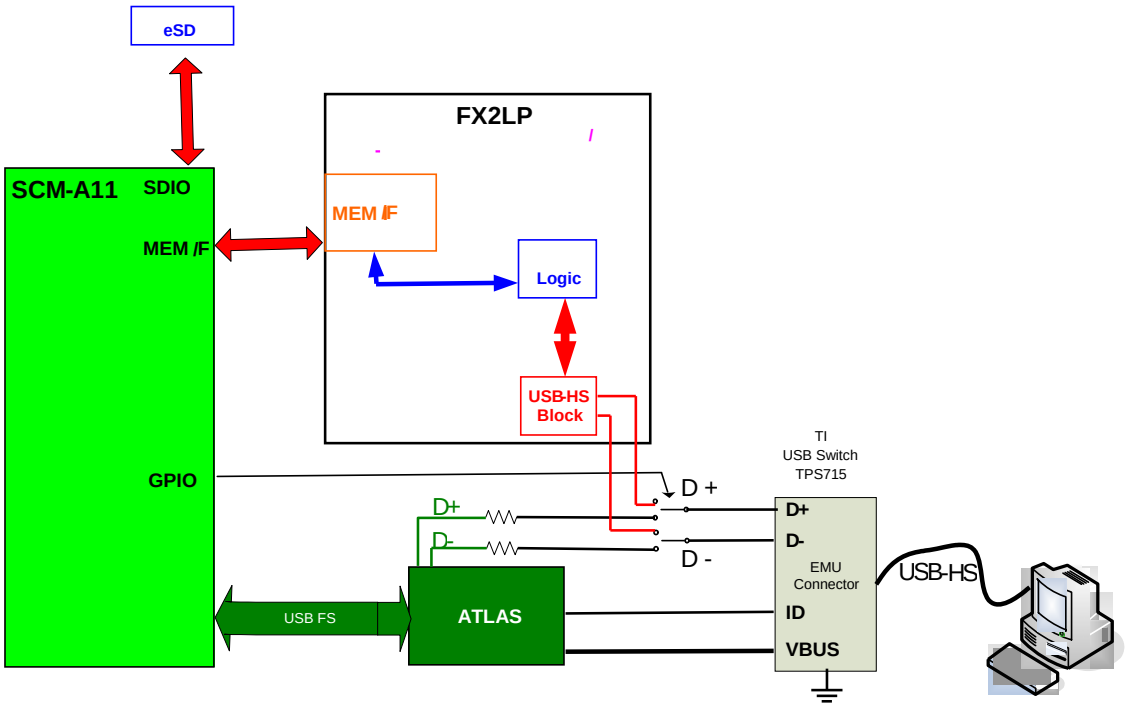


Figure 13: USB 2.0 Interface Block Diagram

17) ROTATOR INTERFACE

The AURA R1 rotator assembly contains the display, a rigid flexible printed circuit board assembly, and two magnets (one North aligned, one South aligned) to trip the Hall effect sensor mounted on the main transceiver board. In order to reduce the number of signal lines needed to connect to the main printed circuit board (PCB), the display data lines are serialized and transmitted as differential clock and data signals (23 signals are reduced to 4). The deserializer IC is on the rotator PCB and drives the display driver IC directly. The block diagram of the rotator circuitry is shown in Figure 14.

The AURA R1 display is a 480 pixel diameter TFT liquid crystal display (LCD). The display is driven by a smart display driver with embedded RAM, supporting up to 24 bits per pixel. Data is transferred to the display using a MCU (6800 type) interface.

The rotator PCB assembly connects to the main PCB through a 30 pin micro-coax assembly and contains the display deserializer, Bluetooth LED indicator, sign of life LED indicator, charging LED indicator, 2GB embedded MMC NAND memory, and the earpiece speaker. The Bluetooth and sign of charge LED's are sourced by VBOOST and sunk by LEDB1 and LEDG1, while the sign of life LED is sourced by USB_POWER and sunk by CHRGLED. The deserializer VDDA and VDDS pins are sourced by VIOHI while VDDP is sourced by VDIG_1.8V. The display module connects to the rotator pcb assembly through a 40 pin board to board connector and contains the display data signals as well as the display backlight LED's power and sink lines. The four white LEDs providing the display backlighting are sourced by VBOOST(SW3) and sunk by LEDMD1 to LEDMD4 respectively. The display VCI voltage is sourced by VIOHI, while the VDDI voltage is sourced by VDIG_1.8V.

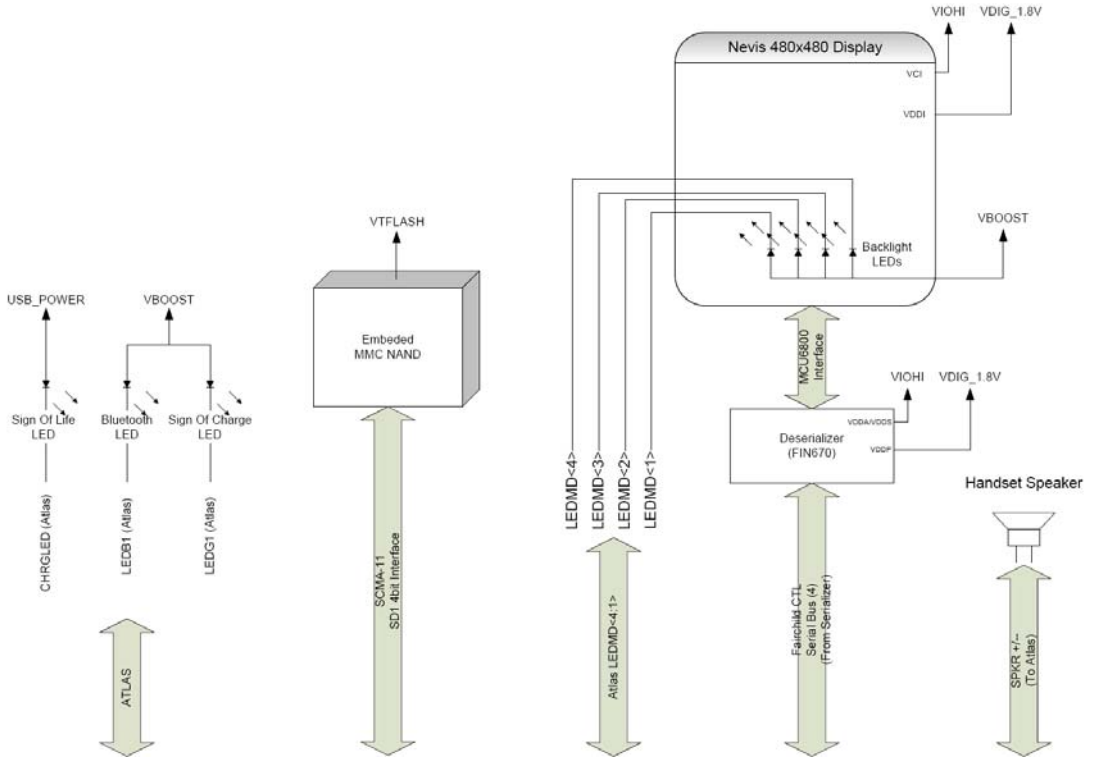


Figure 14: Rotator Block Diagram

18) BLUETOOTH

The AURA R1 supports Bluetooth Version 2.0+EDR and operates at Class 1 power levels for enhanced reception quality. It utilizes the BCM2046 Bluetooth integrated circuit. The Bluetooth system block diagram is shown in Figure 15.

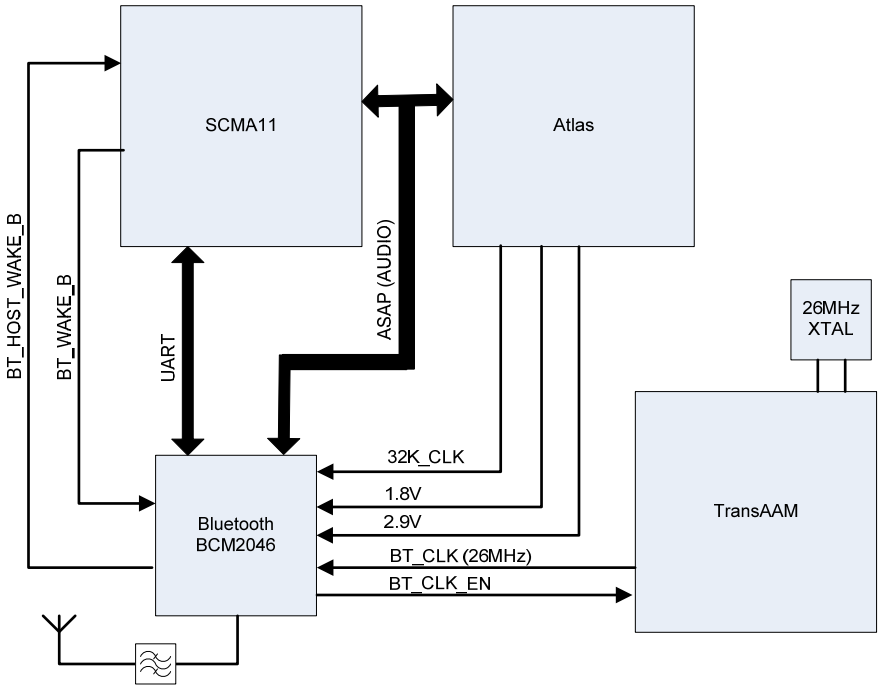


Figure 15. Bluetooth System Block Diagram

The HCI interface utilizes a UART. There are two data signals (TXD and RXD) and two flow control signals (RTS and CTS). The BCM2046 assumes a role as DTE and SCMA11 acts as a DCE. Therefore, when the BT module is connected to SCMA11, the RXD and TXD lines must be crossed, while CTS and RTS on SCMA11 connect directly to CTS and RTS on the BCM2046. RXD and TXD have been crossed on the BT module already; therefore, BLUE_TX of the BT module is connected to TXD2 and BLUE_RX of the BT module is connected to RXD2 on SCMA11. The Bluetooth UART is a dedicated UART from SCMA11. This bus is not shared with external peripherals. Although most signaling is done over the HCI, wakeup signaling is done with dedicated signals. SCMA11 uses a GPIO to wake up the BT IC. The Bluetooth IC uses a dedicated signal BT_HOST_WAKE_B connected to a SCMA11 interrupt to wake-up the host processor.

The codec is connected onto a shared 4 wire bus with SCMA11 and Atlas referred to as the BB_SAP (Base Band Serial Audio Codec Port). Atlas acts as the master and provides the clock and frame sync signals for the bus.

Bluetooth is reset in a number of different ways. When software first initializes Bluetooth, it sends an HCI reset command over the UART interface to place the BCM2046 into a known state. If software fails to detect a response to the initial HCI reset command, it will power cycle the RF and core voltages thus forcing a power-on-reset on the BCM2046. Additionally, SCMA11 can reset Bluetooth using the BT_RESET_B signal. BT_RESET_B is connected to VREG_CTL of the BCM2046 IC. To ensure reset, VREG_CTL must be driven low for minimum of 100 microseconds.

The BCM2046 requires two different frequency references, a lower frequency low power reference (32.768 kHz), and a high frequency main reference (15.36 MHz, 26 MHz, etc.). The low power reference is a standard frequency available on the GSM phone whenever the phone is powered. As such, this reference is directly connected to 32K_CLK, the buffered port from the oscillator on Atlas.

19) CAMERA

AURA R1 uses a 2.0 MP imager that runs on a clock from SCMA11 and runs at 15fps in normal lighting and 7fps in night mode. The imager interface to SCM-A11 is shown in Figure 16. An I2C interface is used to send control data to the sensor and read back status from the imager.

The imager allows for still images as well as video imaging. Imager modes are:

- Four digital zoom levels: X1, X2, X4, X8
- Color styles: Black and white, Antique, Negative, Reddish, Greenish, Bluish
- Borders allows for a time/date stamp
- Scene: Automatic, Night, Manual.

Manual setting allows for exposure settings and lighting conditions of Automatic, Sunny, Night, Cloudy, Indoor (Home), Indoor (Office) The imager has either a 5 or 10 second timer, and a 4, 6 or 8 shot multi-shot setting. mages are stored to internal memory.

Picture resolutions are X-Small (240 x 320), Small (480 x 640), Medium (1024 x 1280), and Large (1200 x 1600). Picture quality can be Good, Better, or Best.

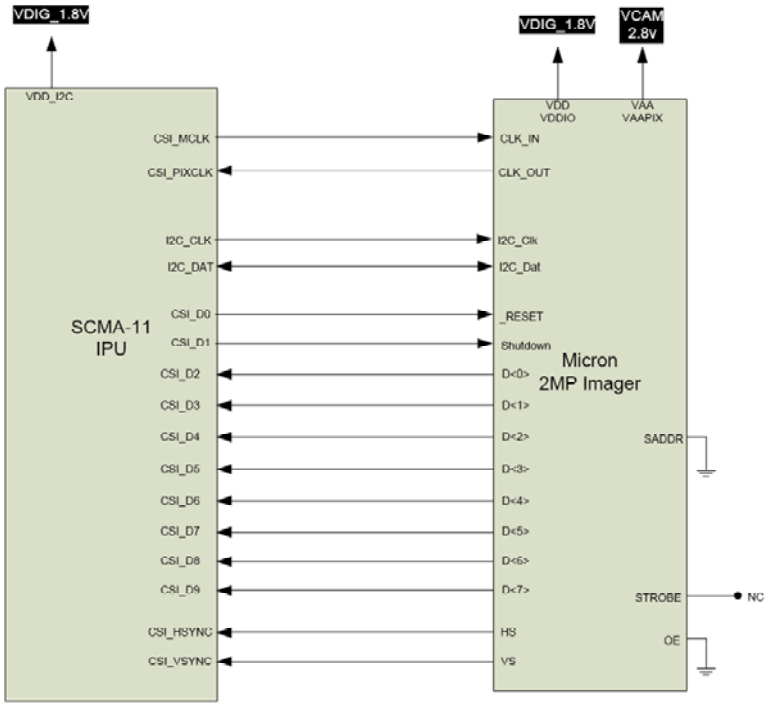


Figure 16: Imager Interface