Service Manual

Level 3

Draft 1.0

MOTOROLA™

DIGITAL WIRELESS TELEPHONE

Model A845

UMTS 1900MHz/PCS 1900MHz/DCS 1800MHz/GSM 850MHz

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Table of Contents

3G Flash Procedures

Introduction

This document is intented to decribe the flashing(software updates) procedures for 3G terminals. The 3G terminal described in this document will be limited to the A845.

Software updates need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the correct software is programmed.

Software updates allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific circumstances, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the 3G terminal.

Power Hardware

1. Fully Charged battery (SNN5638A)

2. Full-rate Charger (PSM5049A)

Interface Options

1. USB Data Kit (S8951)
   USB Cable (SKN6311A)
   Data Software CD

2. RS232 Data Kit (S8952)
   RS232 Cable (SKN6315A)
   RS232 to CE converter (SYN0279B)
   Data Software CD

Software Requirements

The Product Support Tool (PST) is used to allow functions such as flashing, flexing, and memory transfers. Contact your local Motorola service representative to receive download information for the PST and related support files.

For download information on Flash software, contact your local Motorola service representative.

Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1-1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a non-functional (Bricked) 3G terminal.

The A845 contains a Flash EPROM with a total memory of 16MB. The memory resides within two 8MB Intel EPROMs connected in parallel.

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery
2. Full-Rate Charger w/battery (recommended)

If the user decides on using the battery only solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the fhash process. This action may cause unrecoverable failures to the 3G terminal.

Hardware connection solutions

There are two types of hardware solutions to perform a flashing procedure.

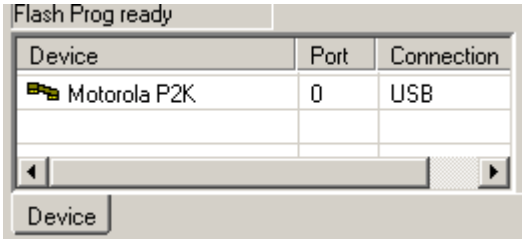
1. USB configuration (recommended)
2. RS232 configuration

RS232 configurations should be used only if the PC is running an operating system (OS) that doesn't support the USB interface. USB configurations will provide a faster data transfer rate than RS232. As a result, flash durations will be reduced when using a USB connection.

PST Flash Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal.

1. Download the desired flash software into the computer.
2. Connect the desired hardware configuration as illustrated in figure 1.
3. Power up the 3G terminal
4. If the 3G terminal doesn't power up, refer to the Force Flash section.
5. Launch the PST application by choosing Start/ Programs/Motorola PST/Flash & Test Commands.
6. Click on the Browse button and select the desired flash software
7. Select the device that will be flashed



8. Once the 3G terminal is placed in flash mode, the Flash button will be enabled.

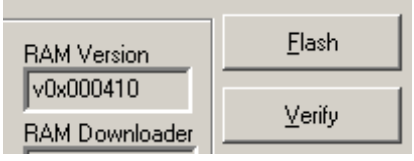


Figure 1-1. PST Hardware Configuration

9. Click on the Flash button to begin flashing. DO NOT interrupt any hardware connections during the flash process. Connection interuptions may cause the flashing process to fail and render the 3G terminal non-operational.

10. When flashing is complete, a message will pop up stating," Flash another phone?". At this time you may safely disconnect the 3G terminal and select the appropriate response.

11. Power up the 3G terminal to insure that the flash procedure was successful.

Force Flash Procedures

The procedures described in this section apply only to situations where the 3G terminal will not initiate it's normal power up sequence, but may recover functionality by a repeat flash procedure.

There are three possible alternatives to place the 3G terminal in force flash mode.

Key Hold Solution

Hardware: Refer to Figure 1 (USB solution)

Step 1. Remove the battery from the 3G terminal

Step 2. Prior to connecting the USB cable, press and hold the "*" and "#" key from the 3G terminal

Step 3. Attach the USB cable

Step 4. Verify that the PST application detects the 3G terminal, if it's not detected, press and hold "*" and "#" once again.

Force Flash USB Cable Solution

Hardware: Refer to Figure 1 (USB solution), except, replace USB cable (SKN6311A) with force flash cable (SKN6168A)

Step 1. Connect the force flash cable in the same manner described in Figure 1.

Step 2. The 3G terminal will automatically be placed in force flash mode. There's no need to press the power key. The PST application will now detect the 3G terminal

Handset Test Commands

Introduction

The Handset Test Command mode of the phone is provided primarily for service personnel without access to equipment capable of exercising Test Commands over a computer connection. This mode collects input from the user and packages it in the format required by the Test Command component within the phone.

User Interface

Three screens are used, as described below, for command data entry and command response display: the opcode entry screen, the field entry screen, and the command results screen. The following screen flow diagrams do not depict an actual test command, but instead demonstrate the general behavior of the mode.

As the phone does not provide an easy method of hexidecimal entry, all input and output will be in decimal format, with the exception of output fields considered to be data streams. This requires careful consideration as a significant portion of this document is described using hexadecimal format. As an aid in the decimal entry of opcodes, Table 1 is provided which indicates the decimal equivalent number for supported opcodes.

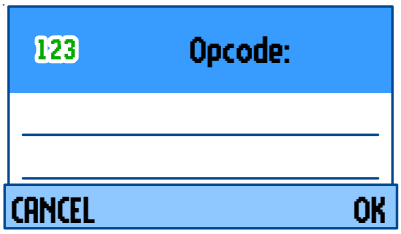
The END key exits handset test command mode or restarts the phone (if suspended). However, pressing the END key in the waiting for results screen (a "frozen" version of the final entry screen) has no effect, though the power key still allows the phone to be powered down.

Handset Test Command Mode Entry

The mode is entered using a key shortcut, "<MENU> 0 HTCMD *".

The user will be taken to the initial screen (the opcode entry screen).

Figure 2-1. Opcode Screen



The mode may only be entered from the idle screen. Entry is not allowed while an active computer test command session exists (ie RS232 or USB); an error will be displayed if a computer session is active.

When the handset test commands feature is invoked, the handset is not suspended by default. The handset can only be suspended by executing the SUSPEND test command. The user can exit the feature and return to idle if the handset has not yet been suspended. Otherwise, exiting the feature will cause a restart.

Command entry

Once the mode is entered, two screens are used to collect command request information from the user. The opcode entry screen (Figure 5) allows the entry of either an entire command as described in this section, or entry of a partial command. If a partial command is entered, the user will be prompted to enter the remaining required information via an appropriate number of field entry screens (Figure 7). Pressing OK with no data entered in the opcode or field entry screen will cause a parse error (unless the field is optional).

The asterisk is used to delimit fields on the opcode entry screen and is not allowed on the field entry screen. On the opcode entry screen, it is not legal to have an asterisk immediately follow another asterisk.

Opcode entry

The opcode entry screen allows the user to enter the opcode for the test command, or the opcode plus additional parameters delimited by the * character.

Figure 2-2. Opcode Entry Screen

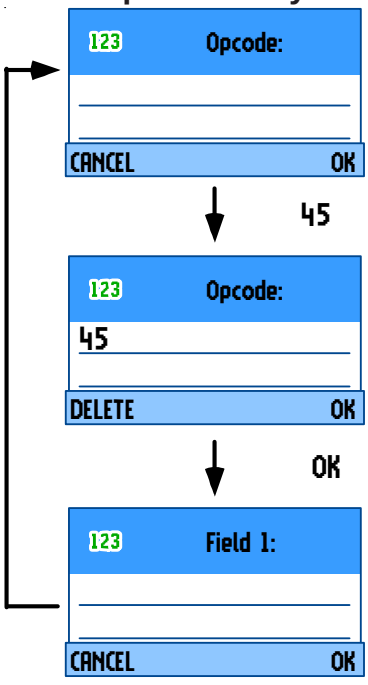
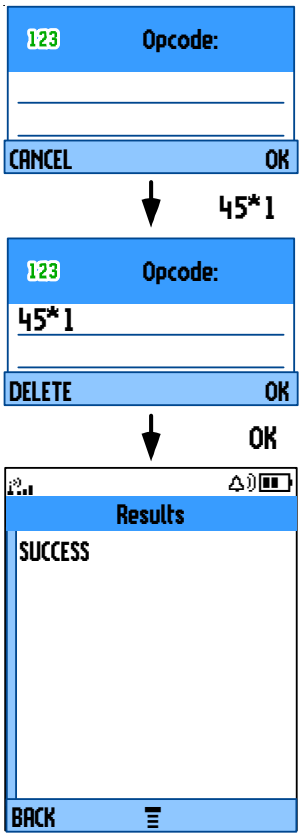


Figure 2-3. Multiple Parameter Entry



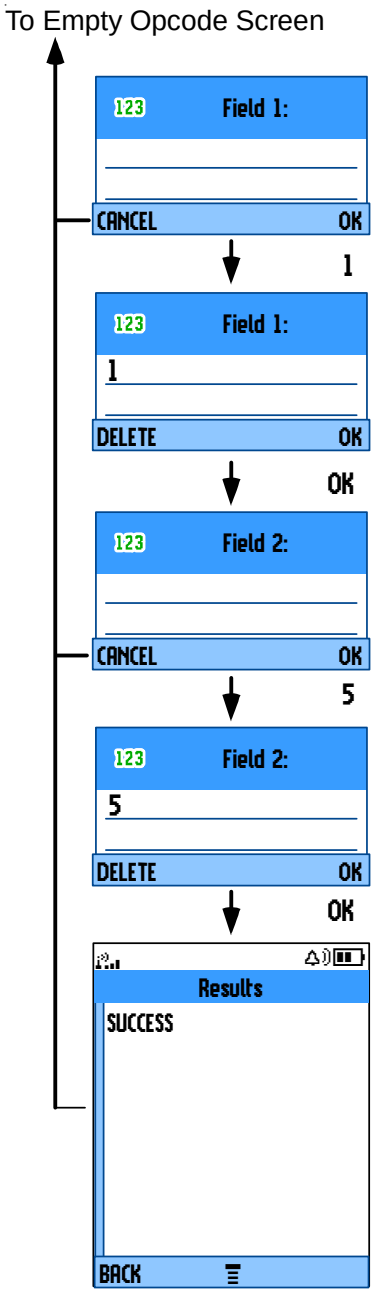
Opcode Entry Screen Keymap:

0-9: command data
*: field delimiter
OK: process value, move to next screen
DELETE (short): delete single char
DELETE (long): delete all chars
CANCEL: return to idle or restart if suspended
End: return to idle or restart if suspended

Field entry

The field entry screen allows the user to enter fields for the test command separately from the opcode. Each field entry screen allows only one field to be entered. The user will be led through the remaining parametersone by one until the command is completed.

Figure 2-4. Field Entry Screen



Field Entry Screen Keymap:

0-9: command data
OK: process value, move to next screen
DELETE (short): delete single char
DELETE (long): delete all chars
CANCEL: return to opcode entry screen
End: return to idle or restart if suspended

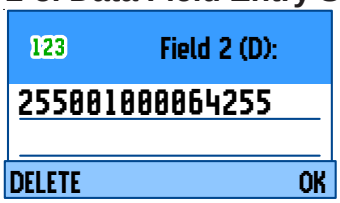
Numeric Field Entry:

Fields are numeric by default. The digits entered for the field will be evaluated as a single decimal number.

Data Field Entry:

The user must enter 3 digits for each byte of a data field (variable or non-variable length). Zero padding is required if all 3 digits are not required to represent the value. Any data field which is not a multiple of 3 digits will generate a parse error. The field title of any data field will be tagged with a (D). Figure 8 is an example of a 5 byte data field.

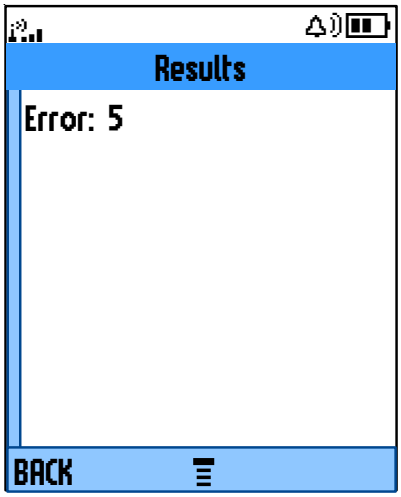
Figure 2-5. Data Field Entry Screen



Command Results

If a command completes successfully with returned data, the data is displayed in a results screen as depicted in Figure 9. If a command is successfully completed but does not produce any output data, the user will be returned to the opcode entry screen. In the case of a command error, the standard response code (Table 2) is displayed on the results screen.

Figure 2-6. Command Results Screen



There is no way to abort or power down from the waiting for results screen. The waiting for results screen is simply a “frozen” version of the final entry screen as opposed to having a dedicated screen.

Table 2-1. Handset Test Command Summary

Opcode Hexadecimal	Opcode Decimal	Opcode Mnemonic	Key Entry Format	Op Code Description
0	0	AUD_TN_LST	0 *<Action> * <Tone Identifier>OK	Generate/disable predefined tone
3	3	AUD_CTRL	3 *<Device/Process> * <Action>OK	Control various audio functions; enable/disable vibrator
4	4	AUD_LPB	4 *<Loopback Type> * <Action>OK	Enable audio loopback
5	5	AUD_LVL	5 *<Get/Set>*<Volume>OK	Set audio level
6	6	AUD_PATH	6 *<Input Path>*<Output Path>*<RX Mute>*<TX Mute>OK	Change audio path
7	7	CARRIER	7 * <Option> * <Action> OK	Enable GSM TX carrier
0A	10	CP_MODE	10 * <Set/Get> * <Sub-mode> OK	Set Call Processing Mode
12	18	INVM	18 * <level> OK	Master clear or reset
14	20	LOAD_SYN	20 * <Channel> * 0 OK	Set GSM channel
22	34	RESTART	34 * OK	Generate a software restart
2D	45	SET_RF_PWR	45 * <Power level> OK	Set GSM Power level
36	54	SUSPEND	54 OK	Terminate normal mode and enter test mode
37	55	TST_DISP	55 * <Parameter> * <Parameter Data> OK	Display predefined patterns
39	57	VERSION	57 *<version Type>OK	Retrieve SW version information
3E	62	LEDS	62 * <LED> * <Action> * <Data> OK	Control status LEDs
C0B	3083	WLOAD_SYN	3083 * <RX_FREQ_ID> * <TX_FREQ_ID> OK	Set WCDMA channels
C0E	3086	W_CARRIER	3086 * <Channel ID> * <Action> * <Tx Pwr> * <Max Pwr> * <Min Pwr> * <Data Pattern> * <Channelization> * <Scrambling> * <DPCCH Spread Factor> * <DPDCH Spread Factor> * <Channelization Code> * <Scrambling Code> OK	Enable WCDMA TX carrier

Table 2-2. Standard Response Codes

Opcode (Hexadecimal)	Opcode (Decimal)	Response Field Definition
0000b (0x00)	0	parse error (no data follows): invalid data length for command
0001b (0x01)	1	parse error (no data follows): inadequate security level for command/parameter
0010b (0x02)	2	parser error (no data follows): command/parameter not supported for current protocol (CDMA, GSM, TDMA)
0011b (0x03)	3	parse error (no data follows): command/parameter not supported for current mode (normal, test mode, handset test mode)
0100b (0x04)	4	parse error (no data follows): unsupported/invalid opcode
0101b (0x05)	5	parse error (no data follows): unsupported/invalid parameter for opcode
0110b (0x06)	6	command response: generic success (no data follows)
0111b (0x07)	7	command response: generic failure (no data follows)
1000b (0x08)	8	command response: data follows
1001b (0x09)	9	unsolicited/multiple response: data follows (sequence tag is 0)
1010b (0x0A)	10	error: couldn't allocate memory
1011b (0x0B)	11	error: internal task error
1100b (0x0C)	12	error: Test Command task timed out waiting for response from another SW component
1101b (0x0D)	13	CDMA: parse error (no data follows): command/parameter not supported for current sub-mode TDMA: command not supported in current Call Stack Test Mode
1110b (0x0E)	14	error: length specified in command header greater than length received by transport layer
1111b (0x0F)	15	error: irrecoverable error; phone state has been lost. Phone is being powered down

Table 2-3. Field and Parameter descriptions

Opcode (Decimal)	Opcode Mnemonic	Field	Description
0	AUD_TN_LST	Field 1	0 = start atone 1 = stop a tone
		Field 2	0-9 = DTMF tones
3	AUD_CTRL	Field 1	0 = Vibrator 2 = Echo canceling 3 = Noise suppressor
		Field 2	0 = Disable 1 = Enable
4	AUD_LPB	Field 1	0 = PCAP loopback 6 = CODEC loopback 7 = VOCODER (speech) loopback
		Field 2	0 = Disable Audio loopback 1 = Enable Audio loopback
		Field 3	This field is valid only for VOCODER loopback 0 = AMR 4.75 1 = AMR 5.15 2 = AMR 5.90 3 = AMR 6.70 4 = AMR 7.40 5 = AMR 7.95 6 = AMR 10.20 7 = AMR 12.20 8 = Full Rate 16 = Enhanced Full Rate 32 = Half Rate
5	AUD_LVL	Field 1	0 = Set the volume specified
		Field 2	0 = lowest, 7 = loudest

Table 2-3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
6	AUD_PATH	Field 1	0 = As is. 1 = Mute input path 2 = Internal (handset) mic 3 = Ext audio input (CE Bus) 4 = Boom (headset) mic 5 = Ext digital audio (USB) 7 = Bluetooth time slot 1 audio input 8 = Bluetooth time slot 2 audio input 9 = Bluetooth time slot 3 audio input
		Field 2	0 = As is 1 = Mute output path 2 = Internal (handset) Speaker 3 = Alert 4 = Ext audio output (CE Bus) 5 = Speakerphone 6 = Boom (headset) speaker
7	CARRIER	Field 1	0 = All zeroes 1 = All ones 2 = pseudo random sequence w/midamble 0 3 = pseudo random sequence w/midamble 1 4 = pseudo random sequence w/midamble 2 5 = pseudo random sequence w/midamble 3 6 = pseudo random sequence w/midamble 4 7 = pseudo random sequence w/midamble 5 8 = pseudo random sequence w/midamble 6 9 = pseudo random sequence w/midamble 7 10 = RACH BURST 12 = pseudo random sequence w/midamble 0 two time slot 13 = pseudo random sequence w/midamble 0 three time slot
		Field 2	0 = disable 1 = enable

Table 2-3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
10	CP_MODE	Field 1	0=set submode 1=get submode
		Field 2	5 = GSM 1900 6 = GSM dual band GSM900/GSM1800 8 = WCDMA Region 1 10 = Automatic - Dual mode: WCDMA region 1 and GSM dual band GSM900/GSM1800.a
18	INVM	Field 1	0 = Master Reset 1 = Master Clear
20	LOAD_SYN	Field 1	Channel number in decimal. Valid channel numbers are: • 1-124 (PGSM 900 MHz) • 0, 975-1023 (EGSM 900 MHz) • 512-885 (DCS 1800 MHz) • 512-810 (PCS 1900 MHz)
		Field 2	Reserved for future use and TDMA; set to 0.
34	RESTART	Field 1	As is
45	SET_RF_PWR	Field 1	PA power level (0-19)
54	SUSPEND	Field 1	As is
55	TST_DISP	Field 1	2 = Display Predefined Pattern 9 = Turn On/Off the Front Light
		Field 2 (Data)	Data for 2, 000 = All pixels off (all black) 001 = All pixels on (all white) 005 = Grey scale block: 16 level, Black to white 006 = Horizontal Zebra Line 014 = Eight Color Box Pattern Data for 9, 000 = Front Light Off 001 = Front Light On, Full Intensity

Table 2-3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
57	VERSION	Field 1	016000 = DSP Version
			017000 = User (login) pf process that created this file
			017001 = Build time (universal) in ISO-8601 format
			017002 = Clearcase view tag name
			017003 = Product base label from Clearcase config spec
			017004 = Product ID
			017005 = Version Number
			017006 = Build commentary
			018000 = Flash Booter version number (P2K Booter Only)
62	LEDS	Field 1	0 = Keypad Backlight LED 3 = Red LED 4 = Green LED
		Field 2	0 = Disable LED (Keypad backlights Only) 1 = Enable LED (Keypad backlights Only) 3 = Set duty cycle (Red/Green LEDS Only)
		Field 3	Duty Cycle setup, (leave blank if field 1 is set to 0) 000 = Off 012 = On
3083	WLOAD_SYN	Field 1	UARFCN for Receive Frequency ID. Valid values are between 0 and 16383. If TX_FREQ_ID is set to 0xFFFF, then RX_FREQ_ID must take values between 190*5 and 16383. **Note:** If a valid TX_FREQ_ID will be entered, RX_FREQ_ID must be set to FFFF.
		Field 2	UARFCN for Transmit Frequency ID. Valid values are between 0 and 16383. If it is set to 0xFFFF the TEST_TASK will derive the TX_FREQ_ID from the RX_FREQ_ID. **Note:** If a valid RX_FREQ_ID is entered, TX_FREQ_ID must be set to FFFF.

Table 2-3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
3086	W_CARRIER	Field 1	Channel identifier (0-16383).
		Field 2	0 = Enable carrier. 1 = Disable carrier.
		Field 3	Initial transmit power (dBm). -128 dBm to 127 dBm
		Field 4	Maximum transmit power (dBm). -128 dBm to 127 dBm
		Field 5	Minimum transmit power (dBm). -128 dBm to 127 dBm
		Field 6	0 = All 0s. 1 = All 1s. 2 = PN9. 3 = PN15.
		Field 7	0 = Disable spreading. 1 = Enable spreading.
		Field 8	0 = Disable scrambling. 1 = Enable long scrambling. 2 = Enable short scrambling.
		Field 9	0 = SF256, slot format 0. 1 = SF256, slot format 1. ... 5 = SF256, slot format 5.
		Field 10	0 = SF256, slot format 0. 1 = SF128, slot format 1. ... 6 = SF4, slot format 6.
		Field 11	Channelization Code Number.
		Field 12	Scrambling Code Number.

Manual Test Procedures

Introduction

The phone allows keypad and computer controlled testing of various digital test parameters.

This chapter includes the keypad/computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM850 handover
4. DCS handover
5. PCS handover

Non-Signalling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signalling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM850/DCS/PCS TX Power Output
- GSM850 RSSI
- WCDMA TX Power Output

The digital phasing parameters are stored in a EPROM on the Transceiver Board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5639B[1] or equivalent)
- Full-Rate Power Supply (PSM5049A[1])
- Battery Eliminator (5-00-3F-10000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

RF Interface

- SMA/N-type Adapter (0-00-00-40042[2])
- SMA Cable 0.5m (0-00-00-40047[2])
- Repair Fixture (5-00-4T-10000[2])
- USIM (0-00-00-40810[2])

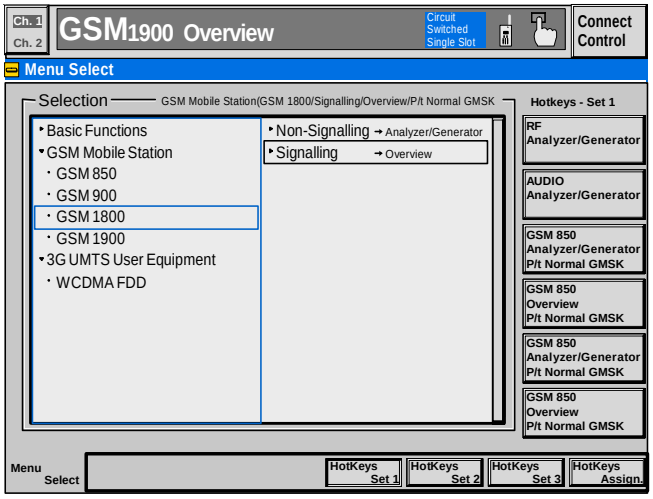
[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

Call Origination

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

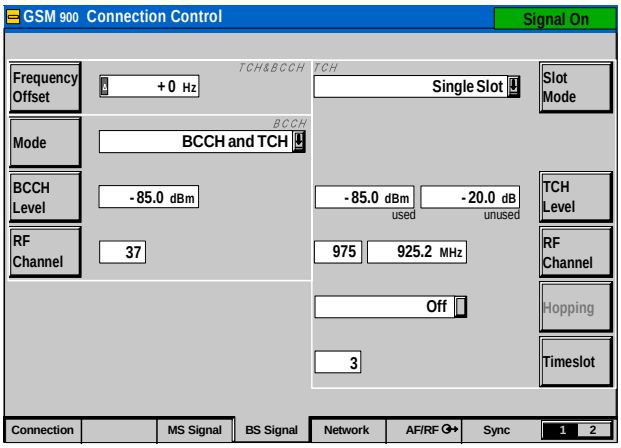
1. Install the test USIM in phone.
2. Connect hardware as illustrated in figure 3-1.

Figure 3-1. GSM Signaling Setup



3. Setup up the test box for GSM, DCS, or PCS Signalling
4. Set Broadcast Channel (BCH) to 194 (GSM850), 700 (DCS), or 661 (PCS)
5. Set Broadcast channel level to -85dBm
6. Set Traffic Channel (TCH) to 128 (GSM850) or 512 (DCS/PCS)
7. Set Traffic channel level to -85dBm

Figure 3-2. GSM Connection Control

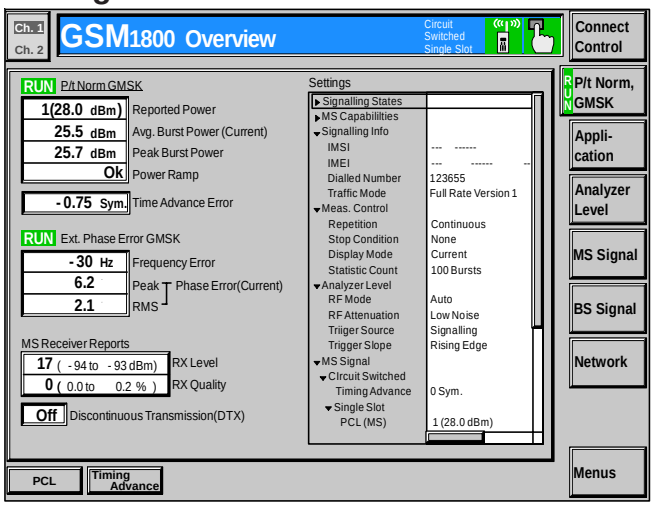


8. Wait until the phone indicates a receive signal

9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 3-3. GSM Call Connected



Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 3-1. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	31	33	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 3-2. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	28	32	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

[1]Power Level = 0
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 3-3. PCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	28	32	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 0
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Figure 3-4. A835 Manual Test Hardware Configuration

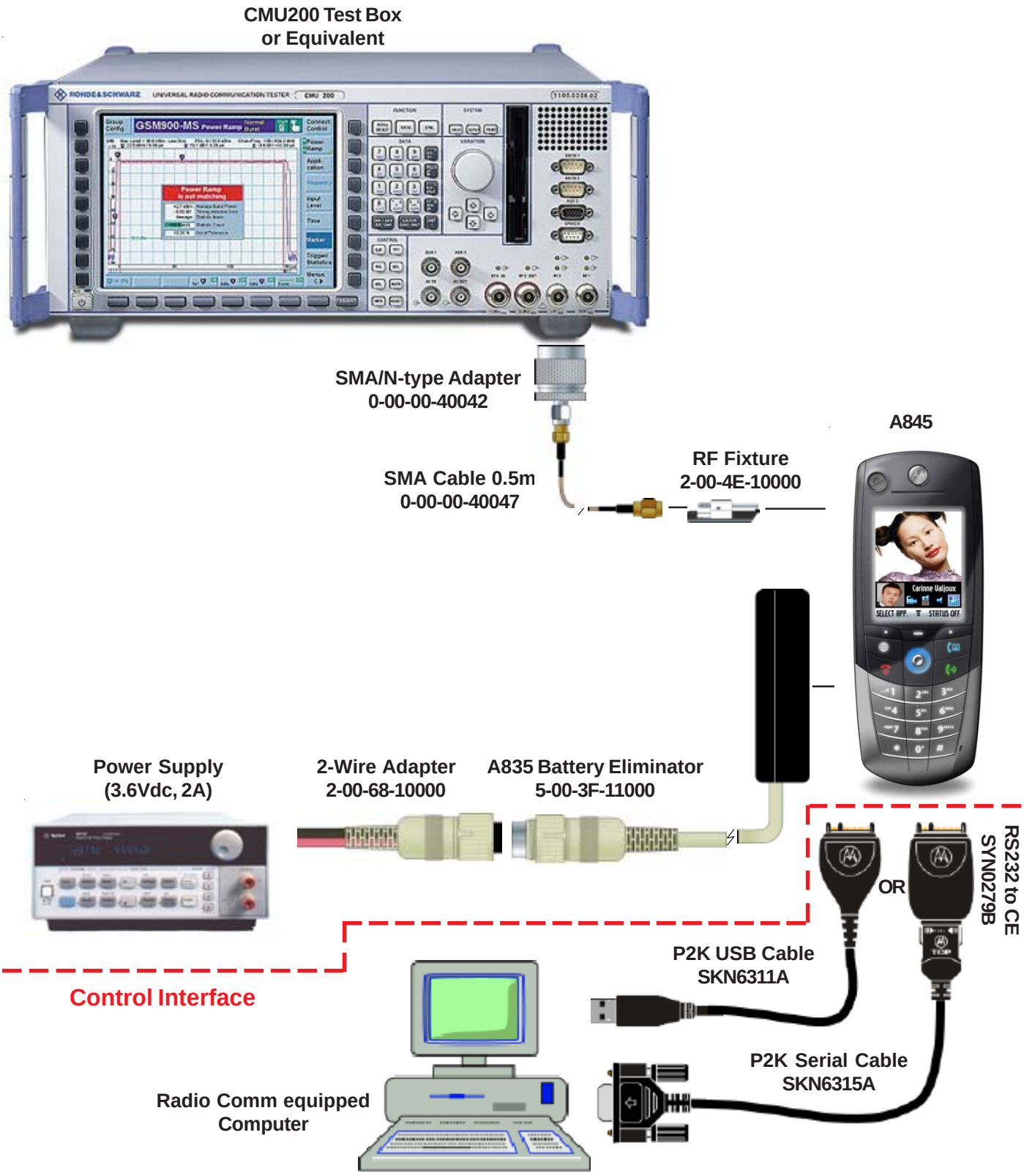
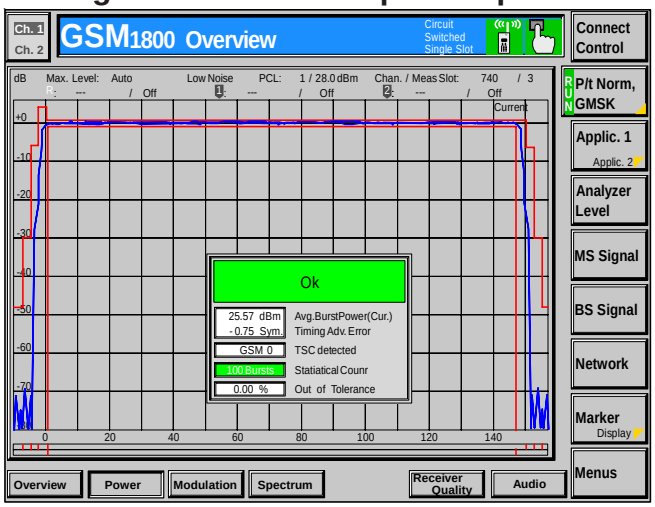


Figure 3-5. Burst Output Shape



Burst Output Shape should fall within the standard limits of the Power Ramp.

BER measurements is only required if RX Quality reads a value of 4 or greater.

Table 3-4. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

It is recommended that handover procedures be performed as shown in the following table.

WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 13.

Software Requirements

None.

Call Origination (WCDMA)

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signalling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

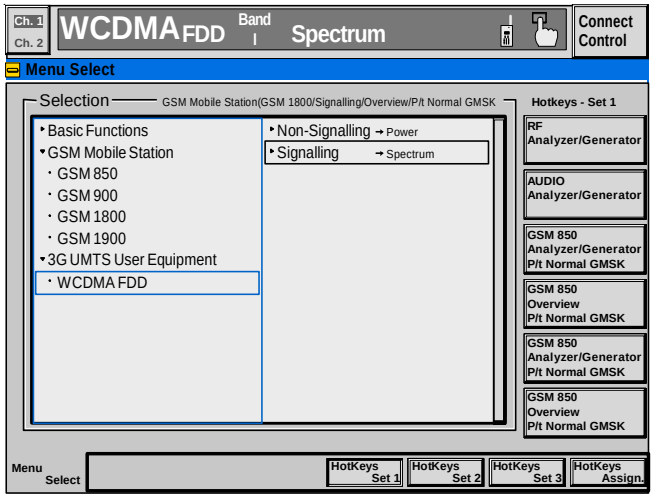
1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

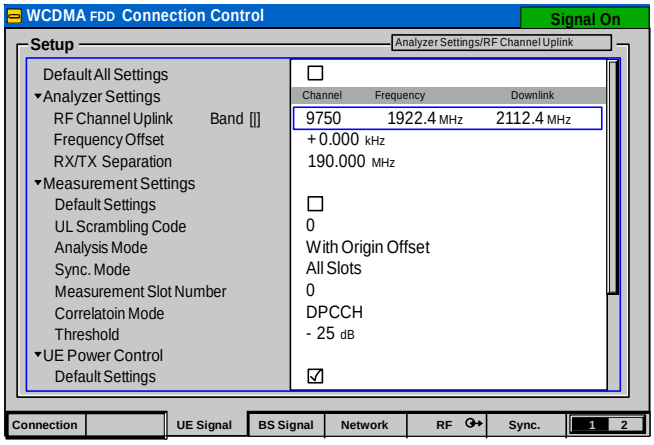
3. Setup up the test box for WCDMA FDD Signalling

Figure 3-6. WCDMA Signalling Setup



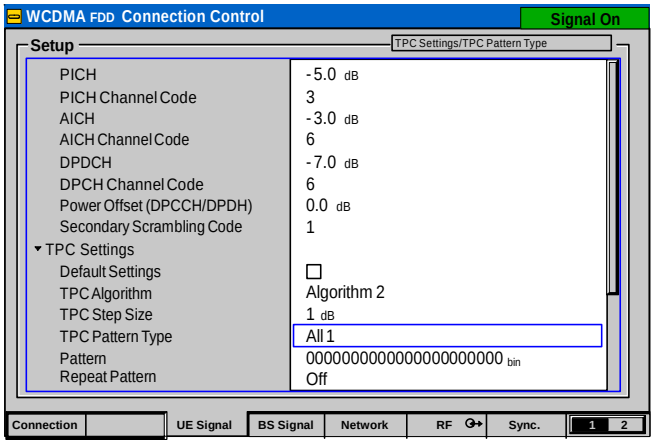
4. Set UE Signal, RF Channel Uplink to 9750

Figure 3-7. Channel Uplink(UE Signal)



5. Set TPC Pattern Type to All 1

Figure 3-8. TPC Pattern Type(UE Signal)

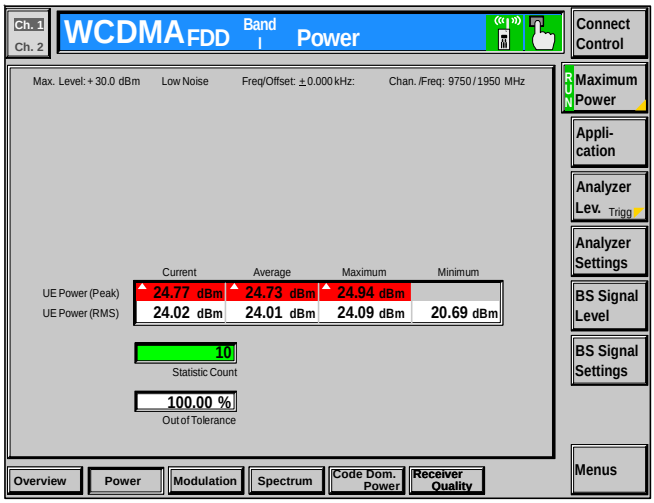


6. Wait until the phone indicates a signal

9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 3-9. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 3-5. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 3-10. WCDMA Modulation

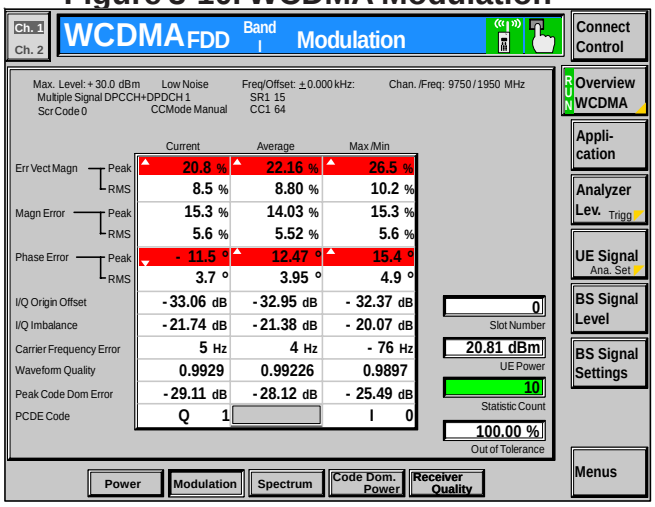
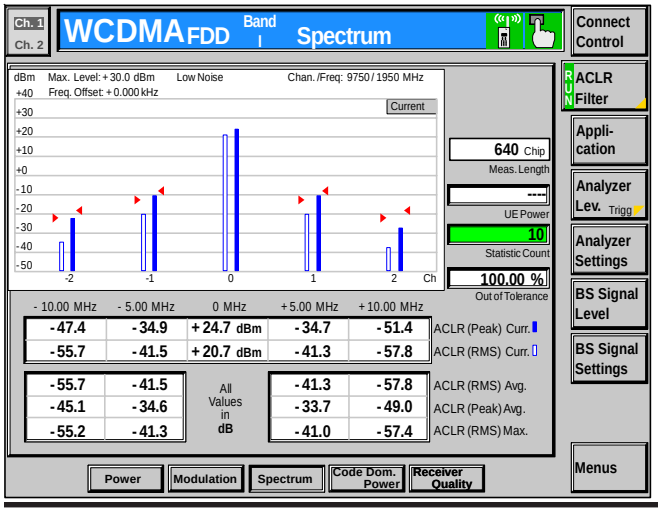


Figure 3-11. ACLR Screen



Non-Signalling Test Procedures (GSM/DCS/PCS)

To perform non-signalling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands can be sent using the Handset test command interface or through a computer. Please refer to section, "Handset Test commands," for details on how to send test commands through phone keypad entry.

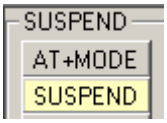
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)



Click SUSPEND (USB Only)

Hardware Requirements

Control Interface Options (Only)

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

Note: If handset test commands are being used, a control interface is not needed.

Refer to page 3-2 for a list of Hardware. Refer to Figure 13 for a configuration illustration.

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

Verify TX Power Output (GSM/DCS/PCS)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 3-6. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28	29.5	dBm
PCS TX Power Out	28	29.5	dBm

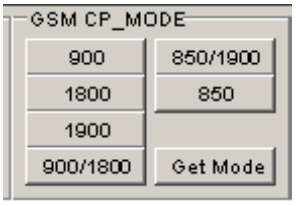
[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

Handset Test Commands

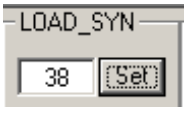
54	Suspend
10*0*10[1]	WCDMA/GSM/DCS mode
20*38*0[2]	Set Channel 38
45*5[3]	Set GSM Power Level 5
7*6*1	Enable Carrier

Radio Comm Test Commands

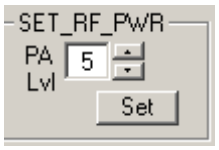
Click on 850/1900 (GSM/ PCS) or 1800 (DCS)



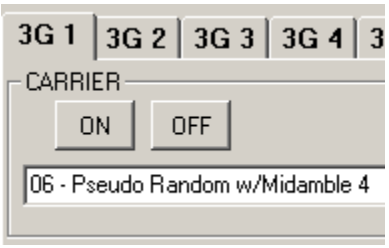
Enter 128 (GSM), 700 (DCS), or 661 (PCS) and then click Set



Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

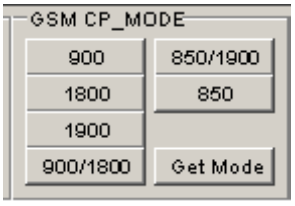
Broadcast Channel (BCH): 20
Broadcast Channel (BCH) Level: -105 dBm

Handset Test Commands

No supported test commands

Radio Comm Test Commands

Click on 850/1900 (GSM/ DCS) or 1800 (DCS)



Enter Channel 194
Click INIT

Click Execute
Verify return data is approximately -105 dBm

Non-signalling Test Procedures (WCDMA)

To perform non-signalling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands can be sent using the Handset test command interface or through a computer. Please refer to section,"Handset Test commands," for details on how to send test commands through phone keypad entry. Also, refer to, "Computer Test Commands," for details on how to send test commands through the computer.

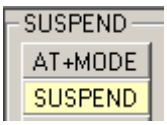
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

Refer to page 3-2 for a list of Hardware. Refer to Figure 3-4 for a configuration illustration.

Software Requirements

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 3-7. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	20.5	21.5	dBm

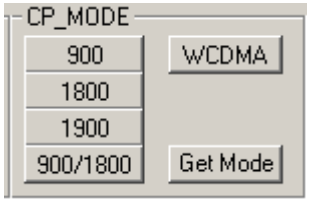
Handset Test Commands

54		Suspend
3086		W_CARRIER
Field 1	9750	Set Channel
Field 2	0	Enable Carrier
Field 3	023	Max Power Out
Field 4	027	Max TX Power
Field 5	206	Min TX power
Field 6	002	PN9 Data pattern
Field 7	1	Enable spreading
Field 8	01	Long scrambling
Field 9	000	SF256, Slot format 0
Field 10	000	SF256, Slot format 0
Field 11	000	Channelization Code
Field 12	000000000	Scrambling Code

Note: Enter 1 in field 2 to disable carrier

Radio Comm Test Commands

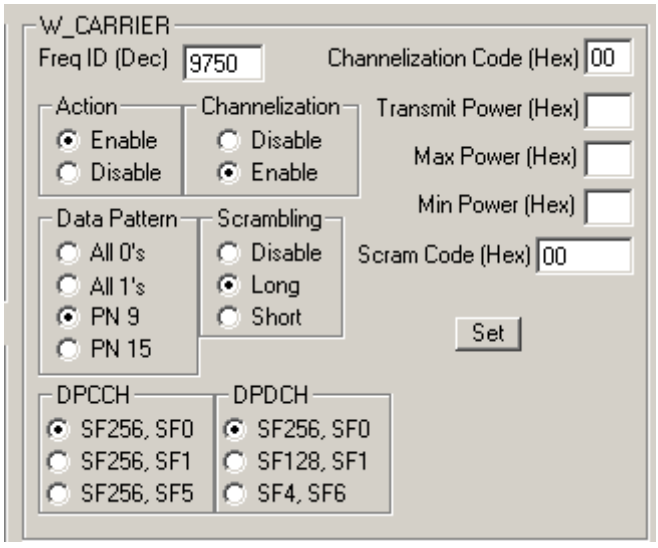
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)



Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

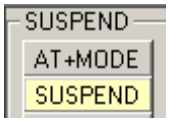
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Vibrator Test

Handset Test Commands

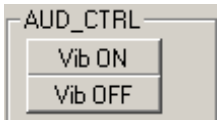
3*0*1 Enable Vibrator
3*0*0 Disable Vibrator

Radio Comm Test Commands

Enable or Disable Vibrator

Verification

Verfiy vibration function when enabled.



Handset Mic/Speaker test

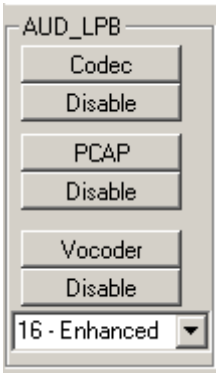
Handset Test Commands

6*2*2	Enable internal mic and handset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

Radio Comm Test Commands

Enable internal mic and headset speaker

Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

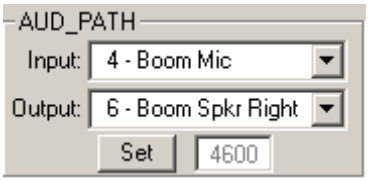
Mono Headset Mic/Speaker test

Handset Test Commands

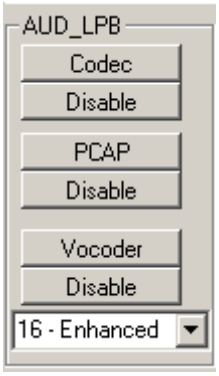
6*4*6	Enable headset mic and headset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

RadioComm Test Commands

Enable headset mic and headset speaker



Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

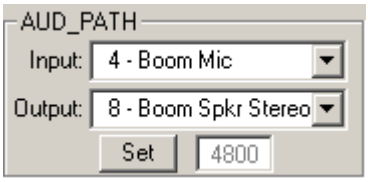
Stereo Headset Mic/Speaker test

Handset Test Commands

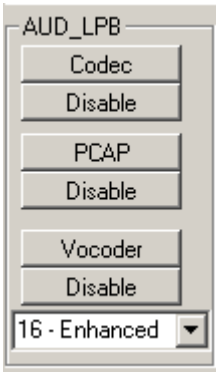
6*4*8	Enable headset mic and headset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

RadioComm Test Commands

Enable headset mic and headset speaker



Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

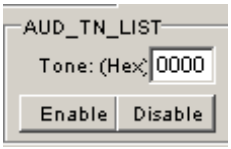
NOTE: DO NOT issue a Suspend command (54 ok) for this test.

Handset Test Commands

0*1*265	Play SONATA_IN_C
0*0*265	Stop SONATA_IN_C

RadioComm Test Commands

Enter 109 and click Enable



Verification

Listen for undistorted audio.

Software Version Check

Use the following procedures to retrieve software information. Software information can also be retrieved from the phone's customer User Interface. Refer to the phone's user manual for details.

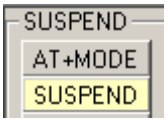
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE (Serial Only)
Click PST Initialize (USB Only)

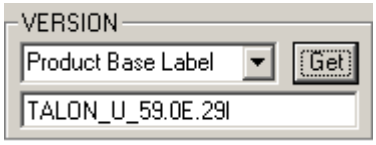


Test Commands

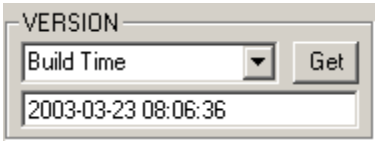
57*017003 Read Software Version
57*017001 Read Build Date

RadioComm Test Commands

Select Product Base Label and click "Get" to retrieve software version



Select Build Time and click "Get" to retrieve Build Date



Display Test Procedures

This section will describe the proper test procedures to determine the functionality of the color display. Any tests that involve displaying a predefined pattern can be returned to the Opcode screen by pressing the right softkey of the phone.

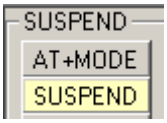
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Display Backlight Test

Handset Test Commands

55*9*000 Backlight Off
55*9*001 Backlight On, full intensity

RadioComm Test Commands

Click "FL Off" to disable backlight
Click "FL On-Full" to enable backlight

Verification

Verify that the backlights respond for each issued command.

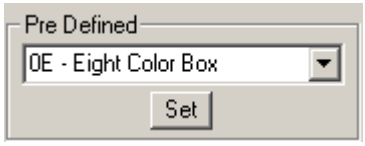
Display Color Test

Handset Test Commands

55*2*014 Eight Color Box Pattern

RadioComm Test Commands

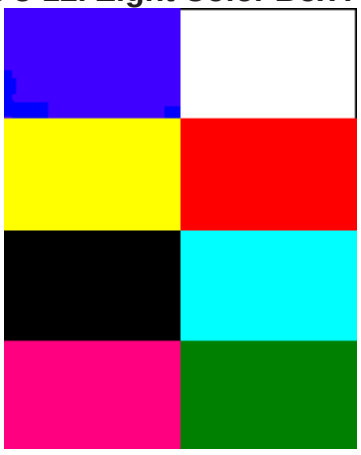
Select Eight Color Box and click “Set”



Verification

Verify that the color pattern on the phone’s display matches the color box in figure 23. Also verify edges (uniform/smooth).

Figure 3-12. Eight Color Box Pattern



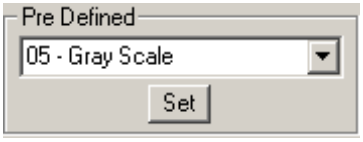
Display Linearity Test

Handset Test Commands

55*2*005 Grey Scale Block

RadioComm Test Commands

Select Grey Scale and click “Set”



Verification

Verify that the Grey scale block on the phone’s display matches the Grey scale block in figure 14. This test can also be used to confirm that the color intensity is linear.

Figure 3-13. Grey Scale Block

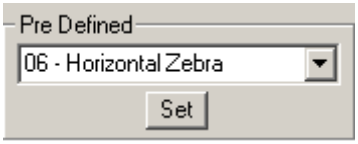
Display Flicker Test

Handset Test Command

55*2*006 Horizontal Zebra Line

RadioComm Test Commands

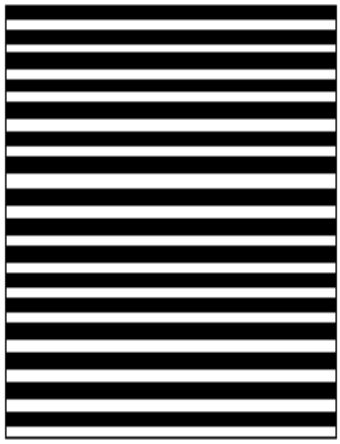
Select Horizontal Zebra and click “Set”



Verification

Verify that no noticable flicker exists.

Figure 3-14. Zebra Pattern



Display Pixel Defect (Bright)

Handset Test Commands

55*2*001 All pixels on (all white)

RadioComm Test Commands

Select All Pixels Off and click “Set”

Verification

Verify that no greater than two pixels are off.

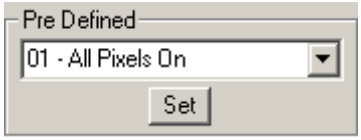
Display Pixel Defect (Dark)

Handset Test Commands

55*2*000 All pixels off (all black)

RadioComm Test Commands

Select All Pixels On and click “Set”



Verification

Verify that no greater than two pixels are on.

LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

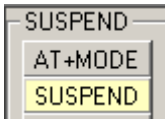
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Keypad Backlight

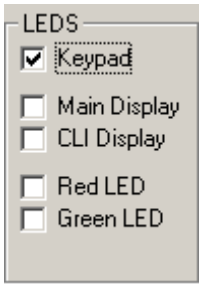
Handset Test Commands

62*0*1[1] Enable Keypad Backlight
62*0*0[1] Disable Keypad Backlight

[1]Leave field 3 blank and press OK

RadioComm Test Commands

Select Keypad to enable. Deselect Keypad to disable.



Verification

Verify that all keypad backlight LEDs activate.

Bluetooth Tests

Use the following procedures to verify functionality of the Bluetooth device integrated in the phone.

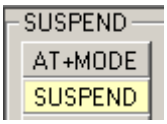
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



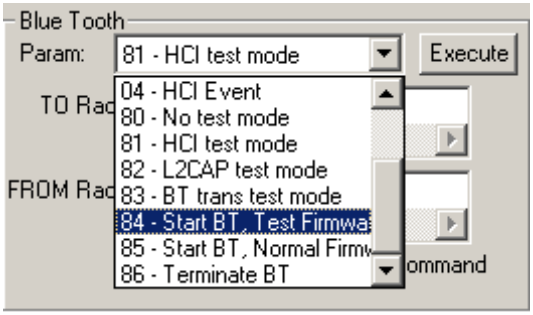
Unmodulated CW TX test

Handset Test Commands

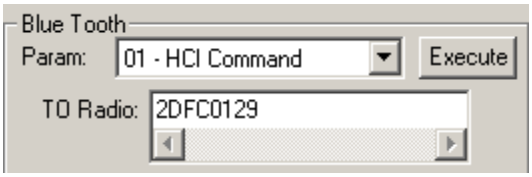
Not Supported

RadioComm Test Commands

Under Bluetooth, select parameter 84 and click execute, then select 81 and click execute.



Under Bluetooth, select parameter 01 and enter 2DFC0129 in the "TO Radio" field. Click Execute.



NOTE: The Bluetooth TX signal will activate momentarily once the HCI command is issued. You must have the RF probe positioned for measurement once you click execute.

Verification

Verify that a 2441MHz signal is present. If the phone is closed, use a RF probe to sniff the strongest signal around the "7" key of the keypad. If the phone is open (shields off), verify that -2dBm to +4dBm is read from TP5600. An high impedance RF probe is required to read this range. Use of lower quality RF probes will result in signal level differences.

Camera Testing

This section is intended to describe the procedures that will determine whether the camera function of a Motorola terminal is under normal operating conditions.

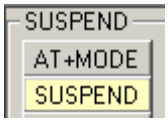
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

Not supported

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click USB Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

The following hardware will be required to properly test the camera function of the phone.

1. Desktop Charger (SPN5032A or equivalent)
2. USB or RS232 control interface (refer to figure 4)
3. Fast Rate Charger (SPN5078A or equivalent)
4. Hardcopy of Macbeth Color Chart
5. Hardcopy of Focus Chart
6. Hardcopy of Grey Chart

Camera Test Configuration

Use any color printer to print a hardcopy of the Macbeth color chart. The Focus chart and Grey chart can be printed using any B/W printer.

For best results follow this recommended setup,

1. Attach chart to a flat vertical surface (wall)
2. Attach the phone to the desktop charger
3. Attach the control interface to desktop charger
4. If necessary, attach power supply to control interface.
5. Turn on phone.
6. Select Camera option in phone
7. Position Desktop charger so that the camera test chart completely fills the viewfinder.

Assign a permanent space in the test lab for these test procedures. Always use the same lighting conditions. Also, it's recommended that a "golden picture" is saved and used for comparison.

There is a variety of ways the camera test charts can be attached to a vertical flat surface. They can be taped, tacked, attached to flip charts, etc. Use your best judgement.

The desktop charger is being used as a fixture to position the phone for test, therefore, it's recommended that the desktop charger is attached to a countertop to prevent any movement.

Figure 3-15. Camera Test Configuration

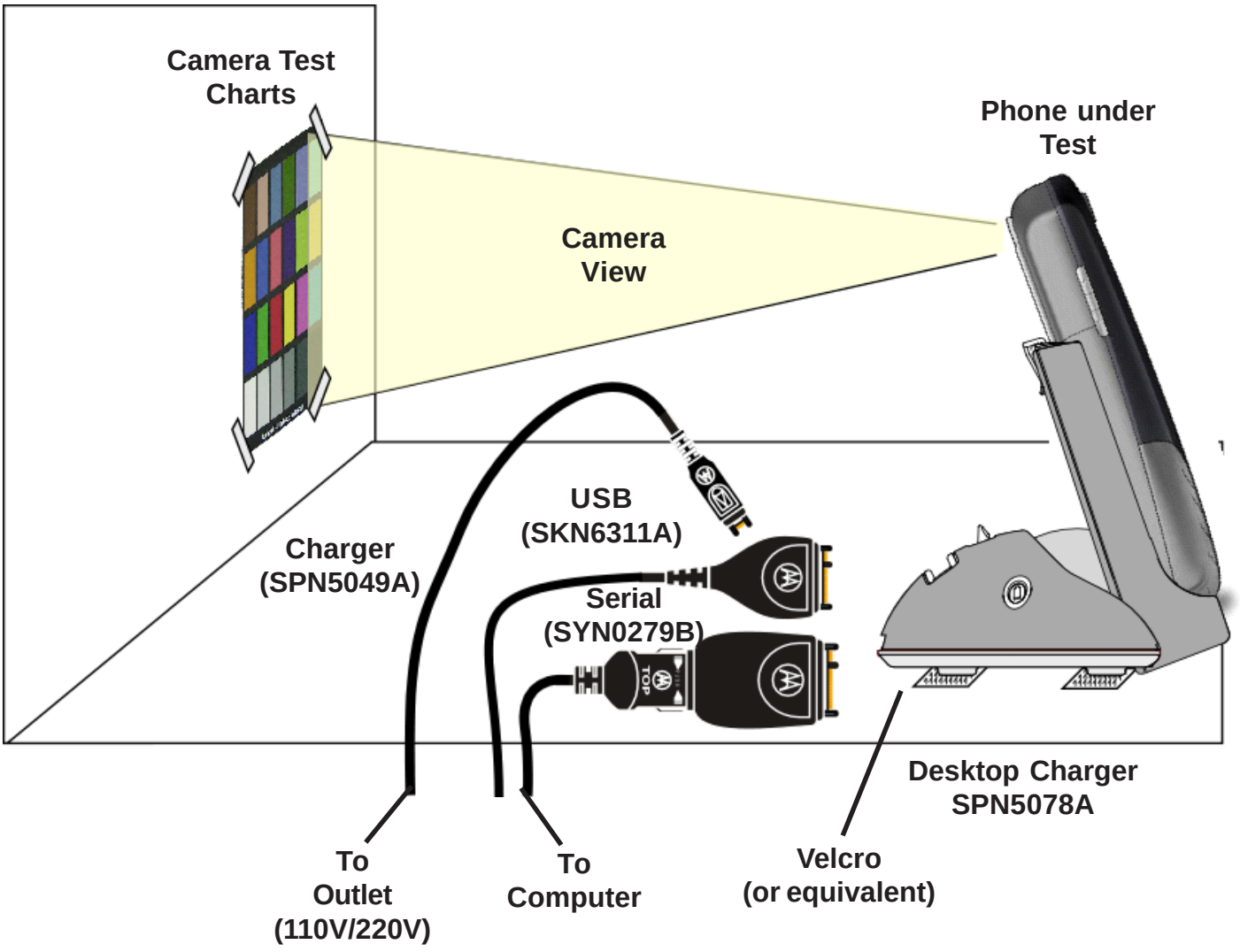


Image Capture

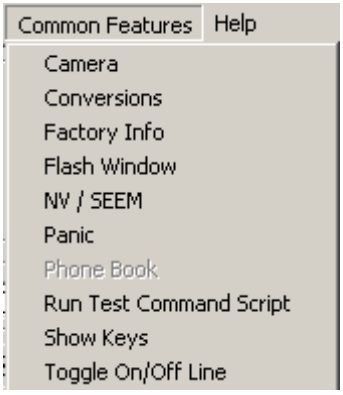
The listed steps should be followed to capture three images (1) the Macbeth color chart, (2) the focus chart, and (3) the grey scale chart. The user will be required to print all images found in Appendix A.

Handset Test Commands

Not supported

Radio Comm Test Commands

Under “Common Features” select Camera



Click “Take Picture”

Once the picture is captured, it’ll be displayed on the screen. Click “Save To File”

Macbeth Color Chart

1. From the computer, open the captured color chart image.

2. Compare, the color blocks of the printed Macbeth color chart to the captured image.

Follow the listed verifications to determine the quality of the image.

1. Minimal noise level for Blue, Green and Red on blocks 19 through 24.

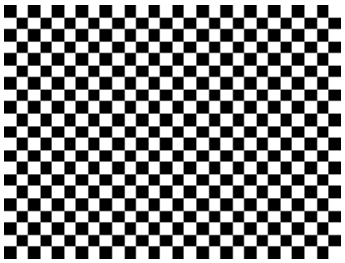
2. Uniformity for grey scale blocks 19 through 24.

3. Good white balance on blocks 19 through 24.

4. Good color reproduction on blocks 13 through 18.

Focus Chart

1. From the computer, open the captured focus chart image.



Verify the focus quality at the center, top-left corner, bottom-left corner, top-right corner, and bottom-right corner.

Grey Scale Chart (Shading Test)

1. From the computer, open the captured grey scale chart image.

Verify that there is minimal shading deviations on all four corners when compared to the center of the image.

GPS Testing

This section is intended to describe the procedures that will determine whether the AGPS function of a Motorola terminal is under normal operating conditions.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

RadioComm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click USB Initialize and click SUSPEND when initialization is complete
(USB Only)

GPS Software Check

Handset Test Commands

Not recommended

RadioComm Test Commands

Under VERSION select GPS Chipset version

Verification

Verify that GPS software version is displayed.

GPS RF Connector Check

Handset Test Commands

Not supported

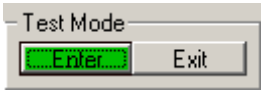
RadioComm Test Commands

Open the GPS form located under the Common Features Menu.

Under SUSPEND_COMP, select 01-GPS Chipset and UnSuspend.

Click Execute

Under Test Mode, click Enter



Verification

Measure the DC voltage on the center of the GPS RF connector. Verify that the GPS DC voltage reads within 2.69Vdc to 2.86Vdc.

Theory of Operation

A845 Overview

The A845 is a 3G device. It will deliver on the "promise" of 3G by providing high speed network access and rich multimedia content all in a superior voice-centric unit. A video camera and Assisted GPS provide additional value by offering unique business and entertainment solutions.

The mechanical architecture features a 176 x 220 pixel, 0.198mm pitch TFT activecolor display, a built-in speaker phone, and a removable Li-Polymer battery. The architecture enables full postponement of the front housing and battery door cover by allowing the transceiver brick assembly, keypad, display, microphone, and earpiece speaker to be fully assembled and retained within the rear housing chassis.

Front covers may then be snapped in at distribution based on specific orders. Front housing branding is accomplished through thermal transfer decals.

As a 3G product, the A845 complies with all key specifications as defined by the 3GPP. Key product features are:

- UMTS: WCDMA 1900, GSM 850/1800 and 1900 MHz Tri-band technology
- GPRS High speed packet data (64kbps UL, 384 kbps DL)
- 176 x 220 TFT Active Color, 64k colors
- 64MB Integrated Flash Memory
- Integrated Bluetooth
- MP3 Player
- Enhanced Multimedia Capability (Audio/Video, Games, MMS)
- Unique 5-way Navigation Key
- New graphical user interface
- Enhanced internet browser (XHTML)
- Full Personal Information Manager (PIM) with

Figure 4-1. A845 Transceiver

SyncML Synchronization (OTA, Desktop)
- Integrated Video/Still Camera and GPS
- Voice Recognition Driven Dialing and Menu Shortcuts
- Voice Note Voice Recorder
- Polyphonic Speakerphone
- Programmable (J2ME)
- iTAP™ Predictive Text Entry
- Integrated Stereo Headset Jack

Video Camera Features:
- JPEG Image Capture @ VGA Resolution
- MPEG4 Video Capture @ QCIF Resolution
- Two imagers (take pictures and video of others or yourself)
- Streaming Video
- Tightly Coupled, Ergonomic Design
- Initial User Applications:
- Sending captured Video Clips and Pictures through MMS, Email, or
- Internet channels
- Simultaneous Voice/Data – Take a picture or video clip and send while you're on the phone
- Future Capabilities:
- Video Conferencing (2-Way Video Telephony)

Location (AGPS) Applications:
- Get to specific location, with appropriate choices of destinations and routes and guidance to destination
- Identify local places of interest for hotels, taxi companies, restaurants, theatres, sight-seeing, and shopping
- Receive information through alerts or display on map ahead of traffic congestion.
- • Receive roadside assistance, with rescue service network and location information from the cellular network used to complement any information the pedestrian/driver is able to separately give.
- E911 Services: When roaming on a 2-2.5G GSM E-OTD-enabled network the mobile phone will respond to a request for location when making an emergency call (Please refer to future AGPS MRS for further details).
- Push, Tracking & B2B Applications such as corporate tracking, routing, fleet management, and Buddy tracking (alert)

Baseband Electrical (Digital)

Digital Logic

The baseband architecture will consist of a POG / PCAP based architecture. The POG IC integrates a 32-bit RISC Communications Engine (M-Core), a 32-bit SC140 Quartz DSP core, and an Interprocessor Communications Module (IPCM) along with associated peripherals to provide the main phone processing. The PCAP will handle all of the power supply requirements, analog audio circuitry, and control for numerous other functions.

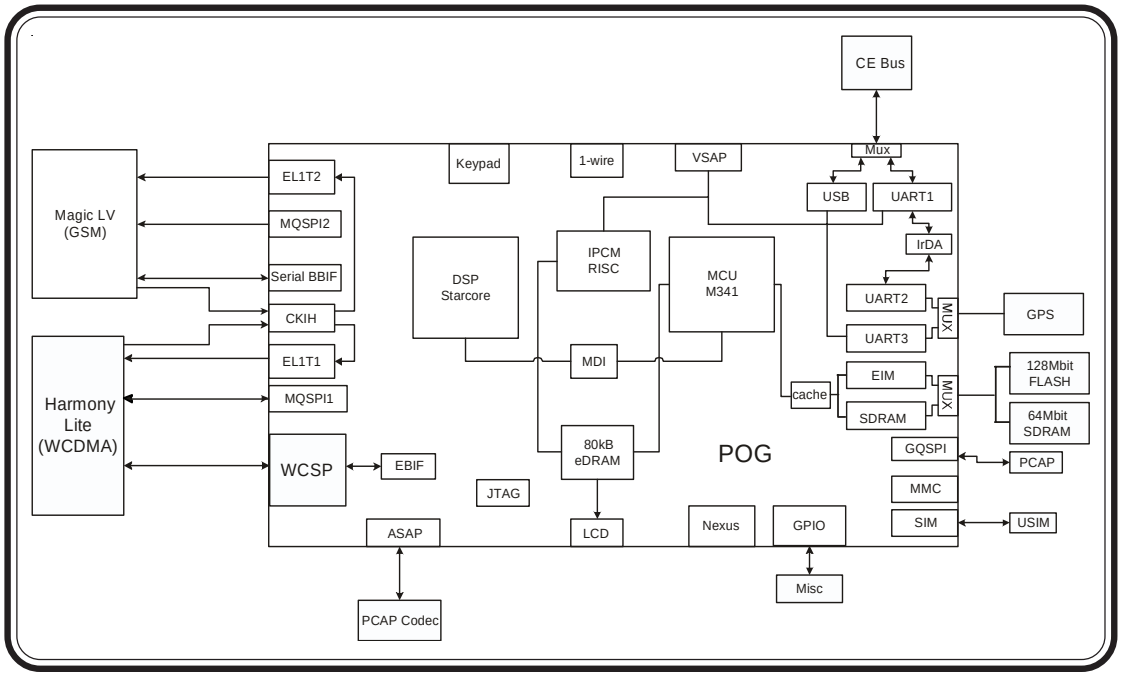
POG is the baseband processor IC of the 3G chipset solution. POG is crafted to provide a high performance embedded solution at low power for 3G mobile devices. POG is a TriCore processor IC integrating a powerful DSP core, a 32bit MCU RISC core with unified cache and a custom 32bit RISC engine for data movement across the processing domains.

The DSP core is a high performance StarCore with four parallel ALUs, the SC140, with a novel Variable Length Execution Set (VLES) architecture which maximizes the execution of multiple instructions in a single clock cycle. The SC140 enables the emergence computational intensive communication applications. The SC140 is assisted by 3G specific hardware accelerators and timers to optimize performance and power. As part of the 3G support, the Wideband CDMA Signal Processor (WCSP) module implements modem functions required by the CDMA subscriber unit in accordance with the 3GPP specifications.

The 32bit MCU RISC core is the M*Core M341 designed for high performance and low power embedded systems. The M341 embodies an 16K unified cache, integer multiplier and MMU in support of virtual memory management OSes.

Data communication across the cores is handled by a flexible 32bit RISC machine, the Inter Processor Communication Module (IPCM). The IPCM supports flexible data flow between the MCU, DSP and the multi-

Figure 4-2. POG Block Diagram



media peripherals.

A video buffer is embedded as SRAM memory to optimize display rendering while lowering power. POG offers an advanced SDRAM controller to maximize external memories throughput.

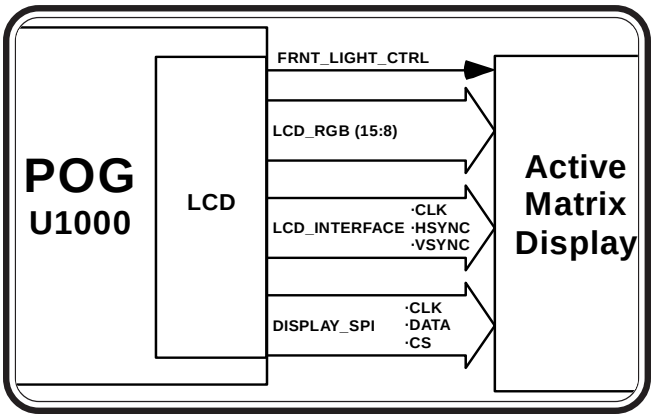
Display Interface

The display uses two programming interfaces, RBG (Red Green Blue) and SPI (Serial Peripheral Interface). The RGB interface is the primary communication bus for the display. It controls how the pixels are displayed. Here is the line descriptions of the RGB interface

- SCLK latches data into the LCD.
- HSYNC causes the panel to start a new line.
- VSYNC causes the panel to start a new frame.
- DISPLAY_ON enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
- LCD (15:8) is used for color mapping pixel data in the LCD controller.

The SPI interface is used for state configurations of the display module. Some states include sleepmode, active, and video modes.

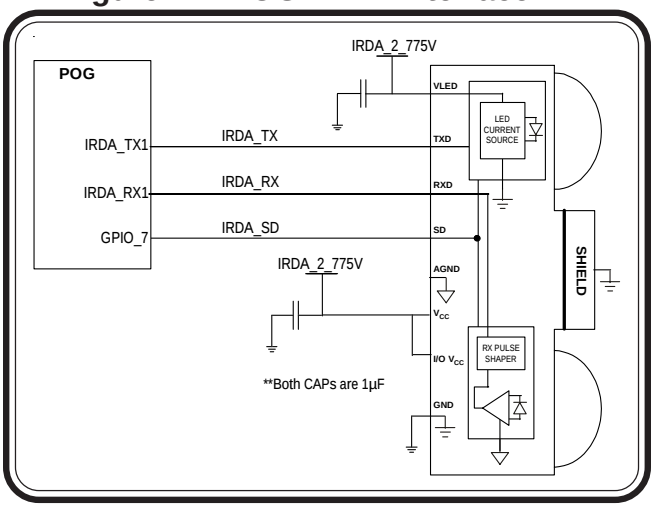
Figure 4-3. POG - LCD Interface



IrDA Interface

The IrDA interface is used to allow infrared data communications between the cellular transceiver and an IrDA device. The IrDA interface will conform to a 30 degree cone angle. The POG IC has integrated the data communications bus for the IrDA device. The IrDA device has a standard baudrate of 9600bps.

Figure 4-4. POG - IrDA Interface

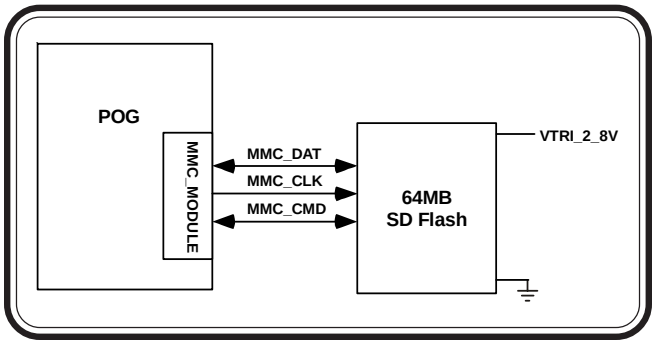


SD Flash Interface

The A845 will interface with an embedded 64 MB NAND flash device. The embedded flash device is a high-density flash memory IC that gives the user the ability to store personal files and use them in low-bandwidth applications.

The MMC/SD interface will operate at 2.8V. The MMC mode will be used; the MMC module in POG does not support SPI mode. The MMC module in POG supports only single bit data transfers at a maximum of 20MHz. Since the MCU will be operating at 90MHz (not 100MHz), the maximum MMC frequency will be 18MHz.

Figure 4-5. MMC/SD - Block Diagram



Keypad Interface

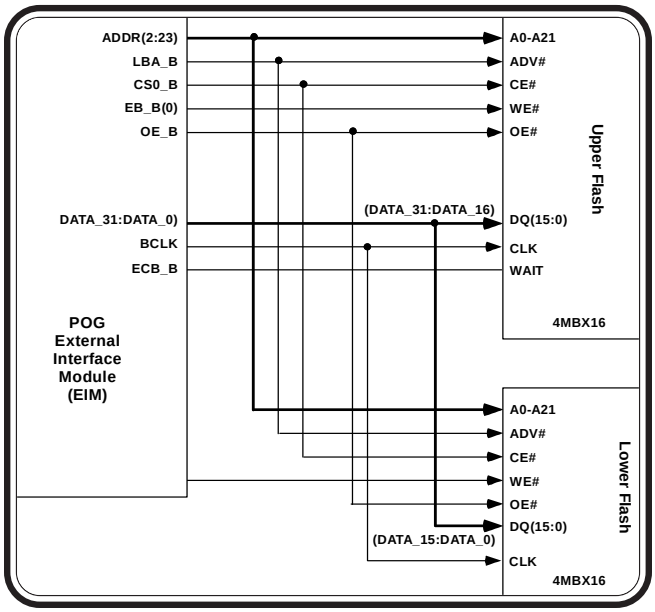
The keypad processor on the POG can support up to an 8 x 8 row-by-column keypad matrix. However, this keypad matrix will use a line configuration and not a row-by-column configuration. In the line configuration, when a key is pressed, two different signals will be shorted through the key's switch to ground. Keypad backlighting is controlled by the PCAP. The available backlight settings will be "On" and "Off."

Flash Memory

The software requirement is for 128Mb of flash memory. Memory is divided into 16 partitions of 8Mb each. There is one parameter partition and 15 main partitions.

Two 16-bit W18 ICs will be required to meet the 128Mb requirement. The Intel flash is packaged in a 56 active ball BGA packages with .75 mm ball pitch and 7.7 x 9.0 mm footprint.

Figure 4-6. Flash Memory Block



Power Supply Architecture

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are illustrated below.

Figure 4-7. PCAP Power supplies - 1

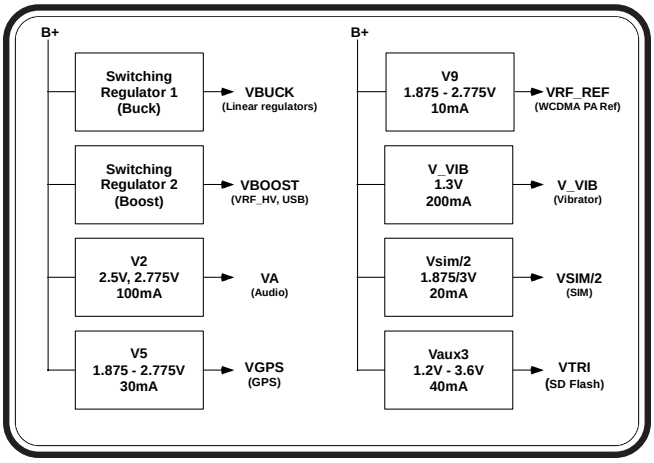


Figure 4-8. PCAP Power supplies - 2

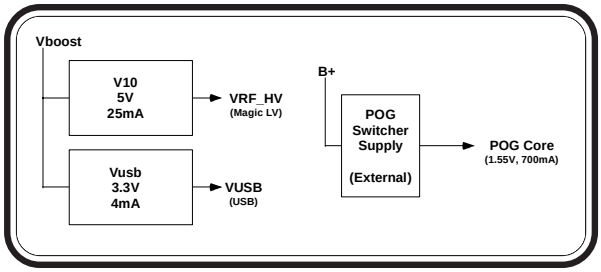
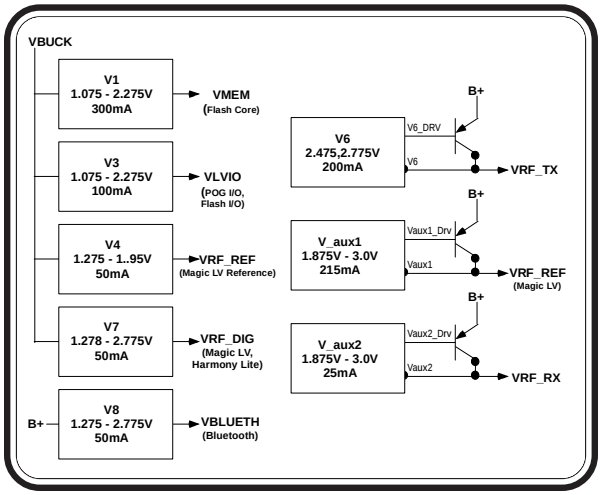


Figure 4-9. PCAP Power supplies - 3

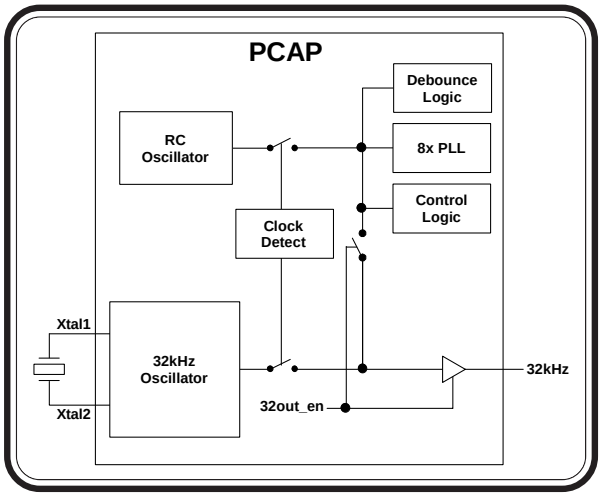


Clock Generation

PCAP can generate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Rainbow requires for optimal performance, therefore, an external 32.768kHz crystal is used.

The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Figure 4-10. PCAP 32kHz Clock

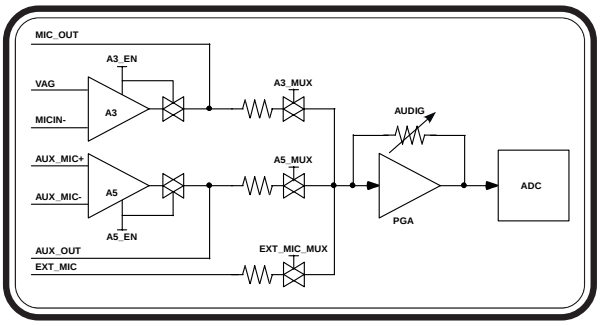


PCAP Audio

TX Audio

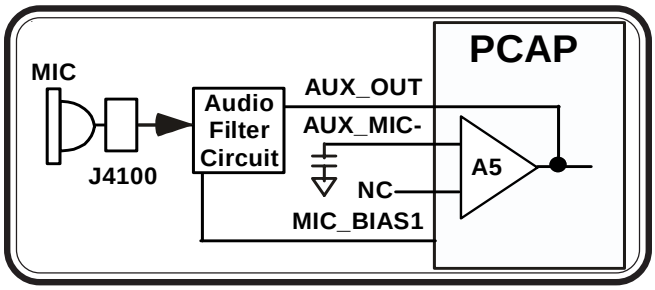
The A845 supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single-ended with respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

Figure 4-11. TX Audio Block



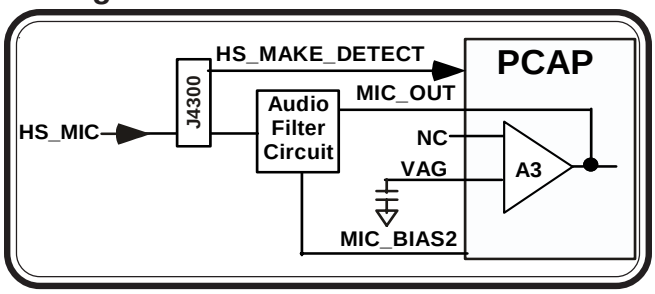
The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 and R4101 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R4102 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

Figure 4-12. Internal Mic Path



The headset microphone path is biased through R4396, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by using R4399 as a pullup resistor and detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

Figure 4-13. Internal Mic Path



The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight/ALeft Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R34003 and R34002 respectively, and then connected to the transducer. Off the Speaker-path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

Figure 4-15. Handset Speaker Path

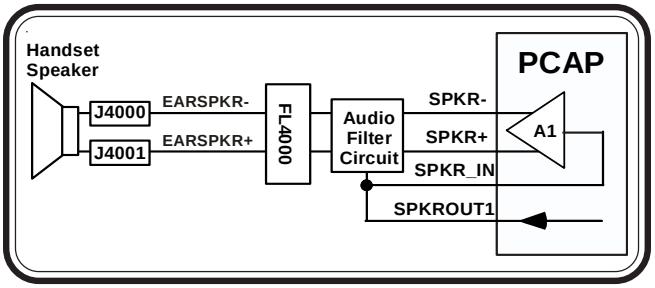
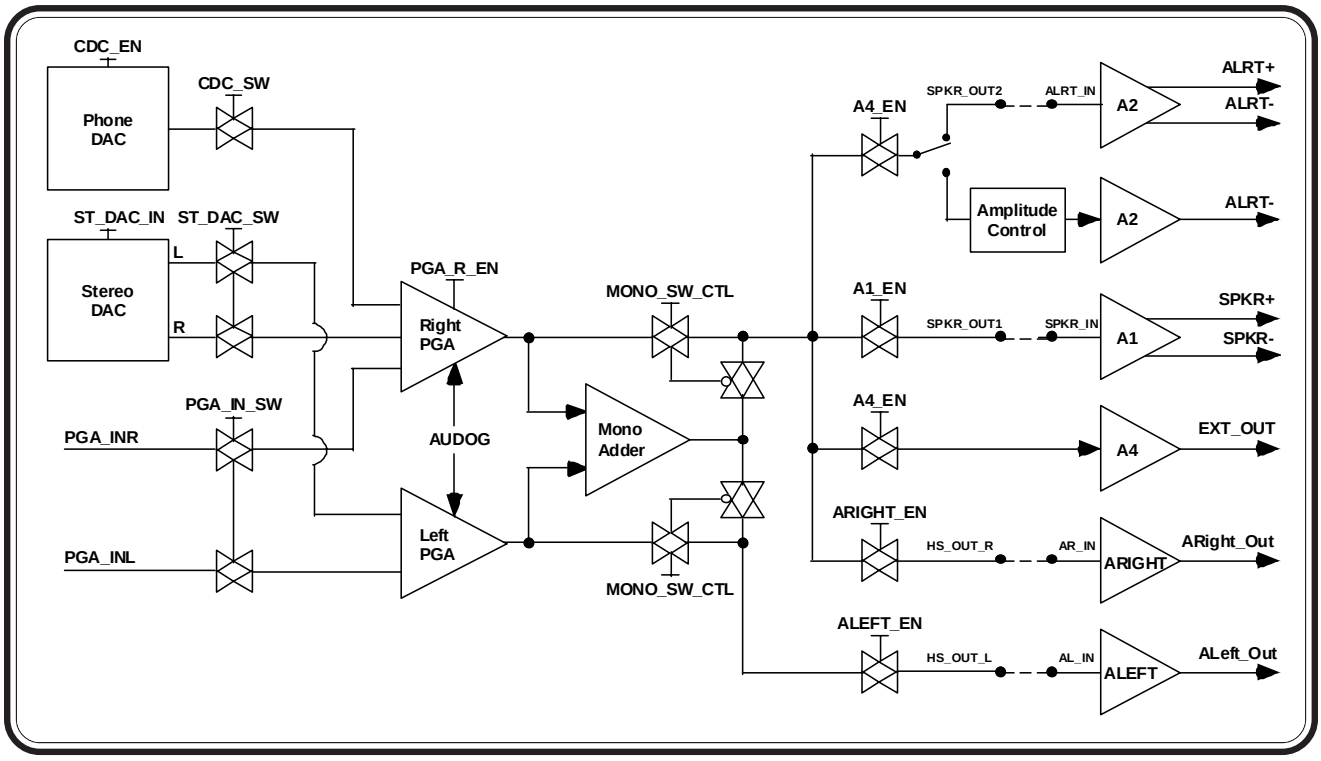
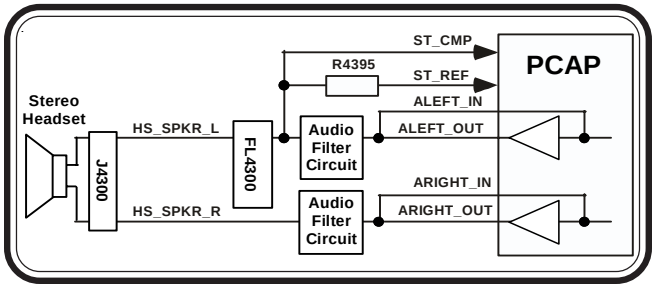


Figure 4-14. RX Audio Block



The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

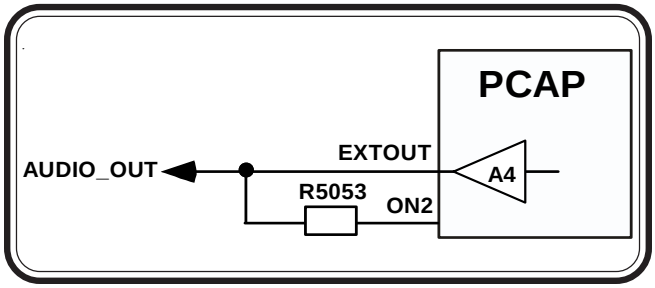
Figure 4-16. Headset Speaker Path



The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R34304 and C4306, R34303 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ARight_Out path, AL_IN is tapped off through C4354 for the inverting input of the audio amp ALEFT.

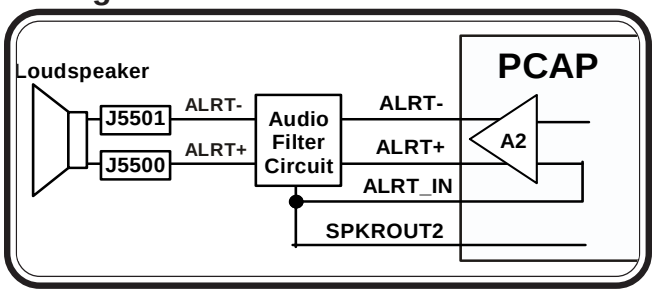
The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

Figure 4-17. External Speaker Path



The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

Figure 4-18. Alert Path



Battery Interface

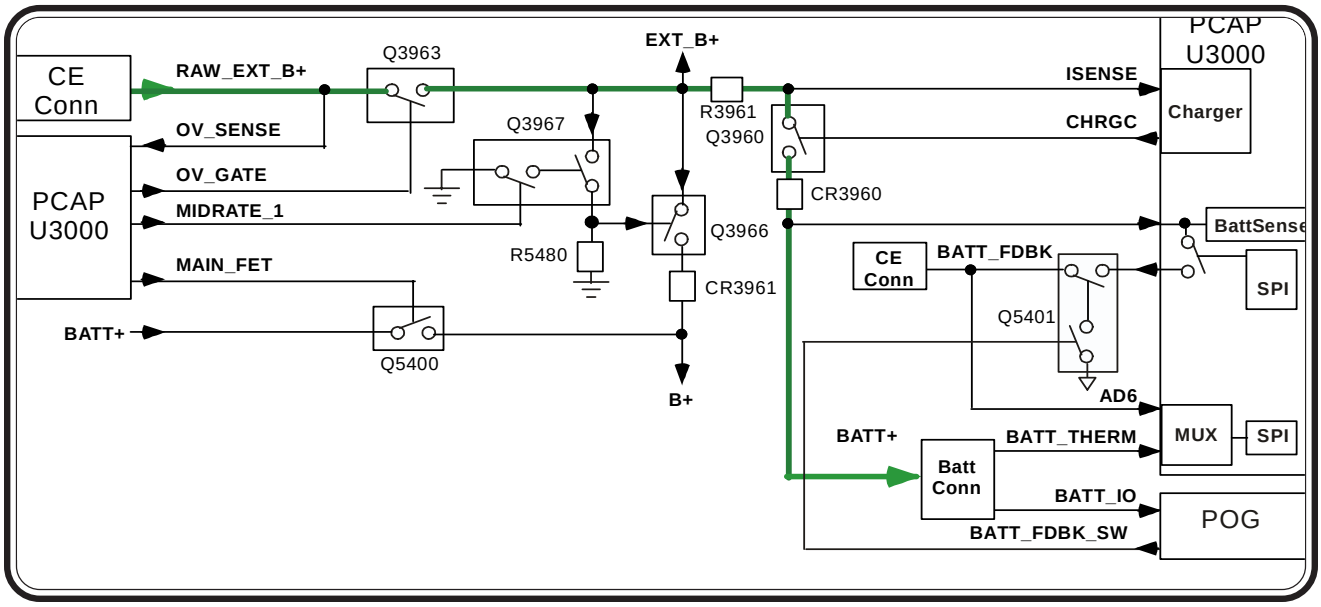
Batteries interface to the main transceiver board via a 4-pin connector (J5400). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q5400 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U3000) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J5000). During full rate charging, Q3966 is turned ON so that current can be supplied from the external source to B+. Q5400 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q3960. A sense resistor (R3961) provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J5000). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 4-19. Battery Interface Block

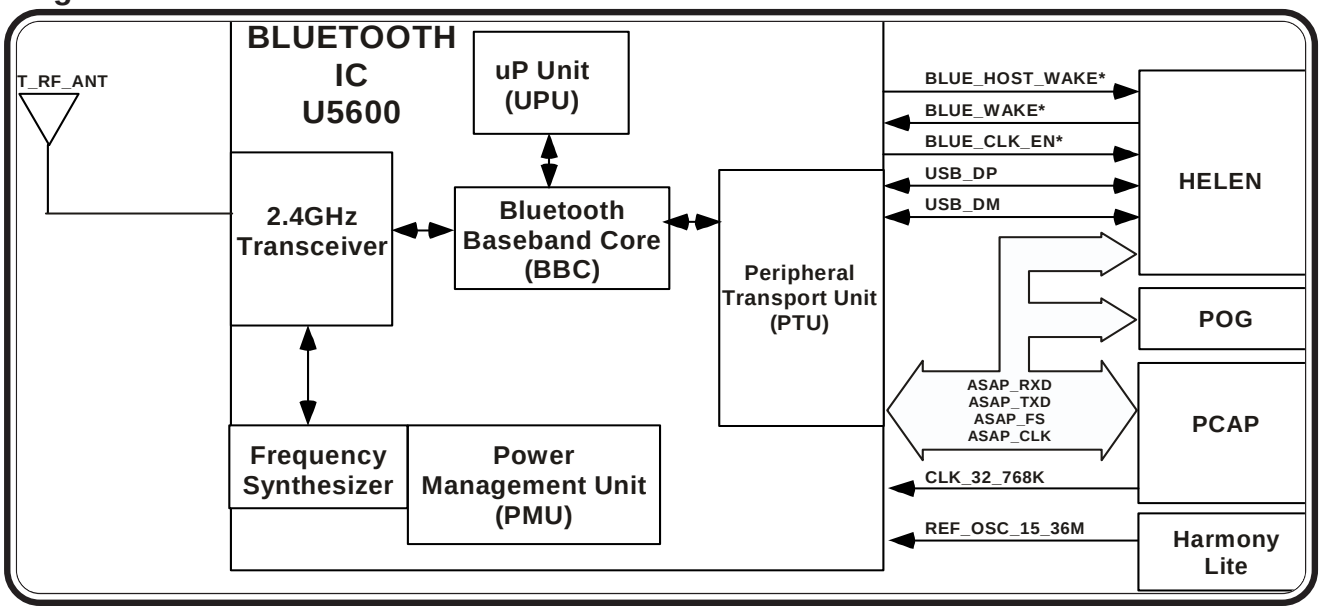


Bluetooth

The Broadcomm 2033 Single Chip Bluettoth solution is being used with this mobile phone. The BMC2033 is a Bluetooth 1.1 compliant stand alone baseband processor with an integrated 2.4GHz transceiver. The baseband section controls all bluetooth functionality from the physical layers to the HCI layer. The radio section includes PLL, VCO, LNA, PA, upconverter, downconverter, modulator, demodulator, and channel select filtering.

The fractional- N synthesizer can support multiple reference frequencies, including 13MHz and 15.36MHz.The UART interface between Rainbow and BCM2033. The SSI interface between Rainbow, PCAP and BCM2033.

Figure 4-20. Bluetooth Block



AGPS

The GPS section is based on the Motorola MG4100 single chip GPS receiver 2M SRAM IC (Phoenix) along with One-Track firmware.

The main blocks of the MG4100 IC consist of the GPS Acquisition Module (GAM), a low IF front-end, an ARM7TDMI microprocessor module, a Boot ROM synthesized in gates, and several processor peripherals.

When Phoenix is configured to OneTrack mode, it will search, acquire, and track satellite signals; decode data without host intervention; calculate position, velocity, and time at a 1Hz rate and perform background data decode. It supports both Oneshot and autonmous (stand alone GPS receiver). In reacquisition mode if more than four satellites with signal strength of more than -140dBm are visible, Phoenix will decode satellite data and autonomously compute a position fix without any assistance. The Tim-To-First-Fix will be greatly reduced comparing to Oneshot.

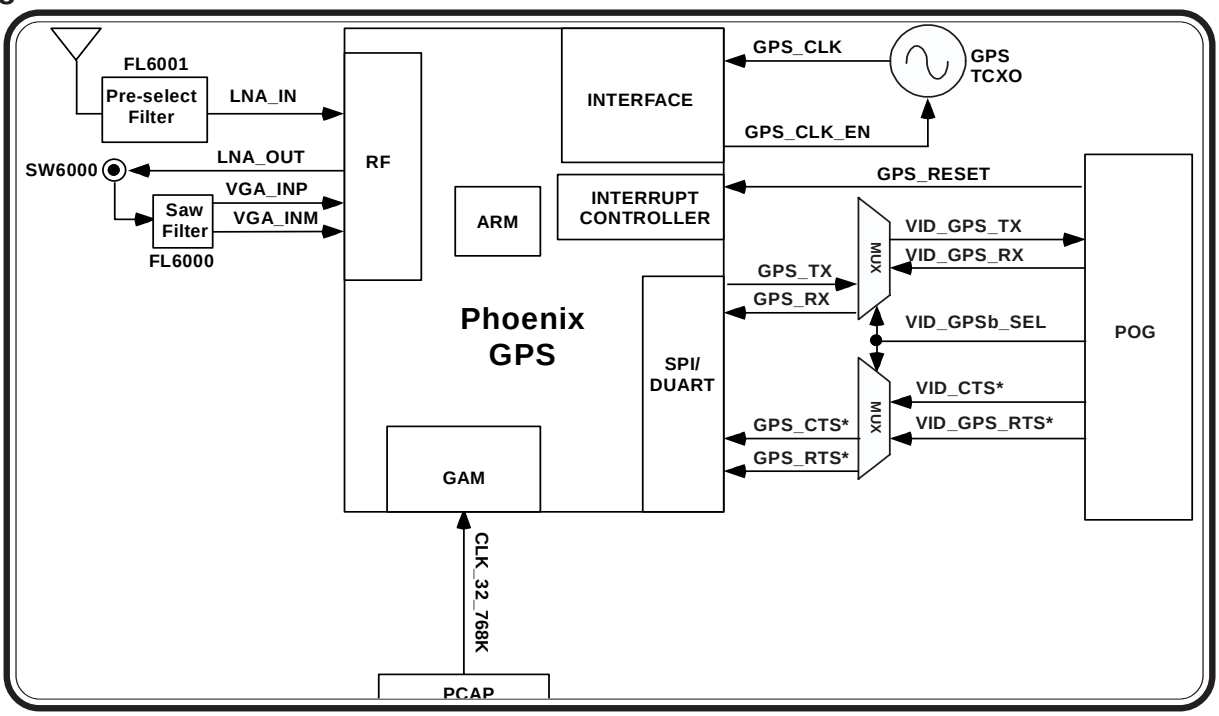
The GPS external RF connector (SW6000) allows users to attach a pro install car kit or external GPS attenae. It provides power supply through the signal pin at 2.775V and 15mA current max.

The control signals for the Phoenix IC will be transported via the POG (U1000) 4-wire UART interface (TXD,RXD,CTS,RTS.)

The 26 MHz TCXO is used as a dedicated accurate input clock to acquire GPS fix at weak signal environment and faster TTFF. This clock is powered off when GAM does not require the clock. A RTC clock is used for low power operation.

GPS_CLK_EN signal is used to turn off external reference clock when Phoenix IC switches to CPU and low power mode. Conversely, the clock will be turned on when the software switches to full power mode.

Figure 4-21. Phoenix GPS Block



Camera

The Imager Module includes two image sensor ICs with the lenses which comprise the optical element and the mechanical mount for the lenses, a flexible interconnection cable, and any required passive components for the image sensors, serial EEPROM and connector.

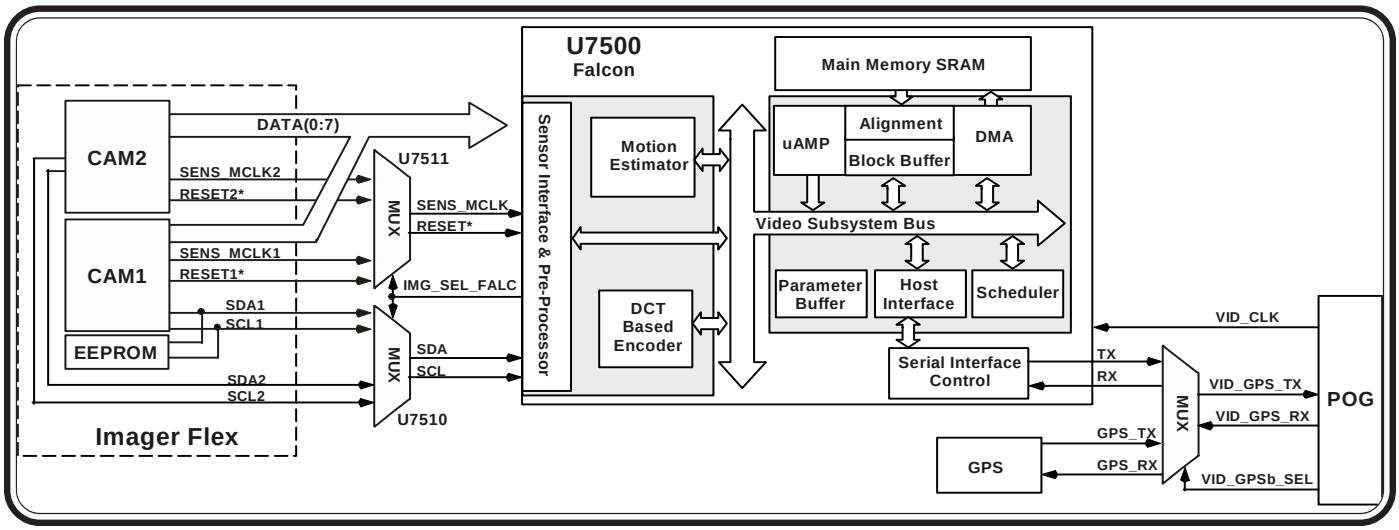
The image sensor is of the color CMOS type, with an imager format of VGA: 640 x 480 pixels. The image sensor produces color image data in the Bayer RGB (Red, Green, Blue) format. The lens system will be a two-element, fixed focal length design. The finished module will have bad pixel data for the both imagers stored in the EEPROM. Imager selection is processed through a multiplexer and IMG_SEL_FALC line.

The Falcon IC (U7500) is a video encoder chip designed to directly interface to a CMOS image sensor and output encoded video to a host processor (POG). The Falcon has on-board memory for QCIF (176x144) sized video. A frame rate of 30 per second is sustainable providing the host removes the compressed images at that same rate. The Falcon is also capable of capturing VGA still images in JPEG format.

The video encoder sensor interface allows the encoder to receive the Bayer formatted data from the image sensor. The Bayer formatted data is then processed through a color interpolation in which Red (R), Green (G), and Blue (B) components will be contained in each pixel. The bitmapped RGB image will contain 8 bits/color and 24 bits/pixel. The RGB image is then sent through a color space conversion where the luminance and chrominance data is compressed and sent to the POG through a RS232 interface.

The POG IO for the camera is multiplexed with the GPS circuit. POG selects whether it's going to interface with GPS or camera via VID_GPSb_SEL

Figure 4-22. Camera Block



RF TOP

Front End Module

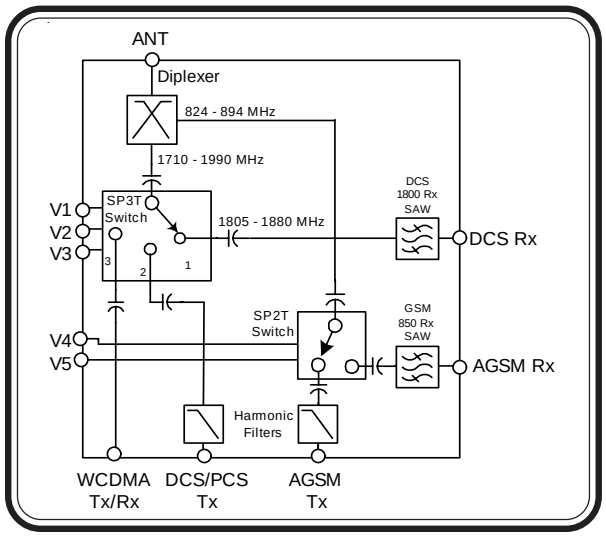
The received signal from the antenna is fed to the FEM (Front End Module) through antenna matching components.

This Front End Module integrates a 3-position GaAs antenna switch, a 2-position GaAs Tx/Rx switch, diplexers, transmit harmonic filters, SAW filters and matching components on a multilayer low-temperature cofired ceramic (LTCC) module. The module provides band selection and filtering between the GSM850 (AGSM), GSM1800 (DCS), GSM1900 (PCS) and WCDMA1900 (PCS) receive and transmit bands in Motorola 3G phones designed for the US market.

A diplexer at the Antenna port is used to separate the GSM850 Tx/Rx paths (low band) from the GSM1800, GSM1900 and WCDMA 1900 paths (high band). Each of these paths is then routed to a GaAs switch.

Two GaAs switches are used. A SP3T switch on the high band side of the Antenna diplexer performs band switching between WCDMA Tx/Rx and GSM1900 Rx (port 3), DCS/PCS Tx (port 2), and DCS Rx (port 1)

Figure 4-23. FEM Block



On the low side of the Antenna diplexer, a SP2T GaAs switch performs the T/R switching function for GSM850

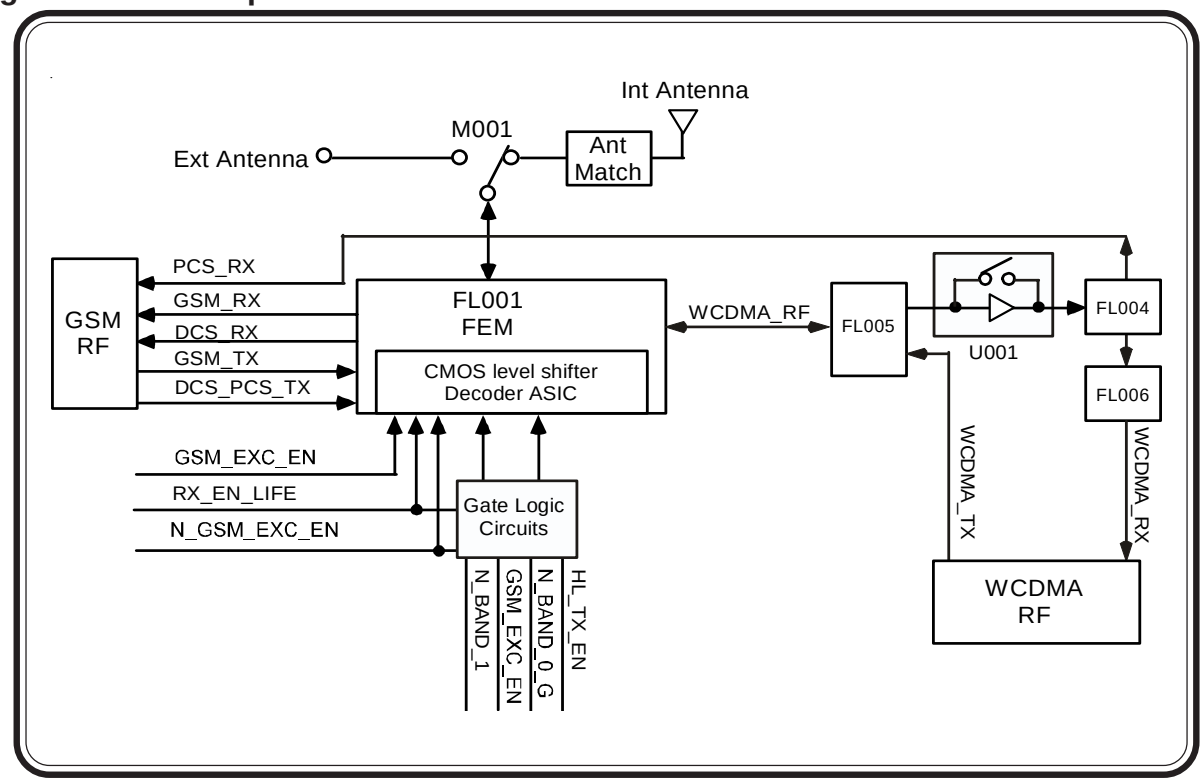
Band selection is done by control lines N_BAND_1 and N_BAND_0_G. Mode selection is done by control lines HL_TX_EN, RX_EN_LIFE, and GSM_EXC_EN.

After the FEM, the GSM850 or DCS receive signal is fed into one of the two transformers for differential conversion. For PCS, the receive signal leaving the FEM is fed into a high rejection band pass filter (FL005), which allows PCS RX and WCDMA TX/RX signals to pass. The PCS RX and WCDMA RX signal is then fed into an adjustable gain LNA (U001).

U001 operates in two gain modes selectable by MBC_EN2. The nominal gain expected while in high gain mode is ~16dB. During high input signal levels of ~–40dBm or stronger, the LNA will be in low gain mode. Currently, signal levels below ~–55dBm would trigger the high gain mode.

FL004 is a digital filter which is used to pass PCS receive signals to a transformer, for differential conversion, located in the GSM circuit. WCDMA receive signal is passed to the WCDMA circuit.

Figure 4-24. RF Top



RF GSM Receiver

The GSM architecture is a direct launch/direct conversion architecture built around the Magic LV and LIFE IC's. The LIFE IC is a direct conversion receiver which converts GSM850/DCS/PCS RF signals to analog I & Q. Receive analog I & Q is converted to digital signals and fed to the DSP within Rainbow by the Magic LV.

LIFE IC

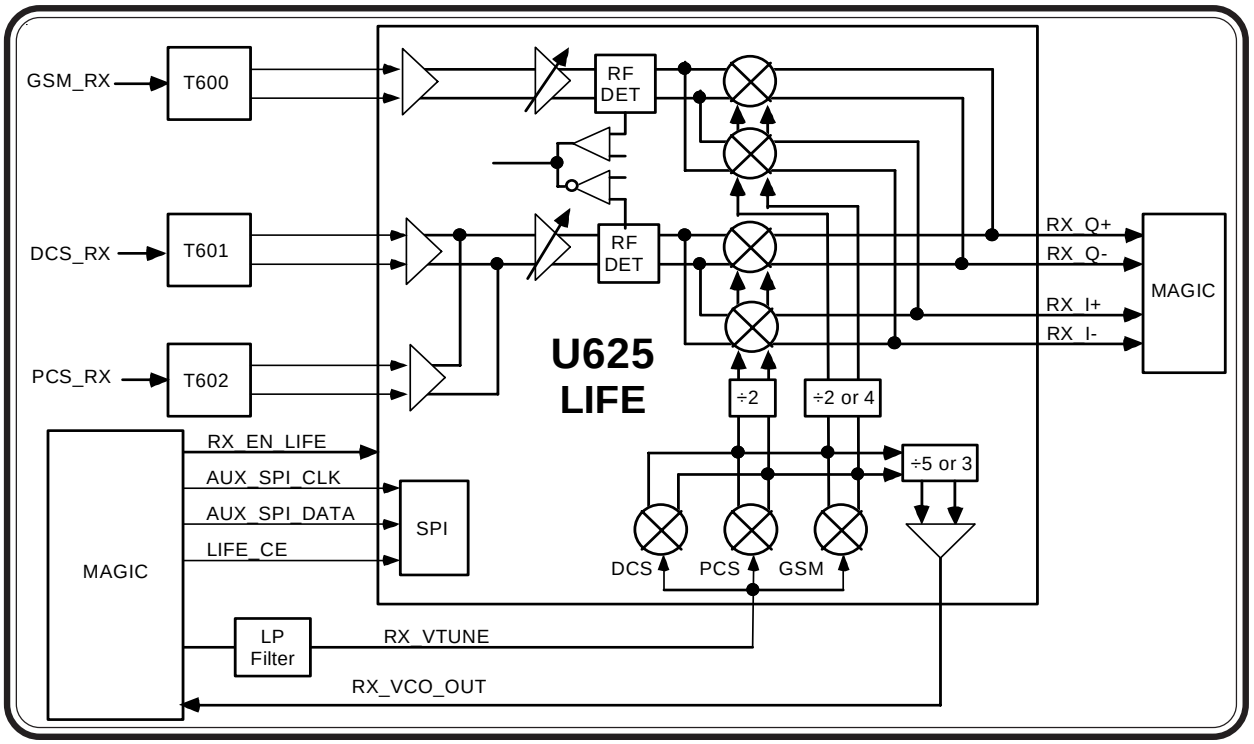
The LIFE is a Low IF Front End complete receiver for GSM/DCS/PCS. The following lists the key components within the LIFE IC.

- Four LNAs with balanced inputs
- Two quadrature mixer paths
- Three integrated RX VCOs at 4 GHz
- Buffered VCO output
- SPI bus for AGC, transformer match, VCO control, and band switching
- All signals within the IC are differential

The differential receive signal is fed into a LNA, AGC amplifier, RF detector, and mixer. The mixer output will be the differential IQ signals which are sent to the Magic IC.

The integrated VCOs within the Life IC provides the channel selectivity function for the receive signals passing through the LIFE IC. The VCO frequency is controlled by the RX_VTUNE line. For proper frequency stabilization, the generated VCO signal is fed to a PLL via RX_VCO_OUT.

Figure 4-25. LIFE IC



Magic IC (Receiver)

The MAGIC_LV (U500) handles the backend processing for the GSM850, DCS and PCS (VLIF: RX_I, RX_I_X, RX_Q, and RX_Q_X) signal lines from LIFE. Simply, MAGIC_LV performs an analog to digital conversion of I /Q and sends it to the data to the board processor (POG) via the SSI (serial synchronous interface).

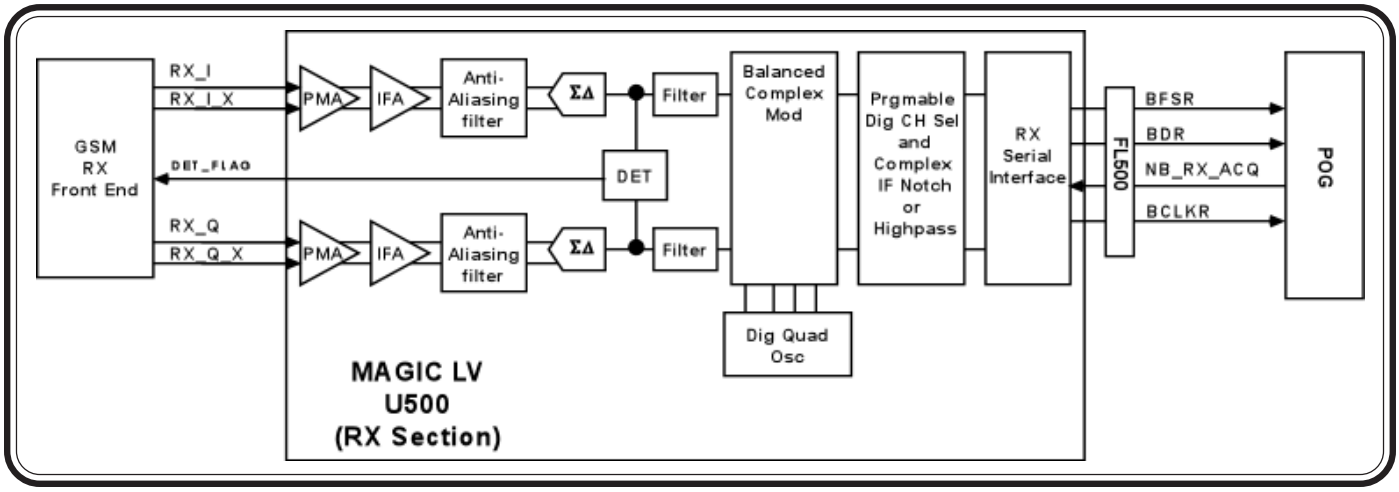
In MAGICLV, each channel is comprised of a Post Mixer Amplifier (PMA), an integrated passive two pole filter, a gain stage followed by an active programmable 2 pole anti-aliasing filter. This is followed by a lowpass sigma-delta ADC with a programmable oversampling clock OVSCLK (derived from the reference oscillator) equal to 13MHz for 200kHz channel spacing (13bits).

Digital detector circuits are placed on each channel at the output of the sigma delta converters. The outputs of these detectors are compared against a level defined by DET_LVL. If either of the detected levels exceeds the programmed threshold then the pin DET_FLAG is set high. This indicates that the signal level is excessively high for the sigma delta modulator. DET_FLAG is read by the processor, which will respond by reprogramming one of the AGC settings to a lower gain until DET_FLAG returns low.

The outputs of the sigma-delta modulators are digitally processed through a noise cancellation circuit, comb and decimation filters. A second programmable digital LO based on a look up ROM generates digital quadrature oscillators with programmable gain/phase correction (called balanced complex multiplier) to digitally downconvert the I/Q signals to baseband (digital zero IF) through four quadrature mixers that provide image rejection of adjacent/alternate channels. Gain/ Phase correction at a single baseband frequency is performed on the Digital Quadrature Oscillator to compensate the analog gain/phase mismatch of the quadrature I and Q paths. After baseband downconversion and image reduction, the quadrature I and Q signals are further processed by digital filters that perform channel selectivity and out of band noise rejection.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data. BDR and BFSR are outputs from MAGIC LV. BFSR is a framing signal which marks the beginning of an I,Q transfer. BDR is the serial data. The clock used for the serial transfer is BCLKR. When NB_RX_ACQ goes high MAGIC LV will activate the SSI interface in the digital receiver section. The data transmission over the serial bus will begin at the next normal occurrence of valid I and Q data, as defined internally to the digital receiver.

Figure 4-26. MAGIC Receiver Section



RF GSM Transmitter

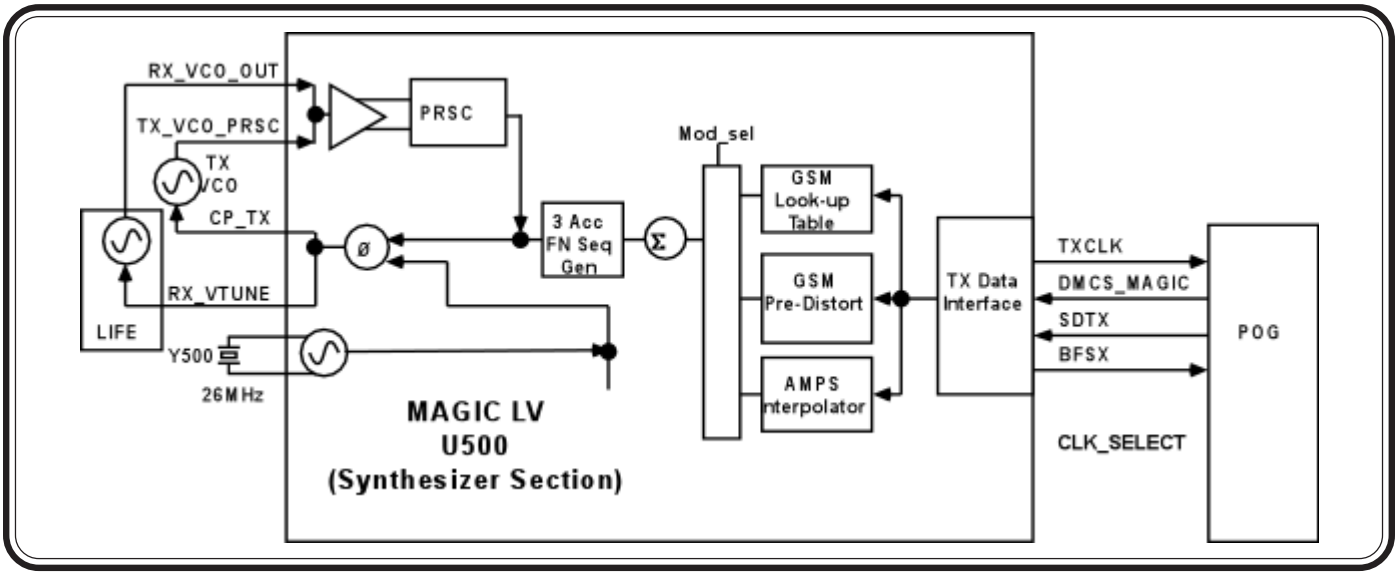
MAGIC IC (Transmitter)

The MAGIC_LV receives SSI Tx data at DMCS (digital input to start Tx modulation), TXCLK (clock for serial transfer) and SDTX (serial Tx data) from POG. The present serial data bit and the three previous data bits are used to set up one of 16 possible waveforms based on the sum of Gaussian pulses stored in a look up ROM. The resulting signal will then be clocked out at a 16x over-sampling rate. This data pattern input to three-accumulator fractional N synthesizer with a 24-bit resolution.

The VCO control lines must have compliance over an output voltage range of 0.3VDC to Vcc-0.3V. The charge pumps will have their own supply pin. The voltage on this pin is expected to be 2.775V typically to obtain sufficient compliance. This will drive external loop filters, which will in turn drive external VCOs.

A dual port modulation mode is obtained with a 9 bit D/A which follows the modulation look up table output waveform is output on the GPO3 pin. This signal is then coupled into the loop filter to add in the higher frequency components of the modulation which may have been attenuated in the main PLL path. This will allow the use of a lower bandwidth main PLL to improve the spectral purity of the transmit signal.

Figure 4-27. MAGIC Transmitter Section



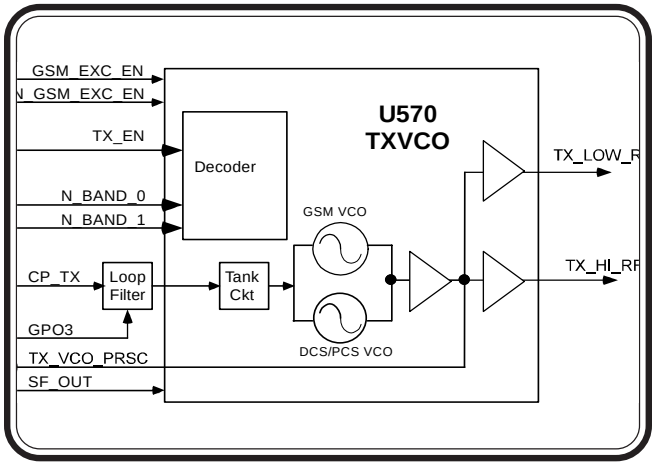
GSM TX VCO

The loop filter is designed as an active device that reacts to changes in output frequency of the MAGIC modulated charge pump and, in addition to performing the 'smoothing' function to stop any discrepancies in CP voltage being fed to the TX VCO, it also adds the high frequency modulation components from the dual port modulation output.

The Charge Pump voltage is fed to the TX VCO, U570. The operating band is selected using the N_BAND_0 and N_BAND_1 control lines. A sample of the generated TX VCO is fed back to MAGIC, via PROUT, for TX PLL operation.

The TX VCO signal is then split into the 2 buffers, which are independently switched on or off by the signals N_GSM_EXC_EN & GSM_EXC_EN. This will pass the operating frequency to it's proper path.

Figure 4-28. GSM TX VCO

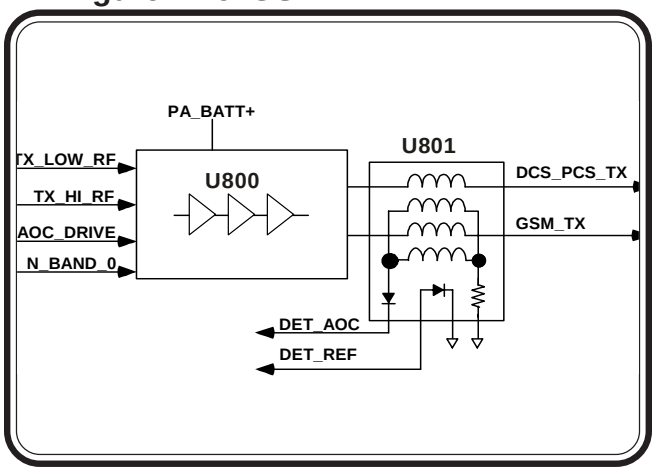


GSM TX PA

The TX signal from the TX VCO is injected into a Dual PA. Band selection for the PA is done with N_BAND_0. The gain of the PA is adjusted with AOC_DRIVE.

The automatic output design consists of a power detector, detector ADC, and TX IF AOC. The power detector U801 couples the radiated power from the output of the PA and then rectifies it into a DC level (DET_AOC). DET_AOC is then sent to a comparator integrated in the MagicLV IC. The comparator will compare the DET_AOC voltage, controlling the gain of the PA, to the sampled voltage at DET_AOC. Any difference in voltage will be applied to the AOC_DRIVE, thus, correctly tuning the PA power level.

Figure 4-29. GSM PA



RF WCDMA Receiver

The WCDMA receiver architecture consists of dual conversion, zero-IF receiver which is built around MAX2400 (U300), and the Harmony Lite ICs. The MAX2400 provides the first conversion to provide the receive IF and converts the receive IF signal into analog I&Q signals which are fed into Harmony Lite.

MAX2400

The MAX2400 (U300) is a fully integrated direct-conversion receiver IC family for WCDMA applications, targeting the emerging 3GPP market.

The MAX2400 provides a complete solution for the 3GPP WCDMA FDD receiver (2110-2170MHz, 3.84Mcps) from antenna to baseband I/Q outputs, eliminating the use of an off-chip IF SAW filter and of RFVCO.

The MAX2400 receiver IC has over 90 dB of dynamic gain control, partitioned between RF and baseband sections. It consists of an ultra-low current LNA with on-chip output matching and two-step gain modes. The zero-IF demodulator has a differential circuit topology for best input IP2 and for minimum LO leakage to receiver‘s input. The channel selectivity is done completely in the baseband section of the receiver with an on-chip low-pass filter. The AGC section has over 50dB of gain control range. LO quadrature generation is done on-chip trough a divide-by-2 prescaler. The DC-offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop connected over the AGC section. For large DC-offsets transients, very fast settling time is obtain by automatic optimization of the time-constant of the DC-offset cancellation circuit.

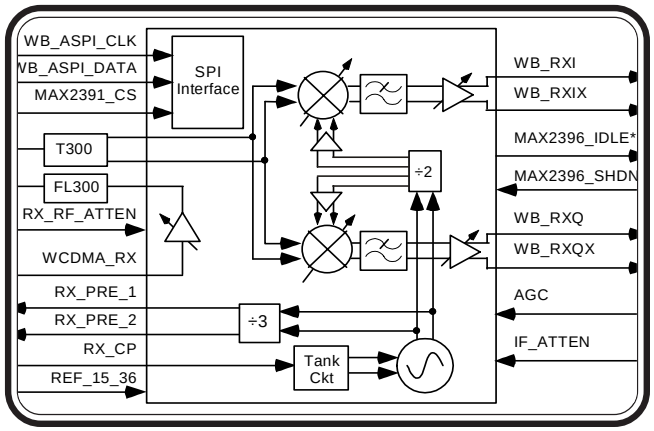
The AGC ensures that the I/Q inputs to HARMONY LITE are at constant signal level. The IF_AGC line is controlled by HARMONY_LITE with a DC control range of 1.2V to 2.1V.

The MAX2400 includes a 3-wire serial bus for PLL programming and for configuring the different receiver modes. The MAX2400_SHDN* line is used for full device shutdown and the MAX2400_ILDE* line is used for device idle mode.

RX_RF_ATTEN controls the LNA gain control pin of the MAX2400(U300), allowing high gain mode operation for low RF signal conditions and low-gain mode for high RF signal conditions. IF_ATTEN controls the mixer gain control pin of the MAX2400, allowing high gain mode operation for low IF signals and low gain mode for high IF signals.

The MAX2400 VCO frequency is controlled by an external phase lock loop (PLL) synthesizer found in the Harmony Lite. The VCO output frequency at RX_PRE_1 and RX_PRE_2 is through a divide-by-3 prescalar. The VCO output signal is then fed into the PLL synthesizer found in the Harmony Lite. . The internal phase detector within Harmony Lite drives the charge pump, RX_CP. The RX_CP line drives the tunable resonant network, altering the VCO frequency and closing the loop.

Figure 4-30. MAX2400 Block



Harmony Lite (Receiver)

The HARMONY LITE (U101) handles the backend processing of the WCDMA in phase (RX_I+, RX_I-) and quadrature (RX_Q+, RX_Q-) signals from the demodulator. The HARMONY LITE performs an analog to digital conversion of gain, phase and DC offset correction of the RX data and sends it to the POG (U1000) via data lines BBIF_RX(9:0).

The analog I and Q signals are applied to the Harmony Lite IC, which processes the analog baseband portion of the radio. The SOS detector is used as an off-channel detector to detect the level of undesired interfering signals. It monitors the voltage swing at the input to the baseband filters, and provides a logic level output to the AGC/RSSI controller to indicate if the level is greater than a threshold specified by SPI bits, which then sets the appropriate gain setting in the front-end and IF stages.

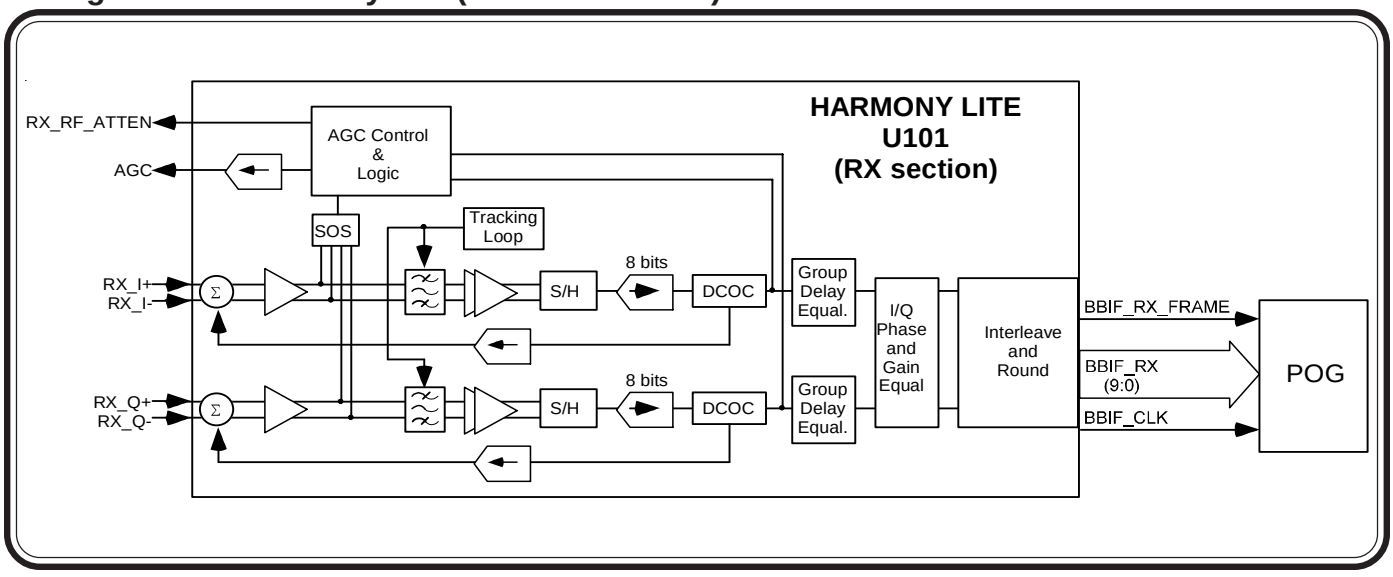
The AGC system provides overload protection for both the strong on-channel signal and the off-channel portion of the signal (interferers) that is present in the RF receive band. Signal levels are detected at the baseband filter inputs of the Harmony Lite (off-channel detector) as well as after the channel filtering and analog-to-digital conversion (on-channel detector). The digital AGC/RSSI block controls the bypass mode of the LNA and the IF variable gain amplifier. A digital representation of the desired received signal strength is sent to the POG via the SPI.

Low pass filtering is performed on the complex I and Q signals, and then applied to the associated 8-bit ADCs and sampled at a rate of 4 times per symbol. A DC offset correction loop corrects for any DC offsets at the I and Q ADC inputs. A group delay equalizer is employed in the receive signal path following the baseband SRRC filter to minimize performance loss from the analog active order SRRC channel filter.

Gain and phase mismatches between the I and Q channels can affect the detectability of a WCDMA signal in static and multipath fading conditions due to distortion caused in the QPSK signal constellation map. Thus, I/Q magnitude and phase imbalance correction circuits are used.

At the output of the Magnitude Equalizer, the I and Q

Figure 4-31. Harmony Lite (Receive Section)



values are rounded from 8 bits to 6 bits and then multiplexed and routed to the digital signal processing circuitry located on the POG IC.

The digital I&Q signals will then be fed into the WCSP module of the POG where RX bit rate data is converted to chip rate data.

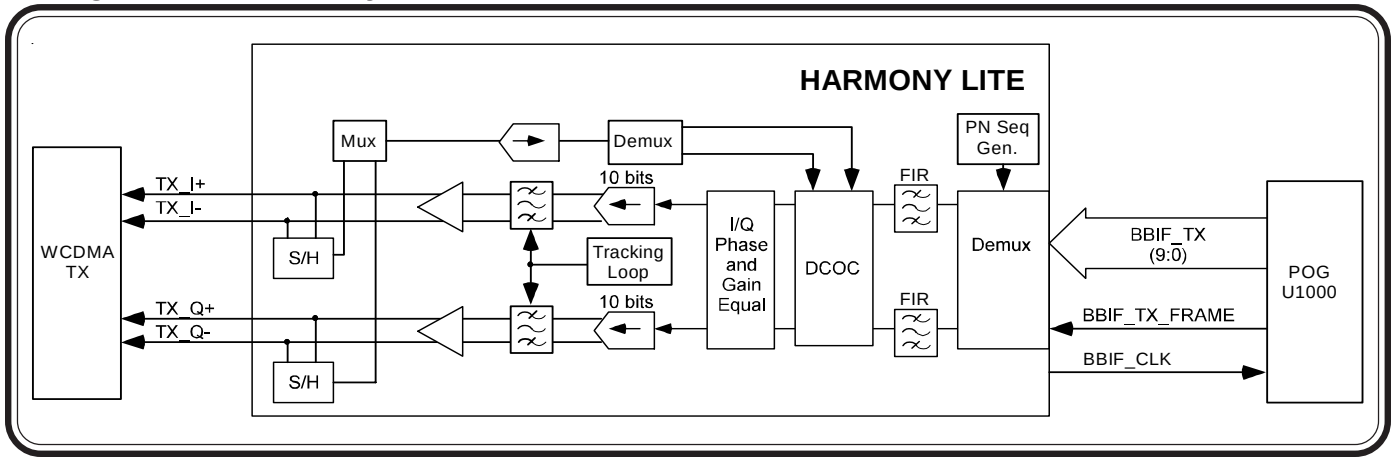
RF WCDMA Transmitter

Harmony Lite (Transmitter)

The BBIF(BBIF_TX) is the transmit data path for transferring digitally sampled I / Q data from the POG. The demultiplexing unit performs the I/Q deinterleaving function to supply separate I and Q channel data into the transmit FIR filters. The FIR filter design is used to meet 3GPP spec requirements of simultaneous transmission of a pilot channel and of multiple data channels each requiring a different spreading code and each requiring separate power control. The PN sequence generator provides I/Q interleaved 8-bit PN data into the demultiplexing section. The DC correction (DCOC) block is able to correct for DC offsets due to the D/A's, anti-aliasing filters, and transmit FIR filters in a feedback control loop. A mixed mode control loop located at the output of the transmit FIR filter is employed to correct DC offsets and I/Q gain imbalances, i.e. DCOC and I/Q Phase and Gain equalizer.

The outputs of the I/Q gain equalization unit is fed into 10-bit I and Q DAC's. The programmable gain anti-aliasing filters, or TX smoothing filters, accepts differential I/Q signals of DC to 1.92MHz frequency components from the D/A Converters to attenuate the unwanted clock signals of 15.36MHz and to smooth the signals for the TX modulator (MAX2400). The output of the TX smoothing filters are then fed into a multiplexed 6-bit A/D with sample/hold scheme. This gives the information of the amplitude and the DC common mode voltage from the I / Q Tx filter outputs by a single Analog-to-Digital Converter (ADC) as the part of digital correction loop.

Figure 4-32. Harmony Lite Transmit Section



MC13786

The MC13786 is an integrated I/Q modulator, IF and RF variable gain amplifier, UHF frequency synthesizer with a fully integrated VCO, image-reject upconverter mixer, and linear PA driver.

The synthesizer or phase locked loop (PLL) consists of a buffer amplifier, multi-modulus prescaler (divide by 4, 5, 6, and 7), a sixbit programmable post divider, reference divider, phase detector, and charge pump. The PLL uses a reference frequency of 15.36 MHz. One frequency synthesizer/VCO provides both the main and offset LO functions. The VCO operates over a frequency range of 2114 MHz to 2263 MHz and is fully integrated.

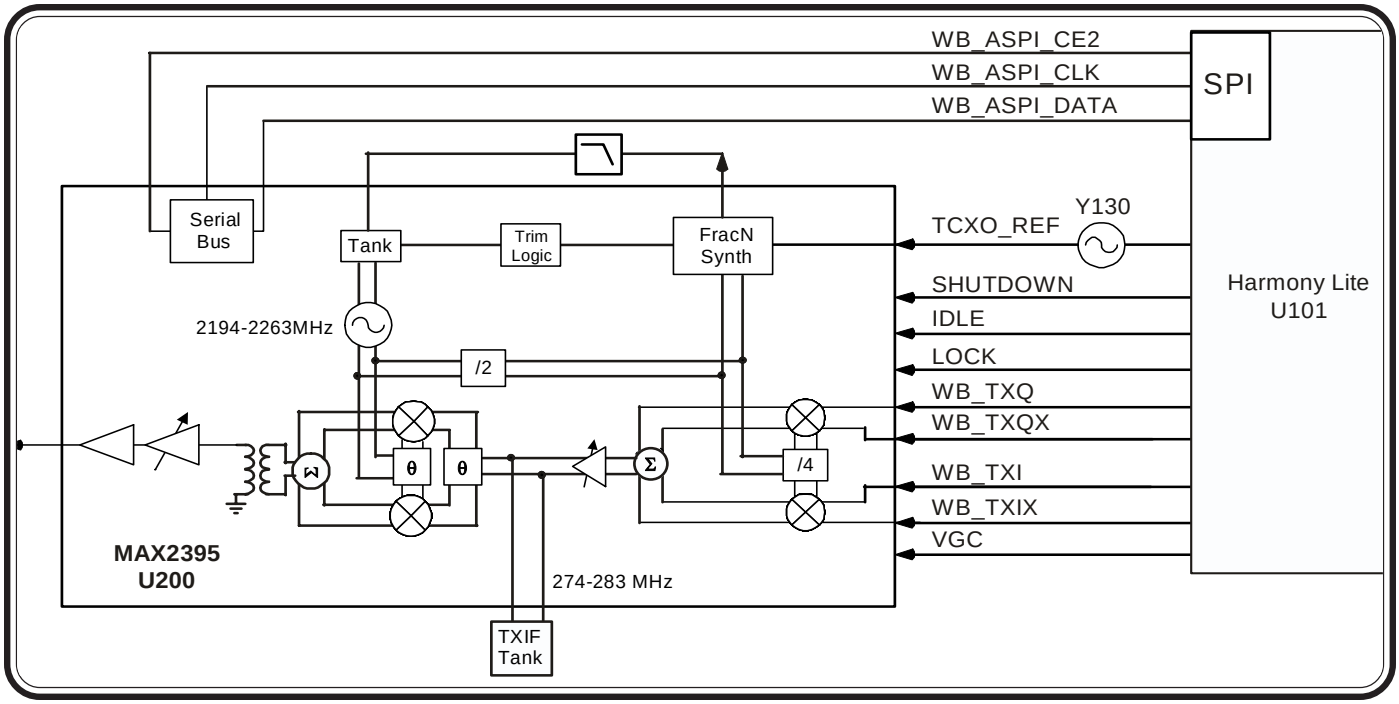
The I/Q Modulator consists of a quadrature generator and two Gilbert Cell active mixers. Using the offset LO and quadrature generator, the active mixers modulate the differential baseband I/Q signals onto a TXIF signal. Depending on the channel selection, the TXIF frequency will range from 274 MHz to 283 MHz.

From the active mixers, the TXIF signal is fed into a IF Variable Gain Amplified (IF VGA). The IF VGA has 70 dB of total typical gain control range and is controlled by the VGC line. The output of the VGA shall have a single pole bandpass tank circuit to provide attenuation to far-out noise.

The upconverter has an image-reject configuration so that the unwanted sideband is rejected to decrease the linearity requirements of the VGA stage. An input polyphase filter shall provide the necessary phase shift for the IR mixer. The TXIF signal is upconverted to a TX carrier frequency ranging from 1920MHz to 1980MHz. An on-chip copper balun shall provide the differential to single ended conversion necessary for the following stages.

The VGA provides a reduction in gain and current to optimize the TX lineup for lower output power levels. The PA driver amplifies the signal to provide sufficient drive for the radio power amplifier.

Figure 4-33. MC13786



WCDMA PA

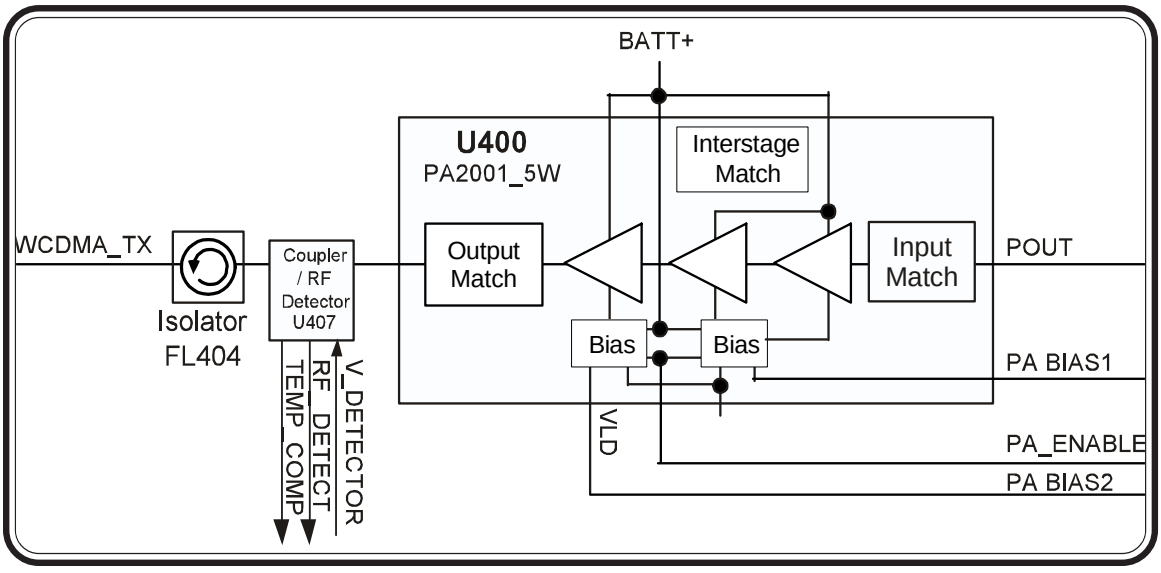
PA2001-5WPCS is a 50 Ohm PA module for 3GPP Wideband CDMA (WCDMA 1900MHz) Band II applications. Operating frequency range is from 1850 to 1910 MHz. The expected nominal gain is ~30 dB.

A Motorola proprietary high power / low power efficiency enhancement load switch (VLD) is included in the output match. VLD adjusts the output load for optimum efficiency from low power to high power out. In conjunction with VLD, bias control (PA_BIAS1/ PA_BIAS2) is performed between high and low power ranges.

The amplified WCDMA carrier is fed into a RF coupler device which has an integrated RF detector. An RF detect and Temp Comp signal will be reported to Harmony Lite for computing of RF power out.

The isolator provides a stable 50 ohm PA load. It also protects the PA from interfering with other frequency bands. Finally, it guards against IM products being produced by the transmitter and affecting receiver circuits.

Figure 4-34. WCDMA PA



Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the A845 UMTS/GSM handset.

Table 5-1. Electrical Parts List - C05x - C12x

Reference Number	Part Number	Description
C050	2113740F01	CAP, 0.5pF
C052	2113740F12	CAP, 2.4pF
C061	2113743N26	CAP, 10pF
C062	2113743N26	CAP, 10pF
C063	2113743N26	CAP, 10pF
C065	2113743N26	CAP, 10pF
C066	2113743N26	CAP, 10pF
C081	2113743N38	CAP, 33pF
C082	2113743N09	CAP, 2pF
C083	2113743L41	CAP, .01uF
C084	2113743L41	CAP, .01uF
C085	2113743N38	CAP, 33pF
C086	2113743N38	CAP, 33pF
C090	2113743N26	CAP, 10pF
C091	2113743N26	CAP, 10pF
C092	2113743N26	CAP, 10pF
C093	2113743N26	CAP, 10pF
C101	2113928P04	CAP, 1.0uF
C102	2113928P04	CAP, 1.0uF
C103	2113928P04	CAP, 1.0uF
C104	2113743L17	CAP, 1000pF
C105	2113743L17	CAP, 1000pF
C106	2113928N01	CAP, 0.1uF
C107	2113743N28	CAP, 12pF
C1029DNP	2113743M24	CAP, 0.1uF
C110	2113928C04	CAP, 4.7uF
C112	2113928P04	CAP, 1.0uF
C113	2113928P04	CAP, 1.0uF
C114	2113928P04	CAP, 1.0uF
C115	2113743L17	CAP, 1000pF
C116	2113928N01	CAP, 0.1uF
C117	2113928N01	CAP, 0.1uF
C118	2113928C04	CAP, 4.7uF
C119	2113928N01	CAP, 0.1uF
C120	2113928N01	CAP, 0.1uF
C121	2113928N01	CAP, 0.1uF
C122	2113928N01	CAP, 0.1uF
C123	2113928N01	CAP, 0.1uF

Table 5-2. Electrical Parts List - C12x - C30x

Reference Number	Part Number	Description
C124	2113928N01	CAP, 0.1uF
C125	2113928C04	CAP, 4.7uF
C126	2113928C04	CAP, 4.7uF
C127	2113928N01	CAP, 0.1uF
C128	2113928C04	CAP, 4.7uF
C130	2113928N01	CAP, 0.1uF
C131	2113743L41	CAP, .01uF
C132	2113743L41	CAP, .01uF
C133	2113743L17	CAP, 1000pF
C140	2113743E10	CAP, .033uF
C141	2113743L21	CAP, 1500pF
C156	2113743N34	CAP, 22pF
C157	2113743N34	CAP, 22pF
C160	2187893N01	CAP, 1.0uF
C200	2113743N38	CAP, 33pF
C201	2113743L41	CAP, .01uF
C202	2113743N38	CAP, 33pF
C203	2113743L41	CAP, .01uF
C204	2113743N38	CAP, 33pF
C205	2113743L41	CAP, .01uF
C206	2113743N38	CAP, 33pF
C208	2187906N01	CAP, 4.7uF
C209	2113743L41	CAP, .01uF
C207DNP	2113743L41	CAP, .01uF
C210	2113743N38	CAP, 33pF
C214	2113743L17	CAP, 1000pF
C216	2113743N40	CAP, 39pF
C217	2113743L41	CAP, .01uF
C218	2113743L09	CAP, 470pF
C219	2113743L41	CAP, .01uF
C212DNP	2113743N36	CAP, 27pF
C213DNP	2113743N50	CAP, 100pF
C220	2113743N38	CAP, 33pF
C222	2113743N60	CAP, 5pF
C243DNP	2187893N01	CAP, 1.0uF
C250	2113743N38	CAP, 33pF
C275	2113743L41	CAP, .01uF
C297	2113947E01	CAP, .01uF
C300	2113743L41	CAP, .01uF
C301	2113743N26	CAP, 10pF
C302	2113743N26	CAP, 10pF
C303	2113743N18	CAP, 4.7pF
C306	2113743N18	CAP, 4.7pF
C309	2113743L41	CAP, .01uF

Table 5-3. Electrical Parts List - C31x - C51x

Reference Number	Part Number	Description
C311	2113743L17	CAP, 1000pF
C312	2113743N50	CAP, 100pF
C313	2113743L41	CAP, .01uF
C317	2113743N50	CAP, 100pF
C360	2113743L41	CAP, .01uF
C361	2113743L41	CAP, .01uF
C390DNP	2113743N43	CAP, 51pF
C3960DNP	2113743L35	CAP, 5600pF
C413	2113743N28	CAP, 12pF
C4105DNP	2113743N38	CAP, 33pF
C420	2113743N30	CAP, 15pF
C421	2113743L41	CAP, .01uF
C422	2113743G26	CAP, 4.7uF
C425	2113743N34	CAP, 22pF
C4202DNP	2113743L13	CAP, 680pF
C4303DNP	2113743N38	CAP, 33pF
C4307DNP	2113743N38	CAP, 33pF
C4352DNP	2113743N38	CAP, 33pF
C4389DNP	2113928P04	CAP, 1.0uF
C441	2113743L41	CAP, .01uF
C444	2113743L41	CAP, .01uF
C445	2113743N50	CAP, 100pF
C448	2113743N26	CAP, 10pF
C449	2113743L41	CAP, .01uF
C4402DNP	2113743N26	CAP, 10pF
C442DNP	2113743N50	CAP, 100pF
C443DNP	2113743N50	CAP, 100pF
C450	2113743N30	CAP, 15pF
C452	2113743N30	CAP, 15pF
C455	2113743L09	CAP, 470pF
C462	2113743N30	CAP, 15pF
C503	2113743L01	CAP, 220pF
C504	2113743L13	CAP, 680pF
C505	2113741F45	CAP, 6800pF
C506	2113743L41	CAP, .01uF
C507	2113743N50	CAP, 100pF
C508	2113743N01	CAP, 0.5pF
C509	2113743N50	CAP, 100pF
C502DNP	2113743L41	CAP, .01uF
C510	2113743M24	CAP, 0.1uF
C511	2113928C03	CAP, 1.0uF
C512	2113743N09	CAP, 2pF
C513	2113743L41	CAP, .01uF
C514	2113743L41	CAP, .01uF

Table 5-4. Electrical Parts List - C51x - C58x

Reference Number	Part Number	Description
C515	2113743L41	CAP, .01uF
C516	2113928C03	CAP, 1.0uF
C517	2113743L17	CAP, 1000pF
C518	2113947E01	CAP, .01uF
C520	2113928C04	CAP, 4.7uF
C521	2113928C04	CAP, 4.7uF
C522	2113928C04	CAP, 4.7uF
C523	2113928C04	CAP, 4.7uF
C524	2113743N34	CAP, 22pF
C525	2113743N28	CAP, 12pF
C526	2113743N30	CAP, 15pF
C527	2113743N32	CAP, 18pF
C528	2113743N38	CAP, 33pF
C534	2113743N34	CAP, 22pF
C535	2113743L17	CAP, 1000pF
C536	2113743L41	CAP, .01uF
C537	2113928C04	CAP, 4.7uF
C538	2113928P04	CAP, 1.0uF
C539	2113743L41	CAP, .01uF
C5300DNP	2113743F18	CAP, 2.2uF
C5301DNP	2113928E03	CAP, 2.2uF
C5302DNP	2113743F18	CAP, 2.2uF
C540	2113743L41	CAP, .01uF
C541	2113743L41	CAP, .01uF
C543	2113928P04	CAP, 1.0uF
C545	2113928P04	CAP, 1.0uF
C546	2113928P04	CAP, 1.0uF
C554	2113743L01	CAP, 220pF
C555	2113743L05	CAP, 330pF
C556	2113743L05	CAP, 330pF
C5501DNP	2113743N26	CAP, 10pF
C5502DNP	2113743N26	CAP, 10pF
C550DNP	2113743N42	CAP, 47pF
C551DNP	2113743N42	CAP, 47pF
C552DNP	2113743N42	CAP, 47pF
C570	2113743M24	CAP, 0.1uF
C571	2113743L03	CAP, 270pF
C572	2113743L19	CAP, 1200pF
C573	0888600M19	CAP, 3300pF
C576	2113743L05	CAP, 330pF
C577	2113743N17	CAP, 4.3pF
C578	2113743N17	CAP, 4.3pF
C579	0662057M34	RES, 22
C580	2113743M24	CAP, 0.1uF

Table 5-5. Electrical Parts List - C58x - C80x

Reference Number	Part Number	Description
C581	2113743N37	CAP, 30pF
C582	2113743N09	CAP, 2pF
C583	2113743N17	CAP, 4.3pF
C600	2113743N34	CAP, 22pF
C601	2113743N13	CAP, 3pF
C602	2113743L41	CAP, .01uF
C604	2113743L05	CAP, 330pF
C605	2113743L05	CAP, 330pF
C606	2113743N54	CAP, 150pF
C607	2113743L05	CAP, 330pF
C608	2113743L05	CAP, 330pF
C609	2113743N54	CAP, 150pF
C6011DNP	2113743N09	CAP, 2pF
C6050DNP	2113743L41	CAP, .01uF
C6051DNP	2113743L41	CAP, .01uF
C6055DNP	2113928C04	CAP, 4.7uF
C614	2311049A76	CAPP, 2.2uF
C615	2113743N36	CAP, 27pF
C6102DNP	2113743N38	CAP, 33pF
C6103DNP	2113743N38	CAP, 33pF
C677	2113743N36	CAP, 27pF
C678	2113743N36	CAP, 27pF
C679	2113743N36	CAP, 27pF
C680	2113743N36	CAP, 27pF
C681	2113743N36	CAP, 27pF
C682	2113743N36	CAP, 27pF
C684	2113928C03	CAP, 1.0uF
C685	2113743L41	CAP, .01uF
C686	2113928C03	CAP, 1.0uF
C7513DNP	2113928N01	CAP, 0.1uF
C7933DNP	2113743M24	CAP, 0.1uF
C800	0662057M01	RES, 0
C801	2113743N12	CAP, 2.7pF
C807	2113743N37	CAP, 30pF
C849	2113743N28	CAP, 12pF
C850	2113743N28	CAP, 12pF
C851	2113743N38	CAP, 33pF
C852DNP	2113743N50	CAP, 100pF
C860	2113743E20	CAP, 0.1uF
C861	2113743N26	CAP, 10pF
C862	2113743E20	CAP, 0.1uF
C863	2113743N26	CAP, 10pF
C864	2113743G26	CAP, 4.7uF
C865	2113743E20	CAP, 0.1uF

Table 5-6. Electrical Parts List - C80x - C13xx

Reference Number	Part Number	Description
C866	2113743E20	CAP, 0.1uF
C867	2113743N30	CAP, 15pF
C868	2113743N30	CAP, 15pF
C901DNP	2113743N42	CAP, 47pF
C902DNP	2113743N42	CAP, 47pF
C903DNP	2113743N42	CAP, 47pF
C911	2113743N26	CAP, 10pF
C1001	2113947H01	CAP, 0.1uF
C1002	2113947H01	CAP, 0.1uF
C1003	2113947H01	CAP, 0.1uF
C1004	2113947H01	CAP, 0.1uF
C1005	2113947H01	CAP, 0.1uF
C1006	2113743M24	CAP, 0.1uF
C1007	2113743M24	CAP, 0.1uF
C1008	2113947H01	CAP, 0.1uF
C1011	2113947H01	CAP, 0.1uF
C1012	2113743M24	CAP, 0.1uF
C1013	2113743M24	CAP, 0.1uF
C1014	2113743M24	CAP, 0.1uF
C1016	2113947H01	CAP, 0.1uF
C1017	2113947H01	CAP, 0.1uF
C1019	2113743M24	CAP, 0.1uF
C1021	2113743M24	CAP, 0.1uF
C1022	2113743M24	CAP, 0.1uF
C1024	2113743M24	CAP, 0.1uF
C1025	2113743M24	CAP, 0.1uF
C1027	2113947H01	CAP, 0.1uF
C1028	2113743M24	CAP, 0.1uF
C1030	2113743M24	CAP, 0.1uF
C1033	2113743M24	CAP, 0.1uF
C1036	2113947H01	CAP, 0.1uF
C1038	2113743M24	CAP, 0.1uF
C1039	2113947H01	CAP, 0.1uF
C1040	2113743M24	CAP, 0.1uF
C1042	2113743M24	CAP, 0.1uF
C1045	2113947H01	CAP, 0.1uF
C1046	2113743M24	CAP, 0.1uF
C1047	2113743M24	CAP, 0.1uF
C1091	2113928P04	CAP, 1.0uF
C1300	2113743M24	CAP, 0.1uF
C1301	2113743M24	CAP, 0.1uF
C1302	2113743M24	CAP, 0.1uF
C1304	2113743M24	CAP, 0.1uF
C1305	2113743M24	CAP, 0.1uF

Table 5-7. Electrical Parts List - C13xx - C36xx

Reference Number	Part Number	Description
C1306	2113743M24	CAP, 0.1uF
C1307	2113743M24	CAP, 0.1uF
C1308	2113743M24	CAP, 0.1uF
C1309	2113743M24	CAP, 0.1uF
C1310	2113743M24	CAP, 0.1uF
C1402	2113743M24	CAP, 0.1uF
C1403	2113743M24	CAP, 0.1uF
C1404	2113743M24	CAP, 0.1uF
C1405	2113743M24	CAP, 0.1uF
C1406	2113743M24	CAP, 0.1uF
C1500	2113743M24	CAP, 0.1uF
C1501	2113743M24	CAP, 0.1uF
C1502	2187893N01	CAP, 1.0uF
C3000	2113928C12	CAP, 10uF
C3001	2113928C12	CAP, 10uF
C3100	2113928C12	CAP, 10uF
C3101	2113928C12	CAP, 10uF
C3150	2113928C04	CAP, 4.7uF
C3200	2113928C12	CAP, 10uF
C3201	2113928C12	CAP, 10uF
C3204	2113743L41	CAP, .01uF
C3205	2113928C04	CAP, 4.7uF
C3207	2113928C12	CAP, 10uF
C3208	2113743N42	CAP, 47pF
C3210	2113928C12	CAP, 10uF
C3212	2113928R03	CAP, 0.47uF
C3250	2113928C04	CAP, 4.7uF
C3300	2113928C04	CAP, 4.7uF
C3350	2113928C12	CAP, 10uF
C3400	2113928C12	CAP, 10uF
C3401	2113928C12	CAP, 10uF
C3402	2113743M24	CAP, 0.1uF
C3450	2113928C04	CAP, 4.7uF
C3500	2113928C12	CAP, 10uF
C3501	2113928C12	CAP, 10uF
C3550	2113928C04	CAP, 4.7uF
C3560	2113928C12	CAP, 10uF
C3561	2113928C12	CAP, 10uF
C3562	2113743M24	CAP, 0.1uF
C3600	2113928C04	CAP, 4.7uF
C3601	2113743M24	CAP, 0.1uF
C3650	2113928C04	CAP, 4.7uF
C3651	2113743M24	CAP, 0.1uF
C3652	2113947B05	CAP, 33pF

Table 5-8. Electrical Parts List - C36xx - C43xx

Reference Number	Part Number	Description
C3660	2113743M24	CAP, 0.1uF
C3661	2113743M24	CAP, 0.1uF
C3670	2113743M24	CAP, 0.1uF
C3673	2113743L41	CAP, .01uF
C3701	2113928C12	CAP, 10uF
C3702	2113928N01	CAP, 0.1uF
C3703	2113928C12	CAP, 10uF
C3704	2113743N26	CAP, 10pF
C3801	2113928C04	CAP, 4.7uF
C3850	2113928C04	CAP, 4.7uF
C3851	2113928C04	CAP, 4.7uF
C3950	2113928C04	CAP, 4.7uF
C3962	2113743M24	CAP, 0.1uF
C3963	2113743M24	CAP, 0.1uF
C3964	2113743M24	CAP, 0.1uF
C3980	2113928C03	CAP, 1.0uF
C3983	2113743N30	CAP, 15pF
C3984	2113743N30	CAP, 15pF
C4000	2113743M24	CAP, 0.1uF
C4002	2113743L21	CAP, 1500pF
C4003	2113743N38	CAP, 33pF
C4007	2113743N38	CAP, 33pF
C4009	2113947B05	CAP, 33pF
C4100	2113928P04	CAP, 1.0uF
C4102	2113928P04	CAP, 1.0uF
C4160	2113743N38	CAP, 33pF
C4161	2113743N26	CAP, 10pF
C4198	2113743M24	CAP, 0.1uF
C4199	2113947H01	CAP, 0.1uF
C4200	2187893N01	CAP, 1.0uF
C4203	2113743N38	CAP, 33pF
C4204	2113743N38	CAP, 33pF
C4207	2113743N38	CAP, 33pF
C4208	2113947B05	CAP, 33pF
C4209	2113743N38	CAP, 33pF
C4210	2113928C04	CAP, 4.7uF
C4300	2113743N26	CAP, 10pF
C4304	2113947E01	CAP, .01uF
C4306	2311049A89	CAPP, 22uF
C4355	2113947B05	CAP, 33pF
C4356	2311049A89	CAPP, 22uF
C4390	2113743M24	CAP, 0.1uF
C4392	2113743N40	CAP, 39pF
C4393	2113743N40	CAP, 39pF

Table 5-9. Electrical Parts List - C43xx - C54xx

Reference Number	Part Number	Description
C4395	2113743M24	CAP, 0.1uF
C4400	2113928P04	CAP, 1.0uF
C4401	2113743M24	CAP, 0.1uF
C4500	2113743M24	CAP, 0.1uF
C4501	2113743N38	CAP, 33pF
C4502	2113928C04	CAP, 4.7uF
C4550	2113743L25	CAP, 2200pF
C4551	2113743L41	CAP, .01uF
C5000	2113743M24	CAP, 0.1uF
C5002	2113947B05	CAP, 33pF
C5004	2113743M24	CAP, 0.1uF
C5005	2113928P04	CAP, 1.0uF
C5007	2113743M24	CAP, 0.1uF
C5050	2113743M24	CAP, 0.1uF
C5051	2113928P04	CAP, 1.0uF
C5103	2113743N38	CAP, 33pF
C5104	2113743N38	CAP, 33pF
C5105	2113743N38	CAP, 33pF
C5106	2113743N38	CAP, 33pF
C5107	2113743N38	CAP, 33pF
C5108	2113743N38	CAP, 33pF
C5109	2113743N38	CAP, 33pF
C5110	2113743N38	CAP, 33pF
C5111	2113743N38	CAP, 33pF
C5112	2113743N38	CAP, 33pF
C5113	2113743N38	CAP, 33pF
C5114	2113743N38	CAP, 33pF
C5115	2113743N38	CAP, 33pF
C5116	2113743L35	CAP, 5600pF
C5117	2113743L35	CAP, 5600pF
C5203	2113743N38	CAP, 33pF
C5204	2113743N38	CAP, 33pF
C5205	2113743N38	CAP, 33pF
C5208	2113743N38	CAP, 33pF
C5209	2113743N38	CAP, 33pF
C5250	2113743M24	CAP, 0.1uF
C5253	2113743M24	CAP, 0.1uF
C5255	2113743M24	CAP, 0.1uF
C5256	2113743M24	CAP, 0.1uF
C5303	2113928P04	CAP, 1.0uF
C5310	2113743N46	CAP, 68pF
C5311	2113743L25	CAP, 2200pF
C5401	2113743L41	CAP, .01uF
C5402	2113743M24	CAP, 0.1uF

Table 5-10. Electrical Parts List - C54xx - C75xx

Reference Number	Part Number	Description
C5405	2113743L41	CAP, .01uF
C5410	2113928C12	CAP, 10uF
C5412	2113928C12	CAP, 10uF
C5503	2113743N26	CAP, 10pF
C5505	2113743N26	CAP, 10pF
C5600	2113743L17	CAP, 1000pF
C5602	2187906N01	CAP, 4.7uF
C5700	2113743N38	CAP, 33pF
C6000	2113743L17	CAP, 1000pF
C6001	2113743N28	CAP, 12pF
C6002	2113743L11	CAP, 560pF
C6003	2113743L25	CAP, 2200pF
C6004	2113743N28	CAP, 12pF
C6005	2113743N28	CAP, 12pF
C6006	2113743N32	CAP, 18pF
C6007	2113743N28	CAP, 12pF
C6008	2113743N13	CAP, 3pF
C6009	2113928C04	CAP, 4.7uF
C6010	2113743L41	CAP, .01uF
C6012	2113743L17	CAP, 1000pF
C6013	2113743L41	CAP, .01uF
C6014	2113928N01	CAP, 0.1uF
C6015	2113743L17	CAP, 1000pF
C6016	2113743L17	CAP, 1000pF
C6017	2113928N01	CAP, 0.1uF
C6018	2113743L41	CAP, .01uF
C6019	2113743N12	CAP, 2.7pF
C6020	2113743N28	CAP, 12pF
C6021	2113743N26	CAP, 10pF
C6022	2113743L17	CAP, 1000pF
C6023	2113928N01	CAP, 0.1uF
C6025	2113928N01	CAP, 0.1uF
C6056	2113928C04	CAP, 4.7uF
C6101	2113928C12	CAP, 10uF
C6105	2113743M24	CAP, 0.1uF
C7501	2113928N01	CAP, 0.1uF
C7502	2113928N01	CAP, 0.1uF
C7503	2113928N01	CAP, 0.1uF
C7504	2113947H01	CAP, 0.1uF
C7506	2113928N01	CAP, 0.1uF
C7507	2113928N01	CAP, 0.1uF
C7508	2113928N01	CAP, 0.1uF
C7509	2113928N01	CAP, 0.1uF
C7510	2113928N01	CAP, 0.1uF

Table 5-11. Electrical Parts List - C75xx - FL5xx

Reference Number	Part Number	Description
C7511	2113928N01	CAP, 0.1uF
C7512	2113928N01	CAP, 0.1uF
C7900	2113928C12	CAP, 10uF
C7914	2113928N01	CAP, 0.1uF
C7915	2113928N01	CAP, 0.1uF
C7917	2113743N30	CAP, 15pF
C7918	2113743N30	CAP, 15pF
C7919	2113743N30	CAP, 15pF
C7922	2113743N42	CAP, 47pF
C7925	2113743N40	CAP, 39pF
C7926	2113743N40	CAP, 39pF
C7927	2113743N30	CAP, 15pF
C7928	2113743N36	CAP, 27pF
C7932	2113928C03	CAP, 1.0uF
C7934	2113928C12	CAP, 10uF
C7935	2113928E03	CAP, 2.2uF
C7938	2113743N30	CAP, 15pF
C7939	2187893N01	CAP, 1.0uF
C7970	2113743N42	CAP, 47pF
CR3000	4809924D18	RB520S-30
CR3100	4809653F02	MBRM120T3
CR3960	4809653F02	MBRM120T3
CR3961	4809653F02	MBRM120T3
CR5401	4809948D42	RB751V40
CR7500	4809606E08	RB715F
D852	4809496B11	QSMG-H799
D5000	4809948D42	RB751V40
E100	SHORT_RES0402	SHORT
E101	SHORT_RES0402	SHORT
E102	SHORT_RES0402	SHORT
E103	SHORT_RES0402	SHORT
E200	SHORT_RES0402	SHORT
E201	SHORT_RES0402	SHORT
E202	SHORT_RES0402	SHORT
E203	SHORT_RES0402	SHORT
E204	SHORT_RES0402	SHORT
E901	SHORT_RES0402	SHORT
FL001	4889729N02	AWS1900
FL004	5885949K03	n LDD15A
FL005	9188203L03	ACMD-7401
FL006	9188203L03	ACMD-7401
FL401	9109239M36	NWT190
FL404	5888916N01	n 16N01
FL500	9188695K04	0_5 95K04

Table 5-12. Electrical Parts List - FL5xx - L43xx

Reference Number	Part Number	Description
FL510	4889767N01	n FLTR
FL4000	4889526L03	0_5 FLTR
FL4300	4889526L04	0_5 FLTR
FL6000	9180310L36	n SAW_1575_42MHZ
FL6001	9189312N01	856228
J4100DNP	5085600J02	SPKR
J4300	0904136G01	n CONN_J
J5000	0987636K05	in CONN_J
J5100	0987817K05	in CONN_J
J5200	0987817K05	in CONN_J
J5400	3989331K01	n CONN_J
J5500DNP	3909301S02	CONTACT
J5501DNP	3909301S02	CONTACT
J7900	0987817K05	in CONN_J
L051	2409377M23	IDCTR, 4.7nH
L053	2409377M03	IDCTR, 6.8nH
L080	2489711L05	IDCTR, 5.1nH
L081	2409154M07	IDCTR, 3.3nH
L201	2409154M06	IDCTR, 2.7nH
L202	2409154M68	IDCTR, 27.0nH
L203	2409154M68	IDCTR, 27.0nH
L204	2409154M67	IDCTR, 22.0nH
L250	2409154M03	IDCTR, 1.5nH
L297	2409377M16	IDCTR, 82nH
L298	2409377M16	IDCTR, 82nH
L300	2409154M30	IDCTR, 3.3nH
L3000	2588866L14	IDCTR, 47uH
L301DNP	2409154M30	IDCTR, 3.3nH
L310	2409154M61	IDCTR, 6.8nH
L360	2462587Q39	IDCTR, 220nH
L361	2462587Q39	IDCTR, 220nH
L508	2409154M36	IDCTR, 10.0nH
L564	2409154M17	IDCTR, 22.0nH
L570	2409154M99	IDCTR, 82.0nH
L572	2409154M68	IDCTR, 27.0nH
L575	2113743N11	CAP, 2.4pF
L578	2409154M59	IDCTR, 4.7nH
L579	2409154M59	IDCTR, 4.7nH
L583	2113743N22	CAP, 6.8pF
L3100	2487659M11	IDCTR, 47uH
L3206	2588866L05	IDCTR, 2.2uH
L4006	SHORT_RES0402	SHORT
L4007	SHORT_RES0402	SHORT
L4399	2409646M13	IDCTR, 39nH

Table 5-13. Electrical Parts List - L44xx - Q39xx

Reference Number	Part Number	Description
L4400	2409646M13	IDCTR, 39nH
L5310	2589326L02	IDCTR, 0.68mH
L5600	2409154M22	IDCTR, 56.0nH
L5603	2113743N03	CAP, 1pF
L580DNP	2113743N09	CAP, 2pF
L615	2409377M03	IDCTR, 6.8nH
L801	2409154M61	IDCTR, 6.8nH
L805	2409154M67	IDCTR, 22.0nH
L806	2409154M12	IDCTR, 8.2nH
L6000	2409154M17	IDCTR, 22.0nH
L6001	2409154M42	IDCTR, 33.0nH
L6002	2409154M10	IDCTR, 5.6nH
L6003	2485984J05	IDCTR, 2.2uH
L6004	2485984J05	IDCTR, 2.2uH
L6010	2409154M22	IDCTR, 56.0nH
L7501	2409154M48	IDCTR, 100nH
L7920	2409154M18	IDCTR, 27.0nH
M001	0987378K01	SWITCH
M5200	3988904N01	CONTACT
M5201	3988904N01	CONTACT
M5400	0985888K01	n SOCKET
M5700	5962882K02	MOTOR
M7777	3989868N01	CONTACT
M7900	0989668N01	SHIELD
M7902	0989668N01	SHIELD
M8888	3989868N01	CONTACT
Q130	4809579E24	2SJ347
Q401	4809608E03	DTA114YE
Q500	4809579E65	TN0200T
Q510	4862830F01	0_80 SI8401DB
Q901	4809579E58	FDG6332C
Q902	4809579E48	FDC6306P
Q906	4809939C34	n EMB10
Q911	4809939C34	n EMB10
Q3301	4809579E35	FDG6301N
Q3302	4809579E35	FDG6301N
Q3310	4862830F01	0_80 SI8401DB
Q3403	4809607E04	2SB1132
Q3502	4809607E04	2SB1132
Q3610	4809607E04	2SB1132
Q3700DNP	4809579E42	FDG6304P
Q3701DNP	4809607E02	2SA1774
Q3960	4862830F01	0_80 SI8401DB
Q3961	4809807C42	0_80 SI8405DB

Table 5-14. Electrical Parts List - Q39xx - R2xx

Reference Number	Part Number	Description
Q3963	4862830F01	0_80 SI8401DB
Q3966	4862830F01	0_80 SI8401DB
Q3967	4809939C39	n EMD9
Q4300	4809940E03	DTC114TE
Q4301	4809579E24	2SJ347
Q5001	5109817F58	17F58
Q5310	4809579E64	FDG6316P
Q5400	4862830F01	0_80 SI8401DB
Q5401	4809579E58	FDG6332C
Q6000	4809579E58	FDG6332C
R061	0662057M01	RES, 0
R062	0662057M01	RES, 0
R063	0662057M01	RES, 0
R065	0662057M01	RES, 0
R066	0662057M01	RES, 0
R070	0662057U54	RES, 130
R071	0662057M41	RES, 43
R072	0662057U54	RES, 130
R080	0662057M81	RES, 2K
R081	0662057M43	RES, 51
R082	0662057M74	RES, 1K
R085	SHORT_RES0402	SHORT
R106	SHORT_RES0402	SHORT
R107	SHORT_RES0402	SHORT
R1019DNP	0662057M01	RES, 0
R1040DNP	0662057M01	RES, 0
R1046DNP	0662057M01	RES, 0
R130	0662057M74	RES, 1K
R131	0662057N09	RES, 27K
R132	0662057N09	RES, 27K
R133	SHORT_RES0402	SHORT
R140	0662057M62	RES, 330
R162	SHORT_RES0402	SHORT
R200	0662057M50	RES, 100
R203	0662057V07	RES, 15K
R204	0662057M78	RES, 1.5K
R205	0662057M61	RES, 300
R206	0662057M32	RES, 18
R207	0662057M61	RES, 300
R250	0662057M19	RES, 5.1
R258	0662057M26	RES, 10
R275	0662057M26	RES, 10
R288	0662057M01	RES, 0
R298	SHORT_RES0402	SHORT

Table 5-15. Electrical Parts List - R2xx - R5xx

Reference Number	Part Number	Description
R295DNP	0662057M41	RES, 43
R300	0662057V04	RES, 12K
R302	0662057M50	RES, 100
R305	0662057M92	RES, 5.6K
R319	SHORT_RES0402	SHORT
R320	SHORT_RES0402	SHORT
R321	SHORT_RES0402	SHORT
R322	SHORT_RES0402	SHORT
R323	SHORT_RES0402	SHORT
R3205DNP	0662057M01	RES, 0
R333	SHORT_RES0402	SHORT
R337	SHORT_RES0402	SHORT
R338	SHORT_RES0402	SHORT
R339	SHORT_RES0402	SHORT
R340	SHORT_RES0402	SHORT
R341	0662057M48	RES, 82
R342	0662057M49	RES, 91
R343	0662057M48	RES, 82
R3662DNP	0662057M01	RES, 0
R3672DNP	0662057M01	RES, 0
R3705DNP	0662057M01	RES, 0
R3706DNP	0662057M01	RES, 0
R3707DNP	0662057M98	RES, 10K
R3708DNP	0662057M98	RES, 10K
R390	0662057M01	RES, 0
R392	0662057M01	RES, 0
R391DNP	0662057M01	RES, 0
R431	SHORT_RES0402	SHORT
R432	SHORT_RES0402	SHORT
R430DNP	0662057M01	RES, 0
R440	SHORT_RES0402	SHORT
R450	0662057M95	RES, 7.5K
R451	0662057M90	RES, 4.7K
R452	0662057N17	RES, 56K
R453	0662057N08	RES, 24K
R460	0662057N01	RES, 12K
R461	0662057N09	RES, 27K
R500	SHORT_RES0402	SHORT
R501	SHORT_RES0402	SHORT
R503	0662057M83	RES, 2.4K
R504	0662057M74	RES, 1K
R506	0662057N21	RES, 82K
R5010DNP	0662057M01	RES, 0
R512	0662057N03	RES, 15K

Table 5-16. Electrical Parts List - R5xx - R8xx

Reference Number	Part Number	Description
R5101DNP	0662057M01	RES, 0
R528	SHORT_RES0402	SHORT
R536	SHORT_RES0402	SHORT
R537	0662057N01	RES, 12K
R5301DNP	0662057M01	RES, 0
R5305DNP	0662057M01	RES, 0
R5315DNP	0662057M01	RES, 0
R5317DNP	0662057N23	RES, 100K
R5406DNP	0662057M01	RES, 0
R554	0662057N07	RES, 22K
R556DNP	0662057N23	RES, 100K
R560	SHORT_RES0402	SHORT
R561	SHORT_RES0402	SHORT
R562	SHORT_RES0402	SHORT
R565	SHORT_RES0402	SHORT
R5603DNP	0662057M01	RES, 0
R571	2409154M99	IDCTR, 82.0nH
R574	0662057M64	RES, 390
R575	0662057M74	RES, 1K
R576	0662057N09	RES, 27K
R577	0662057M95	RES, 7.5K
R582	SHORT_RES0402	SHORT
R601	SHORT_RES0402	SHORT
R6007DNP	0662057M74	RES, 1K
R6031DNP	0662057M01	RES, 0
R6063DNP	0662057M01	RES, 0
R616	0662057M58	RES, 220
R626	SHORT_RES0402	SHORT
R627	0662057N30	RES, 200K
R7501DNP	0662057M01	RES, 0
R7509DNP	0662057M01	RES, 0
R7511DNP	0662057M01	RES, 0
R801	SHORT_RES0402	SHORT
R803	SHORT_RES0402	SHORT
R804	SHORT_RES0402	SHORT
R810	0662057M01	RES, 0
R811	0662057M43	RES, 51
R812	0662057M89	RES, 4.3K
R813	0662057V02	RES, 10K
R814	0662057V02	RES, 10K
R815DNP	0662057M98	RES, 10K
R816DNP	0662057M64	RES, 390
R817DNP	0662057M89	RES, 4.3K
R820	0662057U63	RES, 300

Table 5-17. Electrical Parts List - R8xx - R33xx

Reference Number	Part Number	Description
R821	SHORT_RES0402	SHORT
R901	0662057M98	RES, 10K
R902	0662057M98	RES, 10K
R903	0662057N15	RES, 47K
R904	0662057M98	RES, 10K
R912	0662057N15	RES, 47K
R920	0662057N15	RES, 47K
R921	0662057N15	RES, 47K
R925	0662057N15	RES, 47K
R975	SHORT_RES0402	SHORT
R976	SHORT_RES0402	SHORT
R977	SHORT_RES0402	SHORT
R1010	SHORT_RES0402	SHORT
R1011	SHORT_RES0402	SHORT
R1012	0662057N23	RES, 100K
R1018	SHORT_RES0402	SHORT
R1032	0662057M01	RES, 0
R1041	0662057N23	RES, 100K
R1042	0662057N23	RES, 100K
R1043	0662057M98	RES, 10K
R1047	SHORT_RES0402	SHORT
R1050	SHORT_RES0402	SHORT
R1300	SHORT_RES0402	SHORT
R1301	SHORT_RES0402	SHORT
R1302	SHORT_RES0402	SHORT
R1303	SHORT_RES0402	SHORT
R1305	0662057M86	RES, 3.3K
R1400	SHORT_RES0402	SHORT
R1500	0662057M98	RES, 10K
R1501	0662057N20	RES, 75K
R3000	0687874L02	RES, 0.1
R3001	SHORT_RES0402	SHORT
R3103	SHORT_RES0402	SHORT
R3153	SHORT_RES0402	SHORT
R3203	SHORT_RES0402	SHORT
R3204	SHORT_RES0402	SHORT
R3208	SHORT_RES0402	SHORT
R3210	0662057V40	RES, 240K
R3211	0662057V31	RES, 140K
R3212	0662057M50	RES, 100
R3251	SHORT_RES0402	SHORT
R3301	SHORT_RES0402	SHORT
R3310	SHORT_RES0402	SHORT
R3350	SHORT_RES0402	SHORT

Table 5-18. Electrical Parts List - R34xx - R40xx

Reference Number	Part Number	Description
R3402	SHORT_RES0402	SHORT
R3403	0687874L02	RES, 0.1
R3404	SHORT_RES0402	SHORT
R3451	SHORT_RES0402	SHORT
R3503	SHORT_RES0402	SHORT
R3504	0687874L02	RES, 0.1
R3553	SHORT_RES0402	SHORT
R3554	0662057M50	RES, 100
R3560	SHORT_RES0402	SHORT
R3561	0687874L02	RES, 0.1
R3601	SHORT_RES0402	SHORT
R3650	0662057M78	RES, 1.5K
R3651	0662057M36	RES, 27
R3652	0662057M36	RES, 27
R3653	SHORT_RES0402	SHORT
R3654	0662057M98	RES, 10K
R3660	0662057N23	RES, 100K
R3661	0662057N21	RES, 82K
R3670	0662057N23	RES, 100K
R3673	0662057N23	RES, 100K
R3701	SHORT_RES0402	SHORT
R3702	0662057V02	RES, 10K
R3703	0662057U98	RES, 7.5K
R3704	SHORT_RES0402	SHORT
R3801	SHORT_RES0402	SHORT
R3850	SHORT_RES0402	SHORT
R3851	SHORT_RES0402	SHORT
R3950	0662057M74	RES, 1K
R3951	SHORT_RES0402	SHORT
R3960	SHORT_RES0402	SHORT
R3961	0687874L01	RES, 0.24
R3962	0662057M92	RES, 5.6K
R3963	0662057N30	RES, 200K
R3964	SHORT_RES0402	SHORT
R3965	SHORT_RES0402	SHORT
R3966	0662057M98	RES, 10K
R3967	0662057M98	RES, 10K
R3968	0662057N30	RES, 200K
R3970	SHORT_RES0402	SHORT
R4008	0662057M34	RES, 22
R4009	0662057M34	RES, 22
R4010	0662057N39	RES, 470K
R4011	0662057N39	RES, 470K
R4012	0662057N47	RES, 1MEG

Table 5-19. Electrical Parts List - R41xx - R55xx

Reference Number	Part Number	Description
R4103	0662057M90	RES, 4.7K
R4104	0662057M68	RES, 560
R4200	0662057N03	RES, 15K
R4201	0662057N07	RES, 22K
R4290	2409154M67	IDCTR, 22.0nH
R4291	2409154M67	IDCTR, 22.0nH
R4392	0662057M68	RES, 560
R4393	0609591M37	RESNET, 10K
R4396	0662057M90	RES, 4.7K
R4397	0662057N39	RES, 470K
R4398	0662057N15	RES, 47K
R4400	0662057M50	RES, 100
R4401	0662057M74	RES, 1K
R4550	0662057N06	RES, 20K
R5000	0662057N23	RES, 100K
R5001	0662057N15	RES, 47K
R5050	0662057N15	RES, 47K
R5052	0662057N33	RES, 270K
R5053	0662057M86	RES, 3.3K
R5100	SHORT_RES0402	SHORT
R5201	SHORT_RES0402	SHORT
R5202	SHORT_RES0402	SHORT
R5250	0662057B47	RES, 0
R5251	0662057M01	RES, 0
R5291	SHORT_RES0402	SHORT
R5293	0662057M98	RES, 10K
R5294	0662057N23	RES, 100K
R5300	SHORT_RES0402	SHORT
R5302	SHORT_RES0402	SHORT
R5306	SHORT_RES0402	SHORT
R5307	0662057N21	RES, 82K
R5310	0662057N23	RES, 100K
R5312	0662057N23	RES, 100K
R5401	0662057M90	RES, 4.7K
R5402	0662057M50	RES, 100
R5403	0662057N13	RES, 39K
R5404	0662057M98	RES, 10K
R5405	0662057N39	RES, 470K
R5480	0662057M98	RES, 10K
R5481	0662057V11	RES, 22K
R5482	0662057V43	RES, 330K
R5501	0662057M93	RES, 6.2K
R5502	0662057M01	RES, 0
R5503	0662057M50	RES, 100

Table 5-20. Electrical Parts List - R55xx - R79xx

Reference Number	Part Number	Description
R5504	0662057M50	RES, 100
R5600	0662057M96	RES, 8.2K
R5601	0662057N23	RES, 100K
R5604	0662057M96	RES, 8.2K
R5605	SHORT_RES0402	SHORT
R5606	0662057N37	RES, 390K
R5607	2409154M10	IDCTR, 5.6nH
R6000	0662057U85	RES, 2.2K
R6001	SHORT_RES0402	SHORT
R6002	SHORT_RES0402	SHORT
R6005	2113743N26	CAP, 10pF
R6006	0662057M46	RES, 68
R6008	0662057V27	RES, 100K
R6020	SHORT_RES0402	SHORT
R6021	SHORT_RES0402	SHORT
R6022	SHORT_RES0402	SHORT
R6023	SHORT_RES0402	SHORT
R6025	SHORT_RES0402	SHORT
R6026	SHORT_RES0402	SHORT
R6027	SHORT_RES0402	SHORT
R6028	SHORT_RES0402	SHORT
R6032	SHORT_RES0402	SHORT
R6055	0662057V27	RES, 100K
R6056	0662057V27	RES, 100K
R6060	SHORT_RES0402	SHORT
R6061	SHORT_RES0402	SHORT
R6062	SHORT_RES0402	SHORT
R6100	0662057N23	RES, 100K
R7508	0662057M98	RES, 10K
R7510	SHORT_RES0402	SHORT
R7513	SHORT_RES0402	SHORT
R7576	SHORT_RES0402	SHORT
R7901	0662057M98	RES, 10K
R7902	0609591M25	RESNET, 1K
R7904	0662057M38	RES, 33
R7910	0662057M98	RES, 10K
R7932	0662057M74	RES, 1K
R7933	0662057M74	RES, 1K
R7936	0662057N21	RES, 82K
R7940	0662057M46	RES, 68
R7941	0662057M46	RES, 68
R7942	0662057M46	RES, 68
R7943	0662057M46	RES, 68
R7944	0662057M46	RES, 68

Table 5-21. Electrical Parts List - R79xx - U4xx

Reference Number	Part Number	Description
R7945	0662057M46	RES, 68
R7946	0662057M46	RES, 68
R7947	0662057M46	RES, 68
R7948	0662057M46	RES, 68
S1	4087635K01	SWITCH
S2	4087635K01	SWITCH
S3	4087635K01	SWITCH
SH01	2688097N01	SHIELD
SH02	2687529Y02	SHIELD
SH03	2687339Y02	SHIELD
SH04	2688100N01	SHIELD
SH05	2688101N01	SHIELD
SH06	2688102N01	SHIELD
SH07	2688103N01	SHIELD
SH08	2688104N02	SHIELD
SH09	2688105N01	SHIELD
SH10	2688106N01	SHIELD
SH11	2688107N03	SHIELD
SH12	2688108N03	SHIELD
SH13	2688109N03	SHIELD
SH14	2688110N03	SHIELD
SH15	2688111N01	SHIELD
SH16	2690079N02	SHIELD
SH17	2690080N02	SHIELD
SH18	2687810Y01	SHIELD
SW6000	0987378K01	SWITCH
T300	5885949K07	lb HHM1516
T600	5885949K08	lb HHM1409
T601	5885949K09	lb HHM1410
T602	5885949K05	lb HHM1525
TP1000	TPSM1_016	TEST_POINT
TP1005	TPSM1_016	TEST_POINT
U001	5109944C61	50 MC13820
U010	5109522E63	NC7WZ04
U011	5109522E14	rb TC7S32F
U012	5109522E14	rb TC7S32F
U013	5109522E85	NC7WZ08K
U101	5188450M11	_800 50M11
U1018DNP	5109522E90	5x1 NC7SP125
U200	5188450M22	MC13786
U300	5109817F75	gnd MAX2400
U400	5109908K91	PA2001_5WPCS
U406	5109768D08	LM20
U407	5187970L54	DD02

Table 5-22. Electrical Parts List - U5xx - U75xx

Reference Number	Part Number	Description
U500	5188450M05	0 50M05
U510	5109522E63	NC7WZ04
U570	4888481N06	n 81N06
U580	5885924L15	RAC10-1A-E
U625	5109940K41	0_8 LIFE_30PIN
U626	5185353D14	LP3985
U800	5109908K90	n 08K90
U801	5885811G11	50 DD05-EN722
U911	5109522E85	NC7WZ08K
U1000	5199149J01	4_0_8 DSPIO
U1019	5109522E14	rb TC7S32F
U1020	5109522E82	5x1 NC7SB3157
U1046	5109522E84	5x1 NC7WZ17
U1300	5199146J01	0_75 28F640W18
U1310	5199146J01	0_75 28F640W18
U1400	5109509A55	_80 K4M64163
U1500	5187482N06	00 SDBT2FCH-512
U3000	5188450M06	_5 50M06
U3200	5109512F48	LP2985
U3206	5187970L31	rb LTC3406
U3210	5113837M37	NL17SZ04
U3650	5164751E01	MC74VHC1GT50
U3651	5109522E90	5x1 NC7SP125
U3660	5186311J23	5x1 NC7SZ126
U3670	5186311J23	5x1 NC7SZ126
U3700	5109512F46	ILC7081
U3960	5109512F51	NCP304
U5000	4889526L01	0_50 CSPEMI-306
U5001	4889526L02	0_50 CSPEMI-307
U5010	5109522E82	5x1 NC7SB3157
U5011	5109522E82	5x1 NC7SB3157
U5210	5113837A30	NLSF1174
U5211	5113837A30	NLSF1174
U5220	5113837M32	NL27WZ00
U5240	5113837M31	NL17SZ74
U5300DNP	5185353D23	tgnd LM2665
U5301DNP	5113837M35	TC7W32FK
U5302DNP	5109522E14	rb TC7S32F
U5310	5186569G04	D371A
U5600	4889695L14	d 95L14
U6000	5109841C71	GPS
U6005DNP	5185963A13	LP2988
U6100	5162852A33	rb HSDL3202
U7500	5189251L03	1 MC30200

Table 5-23. Electrical Parts List - U75xx - Y60xx

Reference Number	Part Number	Description
U7510	5162852A58	NLAS44599
U7511	5162852A58	NLAS44599
U7513DNP	5109522E35	TC7S86FU
U7540	5164751E01	MC74VHC1GT50
U7541	5109522E82	5x1 NC7SB3157
VR4099	4813832M85	NZQA6V8AXV5T1
VR4300	4809948D44	0_5 CSPESD304
VR5005	4813830C29	MMSZ5246B
VR5100	4813830M74	MMBZ6V8ALT1
VR5101	4813832M85	NZQA6V8AXV5T1
VR7505	4809948D44	0_5 CSPESD304
VR7507	4809948D44	0_5 CSPESD304
VR7508	4809948D44	0_5 CSPESD304
VR7509	4809948D44	0_5 CSPESD304
VR7510	4809948D44	0_5 CSPESD304
VS4200	4809788E06	UDZTE-176.8B
VS4201	4809788E06	UDZTE-176.8B
VS5001	4813830C29	MMSZ5246B
VS5002	4809788E06	UDZTE-176.8B
VS5402	4813832M84	SD05T1
VS5405	4809788E08	UDZS8_2B
VS5400DNP	4809788E06	UDZTE-176.8B
VS5401DNP	4809788E06	UDZTE-176.8B
Y130	4809718L14	NT5032SA
Y500	4809612J43	XTAL
Y3982	4809995L13	CC5V
Y6000	4809718L20	cw TCO-5871

Service Diagrams

Introduction

The service diagrams were carefully prepared to allow a Motorola certified technician to easily troubleshoot cellular phone failures. Our professional staff provided directional labels, color coded traces and other guidelines to help a technician troubleshoot a cellular phone with speed and accuracy.

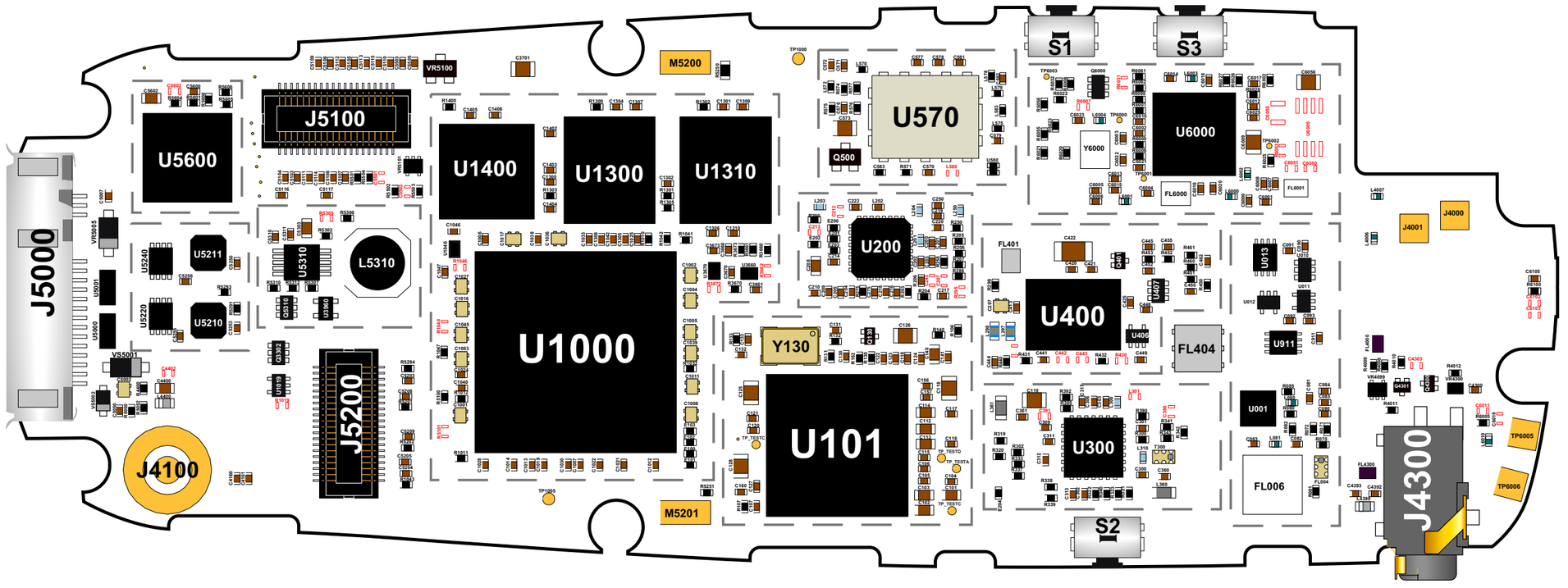
Diagrams

All illustrated diagrams relate to the latest available hardware during development of this document. Some diagrams may deviate slightly in design when compared to actual field returns. Please contact your local Motorola service support center for document updates that may relate to current designs.

The following diagrams are illustration in this section,

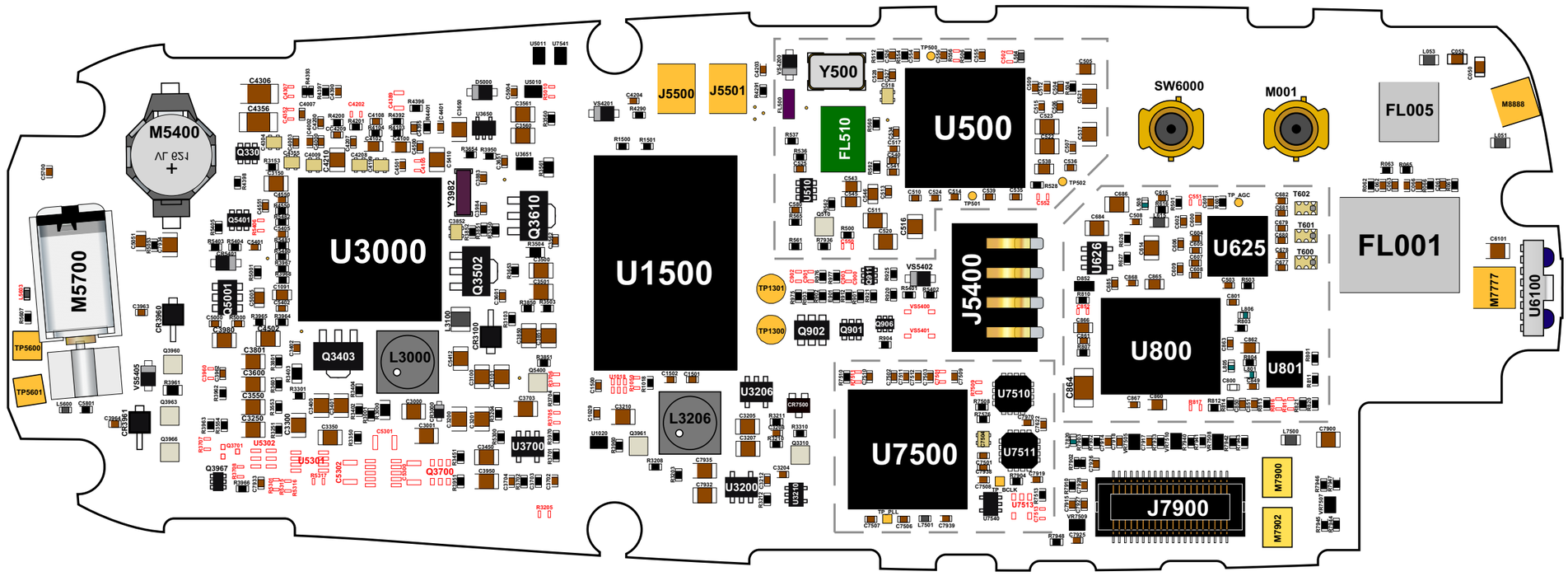
- Board Layout Side 1
- Board Layout Side 2
- Signal Flow Diagram
- Schematic Diagrams

A845: Side 1 Layout (IssO)



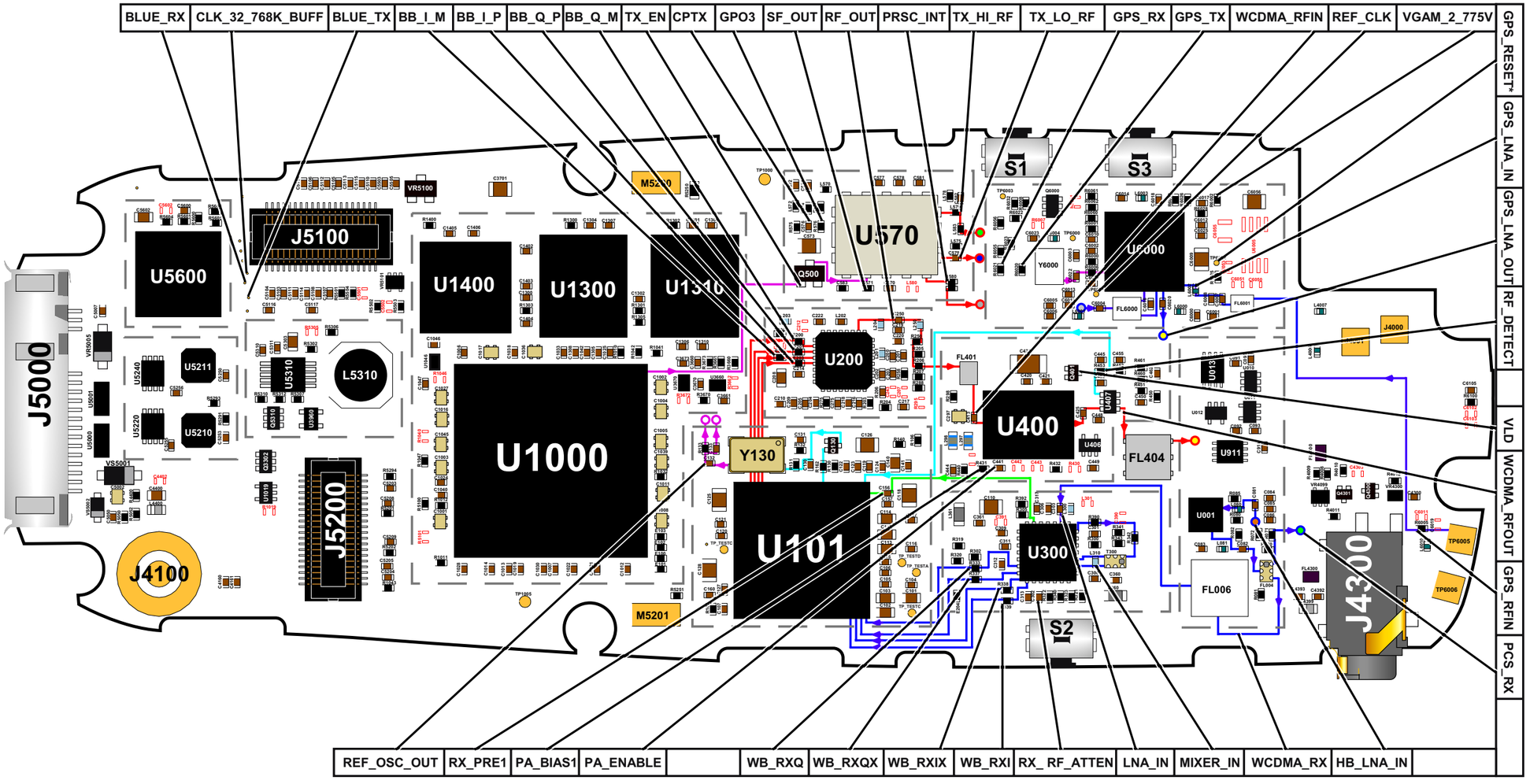
Board: 8489804N05_IssO

A845: Side 2 Layout (IssO)



Board: 8489804N05_IssO

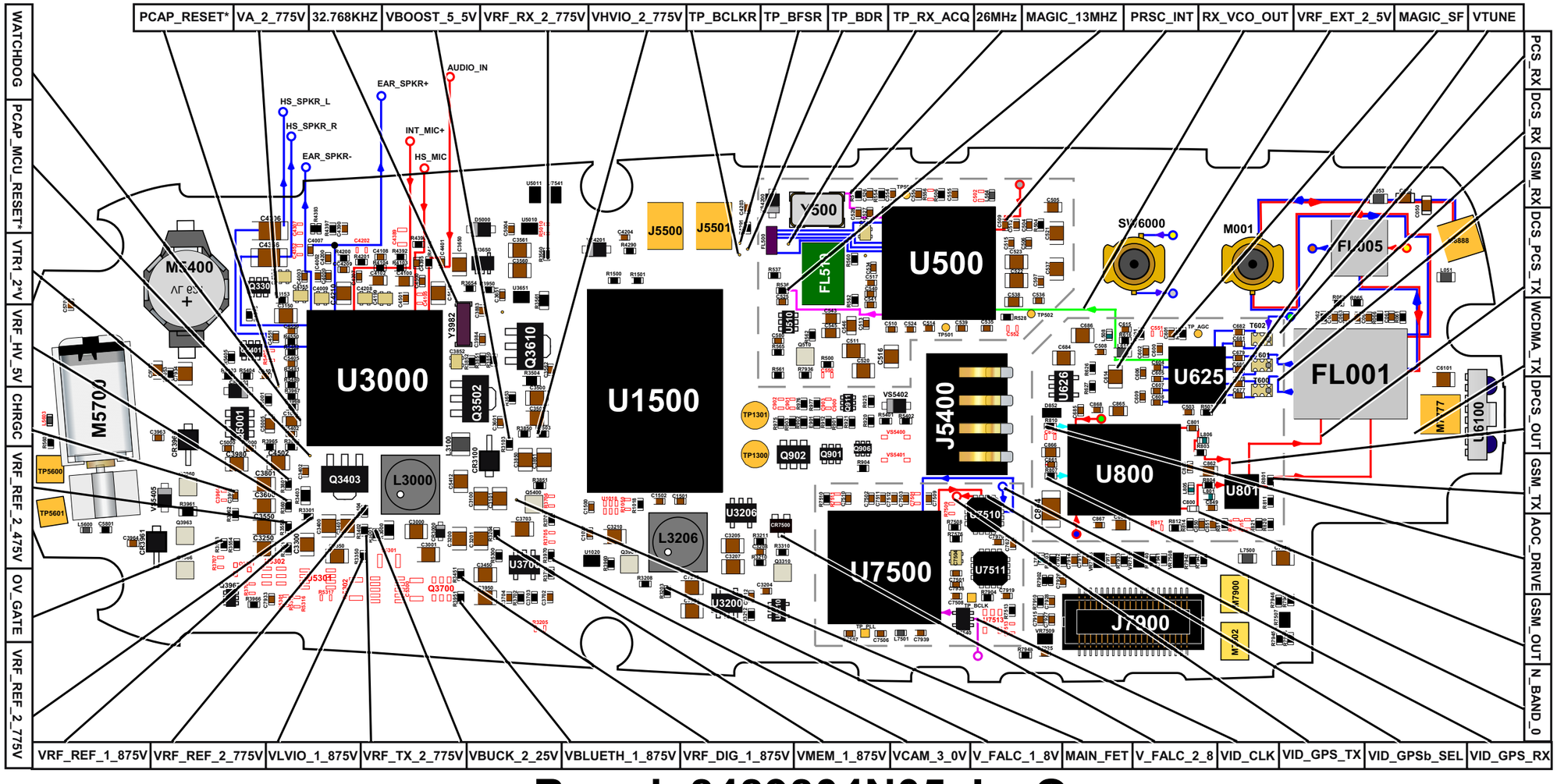
A845: Side 1 Layout (IssO)



Board: 8489804N05_IssO

TX Signal
RX Signal
VCO Signal
Reference Frequency
Control Signal

A845: Side 2 Layout (IssO)

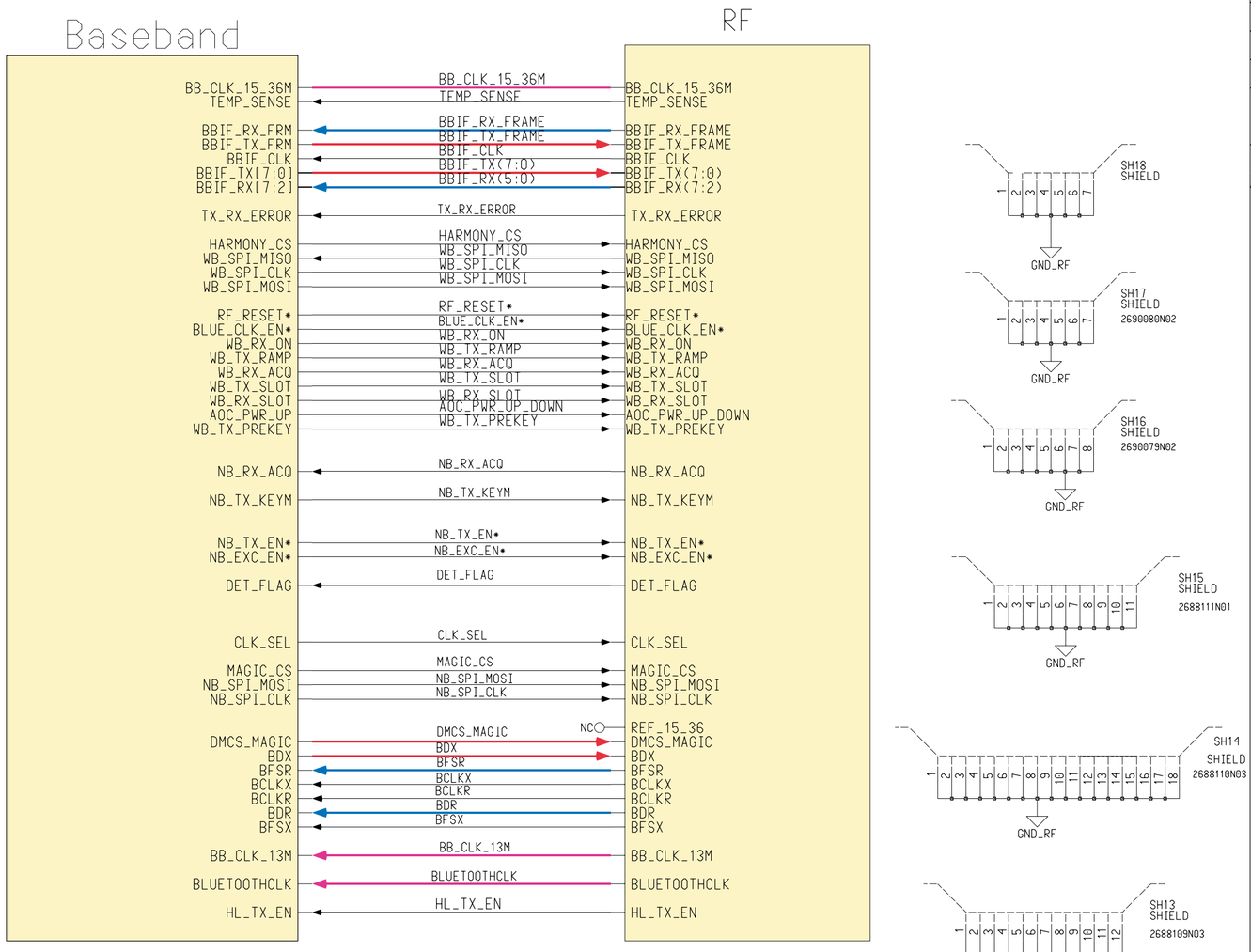


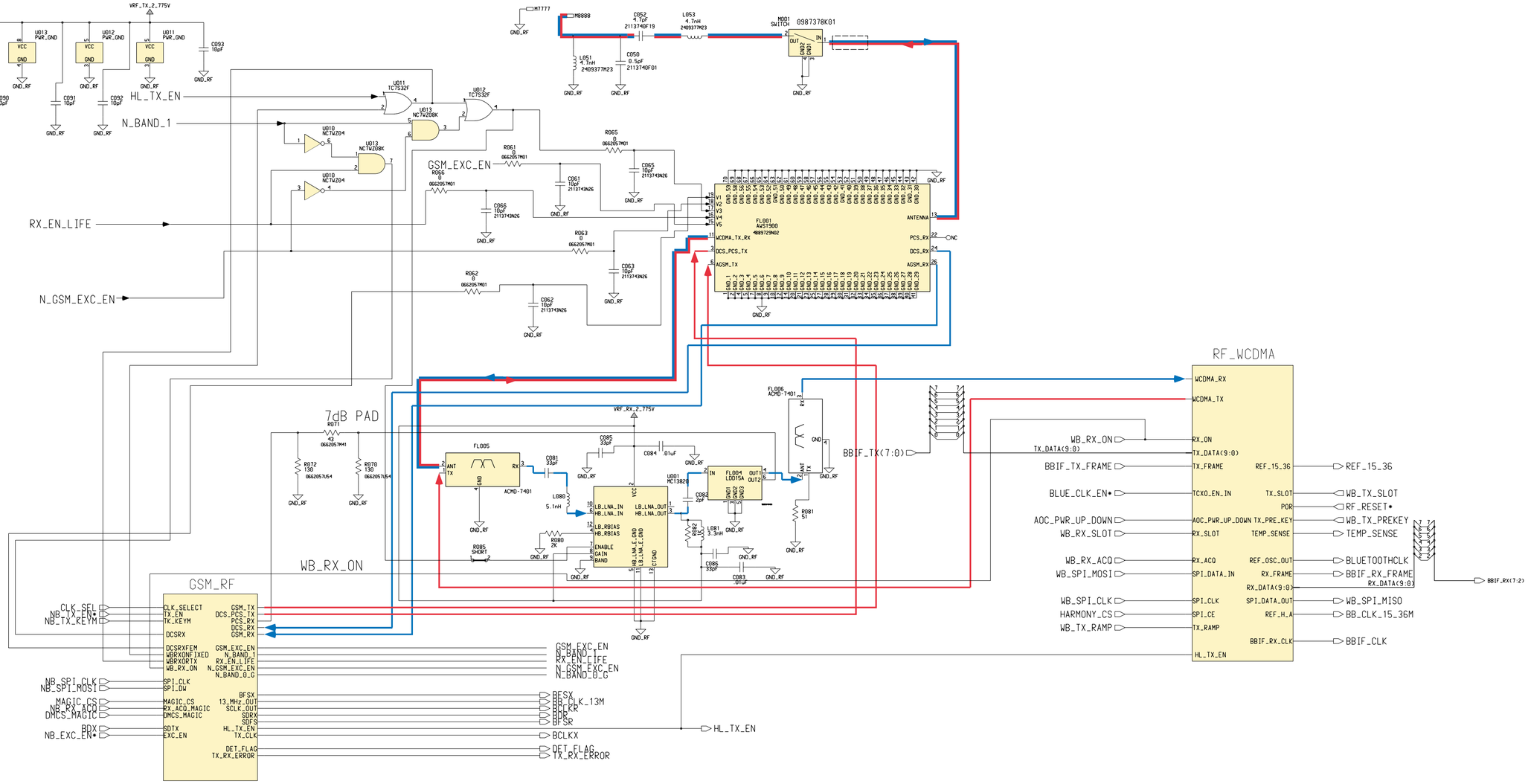
Board: 8489804N05_IssO

TX Signal
RX Signal
VCO Signal
Reference Frequency
Control Signal

MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer: Ed Naddeo	MOTOROLA INC.		
Drawn by: Ed Naddeo			
R&D CHK:	TITLE: Talon Integrated		Size: 11x17
DOC CTRL CHK:			
MFG CTRL CHK:	Top Level		
QA CHK:	REV: P3	Drawing Number: 8489804N03	Page: Of:
Changed by: Ed Naddeo	Date: January 7, 2003		Time: 10:43:18 am

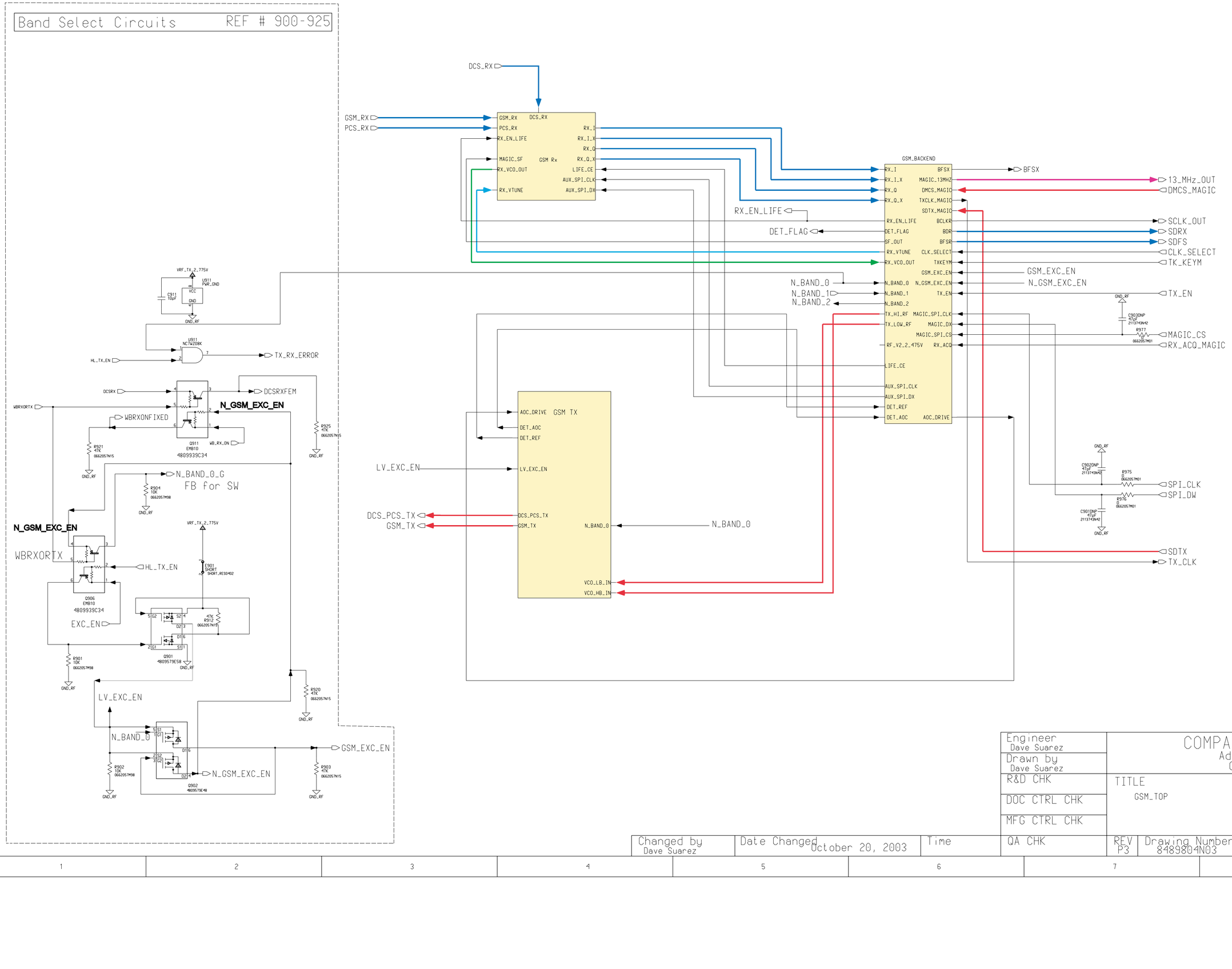




Changed by Dave Suarez	Date Changed February 26, 2004	Time 3:59:05 pm	QA CHK	REV P4B	Drawing Number 8489804N03	Sheet of	

Engineer Dave Suarez	MOTOROLA INC. 600 N US HWY 45 Libertyville, IL
Drawn by Dave Suarez	
R&D CHK	TITLE RF_TOP
DOC CTRL CHK	Size D
MFG CTRL CHK	

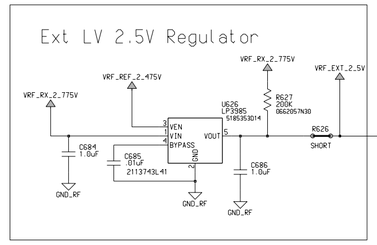
Band Select Circuits REF # 900-925



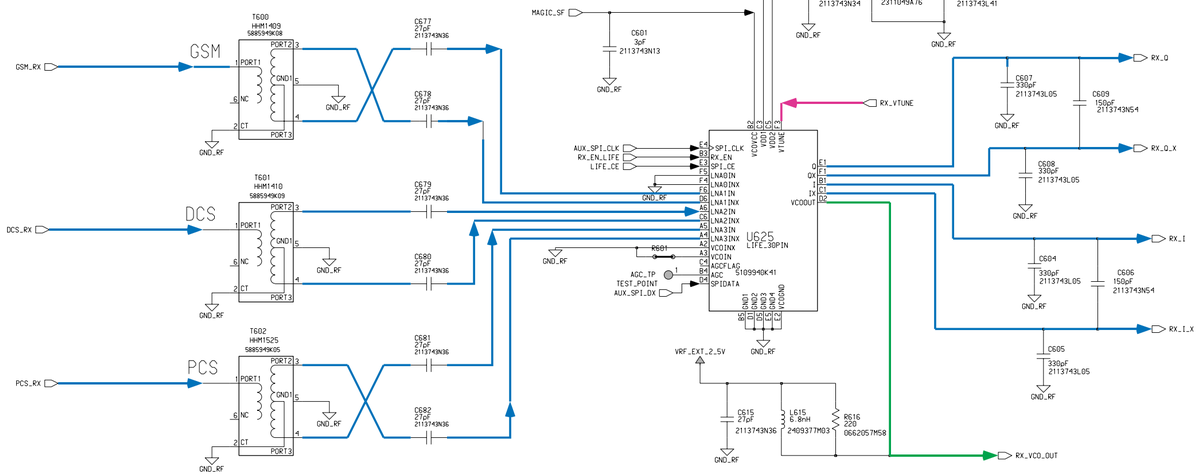
Changed by Dave Suarez	Date Changed October 20, 2003	Time	QA CHK	REV P3	Drawing Number 8489804N03

Engineer Dave Suarez	COMPANY NAME Address City	
Drawn by Dave Suarez		
R&D CHK	TITLE GSM_TOP	Size D
DOC CTRL CHK		
MFG CTRL CHK		

Sheet of



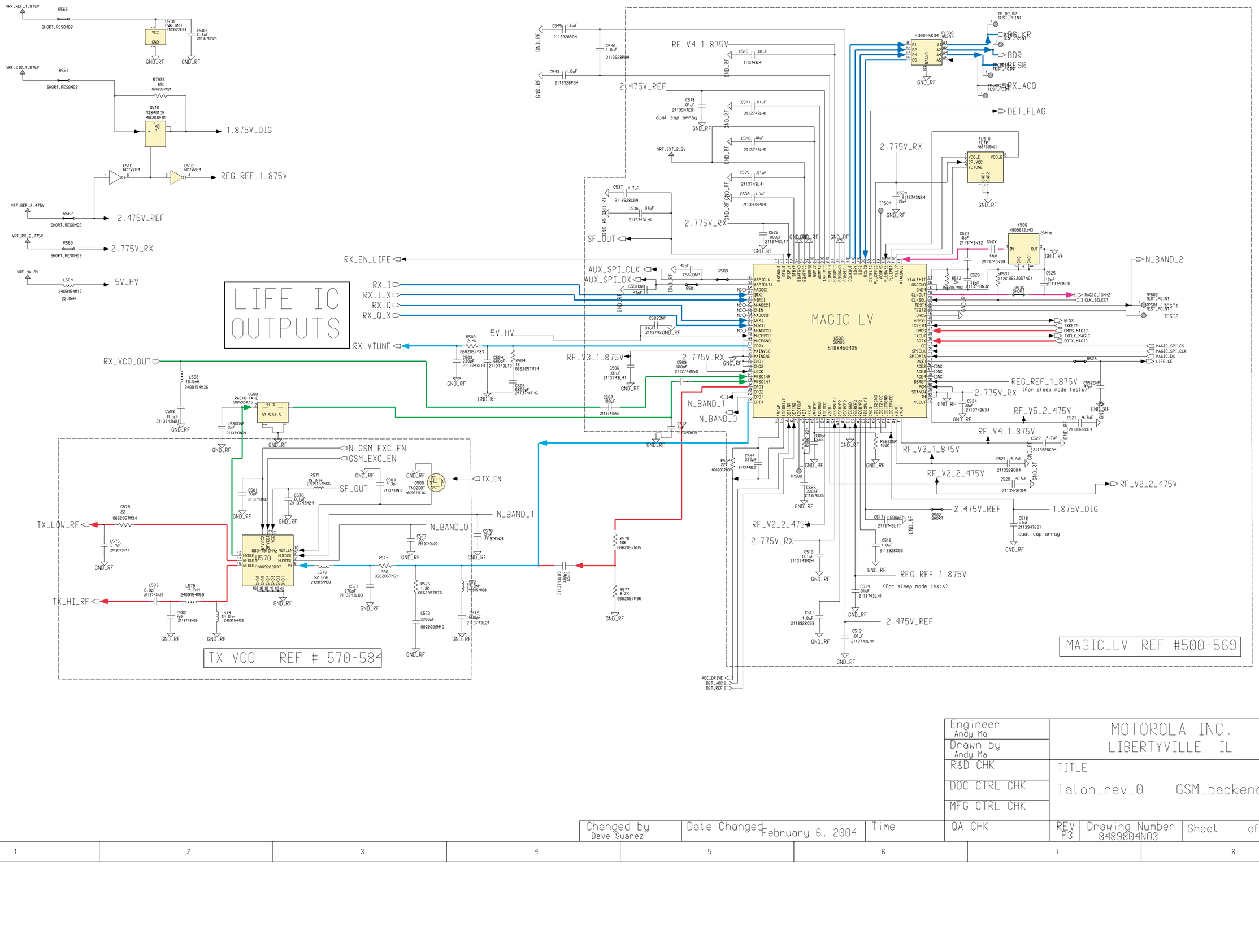
LIFE IC
REF # 600-649



Changed by Dave Suarez	Date Changed January 21, 2003	Time	QA CHK	REV P3	Drawing Number 8487729N03

Engineer Brian Elfers	COMPANY NAME Address City
Drawn by Brian Elfers	
R&D CHK	TITLE GSM_Rx — Size D
DOC CTRL CHK	
MFG CTRL CHK	

Sheet of

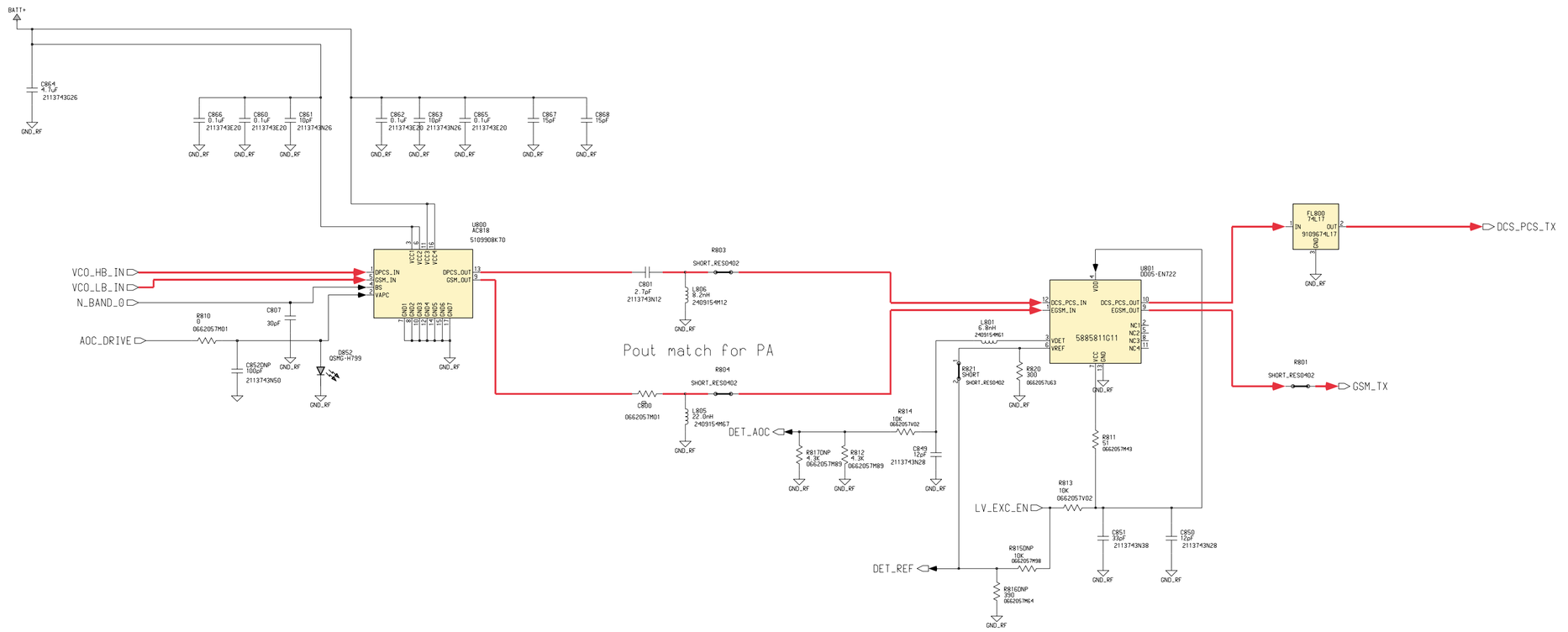


Changed by Dave Suarez	Date Changed February 6, 2004	Time	QA CHK	REV P3	Drawing Number 8489804N03

Engineer Andy Ma	MOTOROLA INC. LIBERTYVILLE IL	
Drawn by Andy Ma		
R&D CHK	TITLE Talon_rev_0 GSM_backend	Size D
DOC CTRL CHK		
MFG CTRL CHK		

Sheet of

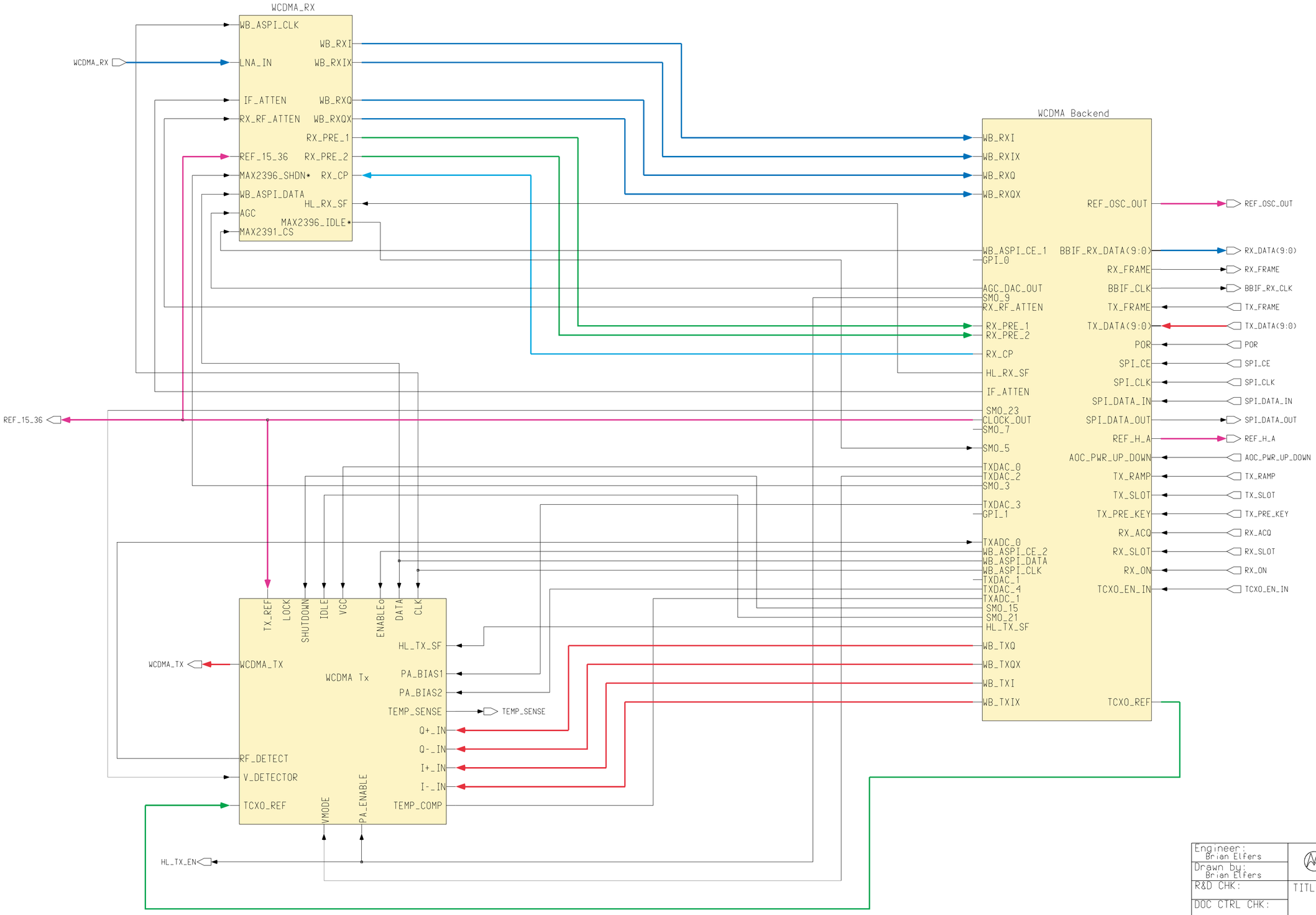
GSM Transmitter



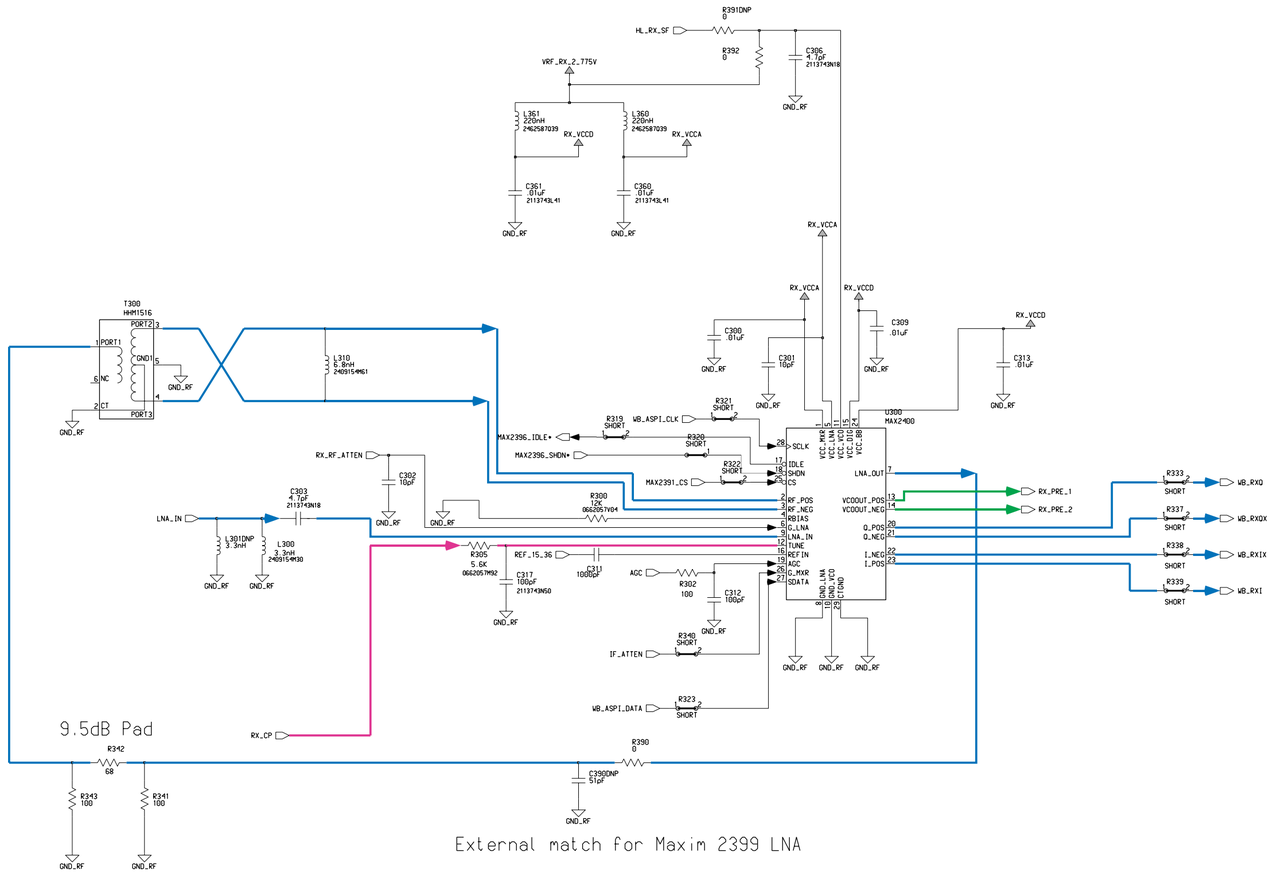
Changed by Dave Suarez	Date Changed December 10, 2003	Time	QA CHK	REV P3	Drawing Number 8489804N03

Engineer Paul Manente	COMPANY NAME Address City
Drawn by Paul Manente	
R&D CHK	TITLE GSM_TX_D GSM_Transmitter
DOC CTRL CHK	Size D
MFG CTRL CHK	

Sheet of

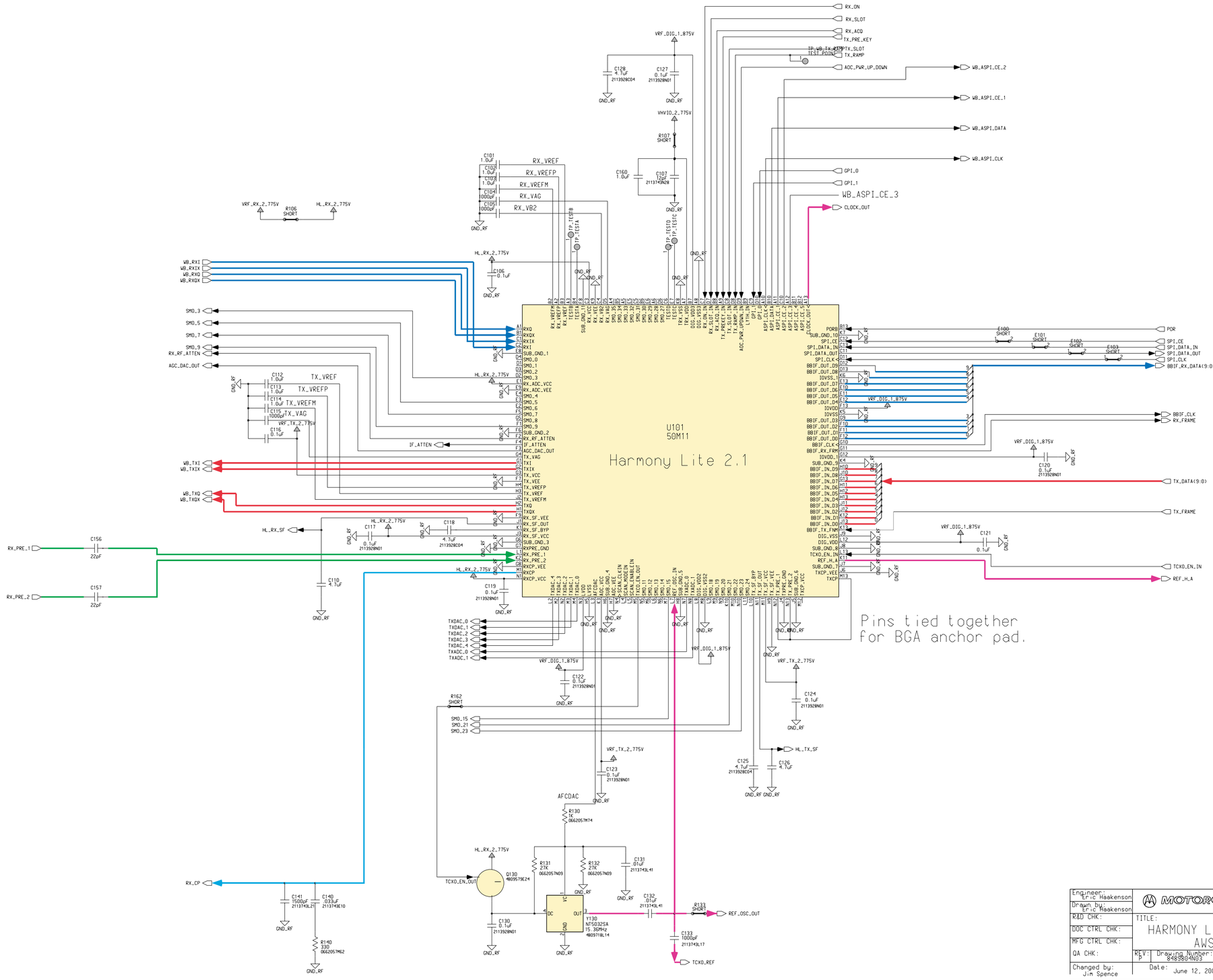


Engineer: Brian Elfers	MOTOROLA INC.		
Drawn by: Brian Elfers			
R&D CHK:	TITLE: Talon_rev_0		Size: 11x17
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV: P3	Drawing Number: 8487729N03	Page: / OF:
Changed by: Dave Suarez	Date: Friday, April 20, 2001		Time: 4:07:28 pm



External match for Maxim 2399 LNA

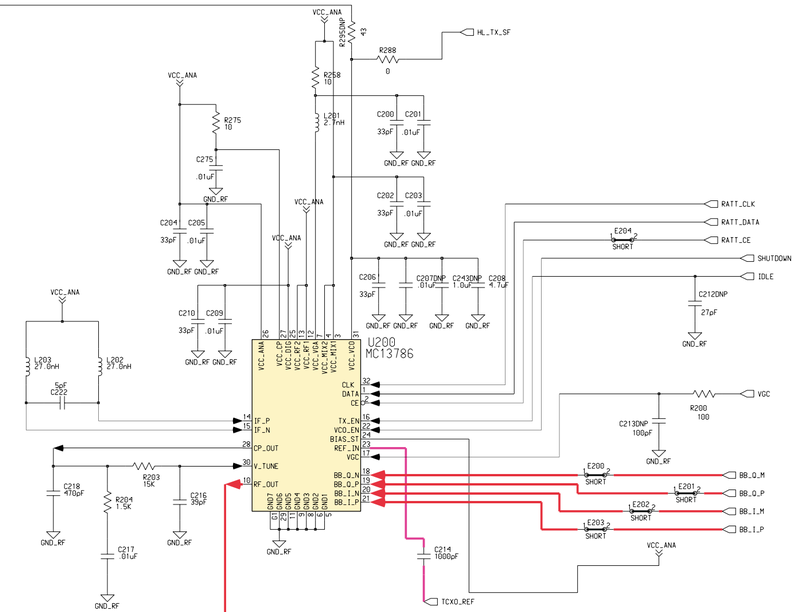
Engineer: Randy Wiessner	MOTOROLA INC.
Drawn by: Randy Wiessner	
R&D CHK:	TITLE: WCDMA_Rx — Size: D
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK: D	REV: P6 — Drawing Number: 8487729N06 — Page: — OF:
Changed by: Dave Suarez	Date: June 12, 2003 — Time: 4:33:16 pm



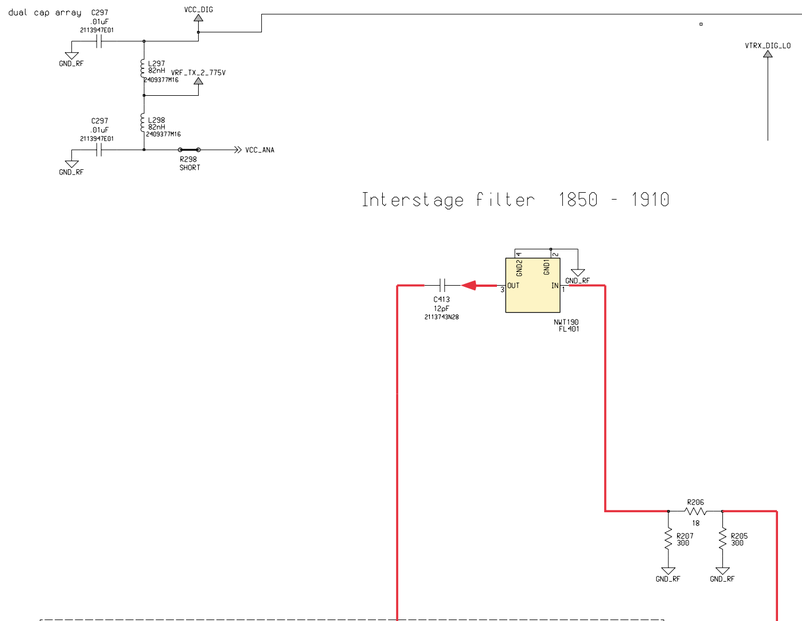
Engineer: Eric Haakenson	MOTOROLA INC.
Drawn by: Eric Haakenson	
R&D CHK:	TITLE: HARMONY LITE AWS
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: P / Drawing Number: 8489804N03 / Page: / OF:
Changed by: Jim Spence	Date: June 12, 2003 / Time:

WCDMA Transmitter (TALON)

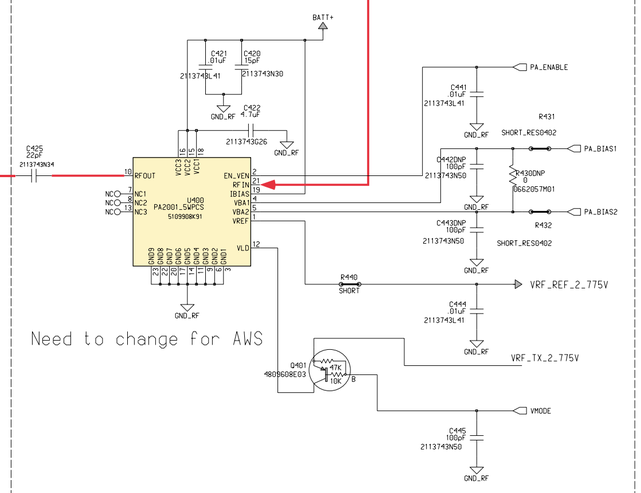
Quadrature modulator and upmixer 200-299



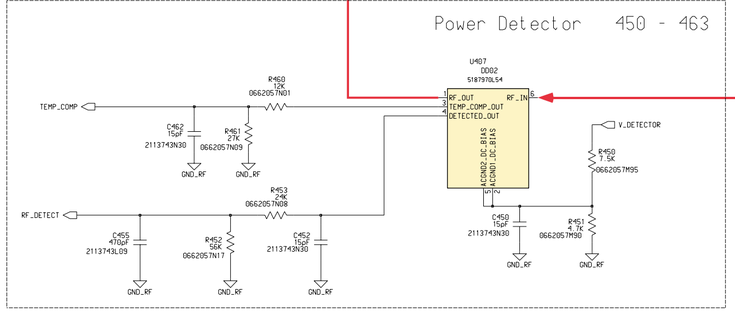
Interstage filter 1850 - 1910

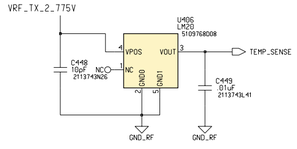


Power Amplifier 420 - 449



Power Detector 450 - 463





Changed by James Spence	Date Changed February 25, 2004	Time 4:39:58 pm	QA CHK	REV P4B	Drawing Number 8489804N04	Sheet 1 of 1	

Engineer John Mura	COMPANY NAME Address City	
Drawn by John Mura		
R&D CHK	TITLE WCDMA_Tx	Size D
DOC CTRL CHK		
MFG CTRL CHK		

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Engineer: John S. Kerr	MOTOROLA INC.
Drawn by: Todd Roesler	
R&D CHK:	TITLE: Talon Integrated Baseband Top Level
DOC CTRL CHK:	Size: 11x17
MFG CTRL CHK:	
QA CHK:	REV: Drawing Number: Page: Of:
Changed by: Ed Naddeo	Date: Monday, March 4, 2002 Time: 10:39:56 am

Misc Connectors

Display Connector USIM
Keypad Connector IrDA
Headset Jack Vibrator
Fun Lights

ALRT+
ALRT-
HS_MAKE_DETECT
HS_MIC
HS_SPKR_L
HS_SPKR_R
ON_OFF_END*
ELEN1
V_VIB
EAR_SPKR-
EAR_SPKR+

FUNLITE_GRN
FUNLITE_RED
FUNLITE_BLU
IRDA_SD
IRDA_RX
IRDA_TX
USIM_CLK
USIM_RST
USIM_IO
USIM_PD*
LCD(15:8)
LCD_CLK
LCD_HSYNC
LCD_VSYNC
CLI_SPI_CLK
CLI_SPI_DATA
CLI_CS
DISPLAY_SPI_CLK
DISPLAY_SPI_DATA
DISPLAY_CS
DISPLAY_ON
FRNT_LIGHT_CTRL
KEY(0:12)

CORE LOGIC BLOCK

POG
Memories
Video
AGPS
Embedded SD

PCAP_CLK_IN
VID_RTS*
LOGIC_SENSE
VID_CTS*
VID_GPS_RTS*
SWB+_EN
HKSW
MUTE*
DSEL2
DSEL1
DSEL0
OPT1
OPT2
DATALOG*
BLUETOOTH_WAKE*
BLUETOOTH_INT*
BLUE_TX
BLUE_CTS*
BLUE_RTS*
BLUE_RX
WB_SPI_CLK
WB_SPI_MOSI
WB_SPI_MISO
HARMONY_CS
CLK_32_768K_BUFF
ASAP_FS
ASAP_CLK
ASAP_RX
ASAP_TX
STEREO_FS
STEREO_CLK
STEREO_TX
VSIMC_EN
MUXCTL
BATT_IO
RXD.VMIN
TXD.VPOUT
RTS*.XRXD
USB_TXEN*
USB_VMOUT
USB_VPIN
USB_DETECT
BB_SPI_CLK
BB_SPI_MISO
BB_SPI_MOSI
PCAP_CS
PCAP_INT
PCAP_RESET*
USER_OFF
POWER_FAIL
PCAP_MCU_RESET*
WATCHDOG
CLK_32_768K
NB_STANDBY
VID_GPSb_SEL
MIDRATE_1
MIDRATE_2
NB_TX_KEYM
BATT_FDBK_SW
BATT_DETB

RF_RESET*
BCLKR
BFSR
BDR
BCLKX
BFSX
BDX
DMCS_MAGIC
BB_CLK_13M
CLK_SEL
NB_EXC_EN*
NB_RX_ACQ
NB_TX_EN*
NB_SPI_CLK
NB_SPI_MOSI
MAGIC_CS
TX_RX_ERROR
DET_FLAG
BBIF_RX_FRM
BBIF_RX(7:2)
BBIF_TX(7:0)
BBIF_TX_FRM
BBIF_CLK
BB_CLK_15_36M
WB_TX_RAMP
WB_RX_SLOT
WB_TX_SLOT
WB_TX_PREKEY
WB_RX_ACQ
WB_RX_ON
AOC_PWR_UP
HL_TX_EN

CE Bus Connector

VID_RTS*
LOGIC_SENSE
VID_CTS*
VID_GPS_RTS*
SWB+_EN
HKSW
MUTE*
DSEL2
DSEL1
DSEL0
OPT1
OPT2
DATALOG*
BATT_FDBK
D+
D-
AUDIO_IN
AUDIO_OUT

Bluetooth

BLUETOOTH_WAKE*
BLUETOOTH_INT*
BLUE_TX
BLUE_CTS*
BLUE_RTS*
BLUE_RX
BLUE_CLK_EN*
BLUETOOTHCLK
ASAP_FS
CLK_32_768K_BUFF
ASAP_CLK
ASAP_RX
ASAP_TX

PCAP (Power/Audio)

ASAP_FS
ASAP_CLK
ASAP_RX
ASAP_TX
STEREO_FS
STEREO_CLK
STEREO_TX
VSIMC_EN
MUXCTL
BATT_IO
RXD.VMIN
TXD.VPOUT
RTS*.XRXD
USB_TXEN*
USB_VMOUT
USB_VPIN
USB_DETECT
BB_SPI_CLK
BB_SPI_MISO
BB_SPI_MOSI
PCAP_CS
PCAP_INT
PCAP_RESET*
USER_OFF
POWER_FAIL
PCAP_MCU_RESET*
WATCHDOG
CLK_32_768K
NB_STANDBY
VID_GPSb_SEL
MIDRATE_1
MIDRATE_2
NB_TX_KEYM
BATT_FDBK_SW
BATT_DETB
AUDIO_OUT
AUDIO_IN
D-
D+
BATT_FDBK
CLK_32_768K_BUFF
PCAP_CLK_IN
ALRT+
ALRT-
HS_MAKE_DETECT
HS_MIC
HS_SPKR_L
HS_SPKR_R
TEMP_SENSE
ON_OFF_END*
ELEN1
V_VIB
EAR_SPKR
EAR_SPKR+

NB_TX_KEYM

EAR_SPKR+
EAR_SPKR-
V_VIB
ELEN1
ON_OFF_END*
HS_SPKR_R
HS_SPKR_L
HS_MIC
HS_MAKE_DETECT

ALRT-
ALRT+

MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A

Vibrator

M5700 MOTOR — OUT, IN, TAB — V_VIB

C5700 33pF

HEADSET JACK

PLUG TIP
PLUG RING
PLUG SLEEVE
PLUG SLEEVE
PLUG OUTER RING

J4300 — S1, S2, S3, S4, S5, S6 — NC

HS_DETECT — Q4300 — R4010 470K — R4011 470K — Q4301 — VHVIO_2_775V

C4303DNP 33pF

HS_MAKE_DETECT

HS_R — R4012 1MEG

HS_L

FL4300 FLTR — INPUT_1 OUTPUT_1 INPUT_2 OUTPUT_2 GND — A1 A3 B2 C1 C3

HS_SPKR_R — HS_SPKR_R / HS_SPKR_L

HS_SPKR_L

VR4300 15KV — NC NC

C4300 10pF

HS_MIC

VR4099 VOLTAGE — NC NC

EAR_SPKR- / EAR_SPKR+

Earpiece Speaker

TEST_POINT J4001 — TEST_POINT J4000

L4006 SHORT — L4007 27.0nH

FL4000 FLTR — INPUT_1 OUTPUT_1 INPUT_2 OUTPUT_2 GND — A1 A3 B2 C1 C3

R4008 22 — R4009 22

EAR_SPKR- / EAR_SPKR+

Side Keys

S1 SWITCH VOL DOWN — S2 SWITCH VA/VR — S3 SWITCH VOL UP

KEY[9] KEY[5] KEY[8] KEY[6]

Alert Speaker

J5501DNP — J5500DNP — ALRT-2 — ALRT+2

Keypad Connector

J5100 28 NC — J5100 26 NC — J5100 24 NC

J5100 32 J5100 — J5100 31 J5100 — J5100 30 J5100

J5100 29 J5100 27 J5100 25 J5100 23

J5100 12 J5100 13 J5100 14 J5100 15 J5100 16 J5100 17 J5100 18 J5100 19 J5100 20 J5100 21 J5100 22

J5100 1 J5100 2 J5100 3 J5100 4 J5100 5 J5100 6 J5100 7 J5100 8 J5100 9 J5100 10 J5100 11

Display Bezel U-clips

R5250 0 — R5251 0 — M5200 — M5201

Sanyo Display Connector

J5200 0987817K05

LCD(7) LCD(6) LCD(5) LCD(4) LCD(3) LCD(2) LCD(1) LCD(0) — R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0

LCD(15) LCD(14) LCD(13) LCD(12) LCD(11) LCD(10) LCD(9) LCD(8)

LCD(15:8) — LCD_OUT(7:0)

65K_LOGIC

LCD_IN(15:8) — LCD_CLK — LCD_OUT(7:0) — SCLK — DISPLAY_ON

LCD(15:8) — LCD_CLK

DGND DGND DGND ON/OFF LED V_LED V_LED DGND V_CC DGND DGND CS SCLK SDATA V_DD NC DGND V_DD RESET MCLK HSYNC VSYNC

FRNT_LIGHT_CTRL — 33pF C5204

R5202 SHORT — B+

C5205 33pF

DISPLAY_CS — DISPLAY_SPI_CLK — DISPLAY_SPI_DATA

R5201 SHORT — VHVIO_2_775V

C5208 33pF — C5209 33pF

DISPLAY_ON

C5203 33pF

LCD_HSYNC — LCD_VSYNC

KEY[0] KEY[1] KEY[2] KEY[3] KEY[4] KEY[5] KEY[6] KEY[7] KEY[8] KEY[9] KEY[10] KEY[11] KEY[12] — KEY[0:12]

R5100 — R5101DNP 0 — ON_OFF_END

C5112 C5111 C5106 C5103 C5109 C5104 C5105 C5114 C5113 C5108 C5115 C5107 C5110 C5116 33pF — 5600pF — C5117 5600pF

EL_LED_5V — ELEN1 — ELEN1_C

FUNLITE_RED — FUNLITE_GRN — FUNLITE_BLU

220V — EL_VOUT

EL LED Control

ELEN1_C — FUNLITE_RED — FUNLITE_GRN — FUNLITE_BLU — EL_VOUT

IrDA

VHVIO_2_775V — R6100 100K — C6105 0.1uF — C6101 10uF

U6100 HSDL3202 5162852A33 — SD VCC IOVCC VLED TXD GND GND1 AGND RXD

IRDA_SD — IRDA_TX — IRDA_RX

C6102DNP 33pF — C6103DNP 33pF

IRDA_TX — IRDA_SD

IRDA_RX

SIM Card Board Connector

VSIMC — C5503 10pF — VSIM — VR5100 6.8V — R5501 6.2K

USIM_PD

J5100 33 J5100 34 J5100 35 J5100 36 J5100 37 J5100 38 J5100 39 J5100 40 J5100

USIM_RST — R5502 — USIM_CLK — R5503 100

R5504 100 — USIM_IO

C5502DNP 10pF — C5505 10pF — C5501DNP 10pF

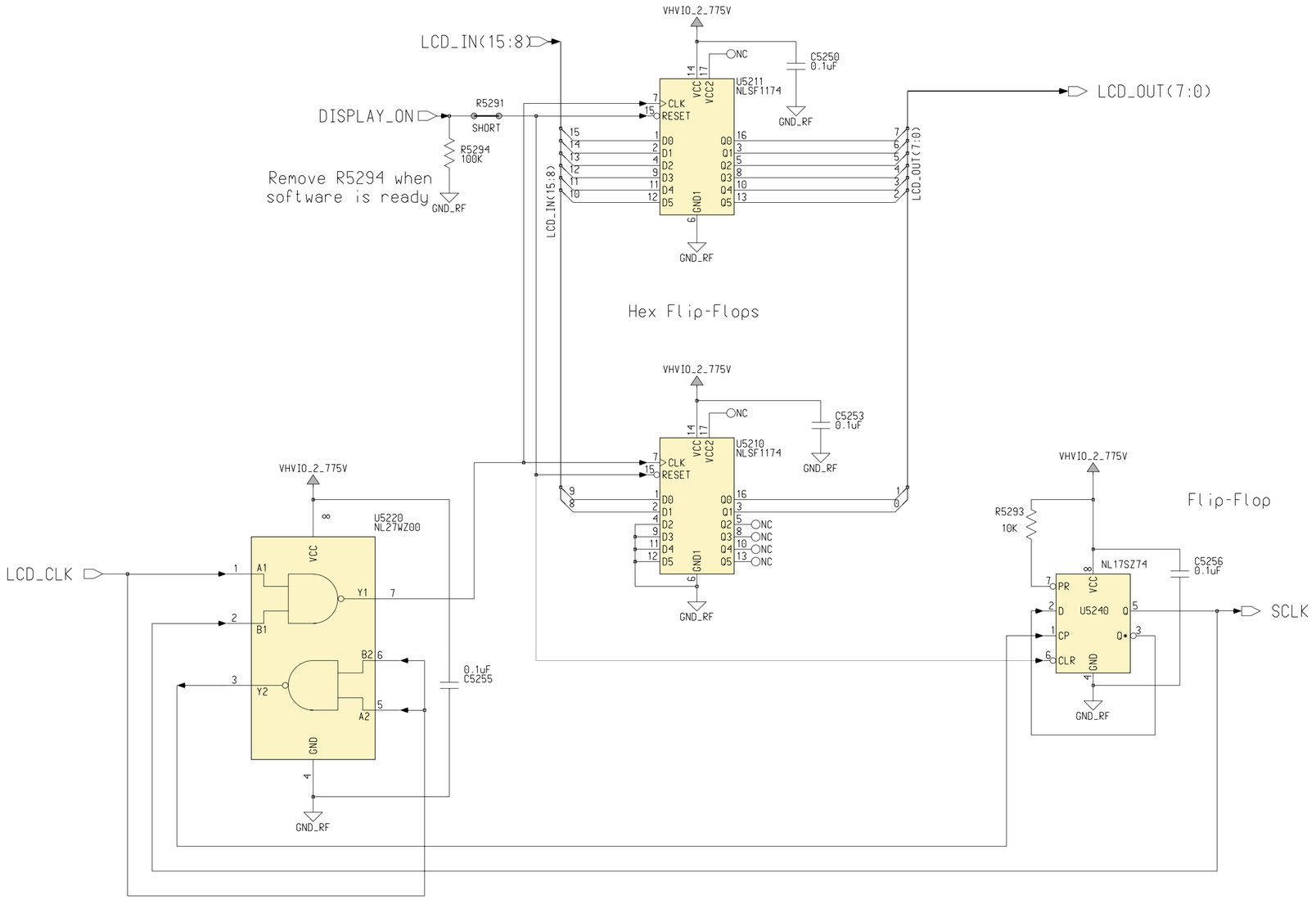
VOLTAGE — VR5101

Engineer: Ed Naddeo	MOTOROLA INC.		
Drawn by: Ed Naddeo	TITLE: TALON INTEGRATED Misc Connectors		Size: 11x21
R&D CHK:			
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV: 1	Drawing Number:	Page: 1 / OF: 1
Changed by: Ed Naddeo	Date: Monday, April 23, 2001		Time: 11:27:59 am

MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A

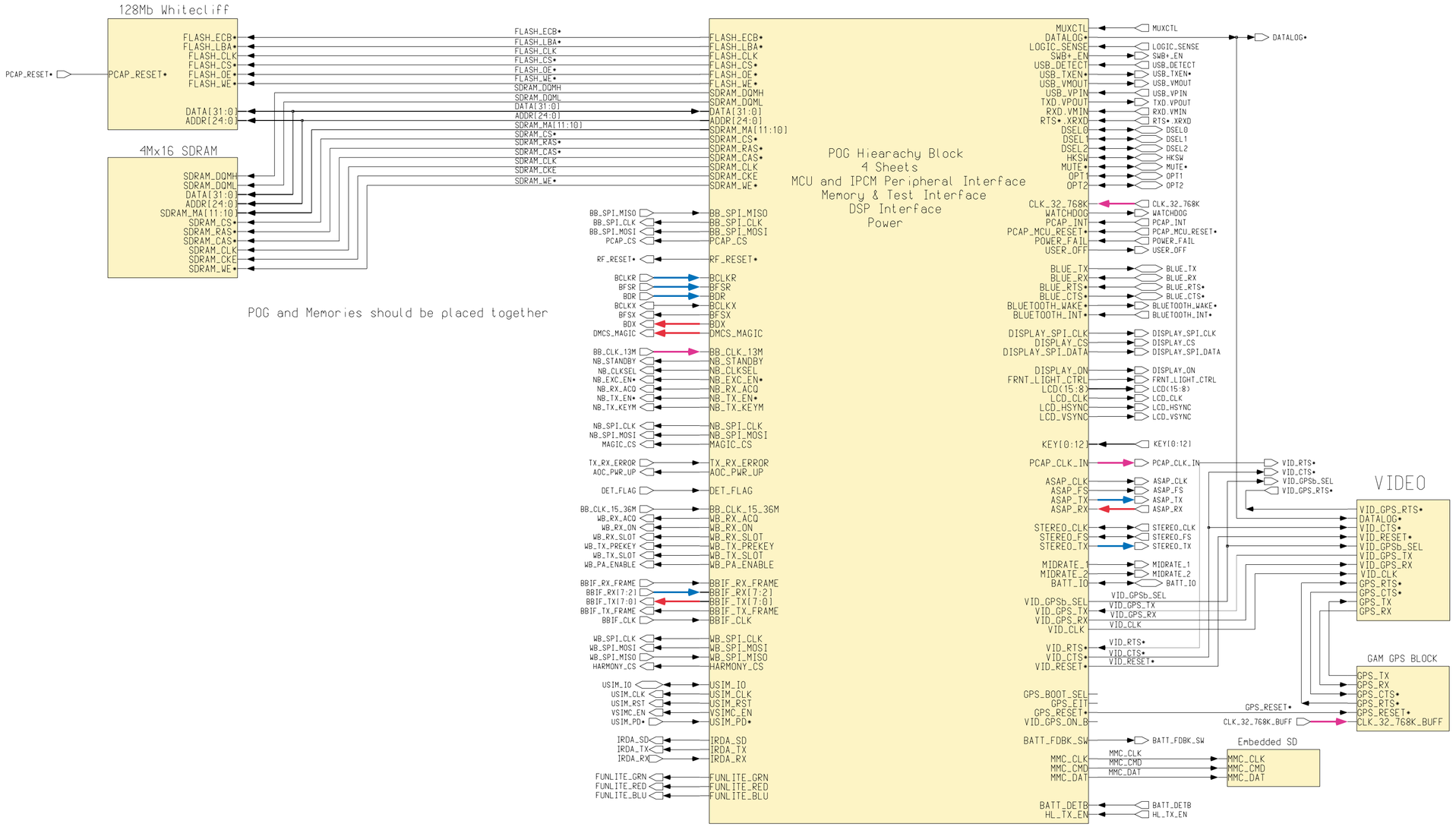
Engineer: Mike Lamfalusi	MOTOROLA INC.
Drawn by: Mike Lamfalusi	
R&D CHK:	TITLE: 65K_LOGIC — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: — Drawing Number: — Page: 1 — Of: 1
Changed by: w16808	Date: Thursday, May 2, 2002 — Time: 2:04:10 pm



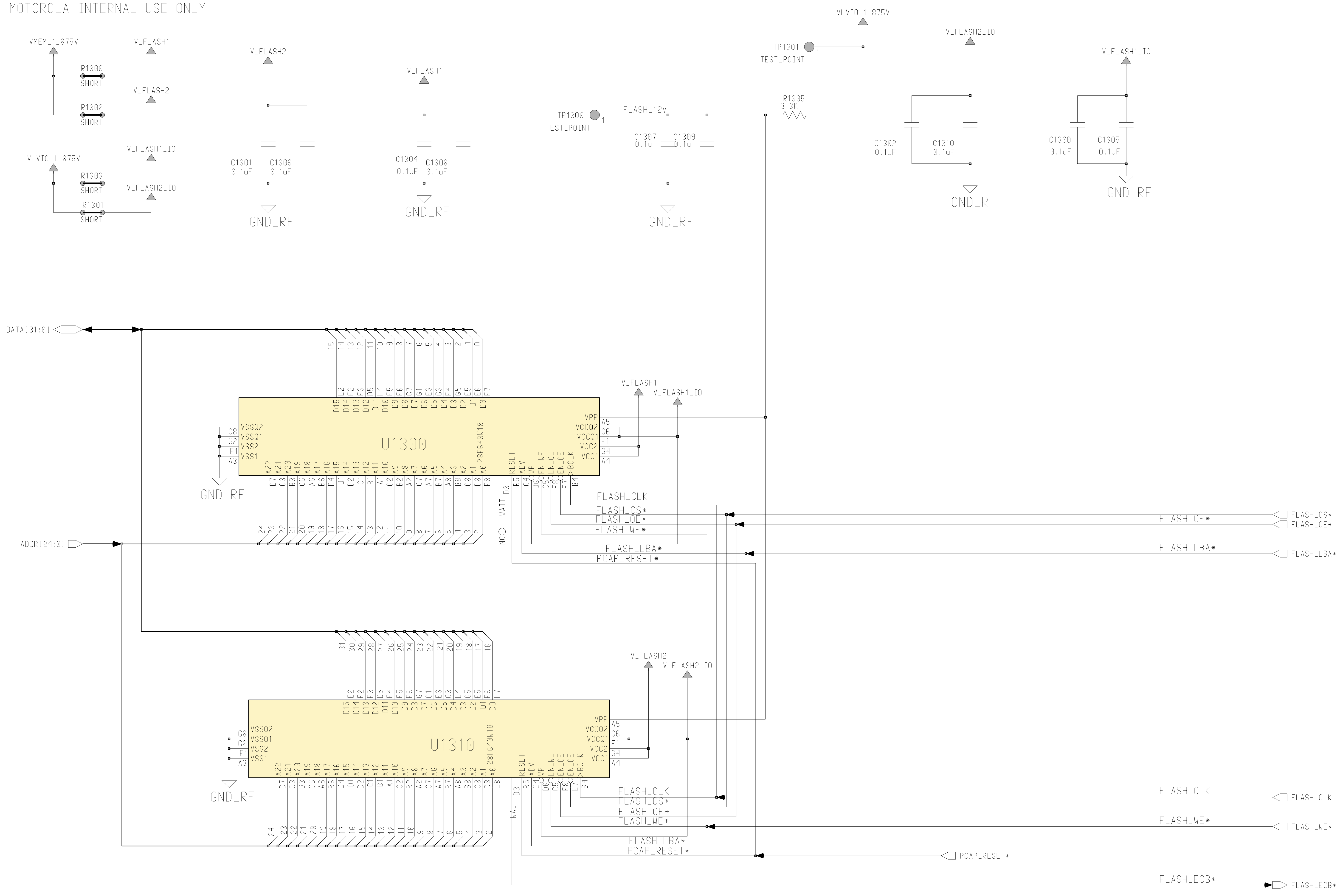
MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated Core Logic — Size: 11x21
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 1.0 — Drawing Number: 8488888x88 — Page: 1 — Of: 1
Changed by: wlen01	Date: Friday, March 1, 2002 — Time: 1:16:44 pm



MOTOROLA INTERNAL USE ONLY



4 1 3 A

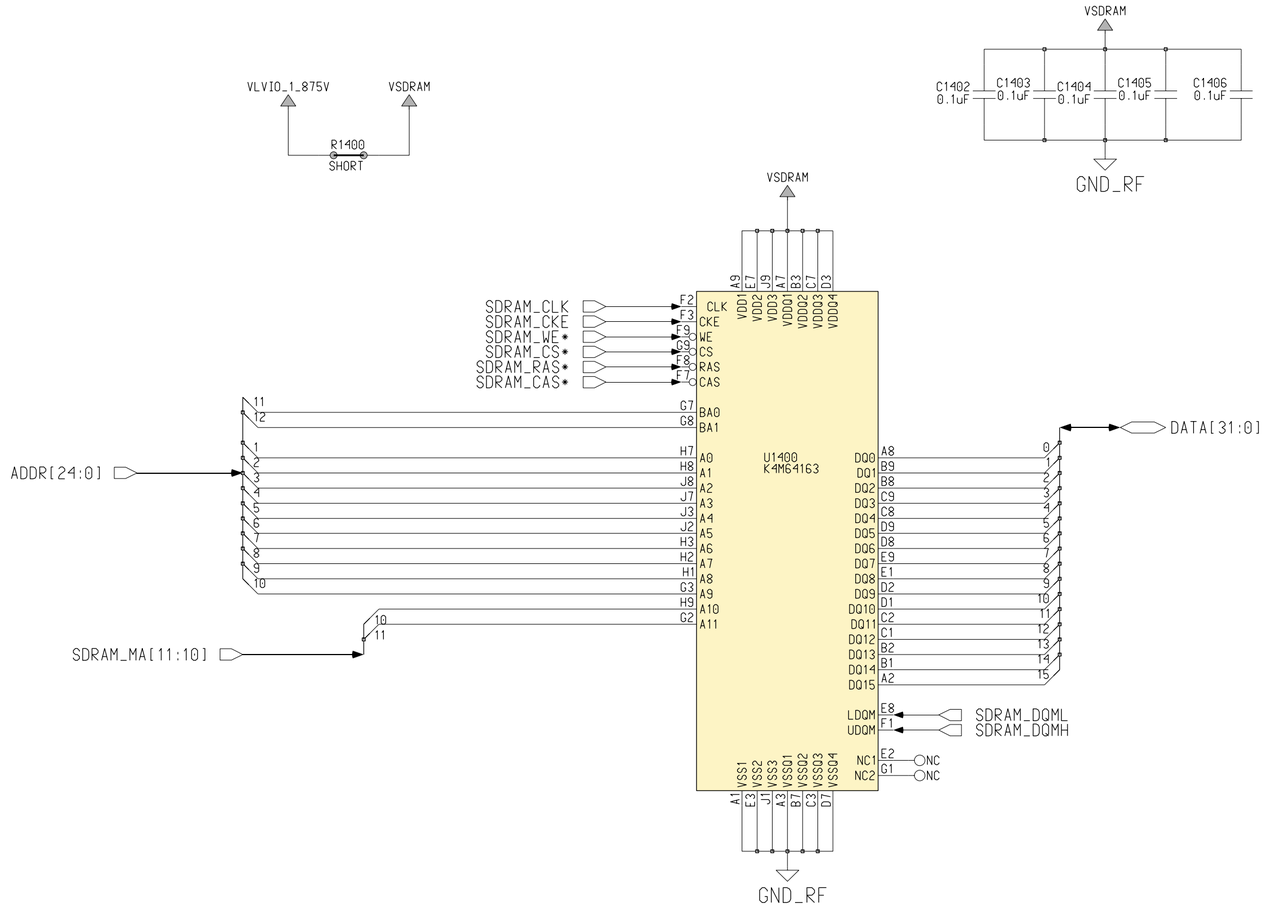
MOTOROLA INC.

Engineer: Ed Naddeo
Drawn by: Ed Naddeo
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
QA CHK:
TITLE: Talon Integrated Flash Memory
Size: 11x21
REV: 0.1
Drawing Number:
Page: 1
OF: 1
Changed by: Chris Pipe
Date: Monday, May 6, 2002
Time: 9:32:29 am

MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated 4Mx16 SDRAM — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 1.0 — Drawing Number: 84888888x88 — Page: 1 — Of: 1
Changed by: wlen01	Date: Friday, March 1, 2002 — Time: 3:37:06 pm



MOTOROLA CONFIDENTIAL PROPRIETARY

Oscillator and Memory Device Removed

Place VR parts as close as to J7900 and before any vias

L7500 is place holder for inductor

Sensor Connector
Molex 54722-0308

Place VR parts as close as to J7900 and before any vias

as close as to Falcon

as close as to J7900 pin 1

as close as to J7900 pin 40

Engineer: Jennifer Seymour	MOTOROLA INC.
Drawn by: Jennifer Seymour	
R&D CHK:	TITLE: TALON Integrated Falcon Camera
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: | Drawing Number: | Page: 1 | OF: 1
Changed by: Jennifer Seymour	Date: Friday, November 9, 2001 | Time: 10:21:35 am

MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A

Engineer: Danny Ng	MOTOROLA INC.
Drawn by: Danny Ng	
R&D CHK:	TITLE: GAM GPS BLOCK for E1000 — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 0.2 — Drawing Number: — Page: 1 — Of: 1
Changed by: W15660	Date: Monday, August 18, 2003 — Time: 3:17:11 pm

B+
U6005DNP
LP2988
INPUT
SHUTDOWN
SENSE
BYPASS
OUTPUT
ERROR
DELAY
GND
VGAM_2_775V
NC
C6055DNP 4.7uF
C6051DNP .01uF
C6050DNP .01uF
GND_RF

VLVIO_1_875V
VGAM_1_875V
R6001
VHVIO_2_775V
VGAM_2_775V
R6002

VGAM_1_875V
C6009 4.7uF
C6025 0.1uF
C6010 .01uF
C6012 1000pF
GND_RF

VGAM_2_775V
L6003 2.2uH
C6017 0.1uF
C6018 .01uF
C6056 4.7uF
VGAM_RF_2_775V
C6013 .01uF
C6014 0.1uF
C6015 1000pF
C6016 1000pF
GND_RF

LNA voltage supply will cut off when external active antenna is connected
L6000 22.0nH
C6000 1000pF
C6001 12pF
GND_RF

VGAM_RF_2_775V
VGAM_1_875V
VGAM_2_775V
VCC_LNA VCC_IF VCC_MIX VCC_PLL VCC_REF VCC_VCO
VDD_CORE_1 VDD_CORE_2 VDD_CORE_3 VDD_CORE_4 VDD_CORE_5 VDD_CORE_6
VDD_IO_1 VDD_IO_2 VDD_IO_3

TP6000
CLK_32_768K_BUFF
TP6001
REF_CLK
GPS_RESET•
R6063DNP 0
TP6002
R6028
NC
R6025
R6026
R6027
GND_RF

PHOENIX GAM
5109841C71
U6000
LOW_REF_CLK
MOD_MCLK
TCK
MCLK_EXT
REF_CLK
BREAKPT
DEGRQ
NRESET
NTRST
TDI
TEST
TMS
MOD_ARM
MOD_BOOT
VEE_LNA1 VEE_LNA2 VEE_IF VEE_MIX VEE_PLL VEE_REF VEE_VCO
VSS_CORE_1 VSS_CORE_2 VSS_CORE_3 VSS_CORE_4 VSS_CORE_5 VSS_CORE_6
VSS_IO_1 VSS_IO_2 VSS_IO_3
GND_ISO1 GND_ISO2
DBGACK TDO ADC3 ADC2 ADC1 ADC0 LNA_IN LNA_OUT EXT_NIRQ MISO_TXD0 MOSI_RXD0 NPSC_RXD1 ONEPPS SCK_TXD1 VGA_INP VGA_INM VTUNE
NC
R6062
SHORT
R6061
GPS_CLK_EN
R6060
SHORT
GND_RF

FLG001
Note: Place holder for epcos b9000 saw filter!
9189312N01
L6002 5.6nH 2409154M10
C6007 12pF
C6008 3pF
IN GND1 GND2 OUT1 OUT2
R6005 10pF
C6011DNP 2pF
GPS Antenna Pad
TP6005
C6019 2.7pF
L6010 56.0nH
TP6006
GND_RF

C6020 12pF

External GPS RF connector
SW6000
SWITCH
IN OUT GND1 GND2
C6004 12pF
SAW Filter
OUTPOS OUTNEG IN GND2 GND1
FL6000
SAW_1575_42MHZ
9180310L36
GND_RF

VGAM_RF_2_775V
L6001 33.0nH
C6005 12pF
C6006 18pF
GND_RF

VGAM_2_775V
R6055 100K
R6056 100K
R6020
R6021
R6022
R6023
GPS_TX
GPS_RX
GPS_CTS•
GPS_RTS•

L6004 2.2uH
Y6000
TCO-5871
26MHz
VCC
OUTPUT
V_CONT
GND
C6023 0.1uF
R6006 68
C6022 1000pF
C6021 10pF
GND_RF

R6000 2.2k
C6002 560pF
C6003 2200pF
GND_RF

TP6003

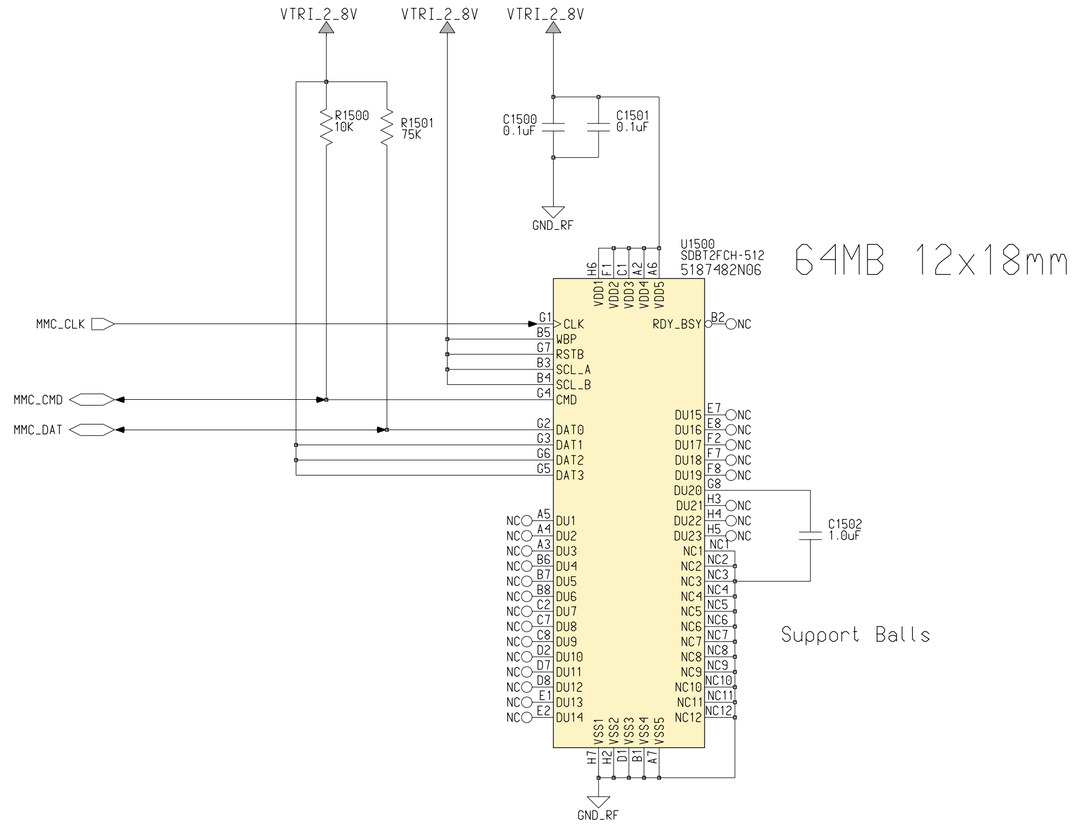
Q6000
S1 G1 D1 S2 G2 D2
R6031DNP 0
R6007DNP 1K
R6032
SHORT
R6008 100K
VGAM_RF_2_775V
GND_RF

TCXO CONTROL CKT

TCXO CONTROL LINES
ADC0: DNP R6032, PLACE R6031, R6007
ADC1: DNP R6031, R6007 PLACE R6032

4 1 3 A

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated Embedded SD Flash
DOC CTRL CHK:	Size: 11x17
MFG CTRL CHK:	
QA CHK:	REV: 1.0 / Drawing Number: 848888888x88 / Page: 1 / Of: 1
Changed by: Chris Pipe	Date: Friday, May 3, 2002 / Time: 1:25:03 pm



MOTOROLA CONFIDENTIAL PROPRIETARY

Accessory Connector
CE Connector (0987636K05)

J5000

BATT_FDBK
EXT_B+
D+ / TXD / TDO
D- / RXD / TDI
USB_PWR / IGN / SEND_END / RTS / RESET_IN
SWB+
HKSW / FM_DATA / CTS / DE_B
MUTE* / FS / DCD
DSEL2 / SCK / RI / TCK
DSEL1 / FM_CLOCK / SRDA / DTR / TMS
DSEL0 / FM_EN / STDA / DSR / TRST_B
OPTION1
OPTION2
AUDIO_OUT / 12V Flash / 8V JTAG
AUDIO_IN

RAW_BATT_FDBK
D+
D-
RAW_HKSW
RAW_MUTE*
RAW_DSEL2
RAW_DSEL1
RAW_DSEL0
RAW_OPT1
RAW_OPT2

Q5001 17F58
C5000 0.1uF
R5000 100K
R5001 47K
C5005 1.0uF
SWB+_EN
B+
RAW_EXT_B+
C5007 0.1uF
VR5005 16V 4813830C29
USB_PWR
U5001 CSPEMI-307
U5000 CSPEMI-306
D5000
BATT_FDBK
OPT2
OPT1
DSEL0
DSEL1
DSEL2
VS5001 16V 4813830C29
C5002 33pF
VS5002 6.8V 4809788E06
C5004 0.1uF
VHVIO_2_775V
VA_2_775V
R5050 47K 0662057N15
R5052 270K 0662057N33
C5050 0.1uF 2113743M24
LOGIC_SENSE
VID_RTS*
U5011 NC7SB3157
VID_GPS_RTS*
R5010DNP 0
U5010 NC7SB3157
VID_CTS*
HKSW
DATALOG*

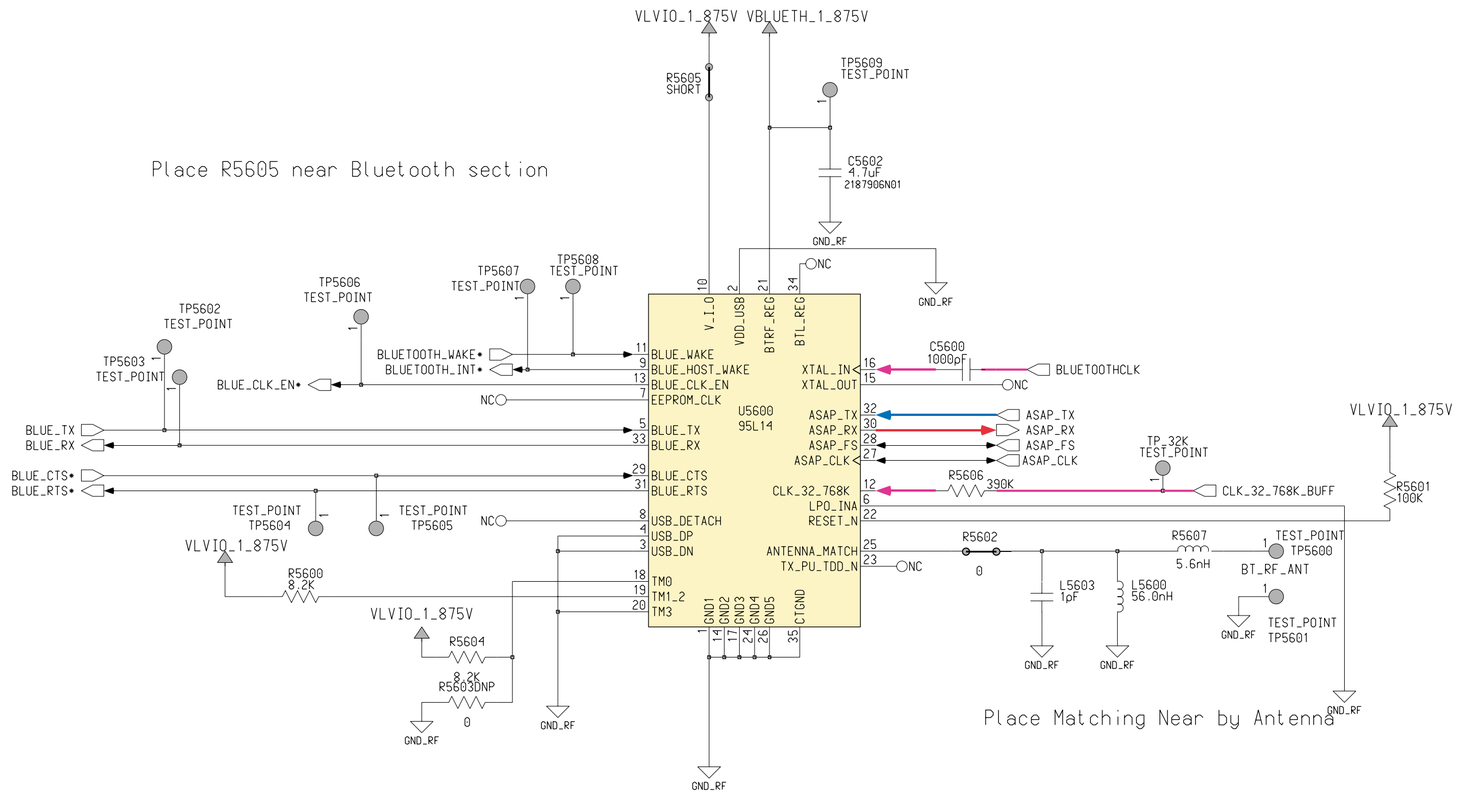
B0 - Normally Closed
B1 - Normally Open
S - Select
A - Common

Engineer: Jennifer Seymour	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: TALON Integrated CE Accessory Connector — Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: Drawing Number: Page: Of:
Changed by: Ed Naddeo	Date: 4/3/02 Time:

MOTOROLA CONFIDENTIAL PROPRIETARY

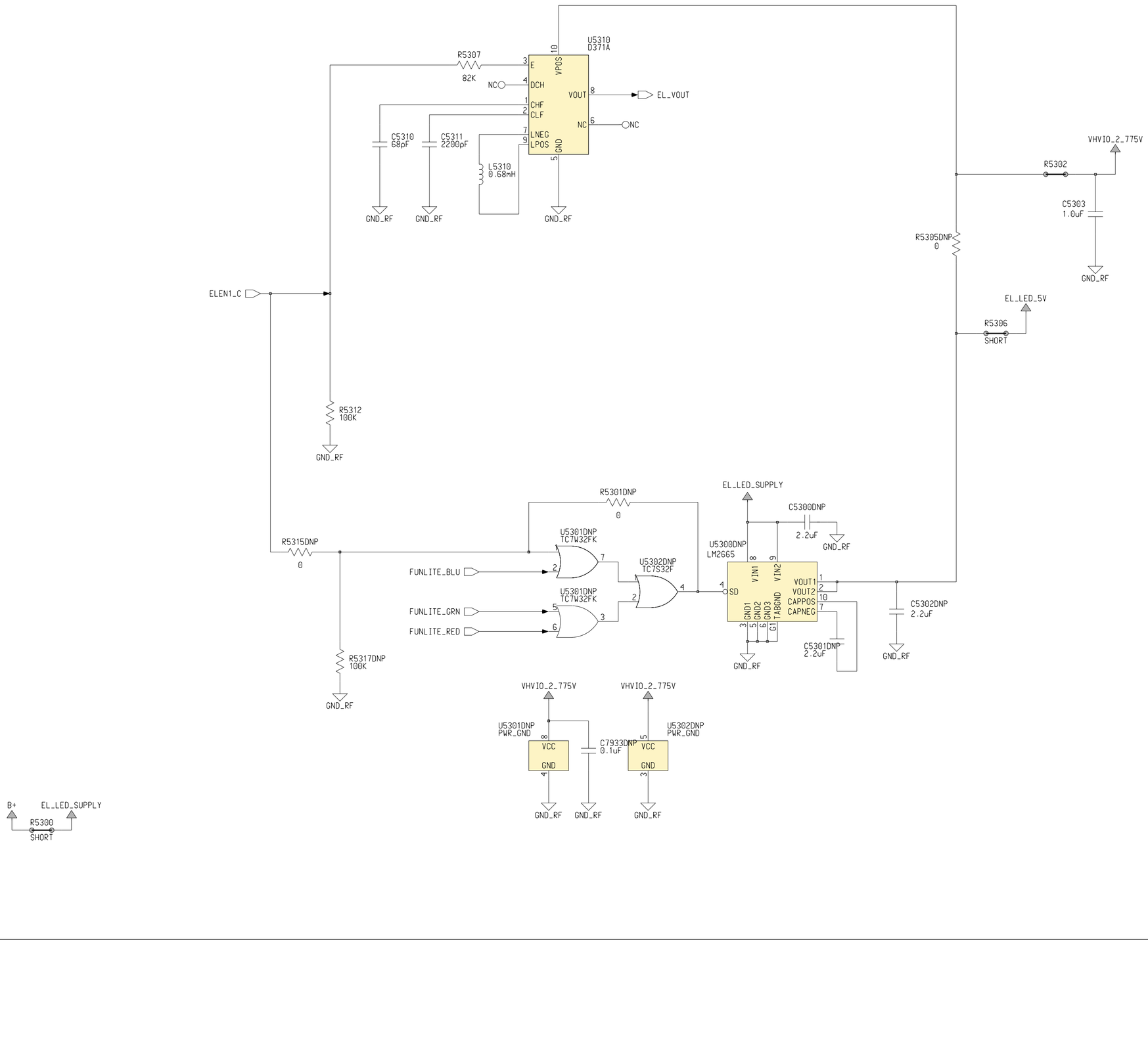
Date : July 23, 2001

Engineer: Dave Stubbs	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: TALON Integrated Bluetooth — Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: Drawing Number: Page: OF:
Changed by: Dave Suarez	Date: February 24, 2003 — Time:



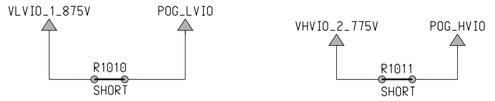
MOTOROLA CONFIDENTIAL PROPRIETARY

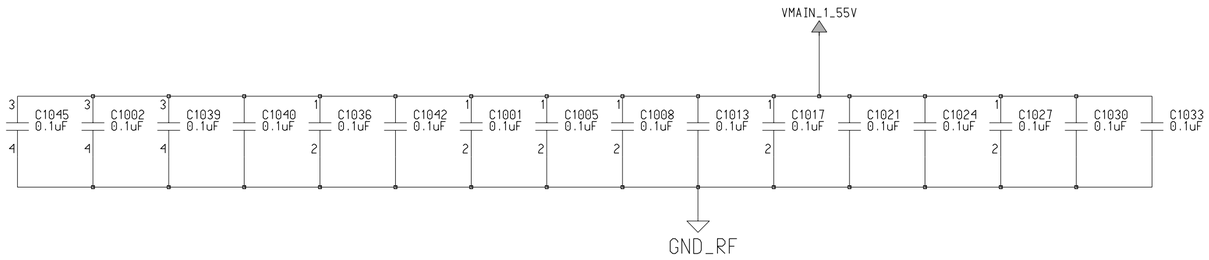
Engineer:	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: Funlites and EL — Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: — Drawing Number: — Page: — OF:
Changed by:	Date: — Time:

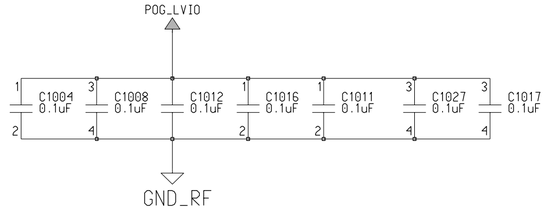


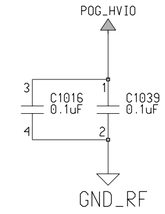
MOTOROLA CONFIDENTIAL PROPRIETARY

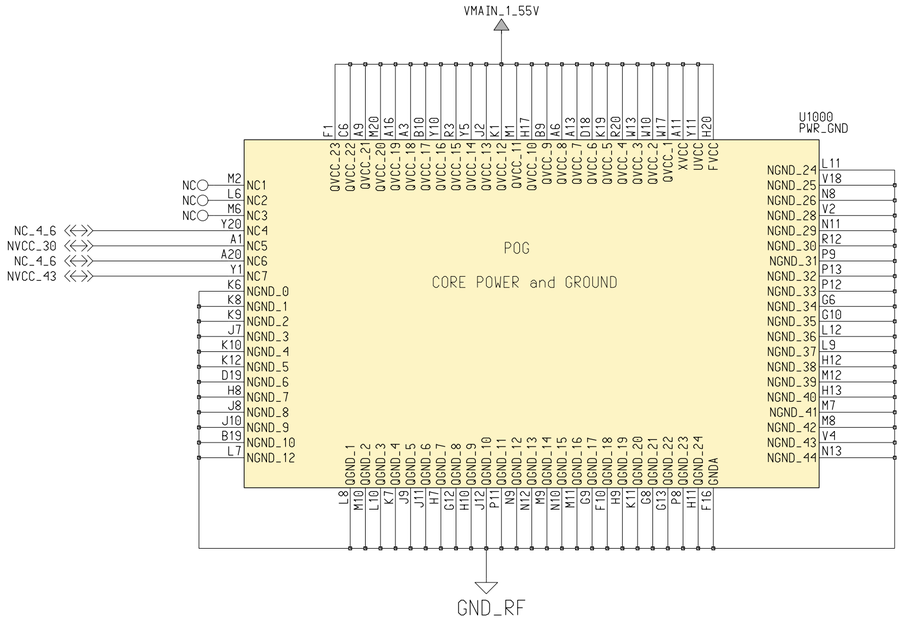
4 1 3 A







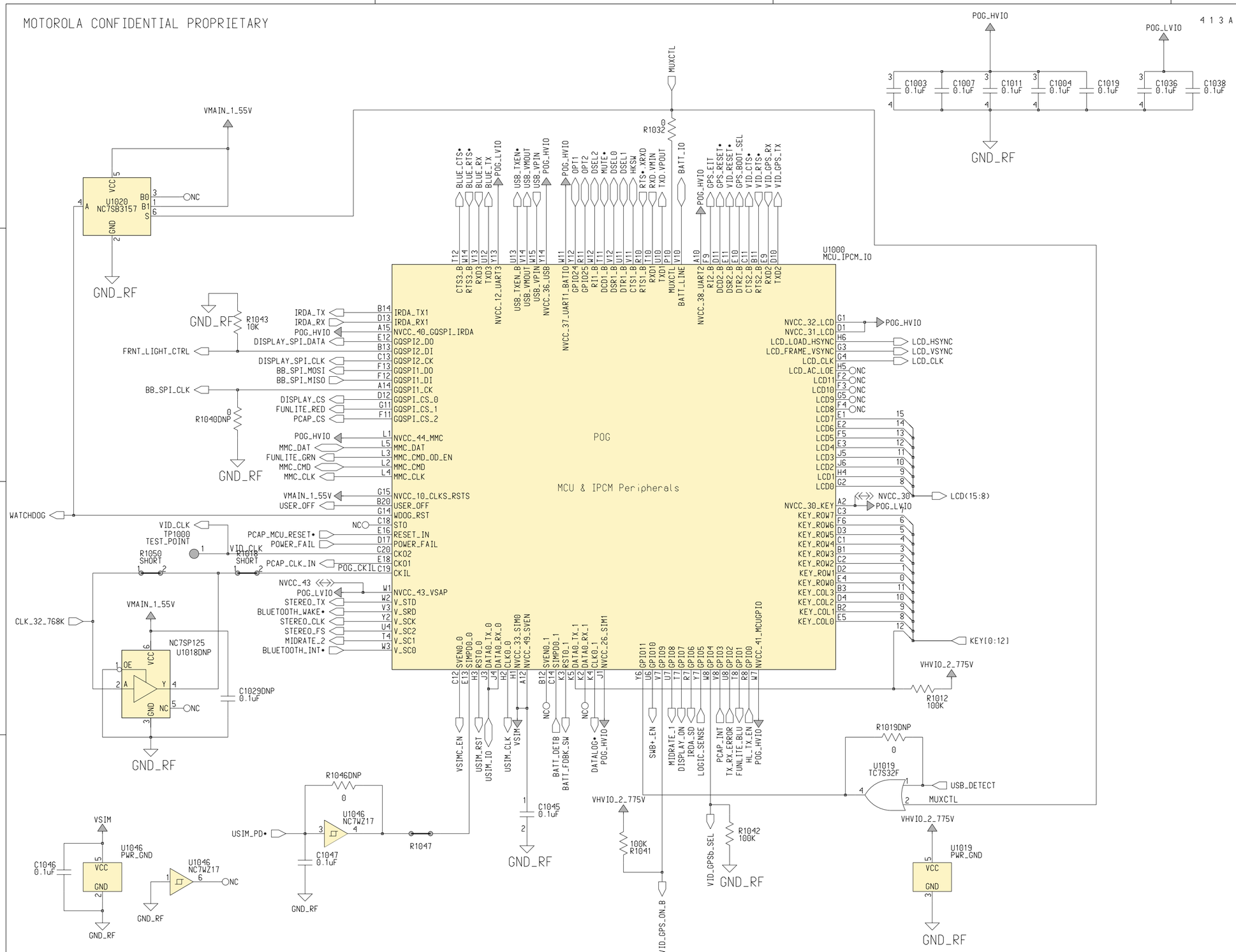




Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated POG Power
DOC CTRL CHK:	Size: 11x17
MFG CTRL CHK:	
QA CHK:	REV: 1 / Drawing Number: 84888888x88 / Page: 1 / OF: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002 / Time: 2:56:17 pm

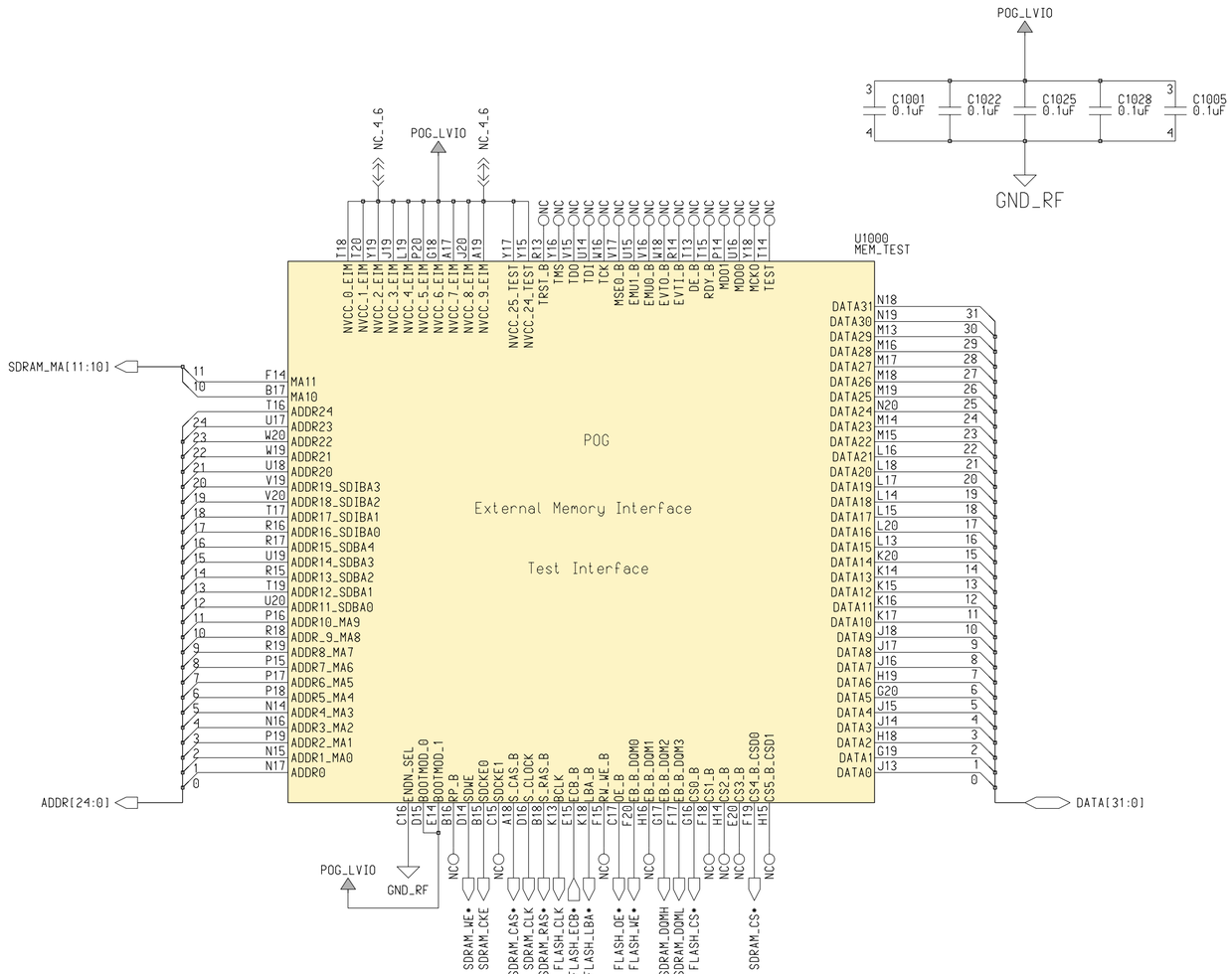
4 1 3 A

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: TALON Integrated POG Accessories Interface
DOC CTRL CHK:	Size: 11x17
MFG CTRL CHK:	
QA CHK:	REV: 1.0 | Drawing Number: 8488888x88 | Page: 2 | Of: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002 | Time: 4:39:04 pm



MOTOROLA CONFIDENTIAL PROPRIETARY

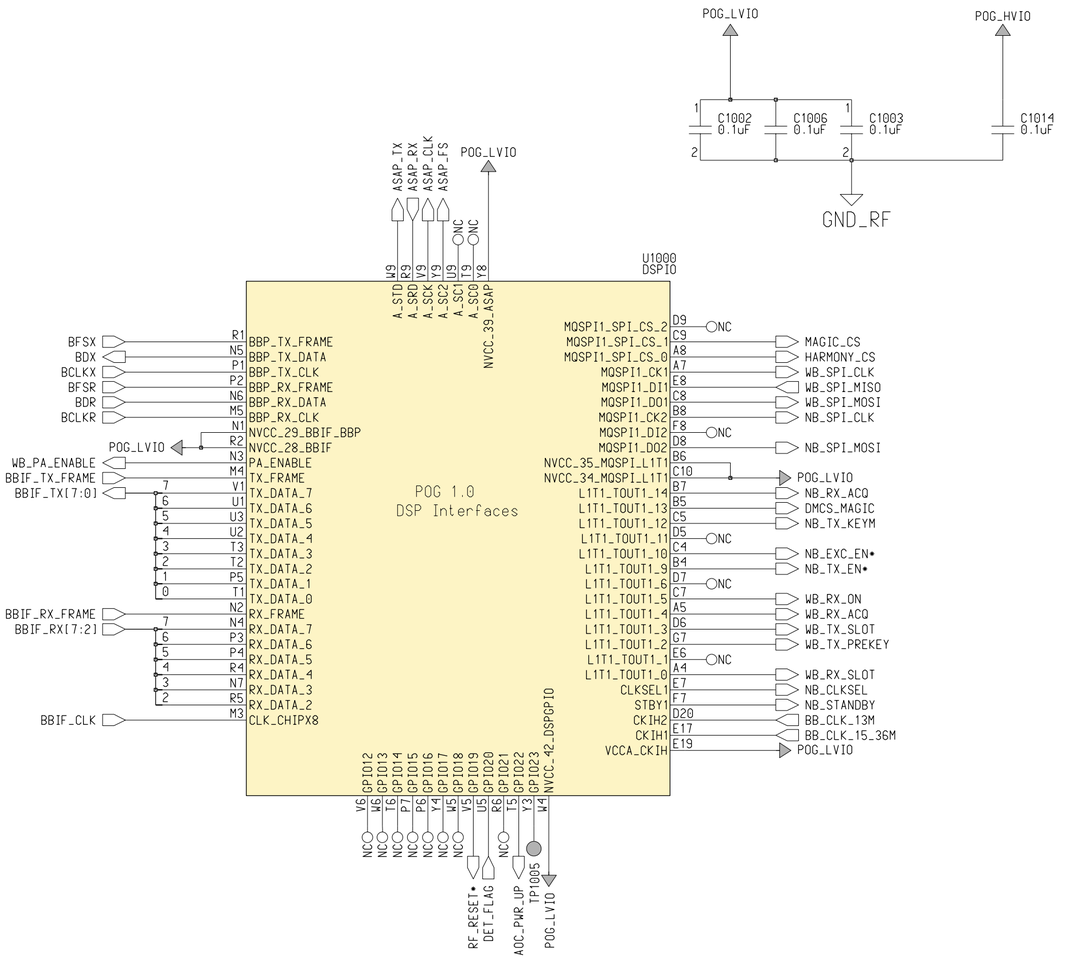
4 1 3 A



Engineer: Ed Naddeo	MOTOROLA INC.		
Drawn by: Ed Naddeo			
R&D CHK:	TITLE: Talon Integrated POG Memory and Test Interface		Size: 11x17
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV: 1.0	Drawing Number: 8488888x88	Page: 3 / Of: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002		Time: 6:15:09 pm

MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A



Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated POG DSP Interface
DOC CTRL CHK:	Size: 11x17
MFG CTRL CHK:	
QA CHK:	REV: 1.0 | Drawing Number: 8488888x88 | Page: 4 | Of: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002 | Time: 6:16:44 pm

Stereo Headset Speakers(4300-4399)

Melody Ringer/Loudspeaker(4200-4299)

Earpiece/Handset Speaker(4000-4099)

Headset Mic and Detection (4300-4399)

Internal Microphone (4100-4199)

Overvoltage Protection

Battery Charge Circuit

Digital Audio Ports

Enumeration Fix

PCAP SYMBOL

U3000

VBUCK_2_25V

VBOOST_5_5V

VMAIN_1_55V

VMEM_1_875V

VA_2_775V

VLVIO_1_875V

VRF_REF_1_875V

VGPS_RF_2_775V

VRF_TX_2_775V

VRF_REF_2_775V

VRF_DIG_1_875V

VBLUETH_1_875V

VRF_REF_2_475V

VRF_HV_5V

VHVIO_2_775V

VRF_RX_2_775V

VTRI_2_8V

V_FALC_2_8

VCAM_3_0V

V_FALC_1_8V

Plot Scale = 0.8

Engineer: Bok Koh & Chuck Farago	MOTOROLA INC.			
Drawn by: John Kerr, Bok K. & Chuck F.				
R&D CHK:	TITLE: Talon Integrated Power and Audio			Size:
DOC CTRL CHK:				
MFG CTRL CHK:				
QA CHK:	REV:	Drawing Number:	Page:	Of:
Changed by: Amanda H. & David D.	Date: 5/3/02			Time: 1:36:56 pm