MSM6550™/MSM6150™ Mobile Station Modem™

Device Specification

80-V7196-1 Rev. H

March 18, 2005

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Revision history

Revision	Date	Description
A	March 2004	Initial release
B	March 26, 2004	Updated Table 2-2.
C	April 2, 2004	Updated Table 2-2, Table 2-4, Table 3-4, and Table 3-5.
D	June 2004	Updated following tables: Table 2-2, Table 2-4, Table 3-4, Table 3-5, Table 3-11, Table 3-12, Table 3-13, Table 3-14, Table 3-18, Table 3-21, and Table 3-22. Updated following figures: Figure 3-2, Figure 3-12, Figure 3-13, Figure 3-14, Figure 3-18, Figure 3-22, Figure 3-39, and Figure 3-41.
E	July 2004	Updated Table 2-2 and Table 3-2. Updated Figure 4-4 and Figure 4-5. Updated Figure 5-1, Figure 5-2, Figure 5-3, and Figure 5-4.
F	January 2005	Updated Figure 1-1 and Figure 1-2. Updated Table 2-2: provided default pull information on pins, added alternate function names. Updated Table 3-4 and Table 3-5: DC Characteristics Updated Section 3.1.6, Power sequencing Updated Sections 3.3 and 3.4: provided AC timing data for EBI1 and EBI2 sections, modified CAMIF timing spec Updated Table 7-1 and Table 7-2: provided Qual data
G	March 2005	Update Table 2-2: additional default pull information on pins Updated Table 3-1: maximum rating data Updated Table 3-6: power consumption data Updated Table 3-7: capacitive loading data Updated Figure 3-18 through Figure 3-25: burst mode timing diagrams Updated Section 3.3.6.2: camera interface timing
H	March 2005	Deleted text in Section 3.1.5.1 Updated Table 3-14

Preface

About this technical manual

This manual provides hardware interface and specifications for the MSM6550/MSM6150 Mobile Station Modem. The manual is divided into the following chapters:

Chapter 1: Overview	This chapter introduces users to the MSM6550/MSM6150 device basic features and functions.
Chapter 2: Pin Descriptions	This chapter lists each MSM6550/MSM6150 pin and its function within the device. The pinout for the 409-ball CSP package is listed by functional grouping.
Chapter 3: Electrical Specifications	This chapter specifies the recommended operating conditions, DC voltage characteristics, I/O timing, and power estimations for the MSM6550/MSM6150 device. Timing diagrams are also included.
Chapter 4: Package Specifications	This chapter shows the part marking and full page drawings of the 409-ball CSP package outline and land pattern.
Chapter 5: Package/Tape and Reel	This chapter details the packaging of the MSM tape and reel.
Chapter 6: Part Mounting Specification	This chapter provides specifications for mounting parts and conditions for storing package.
Chapter 7: Part Reliability Test Specification	This chapter lists the stress tests done on the MSM6550/MSM6150 device and the sample descriptions.

Usage conventions

The following table defines terms commonly used throughout this manual.

Usage conventions

Term	Definition
AAGC	Audio Automatic Gain Control
ACH	Access Channel
ADC	Analog-to-digital converter
AEC	Acoustic Echo Cancellation
AFLT	Advanced Forward Link Trilateration
AGC	Automatic Gain Control
AMPS	Advanced Mobile Phone System (analog IS-95)
APICH	Dedicated Auxiliary Pilot Channel

Term	Definition
ASIC	Application Specific Integrated Circuit
ATDPICH	Auxiliary Transmit Diversity Pilot Channel
BCCH	Broadcast Control Channel
BER	Bit error rate
BPF	Bandpass Filter
Bps	Bits per second
CACH	Common Assignment Channel
CAGC	CDMA AGC
CCCH	Common Control Channel
CDMA	Code Division Multiple Access
CELP	Code Excited Linear Prediction
CODEC	Coder-Decoder
CPCCH	Common Power Control Channel
CR	Command Register
CSM	Cell Site Modem
CRC	Cyclic Redundancy Code
DBR	Data Burst Randomization
DCCH	Dedicated Control Channel
DFM	Digital Frequency Modulation
DTMF	Dual-Tone Multiple-Frequency
EACH	Enhanced Access Channel
ESEC	Ear Seal Echo Cancellation
FBGA	Fine-pitch plastic Ball Grid Array
FCH	Fundamental Channel
FIFO	First-In First-Out
FIR	Finite Impulse Response
FM	Frequency Modulation
FOCC	Forward Control Channel
FVC	Forward Voice Channel
GPIO	General-purpose Input/Output
HEC	Headset Echo Cancellation
HPF	Highpass Filter
ICD	In-Circuit Debugger
IF	Intermediate Frequency
IR	Instruction Register
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1–1990)
kbps	Kilobits per Second
LCD	Liquid Crystal Display
LNA	Low Noise Amplifier
LPF	Lowpass Filter

Term	Definition
LSByte or LSBit	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MSByte or MSBit	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
MSM™	Mobile Station Modem. Trademarked by QUALCOMM.
NMI	Non-maskable Interrupt
NS	Noise Suppression
PA	Power Amplifier
PCM	Pulse Coded Modulation
PCS	Personal Communications Service
PCH	Paging Channel
PDM	Pulse Density Modulation
PICH	Pilot Channel
PN	Pseudo-Random Noise
QCELP	QUALCOMM Code Excited Linear Prediction
QPCH	Quick Paging Channel
RC	Resistance-Capacitance
RF	Radio Frequency
RRM	Reduced Rate Mode
RSSI	Receive Strength Signal Indicator
Rx	Receive
SAT	Supervisory Audio Tone
SCCH	Supplemental Code Channel
SCH	Supplemental Channel
SNR	Signal-to-Noise Ratio
Sps	Symbols Per Second (or Samples Per Second)
SER	Symbol Error Rate
SYNCH	Sync Channel
TAP	Test Access Port
TCXO	Temperature-Compensated Crystal Oscillator
TDPICH	Transmit Diversity Pilot Channel
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
UHF	Ultra High Frequency
WBD	Wide Band Data
ZIF	Zero Intermediate Frequency

Special marks

The following table defines special marks used in this manual.

Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, GPIO[7:0] may indicate a range that is 8 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of "_N" indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term "binary" enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of the page (as shown here) indicates a change or revision since the last release of the document.

1 Overview

1.1 Scope and intended audience

This device specification documents electrical specifications, packaging, and board reliability tests for the MSM6550/MSM6150 409-ball CSP package. The specifications are compiled here for the convenience of company purchasing or procurement departments.

For more information on 409-ball CSP package specifications and manufacturing considerations, refer to BGA/CSP Package User Guide (80-V2560-1).

1.2 Application description

The global expansion of 3G CDMA2000® 1X and 1xEV-DO networks has extended the availability of high-speed, wireless data access. With increased accessibility came increased demand for wireless devices that function as camera, camcorder, personal video player, MP3 audio player, gaming console and phone. To efficiently support next-generation data speeds and functionality, wireless devices must integrate applications processors with high-performance modems.

To address this growing opportunity, QUALCOMM CDMA Technologies (QCT) developed the MSM6550/MSM6150 Mobile Station Modem™ (MSM™) chipset and system software solution. The MSM6550/MSM6150 solution integrates powerful applications processors into QUALCOMM's market-proven wireless modem, offering increased processing capacity combined with lower power consumption. With the MSM6550/MSM6150 chipset solution, handset manufacturers can design sleek wireless devices that boast the industry's most advanced image quality and resolution to provide enhanced 3D animation, gaming, streaming video, videoconferencing and more.

QUALCOMM's MSM6550/MSM6150 solution offers significantly increased processing speeds, higher resolution video and graphics, and extended usage times for gaming and video applications — all on a single chip. This single-chip solution eliminates the need for a separate applications processor, decreasing parts count, reducing bill-of material (BOM) costs and supporting the development of ultra compact devices.

Key distinction between MSM6550 & MSM6150 chipsets:

MSM6550 = MSM6150 features plus 1xEV-DO and GSM-GPRS

MSM6150 = 1X with Rx Diversity and Simultaneous-GPS

Forward compatibility with other chipsets:

MSM6550/MSM6150 devices are intended to be pin compatible with MSM6700™ and MSM6800™ devices. The end of Table 2-2 addresses the minor pinout differences between the MSM6550/MSM6150 chipsets and future chipsets.

MSM6550/MSM6150 chipset solution benefits

- Integrates dedicated hardware cores into the MSM which eliminates the need for multimedia co-processors — offers superior image quality and resolution for mobile devices and extended application time
- Enables impressive, user-compelling 3D graphics, multimedia, animation and video
- Provides longer run time for mobile devices over other industry solutions that use companion processors
- Provides superior quality video and graphics with quarter video graphics array (QVGA) resolution, a fourfold improvement over quarter common intermediate format (QCIF)
- Offers a higher degree of integration (digital and analog functions on a single chip) and dedicated hardware cores, which decrease power consumption while increasing power and quality
- Eliminates the need for intermediate frequency (IF) components, decreasing printed-circuit-board area and reducing time-to market development and BOM costs
- Enables a wide variety of location-based services and applications, including points of interest, personal navigation and friend finder
- Single platform provides dedicated support for all market leading codecs and other multimedia formats to support carrier deployments around the world

MSM6550/MSM6150 device description

The MSM6550/MSM6150 device integrates the ARM926EJ-S™ processor, offering the ARM® Jazelle™ Java® hardware accelerator; two low-power, high-performance QDSP4000™ digital signal processor (DSP) cores; hardware acceleration for video, imaging and graphics; and a wideband stereo codec to support enhanced digital audio applications. The hardware acceleration eliminates the need for the multimedia companion processors normally required for video and audio-based applications that support MP3 music files, a MIDI synthesizer, video and still image record and playback, and 2D/3D graphics functions. By removing the need for costly applications co-processors and memory subsystems, the MSM6550/MSM6150 solution reduces bill-of-material costs and increases standby and talk times. The MSM6550/MSM6150 solution integrates both digital and analog functions into a single chip.

The MSM6550/MSM6150 system solution consists of the MSM6550/MSM6150 baseband processor, complete with CDMA2000 1xRTT/CDMA2000 1xEV-DO/GSM/GPRS protocol stack and multimedia system software. The MSM6550/MSM6150 interfaces with a variety of radio frequency (RF) system solutions supporting quad-mode (RFL6000™, RFR6000™, RFT6100™) and cost optimized cellular only (RFR6120™, RFR6125™, RFT6120™) and multimode (RTR6300™) terminals. The baseband and RF chipsets are supported by QUALCOMM's powerOne™ series PM6650™ power management device.

The 3G CDMA2000 MSM6150(1X) / MSM6550 (1xEV-DO/GSM/GPRS) chipset and system software features radioOne® direct conversion architecture and incorporates a low-power, high

performance RISC microprocessor core featuring the ARM926EJ-S CPU and Jazelle accelerator circuit for advanced Java applications from ARM Limited. The MSM6550/MSM6150 solution integrates two low-power, high performance QDSP4000 digital signal processor (DSP) cores. Use of the ARM926EJ-S CPU and QDSP4000 DSP eliminates the need for the multimedia companion processor(s) normally required for video and audio-based applications that support MP3 music files, a MIDI synthesizer, video and still image record and playback, and 2D/3D graphics functions.

QCT provides a complete software suite, dual mode subscriber software (DMSS), for building handsets around the MSM6550/MSM6150 chipset. DMSS software is designed to run on a subscriber unit reference (SURF) phone platform, an optional development platform optimized to assist in evaluating, testing and debugging DMSS software. The MSM6550/MSM6150 device is offered in a 409-ball, 0.5 mm pitch, lead-free chip scale package (CSP) production package.

The Launchpad™ suite of technologies

The Launchpad™ suite of applications technologies offers wireless operators and manufacturers a cost-effective, scalable and timely solution for providing advanced wireless data services. This seamlessly integrated solution enables advanced next-generation applications and services that incorporate multimedia, position location, connectivity, customized user interface and storage capabilities. Launchpad features are available for each QUALCOMM chipset, closely matching the specific functionality and cost-target objectives agreed upon in joint product planning with manufacturers and wireless service operators worldwide.

The MSM6550/MSM6150 solution supports the advanced feature set of QUALCOMM's Launchpad suite of technologies, including streaming video and audio; still image and video encoding and decoding; 2D and 3D graphics acceleration; Java acceleration and a megapixel camera interface. The MSM6550/MSM6150 solution also integrates gpsOne® functionality, featuring enhancements by SnapTrack, Inc., to support assisted and standalone GPS — enabling a wide variety of location-based services and applications, including points of interest, personal navigation and friend finder.

Integrated into the MSM6550/MSM6150 solution are Bluetooth® wireless connectivity and USB On-The-Go (OTG) host controller functionality, allowing seamless communication directly with printers, digital cameras, keyboards and other accessories.

gpsOne technology (CDMA mode only)

gpsOne technology merges global positioning system (GPS) satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs under the most challenging conditions and provides a platform for both location-based applications and FCC compliance.

When a request for position location is issued, the handset takes pilot phase measurements and requests assistance from the PDE. The PDE sends the assistance information to the handset. The handset/mobile unit measures the GPS pseudoranges and pilot phase (again) and provides data to the PDE. The PDE then calculates position location and returns results to the requesting entity.

This hybrid method uses both GPS satellite pseudoranges and pilot offsets. The strengths of this solution are:

- High-sensitivity solution works in all terrain, indoors, outdoors, urban, rural
- High availability is enabled by using both satellite and pilot information

Hence, while network solutions do poorly in rural areas and areas of poor cell geometry/density, and while pure GPS solutions do not work indoors, the QUALCOMM gpsOne solution combines information from both network and satellites to calculate a fix under all conditions. This is further enabled using assistance provided by the PDE that enhances the sensitivity of the gpsOne receiver by approximately 20 to 30 dB.

As opposed to network solutions that require equipment at each cell site, the gpsOne solution packs a complete GPS receiver into every MSM6550/MSM6150 chipset. This means that each handset is capable of position location without requiring expensive cell site equipment. This solution not only meets the FCC E911 mandate under the most challenging conditions, but also provides a ubiquitous platform for location-based applications. gpsOne and radioOne technologies will enable consumer-priced, position-capable handsets.

radioOne technology

The MSM6550/MSM6150 device interfaces directly with QCT's new radioOne RF ASICs. radioOne is a revolutionary technology for CDMA transceivers that uses zero intermediate frequency (ZIF), or direct conversion, architecture for the wireless handset market. This direct conversion eliminates the need for large IF surface acoustic wave (SAW) filters and additional IF circuitry, which significantly reduces the handset BOM parts count, facilitating multiband and multimode handsets that can be produced in smaller form factors. radioOne technology also incorporates the frequency synthesis and passive elements used in converting baseband signals to and from RF. A single external local oscillator is used for the CDMA receiver, which will provide the capabilities needed to operate on systems around the world and will simplify the procurement of parts.

BREW™ solution

The MSM6550/MSM6150 includes support for QUALCOMM's BREW solution. BREW is a complete product and business system for the development and over-the-air deployment of data services on wireless devices. The BREW solution provides the necessary tools and value added services to developers, device manufacturers and wireless operators for application development and distribution, device configuration, and billing and payment.

1.3 MSM6550/MSM6150 device features

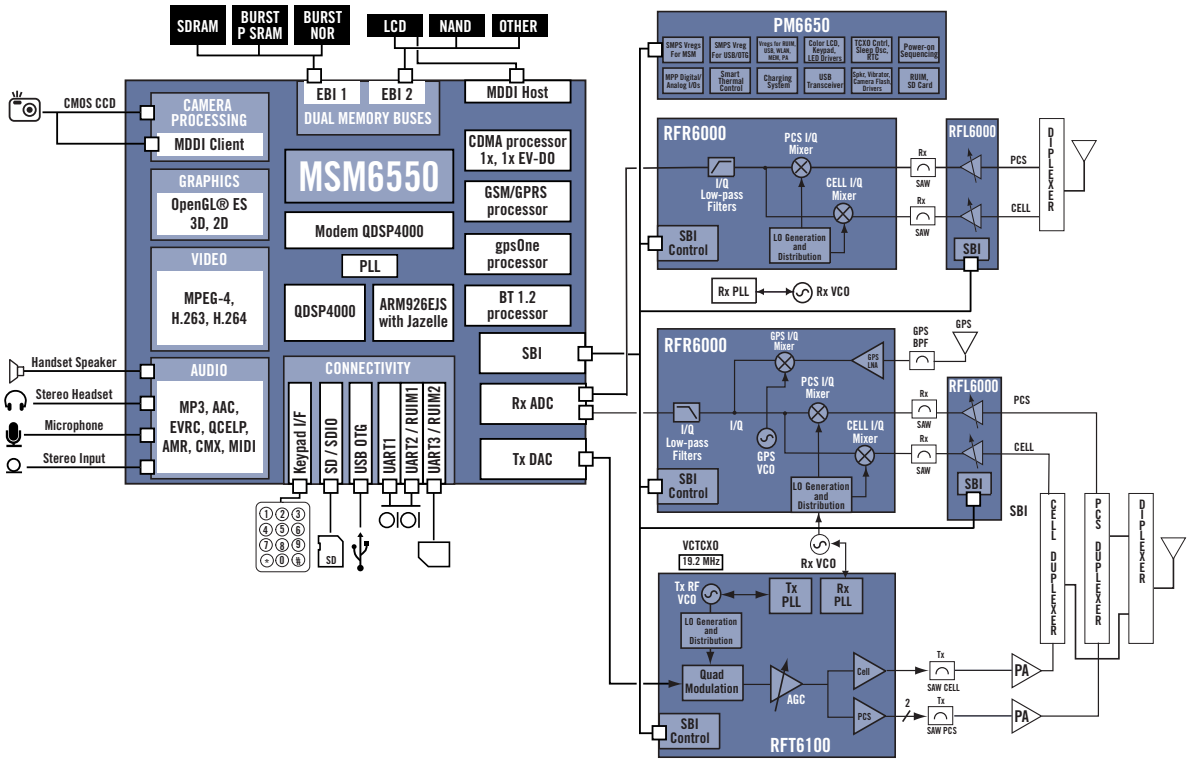

Figure 1-1 MSM6550 device functional diagram

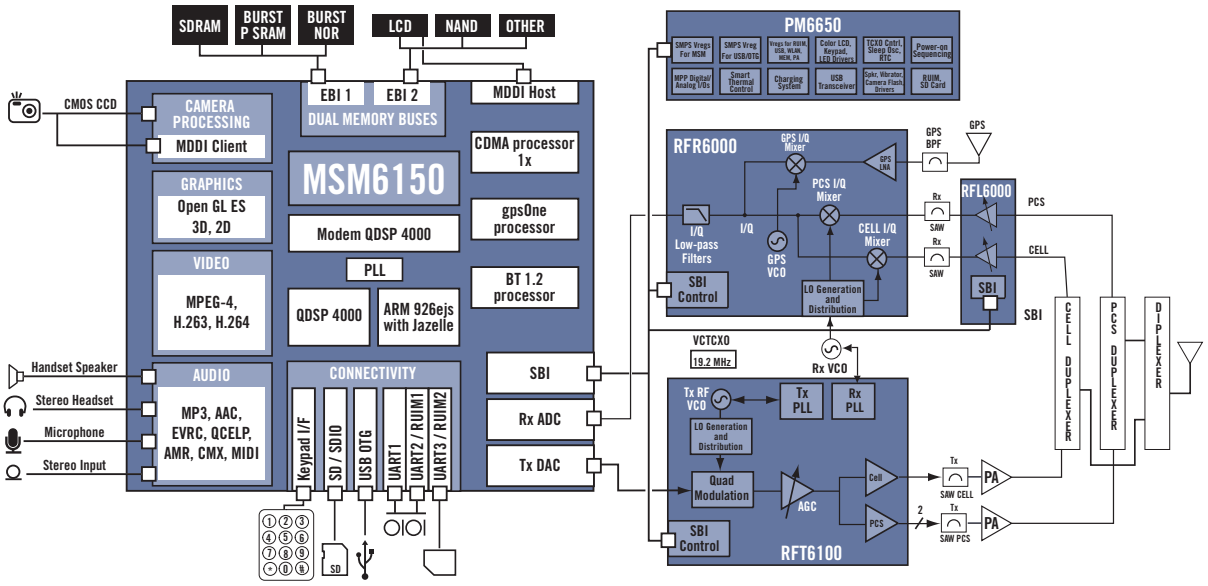

Figure 1-2 MSM6150 device functional design

1.3.1 MSM6550/MSM6150 device general features

- MSM6550/MSM6150 system solution consists of the MSM6550/MSM6150, RFL6000, RFR6000, RFT6100 (or RTR6300 for MSM6550 only), PM6650, DMSS system software and SURF6550™/ SURF6150™
- 1xEV-DO (**MSM6550 only**)
- GSM/GPRS (**MSM6550 only**)
- High-performance ARM926EJ-S running at up to 225 MHz
- Java hardware acceleration for faster Java-based games and other applets
- Integrated Bluetooth 1.2 baseband processor for wireless connectivity to peripherals
- High-speed, serial mobile display digital interface (MDDI), which optimizes the interconnection cost between the MSM device and LCD panel
- Dual receive chain diversity support for IS-95A/B, CDMA2000 1X, providing improved capacity and data throughput
- USB On-the-Go core supports both slave and limited host functionality
- Integrated wideband stereo codec for digital audio applications
- Direct interface to digital camera module with video front end (VFE) image processing
- CDMA cellular and CDMA PCS operation
- gpsOne position location capabilities (CDMA mode only)
- Vocoder support (EVRC, 13 k QCELP, AMR for MMS)
- Advanced 14x14 mm, 0.5 mm pitch, 409-pin lead-free CSP packaging technology

1.3.2 IS-2000 1X features supported by the MSM6550/MSM6150 device

- Fast 800 Hz forward power control
- Quasi-orthogonal functions
- Supplemental channel (SCH) support
- CDMA2000 1X forward quick paging channel (F-QPCH)
- Convolutional and turbo codes on SCH
- Radio link protocol (RLP3)

1.3.3 IS-856 1xEV-DO features (MSM6550 device only)

- High-speed peak data rates of 2.4 Mbps on forward link and 153 kbps on reverse link
- Handoff between IS-2000 and IS-856 systems
- Slotted mode operation for reduced power consumption

1.3.4 GSM/GPRS features (MSM6550 device only)

The following GSM modes and data rates are supported by the MSM6550 hardware. Support modes conform to release ‘99 specification of sub-feature.

- Voice features

  FR

  EFR

  AMR

  HR

  A5/1 and A5/2 ciphering

- Circuit switched data features

  9.6k

  14.4k

  Fax

  Transparent and non-transparent modes for CS data and Fax

  No sub rates are supported

- Packet switched data (GPRS)

  Class B operation

  Multi-slot class 10 data services

  CS schemes CS1, CS2, CS3, and CS4

  GEA1 and GEA2 ciphering

- Maximum of 4 Rx timeslots per frame

1.3.5 MSM6550/MSM6150 audio processing features

- Integrated wideband stereo CODEC

  16-bit DAC with typical 88 dB dynamic range

  Supports sampling rates up to 48 kHz on the speaker path and 16 kHz on the microphone path

  Supports summing of an external device's stereo single-ended analog signal

  Supports summing of I2S digital audio signal

  Supports headset switch press detection

- Voice recognition (PureVoiceVR™), including speaker-independent digit dialing
- Acoustic echo cancellation
- Audio AGC
- Internal Vocoder supporting 13kbps Pure Voice QCELP, SMV, and EVRC
- Standard MIDI with 16 Voices

1.3.6 MSM6550/MSM6150 microprocessor subsystem

- Industry standard ARM926EJ-S embedded microprocessor subsystem

  16 kB instruction and 16 kB data cache

  Instruction set compatible with ARM7TDMI

  ARM version 5TEJ instructions

  Higher performance 5 stage pipeline, Harvard cached architecture

  Higher internal CPU clock rate with on-chip cache

- Java hardware acceleration
- Enhanced memory support

  73 MHz bus clock for SDRAM and PSRAM

  32-bit SDRAM and PSRAM

  Dual memory buses separating the high-speed memory subsystem (EBI1) from low-speed peripherals (EBI2) such as LCD panels

  1.8 V or 2.6 V memory interface support (excluding EBI1)

  Burst mode NOR FLASH or SRAM

  Burst Mode is supported on all four EBI1 chip selects

  NAND FLASH memory interface

  Boot from NAND

  Low-power SDRAM (LP-SDRAM) interface

- Internal watchdog and sleep timers

1.3.7 Supported interface features

- Universal serial bus (USB)
- Three universal asynchronous receiver transmitter (UART) serial ports
- R-UIM/USIM controller (via second or third UART)
- Integrated 4-bit secure digital (SD) controller for SD and mini SD cards
- Parallel LCD interface
- General-purpose I/O pins
- High-speed, serial mobile display digital interface (MDDI), which optimizes the interconnection cost between the MSM and LCD panel

1.3.8 Supported multimedia features

- Provide additional general-purpose MIPS for 2004/2005 applications

  Two powerful QDSP4000s

  Dedicated hardware accelerators and compression engines

- Improve Java, BREW and game performance

  Integrated Java and 2D/3D graphics accelerator with Sprite engine

- Enable various accessories via USB host connectivity

  Integrated USB host controller functionality

- Enable compelling visual and audio applications

  High-quality digital camera processing, supporting CCD or CMOS image sensors up to 4-megapixel

  Dedicated support for market leading codecs such as MPEG-4, H.263, H.264

  Integrated stereo wideband CODEC for music/digital clips

  72-polyphony MIDI wavetable synthesizer for high-quality music playback through the MSM6550 integrated wideband codec

  Video telephony services

  Video telephony at 15 frames per second (fps), qCIF resolution

  Video encode at 15 fps at CIF for camcorder capability

  Video decode at 30 fps at CIF resolution, streaming or offline

- High-speed broadcast services on 1xEV-DO

  Enable TV like functionality on handset

- Location based services

  Integrated gpsOne processing

  Standalone gpsOne mode in which the handset acts as a GPS receiver

- CMX (text, picture, and MIDI streaming)

  72 voices

  44 kHz sampling

  512 kB wave table

  Morphing player and free A.T.

  PNG decoder

  Pitch bend range support

  MLZ decoder

  Integrated PNG/SAF A.T.

2 Pin Descriptions

2.1 I/O description parameters

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Type	
I	CMOS input
IS	Input with Schmitt trigger
O	Output
Z	High-Z output
B	Bidirectional with CMOS input
BS	Bidirectional with Schmitt trigger
P1	Tied to pad group 1 that uses supply voltage V_{DD_P1}
P2	Tied to pad group 2 that uses supply voltage V_{DD_P2}
P3	Tied to pad group 3 that uses supply voltage V_{DD_P3}
V	Power/ground
Special Circuitry	
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
NP	Contains no internal pull
PP	Programmable pull. This pin can be programmed to no pull, pull up, or pull down.
K	Contains an internal weak keeper device (Keepers cannot drive external buses.)
A	Analog pad
H	Digital input where input voltage level may reach up to 3.0V

Symbol	Description
Pad type	Indicate the pad type. The default configuration is in this column. For the pad types that contains “nppdpu”, capital NP, PD, or PU indicates that, upon power up, the pin has no-pull, pull-down, or pull-up, respectively. For the pad types that contains “kpd” or “kpu”, capital K, PD, or PU indicates that, upon power up, the pin has keeper, pull-down, or pull-up, respectively. Examples: *BS-HnpPDpu* ■ Bidirectional Schmitt trigger input with high voltage tolerant pad ■ Default is pull-down, configurable to non pull-up/down, pull-down, pull-up *HBS-nppdPU* Hybrid (analog/digital) pin bidirectional Schmitt trigger input with high voltage tolerant pad Default is pull-up, configurable to non pull-up/down, pull-down, pull-up
n-m	Variable drive strength pins. The number *n* is the drive strength when the PAD_CTL register bit is clear (0). The number *m* is the drive strength when the PAD_CTL register bit is set (1).

Table 2-2 Pin descriptions for the MSM6550/MSM6150 device

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
Clocks								
D18	TCXO	I			A	AI	-	TCXO clock input.
A10	USB_XTAL48_IN	I			C	AI	-	48MHz crystal oscillator input. For USB.
B10	USB_XTAL48_OUT	O			C	AO	-	48MHz crystal oscillator feedback output
A16	SLEEP_XTAL_IN	I			P3	AI	-	Low-power sleep controller crystal oscillator input.
B16	SLEEP_XTAL_OUT	O			P3	AO	-	Low-power sleep controller crystal oscillator output.
C26	Reserved function							Leave this pin unconnected
Modes and Resets								
F13	RESIN_N	I			P3	IS		Hardware reset input to system.
F11	RESOUT_N	O			P3	O	3-5	Reset output generated by synchronized RESIN_N and by wdog_reset. The rising edge of RESOUT_N is delayed from the rising edge of RESIN_N by a few microprocessor clocks.
AA4	RESOUT_N_EBI1	O			P1	O	3-5	Reset output generated by synchronized RESIN_N and by wdog_reset. The rising edge of RESOUT_N is delayed from the rising edge of RESIN_N by a few microprocessor clocks. Same voltage level as the first external memory interface. Connected to pad_group1.

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
AE17	WDOG_EN	I			P3	IS-PU	-	Watchdog timer enable input. WDOG_STB is behind GPIO[0].
H25	WDOG_STB	O	GPIO[0] SBCK1	B O	P3	BS-PP	2-5	Watchdog strobe output muxed behind GPIO[0].
T21	MODE2	I			P3	IS-PD	-	Determines operating mode of the chip. **MODE[2:0] Function** 000 Native, ARM Jtag 001Native, ARM Jtag, ETM 010Native, MSM Jtag 011 Reserved 100Native, MSM Jtag + ARM Jtag (ISDS/RTL can be used in mode 100) 101 Reserved 110 Reserved 111 Reserved
U23	MODE1	I			P3	IS-PD	-	
Y23	MODE0	I			P3	IS-PD	-	
AE22	BOOT_MODE2	I			P3	IS	-	Determines boot mode of the chip.
AE21	BOOT_MODE	I			P3	IS	-	**BOOT_MODE2 BOOT_MODE boot mode:** 0 0 16bit NOR FLASH 0 1 8bit NAND FLASH 1 X 16bit NAND FLASH
External Bus Interface1								
L2	LB1_N	O	SDRAM1_DQM[0]	O	P1	O	10-14	Low byte enable signal for byte access of 16-bit memory.
M6	UB1_N	O	SDRAM1_DQM[1]	O	P1	O	10-14	Upper byte enable signal for byte access of 16-bit memory.
U8	WE1_N	O	SDRAM1_WE_N	O	P1	O	10-14	Write enable signal
V2	OE1_N	O			P1	O	10-14	Output enable signal (effectively read enable signal)
V8	A1[25]	B	GPIO[75] SDRAM1_DQM[3]]	O O	P1	BS-npPDpu	10-14	Peripheral address bus
V1	A1[24]	B	GPIO[79] SDRAM1_A[0]	O O	P1	BS-npPDpu	10-14	
U4	A1[23]	B	GPIO[78] SDRAM1_DQM[2]	O O	P1	BS-npPDpu	10-14	
T8	A1[22]	O	SDRAM1_D[31]	B	P1	B-K	10-14	
T6	A1[21]	O	SDRAM1_D[30]	B	P1	B-K	10-14	
T4	A1[20]	O	SDRAM1_D[29]	B	P1	B-K	10-14	
R8	A1[19]	O	SDRAM1_D[28]	B	P1	B-K	10-14	
T2	A1[18]	O	SDRAM1_D[27]	B	P1	B-K	10-14	
T1	A1[17]	O	SDRAM1_D[26]	B	P1	B-K	10-14	
R6	A1[16]	O	SDRAM1_D[25]	B	P1	B-K	10-14	
R4	A1[15]	O	SDRAM1_D[24]	B	P1	B-K	10-14	
P11	A1[14]	O			P1	O	10-14	
P8	A1[13]	O			P1	O	10-14	
P6	A1[12]	O			P1	O	10-14	
P2	A1[11]	O			P1	O	10-14	
P1	A1[10]	O			P1	O	10-14	
N1	A1[9]	O			P1	O	10-14	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
N2	A1[8]	O			P1	O	10-14	
N6	A1[7]	O			P1	O	10-14	
N8	A1[6]	O			P1	O	10-14	
N11	A1[5]	O			P1	O	10-14	
M4	A1[4]	O			P1	O	10-14	
M8	A1[3]	O			P1	O	10-14	
L4	A1[2]	O			P1	O	10-14	
L1	A1[1]	O	**A1[26] for 32-bit PSRAM**		P1	O	10-14	
L6	D1[15]	B			P1	B-K	10-14	Peripheral data bus
L8	D1[14]	B			P1	B-K	10-14	
K4	D1[13]	B			P1	B-K	10-14	
J1	D1[12]	B			P1	B-K	10-14	
K6	D1[11]	B			P1	B-K	10-14	
J2	D1[10]	B			P1	B-K	10-14	
J4	D1[9]	B			P1	B-K	10-14	
P4	D1[8]	B			P1	B-K	10-14	
H4	D1[7]	B			P1	B-K	10-14	
G2	D1[6]	B			P1	B-K	10-14	
J6	D1[5]	B			P1	B-K	10-14	
AB4	D1[4]	B			P1	B-K	10-14	
D1	D1[3]	B			P1	B-K	10-14	
AB2	D1[2]	B			P1	B-K	10-14	
D2	D1[1]	B			P1	B-K	10-14	
E2	D1[0]	B			P1	B-K	10-14	
Y6	XMEM1_CS_N[3]	O	GPIO[77] SDRAM1_CS_N[1]	B O	P1	BS-PP O	10-14	XMEM chip select
Y4	XMEM1_CS_N[2]	O	SDRAM1_CS_N[0]	B	P1	O	10-14	XMEM chip select
AA1	XMEM1_CS_N[1]	O	GPIO[76]	O	P1	BS-PU	10-14	XMEM chip select
W6	XMEM1_CS_N[0]	O			P1	O	10-14	XMEM chip select
AB1	ROM1_CLK	O	SDRAM1_CLK	O	P1	O	10-14	Burst mode flash clock. Power on as output.
G1	ROM1_ADV_N	O	SDRAM1_RAS_N	O	P1	O	10-14	Burst mode flash's address valid signal.
AA2	HROM1_WAIT_N	I	SDRAM1_CLK_EN2, **A1[26] for 16-bit PSRAM**	O	P1	BS-PU	10-14	Burst flash ready signal. PSRAM, Upper 16 bit ready signal.
K8	ROM1_WAIT_N	I	SDRAM1_CAS_N	O	P1	BS-PU	10-14	Burst flash ready signal. PSRAM, lower 16 bit ready signal.
32-bit SDRAM access signals								
V8	SDRAM1_DQM[3]	O	GPIO[75]	O	P1		10-14	SDRAM byte 3 enable
U4	SDRAM1_DQM[2]	O	GPIO[78]	O	P1		10-14	SDRAM byte 2 enable
M6	SDRAM1_DQM[1]	O	UB1_N	O	P1	O	10-14	SDRAM byte 1 enable
L2	SDRAM1_DQM[0]	O	LB1_N	O	P1	O	10-14	SDRAM byte 0 enable
U8	SDRAM1_WE_N	O	WE1_N		P1	O	10-14	Write enable
AB1	SDRAM1_CLK	O	ROM1_CLK	O	P1	O	10-14	SDRAM clock

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
N4	SDRAM1_CLK_EN	O	PSRAM_CRE		P1	O	10-14	SDRAM clock enable
G1	SDRAM1_RAS_N	O	ROM1_ADV_N	O	P1	O	10-14	SDRAM row address strobe
K8	SDRAM1_CAS_N	O	ROM1_WAIT_N	O	P1	BS-PU	10-14	SDRAM column address strobe
Y4	SDRAM1_CS_N[0]	O	XMEM1_CS_N[2]	O	P1	O	10-14	SDRAM chip select
Y6	SDRAM1_CS_N[1]	O	GPIO[77] XMEM1_CS_N[3]	B O	P1	BS-PP	10-14	SDRAM chip select
V1	SDRAM1_A[0]	O	GPIO[79] A1[24]	B O	P1	BS-PP	10-14	SDRAM address 0
	SDRAM1_D[31:24]	B	A1[22:15]	B	P1	B-K	10-14	
	SDRAM1_D[23:16]	B	GPIO[74:67]	B	P1	B-K	10-14	
	SDRAM1_D[0:15]	B	D1[0:15]	B	P1	B-K	10-14	
External Bus Interface2								
AE10	LB2_N	O	A2[0] NAND2_ALE	O O	P2[1]	O	5-9	Low byte enable signal for byte access of 16-bit memory.
AF10	UB2_N	O	NAND2_CLE	O	P2[1]	O	5-9	Upper byte enable signal for byte access of 16-bit memory.
AF4	WE2_N	O			P2[1]	O	5-9	Write enable signal.
AF7	OE2_N	O	NAND2_RE_N	O	P2[1]	O	5-9	Output enable signal (effectively read enable signal)
AF13	A2[20]	O	GPIO[34]	BS-npPDpu	P2[1]	O	5-9	Second peripheral address bus
AA14	A2[19]	O			P2[1]	B	5-9	
T13	A2[18]	O			P2[1]	B	5-9	
AC14	A2[17]	O			P2[1]	O	5-9	
AE14	A2[16]	O			P2[1]	B	5-9	
W13	A2[15]	O			P2[1]	B	5-9	
AC13	A2[14]	O			P2[1]	B	5-9	
AA13	A2[13]	O			P2[1]	B	5-9	
AF12	A2[12]	O			P2[1]	B	5-9	
AE12	A2[11]	O			P2[1]	B	5-9	
AC12	A2[10]	O			P2[1]	B	5-9	
AA12	A2[9]	O			P2[1]	B	5-9	
W12	A2[8]	O			P2[1]	B	5-9	
T12	A2[7]	O			P2[1]	B	5-9	
AC11	A2[6]	O			P2[1]	B	5-9	
AA11	A2[5]	O			P2[1]	B	5-9	
AC10	A2[4]	O			P2[1]	B	5-9	
W11	A2[3]	O			P2[1]	B	5-9	
AF9	A2[2]	O			P2[1]	B	5-9	
AE9	A2[1]	O			P2[1]	B	5-9	
AE10	A2[0]	O	LB2_N	O	P2[1]	O	5-9	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
AA10	D2[15]	B			P2[1]	B-K	5-9	Second peripheral data bus
AC9	D2[14]	B			P2[1]	B-K	5-9	
W10	D2[13]	B			P2[1]	B-K	5-9	
AA9	D2[12]	B			P2[1]	B-K	5-9	
AE7	D2[11]	B			P2[1]	B-K	5-9	
AC8	D2[10]	B			P2[1]	B-K	5-9	
W9	D2[9]	B			P2[1]	B-K	5-9	
AA8	D2[8]	B			P2[1]	B-K	5-9	
AC7	D2[7]	B			P2[1]	B-K	5-9	
AF5	D2[6]	B			P2[1]	B-K	5-9	
AA7	D2[5]	B			P2[1]	B-K	5-9	
AE5	D2[4]	B			P2[1]	B-K	5-9	
AC6	D2[3]	B			P2[1]	B-K	5-9	
AE4	D2[2]	B			P2[1]	B-K	5-9	
AF3	D2[1]	B			P2[1]	B-K	5-9	
AC5	D2[0]	B			P2[1]	B-K	5-9	
AF14	LCD_CS_N	O	GPIO[38]	B	P2[1]	O	5	Peripheral chip-select.
AE13	LCD_EN	O	GPIO[37]	B	P2[1]	O	5	Peripheral chip-enable.
AA15	XMEM2_CS_N[3]	O	GPIO[36]	B	P2[1]	O	5	Peripheral chip-select.
W15	XMEM2_CS_N[2]	O	GPIO[35]	B	P2[1]	O	5	Peripheral chip-select.
AC15	XMEM2_CS_N[1]	O			P2[1]	O	5-9	Peripheral chip-select.
W14	XMEM2_CS_N[0]	O			P2[1]	O	5-9	Peripheral chip-select.
NAND Interface								
T14	NAND2_FLASH_READY	I	GPIO[33]	B	P2[1]	BS-PP	3-5	NAND flash ready input
AE10	NAND2_ALE	O	LB2_N A2[0]	O O	P2[1]	O	5-9	NAND flash address latch enable
AF10	NAND2_CLE	O	UB2_N	O	P2[1]	O	5-9	NAND flash command latch enable
AF7	NAND2_RE_N	O	OE2_N	O	P2[1]	O	5-9	NAND flash read enable
L26	NAND_BOOT_ERR	O	GPIO[95] UART1_DP_TX_DATA	B O	P3	BS-PP	5	Indicates NAND flash boot error. Powers up as NAND_BOOT_ERR when booting from NAND flash (BOOT_MODE=1)

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
User Interface								
U21	KEYSENSE4_N	I	GPIO[48] ETM_TRACE_PK2	B-PU O	P3	BS-PP	6	Can be used to sense key contact closure when connected to an external keypad. These pins require and active low level sensitive input signal and may cause an interrupt to the microprocessor. So possible implementation is detecting KEYSENSE interrupt and sending out drive signals via GPIOs, then we can decide which keypad was pressed.
R23	KEYSENSE3_N	I	GPIO[47], ETM_TRACE_PK1	B-PU O	P3	BS-PP	6	
D14	KEYSENSE2_N	I	GPIO[46], ETM_TRACE_PK0	B-PU O	P3	BS-PP	6	
P19	KENSENSE1_N	I	GPIO[63], ETM_ PIPESTAT1	B-PU O	P3	BS-PP	6	
R21	KEYSENSE0_N	I	GPIO[62], ETM_PIPESTAT0	B-PU O	P3	BS-PP	6	
L19	RINGER	O	GPIO[18]	B-PD	P3	BS-PP	3-5	DTMF tone generator circuit output which selects the pitch and cadence of the subscriber's ring. This output drives the second transducer. RInger needs a PD on power-up.
UART/UIM Interface								
P21	UART1_RFR_N	O	GPIO[98]	B	P3	BS-PP	5	UART ready-for-receive signal.
P16	UART1_CTS_N	I	GPIO[97]	B	P3	BS-PP	5	UART clear-to-send signal
M23	UART1_DP_RX_DATA	I	GPIO[96]	B	P3	BS-PP	5	UART receive serial data input.
L26	UART1_DP_TX_DATA	O	GPIO[95] NAND_BOOT_ERR	B O	P3	BS-PP	5	UART transmit serial data output. Boot up as NAND_BOOT_ERR when boots from NAND flash.
F4	UART2_RFR_N (UIM_CLK)	O O	GPIO[91]	B	P3	BS-PP	5	2nd UART ready-for-receive signal (also UIM clock)
G6	UART2_CTS_N (UIM_RESET)	I O	GPIO[90]	B	P3	BS-HPP	5	2nd UART clear-to-send signal (also UIM reset)
H6	UART2_DP_RX_DATA (UIM_PWR_EN)	I O	GPIO[89]	B	P3	BS-PP	5	2nd UART receive serial data input (also UIM power enable)
E4	UART2_DP_TX_DATA (UIM_DATA)	O B	GPIO[88]	B	P3	BS-HPP	5	2nd UART transmit serial data output (also UIM data)
L25	UART3_RFR_N (UIM2_CLK)	O O	GPIO[87]	B	P3	BS-PP	5	3rd UART ready-for-receive signal (also UIM2 clock)
L23	UART3_CTS_N (UIM2_RESET)	I O	GPIO[86]	B	P3	BS-HPP	5	3rd UART clear-to-send signal (also UIM2 reset)
M21	UART3_DP_RX_DATA (UIM2_PWR_EN)	I O	GPIO[85]	B	P3	BS-PP	5	3rd UART receive serial data input (also UIM2 power en)
M19	UART3_DP_TX_DATA (UIM2_DATA)	O B	GPIO[84]	B	P3	BS-HPP	5	3rd UART transmit serial data output (also UIM2 data)
USB Transceiver Interface								
N26	USB_DAT_VP	B	UART1_DP_RX_DATA		P3	B-K	4-5	Single-ended data. Differential plus (+)
N23	USB_SE0_VM	B	UART1_DP_TX_DATA		P3	B-K	4-5	Single-ended zero. Differential minus (-)
N25	USB_OE_TP_N	B			P3	B-K	2-5	An active low output used to enable or disable the D+ and D- pins of the transceiver. This is bidirectional, so it can be used as a USB interrupt.

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
N19	USB_RX_DATA	I	GPIO[29]	B	P3	BS-PP	3-5	Single-ended input from USB transceiver
K26	USB_SUSPEND	O	GPIO[17]	B	P3	BS-PP	3-5	Indicating suspending state
MMC Interface								
L14	MMC_DATA	B	GPIO[32]	B	P3	BS-HnppdPU	3-5	High voltage tolerant (3.0V)
M16	MMC_CLK	B	GPIO[31]	B	P3	BS-nppdPU	3-5	
H14	MMC_CMD	O	GPIO[30]	B	P3	BS-HnppdPU	3-5	High voltage tolerant (3.0V)
SD Interface								
L14	SDCC_DATA[0]	B	GPIO[32]	B	P3	BS-HnppdPU	3-5	High voltage tolerant (3.0V)
F25	SDCC_DATA[1]	**B**	GPIO[99]	B	P3	BS-HnpPDpu	5	High voltage tolerant (3.0V)
M25	SDCC_DATA[2]	**B**	GPIO[100]	B	P3	BS-HnpPDpu	5	High voltage tolerant (3.0V)
M26	SDCC_DATA[3]	B	GPIO[101]	B	P3	BS-HnpPDpu	5	High voltage tolerant (3.0V)
M16	SDCC_CLK	B	GPIO[31]	B	P3	BS-nppdPU	3-5	
H14	SDCC_CMD	O	GPIO[30]	B	P3	BS-HnppdPU	3-5	High voltage tolerant (3.0V)
SBI for GZIFTRIC, ZIFLNA0, and ZIFRIC0 (first receive chain)								
H26	SBST	O			P3	O	2-5	I3Q serial bus start/stop
J23	SBDT	B			P3	B-K	2-5	I3Q serial bus data
L21	SBCK	B			P3	B-PP	2-5	I3Q serial bus clock
SBI1 for ZIFLNA1 and ZIFRIC1 (second receive chain)								
H18	SBST1	O	GPIO[93]	B	P3	BS-PP	5	I3Q serial bus start/stop
F26	SBDT1	B	GPIO[1]	B	P3	B-KPU	2-5	I3Q serial bus data
H25	SBCK1	O	GPIO[0]	B	P3	B-PP	2-5	I3Q serial bus clock
AUX_SBI, for use with ZIFTIC in a phone without GSM (GRFCs are unused in that case) [0 dedicated pins]								
D11	AUX_SBST	O	GPIO[8]	B	P3	BS-nppdPU	2-5	I3Q serial bus start/stop
A8	AUX_SBDT	B	GPIO[4]	B	P3	BS-npPDpu	2-5	I3Q serial bus data
H10	AUX_SBCK	O	GPIO[7]	B	P3	BS-nppdPU	2-5	I3Q serial bus clock
I2C								
K21	I2C_SDA	B	GPIO[26]	B	P3	BS-nppdPU	3-5	I2C serial bus data
N16	I2C_SCL	B	GPIO[27]	B	P3	BS-nppdPU	3-5	I2C serial bus clock
Bluetooth								
G23	BT_CLK	I	GPIO[25]	B	P3	BS-nppdPU	3-5	12 MHz Bluetooth clock
F23	BT_SBST	O	GPIO[24]	B	P3	BS-nppdPU	3-5	BT SBI strobe signal

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
E26	BT_SBCK	O	GPIO[23]	B	P3	BS-nppdPU	3-5	BT SBI clock
E25	BT_SBDT	B	GPIO[22]	B	P3	BS-nppdPU	3-5	BT SBI input/output data
H21	BT_TX_RX_N	O	GPIO[21]	B	P3	BS-npPDpu	3-5	Tx/Rx strobe
R19	BT_DATA	B	GPIO[20]	B	P3	BS-npPDpu	3-5	Bluetooth Rx/Tx data
Camera Interface								
J21	CAMCLK_PO	O	GPIO[13]	B	P3	BS-npPDpu	3-5	Clock out to camera module
J26	CAMIF_DATA[1]	I	GPIO[81]	B	P3	BS-npPDpu	2-5	Data from the camera module
J25	CAMIF_DATA[0]	I	GPIO[83]	B	P3	BS-npPDpu	2-5	
F20	CAMIF_DATA[9]	I	GPIO[61]	B	P3	B-K	3-6	
F16	CAMIF_DATA[8]	I	GPIO[60]	B	P3	B-K	3-6	
D20	CAMIF_DATA[7]	I	GPIO[59]	B	P3	B-K	3-6	
L15	CAMIF_DATA[6]	I	GPIO[58]	B	P3	B-K	3-6	
J19	CAMIF_DATA[5]	I	GPIO[57]	B	P3	B-K	3-6	
D22	CAMIF_DATA[4]	I	GPIO[56]	B	P3	B-K	3-6	
C25	CAMIF_DATA[3]	I	GPIO[55]	B	P3	B-K	3-6	
D21	CAMIF_DATA[2]	I	GPIO[54]	B	P3	B-K	3-6	
B3	CAMIF_VSYNC	B	GPIO[16]]	B	P3	BS-npPDpu	3-5	Input vertical reference signal
E23	CAMIF_HSYNC	B	GPIO[15]	B	P3	BS-npPDpu	3-5	Input horizontal reference signal
K23	CAMIF_PCLK	I	GPIO[82]	B	P3	BS-npPDpu	2-5	Input pixel clock
AUX CODEC/PCM/Stereo DAC Interface								
K19	AUX_PCM_CLK	I	GPIO[80] SDAC_CLK	B I	P3	BS-npPDpu	2-5	PCM clock for auxiliary CODEC port
G4	AUX_PCM_DOUT	O	GPIO[103] SDAC_DOUT	B O	P3	BS-npPDpu	3-5	PCM data output for auxiliary CODEC port
N21	AUX_PCM_DIN	I	GPIO[14] SDAC_MCLK	B I	P3	BS-npPDpu	3-5	PCM data input for auxiliary CODEC port
J8	AUX_PCM_SYNC	O	GPIO[102] SDAC_L_R	B O	P3	BS-npPDpu	3- 5	PCM data strobe for auxiliary CODEC port
GP_PDMs								
D17	GP_PDM2	Z-PD	PA_RANGE[1]	O	P3	Z	2-5	General purpose 16-bit PDM. Clocked at TCXO/4 rate. Both microprocessor and DSP control the PDM.
H17	GP_PDM1	Z-PD	PA_RANGE[0]	O	P3	Z	2-5	
F18	GP_PDM0	Z-PD	GPIO[92]	B	P3	BS-npPDpu	2-5	
GP_MN								
J21	GP_MN	O	GPIO[13] GP_CLK	B	P3	BS-npPDpu	3-5	General purpose processor-controlled M/N counter. Clocked at TCXO/4 rate.

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
JTAG Pins								
H15	TRST_N	I			P3	BS-PD	3-5	JTAG reset
D16	TCK	I			P3	BS-PU	3-5	JTAG clock input
F15	TMS	I			P3	BS-PU	3-5	JTAG mode select input
D15	TDI	I			P3	BS-PU	3-5	JTAG data input
A17	TDO	Z			P3	Z	5-9	JTAG data output
H16	RTCK	O			P3	O	5-9	driven only by ARM9 JTAG
D21	AUX_TRST_N	I	GPIO[54]	B	P3	B-K	3-6	Auxiliary JTAG reset
C25	AUX_TCK	I	GPIO[55]	B	P3	B-K	3-6	Auxiliary JTAG clock input
D22	AUX_TMS	I	GPIO[56]	B	P3	B-K	3-6	Auxiliary JTAG mode select input
J19	AUX_TDI	I	GPIO[57]	B	P3	B-K	3-6	Auxiliary JTAG data input
L15	AUX_TDO	O	GPIO[58]	B	P3	B-K	3-6	Auxiliary JTAG data output
RF RX Interface								
H9	RX_VCO_SEL	O	GPIO[43]	B	P3	BS-PU	3-6	Selects which VCO used for Zifric1
A6	UHF_VCO_1_EN	O	GPIO[28]	B	P3	BS-PU	3-5	Enables second UHF VCO
TXDAC Interface								
B13	I_OUT	O			P3	AO	-	Non-inverted current mode output from the I transmit DAC
A13	I_OUT_N	O			P3	AO	-	Inverted current mode output from the I transmit DAC
B12	Q_OUT	O			P3	AO	-	Non-inverted current mode output from the Q transmit DAC
A12	Q_OUT_N	O			P3	AO	-	Inverted current mode output from the Q transmit DAC
F12	DAC_REF	O			P3	AO	-	Input reference to set the gain of the I&Q transmit DACs
RF TX Interface								
H11	PA_ON1	O	GPIO[2]	B	P3	BS-npPDpu	2-5	Control signal that controls the power amplifier. PA_ON is high only when the RF power amplifier is needed for transmission. Supports up to two power amplifiers. There is a design requirement that both PA's are powered off on the hardware reset. For PA_ON0, this is handled by the default state of the web register that drives it. For PA_ON1, this is handled by the default pull-down of GPIO2.
F17	PA_ON0	O			P3	O	3-5	
H12	TX_ON	O			P3	O	3-5	By using TX_ON, we can turn on/off TX IF separately from PA_ON. (PA needs longer warmup time, so this feature could reduce the current consumption of TX IF part.) The default state of the web register that drives TX_ON is '0'.
D17	PA_RANGE1	O	GP_PDM2	Z-PD	P3	Z-PP	2-5	Digital outputs from the transmit

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
H17	PA_RANGE0	O	GP_PDM1	Z-PD	P3	Z-PP	2-5	AGC circuit which can be used to alter the subscriber transmit power amplifier characteristics. These pins are PA_RANGE by default; the web registers for pdm_to_pa_range must be set to use the alternate function.
F19	TCXO_EN	O	GPIO[94]	B	P3	BS-PP	5	Enables TCXO and related circuitry
L13	TRK_LO_ADJ	O			P3	Z-PP	2-5	PDM output from the frequency tracking circuit which sets the subscriber VHF and UHF frequencies.
H13	TX_AGC_ADJ	O			P3	Z-PP	2-5	PDM output from the transmit AGC circuit to control the transmit output power.
MDP Interface Pins								
AD2	MDP_VSYNC_PRIMARY	I	GPIO[105]	B	P2[1]	BS-PP	5	
AD3	MDP_VSYNC_SECONDA	I	GPIO[104]	B	P2[1]	BS-PP	5	
MDDI Interface Pins								
B20	MDDIH_DATP	B			1.8	Custom		Host end of a high speed serial port
B19	MDDIH_DATN	B			1.8	Custom		(LCD interface)
A20	MDDIH_STBP	O			1.8	Custom		
A19	MDDIH_STBN	O			1.8	Custom		
A22	MDDIC_DATP	B			1.8	Custom		Client end of a high speed serial port
A23	MDDIC_DATN	B			1.8	Custom		(Camera interface)
B22	MDDIC_STBP	I			1.8	Custom		
B23	MDDIC_STBN	I			1.8	Custom		
General Purpose I/O and Interrupt Pins								
AD2	GPIO[105]	B	MDP_VSYNC_PRIMARY	I	P2[1]	BS-npPDpu	5	
AE3	GPIO[104]	B	MDP_VSYNC_SECONDA	I	P2[1]	BS-npPDpu	5	
G4	GPIO[103]	B	AUX_PCM_DOUT SDAC_DOUT	O O	P3	BS-npPDpu	5	Same cfg selection as aux_pcm_dout
J8	GPIO[102]	B	AUX_PCM_SYNC SDAC_L_R	O O	P3	BS-npPDpu	5	Same cfg selection as aux_pcm_sync
M26	GPIO[101]	B	SDCC_DAT[3]	B	P3	BS-H nppdPU	5	SDCC_DAT3 is high voltage tolerant (3V)
M25	GPIO[100]	B	SDCC_DAT[2]	B	P3	BS-H nppdPU	5	SDCC_DAT2 is high voltage tolerant (3V)
F25	GPIO[99]	B	SDCC_DAT[1]	B	P3	BS-H nppdPU	5	SDCC_DAT1 is high voltage tolerant (3V)
P21	GPIO[98]	B	UART1_RFR_N	O	P3	BS-npPDpu	5	
P16	GPIO[97]	B	UART1_CTS_N	I	P3	BS-npPDpu	5	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
M23	GPIO[96]	B	UART1_DP_RX_DATA	I	P3	BS-npPDpu	5	
L26	GPIO[95]	B	UART1_DP_TX_DATA NAND_BOOT_ERR	O O	P3	BS-nppdPU	5	
F19	GPIO[94]	B	TCXO_EN	I O	P3	BS-nppdPU	5	Need PU for TCXO_EN (for PMIC)
H18	GPIO[93]	B	SBST1	O	P3	BS-npPDpu	5	
F18	GPIO[92]	B	GP_PDM0 SYNTH0	Z O	P3	BS-npPDpu	5	
F4	GPIO[91]	B	UART2_RFR_N UIM_CLK	O O	P3	BS-npPDpu	5	
G6	GPIO[90]	B	UART2_CTS_N UIM_RESET	I O	P3	BS-HnpPDpu	5	UIM_RESET is high voltage tolerant (3V)
H6	GPIO[89]	B	UART2_DP_RX_DATA UIM_PWR_EN	I O	P3	BS-npPDpu	5	Must be pull down when used as UART2_DP_RX_DATA
E4	GPIO[88]	B	UART2_DP_TX_DATA UIM_DATA	O B	P3	BS--HnpPDpu	5	UIM_DATA is high voltage tolerant (3V)
L25	GPIO[87]	B	UART3_RFR_N UIM2_CLK	O O	P3	BS--npPDpu	5	
L23	GPIO[86]	B	UART3_CTS_N UIM2_RESET	I I	P3	BS-HnpPDpu	5	UIM2_RESET is high voltage tolerant (3V)
M21	GPIO[85]	B	UART3_DP_RX_DATA UIM2_PWR_EN	I O	P3	BS-npPDpu	5	Must be pull down
M19	GPIO[84]	B	UART3_DP_TX_DATA UIM2_DATA	O B	P3	BS-HnpPDpu	5	UIM2_DATA is high voltage tolerant (3V)
J25	GPIO[83]	B	CAMIF_DATA[0]	I	P3	BS-npPDpu	5	Spare GRFC[14]
K23	GPIO[82]	B	CAMIF_PCLK	I	P3	BS-npPDpu	5	Spare GRFC[13]
J26	GPIO[81]	B	CAMIF_DATA[1]	I	P3	BS-npPDpu	2-5	Spare GRFC[12]
K19	GPIO[80]	B	AUX_PCM_CLK	B	P3	BS-npPDpu	2-5	Spare GRFC[11]
V1	GPIO[79]	B	A1[24] SDRAM1_A[0]	O O	P1	BS-npPDpu	10-14	
U4	GPIO[78]	B	A1[23] SDRAM1_DQM[2]	O O	P1	BS-npPDpu	14	
Y6	GPIO[77]	B	XMEM1_CS_N[3], SDRAM1_CS_N[1]	O	P1	BS-nppdPU	14	
AA1	GPIO[76]	B	XMEM1_CS_N[1]	O	P1	BS-nppdPU	10-14	
V8	GPIO[75]	B	SDRAM1_DQM[3] A1[25]	O O	P1	BS-npPDpu	10-14	
W4	GPIO[74]	B	SDRAM1_D[23]	B-K	P1	B-K	10-14	
V6	GPIO[73]	B	SDRAM1_D[22]	B-	P1	B-K	10-14	
Y2	GPIO[72]	B	SDRAM1_D[21]	B-K	P1	B-K	10-14	
Y1	GPIO[71]	B	SDRAM1_D[20]	B-K	P1	B-K	10-14	
E1	GPIO[70]	B	SDRAM1_D[19]	B-K	P1	B-K	10-14	
R11	GPIO[69]	B	SDRAM1_D[18]	B-K	P1	B-K	10-14	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
V4	GPIO[68]	B	SDRAM1_D[17]	B-K	P1	B-K	10-14	
U6	GPIO[67]	B	SDRAM1_D[16]	B-K	P1	B-K	14	
F8	GPIO[66]	B	BACKLIGHT ETM_TRACECLK	O O	P3	BS-nppdPU	6	
B6	GPIO[65]	B	SYNTH2 ETM_TRACESYNC	O O	P3	BS-nppdPU	6	
F14	GPIO[64]	B	UART1_RI ETM_PIPESTAT2	O O	P3	BS-nppdPU	6	
P19	GPIO[63]	B	KEYSENSE1_N KYPD_3 ETM_PIPESTAT1	I-PU O	P3	BS-nppdPU	6	
R21	GPIO[62]	B	KEYSENSE0_N KYPD_1 ETM_PIPESTAT0	I-PU O	P3	BS-nppdPU	6	
F20	GPIO[61]	B	CAMIF_DATA9 ETM_TRACE_PKT15	I O	P3	B-K	6	
F16	GPIO[60]	B	CAMIF_DATA8 ETM_TRACE_PKT14	I O	P3	B-K	6	
D20	GPIO[59]	B	CAMIF_DATA7 ETM_TRACE_PKT13	I O	P3	B-K	6	
L15	GPIO[58]	B	CAMIF_DATA6 AUX_TDO ETM_TRACE_PKT12	I Z O	P3	B-K	6	
J19	GPIO[57]	B	CAMIF_DATA5 AUX_TDI ETM_TRACE_PKT11	I I O	P3	B-K	6	
D22	GPIO[56]	B	CAMIF_DATA4 AUX_TMS ETM_TRACE_PKT10	I I O	P3	B-K	6	
C25	GPIO[55]	B	CAMIF_DATA3 AUX_TCK ETM_TRACE_PKT9	I I O	P3	B-K	6	
D21	GPIO[54]	B	CAMIF_DATA2 AUX_TRST_N ETM_TRACE_PKT8	I I O	P3	B-K	6	
L12	GPIO[53]	B	KYPD_17 ETM_TRACE_PKT7	I O	P3	BS-nppdPU	6	
D10	GPIO[52]	B	KYPD_15 ETM_TRACE_PKT6	I O	P3	BS-nppdPU	6	
A7	GPIO[51]	B	KYPD_13 ETM_TRACE_PKT5	I O	P3	BS-nppdPU	6	
B7	GPIO[50]	B	KYPD_11 ETM_TRACE_PKT4	I O	P3	BS-nppdPU	6	
F9	GPIO[49]	B	KYPD_9 ETM_TRACE_PKT3	I O	P3	BS-nppdPU	6	
U21	GPIO[48]	B	KEYSENSE4_N ETM_TRACE_PKT2	I O	P3	BS-nppdPU	6	
R23	GPIO[47]	B	KEYSENSE3_N KYPD_7 ETM_TRACE_PKT1	I I O	P3	BS-nppdPU	6	
D14	GPIO[46]	B	KEYSENSE2_N KYPD_5 ETM_TRACE_PKT0	I I O	P3	BS-nppdPU	6	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
A4	GPIO[45]	B	KYPD_MEMO ETM_TRACESYNC_B	I O	P3	BS-npPDpu	6	
D8	GPIO[44]	B	UART1_DTR ETM_PIPESTAT0B GP_CLK	I-H O O	P3	BS-nppdPU	6	
H9	GPIO[43]	B	RX_VCO_SEL ETM_PIPESTAT1B	O O	P3	BS-nppdPU	6	
D7	GPIO[42]	B	PS_HOLD ETM_PIPESTAT2B	I O	P3	BS-npPDpu	6	
H23	GPIO[41]	B	SYNTH1 ETM_GPIO_IRQ_SRC	O I	P3	BS-nppdPU	5	
D6	GPIO[40]	B	ETM_GPIO_CS_N	O	P3	BS-nppdPU	5	
F7	GPIO[39]	B	ETM_KEYSENSE_IRQ_SRC	I I	P3	BS-nppdPU	5	
AF14	GPIO[38]	B	LCD_CS_N	O	P2[1]	BS-nppdPU	5	
AE13	GPIO[37]	B	LCD_EN	O	P2[1]	BS-npPDpu	5	
AA15	GPIO[36]	B	XMEM2_CS_N[3]	O	P2[1]	BS-nppdPU	5	
W15	GPIO[35]	B	XMEM2_CS_N[2]	O	P2[1]	BS-nppdPU	5	
AF13	GPIO[34]	B	A2[20]	O	P2[1]	BS-npPDpu	5	
T14	GPIO[33]	B	NAND2_FLASH_READY	I	P2[1]	BS-npPDpu	3-5	
L14	GPIO[32]	B	MMC_DATA SDCC_DAT0	B B	P3	BS-HnppdPU	3-5	MMC_DATA is high voltage tolerant (3V)
M16	GPIO[31]	B	MMC_CLK SDCC_CLK	O O	P3	BS-PP	3-5	
H14	GPIO[30]	B	MMC_CMD SDCC_CMD	B B	P3	BS-HnppdPU	3-5	
N19	GPIO[29]	B	USB_RX_DATA	I	P3	BS-npPDpu	3-5	
A6	GPIO[28]	B	UHF_VCO_1_EN	O	P3	BS-npPDpu	3-5	
N16	GPIO[27]	B	I2C_SCL	B	P3	BS-nppdPU	3-5	
K21	GPIO[26]	B	I2C_SDA	B	P3	BS-nppdPU	3-5	
G23	GPIO[25]	B	BT_CLK	I	P3	BS-nppdPU	3-5	
F23	GPIO[24]	B	BT_SBST	O	P3	BS-nppdPU	3-5	
E26	GPIO[23]	B	BT_SBCK	O	P3	BS-nppdPU	3-5	
E25	GPIO[22]	B	BT_SBDT	B	P3	BS-nppdPU	3-5	
H21	GPIO[21]	B	BT_TX_RX_N	O	P3	BS-npPDpu	3-5	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
R19	GPIO[20]	B	BT_DATA	B	P3	BS-npPDpu	3-5	
G21	GPIO[19]	B	SYNTH_LOCK	I	P3	BS-npPDpu	3-5	
L19	GPIO[18]	B	RINGER	O	P3	BS-npPDpu	3-5	
K26	GPIO[17]	B	USB_SUSPEND	O	P3	BS-nppdPU	3-5	
B3	GPIO[16]	B	CAMIF_VSYNC	B-PD	P3	BS-npPDpu	3-5	
E23	GPIO[15]	B	CAMIF_HSYNC	B-PD	P3	BS-npPDpu	3-5	
N21	GPIO[14]	B	AUX_PCM_DIN SDAC_MCLK	I I	P3	BS-npPDpu	3-5	
J21	GPIO[13]	B	GP_MN CAMCLK_PO	O O	P3	BS-npPDpu	3-5	
D5	GPIO[12]	B			P3	BS-npPDpu	2-5	
B4	GPIO[11]	B			P3	BS-npPDpu	2-5	
T23	GPIO[10]	B			P3	BS-npPDpu	2-5	
T19	GPIO[9]	B			P3	BS-npPDpu	2-5	
D11	GPIO[8]	B	AUX_SBST	O	P3	BS-nppdPU	2-5	
H10	GPIO[7]	B	AUX_SBCK	O	P3	BS-nppdPU	2-5	
F10	GPIO[6]	B			P3	BS-npPDpu	2-5	
D9	GPIO[5]	B			P3	BS-npPDpu	2-5	
A8	GPIO[4]	B	AUX_SBDT	B	P3	BS-npPDpu	2-5	
B8	GPIO[3]	B			P3	BS-npPDpu	2-5	
H11	GPIO[2]	B	PA_ON1	O	P3	BS-npPDpu	2-5	
F26	GPIO[1]	B	SBDT1	B	P3	B-KPU	2-5	
H25	GPIO[0]	B	SBCK1 WDOG_STB	O O	P3	BS-npPDpu	2-5	
Analog RF Rx Interface								
AC25	I_IP_CH0	I			A	AI		Ch0 Differential analog I signal (+)
AB25	I_IM_CH0	I			A	AI		Ch0 Differential analog I signal (-)
Y25	Q_IP_CH0	I			A	AI		Ch0 Differential analog Q signal (+)
AA25	Q_IM_CH0	I			A	AI		Ch0 Differential analog Q signal (-)
W25	I_IP_CH1	I			A	AI		Ch1 Differential analog I signal (+)
V25	I_IM_CH1	I			A	AI		Ch1 Differential analog I signal (-)
V23	Q_IP_CH1	I			A	AI		Ch1 Differential analog Q signal (+)
W23	Q_IM_CH1	I			A	AI		Ch1 Differential analog Q signal (-)

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
Internal Codec Signals								
AE20	MIC1P				A	AI		Mic 1 input (+)
AF20	MIC1N				A	AI		Mic 1 input (-)
AF22	MIC2P				A	AI		Mic 2 input (+)
AF21	MIC2N				A	AI		Mic 2 input (-)
AE19	AUXIP				A	AI		Auxiliary input (+)
AF19	AUXIN				A	AI		Auxiliary input (-)
AA19	MICOUTP				A	AO		Mic output to external Tx high pass filter (+)
AA18	MICOUTN				A	AO		Mic output to external Tx high pass filter (-)
AC20	MICINP				A	AI		Mic input from external Tx high pass filter (+)
AC19	MICINN				A	AI		Mic input from external Tx high pass filter (-)
AC21	MICIFBP				A	AI		Mic amp feedback from external Tx high pass filter (+)
AC22	MICIFBN				A	AI		Mic amp feedback from external Tx high pass filter (-)
AF18	EAR1OP				A	AO		Earphone 1 amplifier output (+)
AE18	EAR1ON				A	AO		Earphone 1 amplifier output (-)
AC17	AUXOP				A	AO		Auxiliary output (+) To carkit, PMIC2, or external speaker
AC18	AUXON				A	AO		Auxiliary output (-) To carkit, PMIC2, or external speaker
T15	MICBIAS				A	AO		Microphone bias supply output, no decoupling capacitors.
AA20	CCOMP				A	AI		External decoupling capacitor input for CODEC voltage reference.
AA17	HPH_R				A	AO		Stereo headphone right output.
W17	HPH_L		EAR2O		A	AO		Stereo headphone left output. (Earphone 2 amplifier output)
General Purpose ADC Signal								
AB23	HKAIN[5]	I			A	AI		Analog mux input channels to the on-chip housekeeping ADC.
Y21	HKAIN[4]	I			A	AI		
V19	HKAIN[3]	I			A	AI		
W21	HKAIN[2]	I			A	AI		
AA23	HKAIN[1]	I			A	AI		
V21	HKAIN[0]	I			A	AI		
ETM Interface								
F8	ETM_TRACECLK	O	BACKLIGHT GPIO[66]	O B	P3	BS-PP	6	ETM debugging interface
B6	ETM_TRACESYNC	O	SYNTH2 GPIO[65]	O B	P3	BS-PP	6	
F14	ETM_PIPESTAT2	O	UART1_RI GPIO[64]	O B	P3	BS-PP	6	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
P19	ETM_PIPESTAT1	O	KEYSENSE1_N KYPD_3 GPIO[63]	I-PU B	P3	BS-PP	6	
R21	ETM_PIPESTAT0	O	KEYSENSE0_N KYPD_1 GPIO[62]	I-PU B	P3	BS-PP	6	
F20	ETM_TRACE_PKT15	O	CAMIF_DATA9 GPIO[61]	I B	P3	B-K	6	
F16	ETM_TRACE_PKT14	O	CAMIF_DATA8 GPIO[60]	I B	P3	B-K	6	
D20	ETM_TRACE_PKT13	O	CAMIF_DATA7 GPIO[59]	I B	P3	B-K	6	
L15	ETM_TRACE_PKT12	O	CAMIF_DATA6 AUX_TDO GPIO[58]	I Z B	P3	B-K	6	
J19	ETM_TRACE_PKT11	O	CAMIF_DATA5 AUX_TDI GPIO[57]	I I B	P3	B-K	6	
D22	ETM_TRACE_PKT10	O	CAMIF_DATA4 AUX_TMS GPIO[56]	I I B	P3	B-K	6	
C25	ETM_TRACE_PKT9	O	CAMIF_DATA3 AUX_TCK GPIO[55]	I I B	P3	B-K	6	
D21	ETM_TRACE_PKT8	O	CAMIF_DATA2 AUX_TRST_N GPIO[54]	I I B	P3	B-K	6	
L12	ETM_TRACE_PKT7	O	KYPD_17 GPIO[53]	I B	P3	BS-PP	6	
D10	ETM_TRACE_PKT6	O	KYPD_15 GPIO[52]	I B	P3	BS-PP	6	
A7	ETM_TRACE_PKT5	O	KYPD_13 GPIO[51]	I B	P3	BS-PP	6	
B7	ETM_TRACE_PKT4	O	KYPD_11 GPIO[50]	I B	P3	BS-PP	6	
F9	ETM_TRACE_PKT3	O	KYPD_9 GPIO[49]	I B	P3	BS-PP	6	
U21	ETM_TRACE_PKT2	O	KEYSENSE4_N GPIO[48]	I B	P3	BS-PP	6	
R23	ETM_TRACE_PKT1	O	KEYSENSE3_N KYPD_7 GPIO[47]	I I B	P3	BS-PP	6	
D14	ETM_TRACE_PKT0	O	KEYSENSE2_N KYPD_5 GPIO[46]	I I B	P3	BS-PP	6	
A4	ETM_TRACESYNC_B	O	KYPD_MEMO GPIO[45]	I B	P3	BS-PP	6	
D8	ETM_PIPESTAT0B	O	UART1_DTR GPIO[44] GP_CLK	I-H B O	P3	BS-PP	6	
H9	ETM_PIPESTAT1B	O	RX_VCO_SEL GPIO[43]	O B	P3	BS-PP	6	
D7	ETM_PIPESTAT2B	O	PS_HOLD GPIO[42]	I B	P3	BS-PP	6	

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
H23	ETM_GPIO_IRQ_SRC	O	SYNTH1 GPIO[41]	O B	P3	BS-PP	5	In ETM mode, this pin is an unmaskable interrupt source and should be pulled low.
D6	ETM_GPIO_CS_N	O	GPIO[40]	B	P3	BS-PP	5	
F7	ETM_ KEYSENSE_IRQ_SRC	O	GPIO[39]	I B	P3	BS-PP	5	In ETM mode, this pin is an unmaskable interrupt source and should be pulled low.
Digital Power/Ground								
B5 **B11** **B14** **B24** **D25** **G25** **T25** **AE16** **AE8** **AC2** **W2** **H2** **C2**	VDD_C							Digital VDD for logic core
A5 **A11** **A14** **A24** **D26** **G26** **T26** **AF16** **AF8** **AC1** **W1** **H1** **C1**	GND							
U2 **R2** **M2** **K2** **F2**	VDD_P1							VDD for Pad group 1
U1 **R1** **M1** **K1** **F1**	GND							

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
AE15 **AE11** **AE6**	VDD_P2							VDD for Pad group 2
AF15 **AF11** **AF6**	GND							
A3 **B9** **B15** **K25** **R25**	VDD_P3							Vdd for Pad group 3
A9 **A15** **B17** **R26**	GND							
MDDI Power/Ground								
B21	VDD_MDDI					A		MDDI host and client
A21	GND					A		
Analog Power/Ground								
D12	VDD_A					A		TX DAC
P23	VDD_A					A		PA_CTL_DAC
B18	VDD_A					A		PLL
AE23	VDD_A					A		Codec
AA16	VDD_A					A		Earphone Amplifier
AF17	VDD_A					A		Stereo DAC.
U25 **U26** **Y26** **AA26**	VDD_A					A		Baseband sigma- delta modulator ch1.
AF23	GND_RET					G		Analog VSS for the CODEC
D13 **P26** **A18** **D19** **W18** **W16** **U19** **V26** **AC16** **AC26**	GND							

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
A1,A2, A25,A26 **B1,B25, B26** **D4,D23** **F6,F21** **H8,H19** **K10** **L11,L16** **M11-15** **N12-15** **P12-15** **R12-16** **T11,T16** **W8,W19** **AA6,AA21** **AC4,AC23** **AE1,AE2** **AE25-26** **AF1,AF2** **AF25-26**	NC							Many of these NC (no connect) pins are shorted together internally. They can be connected to ground for improved thermal flow and reduced RFI.
Pins reserved for re-use with future pin-compatible MSM devices such as MSM6700 and MSM6800								
AD1	Reserved							Connect this pin to ground and to VDD_P with resistors (both DNI)
B2	Reserved							Connect this pin to ground
AD25	Reserved							Internally shorted to GND pin (AC26) – leave this pin unconnected.
AE24	Reserved							Internally shorted to VDD_A pin (AE23) – leave this pin unconnected.
AF24	Reserved							Internally shorted to GND_RET pin (AF23) – leave this pin unconnected.

Note: Drive strength listed is for pad voltage source (VDD_P2) equal to 2.6V. Actual pad drive strength is lower (about half of the ratings shown here) if VDD_P2 is tied to 1.8V.

In addition to Table 2-2, the following table is specific to the MSM6550 device.

Table 2-3 Pin descriptions specific to the MSM6550 device

Ball No.	Native Mode				Volt	Pad_ Type	Drive (mA)	Description
	Main Function	Dir-Pol	Alternate Functions	Dir-Pol				
GSM Interface								
J25	GRFC[14]	O	GPIO[83]	B	P3	BS-PP	5	Spare GRFC
K23	GRFC[13]	O	GPIO[82]	B	P3	BS-PP	5	Spare GRFC
J26	GRFC[12]	O	GPIO[81]	B	P3	B-PP	2-5	Spare GRFC
K19	GRFC[11]	O	GPIO[80]	B	P3	B-PP	2-5	Spare GRFC
H12	GRFC[10]	O	TX_ON	O	P3	B-PP	2-5	TX_ON
D5	GRFC[9]	O	GPIO[12]	B	P3	B-PP	2-5	GPS_SEL
B4	GRFC[8]	O	GPIO[11]	B	P3	B-PP	2-5	GSM_ANT_SEL2_N
T23	GRFC[7]	O	GPIO[10]	B	P3	B-PP	2-5	GSM_ANT_SEL1_N
T19	GRFC[6]	O	GPIO[9]	B	P3	B-PP	2-5	GSM_ANT_SEL0_N
D11	GRFC[5]	O	GPIO[8]	B	P3	B-PP	2-5	TX_VCO_0_EN_N
H10	GRFC[4]	O	GPIO[7]	B	P3	B-PP	2-5	TX_VCO_1_EN_N
F10	GRFC[3]	O	GPIO[6]	B	P3	B-PP	2-5	UHF_BAND_SEL
D9	GRFC[2]	O	GPIO[5]	B	P3	B-PP	2-5	GSM_PA_BAND
A8	GRFC[1]	O	GPIO[4]	B	P3	B-KPU	2-5	GSM_PA_EN
B8	GRFC[0]	O	GPIO[3]	B	P3	B-PP	2-5	UHF_VCO_0_EN
PA control DAC signals								
P25	PA_POWER_CTL	O			P3	AO	-	Output from the PA Power Control DAC. analog control pin to control GSM PA controller. A single ended signal.
AD26	PA_DAC_EXT_REF	I			A	AI	-	External PA DAC reference voltage
Synthesizer Interface								
B6	SYNTH2	O	GPIO[65]	B	P3	BS-PP	6	Software controlled Synthesizer
H23	SYNTH1	O	GPIO[41]	B	P3	BS-PP	5	
F18	SYNTH0	O	GPIO[92]	B	P3	BS-PP	5	

Table 2-4 409-ball CSP pinout for the MSM6550/MSM6150 device

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	NC	NC	vdd_pad3	gpio45	gnd	gpio28	gpio51	gpio4	gnd	usb_xtal48_in	gnd	q_out_n	i_out_n	gnd	gnd	sleep_xtal_in	tdo	gnd	mddih_stbn	mddih_stbp	gnd	mddic_datp	mddic_datn	gnd	NC	NC	A
B	NC	Reserved	gpio16	gpio11	vdd_c	gpio65	gpio50	gpio3	vdd_pad3	usb_xtal48_out	vdd_c	q_out	i_out	vdd_c	vdd_pad3	sleep_xtal_out	gnd	vdd_a	mddih_datn	mddih_datp	vdd_mddi	mddic_stbp	mddic_stbn	vdd_c	NC	NC	B
C	gnd	vdd_c																							gpio55	Reserved	C
D	d1_3	d1_1		NC	gpio12	gpio40	gpio42	gpio44	gpio5	gpio52	gpio8	vdd_a	gnd	gpio46	tdi	tck	pa_range1	tcxo	gnd	gpio59	gpio54	gpio56	NC		vdd_c	gnd	D
E	gpio70	d1_0		gpio88																			gpio15		gpio22	gpio23	E
F	gnd	vdd_pad1		gpio91		NC	gpio39	gpio66	gpio49	gpio6	resout_n	dac_ref	resin_n	gpio64	tms	gpio60	pa_on0	gpio92	gpio94	gpio61	NC		gpio24		gpio99	gpio1	F
G	rom1_adv_n	d1_6		gpio103		gpio90															gpio19		gpio25		vdd_c	gnd	G
H	gnd	vdd_c		d1_7		gpio89		NC	gpio43	gpio7	gpio2	tx_on	tx_agc_adj	gpio30	trst_n	rtck	pa_range0	gpio93	NC		gpio21		gpio41		gpio0	sbst	H
J	d1_12	d1_10		d1_9		d1_5		gpio102											gpio57		gpio13		sbdt		gpio83	gpio81	J
K	gnd	vdd_pad1		d1_13		d1_11		rom1_wait_n		NC									gpio80		gpio26		gpio82		vdd_pad3	gpio17	K
L	a1_1	lb1_n		a1_2		d1_15		d1_14			NC	gpio53	trk_lo_adj	gpio32	gpio58	NC			gpio18		sbck		gpio86		gpio87	gpio95	L
M	gnd	vdd_pad1		a1_4		ub1_n		a1_3			NC	NC	NC	NC	NC	gpio31			gpio84		gpio85		gpio96		gpio100	gpio101	M
N	a1_9	a1_8		sdram1_clk_en		a1_7		a1_6			a1_5	NC	NC	NC	NC	gpio27			gpio29		gpio14		usb_se0_vm		usb_oe_tpn	usb_dat_vp	N
P	a1_10	a1_11		d1_8		a1_12		a1_13			a1_14	NC	NC	NC	NC	gpio97			gpio63		gpio98		vdd_a		pa_power_ctl	gnd	P
R	gnd	vdd_pad1		a1_15		a1_16		a1_19			gpio69	NC	NC	NC	NC	NC			gpio20		gpio62		gpio47		vdd_pad3	gnd	R
T	a1_17	a1_18		a1_20		a1_21		a1_22			NC	a2_7	a2_18	gpio33	micbias	NC			gpio9		mode2		gpio10		vdd_c	gnd	T
U	gnd	vdd_pad1		gpio78		gpio67		we1_n											gnd		gpio48		mode1		vdd_a	vdd_a	U
V	gpio79	oe1_n		gpio68		gpio73		gpio75											hkain3		hkain0		q_ip_ch1		i_im_ch1	gnd	V
W	gnd	vdd_c		gpio74		xmem1_cs_n0		NC	d2_9	d2_13	a2_3	a2_8	a2_15	xmem2_cs_n0	gpio35	gnd	hph_l	gnd	NC		hkain2		q_im_ch1		i_ip_ch1	gnd	W
Y	gpio71	gpio72		xmem1_cs_n2		gpio77															hkain4		mode0		q_ip_ch0	vdd_a	Y
AA	gpio76	hrom1_wait_n		resout_n_ebi1		NC	d2_5	d2_8	d2_12	d2_15	a2_5	a2_9	a2_13	a2_19	gpio36	vdd_a	hph_r	micoutn	micoutp	ccomp	NC		hkain1		q_im_ch0	vdd_a	AA
AB	rom1_clk	d1_2		d1_4																			hkain5		i_im_ch0	gnd	AB
AC	gnd	vdd_c		NC	d2_0	d2_3	d2_7	d2_10	d2_14	a2_4	a2_6	a2_10	a2_14	a2_17	xmem2_cs_n1	gnd	auxop	auxon	micinn	micinp	micfbp	micfbn	NC		i_ip_ch0	gnd	AC
AD	Reserved	gpio105																							Reserved	pa_dac_ext_ref	AD
AE	NC	NC	gpio104	d2_2	d2_4	vdd_pad2	d2_11	vdd_c	a2_1	lb2_n	vdd_pad2	a2_11	gpio37	a2_16	vdd_pad2	vdd_c	wdog_en	ear1on	auxip	mic1p	boot_mode	boot_mode2	vdd_a	Reserved	NC	NC	AE
AF	NC	NC	d2_1	we2_n	d2_6	gnd	oe2_n	gnd	a2_2	ub2_n	gnd	a2_12	gpio34	gpio38	gnd	gnd	vdd_a	ear1op	auxin	mic1n	mic2n	mic2p	gnd_ret	Reserved	NC	NC	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

3 Electrical Specifications

3.1 DC electrical specifications

3.1.1 Absolute maximum ratings

Operating the MSM6550/MSM6150 device under conditions that exceed those listed in Table 3-1 may result in damage to the device. Absolute maximum ratings are limiting values, and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the MSM6550/MSM6150 device under any of the conditions in Table 3-1 is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min	Max	Units
T_S	Storage temperature	-65	+150	°C
T_J	Junction temperature	—	+150	°C
V_I	Voltage on any input or output pin	-0.5	VDD+0.5	V
$V_{DD\_A,P}$	Supply voltage (analog, pad)	-0.3	3	V
V_{DD_C}	Supply voltage (core)	-0.3	2.3	V
I_{IN}	Latchup current	-100	+100	mA
V_{ESDHBM}	Electrostatic discharge voltage (human body model)	—	2500	V
V_{ESDCDM}	Electrostatic discharge voltage (charge device model)	—	750	V

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.1.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol	Description	Min	Typ[1]	Max	Units
T_C	Operating temperature (case)	–30	–	100	°C
V_{DD_C}	Supply voltage for internal digital core	1.30	1.375	1.45	V
V_{DD_A}	Supply voltage for internal analog core	2.5	2.6	2.7	V
V_{DD_P1}	Supply voltage P1 for EBI1 and peripheral interfaces	1.65	1.8	1.95	V
V_{DD_P2}[2]	Supply voltage P2 for EBI2 and peripheral interfaces	1.65 2.5	1.8 2.6	1.95 2.7	V V
V_{DD_P3}	Supply voltage P3 for peripheral interfaces	2.5	2.6	2.7	V
V_{DD_MDDI}	Supply voltage for MDDI	1.65	1.8	1.95	V

Terms and conditions

1. The typical voltages represent recommended output settings of the output regulators on the PM6650 device.
2. This voltage must match the external device voltage. It is a dual voltage pin and can be either 1.8VDC nominal or 2.6VDC nominal.

It is recommended that designers use a programmable voltage regulator for VDD_C, such as the PM6650. This allows best flexibility for using the same design for future pin compatible MSM devices which might require a lower VDD_C.

3.1.3 Thermal characteristics

Table 3-3 Thermal resistance

Symbol	Description	Typ	Units
Θ_{JA}	Junction to still air	37	ºC/W
Θ_{JC}	Junction to case	1	ºC/W

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.1.4 DC characteristics

Table 3-4 DC characteristics (for V_{DD_PX} = 1.8 V)

Symbol	Description	Min	Max	Units	Notes
V_{IH}	High-level input voltage, CMOS/Schmitt	0.65 • V_{DD_Px}	V_{DD_Px} + 0.3	V	—
V_{IL}	Low-level input voltage, CMOS/Schmitt	–0.3	0.35 • V_{DD_Px}	V	—
V_{SHYS}	Schmitt hysteresis voltage	100	–	mV	—
I_{IH}	Input high leakage current	–	1	µA	1, 2
I_{IL}	Input low leakage current	–1	–	µA	1, 2
I_{IHPD}	Input high leakage current with pull-down	3	30	µA	1, 3
I_{ILPU}	Input low leakage current with pull-up	–30	–3	µA	2, 3
V_{OH}	High-level output voltage, CMOS, when driving pin at rated drive strength	V_{DD_Px}–0.45	V_{DD_Px}	V	4, 5
V_{OL}	Low-level output voltage, CMOS, when driving pin at rated drive strength	0	0.45	V	4, 5
I_{OZH}	High-level, three-state leakage current	–	1	µA	1
I_{OZL}	Low-level, three-state leakage current	–1	–	µA	2
I_{OZHPD}	High-level, three-state leakage current with pull-down	3	30	µA	1, 3
I_{OZLPU}	Low level, three-state leakage current with pull-up	–30	–3	µA	2, 3
I_{OZHKP}	High-level, three-state leakage current with keeper	–20	–3	µA	1, 3
I_{OZLKP}	Low level, three-state leakage current with keeper	3	20	µA	2, 3
I_{ISL}	Sleep xtal input leakage	-0.15	0.15	µA	—
I_{IUXTAL}	USB xtal input leakage	-0.15	0.15	µA	—
I_{IHVKP}	High voltage tolerant input leakage with keeper	–0.15	–	µA	—
C_{IN}	Input capacitance	–	7	pF	6

Notes:

1. Pin voltage = V_{DD_P} max. For keeper pins, pin voltage = V_{DD_P} max – 0.45 volts.
2. Pin voltage = V_{ss} and V_{DD_P} = V_{DD_P} max. For keeper pins, pin voltage = 0.45 volts and V_{DD_P} = V_{DD_P} max.
3. Refer to Table 2-2 for pull-up, pull-down, and keeper information on pins.
4. Refer to Table 2-2 for I_{OH} and I_{OL} rated drive strength (current capacity) for output pins (at V_{DD_P} = V_{DD_P} min).
5. The rated drive strength is found in Table 2-2 under the column titled “1.8V Dr mA.”
6. Input capacitance value is guaranteed by design, not 100% tested.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-5 DC characteristics (for V_{DD_PX} = 2.5–2.7 V)

Symbol	Description	Min	Max	Units	Notes
V_{IH}	High-level input voltage, CMOS/Schmitt	0.65 • V_{DD_Px}	V_{DD_Px} + 0.3	V	—
V_{IL}	Low-level input voltage, CMOS/Schmitt	–0.3	0.35 • V_{DD_Px}	V	—
V_{SHYS}	Schmitt hysteresis voltage	150	–	mV	—
I_{IH}	Input high leakage current	–	1	µA	1, 2
I_{IL}	Input low leakage current	–1	–	µA	1, 2
I_{IHPD}	Input high leakage current with pull-down	10	60	µA	1, 3
I_{ILPU}	Input low leakage current with pull-up	–60	–10	µA	2, 3
V_{OH}	High-level output voltage, CMOS, when driving pin at rated drive strength	V_{DD_Px}–0.45	V_{DD_Px}	V	4, 5
V_{OL}	Low-level output voltage, CMOS, when driving pin at rated drive strength	0	0.45	V	4, 5
I_{OZH}	High-level, three-state leakage current	–	1	µA	1
I_{OZL}	Low-level, three-state leakage current	–1	–	µA	2
I_{OZHPD}	High-level, three-state leakage current with pull-down	10	60	µA	1, 3
I_{OZLPU}	Low level, three-state leakage current with pull-up	–60	–10	µA	2, 3
I_{OZHKP}	High-level, three-state leakage current with keeper	–25	–5	µA	1, 3
I_{OZLKP}	Low level, three-state leakage current with keeper	5	25	µA	2, 3
I_{ISL}	Sleep xtal input leakage	-0.15	0.15	µA	—
I_{IUXTAL}	USB xtal input leakage	-0.15	0.15	µA	—
I_{IHVKP}	High voltage tolerant input leakage with keeper	–0.15	0.15	µA	—
C_{IN}	Input capacitance	–	7	pF	6
$V_{TCXOHDC}$	High-level input voltage, TCXO DC input	0.65 • V_{DD_A}	V_{DD_A} + 0.3	V	—
$V_{TCXOLDC}$	Low-level input voltage, TCXO DC input	0.3	0.35 * V_{DD_A}	V	—
V_{TCXOAC}	Peak-to-peak input voltage, TCXO AC input	0.5	V_{DD_A} + 0.3	V	—
I_TCXOIHDC	Input high leakage with pull-down, TCXO DC input	5	45	µA	1

Notes:

1. Pin voltage = V_{DD_P} max. For keeper pins, pin voltage = V_{DD_P} max – 0.45 volts.
2. Pin voltage = V_{ss} and V_{DD_P} = V_{DD_P} max. For keeper pins, pin voltage = 0.45 volts and V_{DD_P} = V_{DD_P} max.
3. Refer to Table 2-2 for pull-up, pull-down, and keeper information on pins.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

4. Refer to Table 2-2 for I_{OH} and I_{OL} rated drive strength (current capacity) for output pins (at V_{DD_P} = V_{DD_P} min).
5. The rated drive strength is found in Table 2-2.
6. Input capacitance value is guaranteed by design, not 100% tested.

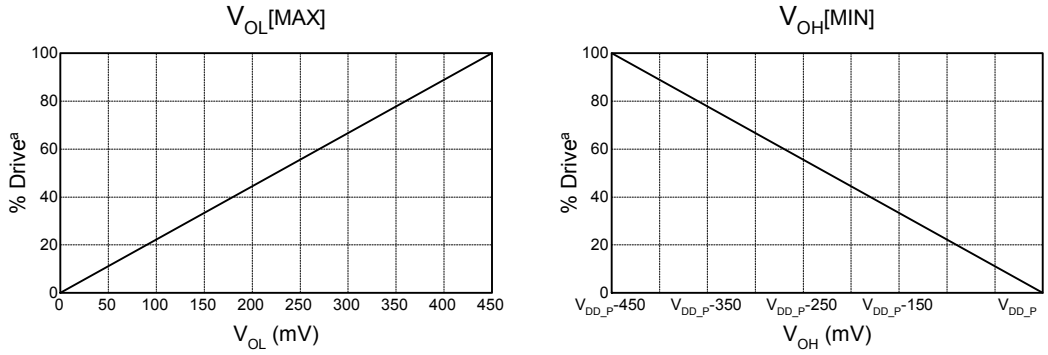

Figure 3-1 IV curve for V_{OL} and V_{OH} for V_{DD_PX} = 1.8 V or 2.6 V

Note:

1. Please see Table 2-2 for maximum drive strength for appropriate voltage range.

V_{OL} and V_{OH} are linear functions for the amount of drive strength used, as shown in Figure 3-1. They can also be calculated using the following equations:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100} \right) mV$$

3.1.5 Power consumption characteristics

3.1.5.1 Average current consumption (profile data in different modes)

These values are an estimation of operating currents for the nominal VDD_C and VDD_P voltages of 1.8V and 2.6 V. The operating currents for VDD_A are shown separately. This information should be used as a general guideline for system design. CDMA modes assume that the subscriber unit is operating in compliance with the CDMA specifications of IS-95-B. FM modes assume that the subscriber unit is operating in compliance with the AMPS specifications of IS-95-A.

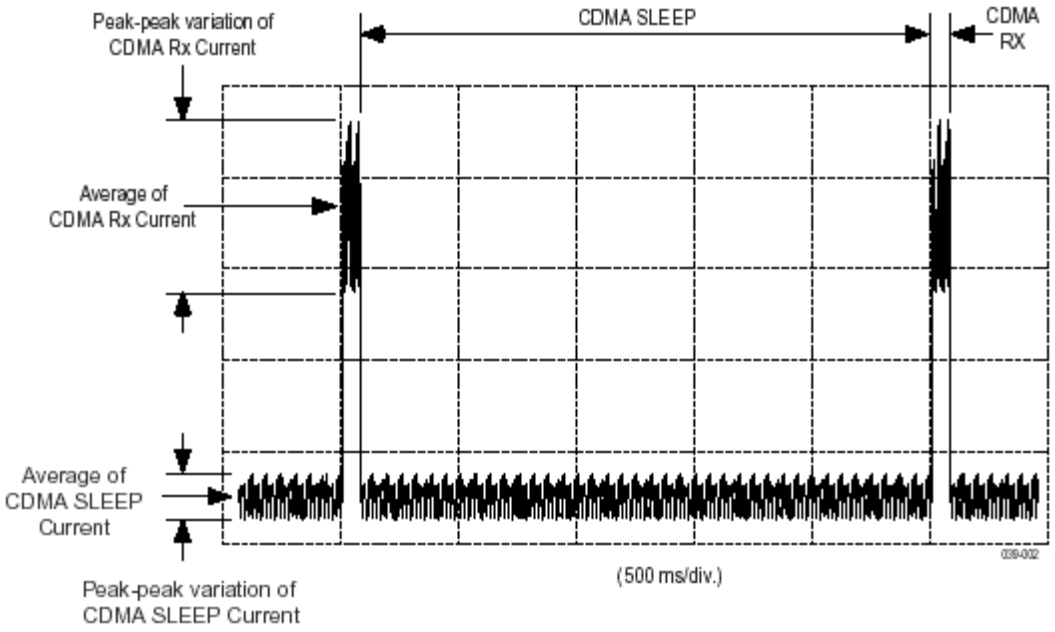

Figure 3-2 Power supply current versus time in slotted paging mode

Table 3-6 Power supply current (typical)

Operating Mode	Digital	Analog	VDD_P1 & VDD_P2	VDD_P3	Units	Notes
	1.4 V	2.60 V	1.9 V	2.6 V		
CDMA Rx/Tx Voice	TBD	30.2	1.2	5.4	mA	1, 2
CDMA Rx/Tx Data	94.1	13.4	1.4	3.9	mA	1,3
CDMA Rx idle	89.6	11.7	1.8	2.7	mA	1
CDMA Sleep	250	35.9	18.6	145.7	µA	1,4,7
EVDO Rx/Tx Data	134.8	16.6	0.7	5.2	mA	1,5
EVDO Rx Data	134.8	16.1	0.7	5.3	mA	1
EVDO Rx idle	121.8	14.1	1.4	3.9	mA	1
EVDO Sleep	250	35.9	17.7	147.7	µA	1,4,7

Notes:

1. Values shown in this table represent a time average of the observed data from recent testing conducted by QUALCOMM over a limited number of devices at room temperature (25 °C). See Figure 3-2 for illustrations of average power supply current. Measurements are done on a FFA6550 and/or reference design phone with AMSS6550/6150 Release 3.0.
2. CDMA voice measurements were done with EVRC vocoder, UART clock regime off, and transmit level of 10 dBm.
3. CDMA data measurements were done with data rates of 153.6 kbps FL and 153.6 kbps RL.
4. TCXO is disabled.
5. EVDO Rx/Tx measurements were done with data rates of 2.4 Mbps FL and 153.6 kbps RL.
6. EVDO Rx measurements were done with a data rate of 2.4 Mbps FL.
7. Typical average Sleep Core Current in this table is at 25°C ambient temperature. Maximum average sleep current on the core for any given part at 25°C ambient temperature is 600 µA.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.1.6 Power sequencing

3.1.6.1 Power-up recommendations

QUALCOMM's power management IC PM6650 includes power-on circuits that provide the power sequencing for the MSM6550/MSM6150 chipsets. The recommended power-up sequence is VREG_MSMC -> VREG_MSME and VREG_MSMP -> VREG_MSMA

NOTE This is described in the PM6650 Power Management IC User Guide 80-V5773-7.

3.1.6.2 Justification

- Sequence
  a. Core voltage needs to come up first so that internal circuits can take control of the IO(s) and Pads.
  b. If the Pad_voltage comes on first, there may be large leakage due to the large driver transistors and the output drivers being stuck in unknown states, until Core_vdd comes on.
  c. Pad_voltage needs to precede analog voltage as SBI is initialized to default before Analog_voltage comes up. (Note: Analog section is controlled by SBI.)
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when Core_VDD reaches 90% of its value, the next domain can start ramping up.
- The power down sequence is the opposite of power up.

3.2 Timing characteristics

3.2.1 Timing diagrams

The timing diagrams illustrate the signals on the external bus as a function of time, as measured by the AHB bus clock (HCLK). Throughout this chapter, the term *HCLK* refers to the AHB bus-clock cycle and refers to **T,** unless otherwise specified. A clock extends from one rising HCLK edge to the next rising HCLK edge. For each signal in the timing diagrams, the high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state. When both the high and low levels are shown, the meaning depends on the signal. A single signal indicates 'don't care'. In the case of bus activity, if both high and low levels are shown, it indicates that the processor or external interface is driving a value, but that this value may or may not be valid.

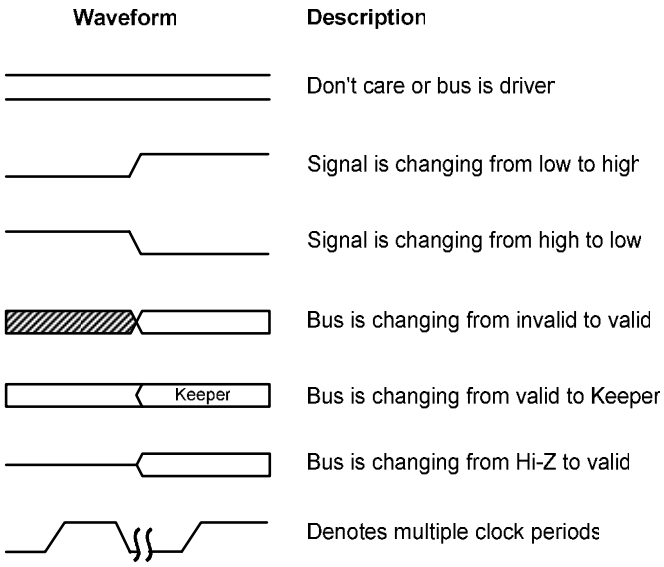

Figure 3-3 Timing diagram waveforms

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.2.2 Rise and fall time

The tester that characterized the MSM6550/MSM6150 device has an actively terminated load. This makes rise and fall transitions quicker (essentially mimicking a no-load condition). ***For this reason, the bus rise or fall time must be added to parameters that start timing at the MSM6550/MSM6150 device and terminate at the memory device.*** One of these parameters is the chip select to data valid on a read cycle. An example of this is **t**(csdv) in EBI2 asynchronous memory timing. Table 3-7 shows the capacitive load de-rating factor for EBI1 and EBI2.

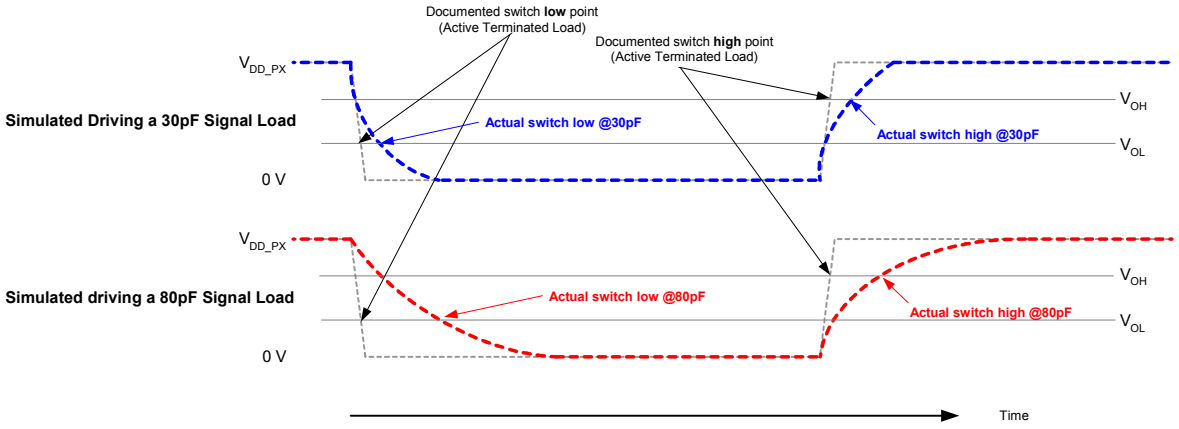

Figure 3-4 Rise and fall time in different load conditions

Table 3-7 Capacitive load de-rating factor

Symbol	EBI 1	EBI 2		Units	Notes
	Max @ 5mA Drive Strength (Pad Voltage 1.8V)	Max @ 2.5mA Drive Strength (Pad Voltage =1.8V)	Max @5mA Drive Strength (Pad Voltage =2.6V)		
t(r) (0-65%)	0.094	0.179	0.115	ns/pF	
t(r) (0-90%)	0.165	0.302	0.202	ns/pF	
t(f) (100-35%)	0.088	0.201	0.128	ns/pF	
t(f)(100-10%)	0.143	0.328	0.218	ns/pF	

3.2.3 Top-level description of pad design methodology

The MSM6550/MSM6150 device uses generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DD_PX} supply. The input switch point for pure input-only pads is designed to be $V_{DD\_PX}/2$ (or 50% of V_{DD_PX}). The documented switch-points (guaranteed over worst-case process/voltage/temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

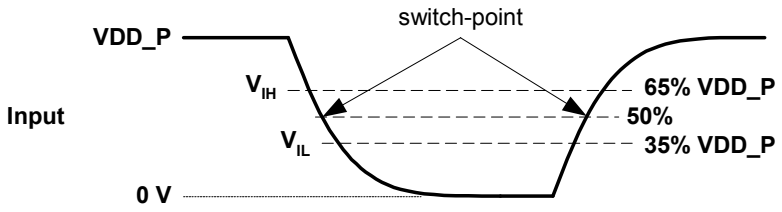

Figure 3-5 MSM6550/MSM6150 input signals DC characteristics

Outputs (e.g., address, chip selects, and clocks) are designed and characterized to source or sink a large (several mA) DC output at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures are essentially CMOS drivers with a possible small amount of worst-case IR loss in the pad ($\leq$50 mV estimate under worst-case conditions), under *zero DC load* the actual output high voltage will *approximate* V_{DD_PX} ─ 50 mV or more, and the actual output low voltage will *approximate* 50 mV or less.

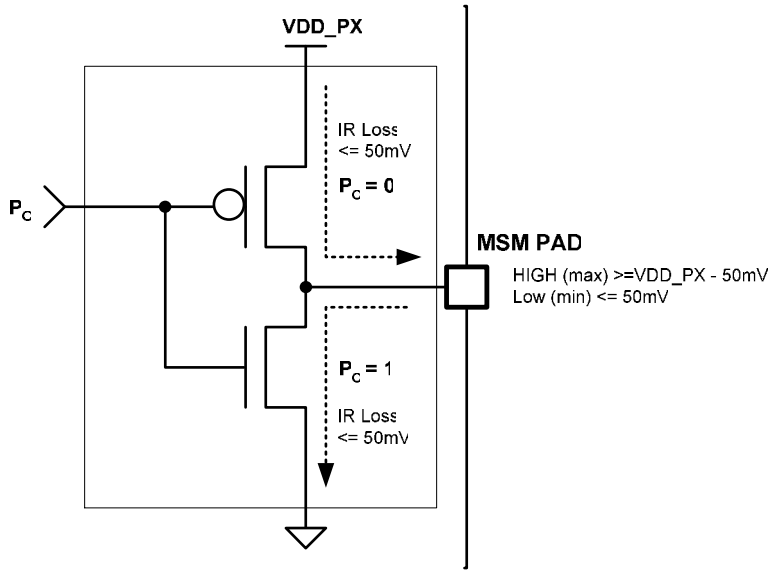

Figure 3-6 MSM6550/MSM6150 output PAD equivalent circuit

You can *approximate* the DC output drive strength between V_{OH} (min) and V_{DD_PX} ─ 50mV, and between V_{OL} (max) and 50 mV, by doing a linear interpolation between these endpoints. For example, an output pad driving low which guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) ─ 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) ─ 50 mV]; and an output pad driving high which guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_PX} ─ 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output transfer voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking Isc (sc=short-circuit) of current, where the magnitude of Isc is larger than the current capability at the driven/intended V_{OH} (min) and V_{OL}(max) output logic levels.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Since the target application includes a radio, output pads are designed such that output slew rates are *minimized*. Decreased slew rates limit high-frequency spectral components emitting from the signaling. Such high-frequency spectral components tend to desensitize the companion radio.

For an output driver, the signal rise time (**t**(r)) or fall time (**t**(f)) is a function of the phone board loading. MSM6550/MSM6150 device EBI1 loading should be on the order of 20 pF (or less for a phone design with a single external memory device) up to around 30 pF of lumped loading (making the assumption that phone designs have tight geometries and layout, and that the memory subsystem may still be treated as a lumped model load as opposed to a transmission line load). It is *strongly* recommended that EBI1 phone board loading is limited to 30 pF or less.[1]

Bidirectional pins (e.g., microprocessor databus) include both input and output pad structures, and behave accordingly when utilized as inputs or outputs within a system. Both input and output behaviors are described above.

In addition to being bidirectional, databus pins also include pad keepers. These keepers are weak flip-flops (easily over-driven by an external source) on the pad-side of the structure to encourage an otherwise-undriven pad voltage to migrate to a power or ground rail, either to help ensure hold-time requirements or to minimize power consumption within otherwise undriven pad structures. Keepers have the following impacts on the physical interface:

- External sources driving these pins must overcome the keepers in order to drive a logic level on such pins. The amount of current required must be greater than the *maximum* I_{OZLKP} value in Table 3-4.
- At the point when an external source releases control of such pins, the keepers tend to hold the last logic level on the pins (subject to system-level leakages and capacitive loading effects). The *minimum* I_{OZLKP} current values may be sustained indefinitely without upsetting the state of the keeper.

[1] Memory vendors intending to support these products are encouraged to provide accurate timing information for the capacitive load levels. For example, in the MSM6550/MSM6150 devices EBI1 operation, vendors should consider providing timing values for 10 pF, 20 pF, 30 pF, and 40 pF loading; or should provide an accurate and reasonable means of calculating/de-rating the timing parameters for the corresponding load levels.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.2.4 Clocks

3.2.4.1 TCXO timing

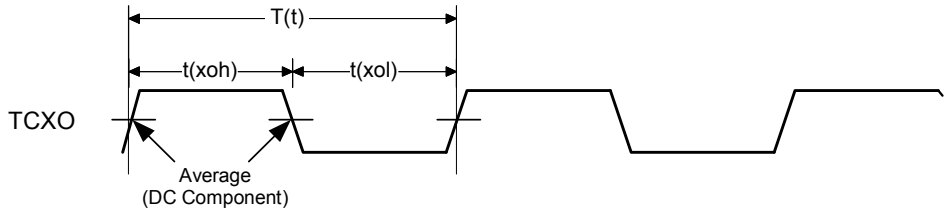

Figure 3-7 TCXO timing parameters

Table 3-8 TCXO timing parameters

Symbol	Parameter	Min	Typ	Max	Units
t(xoh)	TCXO logic high	TBD	—	TBD	ns
t(xol)	TCXO logic low	TBD	—	TBD	ns
T(t)	TCXO clock period	—	52.083	—	ns
1/T(t)	Frequency (19.2 MHz must be used.)	—	19.2	—	MHz

3.2.4.2 HCLK and MCLK timing and jitter

Table 3-9 HCLK and MCLK timing parameters

Symbol	Parameter	Min	Max	Units
HCLK	AHB clock period	1, 2	—	ns
MCLK	ARM microprocessor clock period	2, 3	—	Ns

Notes:

1. The maximum HCLK frequency supported is the maximum frequency defined by the latest of AMSS6550/AMSS6150 software.
2. The maximum MCLK frequency supported is the maximum frequency defined by the latest of AMSS6550/AMSS6150 software
3. HCLK and MCLK are MSM6550/MSM6150 internal clock signals.

The maximum HCLK frequency supported is the maximum frequency defined by the latest release of the AMSS6550/AMSS6150 software. HCLK is a fractional multiple of the TCXO frequency created by the TCXO PLL. The control of this circuitry is determined by feature #defines within the AMSS6550/AMSS6150 code. Do not alter the PLL configuration within these #defines. QCT tests the MSM6550/MSM6150 device and the latest release of the system software to verify operation.

The MSM6550/MSM6150 device has some HCLK jitter due to PLL jitter and the divider circuitry. This jitter affects all timing parameters that use the HCLK **T**, and must be added to or

subtracted from measured timing values, as appropriate. Jitter is not included in any of the values listed in the following sections.

Table 3-10 HCLK clock period

HCLK Frequency	T (cycle)		High Pulse		Low Pulse		Units
	Min	Max	Min	Max	Min	Max	
73.3824 MHz	12.6	14.8	TBD	TBD	TBD	TBD	ns
48.9216 MHz	18.9	22.2	TBD	TBD	TBD	TBD	ns

SDRAM clock for T = 13.63 ns (73.3824 MHz)

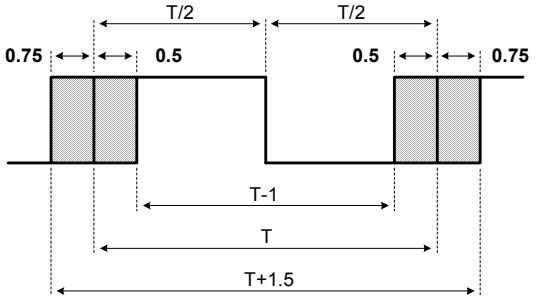

Figure 3-8 SDRAM clock for T = 13.63 ns

SDRAM clock for T = 20.44 ns (48.9216 MHz)

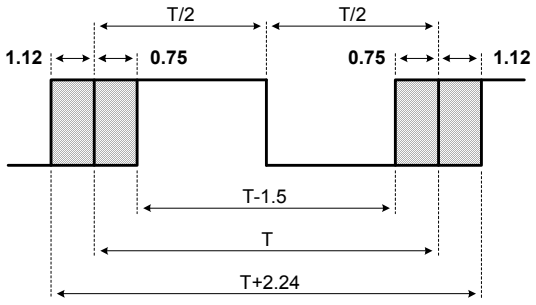

Figure 3-9 SDRAM clock for T = 20.44 ns

3.3 EBI1 timing requirements

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse and hold time numbers may get better.

3.3.1 Asynchronous 16-bit memory read and write

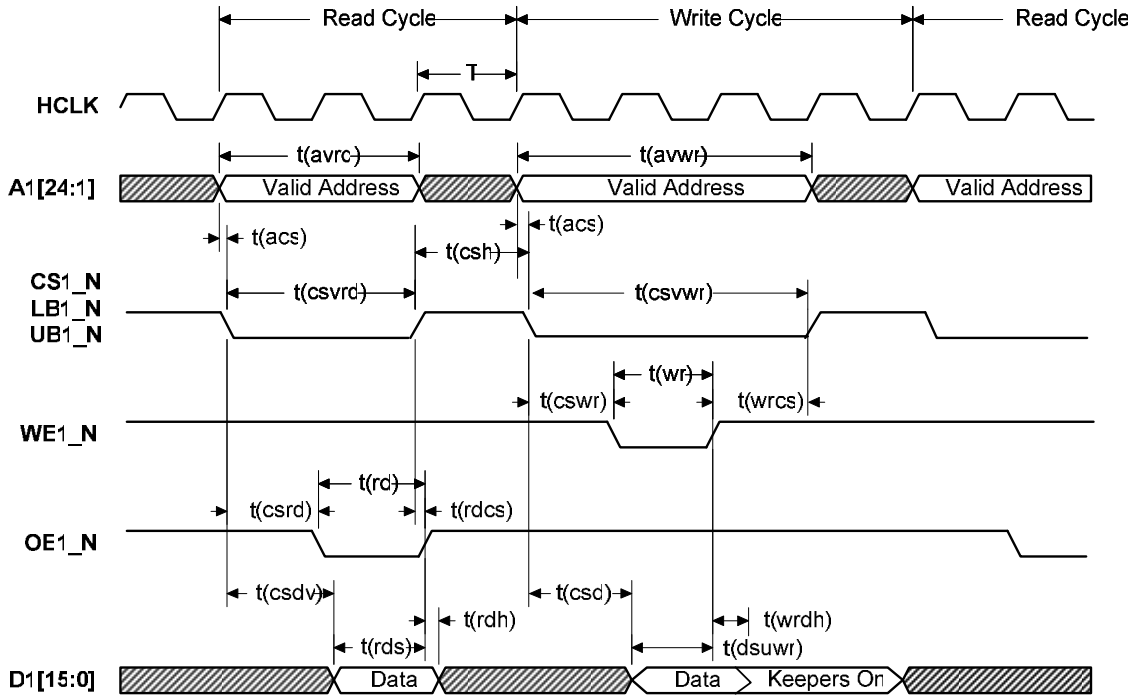

Figure 3-10 Asynchronous 16-bit read-write accesses

Table 3-11 EBI1 asynchronous 16-bit access timing

Symbol	Description	Min	Max	Units	Notes
		Write Cycle			
t(acs)	Address valid to chip select active	rT–2	—	ns	4
t(csvwr)	Write cycle chip select active	(3+w+d+h)T-1	—	ns	1, 2, 3
t(cswr)	Chip select active to write active	T–1	—	ns	
t(csd)	Chip select active to data valid	T–2	—	ns	1, 2
t(wr)	Write active	(1+w+d)T–0	—	ns	1, 2
t(wrcs)	Write inactive to chip select inactive	(1+h)T-1	—	ns	3
t(avwr)	Write cycle address valid	(3+w+d+r+h)T–1	—	ns	1, 2, 3, 4
t(dsuwr)	Write cycle data setup	(1+w+d)T–0	—	ns	1, 2
t(wrdh)	Write data hold	0	—	ns	5

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Symbol	Description	Min	Max	Units	Notes
Read Cycle					
t(acs)	Address valid to chip select active	rT–2	—	ns	4
t(avrd)	Read cycle address valid	(2+w+r+d)T–1	—	ns	1, 2, 4
t(rd)	Read active	(1+w+d)T–0	—	ns	1, 2
t(csvrd)	Read cycle chip select active	(2+w+d)T–1	—	ns	1, 2
t(csrd)	Chip select active to read active	T–1	–	ns	
t(csh)	Chip select inactive	rT– TBD	–	ns	
t(csdv)	Chip select active to data valid	–	(2+w+d)T–12	ns	1, 2
t(rdcs)	Read inactive to chip select inactive	0	—	ns	
t(rdh)	Read data hold	0	—	ns	
t(rds)	Read data setup	13	—	ns	

Notes:

T=HCLK cycle

1. w: (EBI1_CSn_CFG0[7:4]) = write wait, w: (EBI1_CSn_CFG0[3:0]) = read wait
2. d: (EBI1_CSn_CFG0[15:12]) – 1 = delta write, d: (EBI1_CSn_CFG0[11:8]) – 1 = delta read
3. h: (EBI1_CSn_CFG0[19:16]) – 1 = hold wait
4. r: EBI1_CSm_CFG0[23:20] = recovery wait, where m denotes the chip select from the previous access. Recovery cycles are only inserted under certain circumstances as described in the MSM Software Interface document. Precharge cycles and AVD recovery cycles may also impact the chip-select high time as described in the MSM Software Interface document.
5. Keepers can continue to hold data value depending on bus leakage.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.2 Asynchronous bus-sized read-write access to 16-bit memory

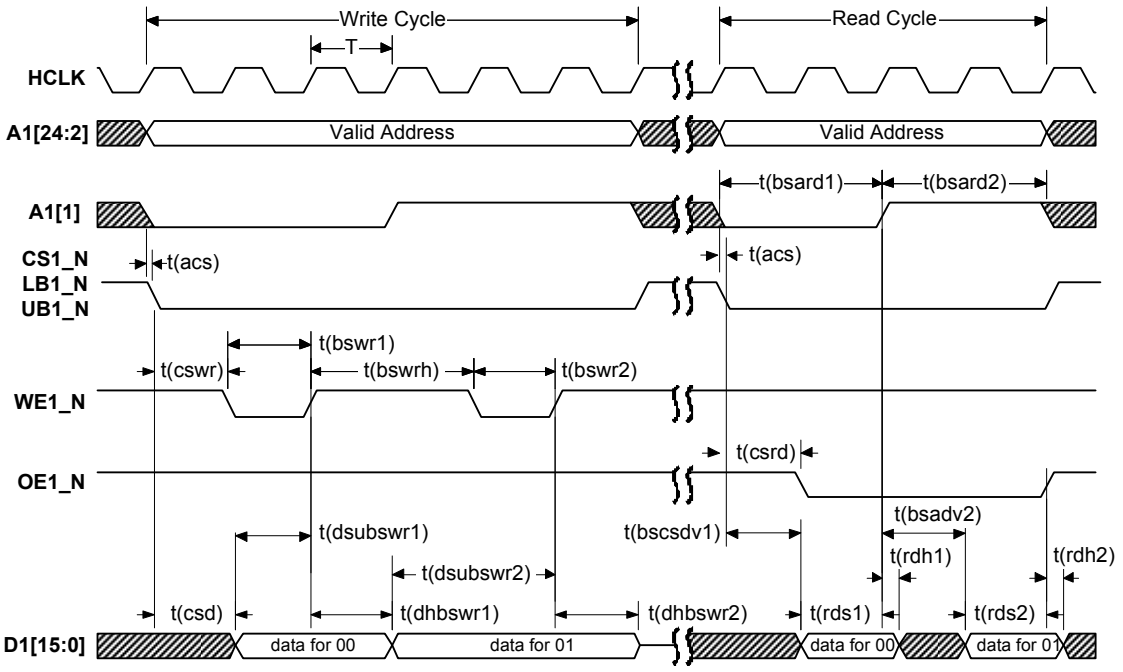

Figure 3-11 Asynchronous bus-sized access to 16-bit memory

Table 3-12 EBI1 asynchronous bus-sized access timing

Symbol	Description	Min	Max	Units	Notes
Write Cycle					
t(acs)	Address valid to chip select active	rT–2	–	ns	4
t(cswr)	Chip select active to write active	T–1	–	ns	
t(bswr1)	1st write active	(1+d+w)T–0	–	ns	1,2
t(bswr2)	2nd write active	(1+d+w)T–0	–	ns	1
t(bswrh)	Write inactive	(2+h)T–1	–	ns	3
t(dsubswr1)	Bus-sized 1st write data setup	(1+d+w)T–0	–	ns	1,2
t(dhbswr1)	Bus-sized 1st data hold	(1+h)T–0	–	ns	3
t(dsubswr2)	Bus-sized 2nd write data setup	(2+d+w)T–1	–	ns	1,2
t(dhbswr2)	Bus-sized 2nd data hold time	0	–	ns	5
t(csd)	Chip select active to data valid	T–2	–	ns	1,2
Read Cycle					
t(acs)	Address valid to chip select active	rT–2	–	ns	4

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Symbol	Description	Min	Max	Units	Notes
t(bsard1)	Address valid to end of 1st read	(2+d+w+r)T–2	–	ns	1,2,4
t(bsard2)	Address valid to end of 2nd read	(2+d+w)T–0	–	ns	1,2
t(csrd)	Chip select active to 1st read active	T–1	–	ns	
t(rds1)	Bus-sized read data setup for the 1st read	8	–	ns	
t(rdh1)	Bus-sized read data hold for the 1st read	0	–	ns	
t(rds2)	Bus-sized read data setup for the 2nd read	13	–	ns	
t(rdh2)	Bus-sized read data hold for the 2nd read	0	–	ns	
t(bscsdv1)	Chip select active to 1st data valid	–	(2+d+w)T–12	ns	1,2
t(bsadv2)	Address valid to 2nd data valid	–	(2+d+w)T–12	ns	1,2

Notes:

T=HCLK cycle

1. w: (EBI1_CSn_CFG0[7:4]) = write wait, w: (EBI1_CSn_CFG0[3:0]) = read wait
2. d: (EBI1_CSn_CFG0[15:12]) – 1 = delta write, d: (EBI1_CSn_CFG0[11:8]) – 1 = delta read
3. h: (EBI1_CSn_CFG0[19:16]) – 1 = hold wait
4. r: EBI1_CSm_CFG0[23:20] = recovery wait, where m denotes the chip select from the previous access. Recovery cycles are only inserted under certain circumstances as described in the MSM Software Interface document.
5. Keepers can continue to hold data value depending on bus leakage.

3.3.3 Asynchronous page-mode memory accesses

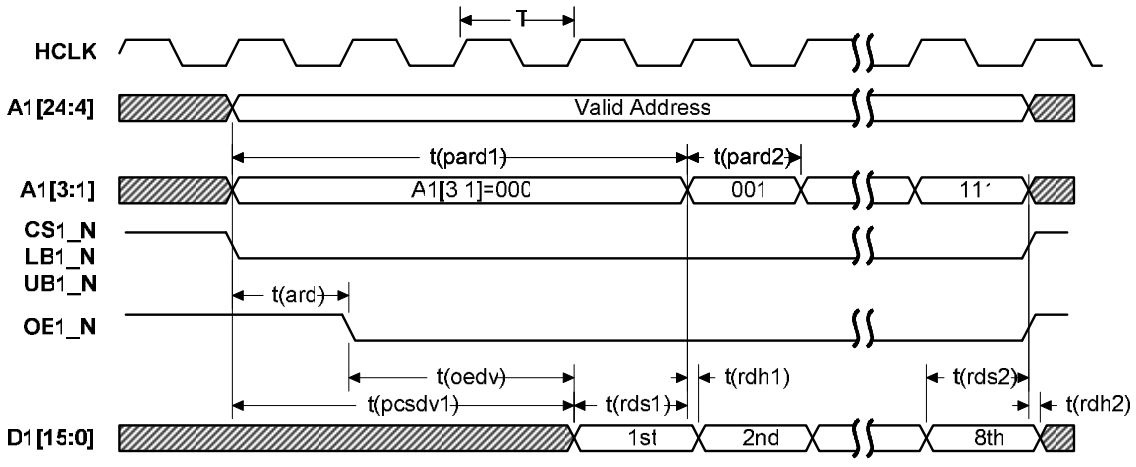

Figure 3-12 Page mode 4-1-1-1 read access [4-WORD]

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

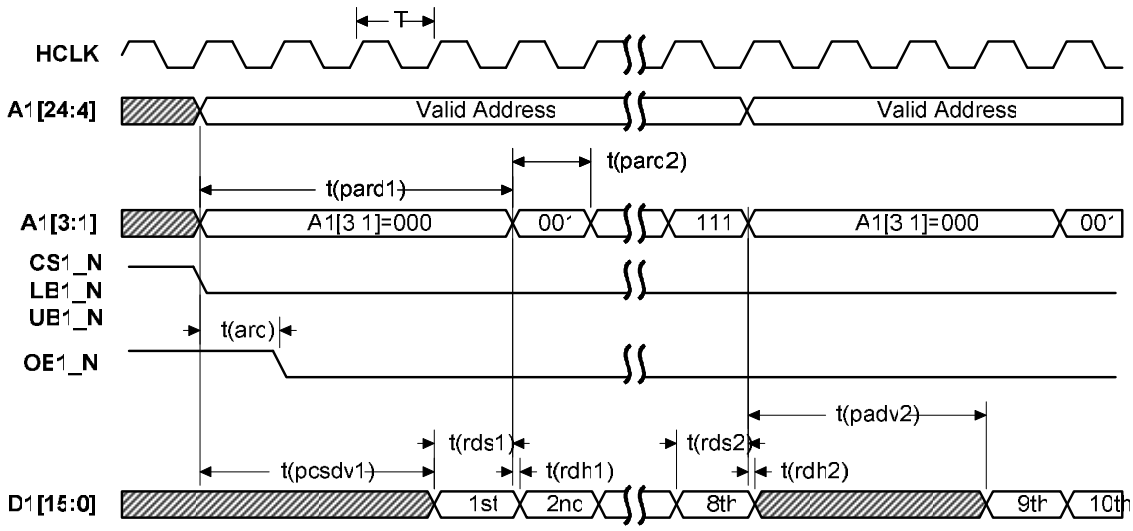

Figure 3-13 Page mode 4-1-1-1 read access [8-WORD]

Table 3-13 Page mode access timing

Symbol	Description	Formula	D		Units	Notes
			Min	Max		
Page-mode read cycle						
t(acs)	Address valid to chip select active	rT–D	TBD	–	ns	4
t(pard1)	1st read cycle address valid	(4+d+w+r)T–D	TBD	–	ns	1, 2, 3, 4
t(pard2)	Consecutive read cycle address valid	(1+w)T–D	TBD	–	ns	1
t(rds1)	1st read data setup	D	TBD	–	ns	
t(rdh1)	1st read data hold	D	TBD	–	ns	
t(rds2)	consecutive read data setup	D	TBD	–	ns	
t(ard)	Address valid to read active	T + D	TBD	–	ns	
t(rdh2)	consecutive read data hold	D	TBD	–	ns	
t(pcsdv1)	Chip select to 1st read data valid	(4+d+w)T–D	–	TBD	ns	1, 2, 4
t(padv2)	2nd 4 word Address to 1st data valid	(4+d+w)T–D	–	TBD	ns	1, 2, 4

Notes:
1. w: (EBI1_CSn_CFG0[7:4]) = write wait, w: (EBI1_CSn_CFG0[3:0]) = read wait
2. d: (EBI1_CSn_CFG0[15:12]) – 1 = delta write, d: (EBI1_CSn_CFG0[11:8]) – 1 = delta read
3. h: (EBI1_CSn_CFG0[19:16]) – 1 = hold wait
4. r: EBI1_CSm_CFG0[23:20] = recovery wait, where m denotes the chip select from the previous access. Recovery cycles are only inserted under certain circumstances as described in the MSM Software Interface document.

3.3.4 SDRAM and burst timing

MSM device configuration:

For any timing analysis, the measurement point for all signals is $V_{IH(min)}$ or $V_{IL(max)}$ (for rising or falling edges, respectively).

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

All output timing parameters represent the point of the output signal transition (additional delays due to signal rise/fall times for a specific bus load have to be accounted for).

3.3.4.1 SDRAM timing

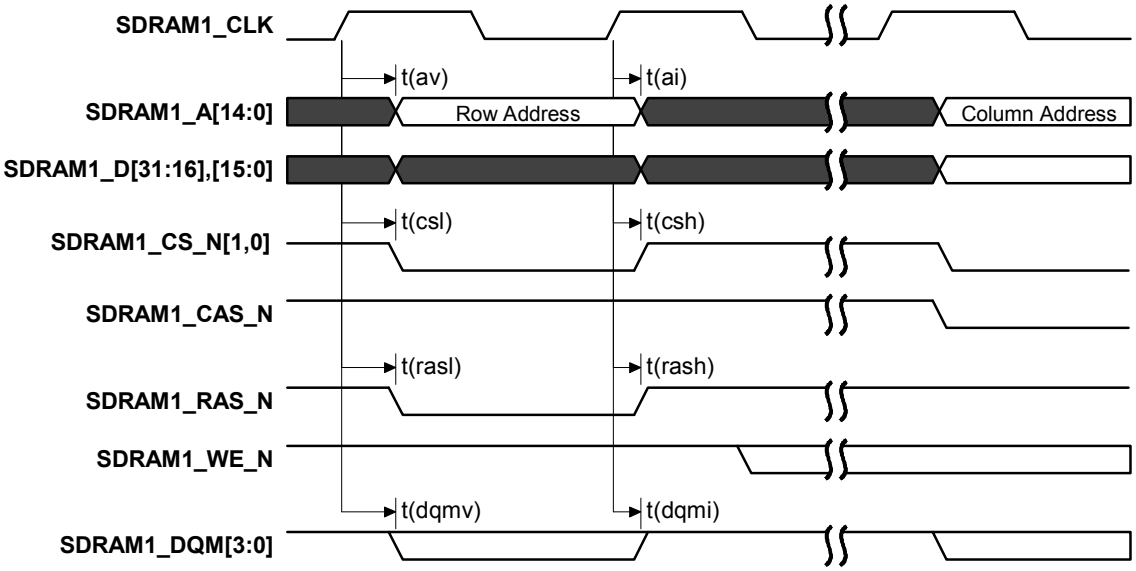

Figure 3-14 SDRAM RAS timing

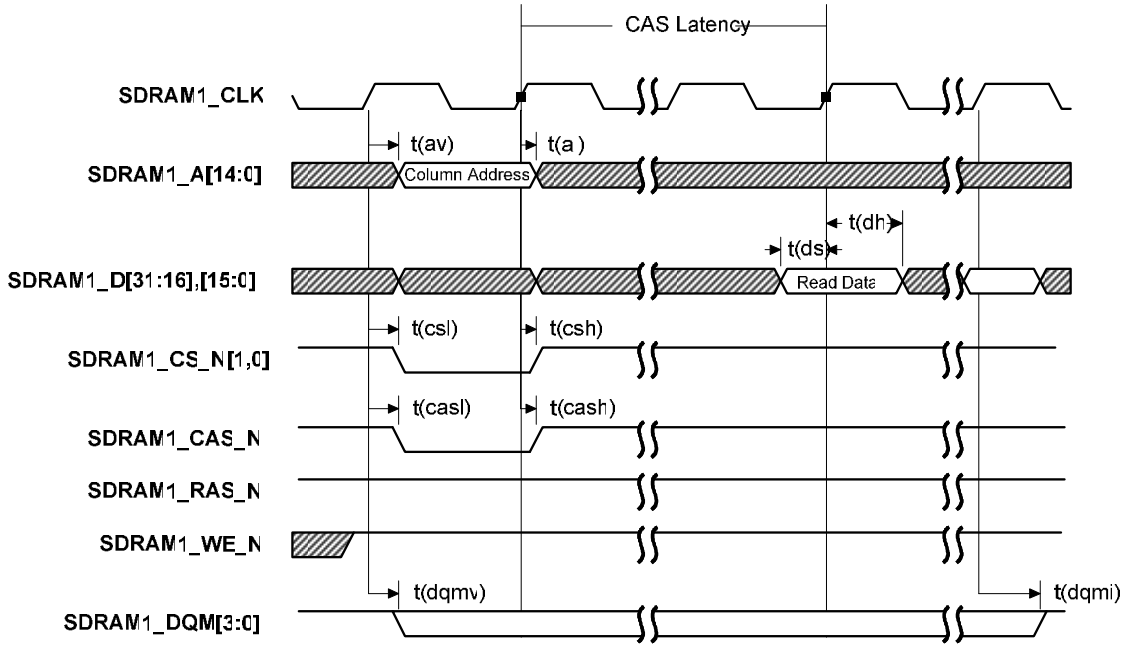

Figure 3-15 SDRAM read timing

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

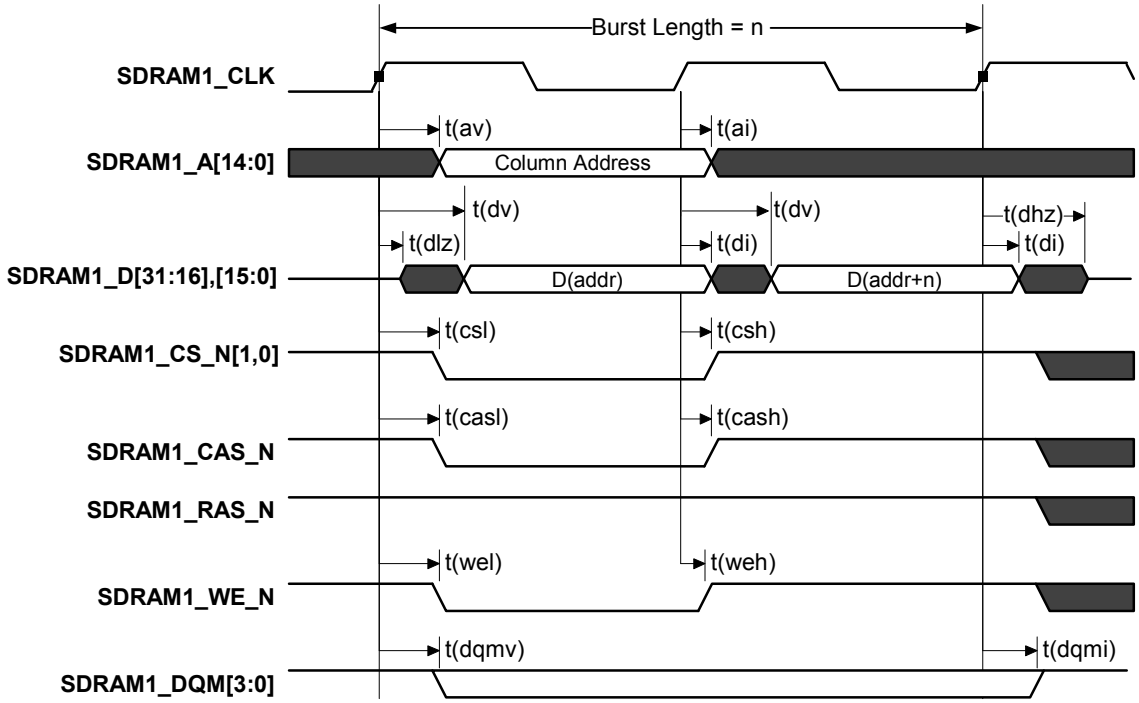

Figure 3-16 SDRAM write timing

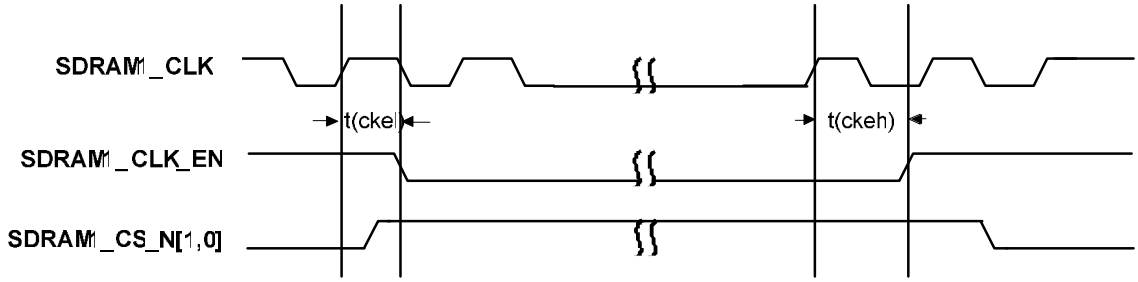

Figure 3-17 SDRAM clock gating: (MPMCDynamicReadConfig[1:0] = "01")

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-14 SDRAM controller timing

Symbol	Description	Min	Max	Unit	Note
t(av)	Clock to address valid	—	6	ns	1, 2
t(ai)	Clock to address invalid	1	—	ns	1, 2
t(csl)	Clock to chip-select low	—	6	ns	1, 2
t(csh)	Clock to chip-select high	1	—	ns	1, 2
t(rasl)	Clock to RAS low	—	6	ns	1, 2
t(rash)	Clock to RAS high	1	—	ns	1, 2
t(casl)	Clock to CAS low	—	6	ns	1, 2
t(cash)	Clock to CAS high	1	—	ns	1, 2
t(dqmv)	Clock to DQM valid	—	6	ns	1, 2
t(dqmi)	Clock to DQM invalid	1	—	ns	1, 2
t(ckel)	Clock to enable low	—	6	ns	1, 2
t(ckeh)	Clock to enable high	1	—	ns	1, 2
Read Cycle					
t(ds)	Read data setup time	2	—	ns	3
t(dh)	Read data hold time	2	—	ns	3
Write Cycle					
t(dv)	Clock to data valid	—	6	ns	1
t(di)	Clock to data invalid	1.5	—	ns	1
t(dlz)	Clock to data bus in low impedance	0.5	—	ns	1
t(dhz)	Clock to data bus in high impedance	—	5	ns	1
t(wel)	Clock to write enable low	—	6	ns	1
t(weh)	Clock to write enable high	1	—	ns	1

Notes:
1. This parameter is an MSM device output driving an external device input.
2. This parameter is common to both read and write.
3. This parameter is an external device output driving an MSM device input.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.4.2 Burst memory interface (CMD_DELAY_ENA=0)

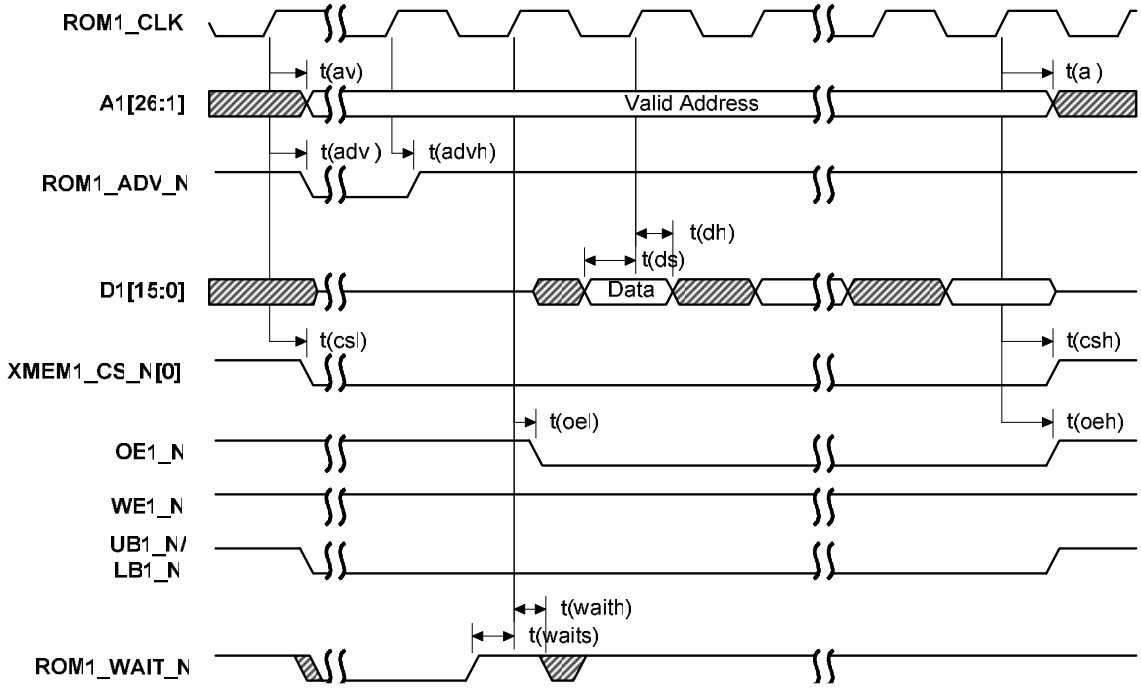

Figure 3-18 Burst memory read timing diagram, 16-bit

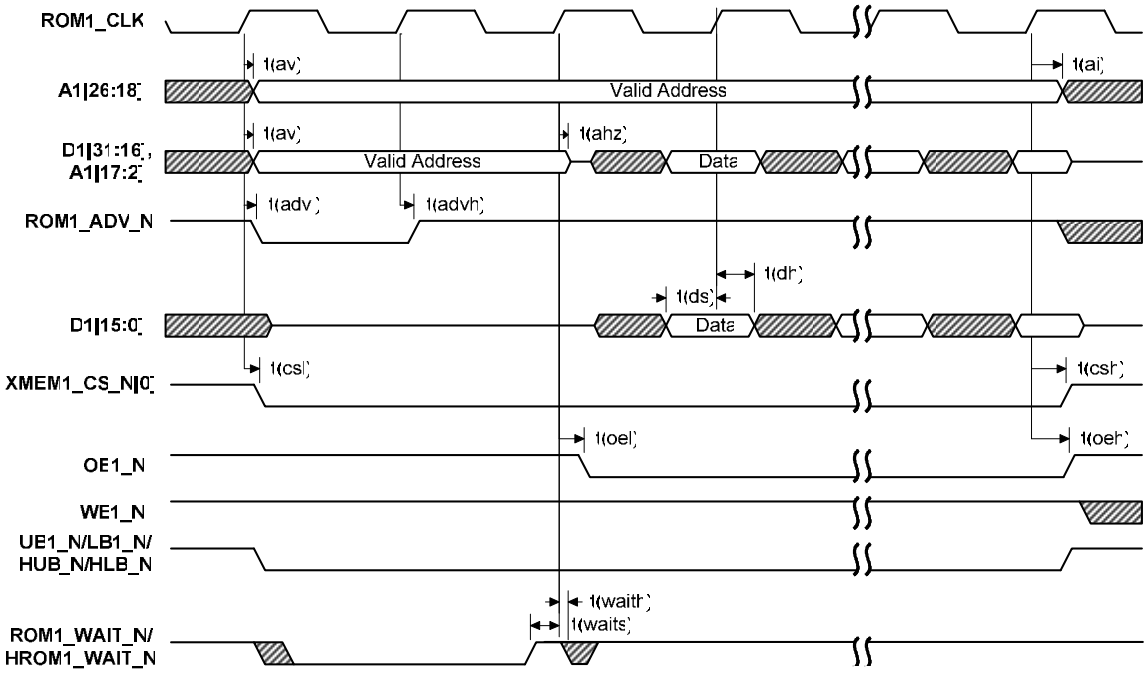

Figure 3-19 Burst memory read timing diagram, 32-bit

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

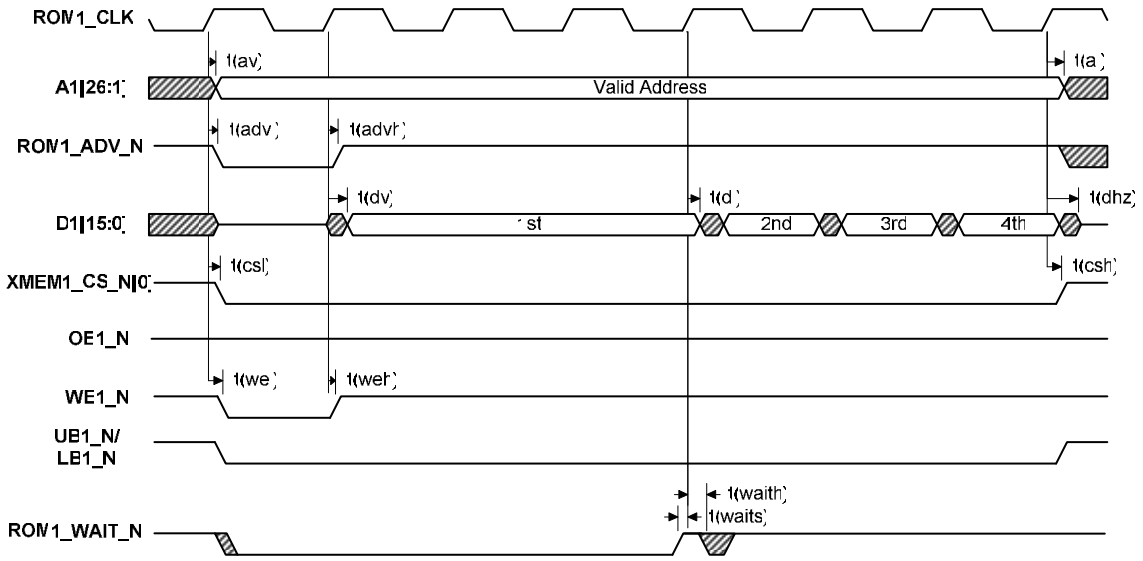

Figure 3-20 Burst memory write timing diagram, 16-bit

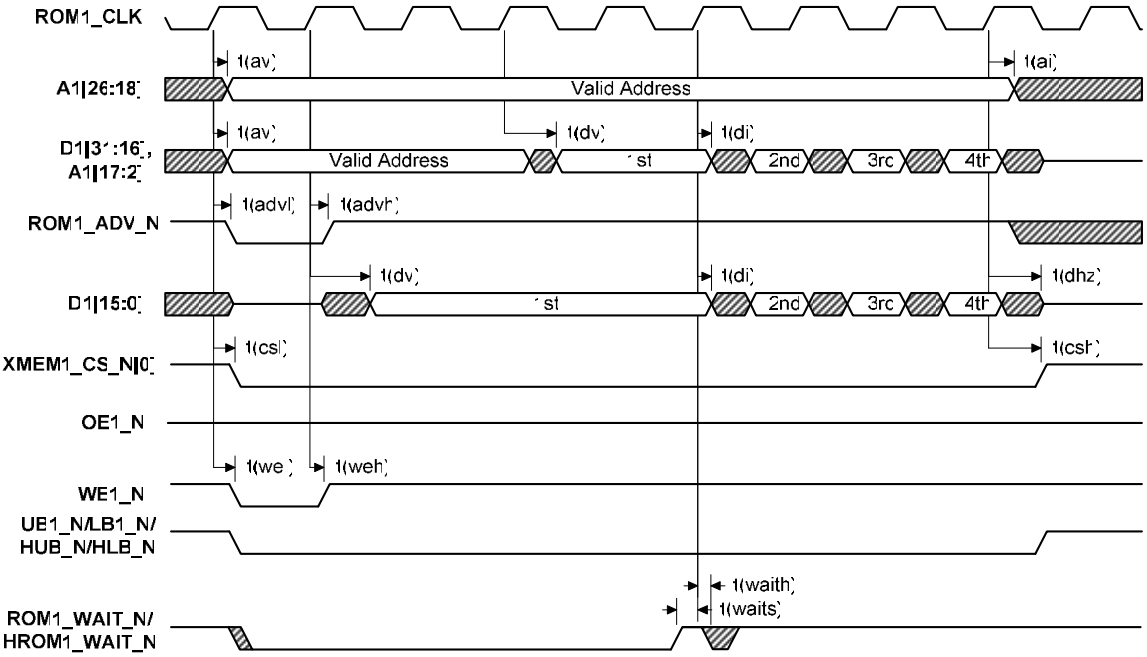

Figure 3-21 Burst memory write timing diagram, 32-bit

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-15 Burst memory controller timing (CMD_DELAY_EN =0)

Symbol	Description	Min	Max	Unit	Note
t(av)	Clock to address valid	—	3	ns	1, 2
t(ai)	Clock to address invalid	–4	—	ns	1, 2
t(csl)	Clock to chip-select low	—	3	ns	1, 2
t(csh)	Clock to chip-select high	–4	—	ns	1, 2
t(advl)	Clock to ADV# low	—	3	ns	1, 2
t(advh)	Clock to ADV# high	–4	—	ns	1, 2
Read Cycle					
t(oel)	Clock to OE# low	—	3	ns	1, 2
t(oeh)	Clock to OE# high	–4	—	ns	1, 2
t(ds)	Read data setup time	3	—	ns	3
t(dh)	Read data hold time	1	—	ns	3
t(ahz)	Clock to data bus in high impedance	—	5	ns	1
t(waits)	WAIT signal setup time w.r.t. clock	3	—	ns	3
t(waith)	WAIT signal hold time w.r.t. clock	1	—	ns	3
Write Cycle					
t(dv)	Clock to data valid	—	3	ns	1
t(di)	Clock to data invalid	–4	—	ns	1
t(dhz)	Clock to data bus in high impedance	—	5	ns	1
t(wel)	Clock to write enable low	—	3	ns	1
t(weh)	Clock to write enable high	–4	—	ns	1

Notes:
1. This parameter is an MSM device output driving an external device input.
2. This parameter is common to both read and write.
3. This parameter is an external device output driving an MSM device input.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.4.3 Burst memory interface (CMD_DELAY_EN = 1)

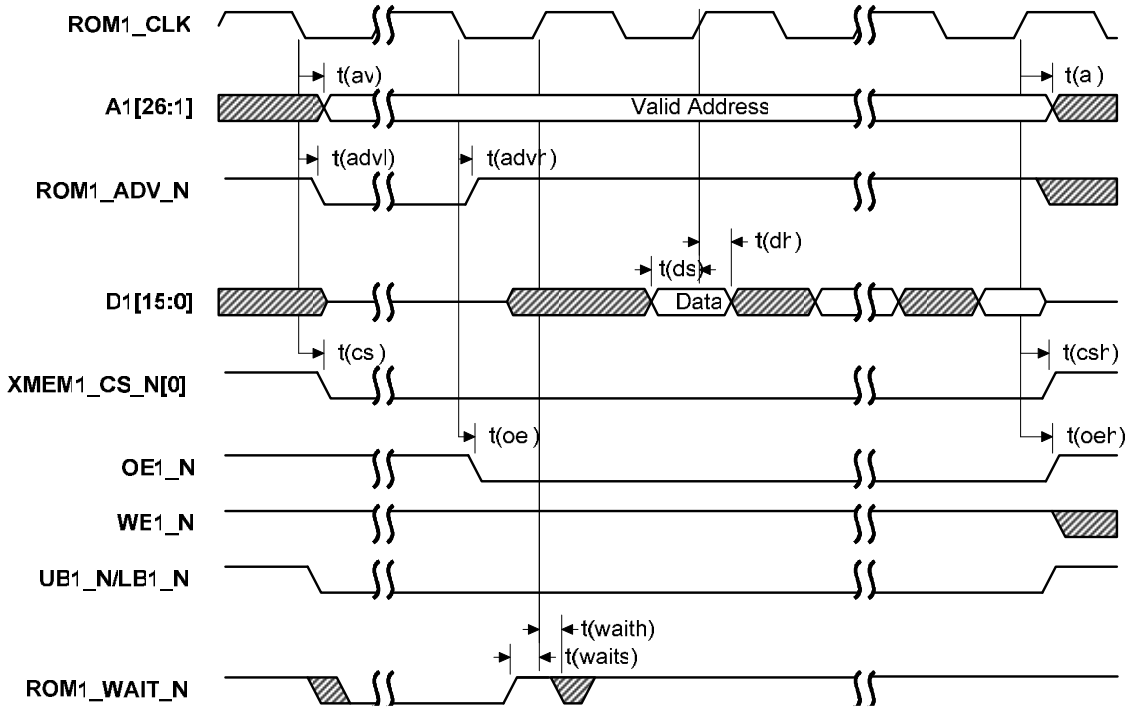

Figure 3-22 Burst read memory, 16-bit

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

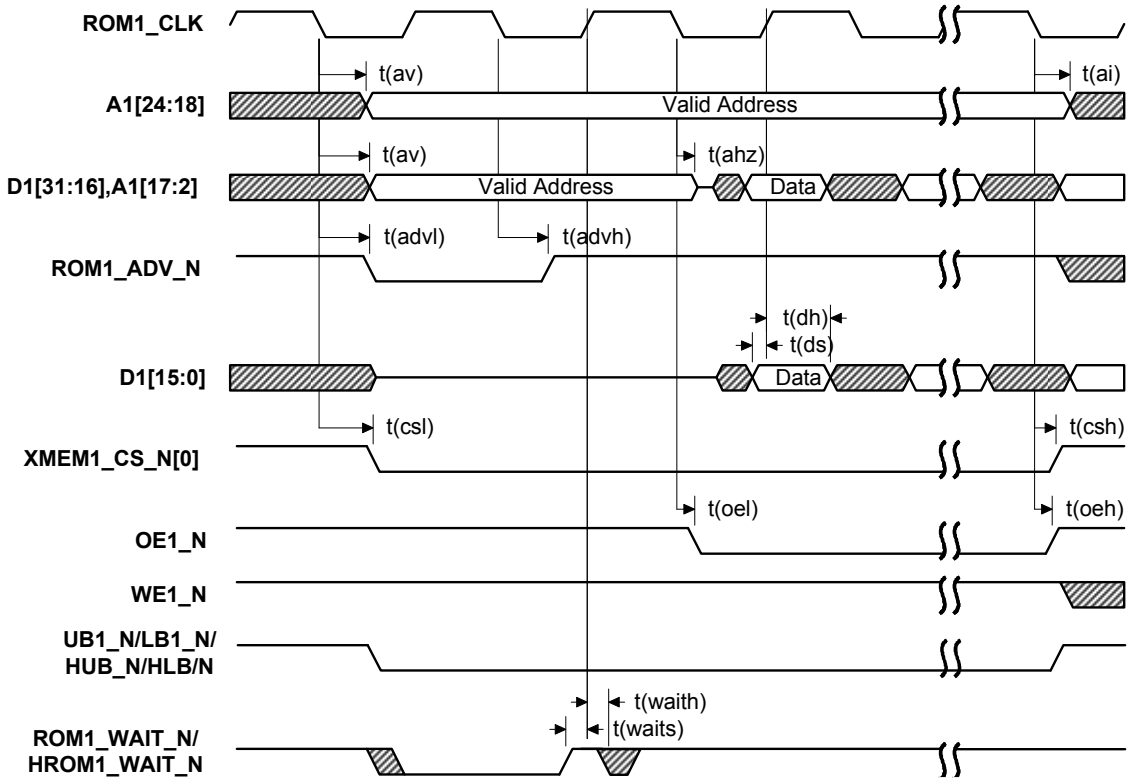

Figure 3-23 Burst read memory, 32-bit

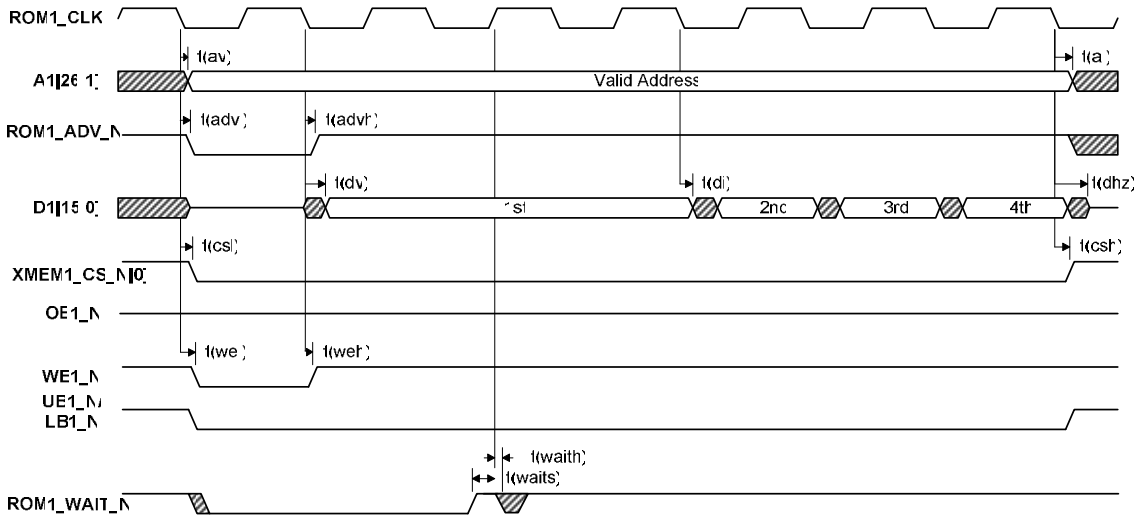

Figure 3-24 Burst write memory, 16-bit

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

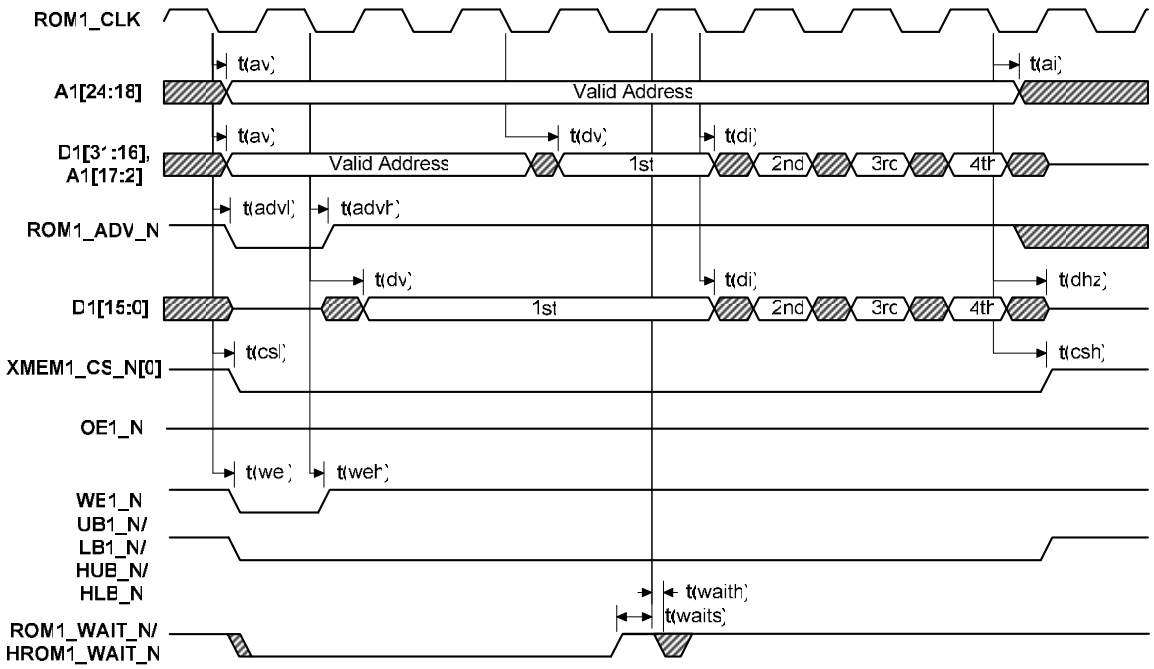

Figure 3-25 Burst write memory, 32-bit

Table 3-16 Burst memory controller timing (CMD_DELAY_EN =1)

Symbol	Description	Min	Max	Unit	Note
t(av)	Clock to address valid	—	6	ns	1, 2
t(ai)	Clock to address invalid	1	—	ns	1, 2
t(csl)	Clock to chip-select low	—	6	ns	1, 2
t(csh)	Clock to chip-select high	1	—	ns	1, 2
t(advl)	Clock to ADV# low	—	6	ns	1, 2
t(advh)	Clock to ADV# high	1	—	ns	1, 2
Read Cycle					
t(oel)	Clock to OE# low	—	6	ns	1, 2
t(oeh)	Clock to OE# high	1	—	ns	1, 2
t(ds)	Read data setup time	2	—	ns	3
t(dh)	Read data hold time	2	—	ns	3
t(ahz)	Clock to data bus in high impedance	—	5	ns	1
t(waits)	WAIT signal setup time w.r.t. clock	2	—	ns	3
t(waith)	WAIT signal hold time w.r.t. clock	2	—	ns	3
Write Cycle					
t(dv)	Clock to data valid	—	6	ns	1
t(di)	Clock to data invalid	1	—	ns	1

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

t(dhz)	Clock to data bus in high impedance	—	5	ns	1
t(wel)	Clock to write enable low	—	6	ns	1
t(weh)	Clock to write enable high	1	—	ns	1

Notes:
1. This parameter is an MSM device output driving an external device input.
2. This parameter is common to both read and write.
3. This parameter is an external device output driving an MSM device input.

3.3.4.4 ROM1_CLK gating for burst mode

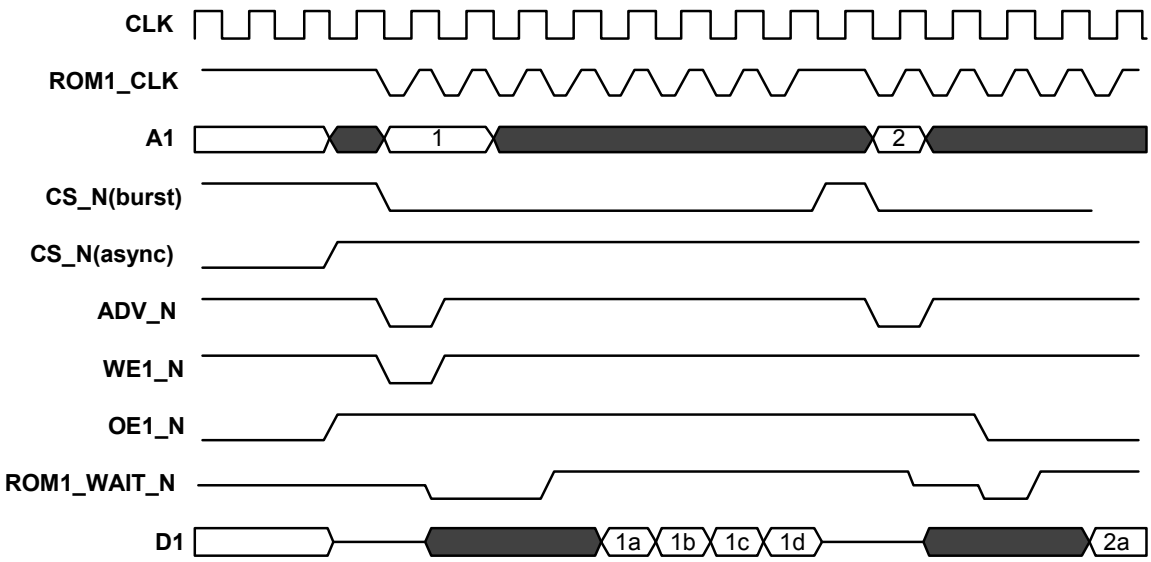

Figure 3-26 Burst memory: EBI1CFG[22] (ROM1_CLK_STATE)=0

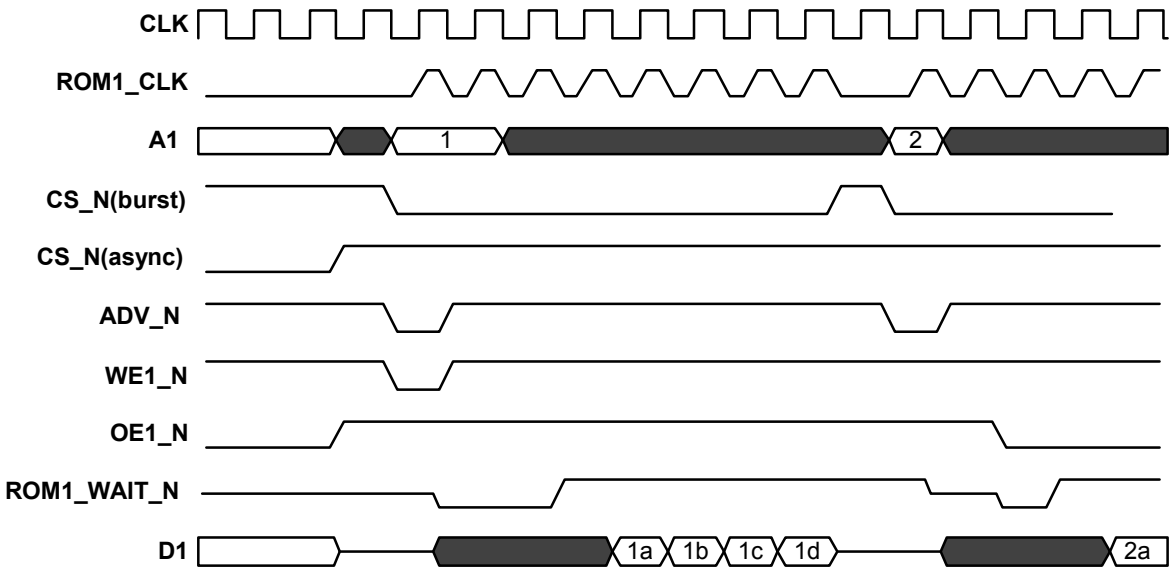

Figure 3-27 Burst memory: EBI1CFG[22] (ROM1_CLK_STATE)=1

3.3.5 EBI2

3.3.5.1 EBI2 asynchronous 16-bit memory read and write

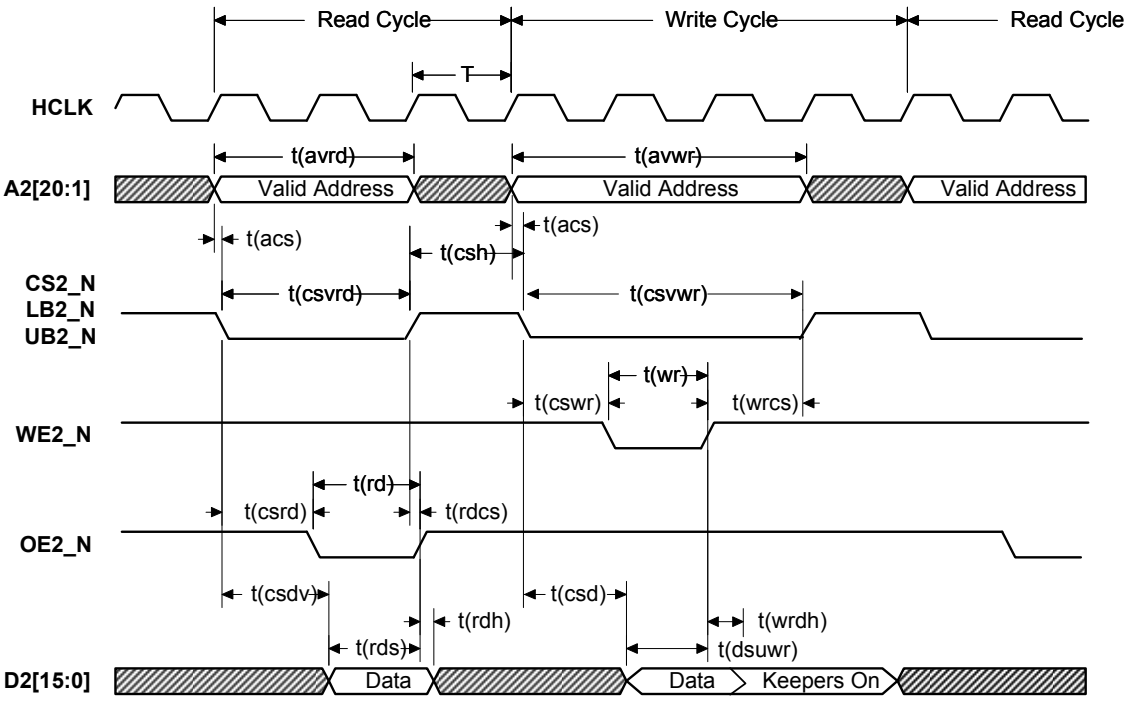

Figure 3-28 Asynchronous 16-bit read-write accesses

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-17 EBI2 asynchronous 16-bit access timing

Symbol	Description	V_{DD_PX} = 1.8 V		V_{DD_PX} = 2.6 V		Units	Notes
		Min	Max	Min	Max		
Write Cycle							
t(acs)	Address valid to chip select active	**rT–2**	–	**rT–2**	–	ns	2
t(csvwr)	Write cycle chip select active	**(3+w+h)T–1**	–	**(3+w+h)T–1**	–	ns	1, 3
t(cswr)	Chip select active to write active	**T–2**	–	**T–2**	–	ns	
t(csd)	Chip select active to data valid	**T–2**	–	**T–2**	–	ns	
t(wr)	Write active	**(1+w)T–0**	–	**(1+w)T–0**	–	ns	1
t(wrcs)	Write active to chip select inactive	**(1+h)T–1**	–	**(1+h)T–1**	–	ns	3
t(avwr)	Write cycle address valid	**(3+w+h+r)T–2**	–	**(3+w+h+r)T–2**	–	ns	1, 2, 3
t(dsuwr)	Write cycle data setup	**(1+w)T–0**	–	**(1+w)T–0**	–	ns	1
t(wrdh)	Write data hold	**0**	–	**0**	–	ns	4
Read Cycle							
t(acs)	Address valid to chip select active	rT–2	–	**rT–2**	–	ns	2
t(avrd)	Read cycle address valid	**(2+w+r)T–1**	–	**(2+w+r)T–1**	–	ns	1, 2
t(rd)	Read active	**(1+w)T–0**	–	**(1+w)T–0**	–	ns	1
t(csvrd)	Read cycle chip select active	**(2+w)T–1**	–	**(2+w)T–1**	–	ns	1
t(csh)	Chip select inactive	**rT–D**	–	**rT–D**	–	ns	2
t(csrd)	Chip select active to read active	**T–2**	–	**T–2**	–	ns	
t(csdv)	Chip select to data valid	–	**(2+w)T–12**	–	**(2+w)T–12**	ns	1
t(rdcs)	Read inactive to chip select inactive	**–1**	–	**–1**	–	ns	
t(rdh)	Read data hold	**0**	–	**0**	–	ns	
t(rds)	Read data setup	**15**	–	**15**	–	ns	

Notes:

T=HCLK cycle

1. w: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [15:8]} –1 = write wait,
   w: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [7:0]} –1 = read wait
2. r: Recovery cycles (**r**) are only inserted when, chip-select turn over or read following by a write on the same chip select. Recovery wait states and cs_setup (**s**) have the same effect on the access. When both wait states are required, only the field with the highest number of wait states is applied, but not both. For a bus-sized access, the cs_setup only affects the first cycle.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Symbol	Description	V_{DD_PX} = 1.8 V		V_{DD_PX} = 2.6 V		Units	Notes
		Min	Max	Min	Max		

3. h: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [23:20]) –1 = write hold wait
4. Keepers can continue to hold data value depending on bus leakage.

3.3.5.2 EBI2 asynchronous bus-sized read-write access to 16-bit memory

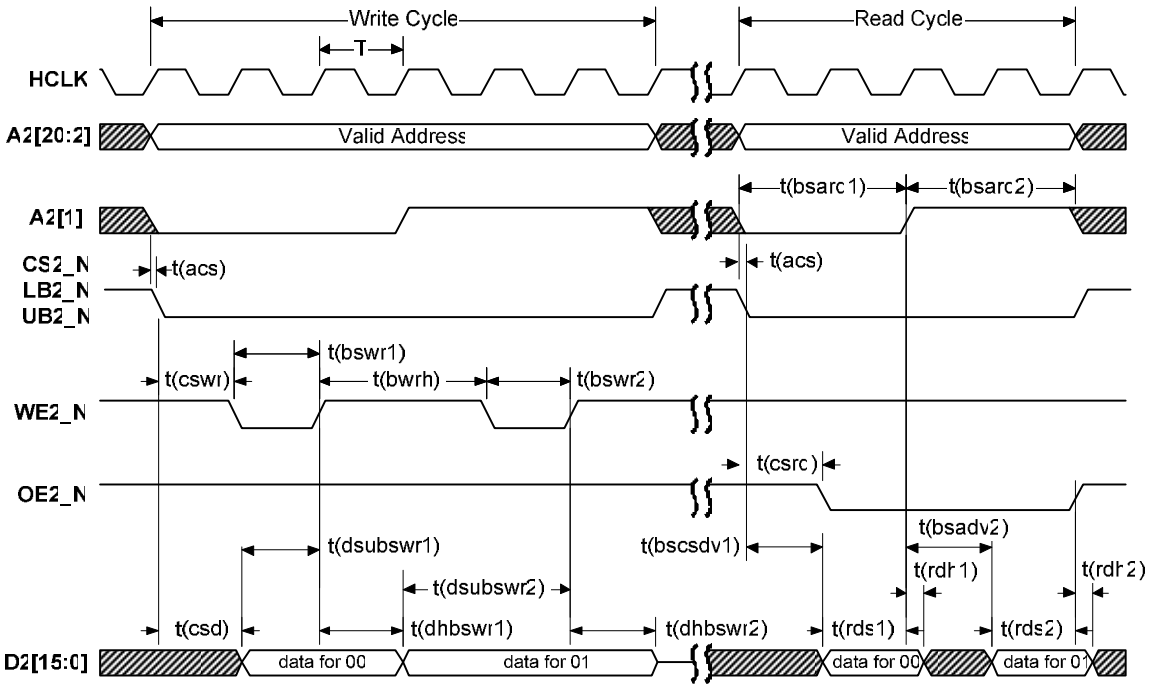

Figure 3-29 EBI2 asynchronous bus-sized access to 16-bit memory

Table 3-18 EBI2 asynchronous bus-sized access timing

Symbol	Description	V_{DD_PX} = 1.8 V		V_{DD_PX} = 2.6 V		Units	Notes
		Min	Max	Min	Max		
Write Cycle							
t(acs)	Address valid to chip select active	rT–2	—	rT–2	—	ns	2
t(cswr)	Chip select active to write active	T–2	—	T–2	—	ns	
t(bswrh)	Write inactive between bus-sized write	(2+h)T–1	—	(2+h)T–1	—	ns	3
t(bswr1)	1st write active	(1+w)T–0	—	(1+w)T–0	—	ns	1
t(bswr2)	2nd write active	(1+w)T–0	—	(1+w)T–0	—	ns	1
t(dsubswr1)	Bus-sized 1st write data setup	(1+w)T–1	—	(1+w)T–1	—	ns	1
t(dhbswr1)	Bus-sized 1st data hold	(1+h)T–0	—	(1+h)T–0	—	ns	3

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Symbol	Description	V_{DD_PX} = 1.8 V		V_{DD_PX} = 2.6 V		Units	Notes
		Min	Max	Min	Max		
t(dsubswr2)	Bus-sized 2nd write data setup	(2+w)T–2	—	(2+w)T–2	—	ns	1
t(dhbswr2)	Bus-sized 2nd data hold time	0	—	0	—	ns	4
Read Cycle							
t(acs)	Address valid to chip select active	rT–2	—	rT–2	—	ns	2
t(bsard1)	Address valid to end of 1st read	(2+w+r)T–2	—	(2+w+r)T–2	—	ns	1,2,3
t(bsard2)	Address valid to end of 2nd read	(2+w)T–2	—	(2+w)T–2	—	ns	1,3
t(csrd)	Chip select active to 1st read active	T–2	—	T–2	—	ns	2
t(rds1)	Bus-sized read data setup for the 1st read	12	—	12	—	ns	
t(rdh1)	Bus-sized read data hold for the 1st read	0	—	0	—	ns	
t(rds2)	Bus-sized read data setup for the 2nd read	15	—	14	—	ns	
t(rdh2)	Bus-sized read data hold for the 2nd read	0	—	0	—	ns	
t(bscsdv1)	Chip select active to 1st data valid	—	(2+w)T–12	—	(2+w)T–12	ns	1
t(bsadv2)	Address Valid to 2nd data valid	—	(2+w)T–14	—	(2+w)T–14	ns	1

Notes:

T=HCLK cycle

1. w: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [15:8]} – 1 = write wait,
   w: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [7:0]} – 1= read wait
2. r: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [27:24]} = recovery wait
3. h: {GP0_CFG0, GP1_CFG0, RAM2_CFG0, ROM2_CFG0 bit [23:20]} – 1 = write hold wait
4. Keepers can continue to hold data value depending on bus leakage.

3.3.5.3 EBI2 NAND interface

The NAND flash memory is connected to XMEM2_CS_N0. The NAND flash controller shares the EBI2 bus with the EBI2 external memory controller. The MSM6550/MSM6150 EBI2 arbiter allows NAND memory access only when the sole request present is that of the NAND controller. In other words, the NAND controller has the lowest priority of all requests to EBI2, and it only gets the grant when all other requests are idle. NAND_FLASH_CFG2[29:0] configures the total clock cycles per access.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

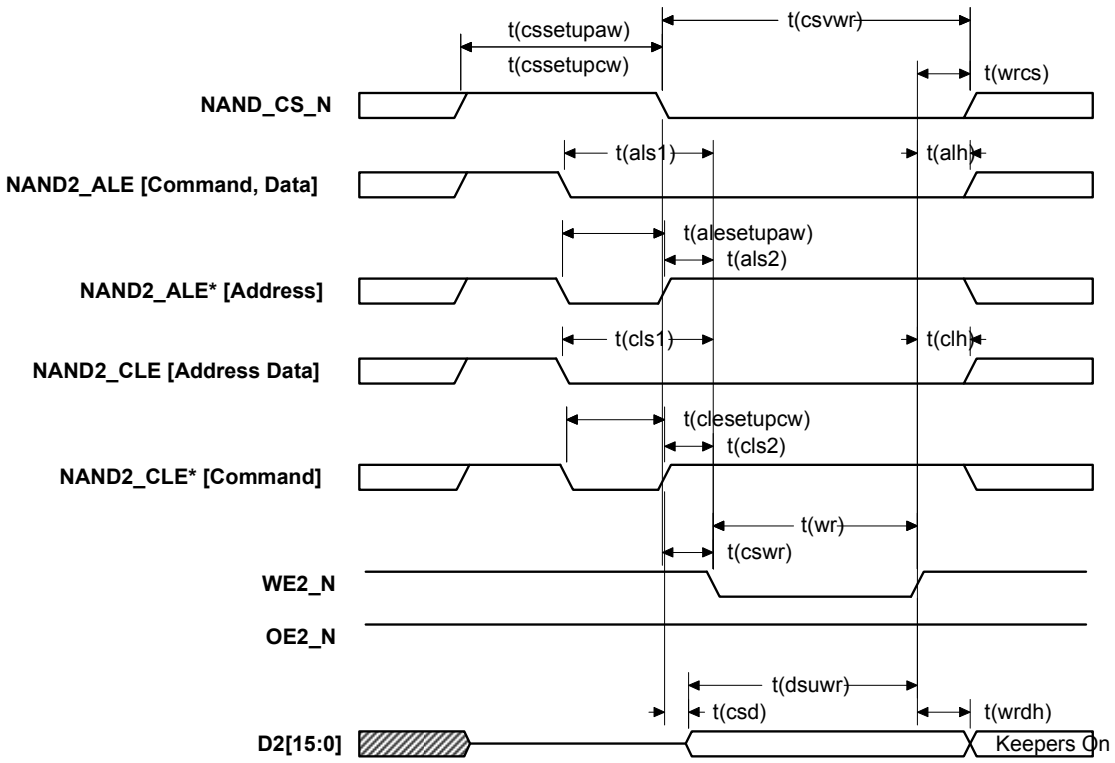

Figure 3-30 Write timing [command/address/data cycles]

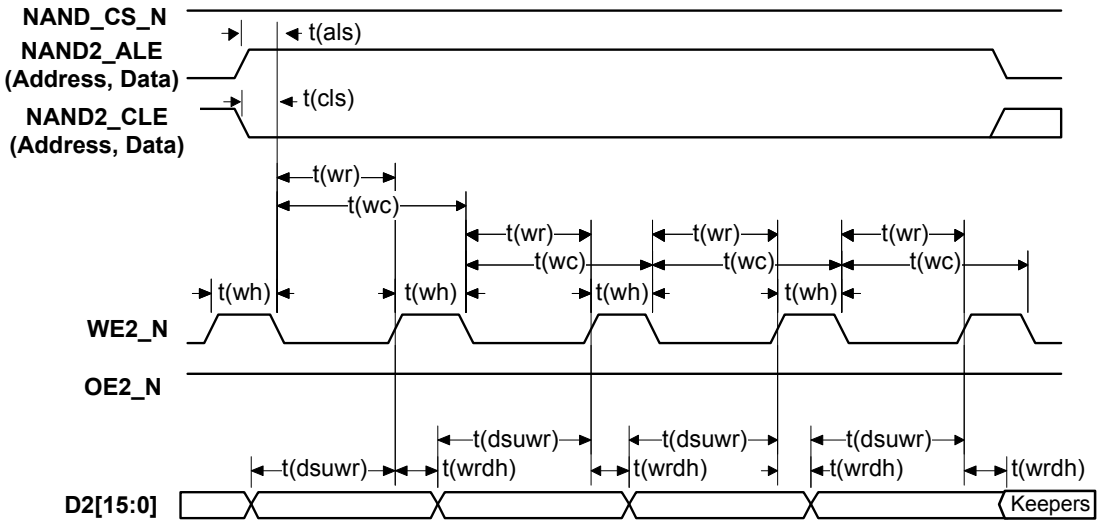

Figure 3-31 Consecutive write access timing sequence

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-19 NAND write timing – AC characteristics

Symbol	Description	V_{DD} =1.8V		V_{DD} =2.6V		Unit	Notes
		Min	Max	Min	Max		
t(cssetupcw)	End of EBI2 XMEM controller access to NAND chip select active {Command and Data cycles}	rT	–	rT	–	ns	3
t(cssetupaw)	End of EBI2 XMEM controller access to NAND chip select active {Address cycle}	rT	–	rT	–	ns	3
t(clesetupcw)	Start of NAND controller access to NAND control latch enable active {Command and Data cycles}	rT–14	–	rT–14	–	ns	3
t(alesetupaw)	Start of NAND controller access to NAND address latch enable active {Address cycle}	rT	–	rT	–	ns	3
t(csvwr)	Chip select active	W_{Wtotal}T–1	–	W_{Wtotal}T–1	–	ns	1, 4
t(dsuwr)	Write data setup	(W_{Wsetup} + $W_{Wactive}$) T–2	–	(W_{Wsetup} + $W_{Wactive}$) T–2	–	ns	1, 4
t(wrdh)	Write data hold	W_{Whold} T–1	–	W_{Whold} T–1	–	ns	1, 4
t(cswr)	Chip select active to write active	W_{Wsetup} T–2	–	W_{Wsetup} T–2	–	ns	1, 4
t(wr)	Write active	$W_{Wactive}$T–0	–	$W_{Wactive}$T–0	–	ns	1, 4
t(wrcs)	Write inactive to chip select inactive	W_{Whold} T–1	–	W_{Whold} T–1	–	ns	1, 4
t(cls1)	Command latch enable setup time to write active {Address and Data cycles}	(r+ W_{Wsetup})T–3	–	(r+ W_{Wsetup})T–3	–	ns	1, 3, 4
t(cls2)	Command latch enable setup time to write active {Command cycle}	W_{Wsetup} T–3	–	W_{Wsetup} T–3	–	ns	1, 4
t(als1)	Address latch enable setup time to write active {Command and Data cycles}	(r+ W_{Wsetup})T–2	–	(r+ W_{Wsetup})T–2	–	ns	1, 3, 4
t(als2)	Address latch enable setup time to write active {Address cycle}	W_{Wsetup} T–2	–	W_{Wsetup} T–2	–	ns	1, 4
t(alh)	Address latch enable hold time from write inactive	W_{Whold} T–1	–	W_{Whold} T–1	–	ns	1, 4
t(clh)	Command latch enable hold time from write inactive	W_{Whold} T–1	–	W_{Whold} T–1	–	ns	1, 4
t(wc)	Write cycle time	W_{Wtotal}T–0	–	W_{Wtotal}T–0	–	ns	1, 4
t(wh)	Write high	(W_{Wsetup}+W_{Whold})T–0	–	(W_{Wsetup}+W_{Whold})T–0	–	ns	1, 4

See notes under Table 3-20.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

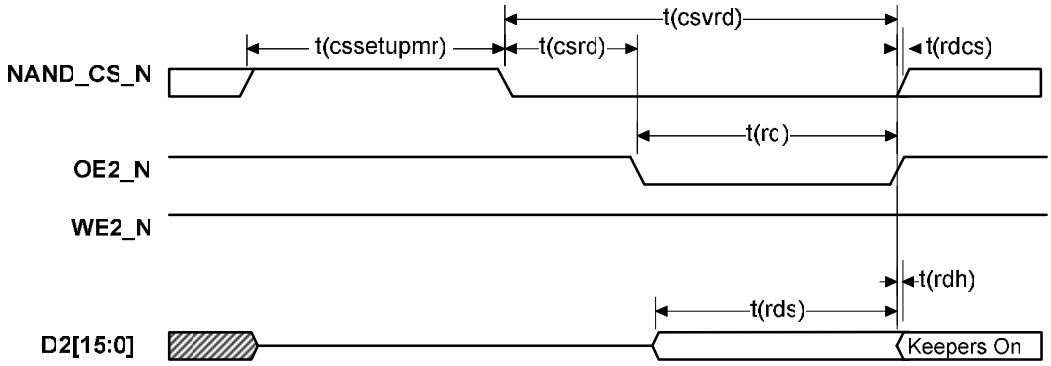

Figure 3-32 NAND read cycles (ID, status, data)

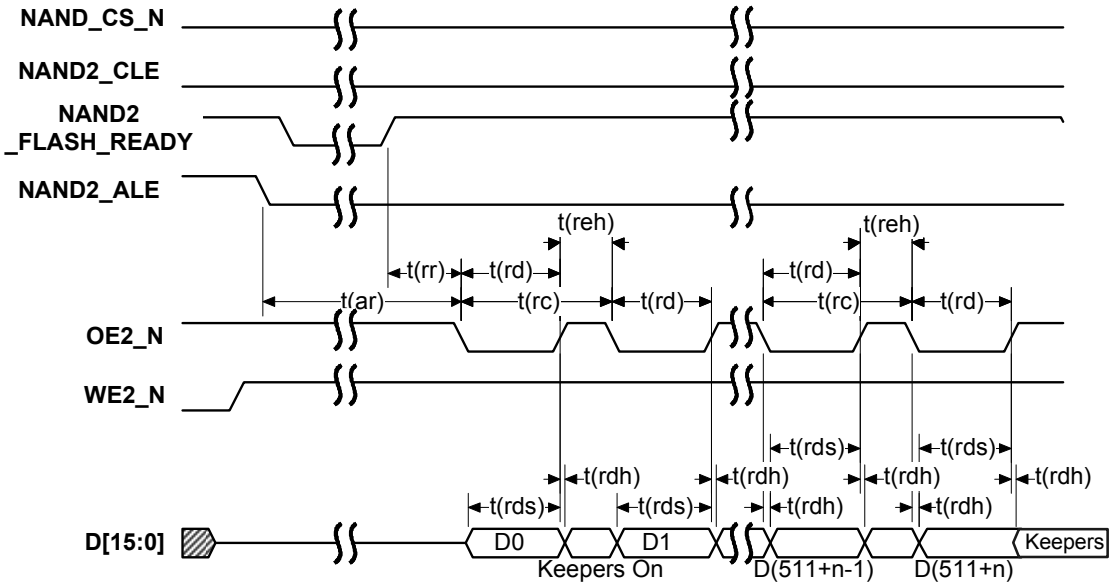

Figure 3-33 Consecutive data read access timing sequence

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-20 NAND read timing – AC characteristics

Symbol	Description	V_{DD} = 1.8V		V_{DD} =2.6V		Unit	Notes
		min	max	Min	max		
t(cssetupmr)	End of EBI2 XMEM controller access to NAND chip select active	rT	–	rT	–	ns	3
t(csvrd) **	Chip select active	$(W_{Rtotal})T–1$	–	$(W_{Rtotal})T–1$	–	ns	2, 4
t(rds)	Read data setup	4	–	4	–	ns	2
t(rdh)	Read data hold	0	–	0	–	ns	2
t(csrd) **	Chip select active to read active	$(W_{Rsetup})T–2$	–	$(W_{Rsetup})T–2$	–	ns	2, 4
t(rd)	Read active	$(W_{Ractive})T–0$	–	$(W_{Ractive})T–0$	–	ns	2, 4
t(rdcs)	Read inactive to chip select inactive	1	–	1	–	ns	2
t(rc) **	Read cycle time	$(W_{Rtotal})T–1$	–	$(W_{Rtotal})T–1$	–	ns	2, 4
t(reh) **	Read high	$(W_{Rsetup})T–1$	–	$(W_{Rsetup})T–1$	–	ns	2, 4
t(ar)	ALE inactive to read active	$t_r + 3.5T$	–	$t_r + 3.5T$	–	ns	2
t(ar) {ID READ} **	ALE inactive to read active	$(W_{Rsetup})T–5$	–	$(W_{Rsetup})T–5$	–	ns	2
t(rr)	R/B_N high to read active	3T	–	3T	–	ns	2, 4

Notes: The following applies to all NAND timing parameters:

T = HCLK cycle, D = characterization data

1. W_{Wsetup} (Write setup) = NAND_FLASH_CFG2[29:25] + 1.
   $W_{Wactive}$ (Write active) = NAND_FLASH_CFG2[24:20] + 1.
   W_{Whold} (Write hold) = NAND_FLASH_CFG2[19:15] + 1.
   $W_{Wtotal} = W_{Wsetup} + W_{Wactive} + W_{Whold}$.
2. $W_{Ractive}$ (Read active) = NAND_FLASH_CFG2[14:10] + 1.
   W_{Rsetup} (Read setup) = NAND_FLASH_CFG2[9:5] + 1.
   $W_{Rtotal} = W_{Rsetup} + W_{Ractive}$.
3. ** For "ID READ" commands, use the following register bits:
   W_{Rsetup} (ID_Read setup) = NAND_FLASH_CFG2[4:0] + 1.
   $W_{Rtotal} = W_{Rsetup}$ (ID_Read setup) + $W_{Ractive}$.
4. r = Number of recovery wait states from previous memory (when previous memory access was a read) = 1+ **Recovery Value**. If a NAND access comes immediately after a read to an EBI2 chip select controlled by the EBI2 external memory controller (GP0_CS_N, GP1_CS_N, GP2_CS_N, GP3_CS_N, LCD_CS_N), the NAND controller may need to provide enough time for that memory to get off the EBI2 bus (stop driving the bus). That time is referred to as "recovery time". Each configuration register for the chip selects mentioned above has a RECOVERY wait state field that indicates to the next access (the NAND access in this context) the required amount of recovery time. Thus, **Recovery value** can be one of the following register values, provided the NAND access immediately follows an XMEM read access:

   GP0_CFG0[27:24], GP1_CFG0[27:24], GP2_CFG0[27:24], GP3_CFG0[27:24], LCD_CFG0[27:24].
5. If the MSM device boots from the NAND flash, the timing requirement for this parameter must be satisfied when the following variables are set to these described values: T=52.08ns, W_{Wsetup} = 1, $W_{Wactive}$ = 5, W_{Whold} = 3, W_{Rsetup} = 4, $W_{Ractive}$ = 4.
6. t_r =memory cell array access time.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.5.4 EBI2 LCD interface

3.3.5.4.1 Motorola-style LCD interface write timing

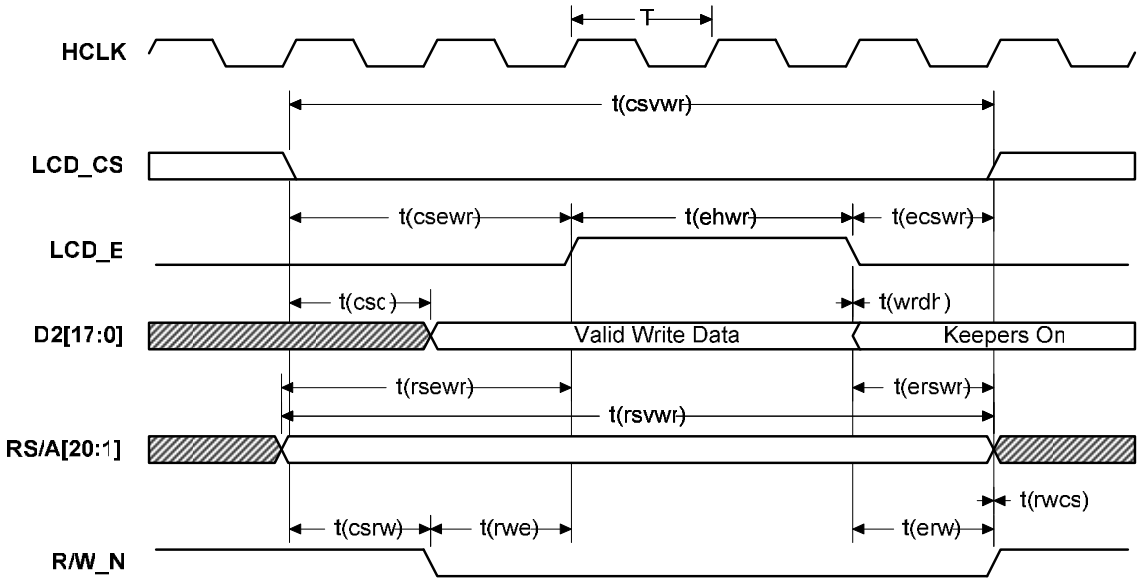

Figure 3-34 Motorola-style LCD interface write timing

Table 3-21 Motorola-style LCD write

Parameter	Description	V_{DD} = 1.8 V		V_{DD} = 2.6V		Units	Notes
		Min	Max	Min	Max		
t(csvwr)	Chip select active	(A+1)T–2	—	(A+1)T–2	—	ns	
t(rsvwr)	Address/RS valid	(A+R+1)T–2	—	(A+R+1)T–1	—	ns	
t(wrdh)	Write data hold	0	—	0	—	ns	
t(csewr)	Chip select active to LCD_E active	ST–0	—	ST–0	—	ns	
t(rsewr)	RS/address valid to LCD_E active	(S+R)T–0	—	(S+R)T–0	—	ns	
t(ehwr)	LCD_E active	PT–1	—	PT–0	—	ns	
t(csd)	Chip select active to data valid	T–2	—	T–1	—	ns	
t(ecswr)	LCD_E inactive to chip select inactive	(1+A–S–P)T–1	—	(1+A–S–P)T–1	—	ns	
t(erswr)	LCD_E inactive to RS/address invalid	(1+A–S–P)T–2	—	(1+A–S–P)T–1	—	ns	
t(csrw)	Chip select active to R/W low	T–2	—	T–2	—	ns	
t(rwe)	R/W low to LCD_E active	(S–1)T–0	—	(S–1)T–0	—	ns	
t(erw)	LCD_E inactive to R/W high	(1+A–S–P)T–2	—	(1+A–S–P)T–2	—	ns	
t(rwcs)	R/W high to chip select	–0.6	—	–0.6	—	ns	

Notes:
T=HCLK cycle; A corresponds **to** LCD_WAIT_WRITE, S corresponds to LCD_E_SETUP time, P corresponds to LCD_E_HIGH, R corresponds to RECOVERY time.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.5.4.2 Motorola-style LCD interface read timing

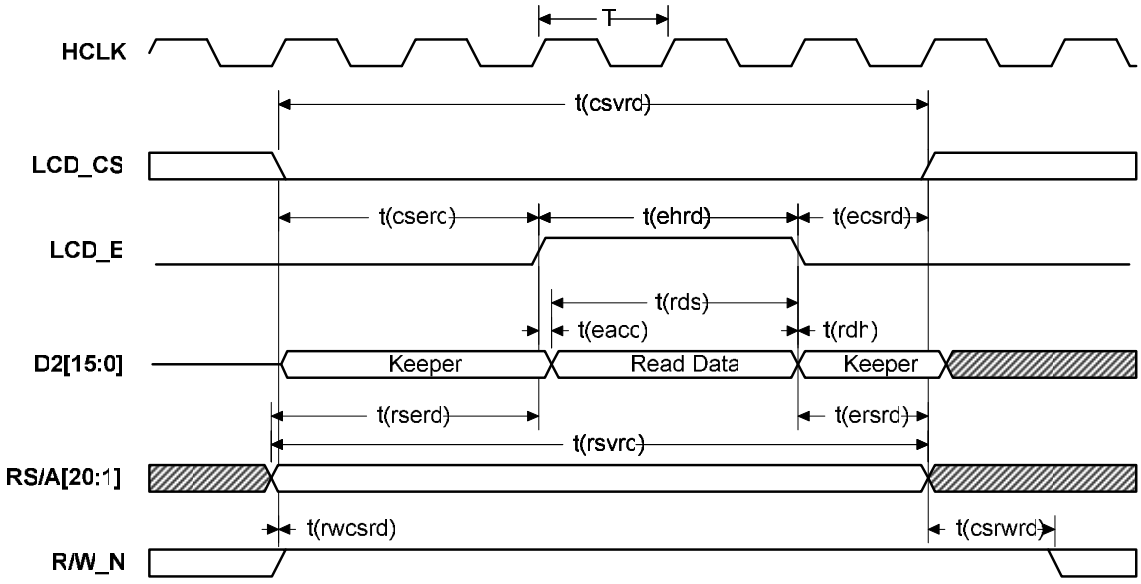

Figure 3-35 Motorola-style LCD interface read timing

Table 3-22 Motorola-style LCD read

Parameter	Description	V_{DD} = 1.8 V		V_{DD} = 2.6 V		Units	Notes
		Min	Max	Min	Max		
t(csvrd)	Chip select active	(A+1)T–2	—	(A+1)T–2	—	ns	
t(rsvrd)	Address/RS valid	(A+R+1)T–2	—	(A+R+1)T–2	—	ns	
t(rds)	Read data setup	16	—	15	—	ns	1,2
t(rdh)	Read data hold	0	—	0	—	ns	1,2
t(cserd)	Chip select active to LCD_E active	ST–0	—	ST–0	—	ns	
t(rserd)	RS/Address valid to LCD_E active	(S+R)T–0	—	(S+R)T–0	—	ns	
t(ehrd)	LCD_E active	PT–1	—	PT–1	—	ns	
t(ecsrd)	LCD_E inactive to chip select inactive	0	—	0	—	ns	2
t(ersrd)	LCD_E inactive to RS/address invalid	0	—	0	—	ns	2
t(rwcsrd)	R/W high to chip select active	0	—	0	—	ns	
t(csrwrd)	Chip select inactive to R/W low	T	—	T	—	ns	
t(eacc)	LCD_E access time	**t**(ehrd)–TBD	—	**t**(ehrd)–TBD	—	ns	

Notes: T=HCLK cycle; A corresponds **to** LCD_WAIT_READ, S corresponds to LCD_E_SETUP time, P corresponds to LCD_E_HIGH, R corresponds to RECOVERY time.

1. Read data setup and hold times are measured with respect to the LCD_E falling edge, even though the ARM may be latching data later in some cases.
2. A+1 must be equal to S+P; the chip-select signal should de-assert at the same cycle as the enable signal.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.5.4.3 Intel-style LCD interface write timing

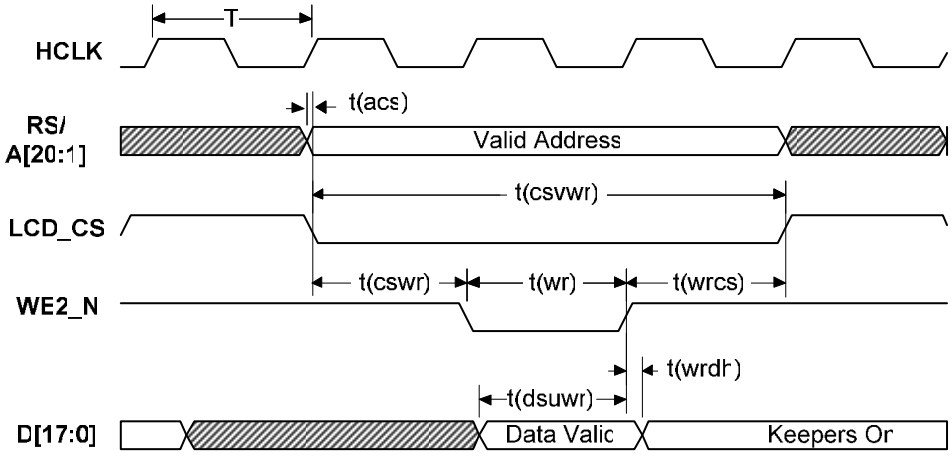

Figure 3-36 Intel-style LCD interface write timing

Table 3-23 Intel-style LCD write

Parameter	Description	V_{DD} = 1.8 V		V_{DD} = 2.6 V		Units	Notes
		Min	Max	Min	Max		
t(acs)	Address valid to chip select active	RT–0	—	RT–0	—	ns	
t(csvwr)	Chip select active	(W+H+3)T–1	—	(W+H+3)T–1	—	ns	
t(wrdh)	Write data hold	0	—	0	—	ns	
t(cswr)	Chip select active to write active	T–2	—	T–2	—	ns	
t(wr)	Write active	(1+W)T–0	—	(1+W)T–0	—	ns	
t(dsuwr)	Write data setup	(1+W)T–1	—	(1+W)T–1	—	ns	
t(wrcs)	Write inactive to chip select inactive	(1+H)T–0	—	(1+H)T–0	—	ns	

Notes: T=HCLK cycle, W: Write Wait: LCD_CFG0[15:8] {LCD_WAIT_WR} - 1, H: Write Hold: LCD_CFG0[21:20] {LCD_HOLD_WR} -1, R corresponds to RECOVERY time. Recovery cycles (R) are only inserted when chip-select turn over or read following by a write on the same chip select. Recovery wait states and cs_setup have the same effect on the access. When both wait states are required, only the field with the highest number of wait states is applied, but not both.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.5.4.4 Intel-style LCD interface read timing

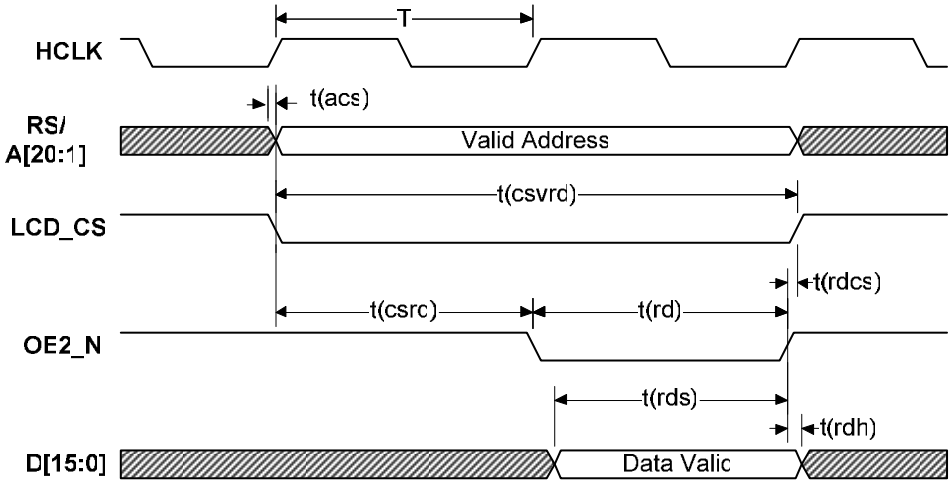

Figure 3-37 Intel-style LCD interface read timing

Table 3-24 Intel-style LCD read

Parameter	Description	V_{DD} = 1.8 V		V_{DD} = 2.6 V		Units	Notes
		Min	Max	Min	Max		
t(acs)	Address valid to chip select active	RT–1	—	RT–1	—	ns	
t(csvrd)	Chip select active	(W+2)T–1	—	(W+2)T–1	—	ns	
t(csrd)	Chip select active to read active	T–1	—	T–1	—	ns	
t(rd)	Read active	(W+1)T–0	—	(W+1)T–0	—	ns	
t(rds)	Read data setup	15	—	15	—	ns	
t(rdh)	Read data hold	0	—	0	—	ns	
t(rdcs)	Read inactive to chip select inactive	–0.4	0.1	–0.4	0.1	ns	

Notes:

T=HCLK cycle, W: Read Wait: LCD_CFG0[7:0] {LCD_WAIT_RD} – 1, R corresponds to RECOVERY time. Recovery cycles (R) are only inserted when, chip-select turn over or read following by a write on the same chip select. Recovery wait states and cs_setup have the same effect on the access. When both wait states are required, only the field with the highest number of wait states is applied, but not both.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.6 Auxiliary interface

3.3.6.1 ETM

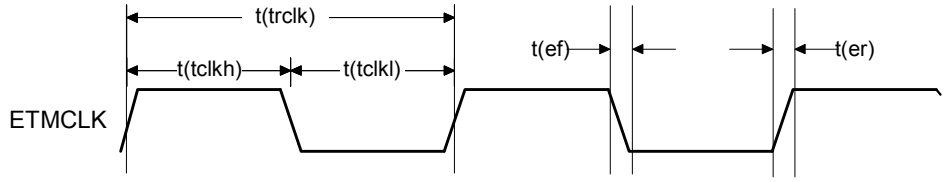

Figure 3-38 ETM clock timing

Table 3-25 Trace clock timing

Symbol	Description	Min	Max	Units
t(trclk)	TRACECLK clock period	TBD	—	ns
t(er)	TRACECLK rise time	—	TBD	ns
t(ef)	TRACECLK fall time	—	TBD	ns
t(tclkh)	TRACECLK high period	TBD	—	ns
t(trclkl)	TRACECLK low period	TBD	—	ns
	Duty cycle	TBD	TBD	%

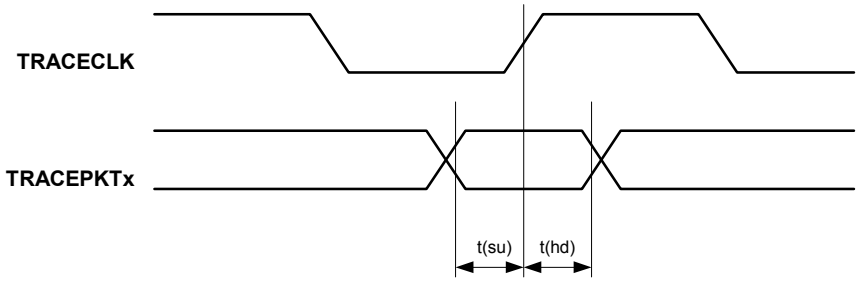

Figure 3-39 ETM trace signals

Table 3-26 ETM trace signals

Symbol	Description	Min	Max	Units
t(su)	TRACE signal setup time	TBD	—	ns
t(hd)	TRACE signal hold time	—	TBD	ns

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.6.2 CAMIF

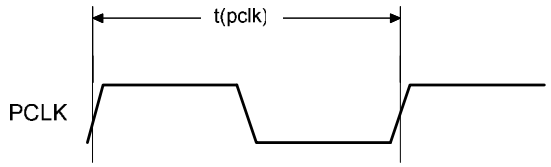

Figure 3-40 CAMIF CLK timing

Table 3-27 CAMIF CLK timing

Symbol	Description	Min	Max	Units
t(pclk)	CAMIF PCLK clock period	15.4	—	ns

Note:
1. CAMIF PCLK maximum frequency is limited to 65 MHz.
2. Recommended duty cycle is 40-60%.

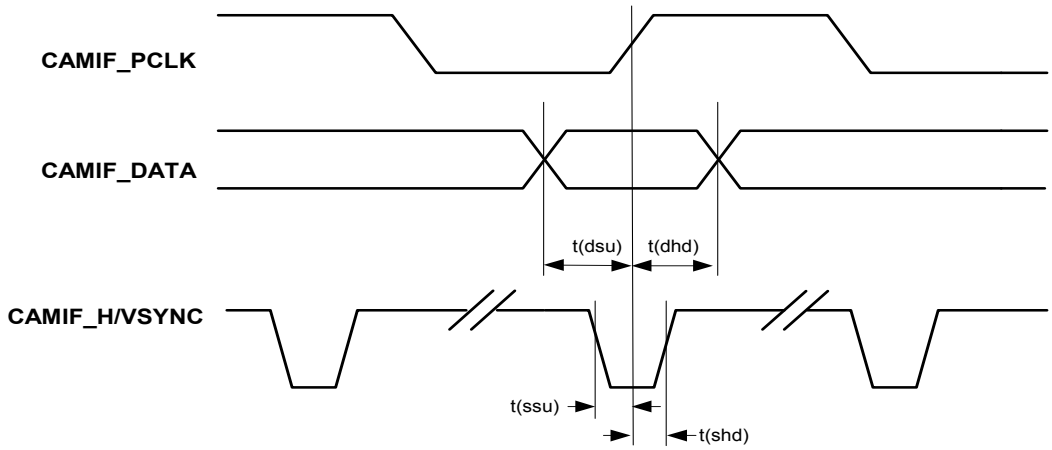

Figure 3-41 CAMIF signals

Table 3-28 CAMIF signals

Symbol	Description	Min	Max	Units
t(dsu)	CAMIF DATA signal setup time	2	—	ns
t(dhd)	CAMIF DATA signal hold time	3	—	ns
t(ssu)	CAMIF V/HSYNCH signal setup time	1	—	ns
t(shd)	CAMIF V/HSYNCH signal hold time	1	—	ns

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.3.6.3 JTAG

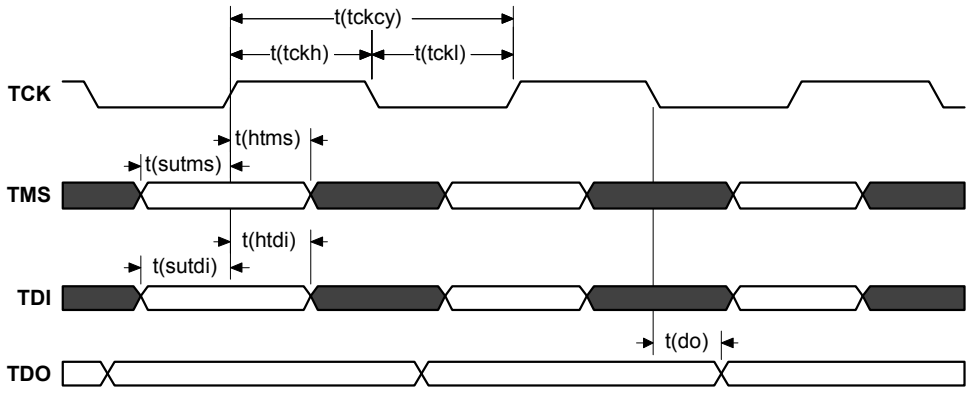

Figure 3-42 JTAG interface timing

Table 3-29 JTAG interface timing

Parameter	Description	Min	Typical	Max	Units
t(tckcy)	TCK period t	100	—	—	ns
t(tckh)	TCK pulse width high	40	—	—	ns
t(tckl)	TCK pulse width low	40	—	—	ns
t(sutms)	TMS input set-up time	25	—	—	ns
t(htms)	TMS input hold time	25	—	—	ns
t(sutdi)	TDI input set-up time	25	—	—	ns
t(htdi)	TDI input hold time	25	—	—	ns
t(do)	TDO data output delay	—	—	70	ns

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.4 Mixed signal characteristics

3.4.1 HKADC specifications

Table 3-30 HKADC performance specification

Specification	Min	Typ	Max	Units	Comments/Conditions
Resolution	—	8	—	BITS	
DNL	–0.75	—	+0.75	LSB	Analog Vdd = ADC reference 300 kHz – 1.2 MHz sample rate
INL	–1.5		+1.5	LSB	
Gain error	–2.5		+2.5	%	
Offset error	–3		+3	LSB	
DNL	–0.75	—	+0.75	LSB	V2 = ADC reference 300 kHz sample rate
INL	–1.5		+1.5	LSB	
Gain error	–7		+7	%	
Offset error	–4		+4	LSB	
DNL	–0.75	—	+0.75	LSB	Internal bandgap = ADC reference 300 kHz
INL	–1.5		+1.5	LSB	
Gain error	–7		+7	%	
Offset error	–5		+5	LSB	
DNL	–0.75	—	+0.75	LSB	Internal bandgap Div2 = ADC reference 300 kHz
INL	–1.5		+1.5	LSB	
Gain error	–7		+7	%	
Offset error	–10		+10	LSB	
Channel isolation	—	50	—		@ DC
Full-scale input range	GND	—	V_{RT}		V_{RT} is variable 0 V to V_{DD_A}
3 dB input bandwidth	—	2500	—		Source resistance = 50 Ω
Input serial resistance	—	5	—	kΩ	Sample and hold switch resistance
Input capacitance	—	12	—	pF	
Power-down to wakeup	—	—	5	µs	
Throughput rate	20.8		170.7	kHz	

Notes:

1. For an acquisition time of 3 clk periods, the CLK period > 2 • τ, τ = 2 • (input resistance + source resistance) • input capacitance.
2. Integral nonlinearity (INL), differential nonlinearity (DNL).

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.4.2 PCM interface

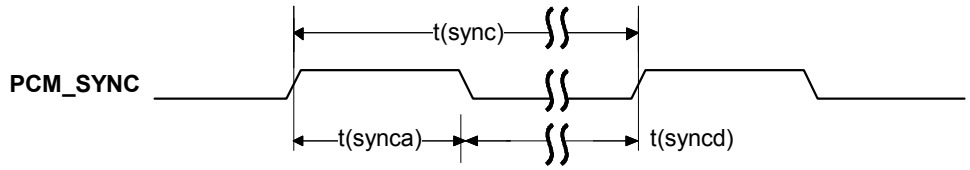

Figure 3-43 PCM_SYNC timing

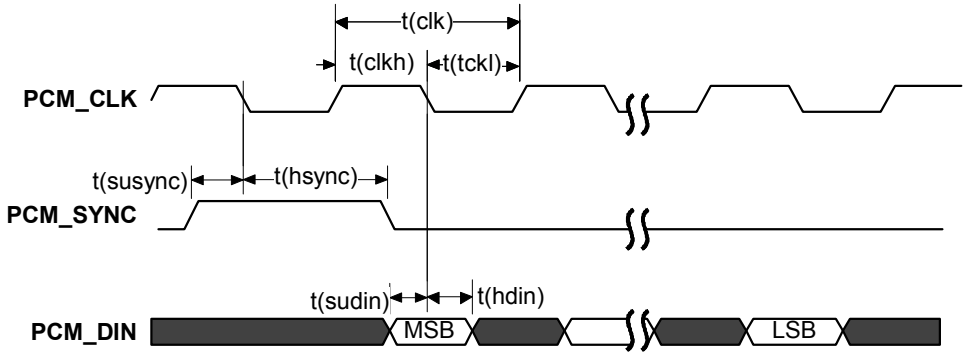

Figure 3-44 PCM_CODEC to MSM6550/MSM6150 device timing

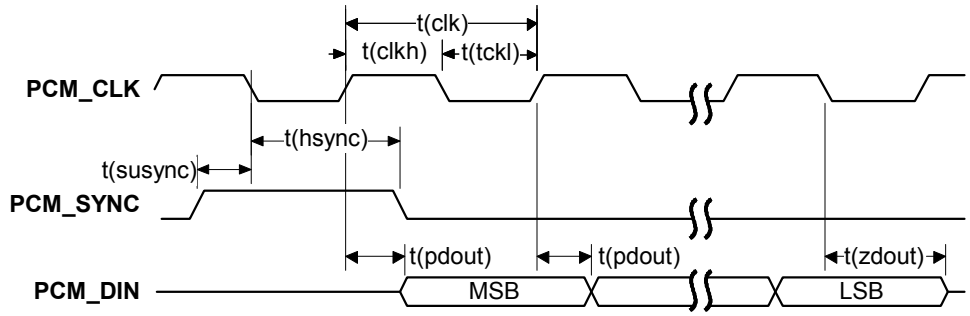

Figure 3-45 MSM6550/MSM6150 device to PCM_CODEC timing

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-31 PCM_CODEC timing parameters

Parameter	Description	Min	Typical	Max	Units	Notes
t(sync)	PCM_SYNC cycle time (PCM_SYNC_DIR=1)	—	125	—	µs	1
	PCM_SYNC cycle time (PCM_SYNC_DIR=0)	—	125	—	µs	
t(synca)	PCM_SYNC asserted time (PCM_SYNC_DIR=1)	400	500	—	ns	1
	PCM_SYNC asserted time (PCM_SYNC_DIR=0)	—	—	—	ns	
t(syncd)	PCM_SYNC de-asserted time (PCM_SYNC_DIR=1)	—	124.5	—	µs	1
	PCM_SYNC de-asserted time (PCM_SYNC_DIR=0)	—	—	—	µs	
t(clk)	PCM_CLK cycle time (PCM_CLK_DIR=1)	400	500	—	ns	1
	PCM_CLK cycle time (PCM_CLK_DIR=0)	—	—	—	ns	
t(clkh)	PCM_CLK high time (PCM_CLK_DIR=1)	200	250	—	ns	1, 2
	PCM_CLK high time (PCM_CLK_DIR=0)	—	—	—	ns	
t(clkl)	PCM_CLK low time (PCM_CLK_DIR=1)	200	250	—	ns	1, 2
	PCM_CLK low time (PCM_CLK_DIR=0)	—	—	—	ns	
t(susync)	PCM_SYNC setup time to PCM_CLK falling	—	150	—	ns	
	(PCM_SYNC_DIR = 1, PCM_CLK_DIR = 1)					
	PCM_SYNC setup time to PCM_CLK falling	—	—	—	ns	
	(PCM_SYNC_DIR = 0, PCM_CLK_DIR = 0)					
t(hsync)	PCM_SYNC hold time after PCM_CLK falling	—	300	—	ns	
	(PCM_SYNC_DIR = 1, PCM_CLK_DIR = 1)					
	PCM_SYNC hold time after PCM_CLK falling	—	—	—	ns	
	(PCM_SYNC_DIR = 0, PCM_CLK_DIR = 0)					
t(sudin)	PCM_DIN setup time to PCM_CLK falling	50	—	—	ns	
t(hdin)	PCM_DIN hold time after PCM_CLK falling	10	—	—	ns	
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	—	—	350	ns	
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z	—	160	—	ns	

Notes:

1. This value assumes that CODEC_CTL is not being used to override the CDMA CODEC clock and sync operation.
2. t(clkh) and t(clkl) are independent of PCM_CLK_SENSE.

3.4.3 Auxiliary PCM interface

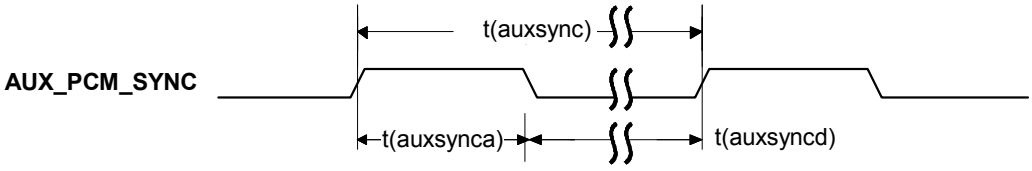

Figure 3-46 AUX_PCM_SYNC timing

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

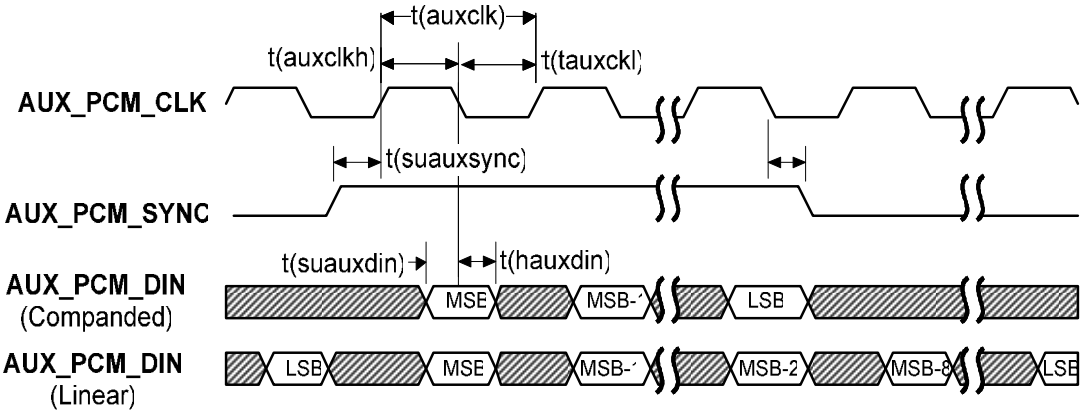

Figure 3-47 AUX_PCM_CODEC to MSM6550/MSM6150 device timing

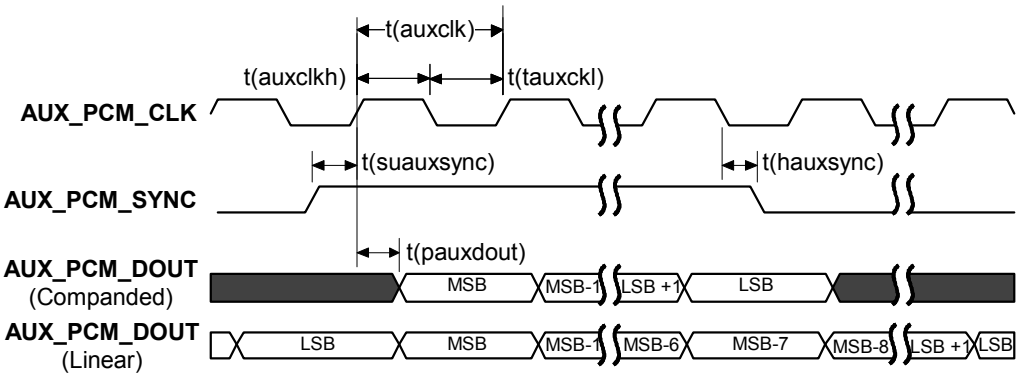

Figure 3-48 MSM6550/MSM6150 device to AUX_PCM_CODEC timing

Table 3-32 AUX_CODEC timing parameters

Parameter	Description	Min	Typical	Max	Units	Notes
t(auxsync)	AUX_PCM_SYNC cycle time	—	125	—	µs	1
t(auxsynca)	AUX_PCM_SYNC asserted time	62.4	62.5	—	µs	1
t(auxsyncd)	AUX_PCM_SYNC de-asserted time	62.4	62.5	—	µs	1
t(auxclk)	AUX_PCM_CLK cycle time	—	7.8	—	µs	1
t(auxclkh)	AUX_PCM_CLK high time	3.8	3.9	—	µs	1
t(auxclkl)	AUX_PCM_CLK low time	3.8	3.9	—	µs	1
t(suauxsync)	AUX_PCM _SYNC setup time to AUX_PCM_CLK rising	1.95	—	—	µs	
t(hauxsync)	AUX_PCM _SYNC hold time after AUX_PCM_CLK rising	1.95	—	—	µs	
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling	70	—	—	ns	

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Parameter	Description	Min	Typical	Max	Units	Notes
t(hauxdin)	AUX_PCM_DIN hold time after AUX_PCM_CLK falling	20	—	—	ns	
t(pauxdin)	Propagation delay from AUX_PCM_CLK AUX_PCM_DOUT valid	—	—	50	ns	

Notes:

1. This value assumes that CODEC_CTL is not being used to override the CDMA CODEC clock and sync operation.

3.4.4 CODEC specifications

Table 3-33 Microphone interface requirements

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IO}	Input offset voltage at MIC1, MIC2 and AUX inputs	Over recommended ranges of supply voltage and free-air temperature	–5		+5	mV
C_I	Input capacitance at MIC1, MIC2 and AUX inputs		—	5	—	pF
	Input DC common mode voltage		0.90	1.0	1.10	V
V_{mbias}	Microphone bias supply voltage	Open circuit DC voltage	1.69	1.8	1.91	V
	MBIAS output DC source current	1.69 kΩ 1% resistive load	1	1.07	—	mA
	MICMUTE attenuation	+3 dBm0 analog input level 1.02 kHz sine wave	80	—	—	dB
Z_{in1}	Input impedance, MIC1, MIC2 and AUX inputs	Fully differential	61	72	83	kΩ
Z_{in2}	Input impedance, AUX inputs	Single-ended, earphone amp summing path	30.6	36	41.4	kΩ

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-34 Speaker interface requirements

Parameter		Test Conditions	Min	Typ	Max	Unit
P_{O1}	EAR_AMP1 output power (rms)	Differential, 32 Ω load, PCMI = +3 dBm0, 1.02 kHz sine wave	—	70	—	mW
P_{O2}	EAR_AMP2 output power (rms)	Single-ended, 16 Ω load, PCMI = +3 dBm0, 1.02 kHz sine wave	—	21.6		mW
P_{O3}	EAR_AMP2 output power (rms)	Single-ended, 16 Ω load, PCMI = +3 dBm0, 1.02 kHz sine wave	—	21.6	—	mW
P_{O4}	AUX_AMP output power (rms)	Differential, 600 Ω load, PCMI = +3 dBm0, 1.02 kHz sine wave	—	2.30	—	mW
P_{O5}	AUX Amp output power (rms)	Single-ended, 600 Ω load, PCMI = +3 dBm0, 1.02 kHz sine wave (AUXOP, AUXON)	—	0.58	—	mW
	Output DC offset voltage between EAR1OP and EAR1ON, AUXOP and AUXON	Fully differential	–50	—	50	mV
	Output common mode voltage, EAR1OP, EAR1ON, EAR2O, AUXOP, AUXON	Measured at each output pin with respect to GND: Vdd = 2.5 V to 2.7 V	1.125	1.25	1.375	V
Z_{OUT1}	Differential output impedance	At 1.02 kHz, for outputs EAR1 and AUX amp	—	—	1	Ω
Z_{OUT2}	Single-ended output impedance	At 1.02 kHz, for output EAR2 and AUX amps	—	—	0.5	Ω
THD	Total harmonic distortion +Noise (voice)	AV_{DD}= 2.5 V, 13-bit mode, PCMI = +3 dBm0, 498 Hz sine-wave, 32 Ω load for EAR1 and EAR2 amps, 600 Ω load for differential line outputs.	—	—	4	%
THD	Total harmonic distortion + Noise (audio)	AV_{DD}= 2.5 V, 16-bit mode, PCMI = +3 dBm0, 1.02 kHz and 5 kHz sine waves, 32 Ω load for EAR2 amps, 600 Ω load for single-ended line outputs.	—	0.05	0.1	%
	EARMUTE attenuation	PCMI = +3 dBm0, 1.02 kHz sine wave	80	—	—	dB

Notes:

1. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
2. RXPGA = 0 dB.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-35 Transmit voice path level translation and linearity, mic amp2 enabled

Parameter	Test Conditions	Min	Typ	Max	Unit
Transmit reference-signal level (0 dBm0)	Differential analog input	—	57.3	—	mV_{rms}
Overload-signal level (+3 dBm0)	Differential analog input	—	229	—	mV_{pp}
Overload-signal level (+3 dBm0) at the analog modulator input (MICFBN, MICFBP)	Differential analog input	—	3.626	—	V_{pp}
Absolute gain error **	0 dBm0 analog input level, 1.02 kHz sine wave	–1	—	1	dB
Gain error relative to gain at –10 dBm0	Analog input level from +3 dBm0 to –30 dBm0	–0.5	—	0.5	dB
Gain error relative to gain at –10 dBm0	Analog input level from –31 dBm0 to –45 dBm0	–1	—	1	dB
Gain error relative to gain at –10 dBm0	Analog input level from –46 dBm0 to –55 dBm0	–1.2	—	1.2	dB

Notes:

** This spec must be applicable to all microphone amplifier gain settings (i.e., –2 dB, +6 dB, +8 dB, +16 dB)

1. These specifications apply to all three Tx path inputs: mic inputs 1 and 2 and aux In.
2. The total transmit channel gain in this default configuration is +24 dB (microphone amplifier 1 is set to +6 dB, the external gain is set to +18 dB, and the TXPGA is set to 0 dB).
3. Fs = Sampling rate, 8 kHz or 16 kHz

Table 3-36 Transmit voice path level translation and linearity, mic amp2 bypassed

Parameter	Test Conditions	Min	Typ	Max	Unit
Transmit reference-signal level (0 dBm0)	Differential analog input	—	455	—	mV_{rms}
Overload-signal level (+3dBm0)	Differential analog input	—	1.82	—	V_{pp}
Overload-signal level (+3dBm0) at the analog modulator input (MICFBN, MICFBP)	Differential analog input	—	3.626	—	V_{pp}
Absolute gain error **	0 dBm0 analog input level, 1.02 kHz sine wave	–1	—	1	dB
Gain error relative to gain at –10 dBm0	Analog input level from +3 dBm0 to –30 dBm0	–0.5	—	0.5	dB
Gain error relative to gain at –10 dBm0	Analog input level from –31 dBm0 to –45 dBm0	–1	—	1	dB
Gain error relative to gain at –10 dBm0	Analog input level from –46 dBm0 to –55 dBm0	–1.2	—	1.2	dB

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Parameter	Test Conditions	Min	Typ	Max	Unit

Notes:

** This spec must be applicable to all microphone amplifier gain settings (i.e., –2 dB, +6 dB, +8 dB, +16 dB).

1. These specifications apply to all three Tx path inputs: mic inputs 1 and 2 and aux In.
2. The total transmit channel gain in this default configuration is +6 dB (microphone amplifier 1 is set to +6 dB and the TXPGA is set to 0 dB).
3. Fs = Sampling rate, 8 kHz or 16 kHz

Table 3-37 Transmit voice path frequency response and image rejection, digital transmit slope filter disabled, mic amp2 bypassed

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz, digital Tx high-pass filter disabled.	Frequency <0.0125xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.025xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.425xFs Hz	–1.5	—	0	dB
	Frequency = 0.4975xFs Hz	—	—	–14	dB
	Frequency = 0.575xFs Hz	—	—	–35	dB
	Frequency = 0.9975xFs Hz	—	—	–47	dB
Gain relative to input signal gain at 1.02 kHz, digital Tx high-pass filter enabled.	Frequency < 0.0125xFs Hz	—	—	–15	dB
	Frequency = 0.025xFs Hz	—	—	–5	dB

Notes:

1. The Tx path input level is –10 dBm0.
2. Frequencies 0.575xFs Hz and 0.9975xFs Hz are used to determine image rejection performance.
3. Fs = Sampling rate, 8 kHz or 16 kHz.

Table 3-38 Transmit voice path frequency response and image rejection, digital transmit slope filter enabled, mic amp2 bypassed

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz, with slope filter selected, digital Tx high pass filter enabled	Frequency = 0.0125xFs Hz	—	—	–27	dB
	Frequency = 0.025xFs Hz	—	—	–8	dB
	Frequency = 0.03125xFs Hz	—	—	–4	dB
	Frequency = 0.0375xFs Hz	—	–1.80	—	dB
	Frequency = 0.05xFs Hz	—	–1.50	—	dB
	Frequency = 0.0625xFs Hz	—	–1.30	—	dB
	Frequency = 0.075xFs Hz	—	–1.1	—	dB
	Frequency = 0.0875xFs Hz	—	–0.8	—	dB
	Frequency = 0.1xFs Hz	—	–0.57	—	dB
	Frequency = 0.1125xFs Hz	—	–0.25	—	dB
	Frequency = 0.1275xFs Hz	—	0	—	dB
	Frequency = 0.1875xFs Hz	—	1.867	—	dB

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Parameter	Test Conditions	Min	Typ	Max	Unit
	Frequency = 0.2475xFs Hz	—	4.0	—	dB
	Frequency = 0.3125xFs Hz	—	6.5	—	dB
	Frequency = 0.375xFs Hz	—	7.6	—	dB
	Frequency = 0.3875xFs Hz	—	7.7	—	dB
	Frequency = 0.4125xFs Hz	—	8.0	—	dB
	Frequency = 0.4375xFs Hz	—	6.48	—	dB
	Frequency = 0.4975xFs Hz	—	—	–13	dB
	Frequency = 0.5625xFs Hz	—	—	–35	dB
	Frequency = 0.625xFs Hz	—	—	–45	dB
	Frequency = 0.9975xFs Hz	—	—	–50	dB

Notes:

1. The passband tolerance is ± 0.25 dB from 300 Hz to 3500 Hz.
2. The Tx path input level is –10 dBm0.
3. Frequencies 0.5625xFs, 0.625xFs and 0.9975xFs Hz are used to determine image rejection performance.
4. Fs = Sampling rate, 8 kHz or 16 kHz.

Table 3-39 Transmit voice path idle channel noise and distortion (8K)

Parameter	Test Conditions	Min	Typ	Max	Unit
Transmit noise	TXPGA gain = 0dB, external gain = +18dB, microphone amplifier 1 gain = +6dB	—	10	15	µVrms
Transmit signal-to-THD+N ratio with 1020 Hz sine wave input	Analog input level at +3dBm0	35	—	—	dB
	Analog input level at 0dBm0	50	—	—	dB
	Analog input level at –5dBm0	50	—	—	dB
	Analog input level at –10dBm0	46	—	—	dB
	Analog input level at –20dBm0	45	—	—	dB
	Analog input level at –30dBm0	40	—	—	dB
	Analog input level at –40dBm0	30	—	—	dB
	Analog input level at –45dBm0	25	—	—	dB

Notes:

1. Specifications must be met with and without Tx slope filter enabled.
2. Specifications must be met for all inputs MIC1, MIC2 and AUX.
3. C-message weighted for 8 kHz sampling rate.
4. Fs = Sampling rate, 8 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-40 Transmit voice path idle channel noise and distortion (16K)

Parameter	Test Conditions	Min	Typ	Max	Unit
Transmit noise	TXPGA gain = 0dB, external gain = +18dB, microphone amplifier 1 gain = +6dB	—	12	22	μVrms
Transmit signal-to-THD+N ratio with 1020 Hz sine wave input	Analog input level at +3dBm0	35	—	—	dB
	Analog input level at 0dBm0	46	—	—	dB
	Analog input level at –5dBm0	46	—	—	dB
	Analog input level at –10dBm0	42	—	—	dB
	Analog input level at –20dBm0	41	—	—	dB
	Analog input level at –30dBm0	36	—	—	dB
	Analog input level at –40dBm0	27	—	—	dB
	Analog input level at –45dBm0	21	—	—	dB

Notes:

1. Specifications must be met with and without Tx slope filter enabled.
2. Specifications must be met for all inputs MIC1, MIC2 and AUX.
3. A-weighted for 16K sampling rate.
4. Fs = Sampling rate, 16 kHz.

Table 3-41 Receive voice path level translation and linearity, EAR_AMP1 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave		1.06		V_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	4.24	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3dBm0 to –40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured differentially between EAR1ON and EAR1OP.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. Loaded condition (32 Ω).
5. 13-bit mode.
6. Fs = Sampling rate = 8 kHz or 16 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-42 Receive voice path level translation and linearity, EAR_AMP2 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave		416.5		mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	1.664	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3dBm0 to –40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50 dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55 dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_L and AVSS.
3. Output measured single-ended with 16-Ω load and DC blocking capacitor (450 µF) connected between HPH_L and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 13-bit mode.
6. Fs = Sampling rate = 8 kHz or 16 kHz.

Table 3-43 Receive voice path level translation and linearity, EAR_AMP3 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave	—	416.5	—	mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	1.664	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3dBm0 to -40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to -50 dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to -55 dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_R and AVSS.
3. Output measured single-ended with 16-Ω load and DC blocking capacitor (450 µF) connected between HPH_R and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 13-bit mode Fs = Sampling rate = 8 kHz or 16 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-44 Receive voice path level translation and linearity, AUX_AMP selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave	—	831	—	mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	3.32	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to –40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50 dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55 dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured differentially between AUXOP and AUXON.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. Loaded condition (600 Ω).
5. 13-bit mode.
6. Fs = Sampling rate = 8 kHz or 16 kHz.

Table 3-45 Receive voice path frequency response and image rejection

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz, digital Rx high-pass filter disabled.	Frequency <0.0125xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.025xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.425xFs Hz	–1.5	—	0	dB
	Frequency = 0.4975xFs Hz	—	—	–14	dB
	Frequency = 0.575xFs Hz	—	—	–46	dB
	Frequency = 0.9975xFs Hz	—	—	–50	dB
Gain relative to input signal gain at 1.02 kHz, digital Rx high-pass filter enabled.	Frequency < 0.0125xFs Hz	—	—	–15	dB
	Frequency = 0.025xFs Hz	—	—	–5	dB

Notes:

1. RXPGA = 0 dB.
2. The Rx path input level is –10 dBm0.
3. This specification applies to EAR_AMP1, EAR_AMP2, EAR_AMP3, AUXOP, AUXON outputs
4. Loaded condition.
5. Frequencies 0.4975xFs, 0.575xFs Hz and 0.9975xFs Hz are used to determine image rejection performance.
6. Fs = Sampling rate = 8 kHz or 16 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-46 Receive voice path idle channel noise and distortion, EAR_AMP1 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMIN = "0000000000000"	—	150	200	μV_{rms}
Receive signal-to-THD+N ratio with 1020 Hz sine wave input	PCMI = +3 dBm0	29	—	—	dB
	PCMI = 0 dBm0	50	—	—	dB
	PCMI = –5 dBm0	47	—	—	dB
	PCMI = –10 dBm0	46	—	—	dB
	PCMI = –20 dBm0	42	—	—	dB
	PCMI = –30 dBm0	40	—	—	dB
	PCMI = –40 dBm0	30	—	—	dB
	PCMI = –45 dBm0	25	—	—	dB
Intermodulation distortion (2 tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to 0 dBm0 sine wave	50	—	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured differentially between EAR1ON and EAR1OP.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. Loaded condition (32 Ω).
5. 13-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 8 kHz or 16 kHz.
8. Measurement Bandwidth = 100 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-47 Receive voice path idle channel noise and distortion, EAR_AMP2 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMI = "0000000000000"	—	—	106	μV_{rms}
Receive signal-to- THD+N ratio with 1020Hz sine wave input	Output Level at +3 dBm0	26	—	—	dB
	Output Level at 0 dBm0	45	—	—	dB
	Output Level at –5 dBm0	44	—	—	dB
	Output Level at –10 dBm0	42	—	—	dB
	Output Level at –20 dBm0	39	—	—	dB
	Output Level at –30 dBm0	37	—	—	dB
	Output Level at –40 dBm0	27	—	—	dB
	Output Level at –45 dBm0	22	—	—	dB
Intermodulation distortion (2 tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to 0 dBm0 sine wave.	50	—	—	dB

Notes:

1. RXPGA = 0 dB
2. Output measured single-ended between HPH_L and AVSS
3. Output measured single-ended with 16-Ω load and DC blocking capacitor (450 µF) connected between HPH_L and AVSS
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave
5. 13-bit mode
6. A-weighted
7. Fs = Sampling rate, 8 kHz or 16 kHz
8. Measurement bandwidth = 100 Hz to 20 kHz

Table 3-48 Receive voice path idle channel noise and distortion, EAR_AMP3 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMI = "0000000000000"	—	—	106	μV_{rms}
Receive signal-to- THD+N ratio with 1020 Hz sine wave input	Output level at +3 dBm0	26	—	—	dB
	Output level at 0 dBm0	45	—	—	dB
	Output level at –5 dBm0	44	—	—	dB
	Output level at –10 dBm0	42	—	—	dB
	Output level at –20 dBm0	39	—	—	dB
	Output level at –30 dBm0	37	—	—	dB
	Output level at –40 dBm0	27	—	—	dB
	Output level at –45 dBm0	22	—	—	dB

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Parameter	Test Conditions	Min	Typ	Max	Unit
Intermodulation distortion (2-tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to 0 dBm0 sine wave.	50	—	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_R and AVSS.
3. Output measured single-ended with 16-Ω load and DC blocking capacitor (450 µF) connected between HPH_R and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 13-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 8 kHz or 16 kHz.
8. Measurement bandwidth = 100 Hz to 20 kHz.

Table 3-49 Receive voice path idle channel noise and distortion, AUX_AMP selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMIN = “0000000000000000”	—	150	200	μV_{rms}
Receive signal-to-THD+N ratio with 1020 Hz sine wave input	PCMI = +3 dBm0	29	—	—	dB
	PCMI = 0 dBm0	50	—	—	dB
	PCMI = –5 dBm0	47	—	—	dB
	PCMI = –10 dBm0	46	—	—	dB
	PCMI = –20 dBm0	42	—	—	dB
	PCMI = –30 dBm0	40	—	—	dB
	PCMI = –40 dBm0	30	—	—	dB
	PCMI = –45 dBm0	25	—	—	dB
Intermodulation distortion (2 tone method)	PCMI = 498 Hz and 2.02 kHz equal amplitude tones, composite peak level equivalent to 0 dBm0 sine wave.	50	—	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured differentially between AUXOP and AUXON.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. Loaded condition (600 Ω).
5. 13-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 8 kHz or 16 kHz.
8. Measurement bandwidth = 100 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-50 Receive audio path level translation and linearity, EAR_AMP2 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave	—	416.5	—	mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	1.664	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3dBm0 to –40 dBm0	–0.5		+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50 dBm0	–1		+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55 dBm0	–1.2		+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_L and AVSS.
3. Output measured single-ended with 16-Ω load and DC blocking capacitor (450 µF) connected between HPH_L and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 16-bit mode.
6. Fs = Sampling rate = 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.

Table 3-51 Receive audio path level translation and linearity, EAR_AMP3 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave	—	416.5	—	mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	1.664	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3dBm0 to –40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50 dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55 dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_R and AVSS.
3. Output measured single-ended with 16-Ω load and DC blocking capacitor (450 µF) connected between HPH_R and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 16-bit mode.
6. Fs = Sampling rate = 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-52 Receive audio path level translation and linearity, AUX_AMP (L or R) selected configured single-ended

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave	—	416.5	—	mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	1.664	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to –40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50 dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55 dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured differentially with 600-Ω load connected between AUXOP and AUXON.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. 16-bit mode.
5. Fs = Sampling rate = 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.

Table 3-53 Receive audio path level translation and linearity, AUX_AMP selected configured differential

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive reference-signal level (0 dBm0)	PCMI = 0 dBm0, 1.02 kHz sine wave	—	831	—	mV_{rms}
Overload-signal level (+3 dBm0)	PCMI = +3 dBm0, 1.02 kHz sine wave	—	3.32	—	V_{pp}
Absolute gain error	PCMI = 0 dBm0, 1.02 kHz sine wave	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = +3 dBm0 to –40 dBm0	–0.5	—	+0.5	dB
Gain error relative to gain at -10 dBm0	PCMI = –41 dBm0 to –50 dBm0	–1	—	+1	dB
Gain error relative to gain at -10 dBm0	PCMI = –51 dBm0 to –55 dBm0	–1.2	—	+1.2	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between AUXOP and AVSS; AUXON and AVSS.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. 16-bit mode
5. Fs = Sampling rate = 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-54 Receive audio path frequency response and image rejection

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain relative to input signal gain at 1.02 kHz, digital Rx high-pass filter disabled.	Frequency <0.0125xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.025xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.0375xFs Hz to 0.375xFs Hz	–0.5	—	0.5	dB
	Frequency = 0.425xFs Hz	–1.5	—	0	dB
	Frequency = 0.4975xFs Hz	—	—	–14	dB
	Frequency = 0.575xFs Hz	—	—	–35	dB
	Frequency = 0.9975xFs Hz	—	—	–47	dB
Gain relative to input signal gain at 1.02 kHz, digital Rx high-pass filter enabled.	Frequency < 0.0125xFs Hz	—	—	–15	dB
	Frequency = 0.025xFs Hz	—	—	–5	dB

Notes:

1. RXPGA = 0 dB.
2. The Rx path input level is –10 dBm0.
3. This specification applies to EAR_AMP2, EAR_AMP3, AUX_AMP outputs.
4. Loaded condition.
5. Frequencies 0.4975xFs, 0.575xFs Hz and 0.9975xFs Hz are used to determine image rejection performance.
6. Fs = Sampling rate = 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.

Table 3-55 Receive audio path idle channel noise and distortion, EAR_AMP2 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMI = “0000000000000000”	—	22.4	26.6	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–66	–60	dB
Total harmonic distortion + noise (THD+N)	Output level at –57 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–28	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_L and AVSS.
3. Output measured single-ended with 16 Ω load and DC blocking capacitor (450 µF) connected between HPH_L and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 16-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.
8. Measurement bandwidth = 20 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-56 Receive audio path idle channel noise and distortion, EAR_AMP3 selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMI = "0000000000000000"	—	22.4	26.6	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–66	–60	dB
Total harmonic distortion + noise (THD+N)	Output level at –57 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–28	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-ended between HPH_R and AVSS.
3. Output measured single-ended with 16 Ω load and DC blocking capacitor (450 µF) connected between HPH_R and AVSS.
4. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
5. 16-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.
8. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-57 Receive audio path idle channel noise and distortion, AUX_AMP (R or L) selected and configured single-ended

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMI = "0000000000000000"	—	29.48	33.08	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–66	–60	dB
Total harmonic distortion + noise (THD+N)	Output level at –57 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–25	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured single-end with 600 Ω load and DC blocking capacitor (15 µF) connected between AUXOP and AVSS; AUXON and AVSS.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. Loaded condition (600 Ω).
5. 16-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1 kHz or 48 kHz.
8. Measurement bandwidth = 20 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-58 Receive audio path idle channel noise and distortion, AUX_AMP selected and configured differential

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive noise	PCMI = "0000000000000000"	—	46.73	52.0	μV_{rms}
Total harmonic distortion + noise (THD+N)	Output level at +3 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–66	–60	dB
Total harmonic distortion + noise (THD+N)	Output level at –57 dBm0, 1.02 kHz and 5 kHz, Vdd=2.5 V	—	–28	—	dB

Notes:

1. RXPGA = 0 dB.
2. Output measured differentially between AUXOP and AUXON.
3. +3 dBm0 level corresponds to 0 dB full-scale sine wave.
4. Loaded condition (600 Ω).
5. 16-bit mode.
6. A-weighted.
7. Fs = Sampling rate, 16 kHz or 22.05 kHz or 24 kHz or 32 kHz or 44.1K or 48 kHz.
8. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-59 Power supply rejection and crosstalk attenuation

Parameter	Test Conditions	Min	Typ	Max	Unit
Supply voltage rejection, transmit channel	Analog input level = 0 Vpp, AV_{DD} = $2.5V_{dc}$ + $100mV_{rms}$,frequency = 0 - 30 kHz	45	—	—	dB
Supply voltage rejection, receive channel	PCMIN = "0000000000000". AV_{DD} = 2.5 V_{dc} + 100 mV_{rms} , frequency = 0 - 30 kHz	45	—	—	dB
Crosstalk attenuation, transmit-to-receive (differential outputs) with sidetone disabled	0 dBm0 analog input level. frequency = 0.0375xFs - 0.425xFs Hz. measured differentially at Rx path output	70	—	—	dB
Crosstalk attenuation, receive-to-transmit	PCMI = 0 dBm0, frequency = 0.0375xFs - 0.425xFs Hz. Measured at PCMO, EAR/HPh_L/HPh_R/AUXOP/ AUXON amp unloaded	70	—	—	dB
Inter-channel isolation, left to right channels	Left channel input = 0 dBm0, Right channel = all zeros input. frequency = 20 Hz – 20 kHz. measured HPh_R output	70	—	—	dB
Inter-channel isolation, right to left channels	Right channel input = 0 dBm0, Left channel = all zeros input. frequency = 20Hz – 20kHz. measured HPh_L output	70	—	—	dB
Inter-channel isolation, left to right channels	Left channel input = 0 dBm0, Right channel = all zeros input. Frequency = 20Hz – 20kHz. Measured AUXON output	66	—	—	dB

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Parameter	Test Conditions	Min	Typ	Max	Unit
Inter-channel isolation, right to left channels	Right channel input = 0 dBm0, Left channel = all zeros input. Frequency = 20Hz – 20kHz. Measured AUXOP output	66	—	—	dB

Notes:

1. RXPGA = 0 dB.
2. Applies to all three Tx path inputs and all four Rx Path outputs.
3. Fs = Sampling rate = 8 kHz or 16 kHz.

Table 3-60 AUXIP (Line_In_L) input to EAR_AMP1 output selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	4.24	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_L) = 0 V_{PP} AUX PGA = +5.5dB	—	—	106	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–28	dB
Absolute gain error	AUXIP (Line_In_L) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, –0.5dB, –3.5dB, –6.5dB, respectively.

1. Output measured differentially between EARN and EARP, loaded condition (32 Ω).
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-61 AUXIP (Line_In_L) input to EAR_AMP2 output selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	1.664	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_L) = 0 V_{PP} AUX PGA = +5.5dB	—	—	42	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–66	dB
Absolute gain error	AUXIP (Line_In_L) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, –0.5dB, –3.5dB, –6.5dB, respectively.

1. Output measured single-ended with 16 Ω load and DC blocking capacitor (450 µF) connected between HPh_L and GND.
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-62 AUXIP (Line_In_L) input to AUX_AMP output selected and configured differential

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	3.32	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_L) = 0 V_{PP} AUX PGA = +5.5dB	—	—	84	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–66	dB
Absolute gain error	AUXIP (Line_In_L) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, –0.5dB, –3.5dB, –6.5dB, respectively.

1. Output measured differentially between AUXOP and AUXON.
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-63 AUXIP (Line_In_L) input to AUX_AMP output selected and configured single-ended

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	1.664	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_L) = 0 V_{PP} AUX PGA = +5.5dB	—	—	42	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_L) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–66	dB
Absolute gain error	AUXIP (Line_In_L) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–-1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, -0.5dB, -3.5dB, -6.5dB, respectively.

1. Output measured single-ended with 600 Ω load and DC blocking capacitor (15 µF) connected between AUXOP and GND.
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-64 AUXIN (Line_In_R) input to EAR_AMP3 output selected

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_R) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	1.664	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_R) = 0 V_{PP} AUX PGA = +5.5dB	—	—	42	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_R) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–66	dB
Absolute gain error	AUXIP (Line_In_R) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, –0.5dB, –3.5dB, –6.5dB, respectively.

1. Output measured single-ended with 16 Ω load and DC blocking capacitor (450 µF) connected between HPh_R and GND.
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

Table 3-65 AUXIN (Line_In_R) input to AUX_AMP output selected and configured differential

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_R) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	3.32	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_R) = 0 V_{PP} AUX PGA = +5.5dB	—	—	84	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_R) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–66	dB
Absolute gain error	AUXIP (Line_In_R) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, -0.5dB, -3.5dB, -6.5dB, respectively.

1. Output measured differentially between AUXOP and AUXON.
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

Table 3-66 AUXIN (Line_In_R) input to AUX_AMP output selected and configured single-ended

Parameter	Test Conditions	Min	Typ	Max	Unit
Overload-signal level *	AUXIP (Line_In_R) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	—	1.664	—	V_{PP}
Output referred noise * (A-weighted)	AUXIP (Line_In_R) = 0 V_{PP} AUX PGA = +5.5dB	—	—	42	μV_{rms}
Total harmonic distortion + noise (THD+N) * (A-weighted)	AUXIP (Line_In_R) = 1.5 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB, V_{DD} = 2.5 V	—	—	–66	dB
Absolute gain error	AUXIP (Line_In_R) = 1.06 V_{PP}, 1.02 kHz sine wave, AUX PGA = +5.5dB	–-1	—	1	dB

Notes:

* Levels should scale to AUX PGA gains = +2.5dB, –0.5dB, –3.5dB, –6.5dB, respectively.

1. Output measured single-ended with 600 Ω load and DC blocking capacitor (15 µF) connected between AUXOP and GND.
2. Left and right DAC channels are in mute condition.
3. Measurement bandwidth = 20 Hz to 20 kHz.

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

3.4.5 Sleep clock

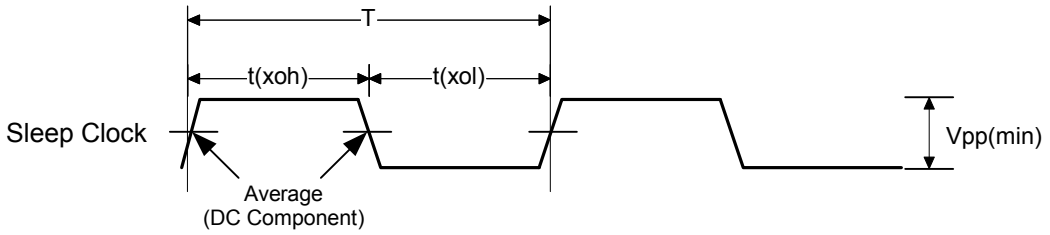

Figure 3-49 Sleep clock timing parameters

Table 3-67 Sleep clock timing parameters

Symbol	Parameter	Min	Typ	Max	Units
t(xoh)	Sleep clock logic high	TBD	—	TBD	ns
t(xol)	Sleep clock logic low	TBD	—	TBD	ns
T(t)	Sleep clock period	—	30.518	—	us
1/T(t)	Frequency	—	32.768	—	kHz
Vpp(min)	Minimum peak-to-peak voltage				mV_{PP}

3.4.6 USB clock

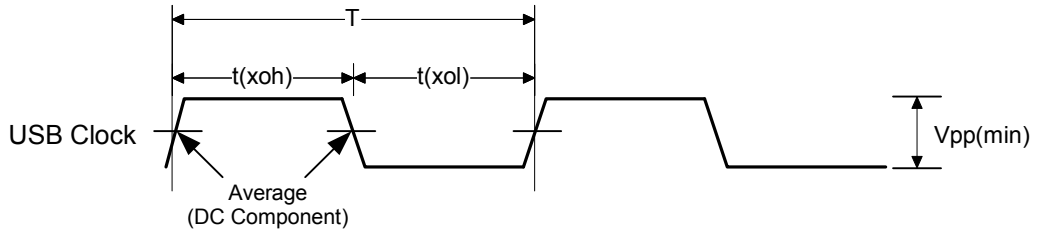

Figure 3-50 USB clock timing parameters

Table 3-68 USB clock timing parameters

Symbol	Parameter	Min	Typ	Max	Units
t(xoh)	USB clock logic high	TBD	—	TBD	ns
t(xol)	USB clock logic low	TBD	—	TBD	ns
T(t)	USB clock period	—	20.883	—	ns
1/T(t)	Frequency	—	48	—	MHz
Vpp(min)	Minimum peak-to peak-voltage				mV_{PP}

(Specifications listed in this chapter are TARGET specifications for the MSM6550/MSM6150 devices and are subject to change without notice)

4 Package Specifications

The 409-ball CSP package outline is specified in QUALCOMM document *BGA/CSP Package User Guide*, 80-V2560-1.

4.1 409 CSP

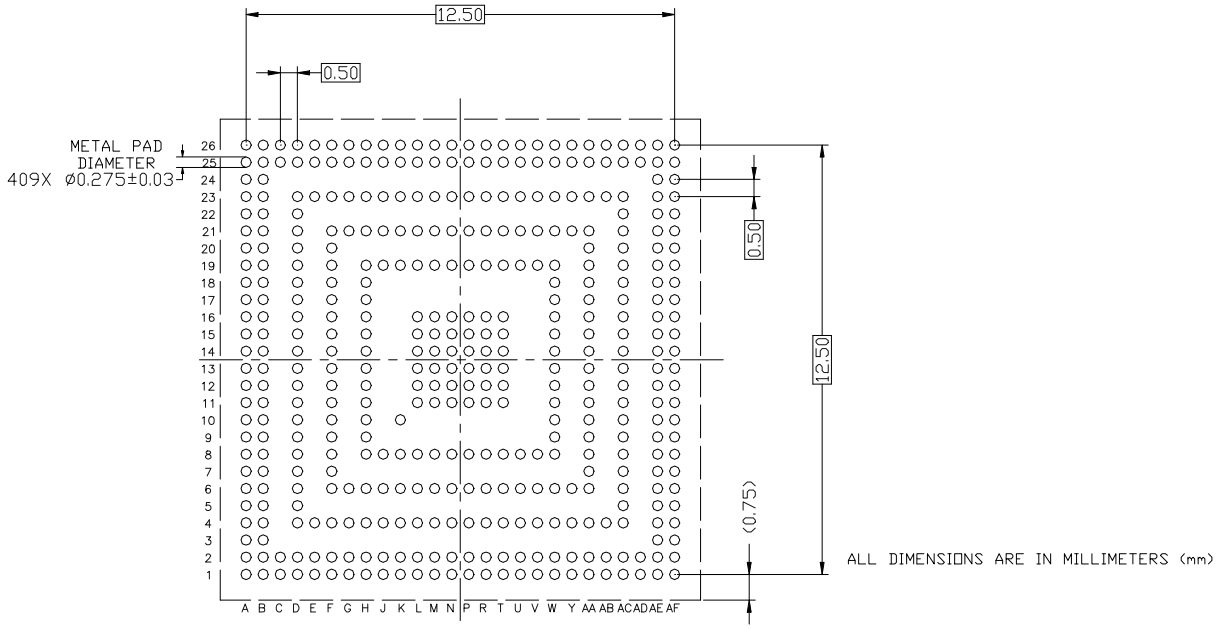

Figure 4-1 409 CSP land pattern drawing

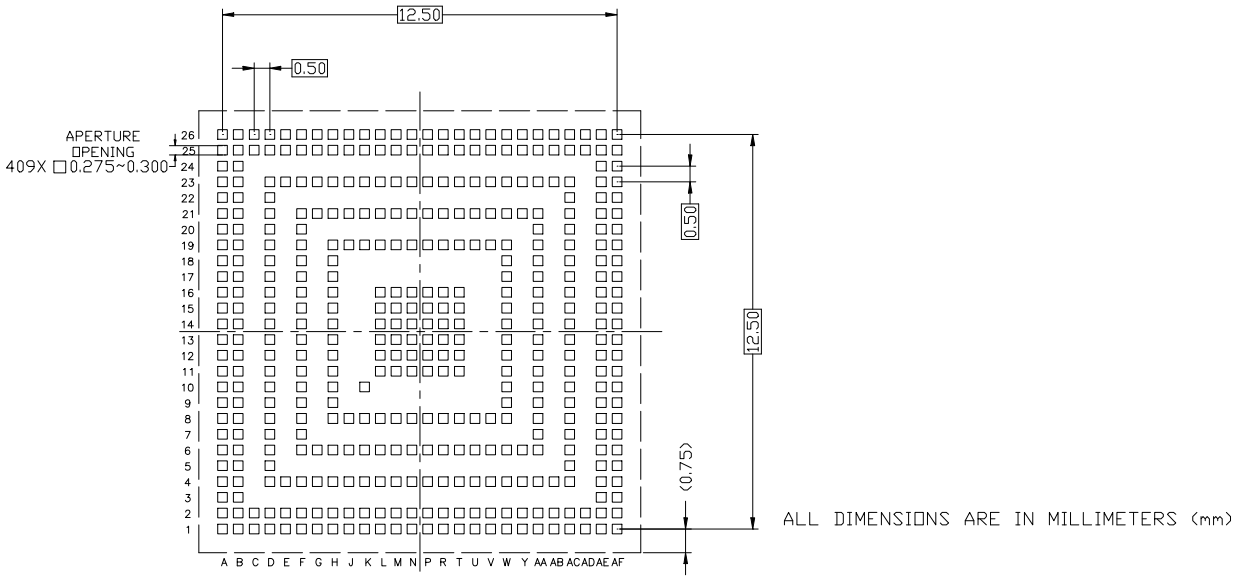

Figure 4-2 409 CSP solder stencil design – square aperture

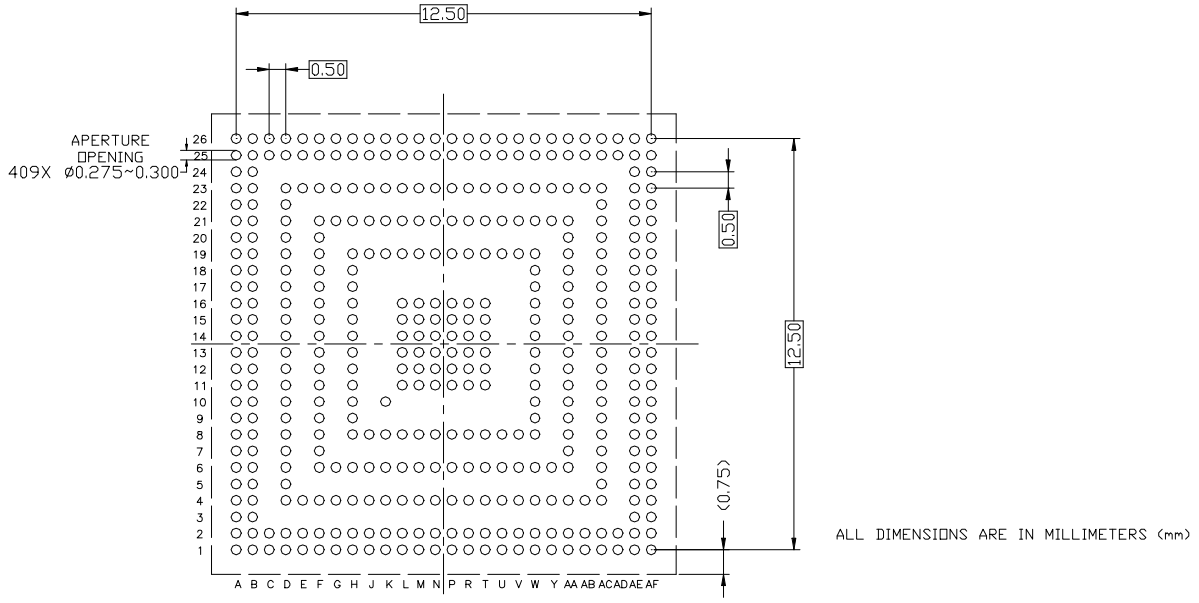

Figure 4-3 409 CSP solder stencil design – circular aperture

4.2 MSM6550 part marking

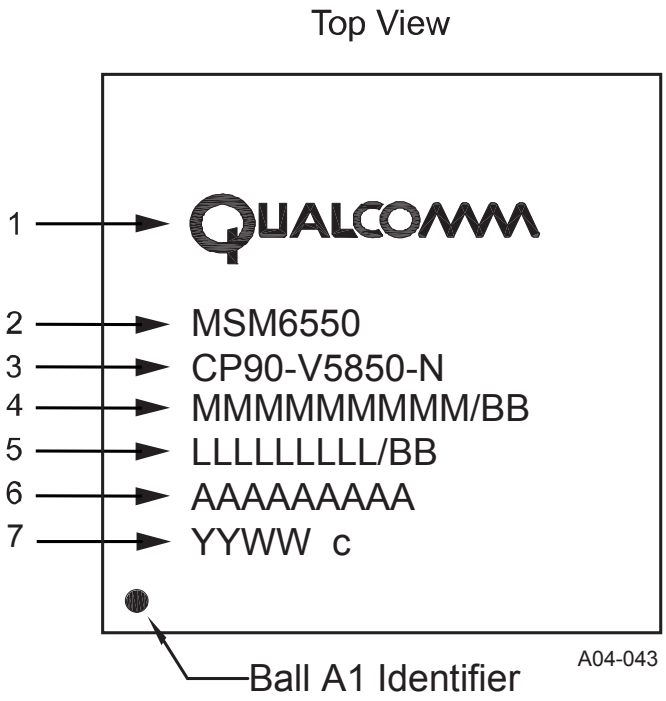

Figure 4-4 MSM6550 part marking

Line	Description
1	QUALCOMM logo (available via QUALCOMM document AW17-3902)
2	QUALCOMM product # (MSM6550)
3	QUALCOMM MCN (CP90-V7850-N) N = device version
4	Traceability number
5	Traceability number
6	Assembly lot code: AAAAAAAAA
7	Assembly encapsulation date and site codes: YY = Year (last 2 digits) WW = Workweek (based upon calendar year) c = Assembly site code (c="A" for ASE, Taiwan and "R" for ChipPAC, S. Korea)

4.3 MSM6150 part marking

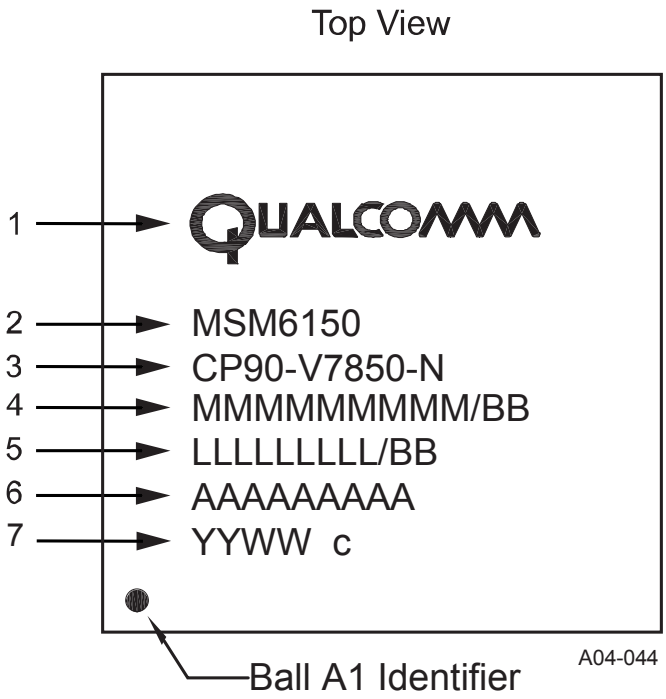

Figure 4-5 MSM6150 part marking

Line	Description
1	QUALCOMM logo
2	QUALCOMM product # (MSM6150)
3	QUALCOMM MCN (CP90-V7850-N) N = device version
4	Traceability number
5	Traceability number
6	Assembly lot code: AAAAAAAAA
7	Assembly encapsulation date and site codes: YY = Year (last 2 digits) WW = Workweek (based upon calendar year) c = Assembly site code (c="A" for ASE, Taiwan and "R" for ChipPac, S. Korea)

5 Package/Tape and Reel

5.1 Packing of shipments

Tape and Reel. Units shipped in tape and reel conform to the industry standard EIA-481 and are packed as indicated in Figure 5-1 through Figure 5-4.

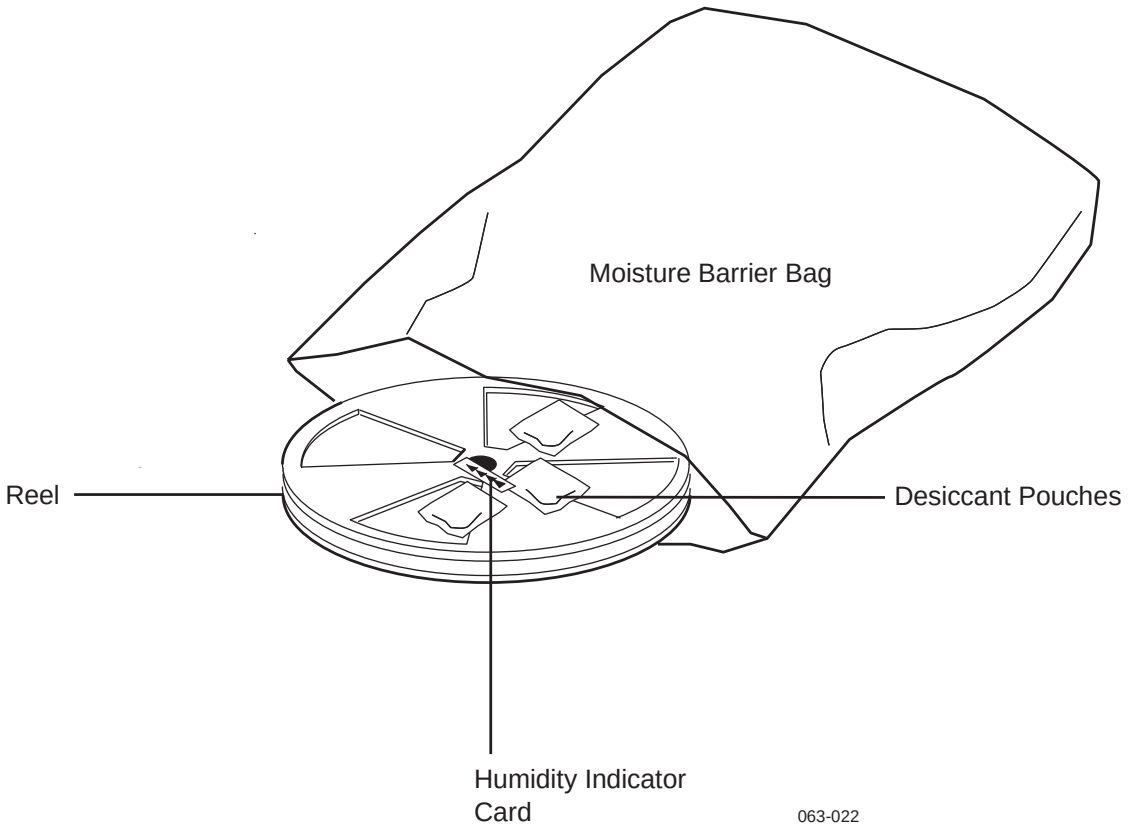

Figure 5-1 Bag packing for tape and reel

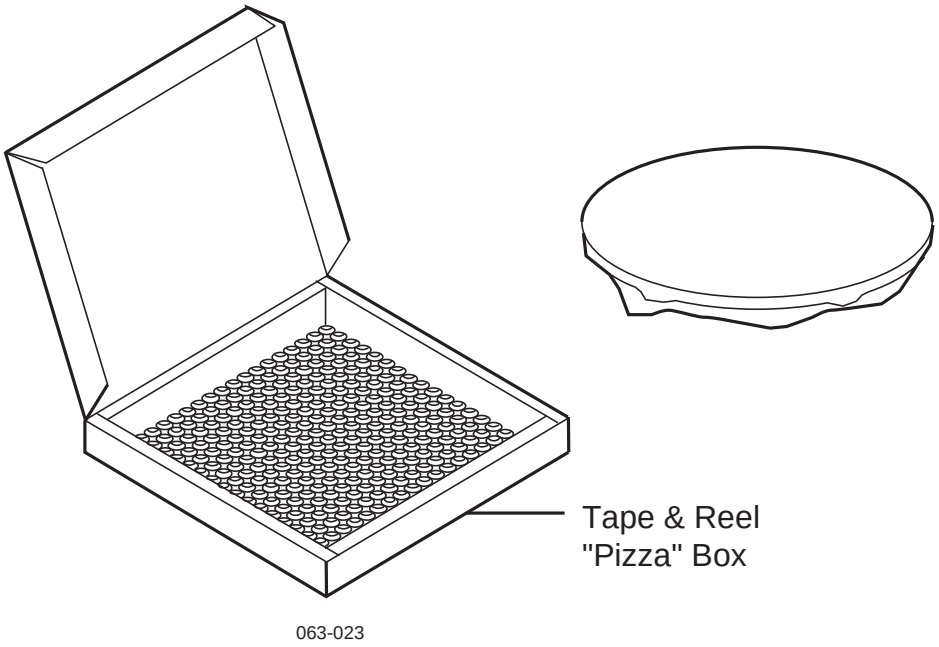

Figure 5-2 Box packing for tape and reel

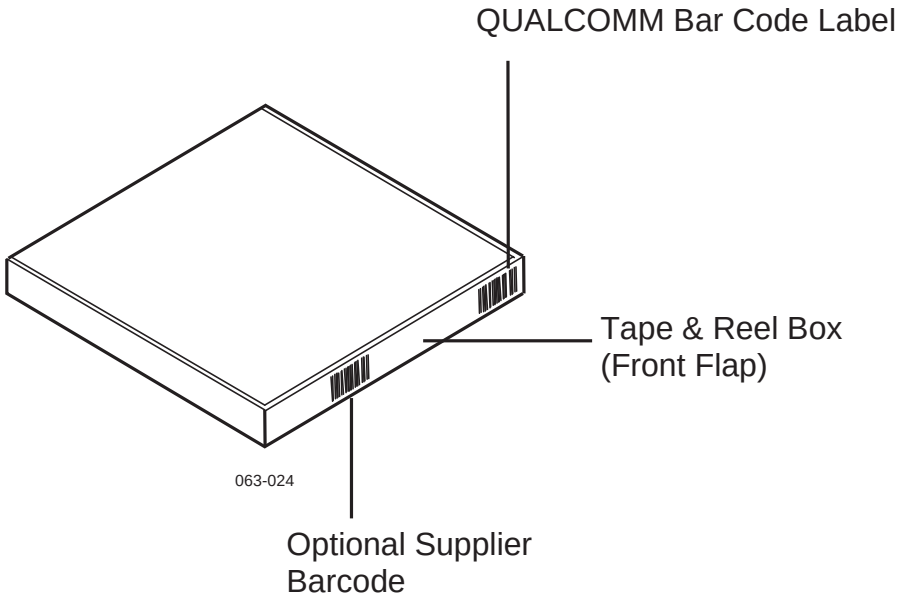

Figure 5-3 Tape and reel box

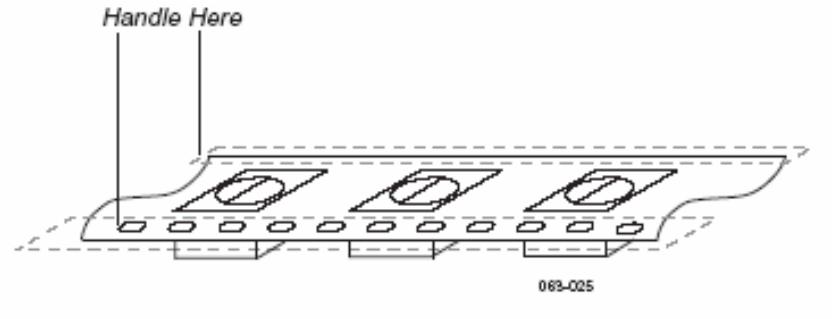

Figure 5-4 Tape handling

Tape/reel information

The single-feed tape carrier for this device is illustrated in Figure 5-5. The tape width is 24 mm and the pitch of the parts places on the tape is 24 mm. Please refer to QUALCOMM document *BGA/CSP Package User Guide*, 80-V2560-1 for further information on 409 CSP Package Specification.

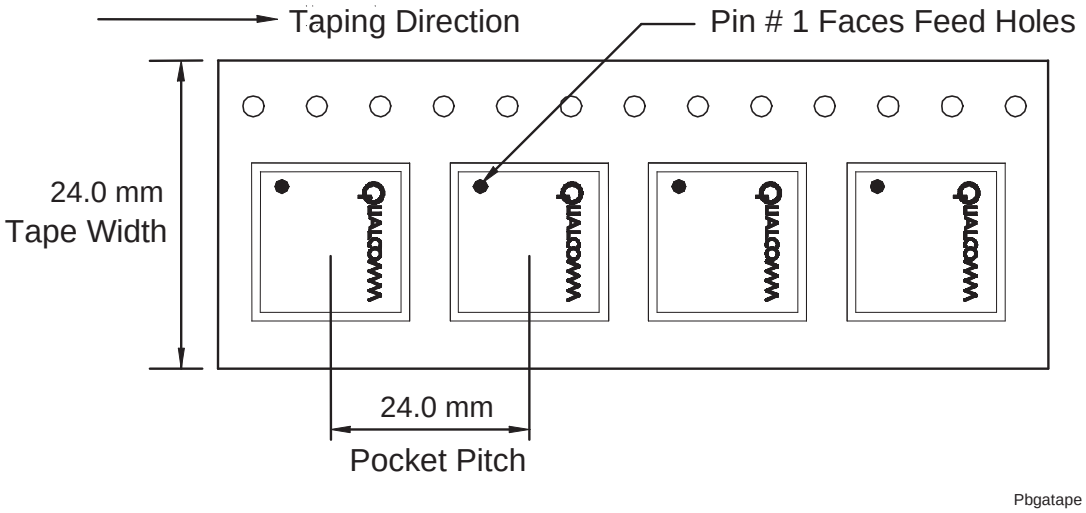

Figure 5-5 Tape dimensions for the 409-ball CSP

5.2 Packing materials

Moisture-sensitive surface mount technology (SMT) components packed on tape and reel are shipped in desiccant packing. Each shipment contains units that have been baked dry and are enclosed in sealed moisture barrier bags (MBB) with desiccant pouches and humidity indicator cards (HIC).

Shipping Box. The label on the shipping box provides the necessary information for incoming inspection or inventory control (see Figure 5-6). These include; customer product ID, QUALCOMM part number, date code of the SMT components, and quantity.

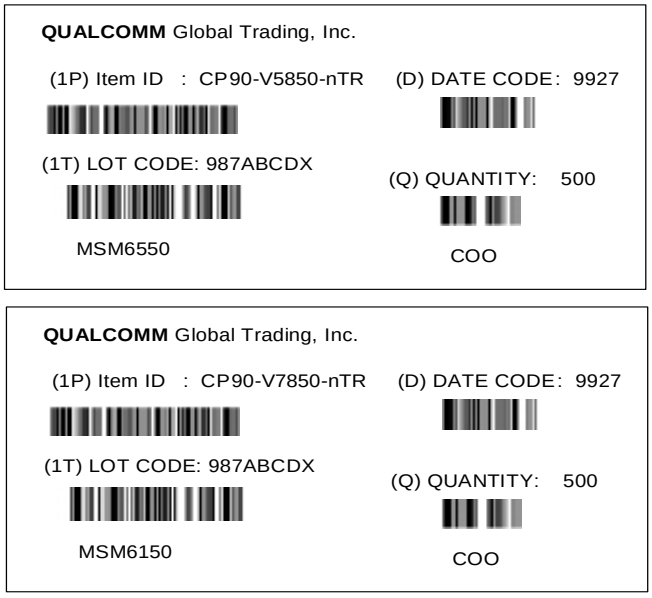

Figure 5-6 Barcode label examples

Moisture Barrier Bag (MBB). Inside the shipping box is an MBB containing components. The bag is strong, electrostatic discharge (ESD) safe, and allows **minimal** moisture transmission. It is sealed at the factory and should be handled carefully to avoid puncturing or tearing of the materials. A caution label (see Figure 5-8) on the bag outlines precautions that must be taken with desiccant-packed units. This label indicates the seal date of the enclosed MBB and the remaining shelf life. This bag protects the enclosed devices from moisture exposure and should not be opened until the devices are ready to be board mounted.

Desiccant. Each MBB contains pouch(es) of desiccant to absorb moisture that may be present in the bag. The humidity indicator card (see Figure 5-7) should be used as the primary method to determine whether the enclosed parts have absorbed excessive moisture. Do not bake or reuse the desiccant once it is removed from the MBB.

Humidity Indicator Card (HIC). Along with the desiccant pouches, the MBB contains a HIC. This card is a moisture indicator and is included to show the user the approximate relative humidity level within the bag. If the components have been exposed to moisture beyond the recommended limits for use in an SMT process, the units must be rebaked.

Six-dot and three-dot representations of the HIC are shown in Figure 5-7. If the 20% dot is *pink* and the 30% dot is *not blue* (six-dot HIC)—or the 5% dot is *pink* and the 10% dot is *not blue* (three-dot HIC)—then the components have exceeded the limit for moisture exposure and must be rebaked. The HIC is reversible and can be reused. The HIC is required for all moisture-sensitive devices.

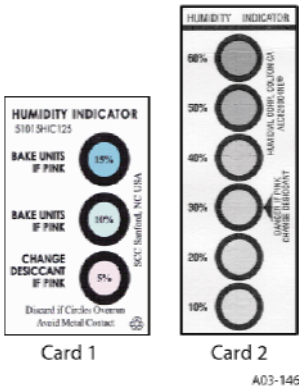

Figure 5-7 Humidity indicator card examples

Labels. Labels relevant to this process are the barcode label and caution label mentioned in the section on MBBs. The caution label (see Figure 5-8) outlines precautions that must be taken when handling desiccant-packed units if they are to be kept dry. The caution label is attached to the MBB; and contains the date that the bag was sealed (MM/DD/YY), the IPC/JEDEC J-STD-020 moisture sensitivity level, and the maximum floor life. The remaining storage life of the units in the bag is determined from the seal date. All components are guaranteed 12 months of shelf life starting from the seal date on the caution label.

Figure 5-8 Caution label

5.3 Moisture sensitivity level

Plastic encapsulated surface mount packages are sensitive to damage induced by absorbed moisture and temperature. QCT follows the latest revision IPC/JEDEC J-STD-020. Each package type is classified for moisture sensitivity by starting with a known dry part and soaking at various temperatures, relative humidity, and times. After soak, the packages are subjected to a reflow three times, with one of the following peak temperature conditions. All temperatures are measured at component body top.

- Standard component classification, 240 deg C max body temperature
- High temperature classification (lead-free solder), 250 deg C max body temperature.

6 Part Mounting Specification

6.1 Characterization

Characterization tests consist of optimizing the SMT process for the best board-level reliability possible. This is done by performing physical test on PCB test vehicles. The physical tests include bend-to-failure, bend cycle, tensile pull, drop shock, and temperature cycling.

Characterizing the land pattern, stencil design, and reflow profile prior to production is recommended.

The solder stencil print process must be optimized to ensure good print uniformity, which affects the reflowed solder fillet.

The solder stencil pattern design should also be optimized to decrease voiding and increase board level reliability.

Daisy chain packages are suitable for SMT characterization.

Solder paste manufacturing conditions should follow paste vendor recommendations for printing and reflow profile. See Table 6-1 for typical conditions and maximum component heat exposure.

Table 6-1 Typical reflow profile conditions and max component heat exposure

Profile Zones (Temp. measured at solder joint)	Description	Condition Limits (SnPb) STANDARD	Condition Limits (Lead-free) HIGH TEMPERATURE
Preheat	Initial heating	3 degrees C/sec max	3 degrees C/sec max
Soak	Dry out and flux activation	100 to 180 degrees C 120 to 180 sec typical	100-180 degrees C 180 to 240 sec
Reflow	Time above solder paste melting point	60 to 120 seconds	60-120 seconds
	Max component heat exposure*	230 degrees C	250 degrees C
Cool Down	Cool rate	6 degrees C/sec max	6 degrees C/sec max

Note: *Component heat exposure units are measured with thermocouple at the top surface of the QCT component.

6.2 Conditions for storage after unpacking

6.2.1 Storage conditions

The packages described in this document must be stored in a sealed moisture barrier, anti-static bag. Shelf life in a sealed moisture bag is 12 months at <40 °C and <90% RH.

6.2.2 Out-of-bag time duration

After unpacking, the package must be soldered to the PCB within the time listed on the moisture bag label, when factory conditions are <30 °C and <60% RH.

6.2.3 Baking

It is **not necessary** to bake the devices if the conditions described in Section 6.2.1 and Section 6.2.2 have **not** been exceeded.

It **is necessary** to bake the devices if the conditions described in either Section 6.2.1 or Section 6.2.2 **have been exceeded**. The baking conditions are 125 °C for 24 hours.

Devices cannot be baked in tape and reels (typically supplied by QCT) at the temperature described above.

7 Part Reliability Test Specification

7.1 Reliability qualifications summary

Table 7-1 and Table 7-2 present pre-qualification data taken on MSM6550 and MSM6150 engineering samples. Qualification of commercial-grade devices is underway and data will be provided by March 2005.

Table 7-1 Stress tests for the MSM6150 device (prequalification data)

Tests, Standards and Conditions	CP90-V7850-2	Pre-qual Data Result
Average Failure Rate (AFR) – HTOL JESD22-A108-A Temperature 140°C, Hours: 36	40	Pass
ESD – Human Body Model (HBM) JESD22-A114-B	3	2500 V
ESD – Charge Device Model (CDM) JESD22-C101-A	3	500 V
Latch-up (I-Test) EIA/JESD78 Trigger current ± 100 ma Temperature 85 °C	6	Pass
Latch-up (Vsupply Overvoltage) EIA/JESD78 Trigger voltage 1.5 X Vnominal Temperature 85 °C	6	Pass
Moisture Resistance Test (MRT) J-STD-020A Reflow @ 255 +5/-0 °C	Qualified by similarity	MSL 2A
Temperature Cycle JESD22-A104-B Temperature -55 °C to 125 °C, number of cycles: 1000 Soak mode: 1, minimum time at min/max temperature: 1 minute Cycle rate: 2 cycles per hour (cph) **Preconditioning** JESD22-A113-C MSL 2A Reflow temperature 255 +5/-0 °C	Qualified by similarity	Pass (using applicable generic data)

Tests, Standards and Conditions	CP90-V7850-2	Pre-qual Data Result
Highly Accelerated Stress Test (HAST) JESD22-A110-B Preconditioning JESD22-A113-D MSL 2A Reflow temperature 255 +5/-0 °C	Qualified by similarity	Pass (using applicable generic data)
High Temperature Storage Life JESD22-A103-B Temperature 175 °C, hours: 500	Qualified by similarity	Pass (using applicable generic data)
Flammability UL-STD-94	Certificate	Pass
Physical Dimensions JESD22-B100-A BGA/CSP package user guide	3 X 1	Pass

Table 7-2 Stress tests for the MSM6550 device (prequalification data)

Tests, Standards and Conditions	CP90-V5850-2	Pre-qual Data Result
Average Failure Rate (AFR) – **HTOL** JESD22-A108-A Temperature 140°C, hours: 36	40	Pass
ESD – Human Body Model (HBM) JESD22-A114-B	3	2500 V
ESD – Charge Device Model (CDM) JESD22-C101-A	3	500 V
Latch-up (I-Test) EIA/JESD78 Trigger current ±100 ma Temperature 85 °C	6	Pass
Latch-up (Vsupply Overvoltage) EIA/JESD78 Trigger voltage 1.5 X Vnominal Temperature 85°C	6	Pass
Moisture Resistance Test (MRT) J-STD-020A Reflow @ 255 +5/-0 °C	Qualified by similarity	MSL 2A

Tests, Standards and Conditions	CP90-V5850-2	Pre-qual Data Result
Temperature Cycle JESD22-A104-B Temperature: -55 °C to 125 °C; number of cycles: 1000 Soak mode: 1, minimum time at min/max temperature: 1 minute Cycle Rate: 2 cycles per hour (cph) **Preconditioning** JESD22-A113-C MSL 2A Reflow temperature 255 +5/-0 °C	Qualified by similarity	Pass (using applicable generic data)
Highly Accelerated Stress Test (HAST) JESD22-A110-B Preconditioning JESD22-A113-D MSL 2A Reflow temperature 255 +5/-0 °C	Qualified by similarity	Pass (using applicable generic data)
High Temperature Storage Life JESD22-A103-B Temperature 175 °C, hours: 500	Qualified by similarity	Pass (using applicable generic data)
Flammability UL-STD-94	Certificate	Pass
Physical Dimensions JESD22-B100-A BGA/CSP package user guide	3 X 1	Pass

7.2 Qualification sample description

Device Characteristics:

Device Name	MSM6150
Package Type	409CSP
Package Body Size	14 mm x 14 mm
Ball Count	409
Ball Composition	Sn/4.0Ag/0.5Cu % by weight
Process	0.13 µm
Fab Site	TSMC
Assembly Site	ChipPAC and ASE
Ball Pitch	0.5 mm

Device Characteristics:

Device Name	MSM6550
Package Type	409CSP
Package Body Size	14 mm x 14 mm
Ball Count	409
Ball Composition	Sn/4.0Ag/0.5Cu % by weight
Process	0.13 µm
Fab Site	TSMC
Assembly Site	ChipPAC and ASE
Ball Pitch	0.5 mm