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REVISION RECORD

SYM	ECO NO.	APPROVED:	DATE:

DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code> SIZE: A0 DRAWING NO: Drawing Number REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale> SHEET: 1 OF 34

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02.26 By wangxiuqun

1. TP2706, 100k R2720
2. U2710 SN74AUC1G240YZPR FORCE_USB_BOOT VREG_L5_1P8 ,TP2725,TP2726
3. R2837 NC R2840 EN_N
4. battery thermal NTC R2730,
5. GPIO140 Nmos Q2703,R2732(100K)
6. ADC ,PMI8952 MPP1(PIN22) J2701PIN26.
7. TP3,TP4,FV2411,FV2412
8. FV2702 2 TVSFV2701FV2702.
9. WPC_LS_FLAG 2 R2841,R2842
10. NTC R2728

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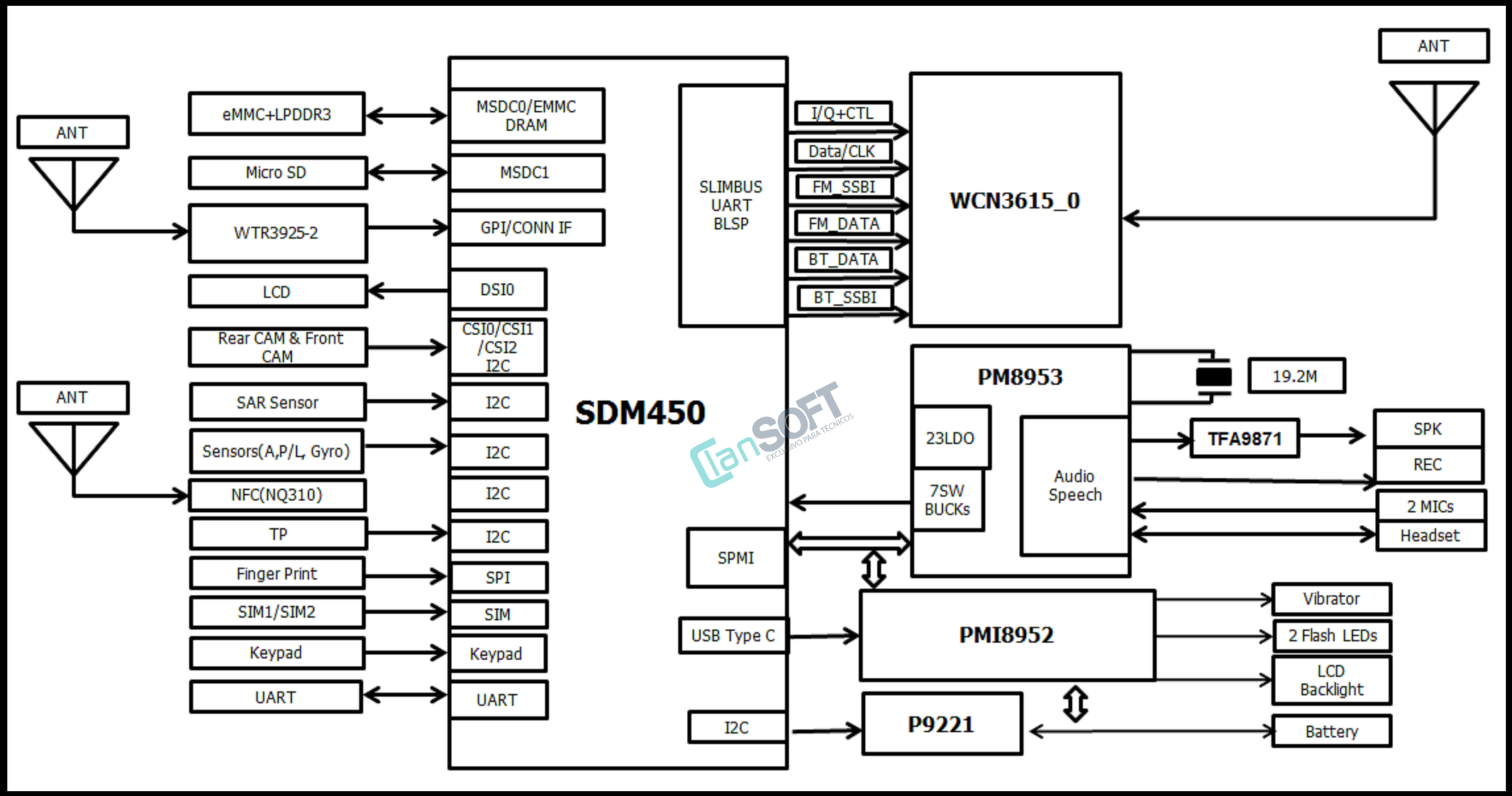
ANT
ANT
ANT
eMMC+LPDDR3
Micro SD
WTR3925-2
LCD
Rear CAM & Front CAM
SAR Sensor
Sensors(A,P/L, Gyro)
NFC(NQ310)
TP
Finger Print
SIM1/SIM2
Keypad
UART
MSDC0/EMMC DRAM
MSDC1
GPI/CONN IF
DSI0
CSI0/CSI1 /CSI2 I2C
I2C
I2C
I2C
I2C
SPI
SIM
Keypad
UART
SDM450
SLIMBUS UART BLSP
I/Q+CTL
Data/CLK
FM_SSBI
FM_DATA
BT_DATA
BT_SSBI
WCN3615_0
ANT
PM8953
19.2M
23LDO
7SW BUCKs
Audio Speech
TFA9871
SPK
REC
2 MICs
Headset
SPMI
USB Type C
I2C
PMI8952
P9221
Vibrator
2 Flash LEDs
LCD Backlight
Battery

MSM8953 GPIO Configuration For QRD8953

GPIO_0	NFC_SPI_ESE_MOSI	GPIO_41		GPIO_82	FM_DATA
GPIO_1	NFC_SPI_ESE_MISO	GPIO_42	ACCL_INT1	GPIO_83	BT_CTL
GPIO_2	NFC_SPI_ESE_CS_N	GPIO_43	ALSP_INT_N	GPIO_84	BT_DATA
GPIO_3	NFC_SPI_ESE_CLK	GPIO_44	MAG_DRDY_INT	GPIO_85	KEY_VOL_UP_N
GPIO_4	UART_MSM_TX	GPIO_45	GYRO_INT	GPIO_86	
GPIO_5	UART_MSM_RX	GPIO_46	SCAM_D_ELDO_EN	GPIO_87	
GPIO_6		GPIO_47	SENSOR_SPI_CS2_N	GPIO_88	
GPIO_7		GPIO_48	FP_INT_N	GPIO_89	
GPIO_8		GPIO_49	UIM_BATT_ALARM	GPIO_90	
GPIO_9		GPIO_50	WCD_ELDO_EN	GPIO_91	
GPIO_10	TP_I2C_SDA	GPIO_51	UIM1_DATA	GPIO_92	
GPIO_11	TP_I2C_SCL	GPIO_52	UIM1_CLK	GPIO_93	SCAM_ID
GPIO_12		GPIO_53	UIM1_RESET	GPIO_94	
GPIO_13		GPIO_54		GPIO_95	
GPIO_14	SENSOR_I2C_SDA	GPIO_55	UIM2_DATA	GPIO_96	WSA_EN
GPIO_15	SENSOR_I2C_SCL	GPIO_56	UIM2_CLK	GPIO_97	
GPIO_16	NFC_DISABLE	GPIO_57	UIM2_RESET	GPIO_98	
GPIO_17	NFC_IRQ	GPIO_58		GPIO_99	
GPIO_18	NFC_I2C_SDA	GPIO_59		GPIO_100	GRFC0_SEL
GPIO_19	NFC_I2C_SCL	GPIO_60	GP_PDM_A0	GPIO_101	GRFC1_SEL
GPIO_20	SENSOR_SPI_MOSI	GPIO_61	LCD_RST_N	GPIO_102	GRFC2_SEL
GPIO_21	SENSOR_SPI_MISO	GPIO_62	NFC_DWL_REQ	GPIO_103	GRFC3_SEL
GPIO_22	SENSOR_SPI_CS0_N	GPIO_63		GPIO_104	GRFC4_SEL
GPIO_23	SENSOR_SPI_CLK	GPIO_64	TP_RST_N	GPIO_105	GRFC5_SEL
GPIO_24	LCD_TE0	GPIO_65	TP_INT_N	GPIO_106	WDOG_DISABLE
GPIO_25		GPIO_66		GPIO_107	GRFC7_SEL
GPIO_26	CAM_MCLK0	GPIO_67	WCD_RST_N	GPIO_108	GRFC8_SEL
GPIO_27	CAM_MCLK1	GPIO_68		GPIO_109	GRFC9_SEL
GPIO_28		GPIO_69	WCD_MSM_MCLK	GPIO_110	
GPIO_29	CAM_I2C_SDA0	GPIO_70	SLIMBUS_CLK	GPIO_111	
GPIO_30	CAM_I2C_SCL0	GPIO_71	SLIMBUS_DATA0	GPIO_112	
GPIO_31	CAM_I2C_SDA1	GPIO_72		GPIO_113	
GPIO_32	CAM_I2C_SDA1	GPIO_73	WCD_INTR1	GPIO_114	
GPIO_33		GPIO_74	WCD_INTR2	GPIO_115	
GPIO_34	FLASH_STROBE_NOW	GPIO_75	BT_SSBI	GPIO_116	EXT_GPS_LNA_EN
GPIO_35		GPIO_76	WL_CMD_DATA_2	GPIO_117	CHO_GSM_TX_PHASE_D0
GPIO_36		GPIO_77	WL_CMD_DATA_1	GPIO_118	RFFE1_CLK
GPIO_37	FORCE_USB_BOOT	GPIO_78	WL_CMD_DATA_0	GPIO_119	RFFE1_DATA
GPIO_38		GPIO_79	WL_CMD_SET	GPIO_120	RFFE2_CLK
GPIO_39	MCAM_PWD_N	GPIO_80	WL_CMD_CLK	GPIO_121	RFFE2_DATA
GPIO_40	MCAM_RST_N	GPIO_81	FM_SSBI	GPIO_122	RFFE4_CLK

GPIO_123	RFFE4_DATA	GPIO_134	
GPIO_124		GPIO_135	FP_SPI_CLK
GPIO_125		GPIO_136	FP_SPI_CS
GPIO_126	RFFE3_CLK	GPIO_137	FP_SPI_MOSI
GPIO_127	RFFE3_DATA	GPIO_138	FP_SPI_MISO
GPIO_128		GPIO_139	USB_SS_SEL
GPIO_129	SCAM_RST_N	GPIO_140	FP_RST_N
GPIO_130	SCAM_PWD_N	GPIO_141	NFC_ESE_PWR_REQ
GPIO_131			
GPIO_132			
GPIO_133	SDCARD_DET_N		

PMI8952 GPIO/MPP Configuration For QRD8953

GPIO_1		MPP_1	
GPIO_2		MPP_2	GREEN_LED
		MPP_3	
		MPP_4	FLASH_STROBE_NOW

PM8953 GPIO/MPP Configuration For QRD8953

GPIO_1	CODEC_DIV_CLK	MPP_1	VDD_PX_BIAS_MPP_1
GPIO_2	NFC_CLK_REQ(SDCARD_DET_N)	MPP_2	PA_THERM1
GPIO_3	UIM_BATT_ALARM	MPP_3	VREF_DAC_MPP_3
GPIO_4		MPP_4	QUIET_THERM
GPIO_5			
GPIO_6			
GPIO_7	VBUS_USB_IN		
GPIO_8	USB_ID		

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GPIO TABLE

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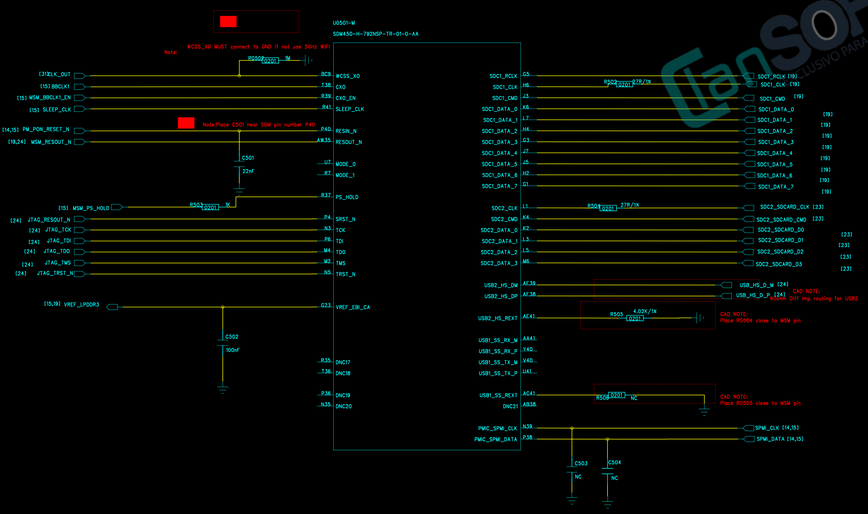

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MSM8953 Control

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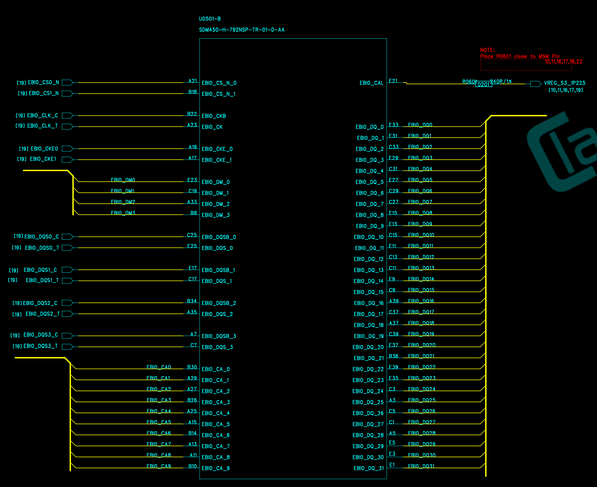

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MSM8953 EBI

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GPIO_37	FORCED_USB_BOOT
GPIO_106	WDOG_DISABLE
GPIO_108	APPS_BOOT_FROM_ROW

BOOT_CONFIG[2:1]	BOOT_CONFIG
0b000	SDC1 -> SDC2 -> USB2.0
0b001	SDC2 -> SDC1-> USB2.0
0b010	SDC1-> USB2.0
0b011	USB2.0

Default Boot Config (0b000) is SDC1(eMMC)

MSM8953 GPIO

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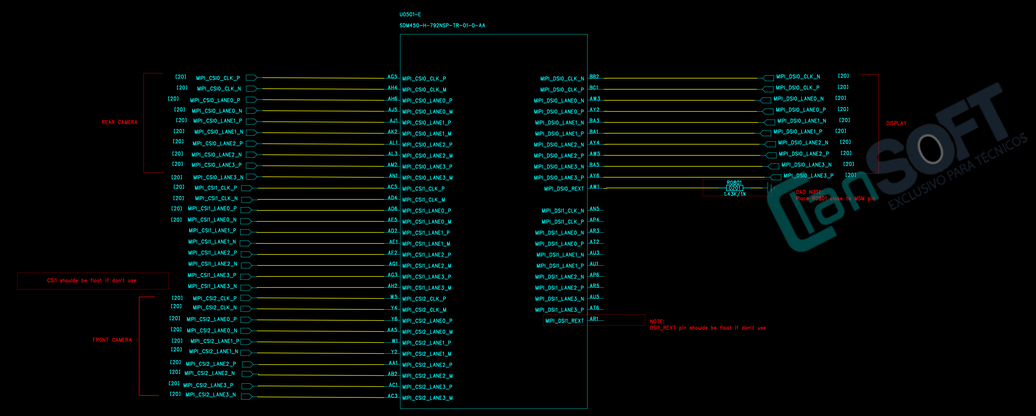
DRAWING NO: <Drawing Number> REV: <Revision>



CSI Pin Name	CSI DPHY 4-lane	CSI DPHY 2+1 Mode	CSI CPHY 3Phase Mode
CSI0_3PHASE_PIN0	CSI0_CLKP	CSI0_2LANE_CLKP	NC
CSI0_3PHASE_PIN1	CSI0_CLKN	CSI0_2LANE_CLKN	CSI0_TRI0_A
CSI0_3PHASE_PIN2	CSI0_DP0	CSI0_2LANE_DP0	CSI0_TRI0_B
CSI0_3PHASE_PIN3	CSI0_DN0	CSI0_2LANE_DN0	CSI0_TRI0_C
CSI0_3PHASE_PIN4	CSI0_DP1	CSI0_2LANE_DP1	CSI0_TRI1_A
CSI0_3PHASE_PIN5	CSI0_DN1	CSI0_2LANE_DN1	CSI0_TRI1_B
CSI0_3PHASE_PIN6	CSI0_DP2	CSI0_1LANE_DP0	CSI0_TRI1_C
CSI0_3PHASE_PIN7	CSI0_DN2	CSI0_1LANE_DN0	CSI0_TRI2_A
CSI0_3PHASE_PIN8	CSI0_DP3	CSI0_1LANE_CLKP	CSI0_TRI2_B
CSI0_3PHASE_PIN9	CSI0_DN3	CSI0_1LANE_CLKN	CSI0_TRI2_C
CSI1_3PHASE_PIN0	CSI1_CLKP	CSI1_2LANE_CLKP	NC
CSI1_3PHASE_PIN1	CSI1_CLKN	CSI1_2LANE_CLKN	CSI1_TRI0_A
CSI1_3PHASE_PIN2	CSI1_DP0	CSI1_2LANE_DP0	CSI1_TRI0_B
CSI1_3PHASE_PIN3	CSI1_DN0	CSI1_2LANE_DN0	CSI1_TRI0_C
CSI1_3PHASE_PIN4	CSI1_DP1	CSI1_2LANE_DP1	CSI1_TRI1_A
CSI1_3PHASE_PIN5	CSI1_DN1	CSI1_2LANE_DN1	CSI1_TRI1_B
CSI1_3PHASE_PIN6	CSI1_DP2	CSI1_1LANE_DP0	CSI1_TRI1_C
CSI1_3PHASE_PIN7	CSI1_DN2	CSI1_1LANE_DN0	CSI1_TRI2_A
CSI1_3PHASE_PIN8	CSI1_DP3	CSI1_1LANE_CLKP	CSI1_TRI2_B
CSI1_3PHASE_PIN9	CSI1_DN3	CSI1_1LANE_CLKN	CSI1_TRI2_C
CSI2_3PHASE_PIN0	CSI2_CLKP	CSI2_2LANE_CLKP	NC
CSI2_3PHASE_PIN1	CSI2_CLKN	CSI2_2LANE_CLKN	CSI2_TRI0_A
CSI2_3PHASE_PIN2	CSI2_DP0	CSI2_2LANE_DP0	CSI2_TRI0_B
CSI2_3PHASE_PIN3	CSI2_DN0	CSI2_2LANE_DN0	CSI2_TRI0_C
CSI2_3PHASE_PIN4	CSI2_DP1	CSI2_2LANE_DP1	CSI2_TRI1_A
CSI2_3PHASE_PIN5	CSI2_DN1	CSI2_2LANE_DN1	CSI2_TRI1_B
CSI2_3PHASE_PIN6	CSI2_DP2	CSI2_1LANE_DP0	CSI2_TRI1_C
CSI2_3PHASE_PIN7	CSI2_DN2	CSI2_1LANE_DN0	CSI2_TRI2_A
CSI2_3PHASE_PIN8	CSI2_DP3	CSI2_1LANE_CLKP	CSI2_TRI2_B
CSI2_3PHASE_PIN9	CSI2_DN3	CSI2_1LANE_CLKN	CSI2_TRI2_C

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MSM8953 MIPI

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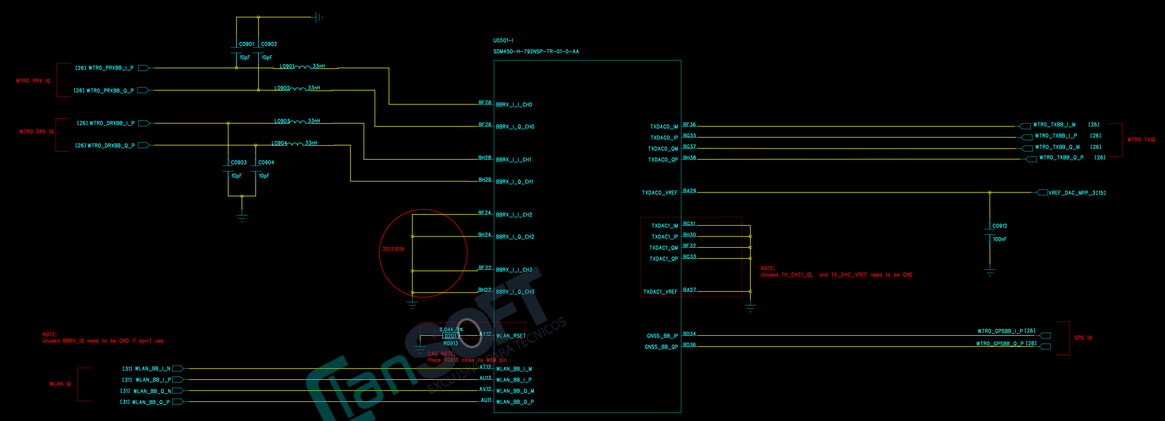

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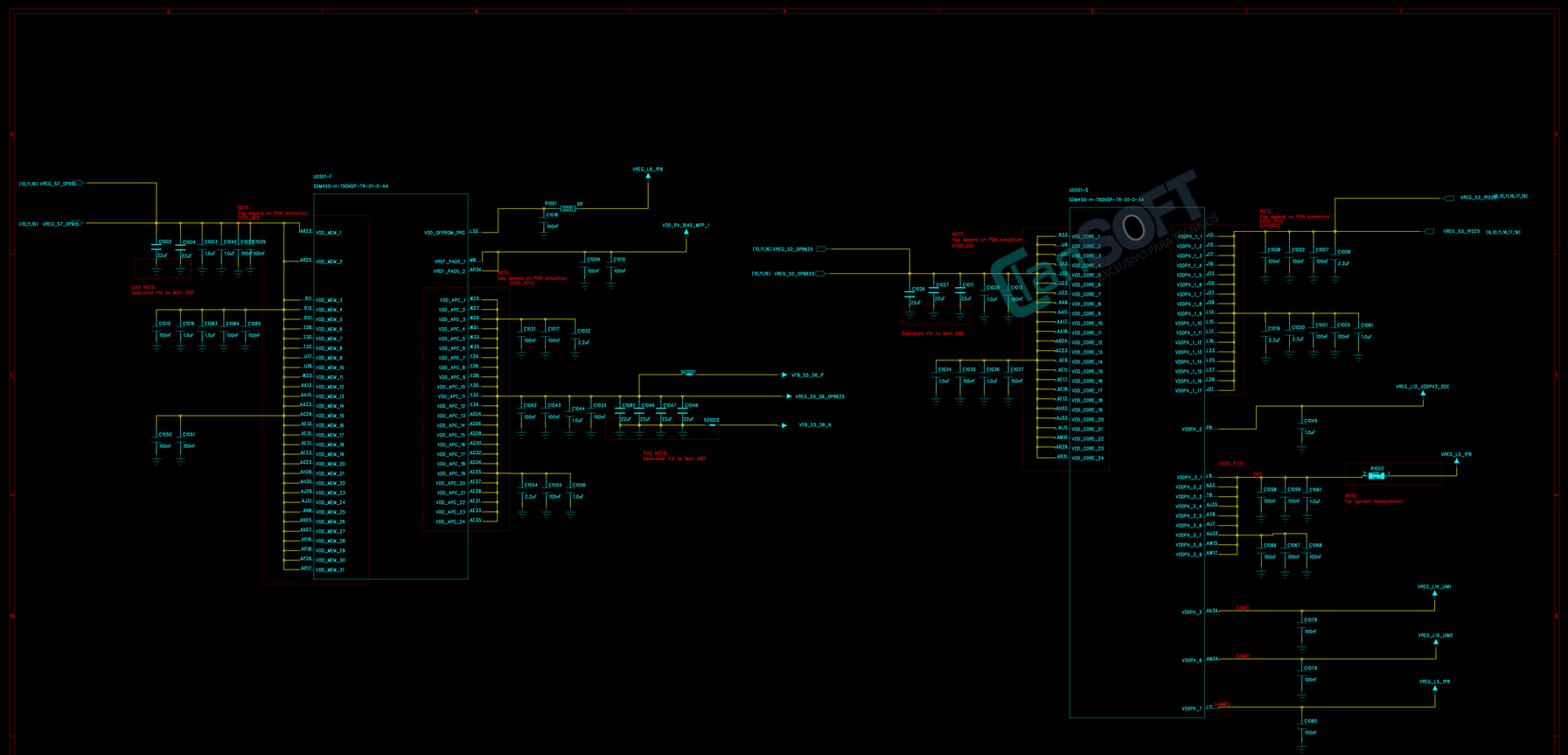

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SDM450 POWER1

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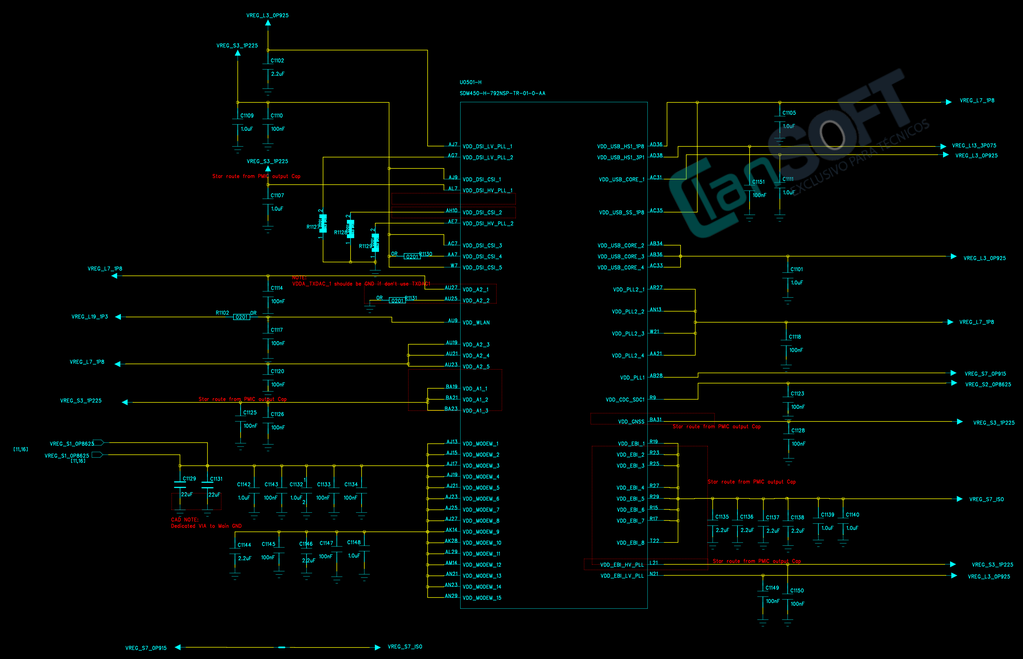

CAD NOTE:
About star route from PMIC output Cap:

SDM450 POWER2

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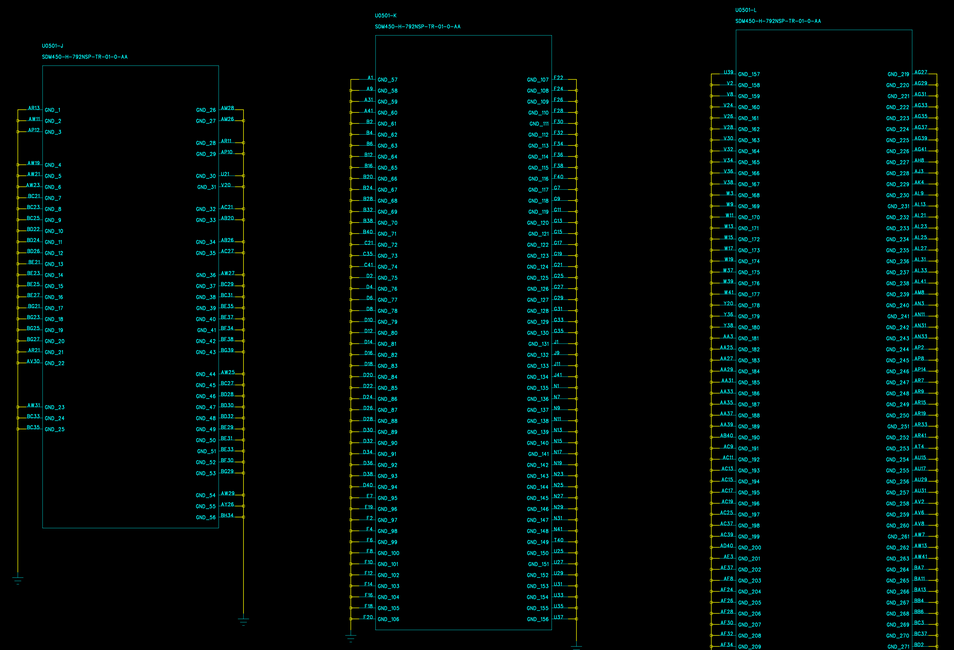

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MSM8953 GND

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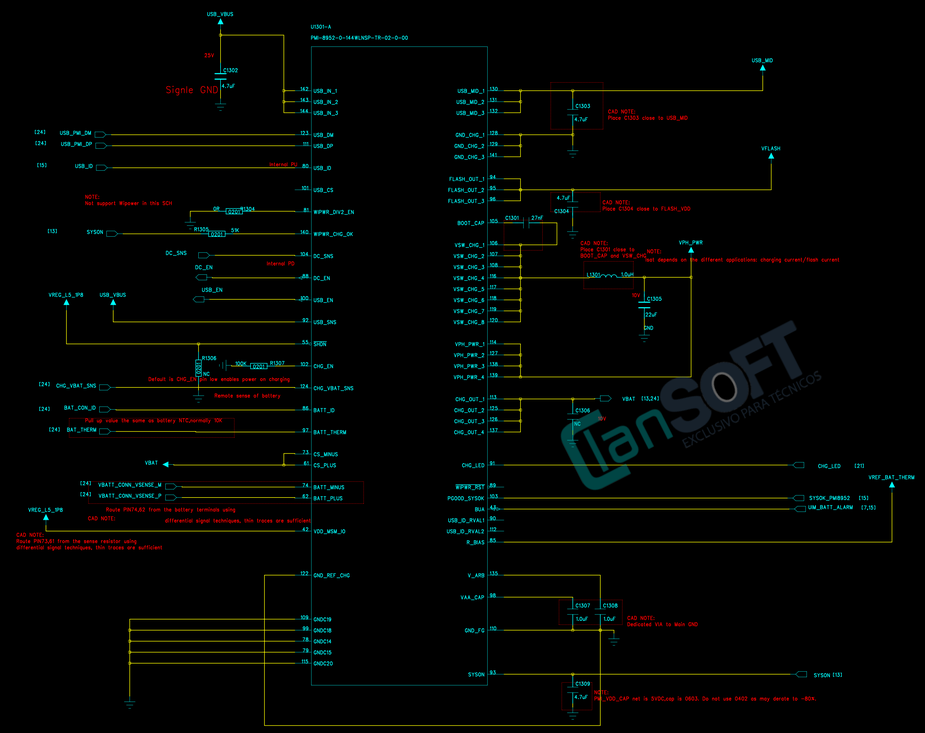
PM_PIN	connection on device without Wipower	connection on device with Wipower
CHG_OK	Pull up to VDD_CAP with 51ohm	Stark PMU CHG_OK
DVD_EN	Pull down to GND with 0ohm	Stark PMU DVD_EN
CPVD2	No Connect For parallel charging Connects to SMB EN Do NOT pull up to VDD_CAP	10ohm pull down to gnd For parallel charging Connects to SMB EN pin Do NOT pull up to VDD_CAP

Use C1302= 4.7uF for Single Charging Config
Use C1302 = 2.2uF for Parallel Charging Config



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PMI8952 Charger

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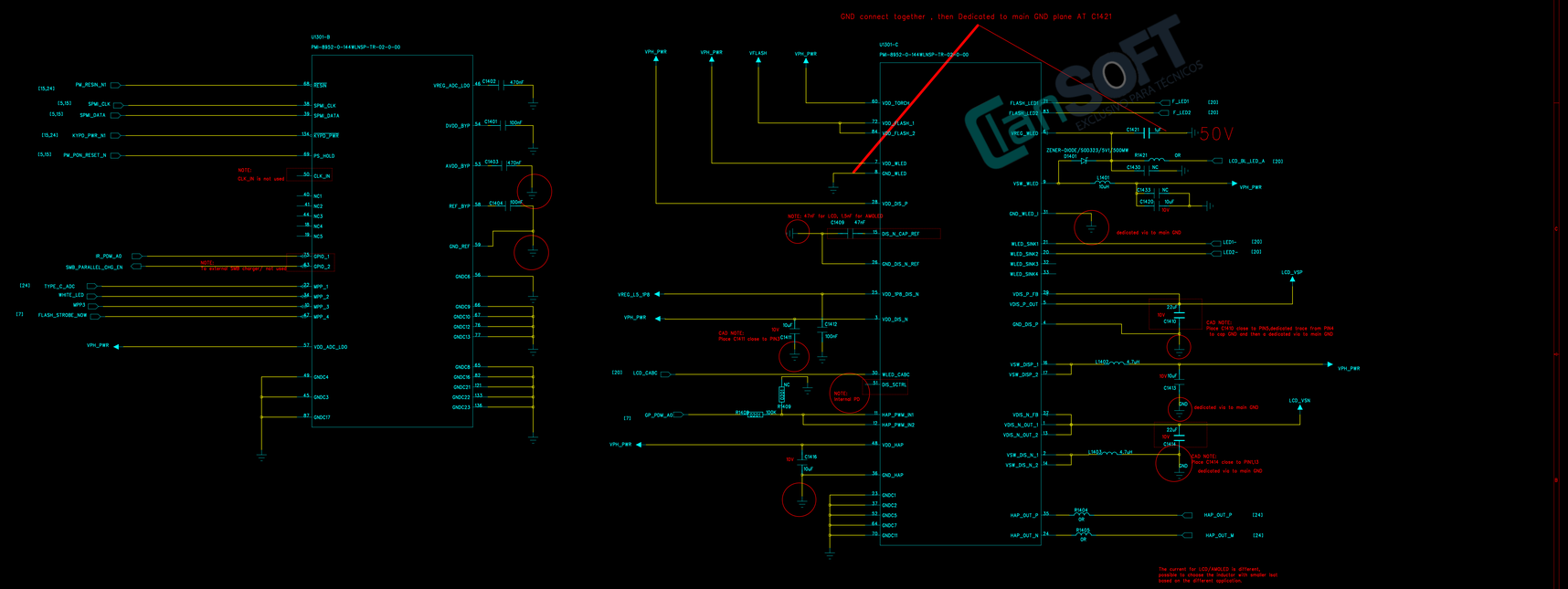

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PMI8952 Control/Interface

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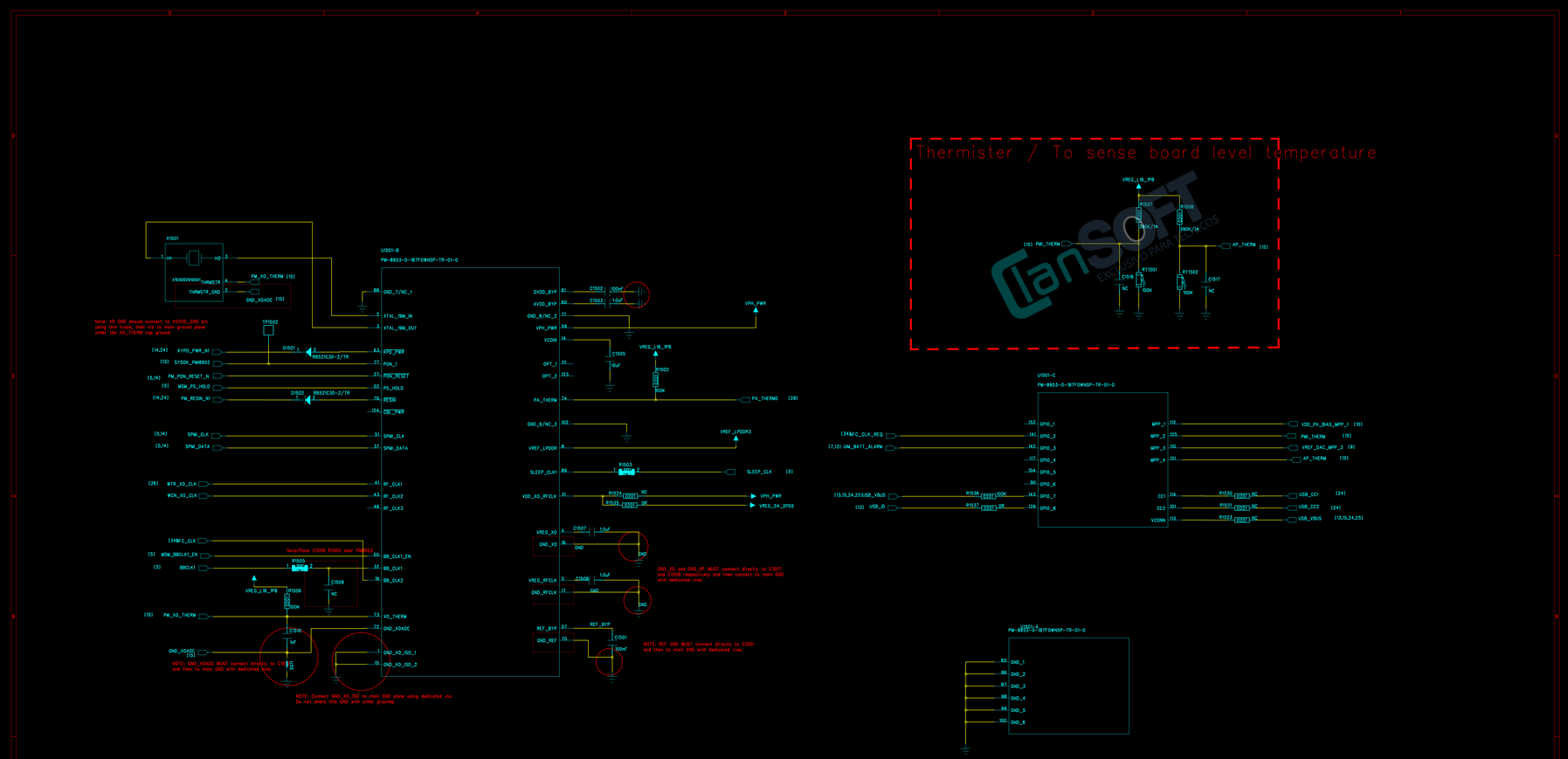

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PM8953 Control/Interface

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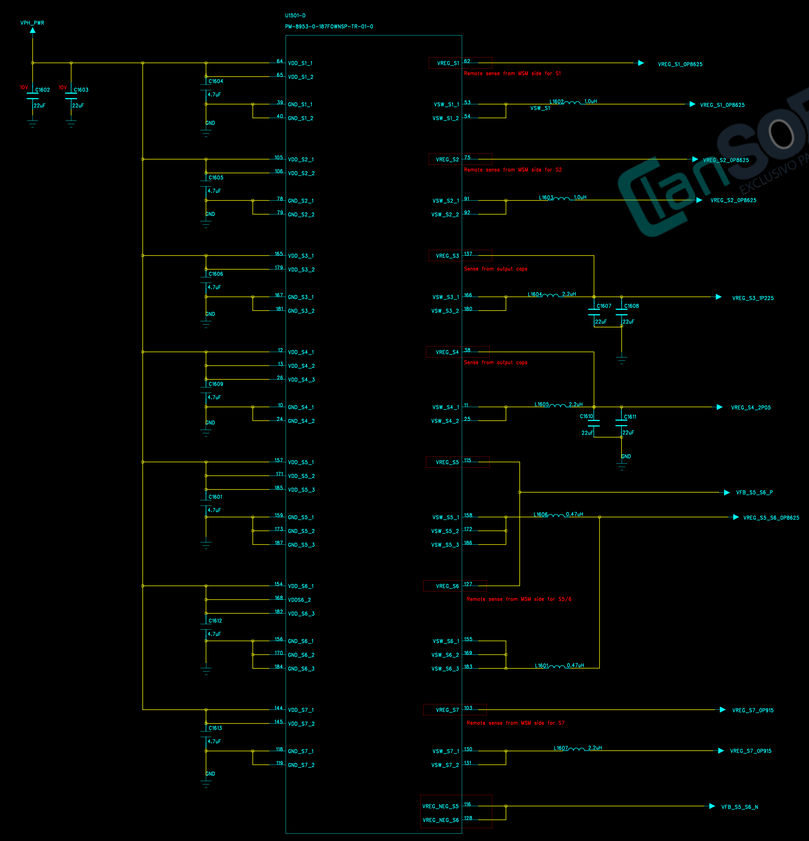

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PM8953 SMPS

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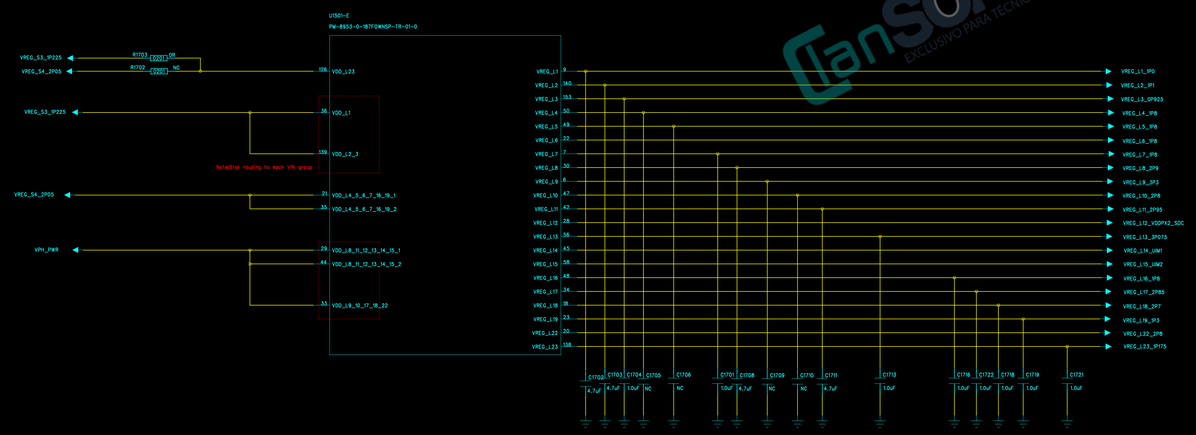

Table 3-6 PM8937/PM8940 regulators and their intended uses

Function	Circuit type	Default V (V) [1]	Specified range (V) [2] (MSM8937)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8937)
S1	ULT-SMPS	1.225	0.900–1.350	0.375–1.5625	2000[3]	N	MSM modem
S2	ULT-SMPS	1.225	0.550–1.350	0.375–1.5625	3000	Y	MSM core and graphics
S3	HF-SMPS	1.288	1.200–1.4125	0.375–1.5625	2700	Y	Low-voltage LDOs (1, 2, 3, 19, and 23)
S4	ULT-SMPS	2.050	1.800–2.050	1.550–3.126	2500	Y	High-voltage LDOs (4, 5, 6, 7, 16, RFCLK, and XO)
S5	FT-SMPS	1.225	1.050–1.350	0.350–1.355	3000	Y	MSM applications processor
S6	FT-SMPS	1.225	1.050–1.350	0.350–1.355	3000	N	MSM applications processor
L1	NMOS LDO	1.000	1.000	0.375–1.5375	1200	N	RFICs
~~L2~~	~~NMOS LDO~~	~~1.200~~	~~1.200~~	~~0.375–1.5375~~	~~1200~~	~~Y~~	~~LPDDR2/LPDDR3, MIPI CSI, and DSI~~
L3	NMOS LDO	1.225	0.750–1.350	0.375–1.5375	1200	Y	VDDMX
L4	PMOS LDO	1.800	1.800	1.750–3.3375	450	N	RFICs and GPS eLNA
L5 [4]	PMOS LDO	1.800	1.800	1.750–3.3375	500	Y	Most digital I/Os, MSM pad groups 3 and 7, LPDDR, and eMMC
L6	PMOS LDO	1.800	1.800	1.750–3.3375	300	N	MSM DSI PLL and OTP, camera, touchscreen, display, and sensors
L7	PMOS LDO	1.800	1.800	1.750–3.3375	150	Y	MSM analog and PLLs, WCN XO, and PM baseband clock driver
L8	PMOS LDO	2.900	2.900	1.750–3.3375	600	Y	eMMC
L9	PMOS LDO	V_{out} = 3.3 V for VBAT > 3.575 V; V_{out} = 3 V for VBAT < 3.575 V	3.000–3.300	1.750–3.3375	600	N	WCN
L10	PMOS LDO	2.8	2.800	1.750–3.3375	150	N	Sensors
L11 [5]	PMOS LDO	2.950	2.950	1.750–3.3375	800	Y	Micro SD
L12 [4]	PMOS LDO	2.950	1.800/2.950	1.750–3.3375	150	Y	MSM pad group 2 and SDC2
L13	PMOS LDO	3.075	3.075	1.750–3.3375	50	Y	MSM USB and audio

Function	Circuit type	Default V (V) [1]	Specified range (V) [2] (MSM8937)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8937)
L14 [5]	PMOS LDO	1.800	1.800/2.925/3.050	1.750–3.3375	50	N	MSM pad group 5, dual-voltage UIM1, a
L15 [5]	PMOS LDO	1.800	1.800/2.925/3.050	1.750–3.3375	50	N	MSM pad group 6 and dual-voltage UIM
L16	PMOS LDO	1.800	1.800	1.750–3.3375	5	N	PMIC HKADC
L17	PMOS LDO	2.850	2.850	1.750–3.3375	600	N	Camera, display, and touchscreen
L18	PMOS LDO	2.700	2.700	1.750–3.3375	150	N	QTI RF front-end
L19	NMOS LDO	1.350	1.350	0.375–1.5375	1200	N	MSM analog, WCN, and WGR
L20	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC XO circuits
L21	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC RF clock buffers
L22	PMOS LDO	2.800	2.800	1.750–3.3375	300	N	Camera – analog
L23	NMOS LDO	1.3	1.2	0.375–1.5375	300	N	Camera – digital

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PM8953 LD

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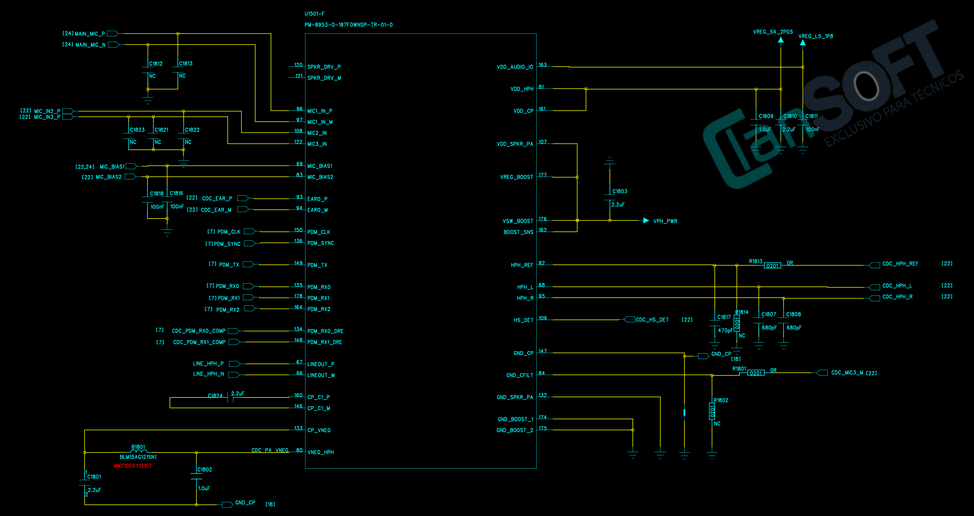
San Diego, CA 92121-1714
U.S.A.

Title
Size Name Rev
Date Sheet of



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PM8953 CODEC/Audio PA

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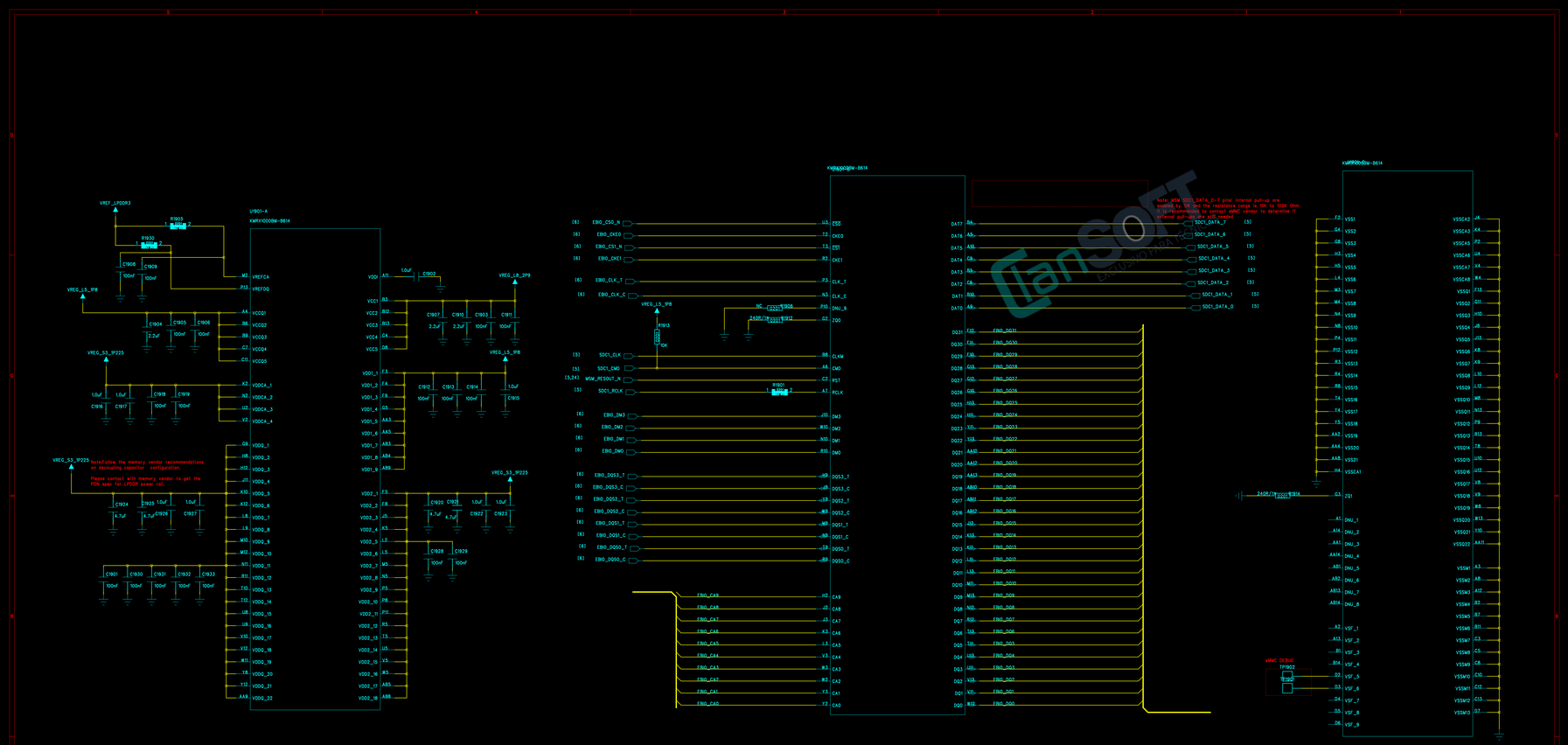
Size | Name | Sheet | Rev

Date | Sheet of



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MEMORY(LPDDR3+EMMC V5.1)

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Title

Size | Sheet Name | Rev

Date | Sheet of

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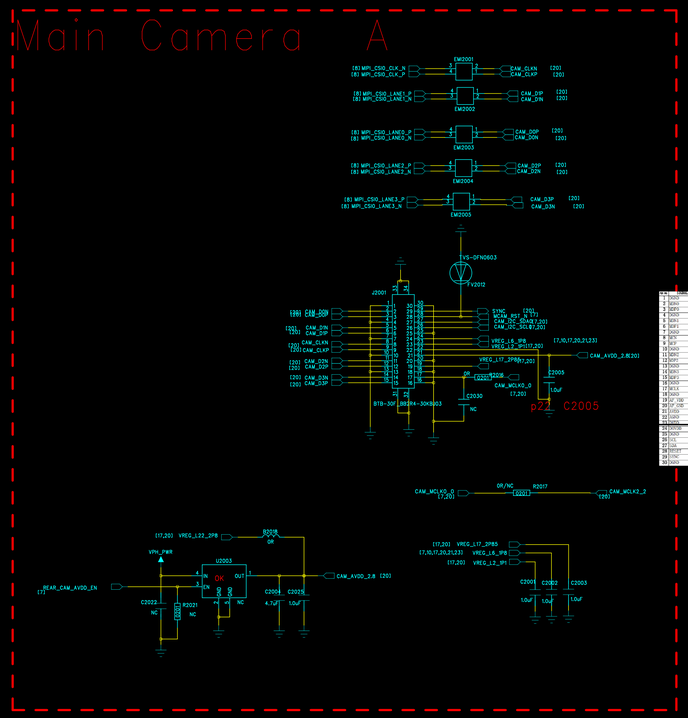
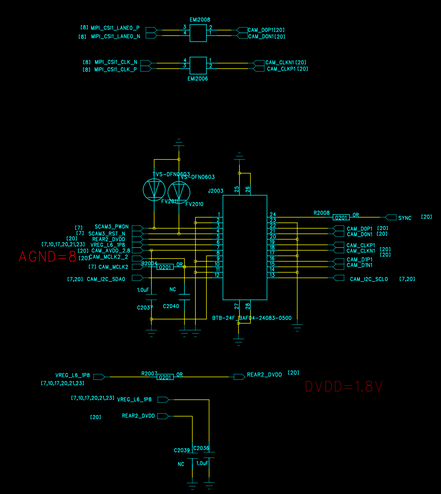
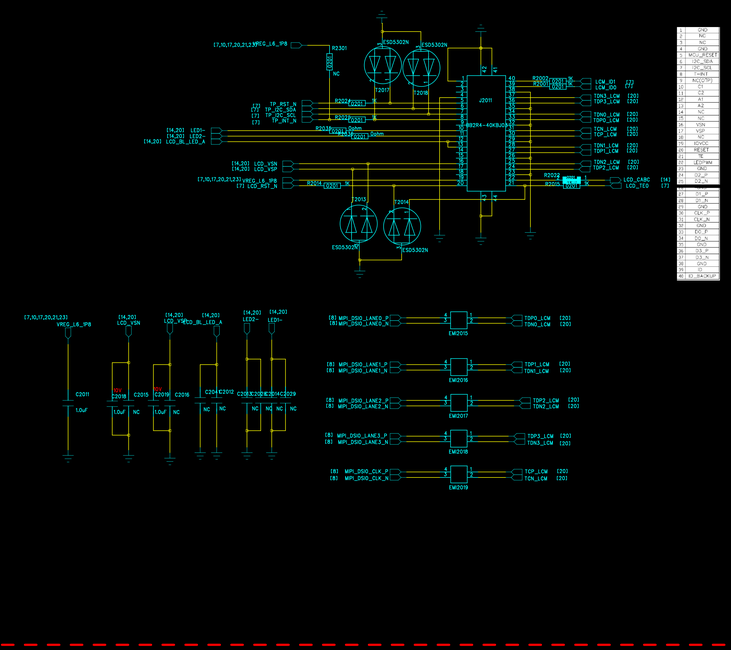
Main Camera A



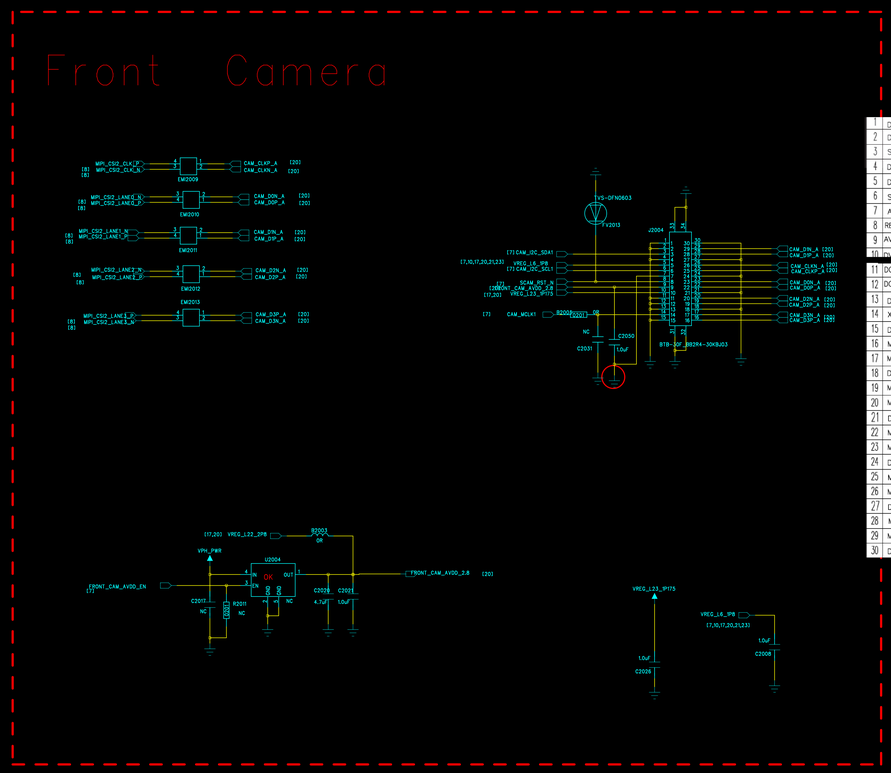
Main Camera B



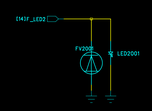
LCM



Front Camera

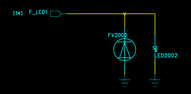


Front FLASHLIGHT



1	DGND
2	DGND
3	SDA
4	DGND
5	DOVDD
6	SCL
7	AGND
8	RESET
9	AVDD
10	NVDD
11	DGND
12	DGND
13	DGND
14	XCLK
15	DGND
16	MDP3
17	MDN3
18	DGND
19	MDP2
20	MDN2
21	DGND
22	MDP0
23	MDN0
24	DGND
25	MCP
26	MCN
27	DGND
28	MDP1
29	MDN1
30	DGND

Main FLASHLIGHT



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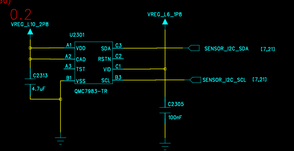
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 20 OF 34

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

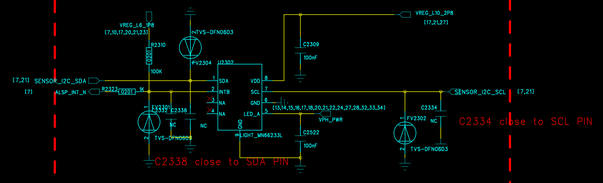
M-Sensor

I2C address :110000(30)

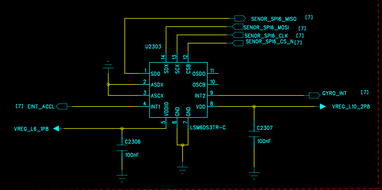
0.2

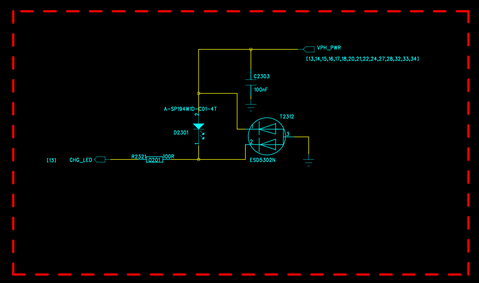


P_SENSOR 0x92

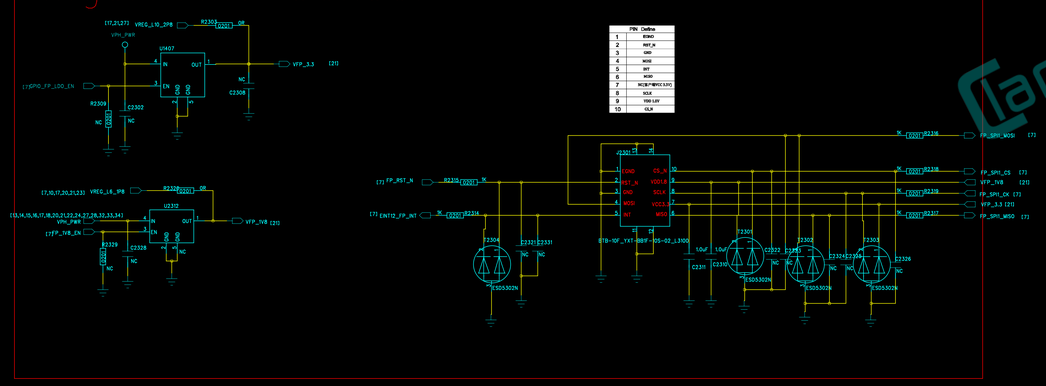


A+Gyro-Sensor





FingerPrint-Sensor



PIN	Define
1	CONO
2	RST_N
3	GND
4	MOSI
5	INT
6	MISO
7	VCC3.3(+3V3(1.5V))
8	SCLK
9	VDD1.8(1.8V)
10	CLK

[7,10,17,20,21,23] VREG_L6_1P8

MARK POINT

COMPANY: <Company Name>					
TITLE: <Title>					
DRAWN: <Drawn By>	DATED: <Drawn Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
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REVISION RECORD			
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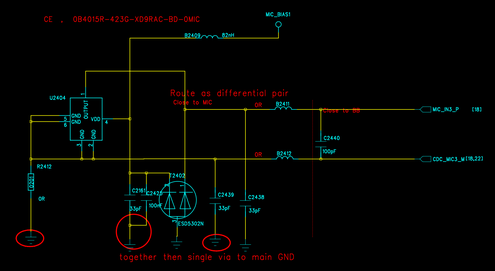
Sub MIC



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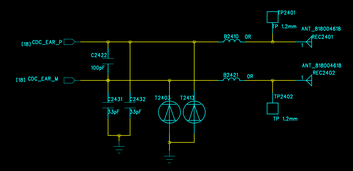
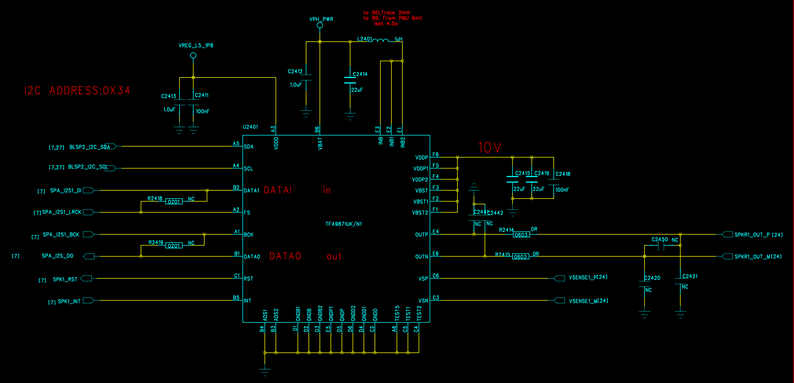
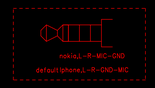


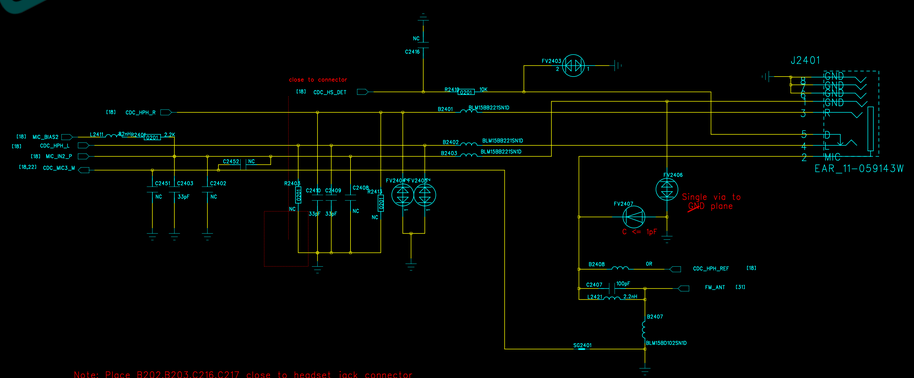
Audio PA



Earphone Audio



Note: Ferrite beads and their corresponding bypass capacitors on on CDC_HPH_L_P, CDC_HPH_L_M and CDC_HPH_REF are needed to reduce noise generated by audio/FM concurrency



Note: Place B202,B203,C216,C217 close to headset jack connector

Note: For Cable detection

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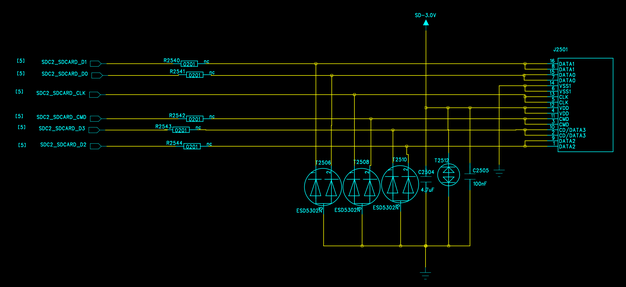
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 22 OF 34

LTR	ECO NO:	APPROVED:	DATE:

T-Card



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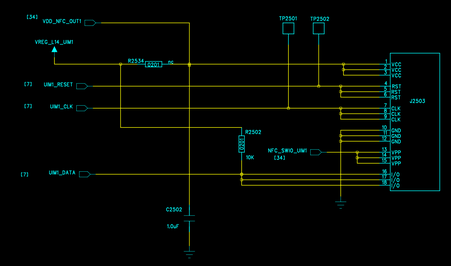

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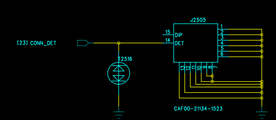
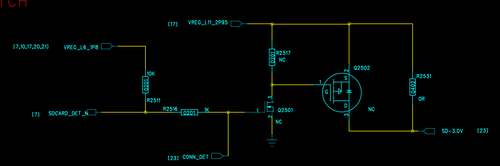
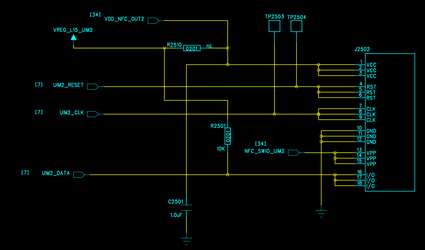


TF SWITCH



SIM2



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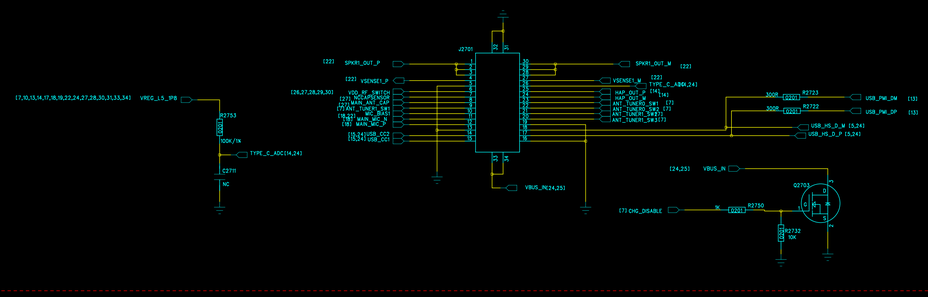
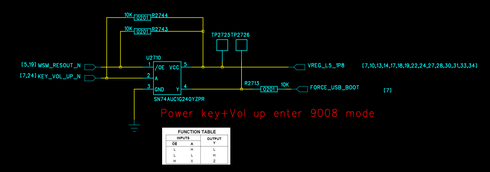
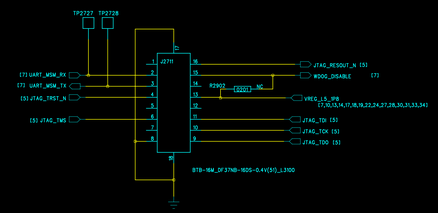
SUB_FPC



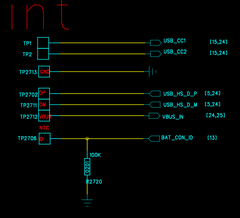


Power key+Vol up enter 9008 mode

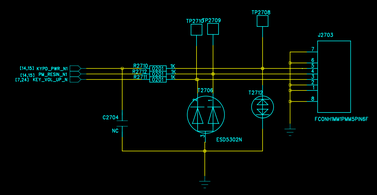
FUNCTION TABLE		
INPUTS		OUTPUT
OE	A	Y
L	L	L
L	H	H
H	L	Z
H	H	Z



Test point



Power Key

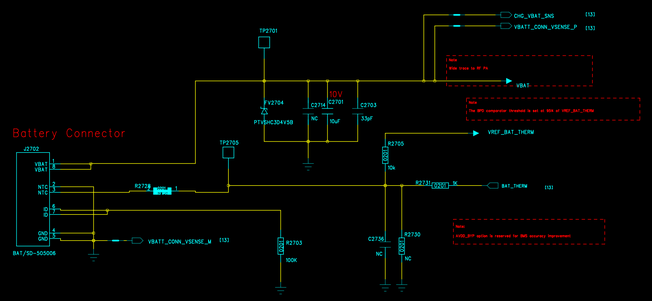


Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 65-1: DO NOT put pull-up resistor on PWRKEY

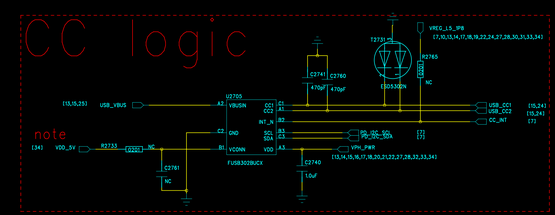
Note 65-2: Volume Up : HOME Key / GND
Volume Down : (KPROW0/KPCOL0) or KPCOL0 / GND

BAT



Note:
Battery ID resistor value require 20K~150K,
Add 100K to ground if battery package ID not meet requirement

CC logic



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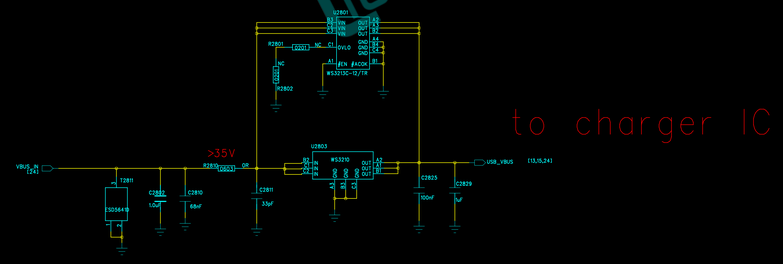

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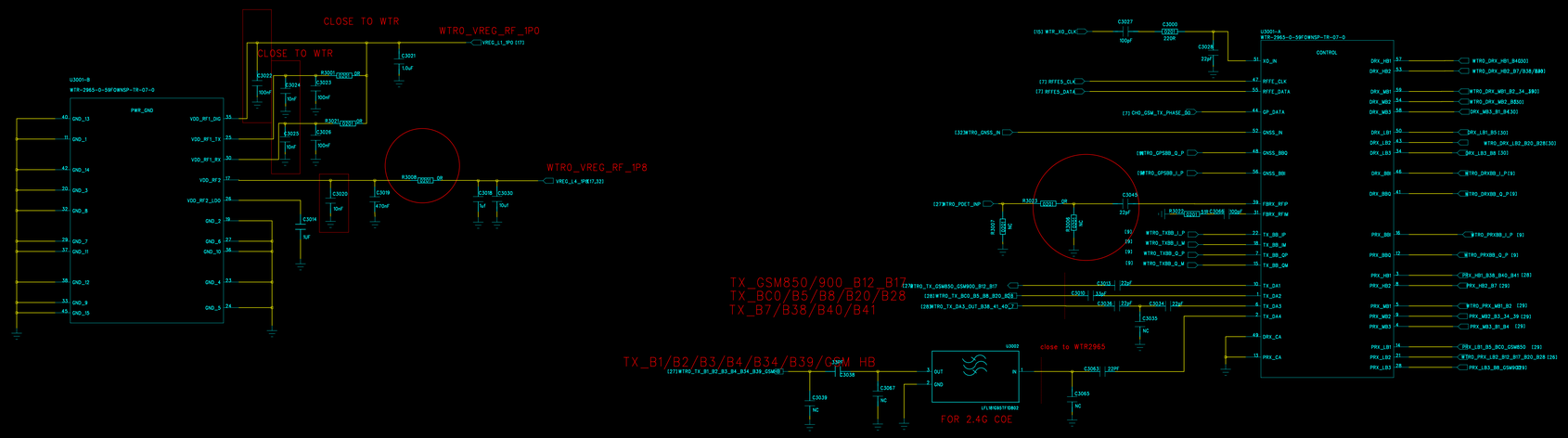

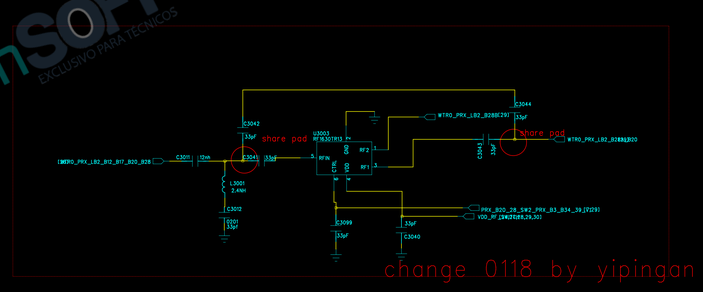

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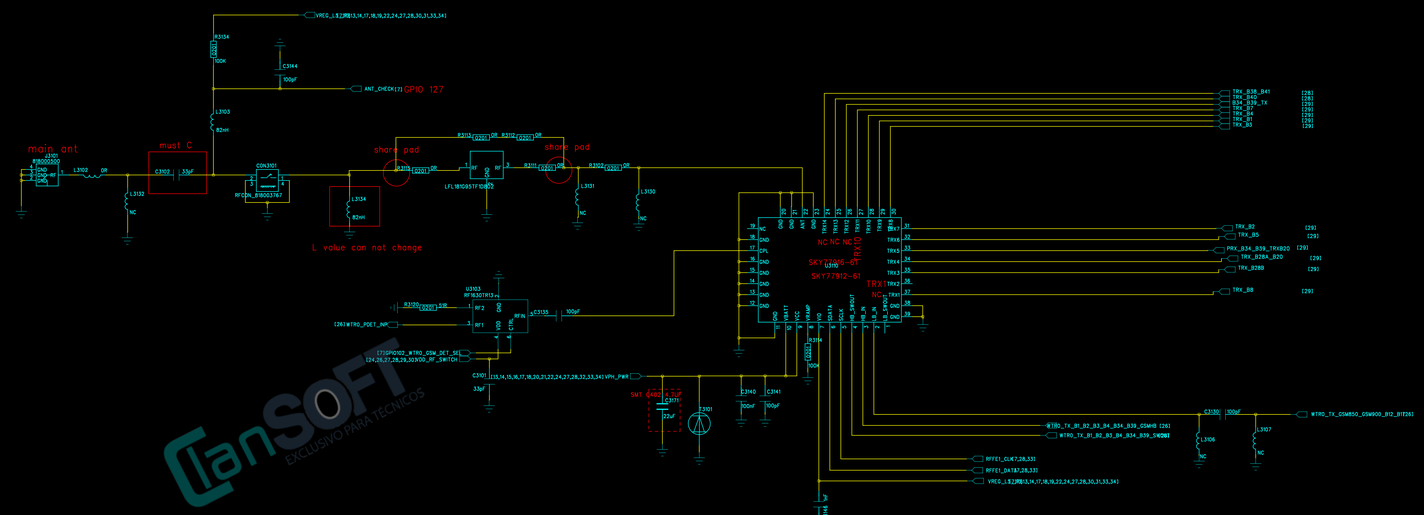

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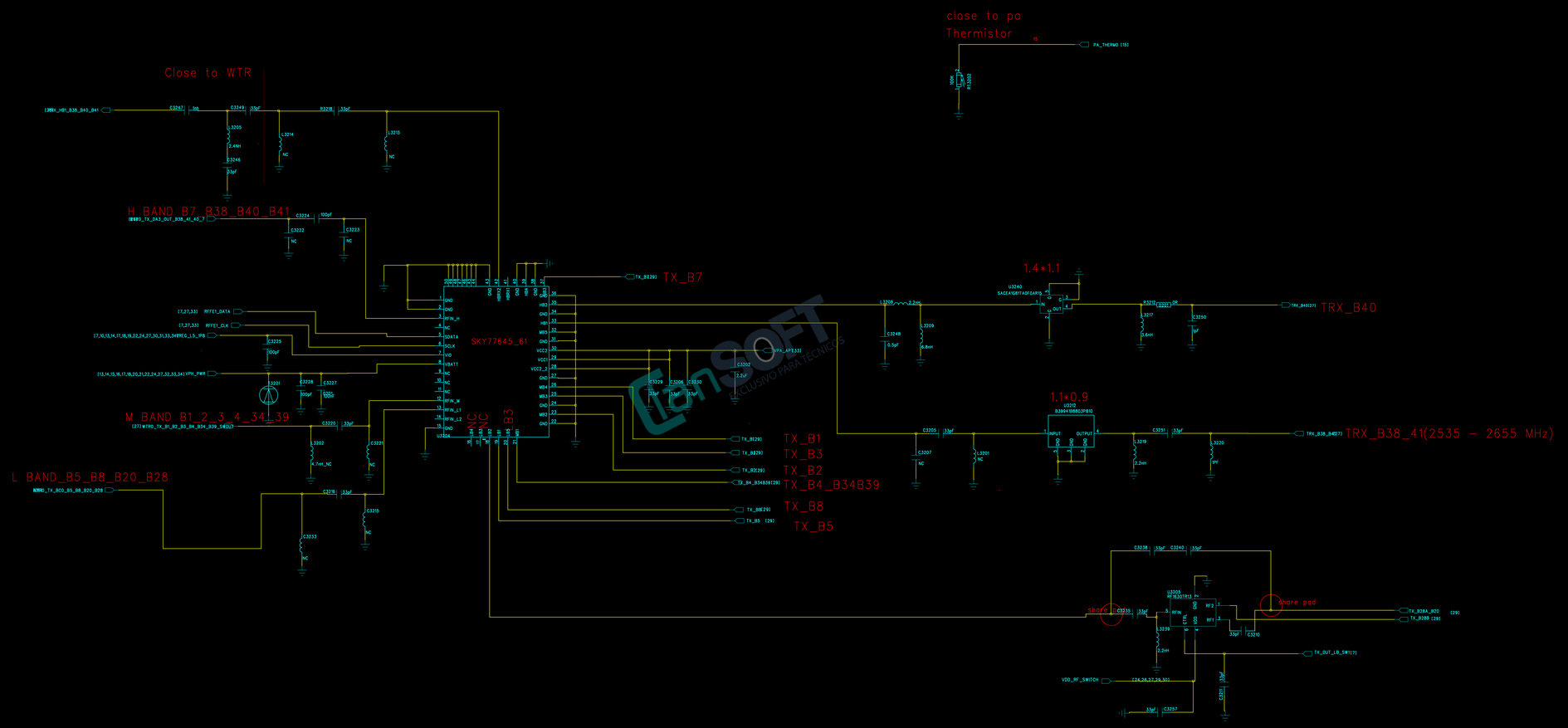

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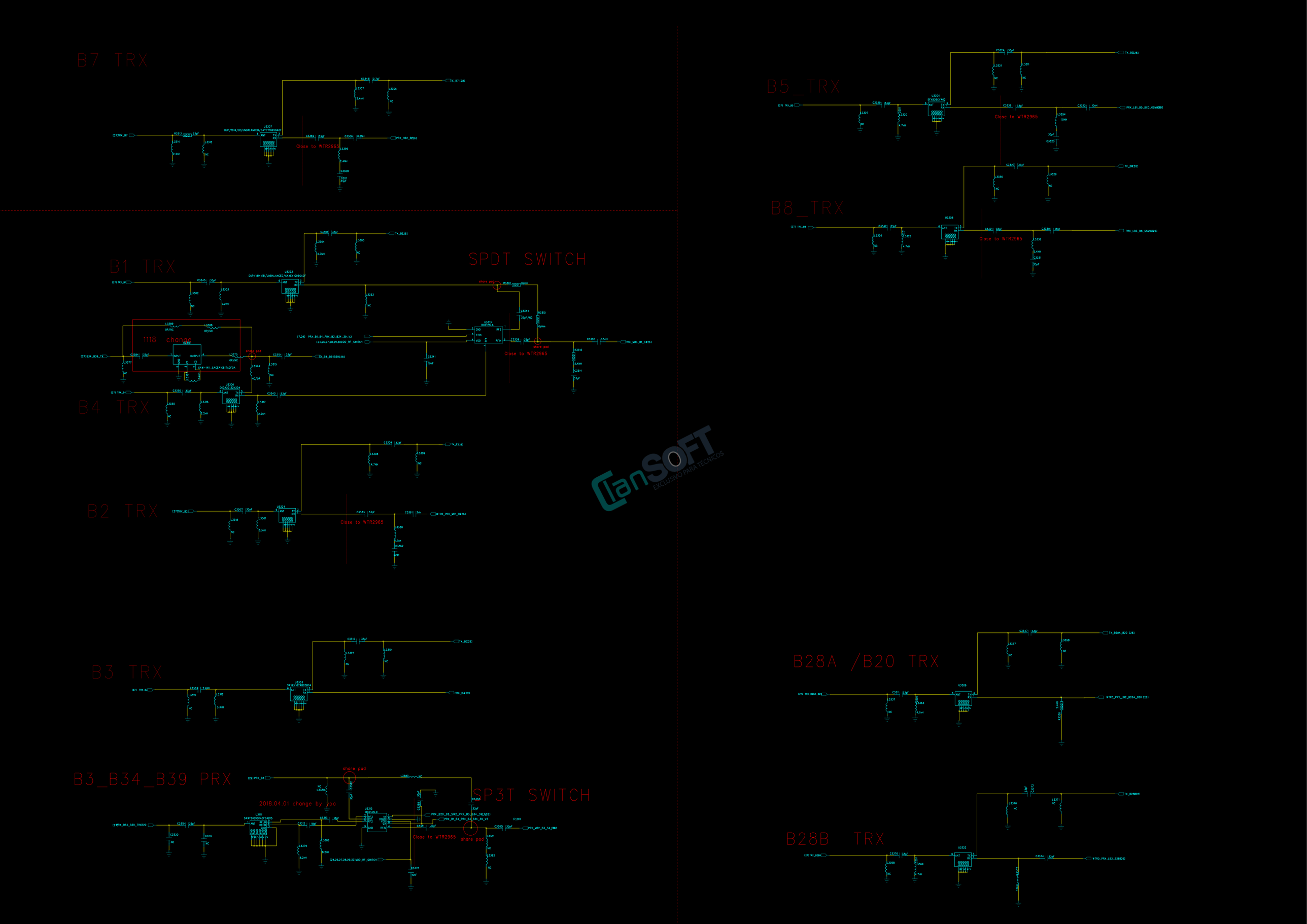
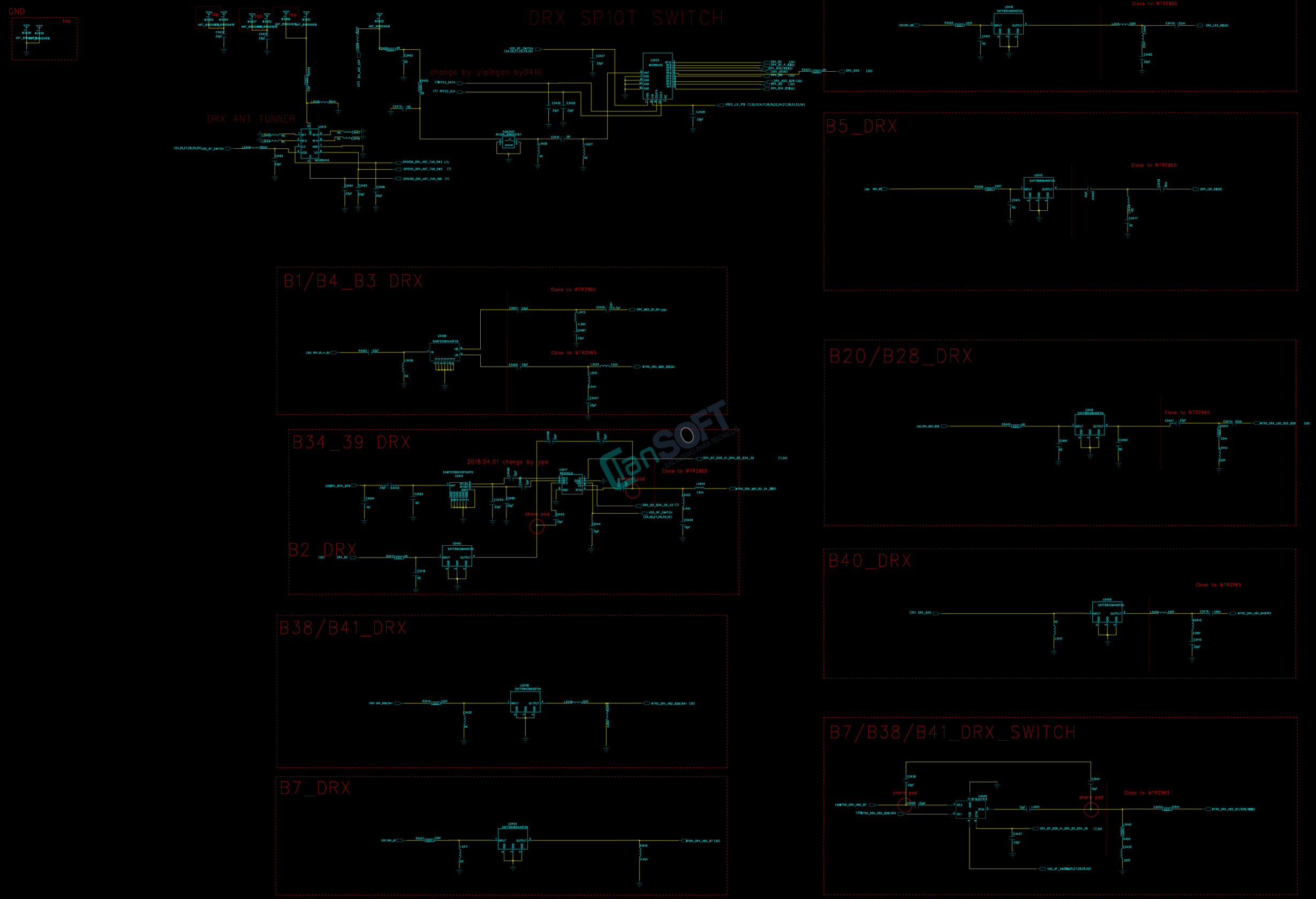
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 28 OF 34


B7 TRX
B5_TRX
B8_TRX
B1 TRX
SPDT SWITCH
1118 change
B4 TRX
B2 TRX
B3 TRX
B3_B34_B39 PRX
SP3T SWITCH
2018.04.01 change by jpa
B28A /B20 TRX
B28B TRX
Close to WTR2965
share pad



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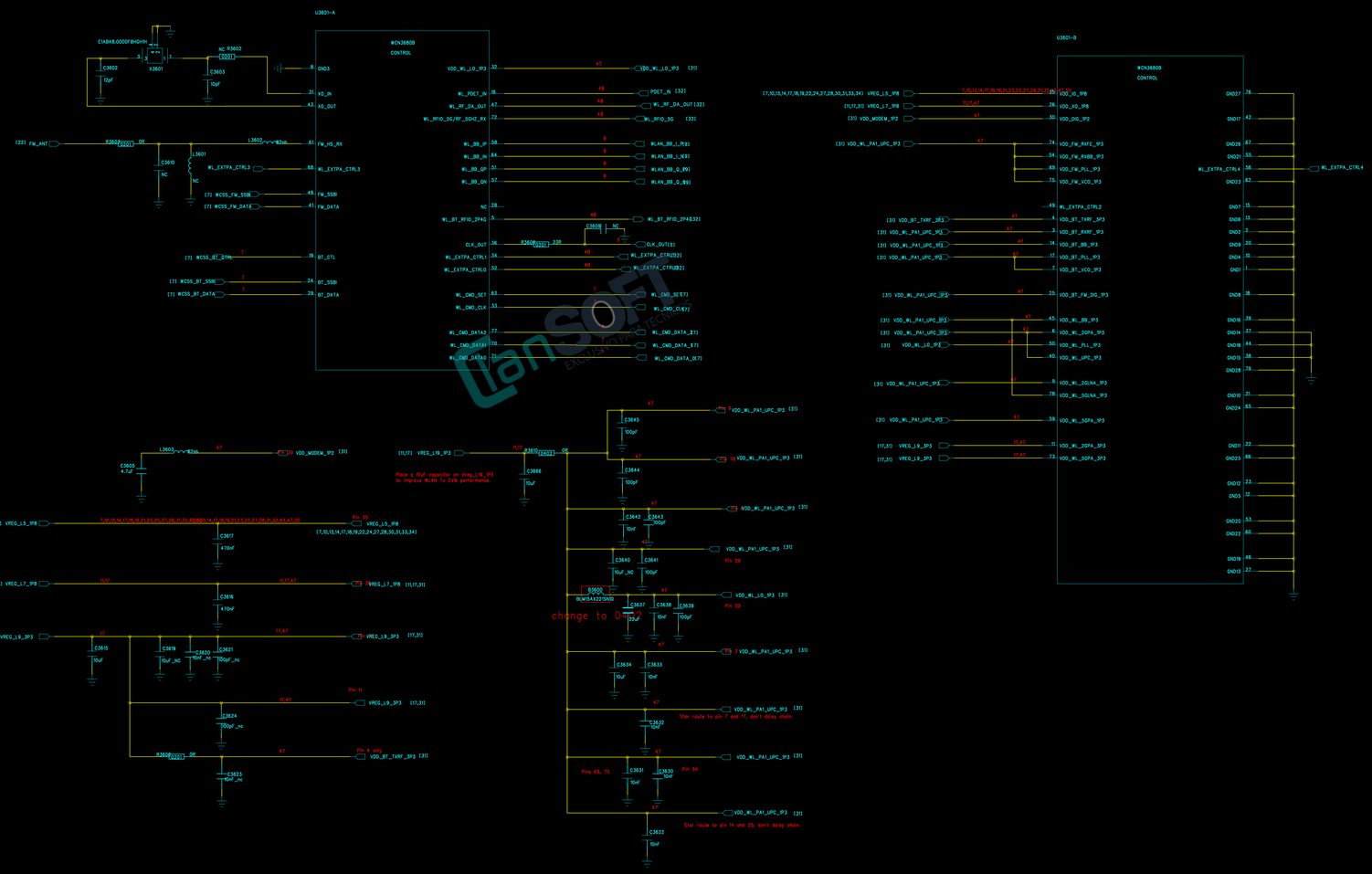
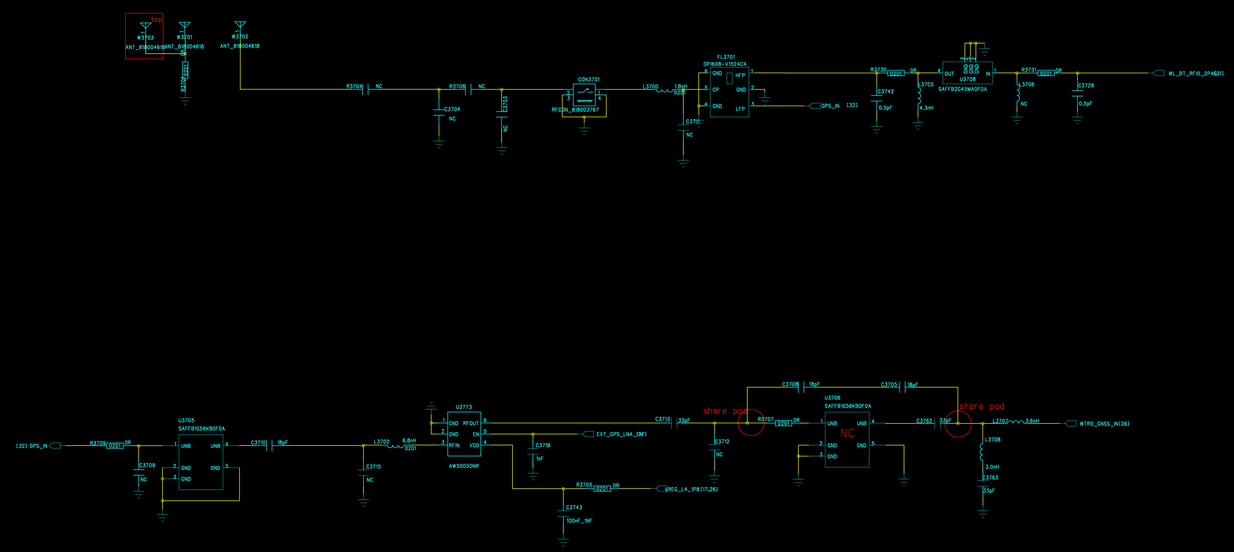
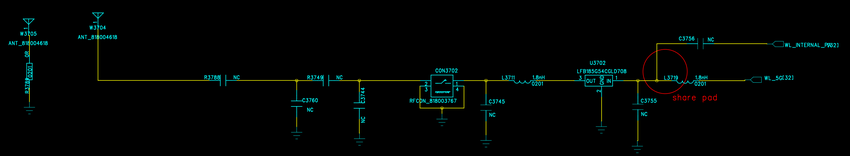
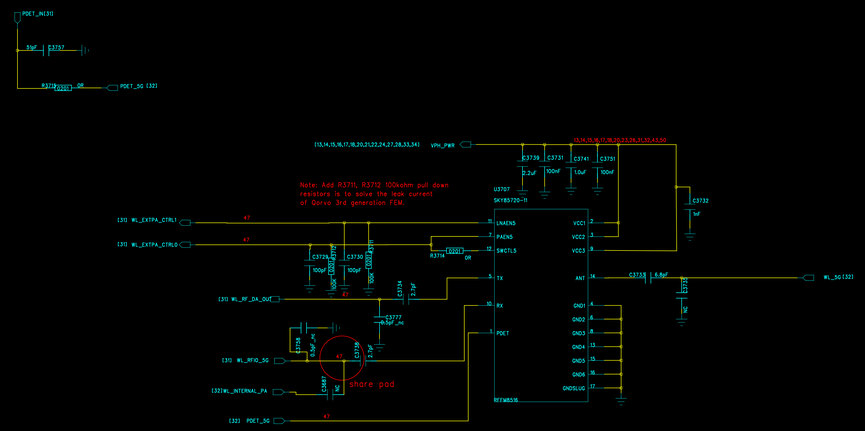

U3601-A
WCN3680B
CONTROL
E1A848.0000F8H0YW
X3601
C3602
12pF
C3603
10pF
NC R3602
0201
GND3
XO_IN
XO_OUT
[22] FW_ANT
R3601 0201 0R
L3601
C3610
NC
L3603 62nm
FM_HS_RX
WL_EXTPA_CTRL3
FM_SSBB
FM_DATA
[7] WCSS_FM_SSBB
[7] WCSS_FM_DATA
[7] WCSS_BT_DTA
BT_CTL
[7] WCSS_BT_SSBB
BT_SSBB
[7] WCSS_BT_DATA
BT_DATA
VDD_WL_LO_1P3
WL_PDET_IN
WL_RF_DA_OUT
WL_RFIO_5G/RF_5GHZ_RX
WL_BB_IP
WL_BB_IN
WL_BB_QP
WL_BB_QN
NC
WL_BT_RFIO_2P4G
CLK_OUT
WL_EXTPA_CTRL1
WL_EXTPA_CTRL0
WL_CMD_SET
WL_CMD_CLK
WL_CMD_DATA2
WL_CMD_DATA1
WL_CMD_DATA0
VDD_WL_LO_1P3 [3]
PDET_IN [32]
WL_RF_DA_OUT [32]
WL_RFIO_5G [32]
WLAN_BB_I_P[9]
WLAN_BB_I_N[9]
WLAN_BB_Q_P[9]
WLAN_BB_Q_N[9]
WL_BT_RFIO_2P4G[32]
C3608 NC
R3604 0201 33R
CLK_OUT[5]
WL_EXTPA_CTRL[32]
WL_CMD_SET[7]
WL_CMD_CLK[7]
WL_CMD_DATA_E7]
WL_CMD_DATA_E7]
WL_CMD_DATA_E7]
U3601-B
WCN3680B
CONTROL
[7,10,13,14,17,18,19,22,24,27,28,30,31,33,34] VREG_L5_1P8
[11,17,31] VREG_L7_1P8
[3] VDD_MODEM_1P2
[3] VDD_WL_PA1_UPC_1P3
VDD_XO_1P8
VDD_XO_1P8
VDD_DIG_1P2
VDD_FW_RXFE_1P3
VDD_FW_RXBB_1P3
VDD_FW_PLL_1P3
VDD_FW_VCO_1P3
WL_EXTPA_CTRL2
VDD_BT_TXRF_1P3
VDD_BT_RXRF_1P3
VDD_BT_BB_1P3
VDD_BT_PLL_1P3
VDD_BT_VCO_1P3
VDD_BT_FW_DIG_1P3
VDD_WL_BB_1P3
VDD_WL_2GPA_1P3
VDD_WL_PLL_1P3
VDD_WL_LPC_1P3
VDD_WL_2GLNA_1P3
VDD_WL_5GLNA_1P3
VDD_WL_5GPA_1P3
VDD_WL_2GPA_1P3
VDD_WL_5GPA_1P3
[3] VDD_BT_TXRF_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_PA1_UPC_1P3
[3] VDD_WL_LO_1P3
[17,31] VREG_L9_1P3
[17,31] VREG_L9_1P3
GND27
GND17
GND26
GND21
WL_EXTPA_CTRL4
GND23
GND7
GND6
GND2
GND9
GND4
GND1
GND8
GND16
GND14
GND18
GND15
GND28
GND10
GND24
GND11
GND25
GND12
GND5
GND20
GND22
GND19
GND13
WL_EXTPA_CTRL4
C3605 4.7uF
L3605 62nm
VDD_MODEM_1P2 [3]
[7,10,13,14,17,18,19,22,24,27,28,30,31,33,34] VREG_L5_1P8
Pin 35
VREG_L5_1P8
[7,10,13,14,17,18,19,22,24,27,28,30,31,33,34]
C3617 470nF
[11,17,31] VREG_L7_1P8
VREG_L7_1P8 [11,17,31]
C3618 470nF
[17,31] VREG_L9_1P3
VREG_L9_1P3 [17,31]
C3615 10uF
C3619 10uF_NC
C3620 10uF_NC
C3621 100pF_NC
Pin 11
VREG_L9_1P3 [17,31]
C3624 100pF_NC
R3605 0201 0R
Pin 4 only
VDD_BT_TXRF_1P3 [3]
C3623 10uF_NC
[11,17] VREG_L9_1P3
L3610 0201 0R
C3666 10uF
Place a 10uF capacitor on Vreg_L9_1P3 to improve WLAN 7x EVM performance.
C3645 100pF
C3644 100pF
C3642 10nF
C3643 100pF
C3640 10uF_NC
C3641 100pF
R3601 0201
RC0816A2270ND
C3637 22uF
C3638 10nF
C3639 100pF
change to 0Ω
C3634 10uF
C3633 10nF
C3632 10uF
Star route to pin 7 and 17, don't daisy chain.
Pins 69, 75
C3631 10nF
C3630 10uF
Pin 54
C3622 10uF
Star route to pin 14 and 25, don't daisy chain.

GPS WIFI 2.4G Ant



WIFI 5G Ant





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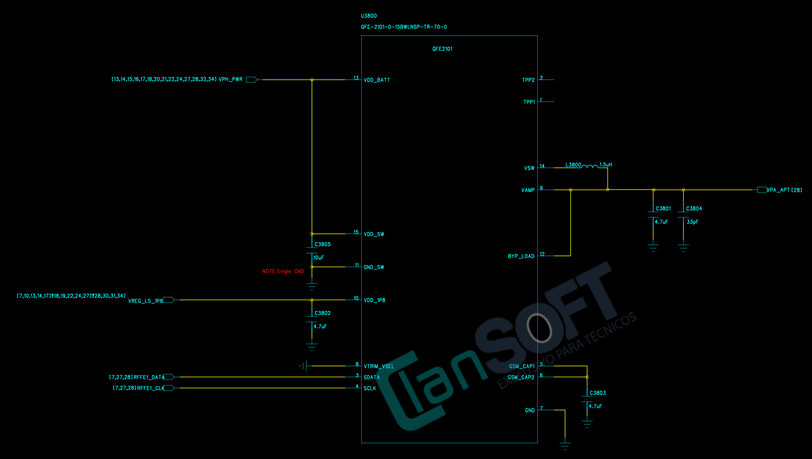
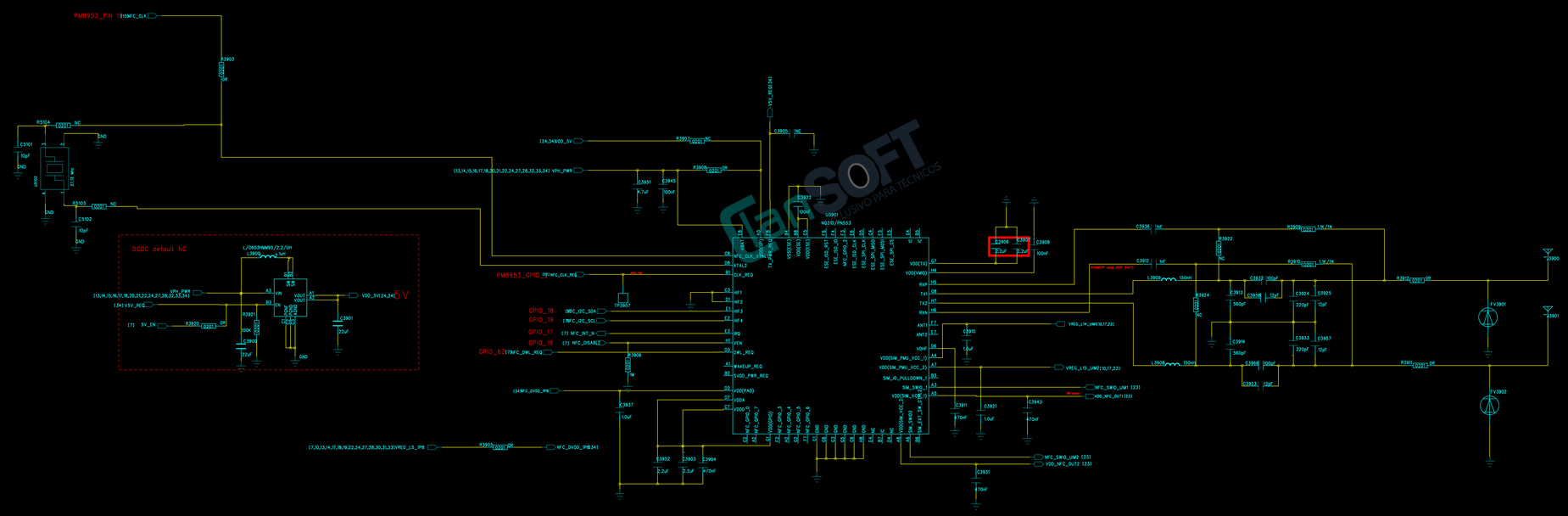
APT


U3800
QFE-2101-0-15DB#LNSP-TR-70-0
QFE2101
[13,14,15,16,17,18,20,21,22,24,27,28,32,34] VPA_PWR
13 VDD_BATT
TPP2 2
TPP1 1
VSW 14
L3800 1.5uH
VAMP 9
VPA_APT [28]
C3801 4.7uF
C3804 33pF
15 VDD_SW
C3805 10uF
BYP_LOAD 12
NOTE:Simple GND
11 GND_SW
[7,10,13,14,17,18,19,22,24,27,28,30,31,34] VREG_L5_1P8
10 VDD_1P8
C3802 4.7uF
8 VTRM_VSEL
[7,27,28] RFFE1_DATA
3 SDATA
[7,27,28] RFFE1_CLK
4 SCLK
GSM_CAP1 5
GSM_CAP2 6
C3803 4.7uF
GND 7

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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SOLUCIONES EXCLUSIVO PARA TÉCNICOS

DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A3 / DRAWING NO: <Drawing Number> / REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 34 OF 34