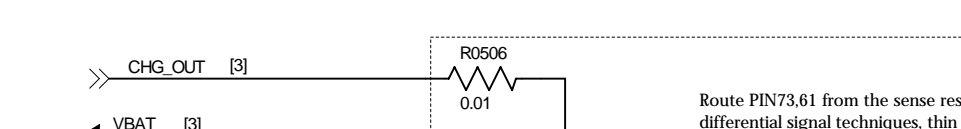


# PMI8940 CHARGER

PMI_FIN	connection on device without Wipower	connection on device with Wipower
CHG_OK	Pull up to VDD_CAP with 51kohm	Stark PRU CHG_OK
DIV2_EN	Pull down to GND with 0ohm	Stark PRU DIV2_EN
GPIO2	No Connect For parallel charging: Connects to SMB EN pin. Do NOT pull up to VDD_CAP	10kohm pull down to gnd For parallel charging: Connects to SMB EN pin. Do NOT pull up to VDD_CAP



Route PIN73.61 from the sense resistor using differential signal techniques, thin traces are sufficient

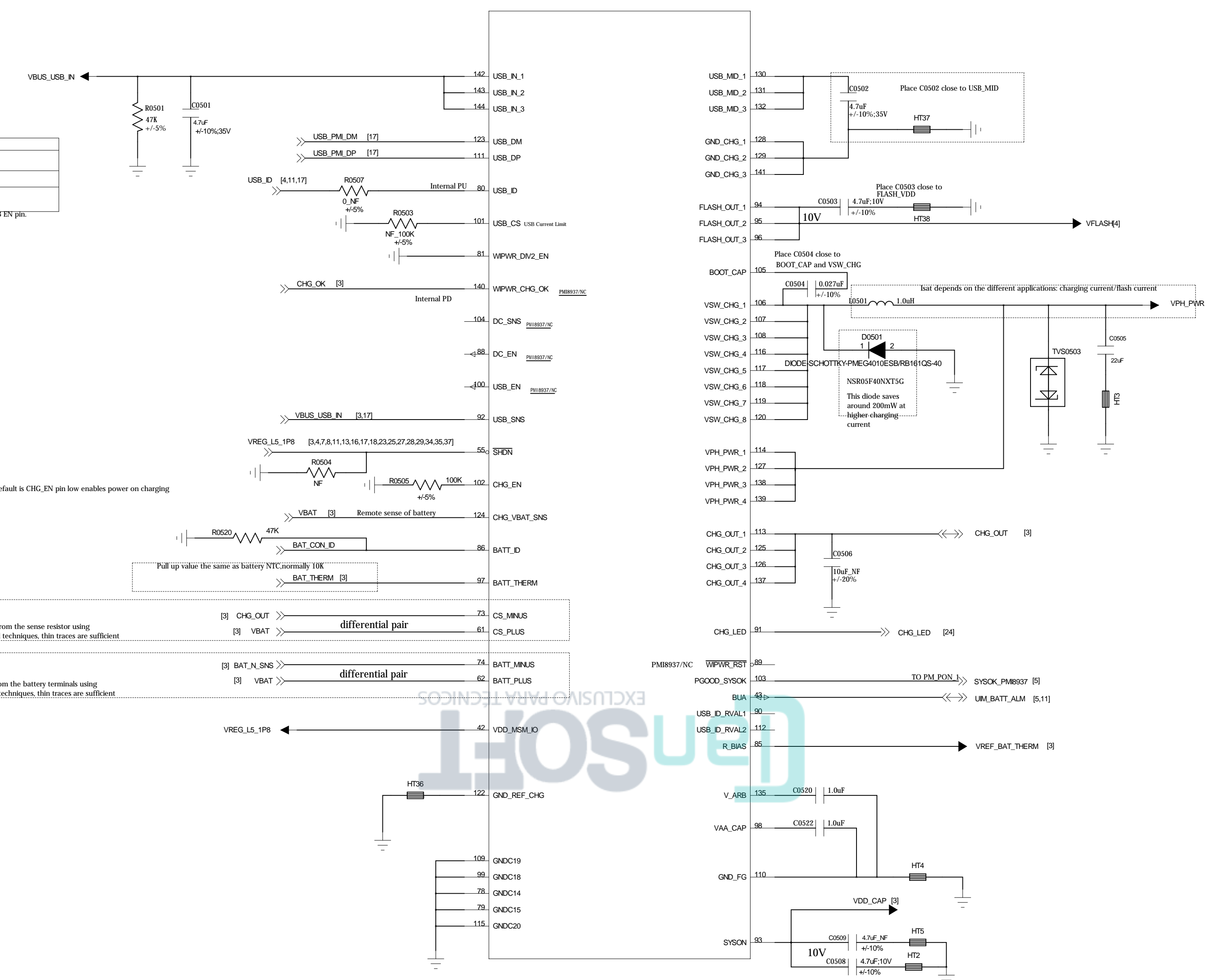
Route PIN74.82 from the battery terminals using differential signal techniques, thin traces are sufficient

Default to CHG\_EN pin low enables power on charging

Pull up value the same as battery NTC, normally 10K

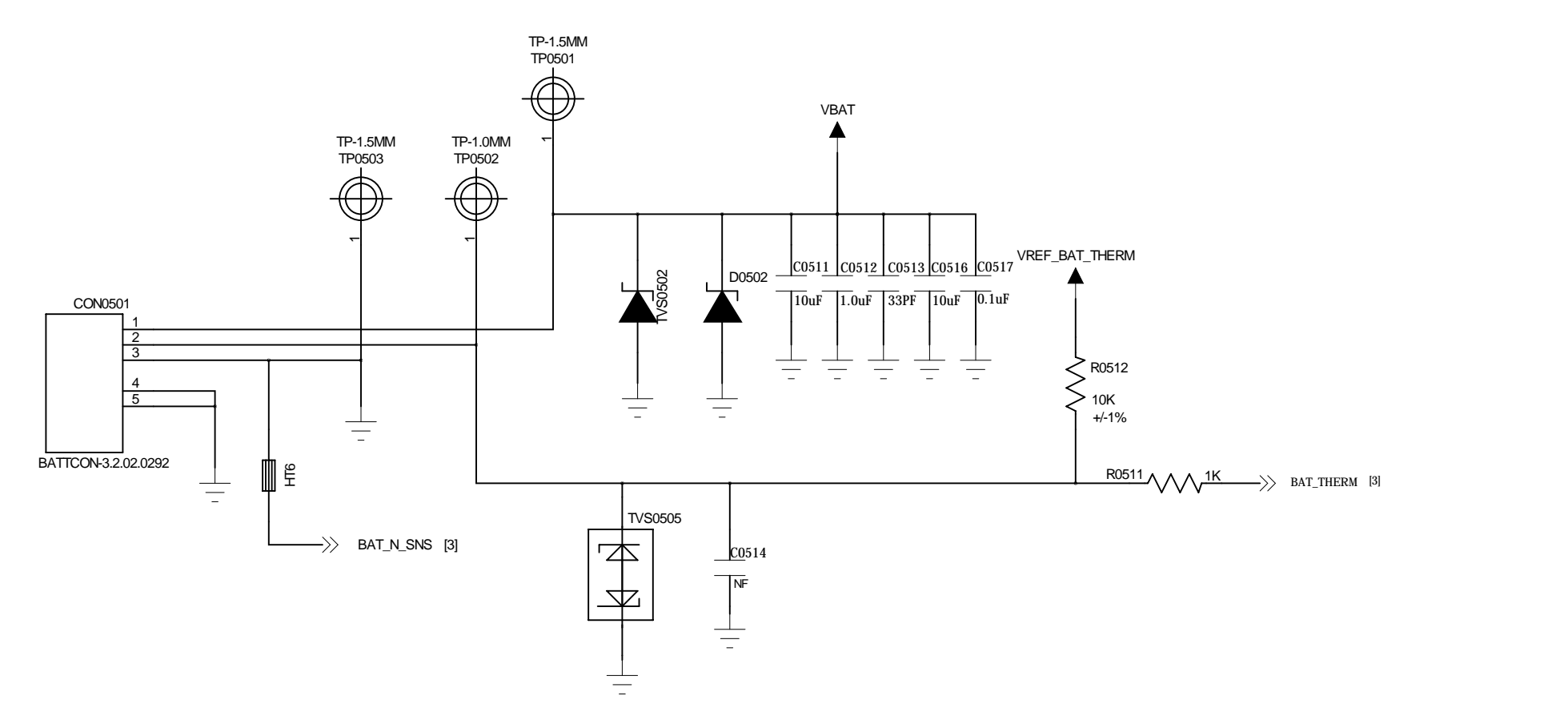
Remote sense of battery

U0901-A

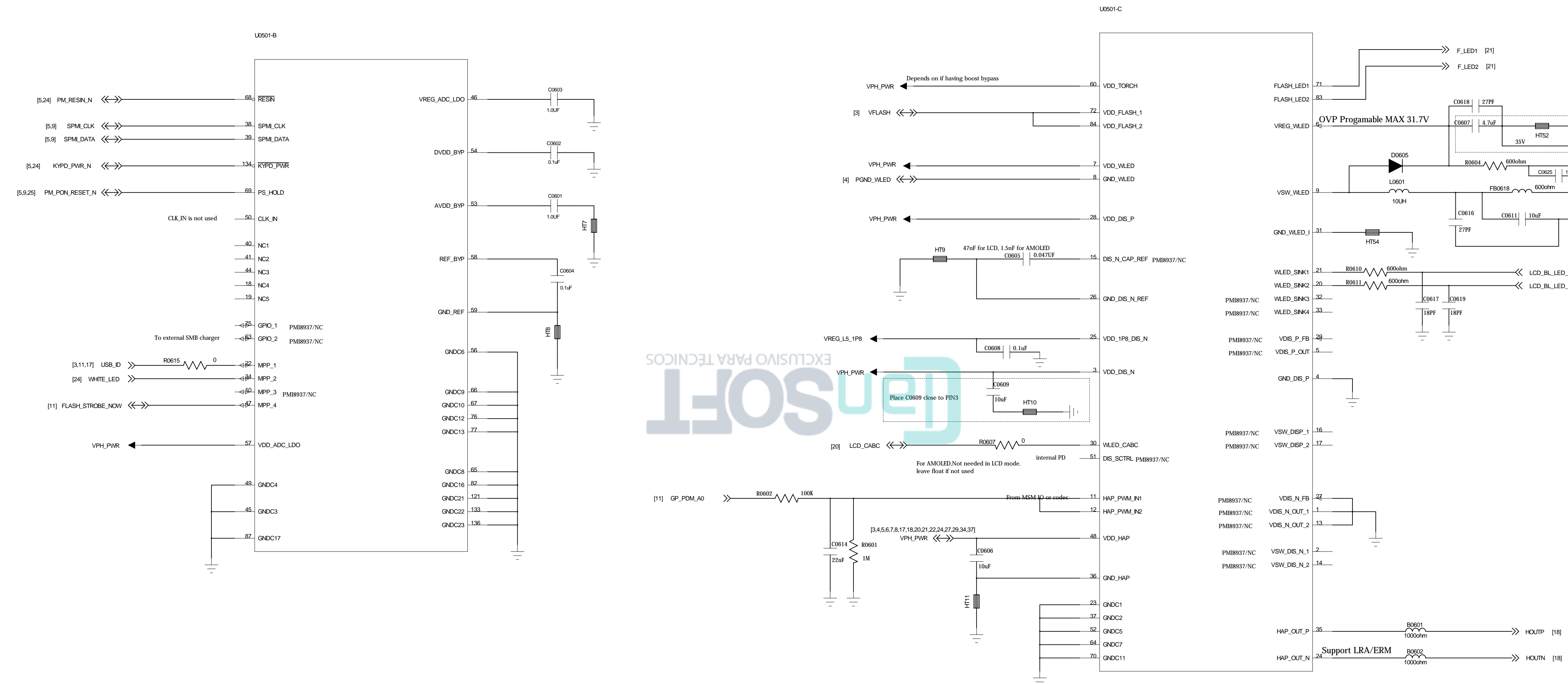


PMI\_VDD\_CAP net is 5VDC, cap is 0603.  
Do not use 0402 as may derate to -80%.

## BATTERY CONNECTOR

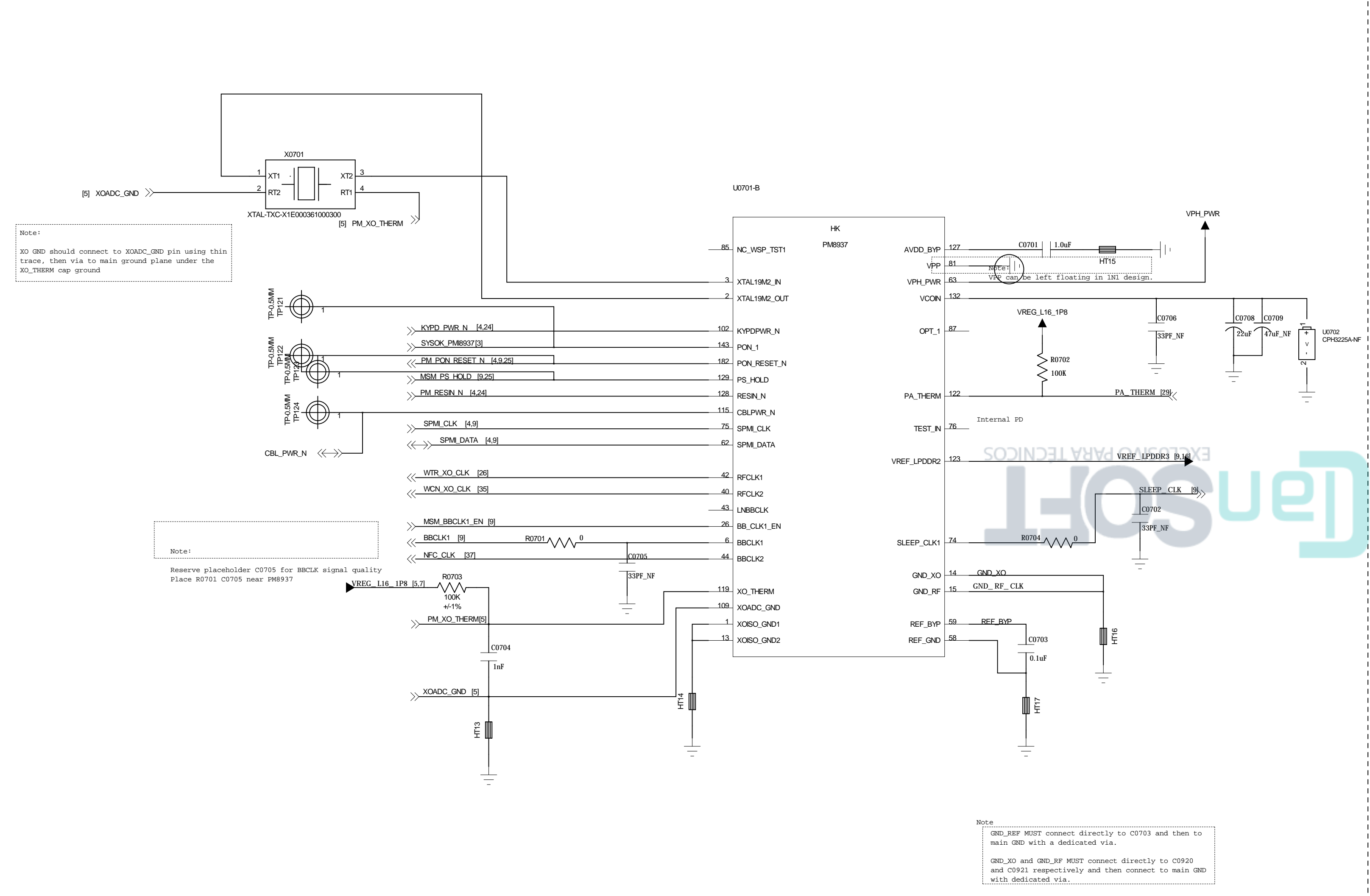


# PMI8940 Control/Interface

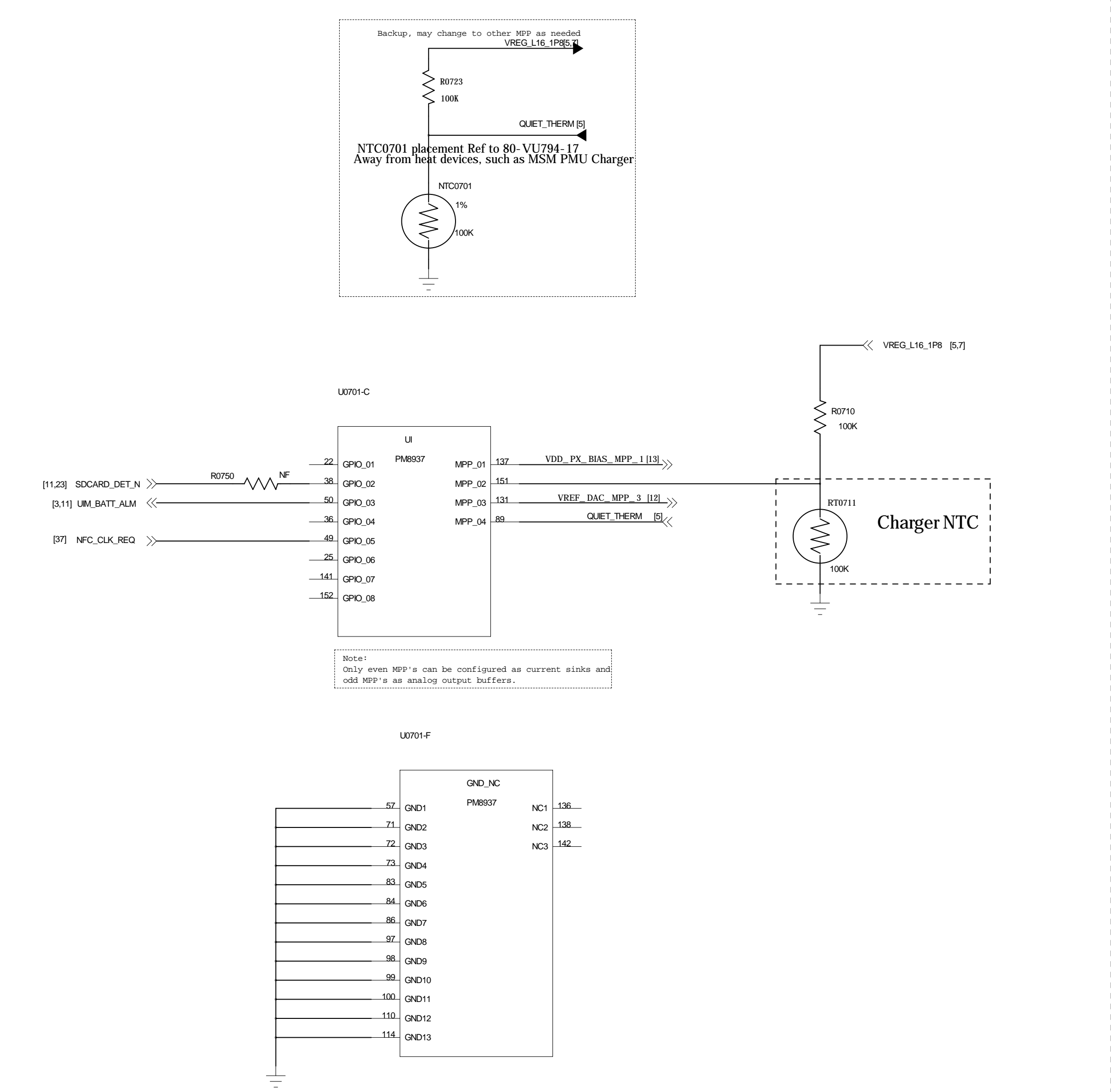


EXCLUSIVO PARA TÉCNICOS

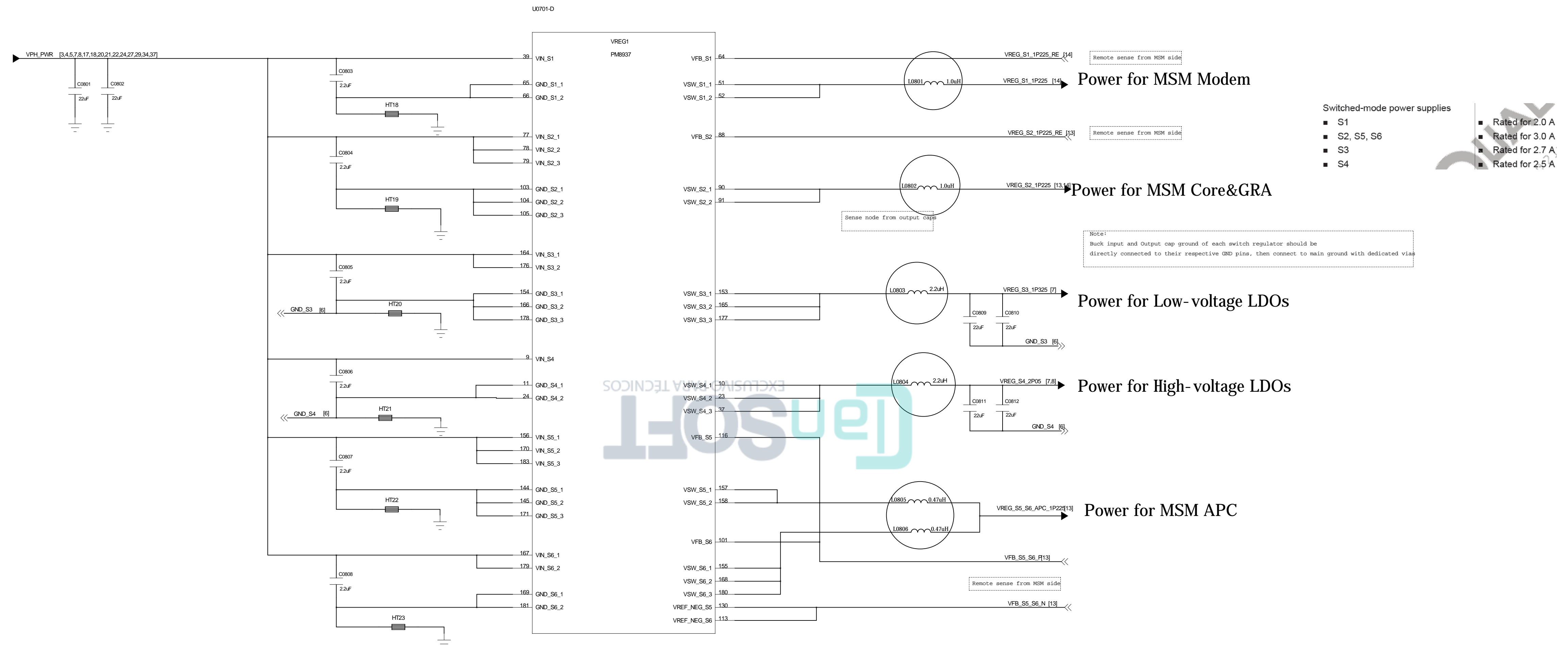
# PM8937 Control



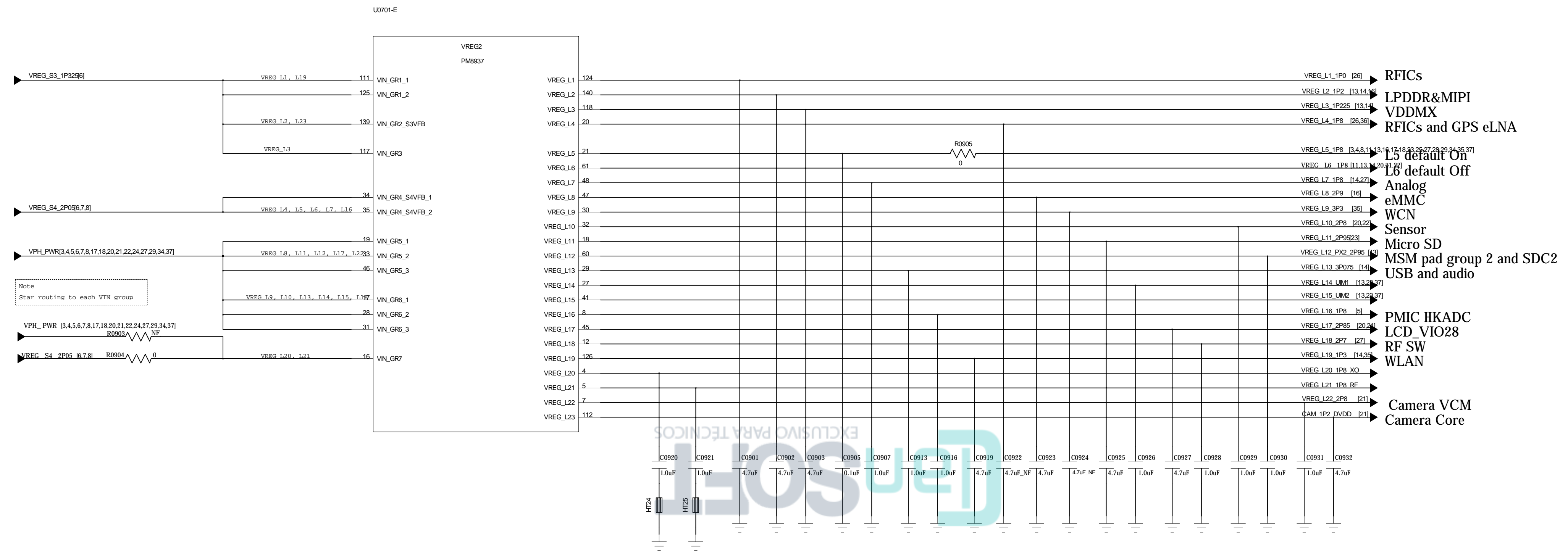
# PM8937 MPPs



# PM8937 BUCK CONVERTER

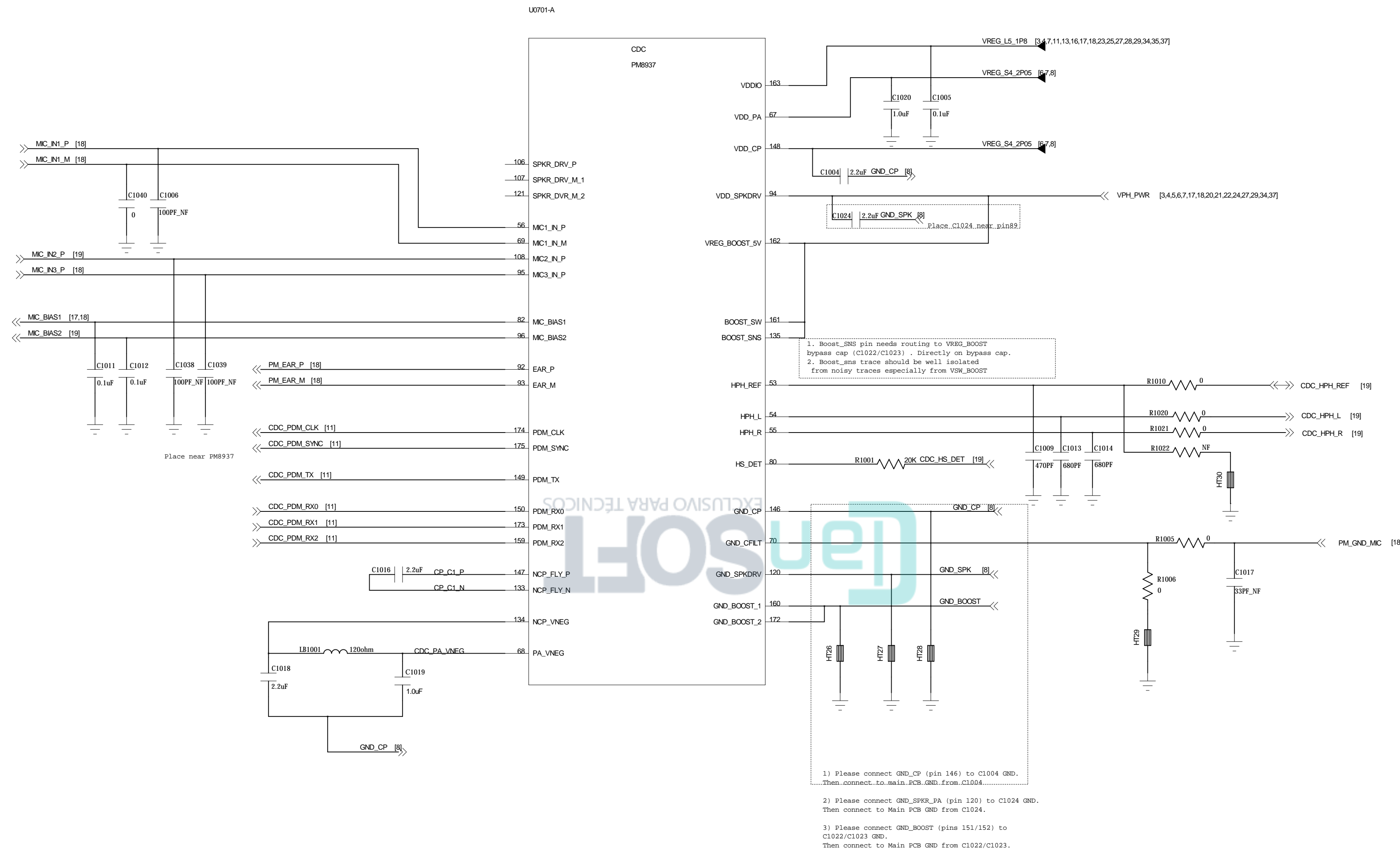


# PM8937 LDO CIRCUITS



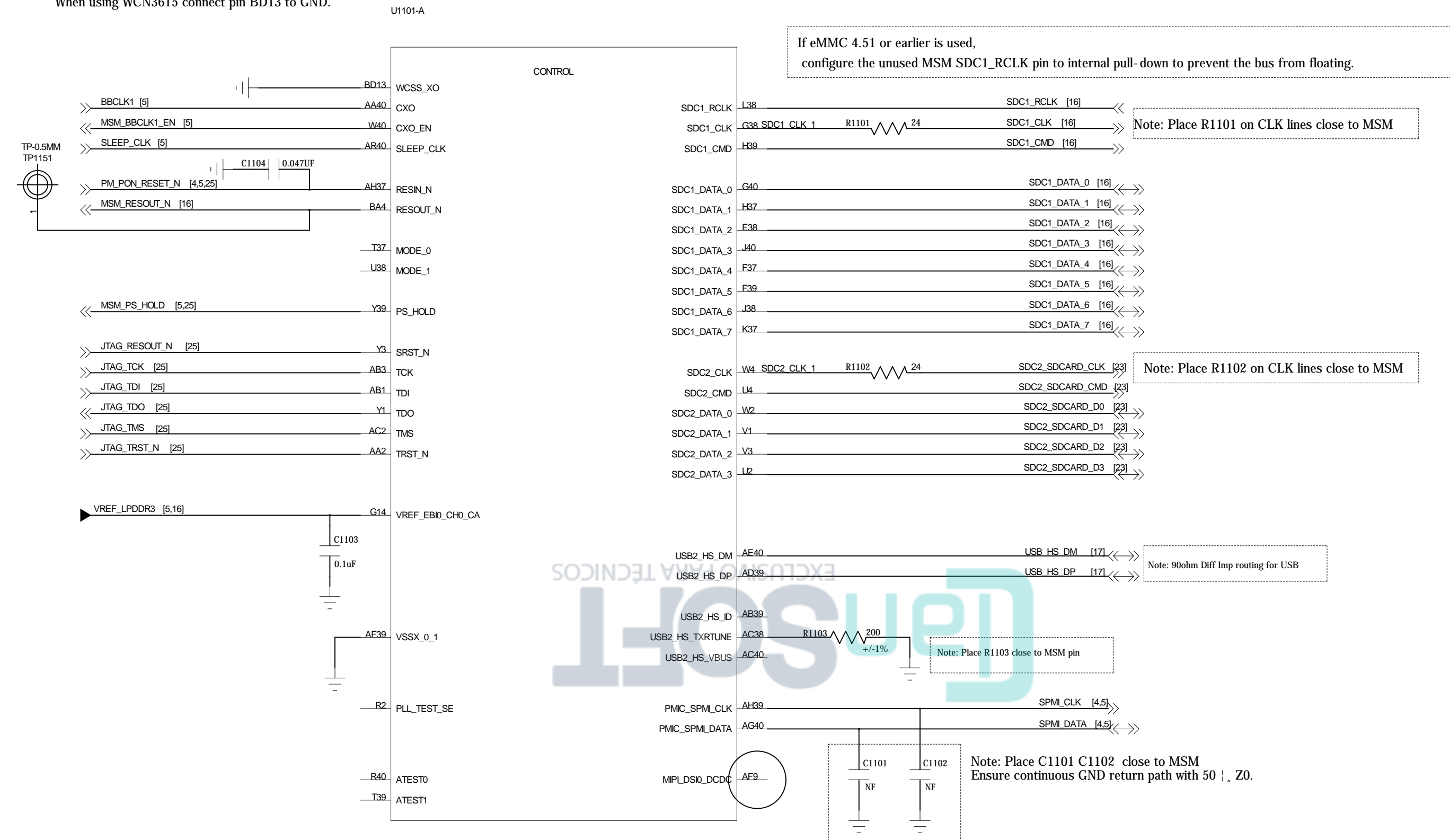
PSEUDO CAPLESS LDOs  
 L4\*, L6, L8\*, L9\*, L10, L11\*, L12, L14, L15, L17\*, L18, L22, L23  
 L4\*, L8\*, L9\*, L11\*, L17\*, still need validation as Pseudo-capless  
 L5, L7, L13, L16 have internal PMIC Loads and require local CAPS.

# PM8937 Codec



# MSM8917 Control

Note: WCSS\_XO signal required only for 5GHZ.  
When using WCN3615 connect pin BD13 to GND.



If eMMC 4.51 or earlier is used, configure the unused MSM SDC1\_RCLK pin to internal pull-down to prevent the bus from floating.

Note: Place R1101 on CLK lines close to MSM

Note: Place R1102 on CLK lines close to MSM

Note: 90ohm Diff Imp routing for USB

Note: Place R1103 close to MSM pin

Note: Place C1101 C1102 close to MSM  
Ensure continuous GND return path with 50 |, Z0.

Note: MIP1\_DSI can be configured as DCDC or LDO mode.  
When configured as LDO mode, pin AF9 should be left floating and L1101 should be DNI.

DC-DC mode "C For better power ~3 mA lower

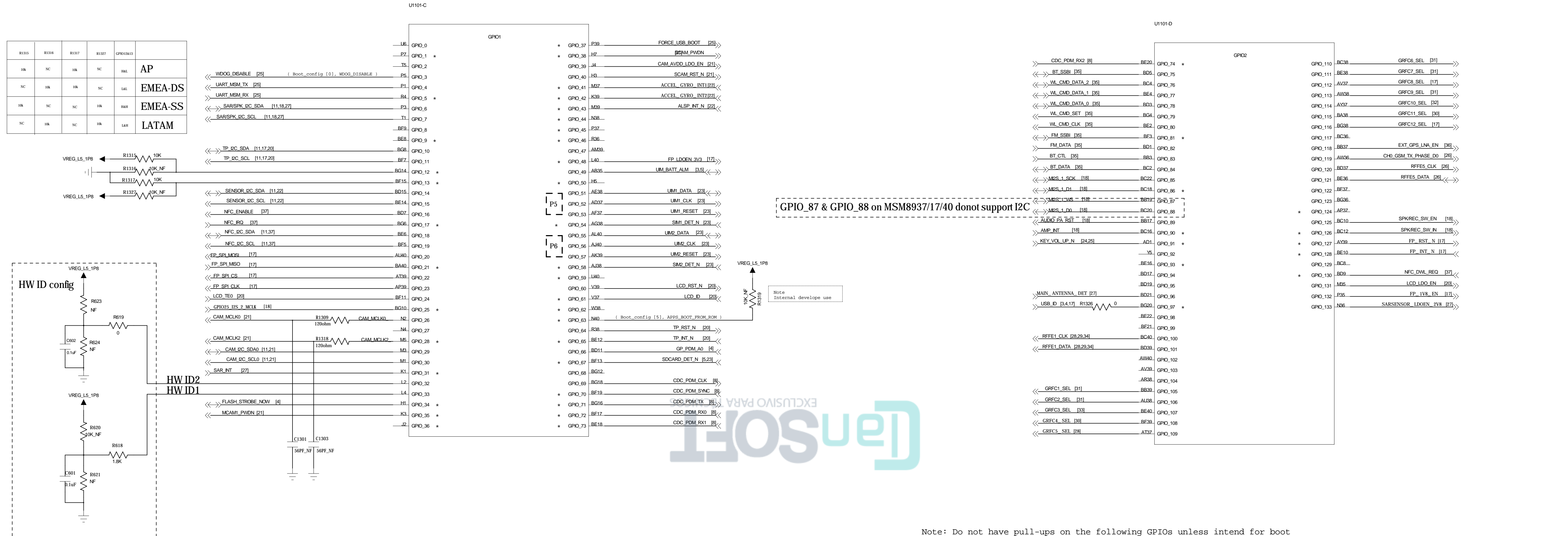
# MSM8917 EBI





# MSM8917 GPIO

Note: Asterisks (\*) indicate modem power management (MPM) wake-up pins

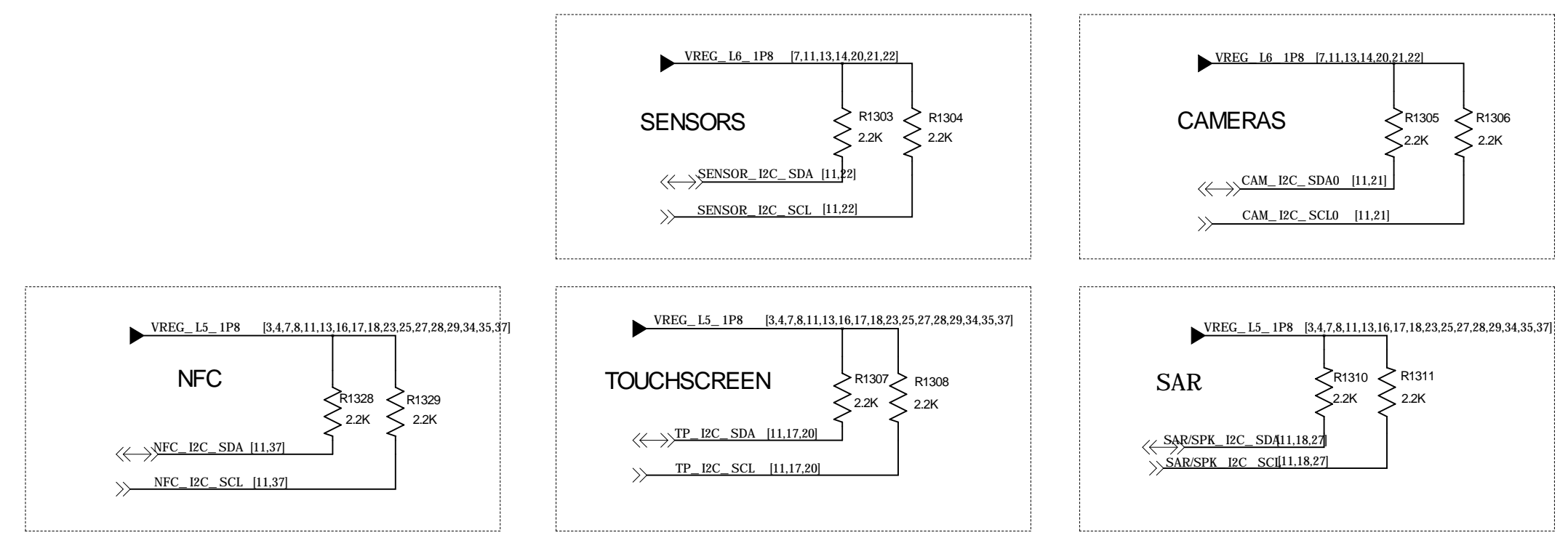


GPIO\_87 & GPIO\_88 on MSM8937/17/40 donot support I2C

Note: Do not have pull-ups on the following GPIOs unless intend for boot or secure- boot related configurations:  
GPIO\_91, 107, 109

## I2C PULL-UP RESISTORS

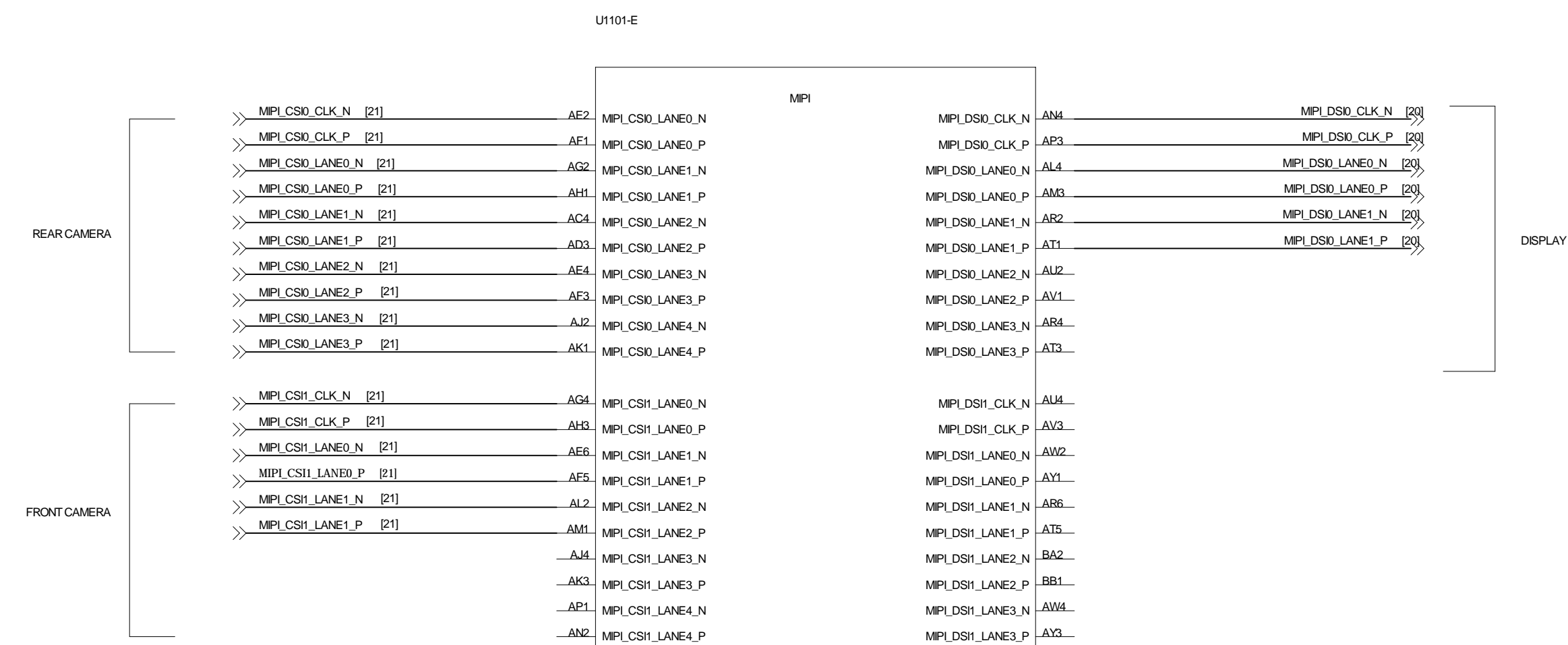
Note: Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.



GPIO	BOOT_CONFIG	BOOT_CONFIG[3:1]	BOOT_CONFIG
GPIO_3	BOOT_CONFIG[0]/WDOG_DISABLE	0b000	SDC1 -> SDC2 -> USB2.0
GPIO_111	BOOT_CONFIG[1]	0b010	SDC1
GPIO_112	BOOT_CONFIG[2]	0b100	SDC2 -> SDC1
GPIO_88	BOOT_CONFIG[3]		

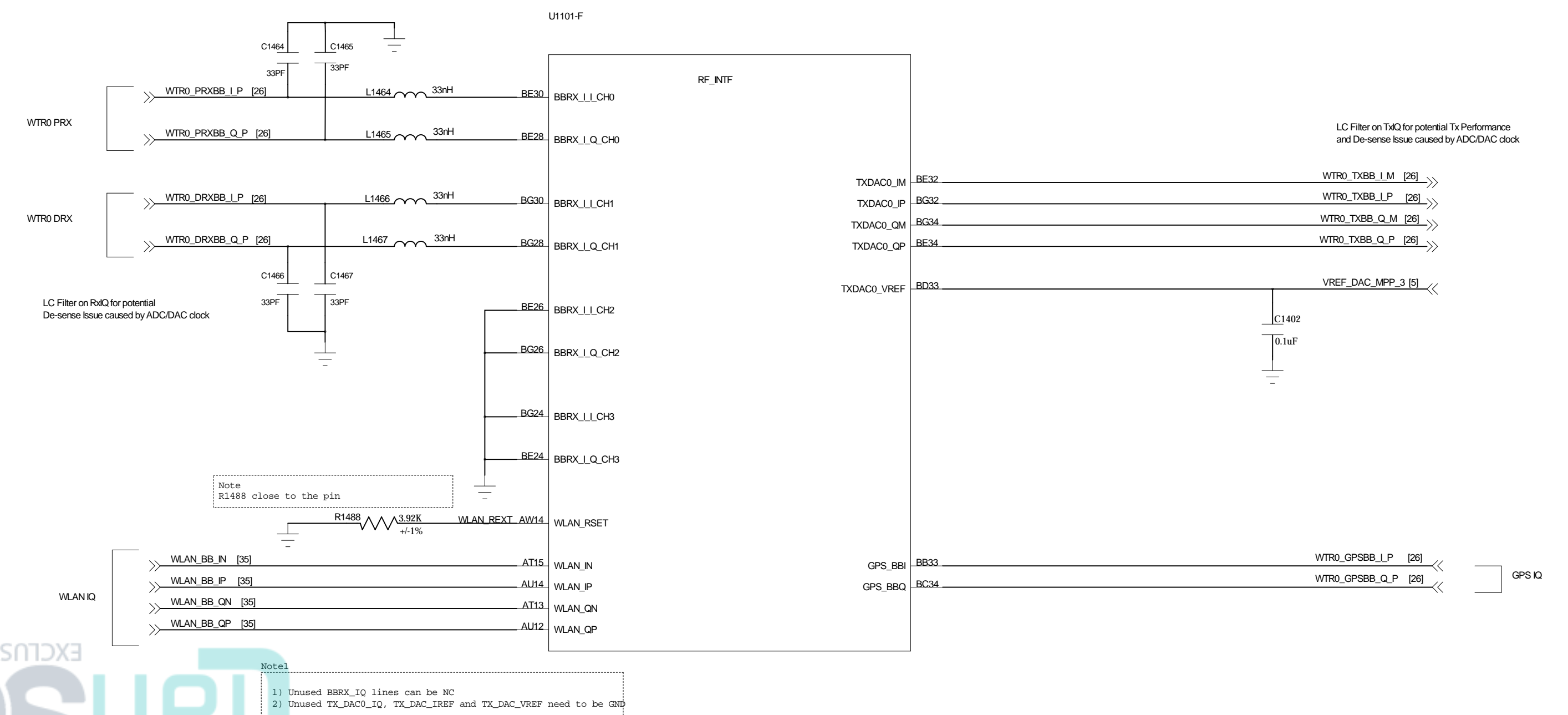
Default Boot Config (0b000) is SDC1@0%

# MSM8917 MIPI

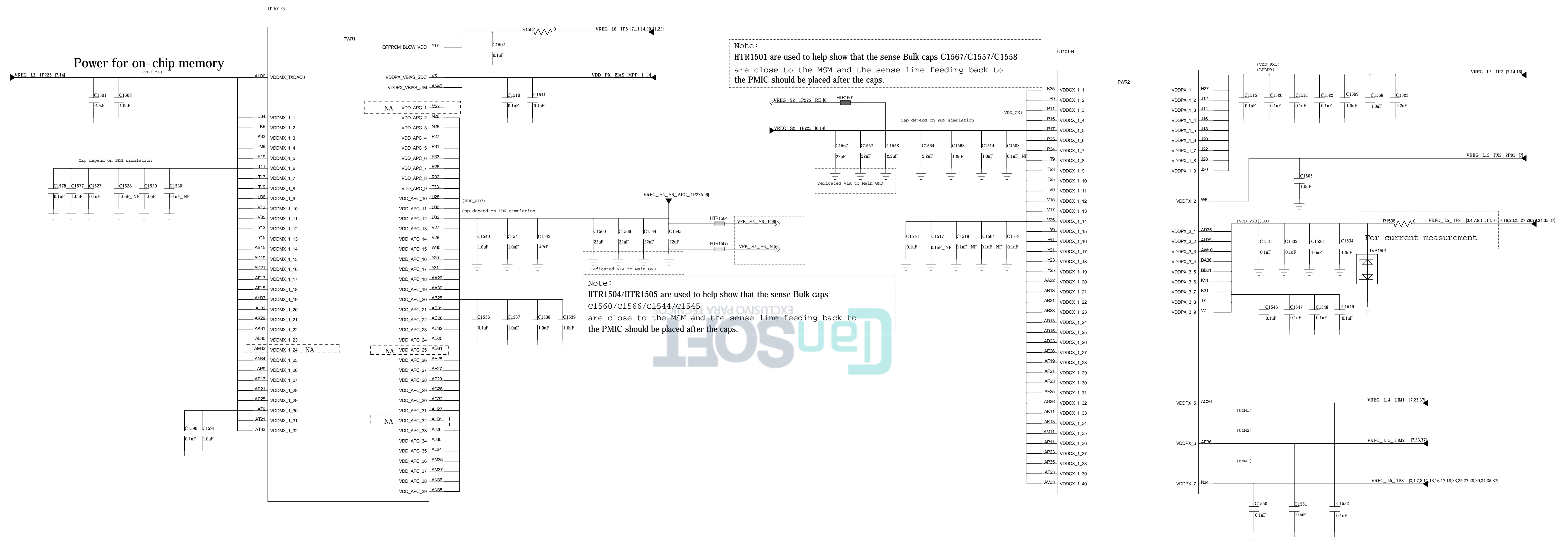


Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

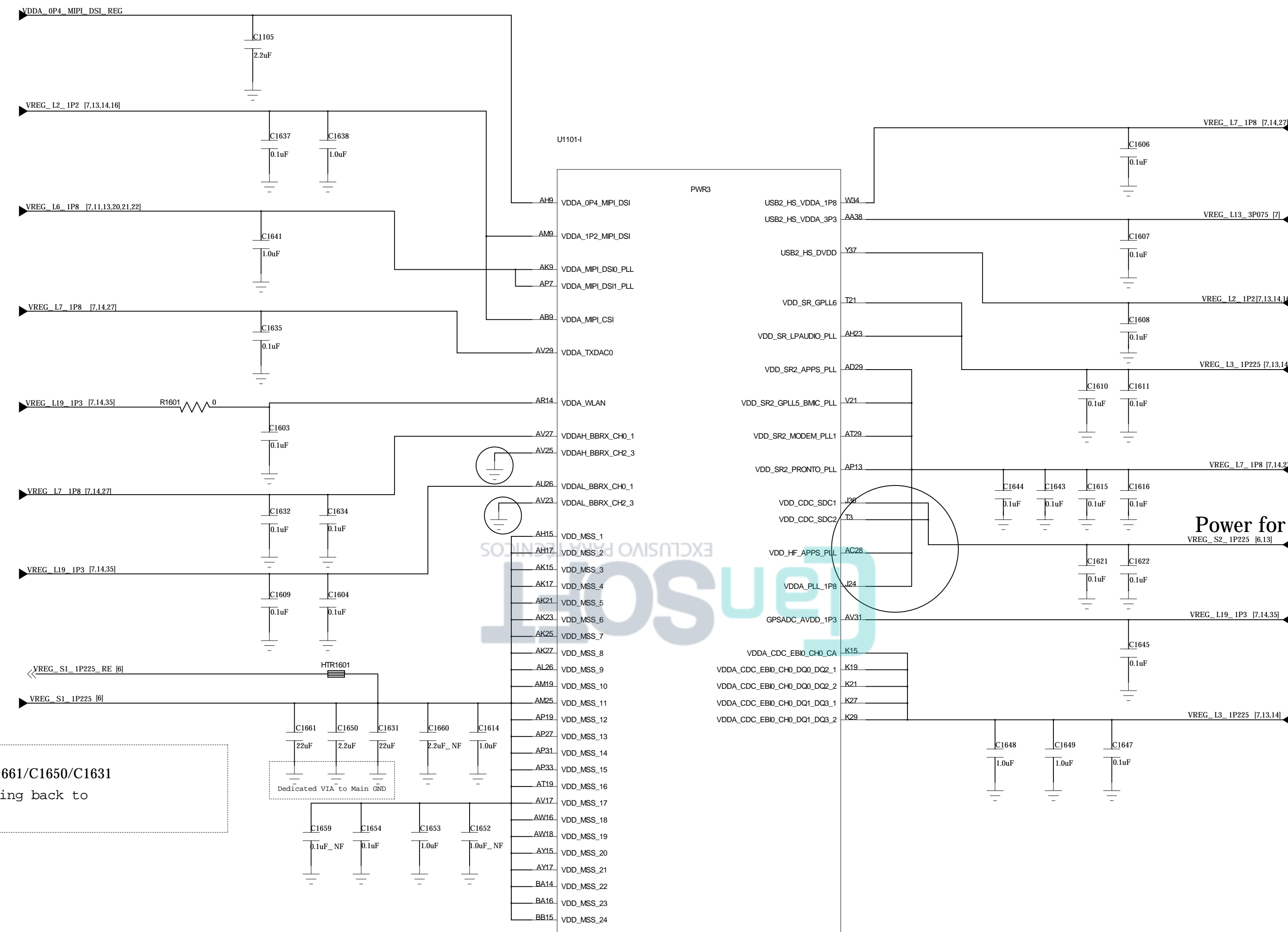
# MSM8917 RF Control



# MSM8917 POWER1



# MSM8917 POWER2



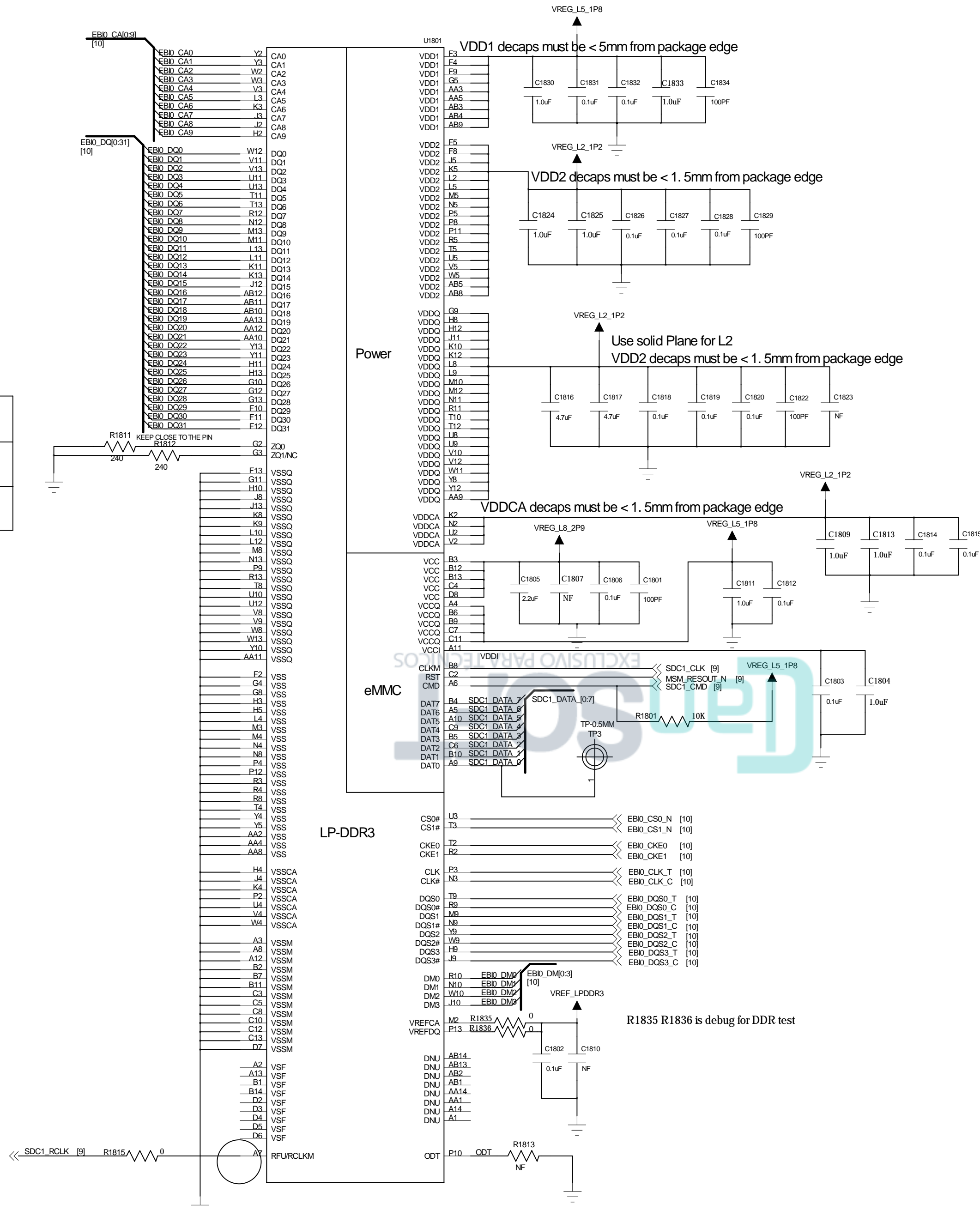
Note:  
HTR1601 are used to help show that the sense Bulk caps C1661/C1650/C1631 are close to the MSM and the sense line feeding back to the PMIC should be placed after the caps.

Power for secure digital calibration delay circuits

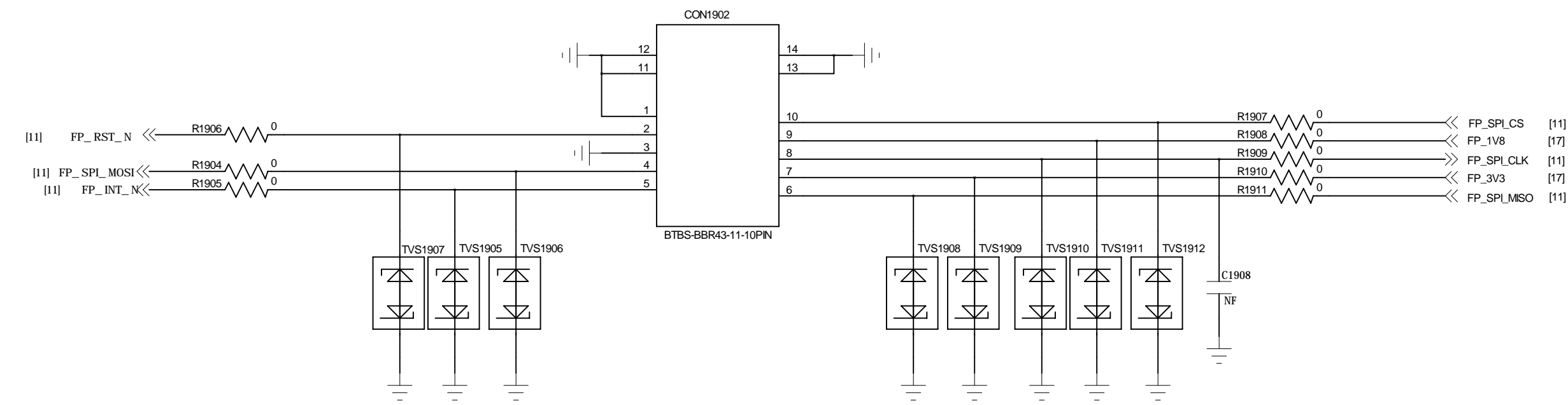


# MEMORY:LPDDR3+EMMC

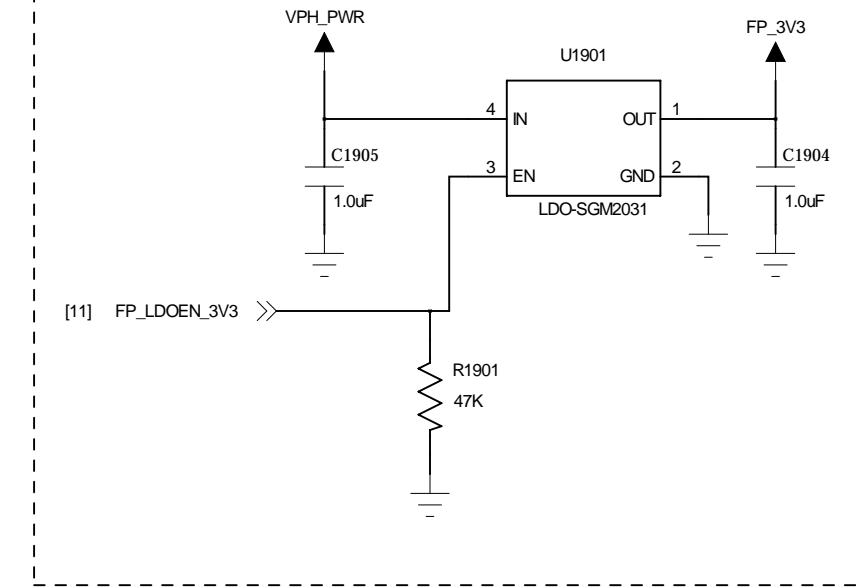
	MICRO/HYNIX	SAMSUNG
U1501.G3	ZQ1	NC
U1501.A7	RFU	RCLK



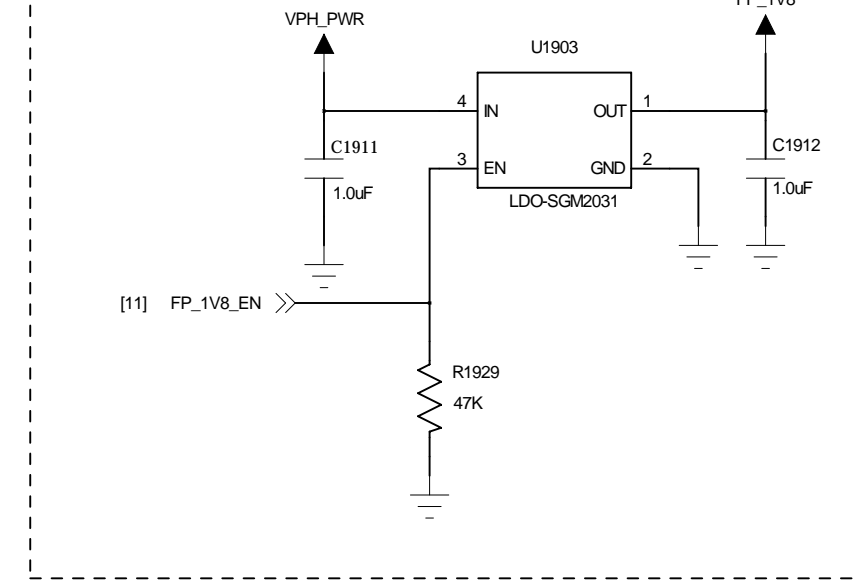
# FingerPrint



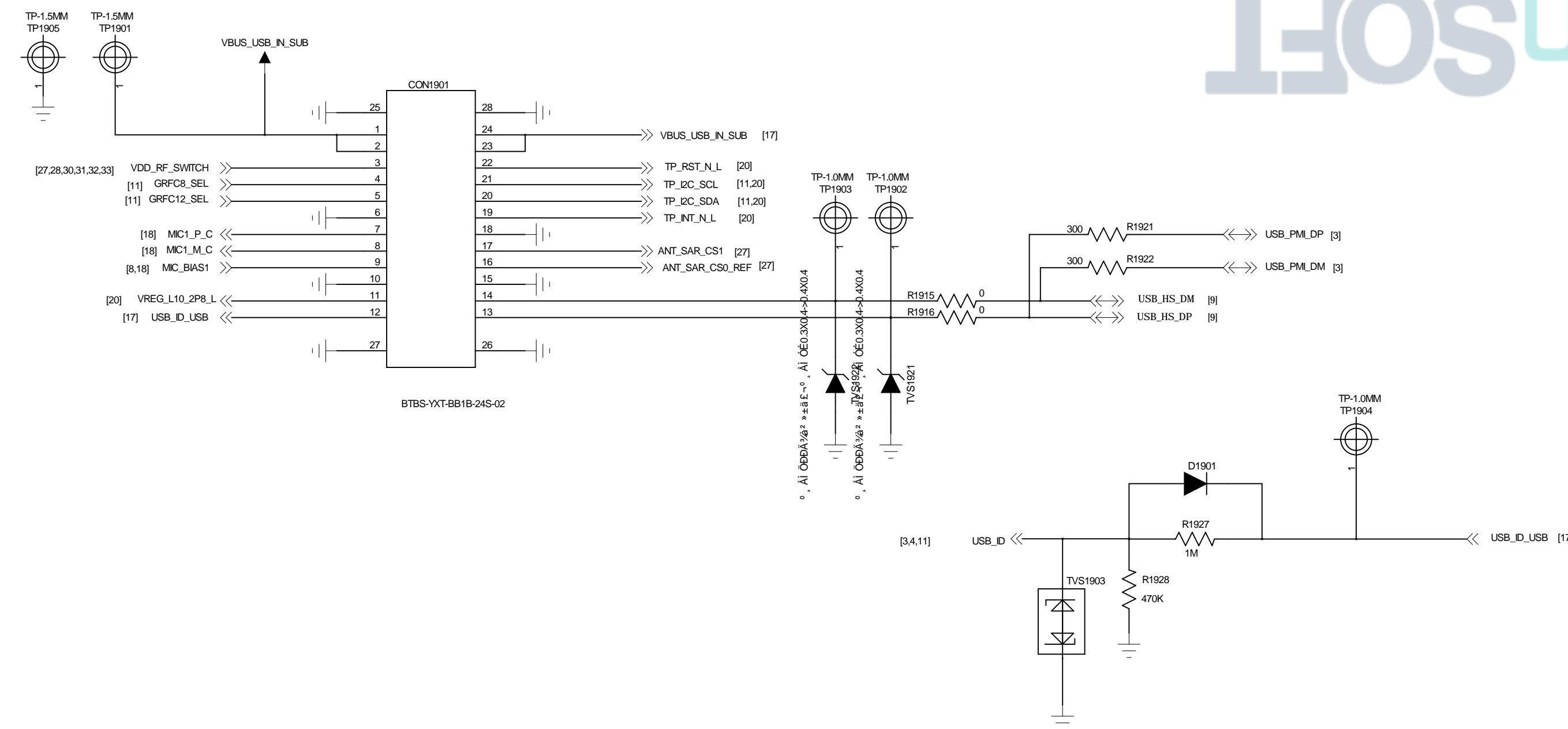
# LDO-3.3V



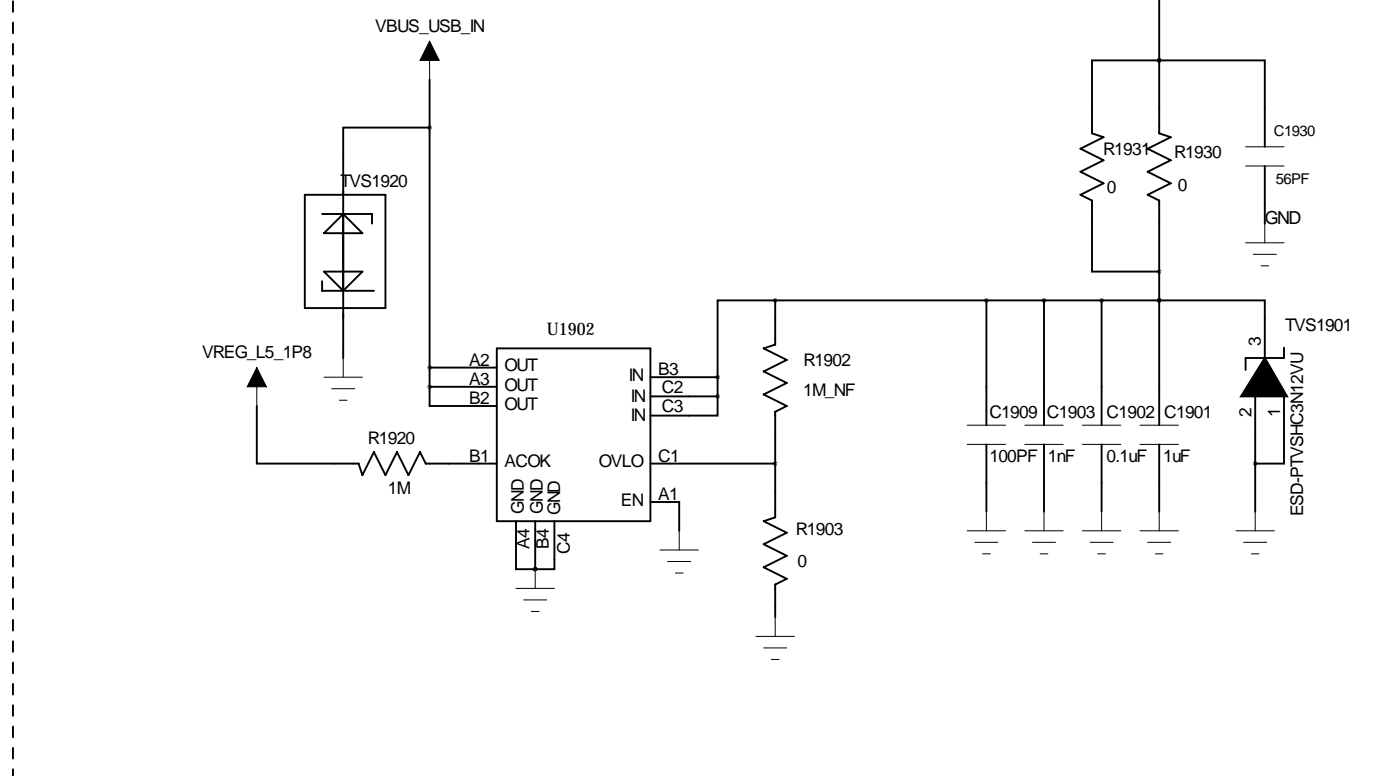
# LDO-1.8V



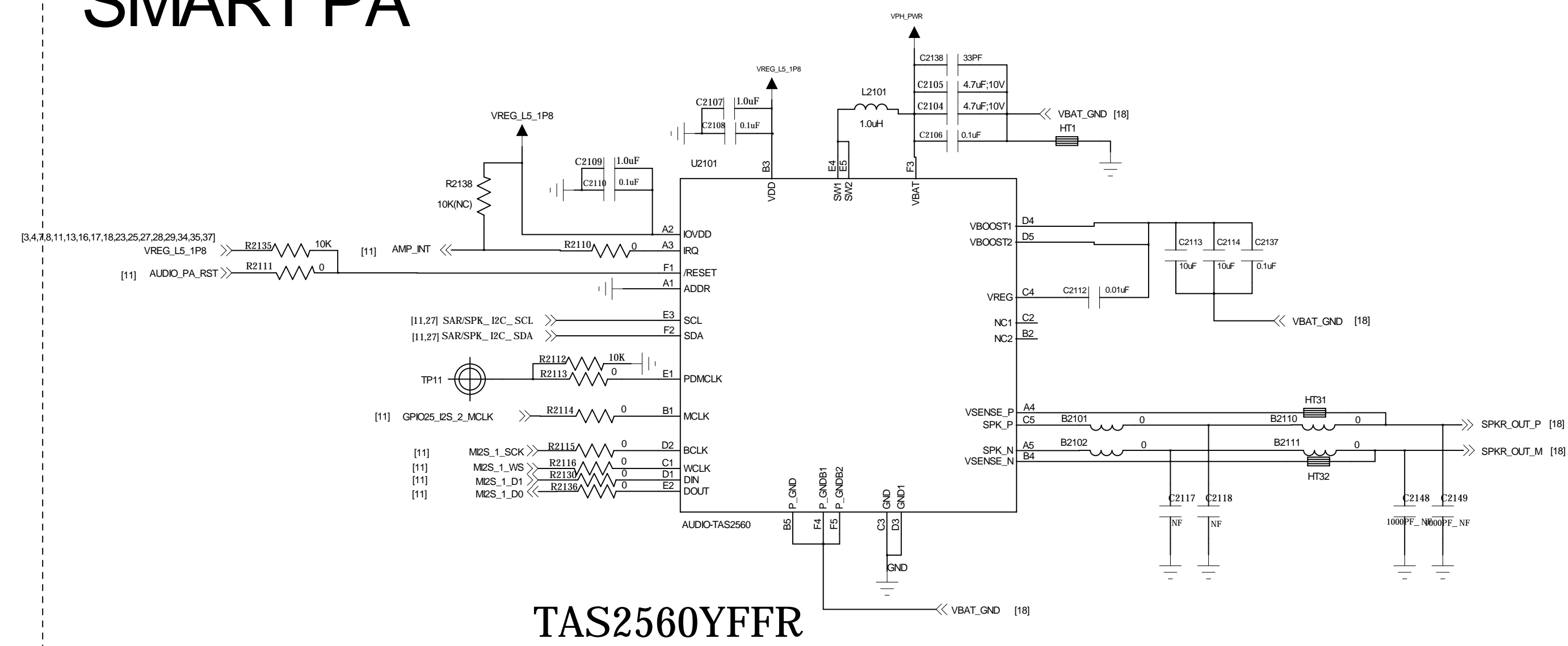
# SUB\_CONNECTOR



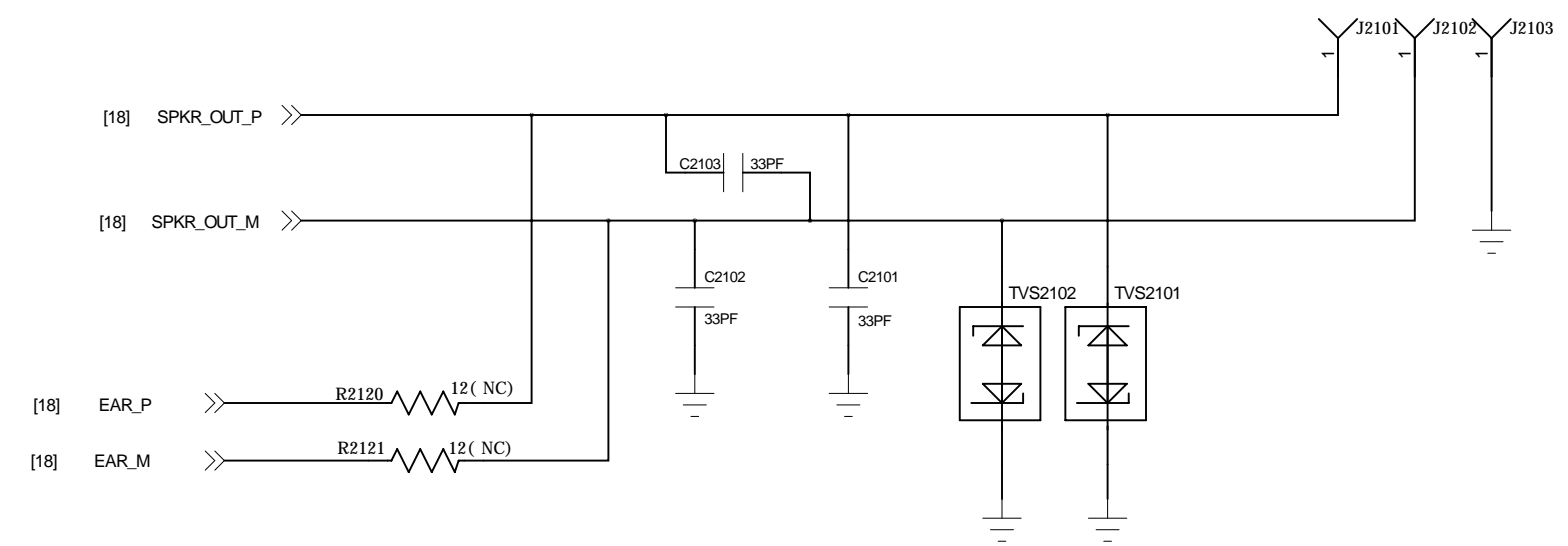
# OVP



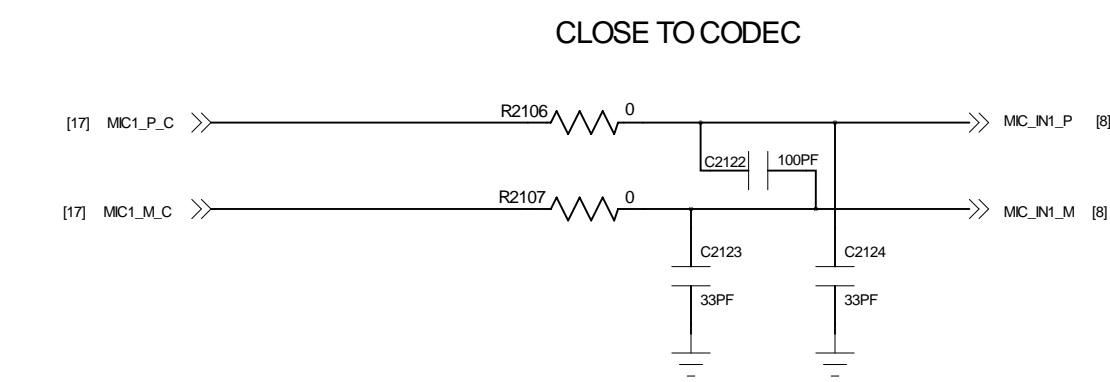
# SMART PA



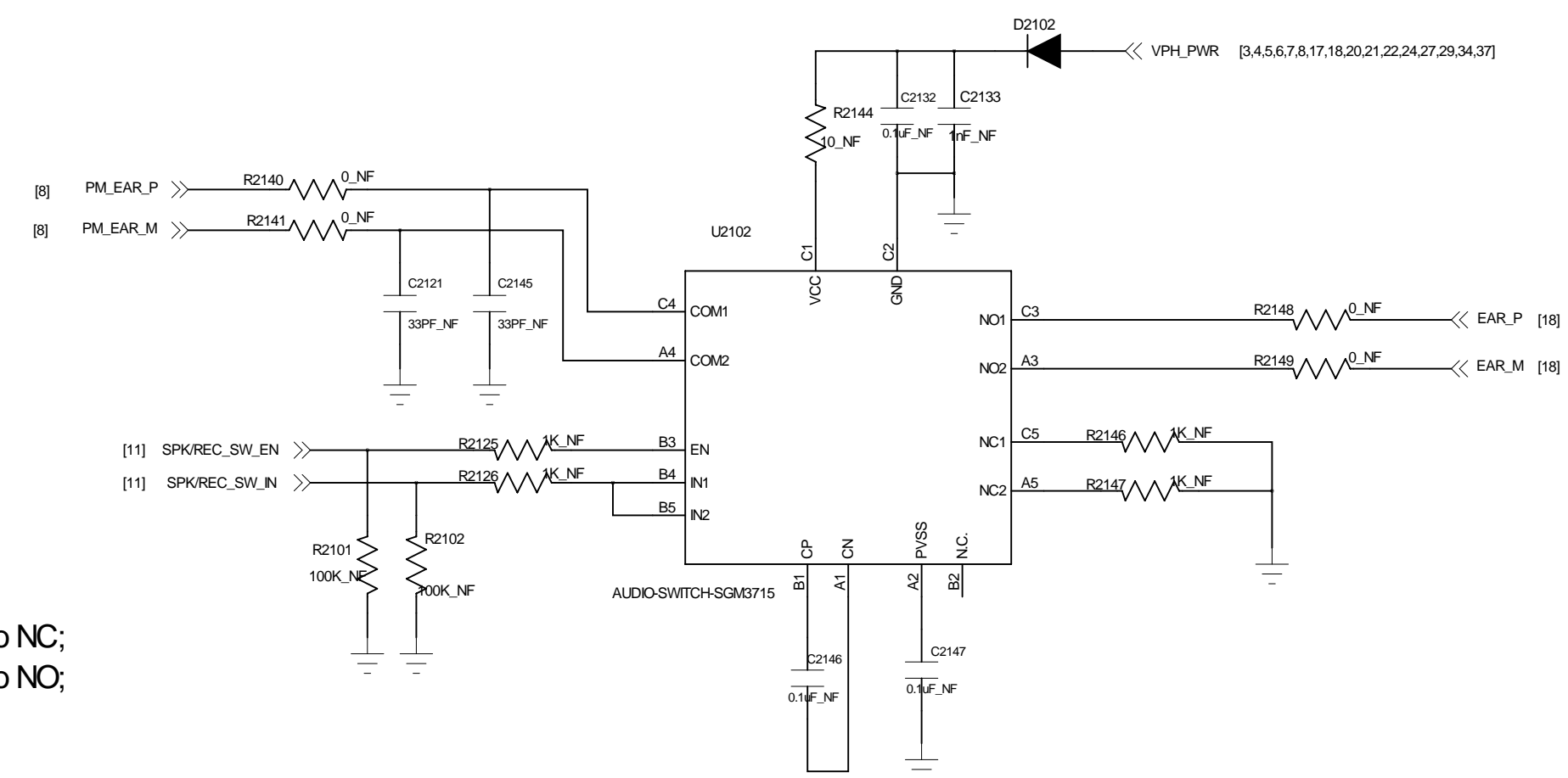
# REC&SPK



# PRIMARY MIC

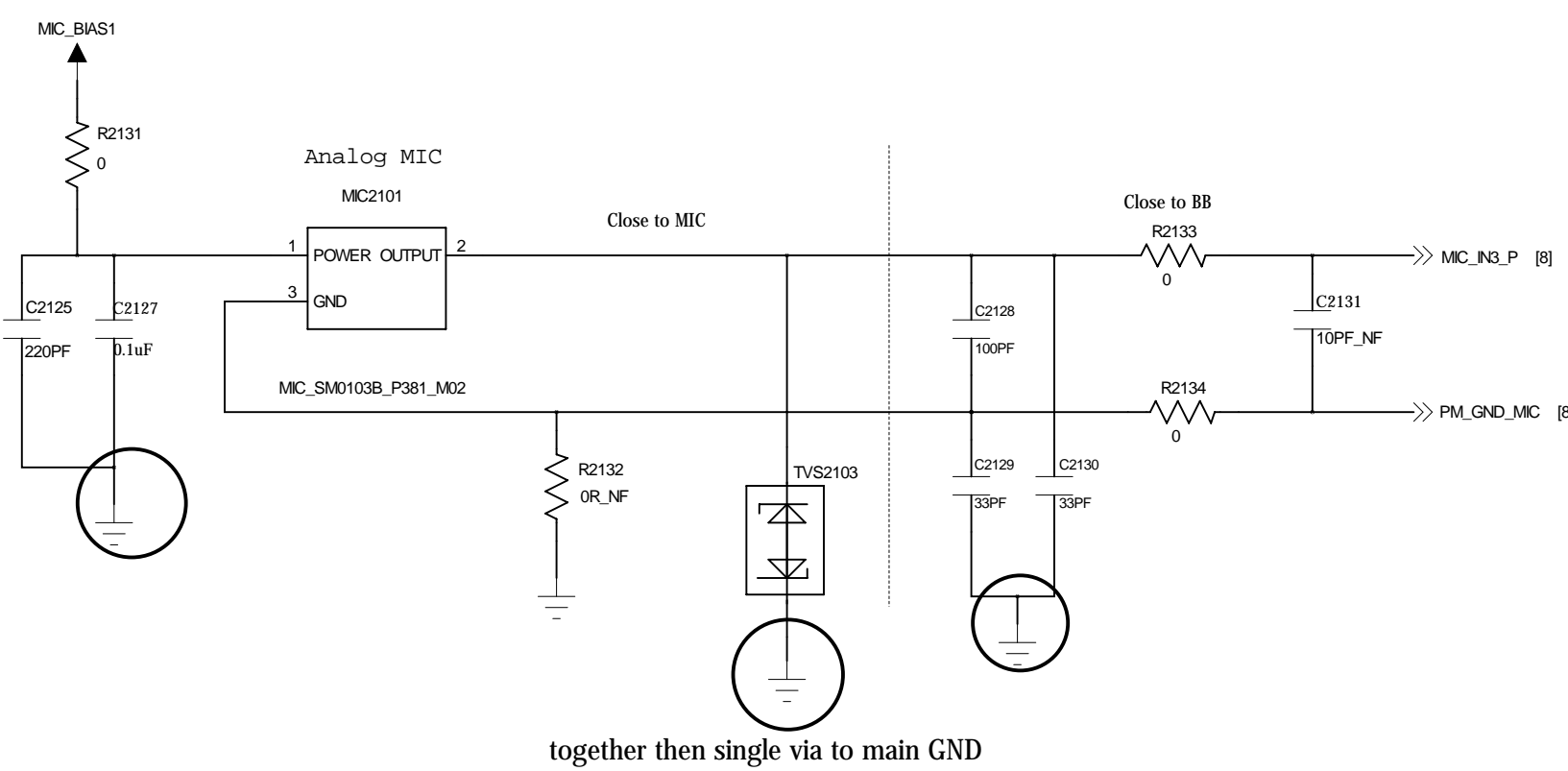


# SWITCH-ANOLOG-SGM3715

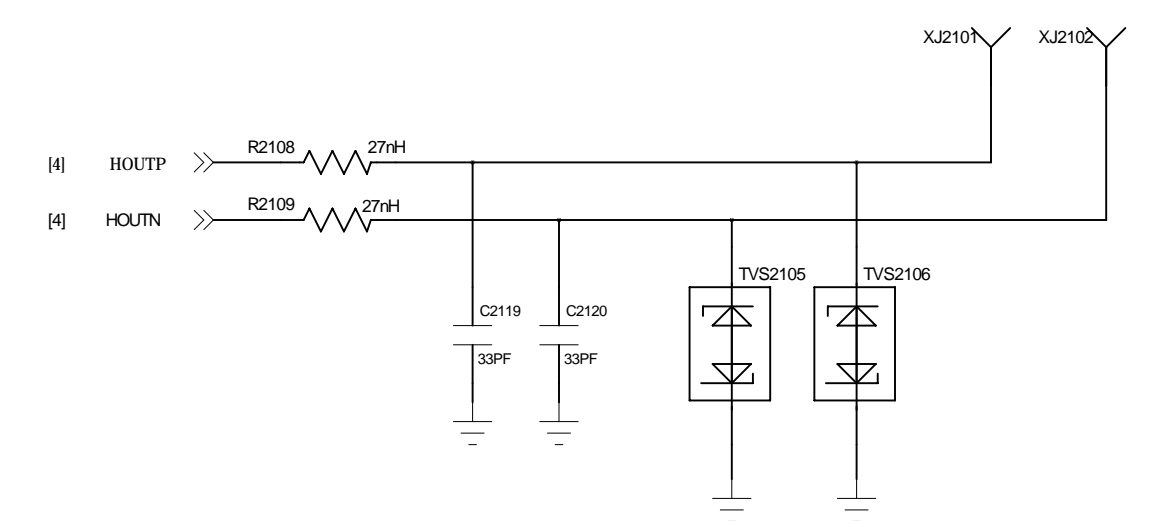


IN=0, COM Connected to NC;  
IN=1, COM Connected to NO;

# AUXMIC



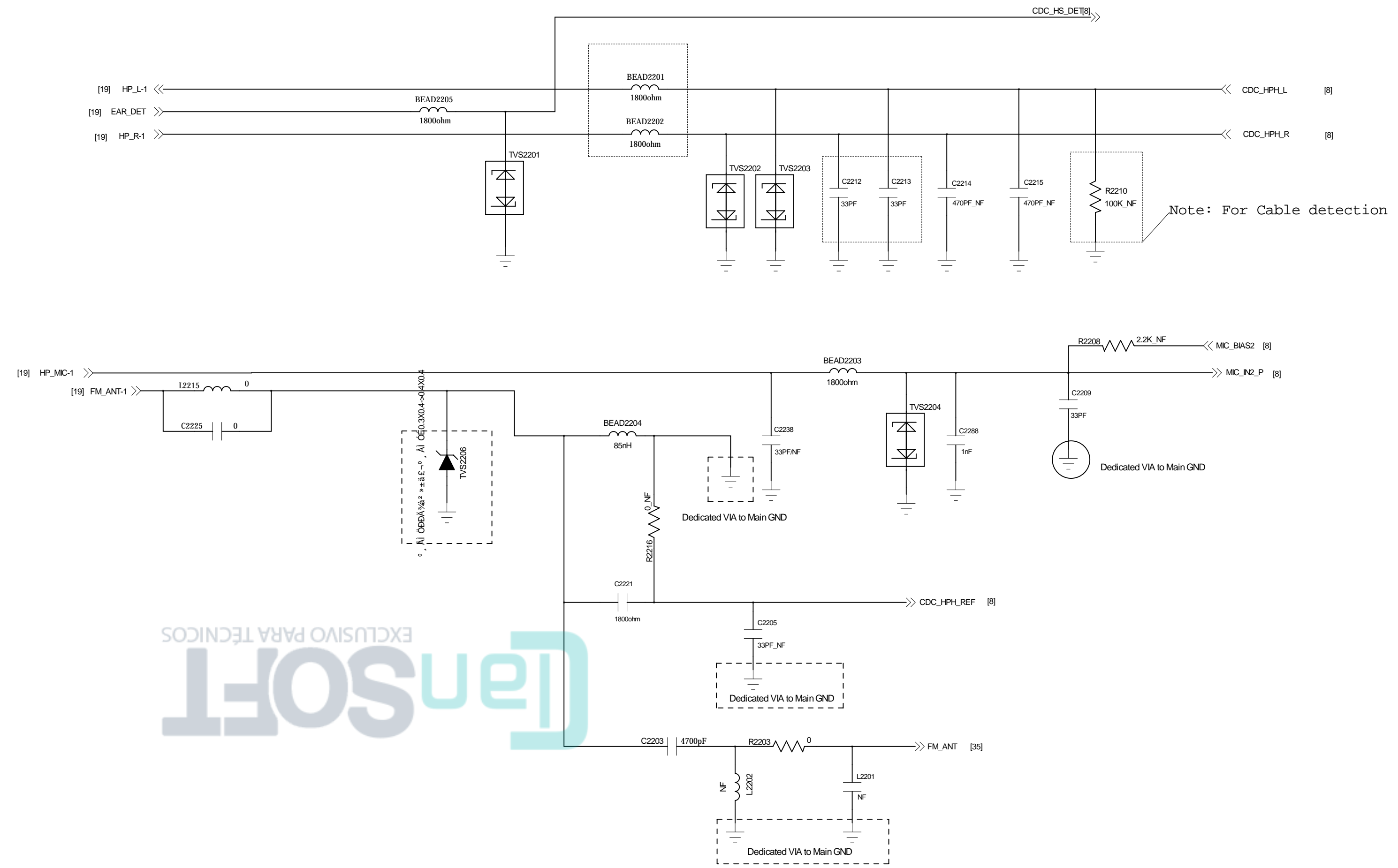
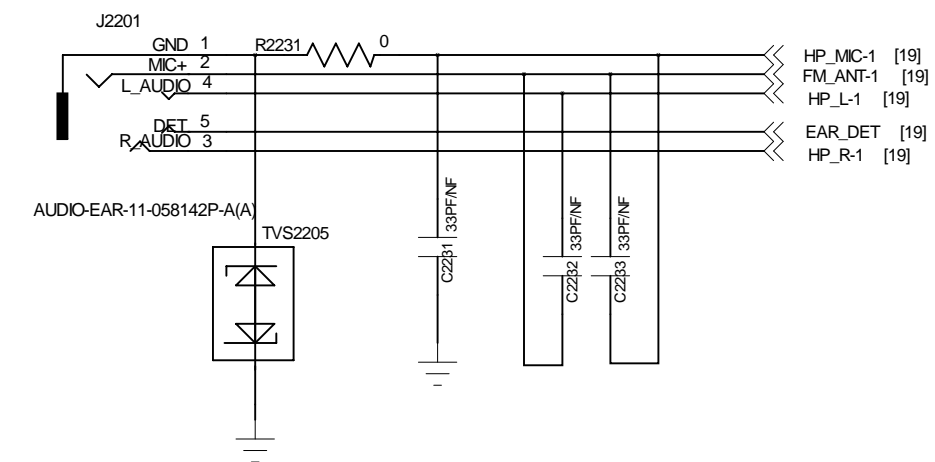
# MOTOR





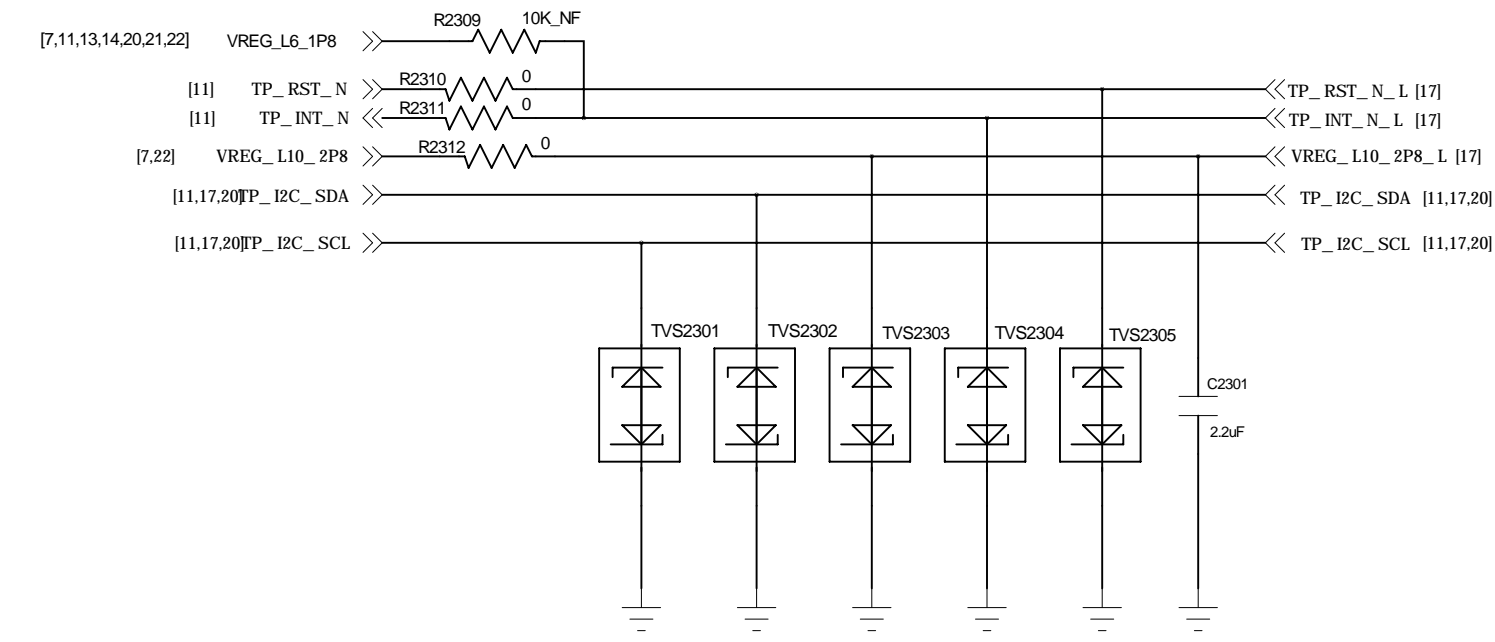
# EARPHONE

Note: Ferrite beads and their corresponding bypass capacitors on CDC\_HPH\_L, CDC\_HPH\_R and CDC\_HPH\_REF are needed to reduce noise generated by audio/FM concurrency

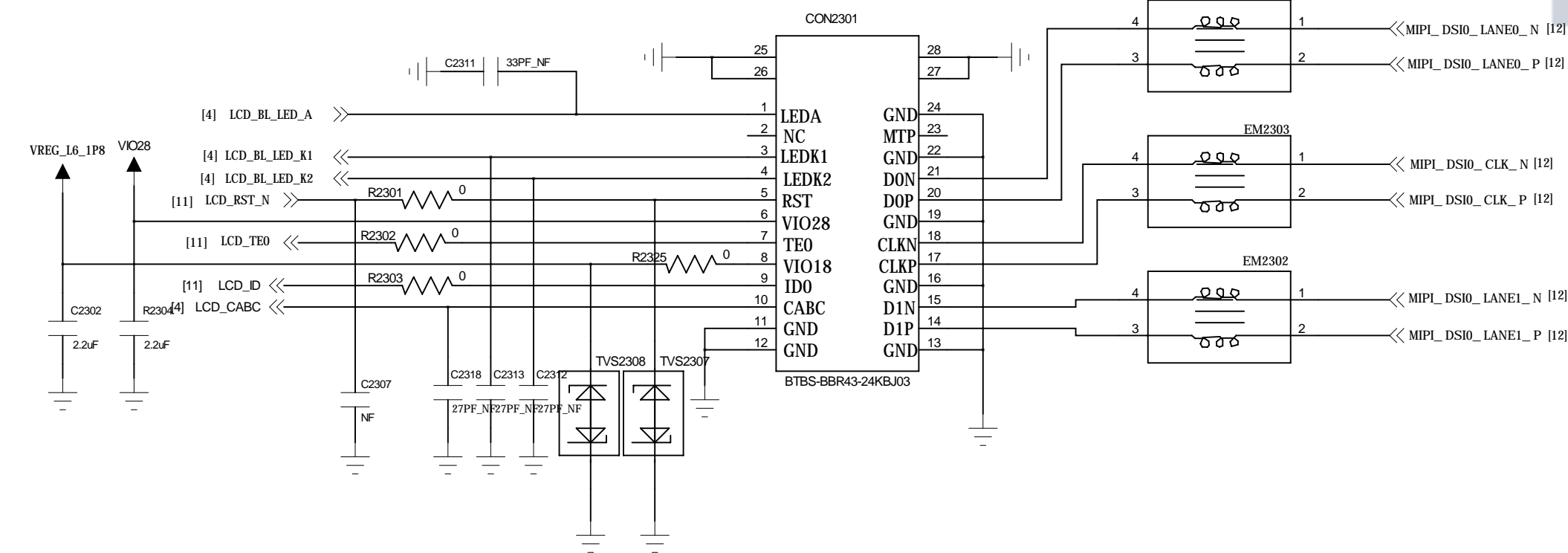


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**Tansoft**

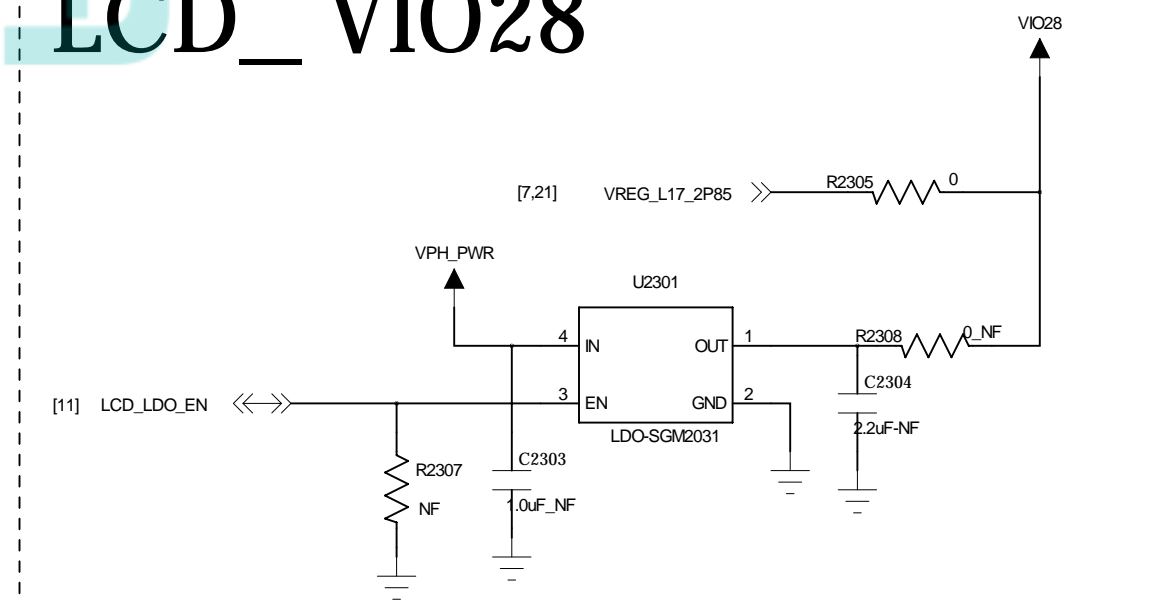
# CTP



# LCD

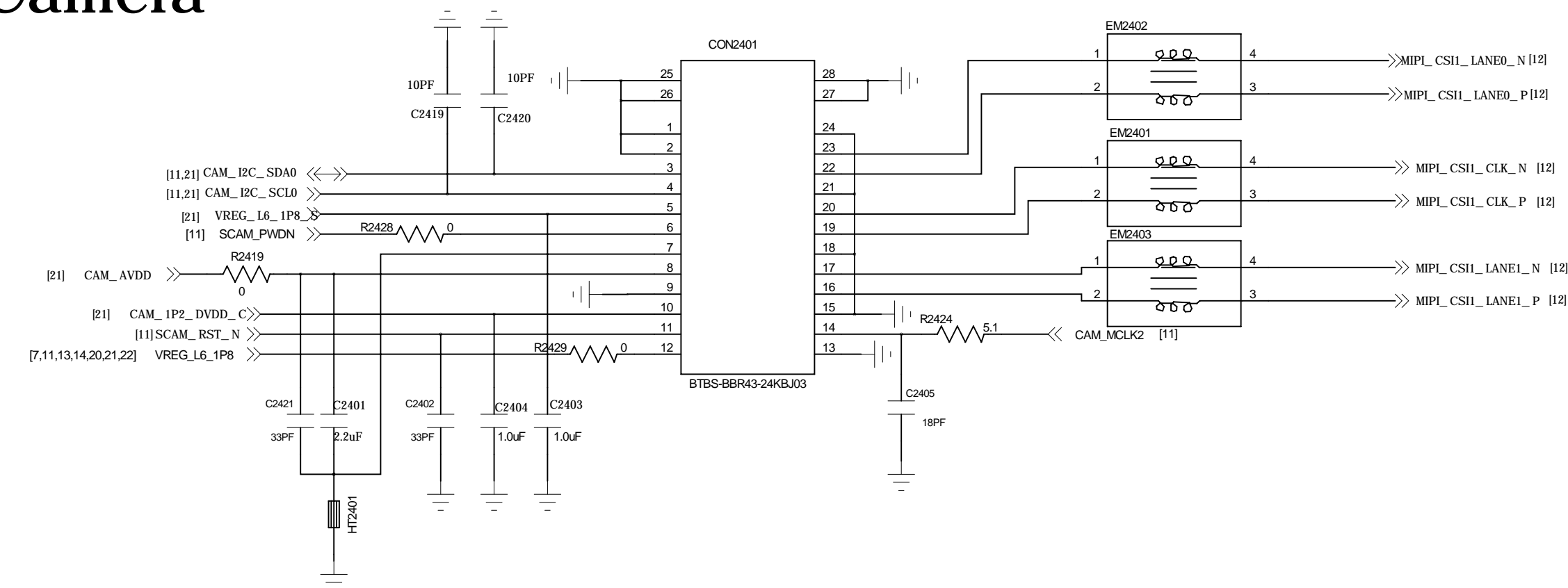


# LCD\_VIO28



Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

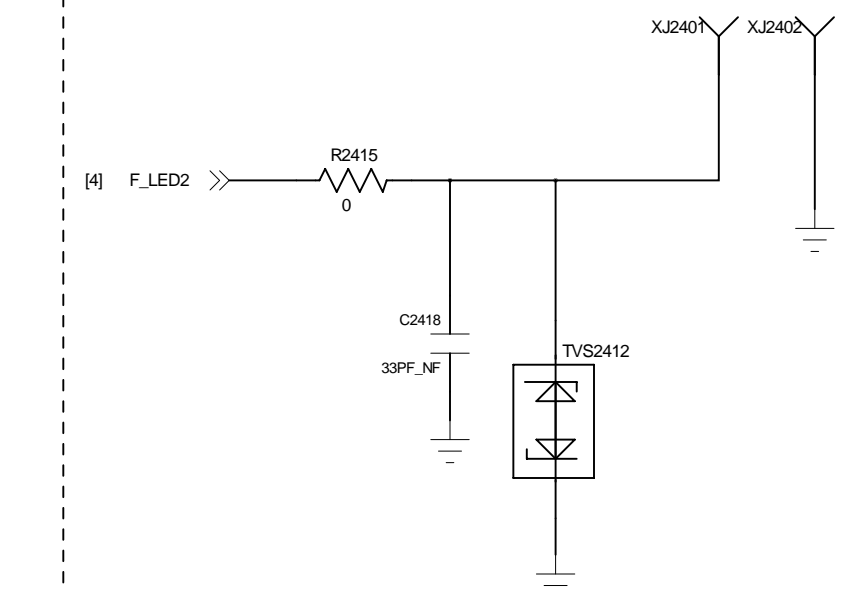
# Front Camera



PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	GND	GND	SDA	SCL	DOVDD	CAM_PDN (NC)	AGND	AVDD	GND	DVDD	CAM_RST	NC	GND	CMCLK	GND	ROP1_A	ROW_A	GND	RCP_A	RCN_A	GND	ROP0_A	ROW_A	GND

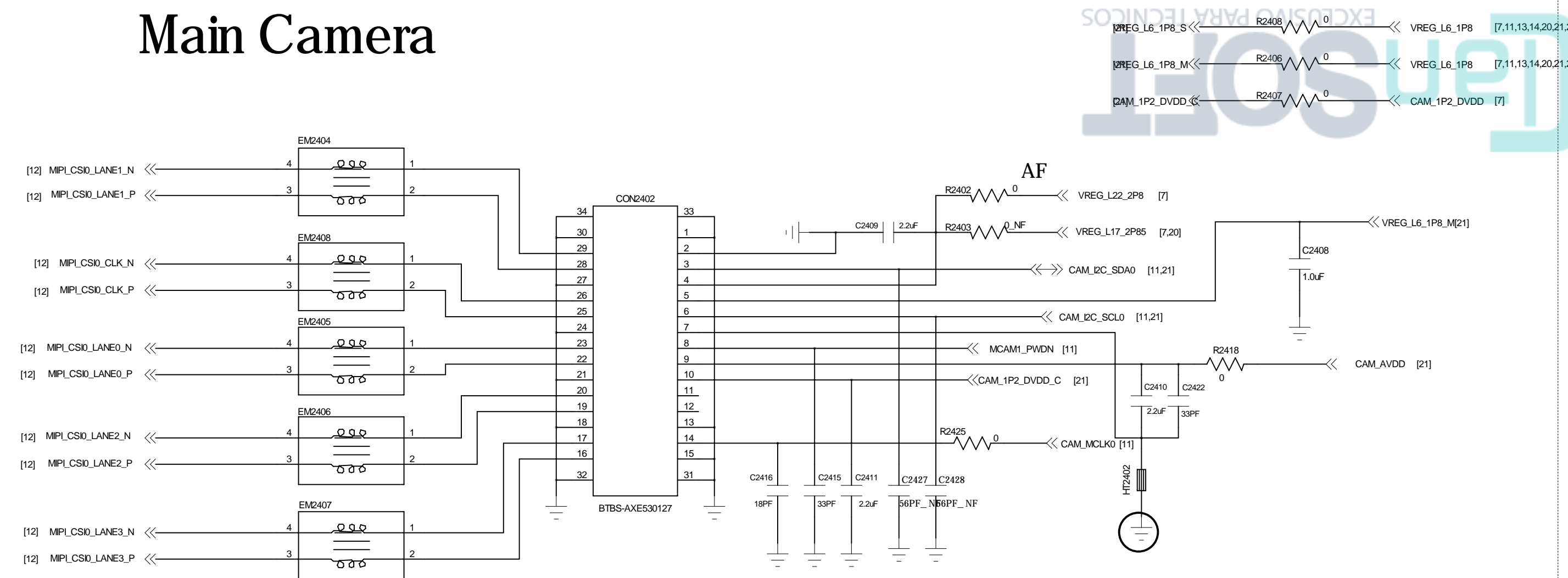
Main Camera / Sub Camera share power domain design should double check the voltage level is compatible

# Front Flash LED

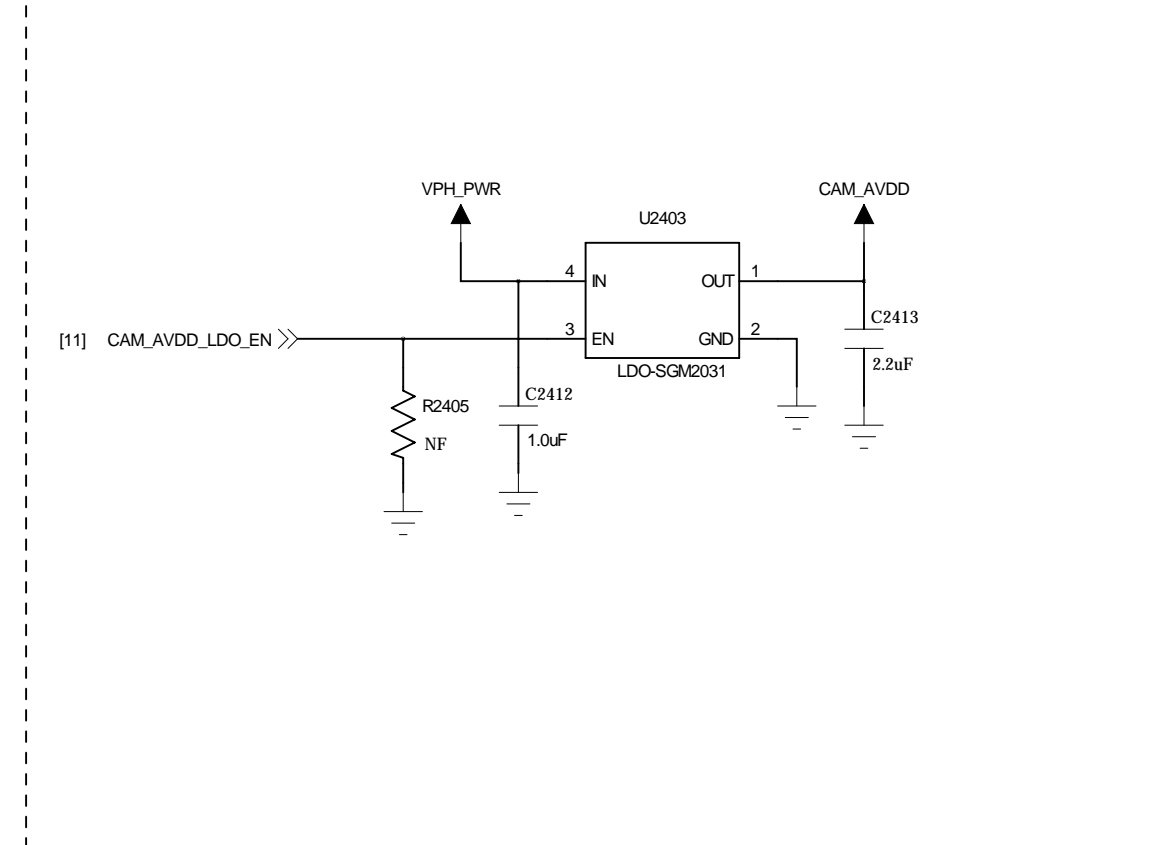


PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	DGND	AF-GND	SDA	AF-VCC	DOVDD	SCL	AGND	PWDN	AVDD	DVDD	NC	NC	DGND	XCLK	DGND	MDP3	MDN3	DGND	MDP2	MDN2	DGND	MDP0	MDN0	DGND	MCP	MCN	DGND	MDP1	MDN1	DGND

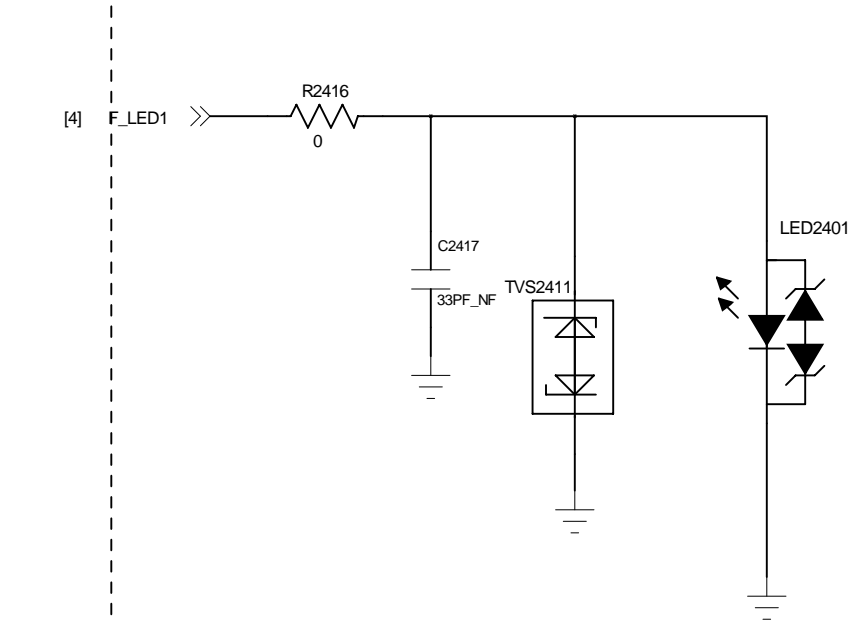
# Main Camera



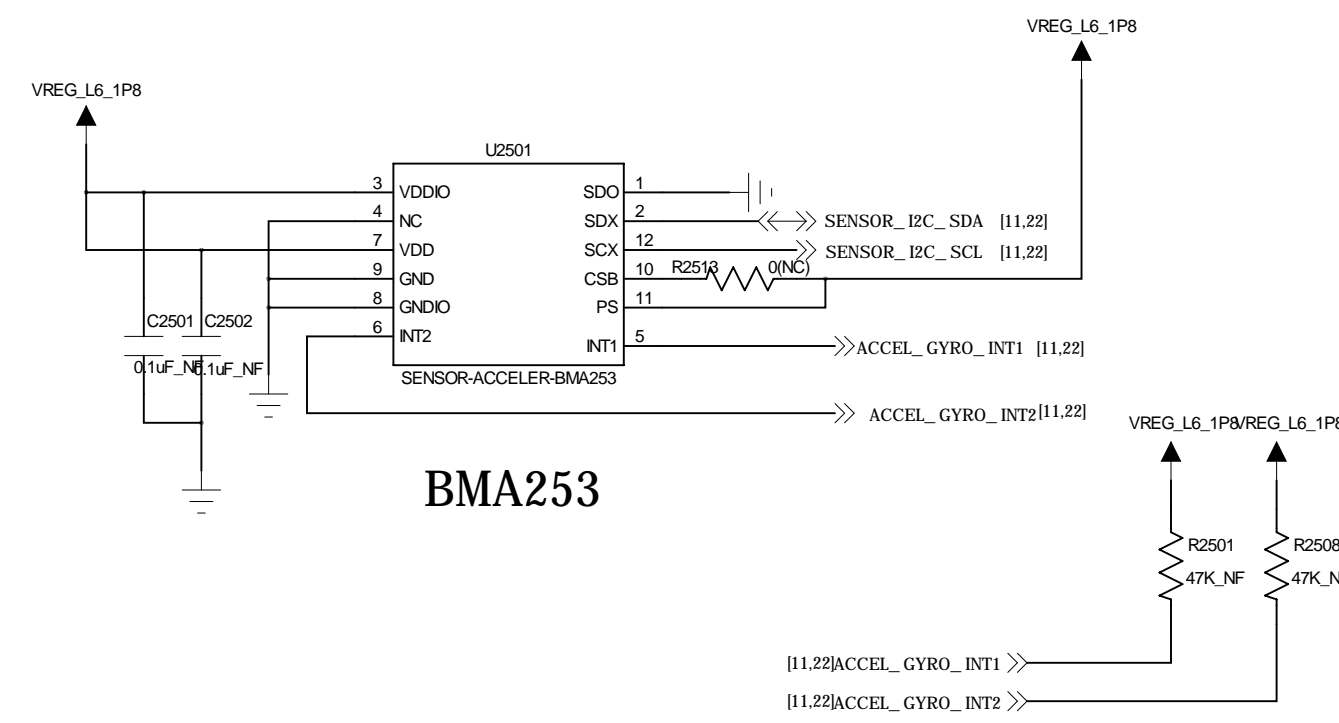
# EXT\_AVDD



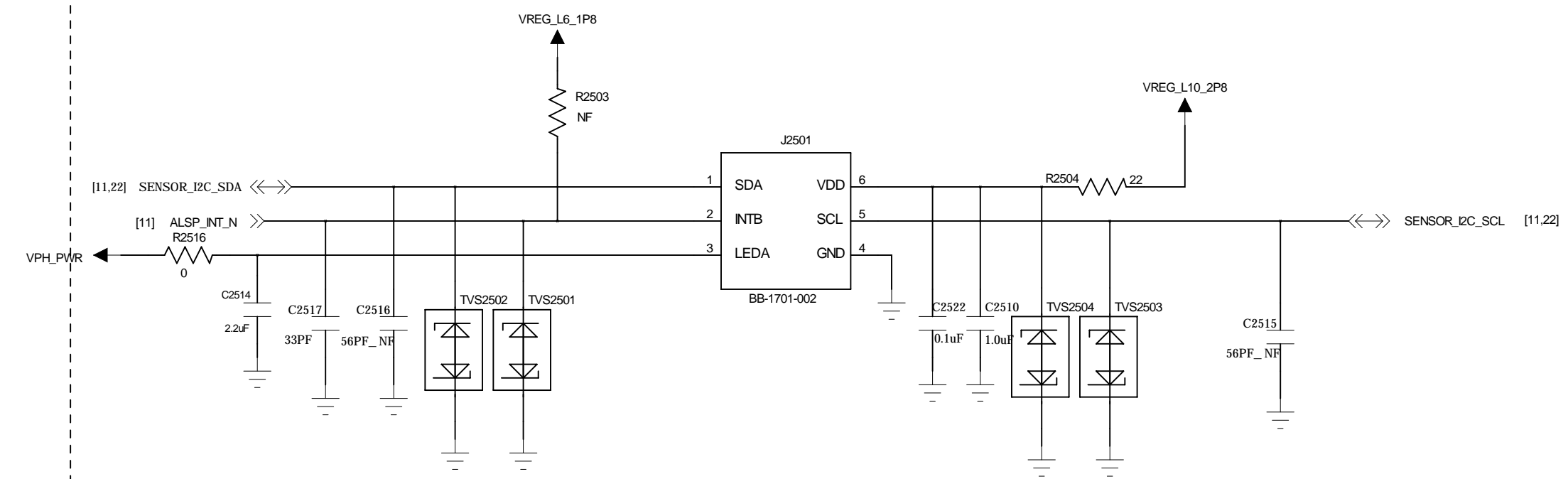
# Main Flash LED



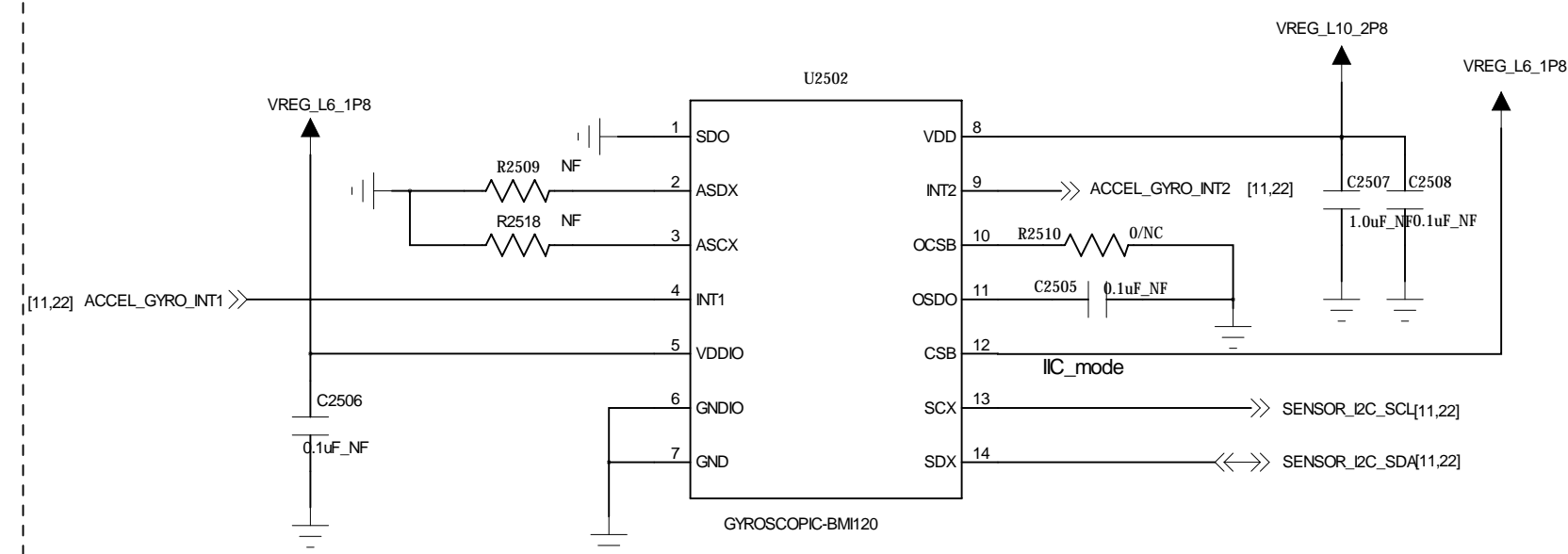
## G-Sensor



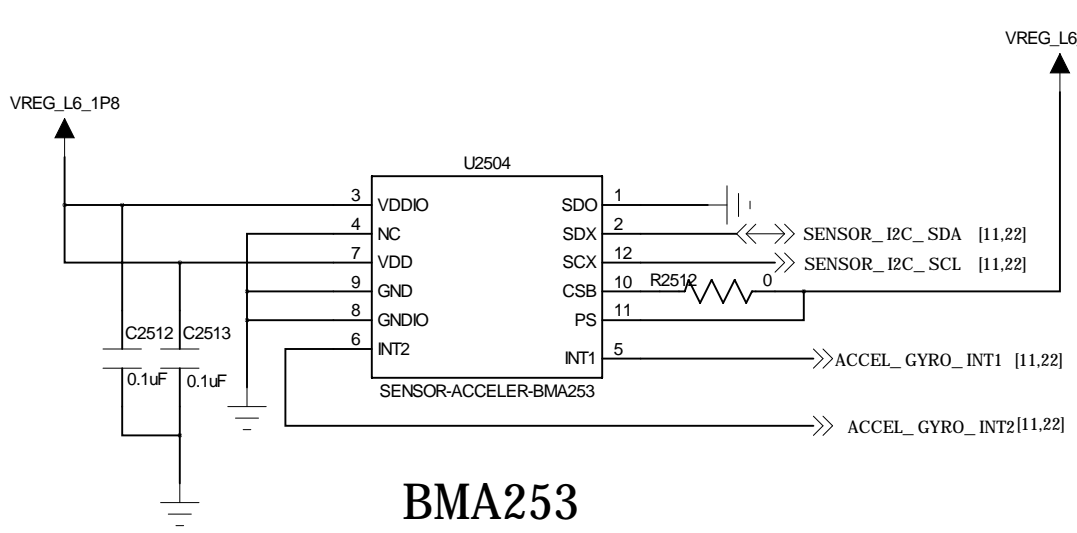
## ALS+PS+IR

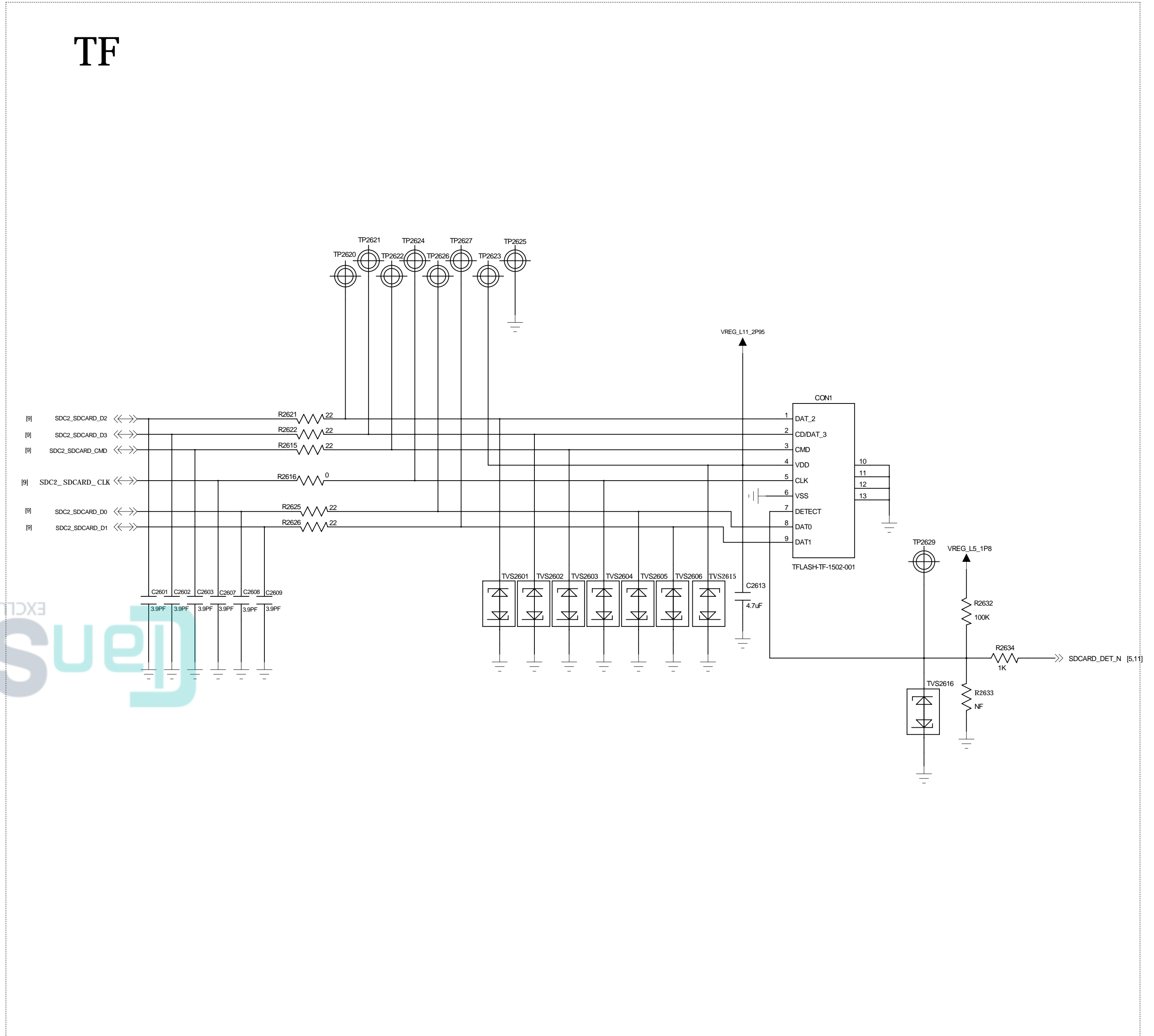
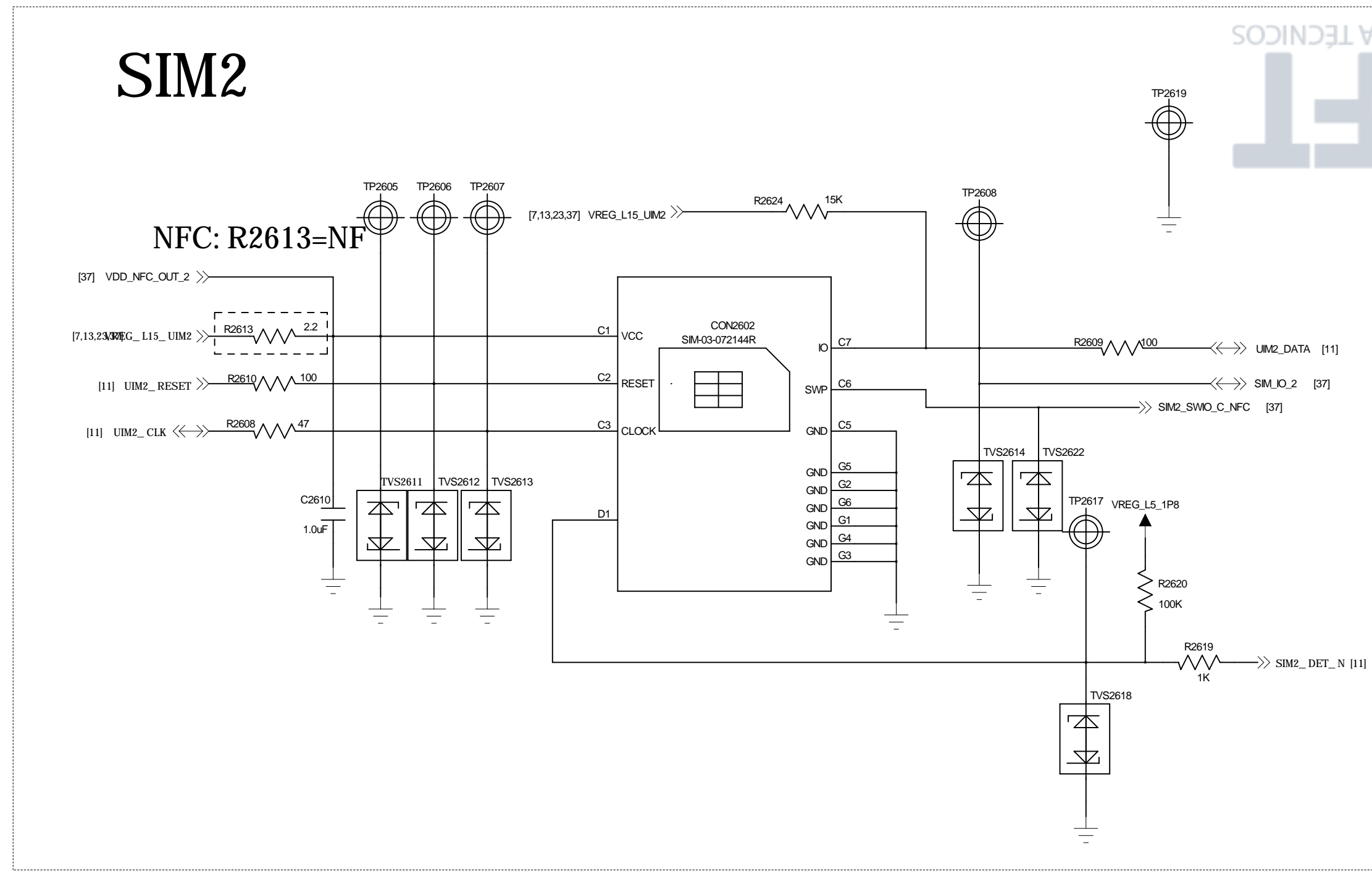
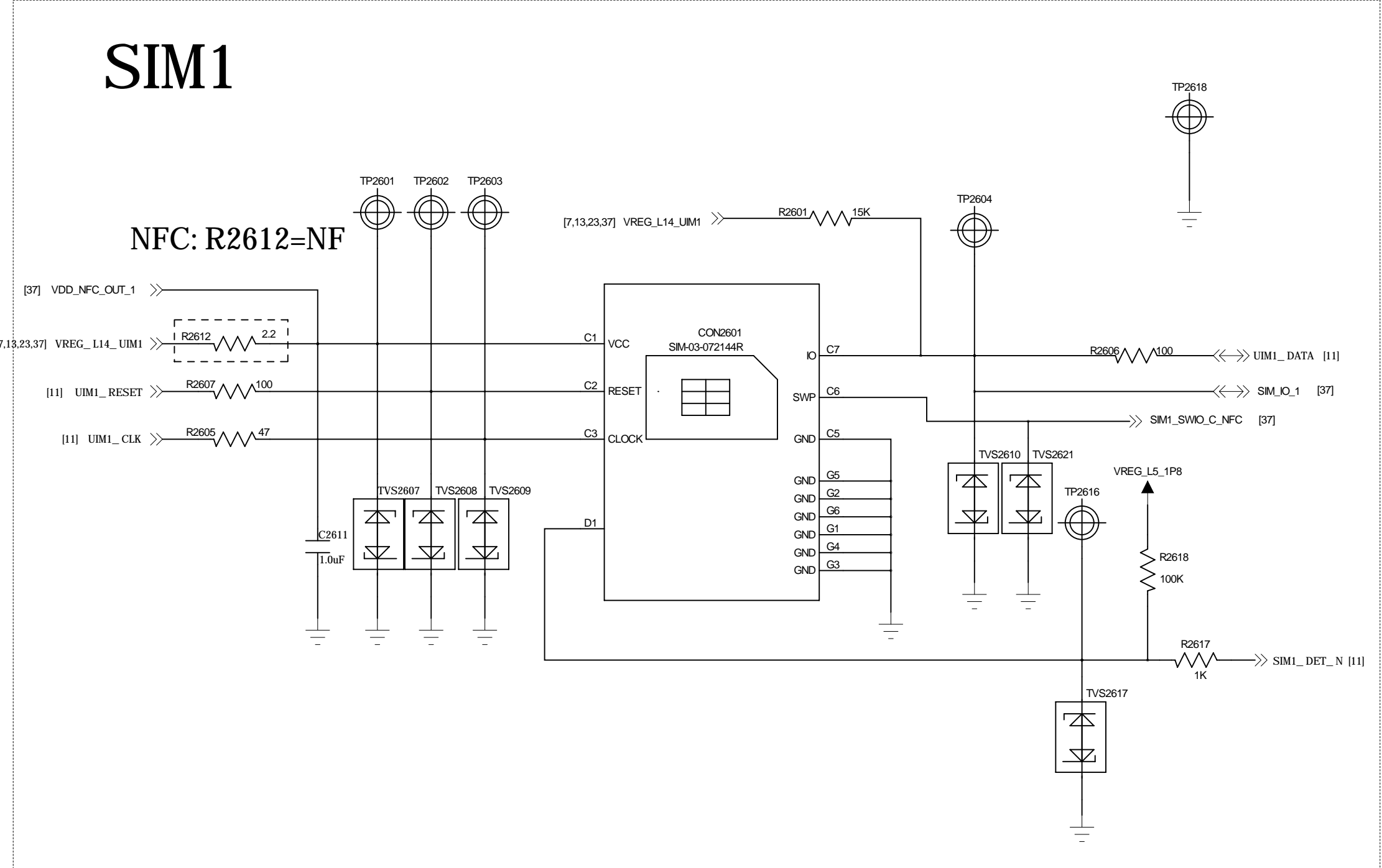


## Gyroscope



## G-Sensor



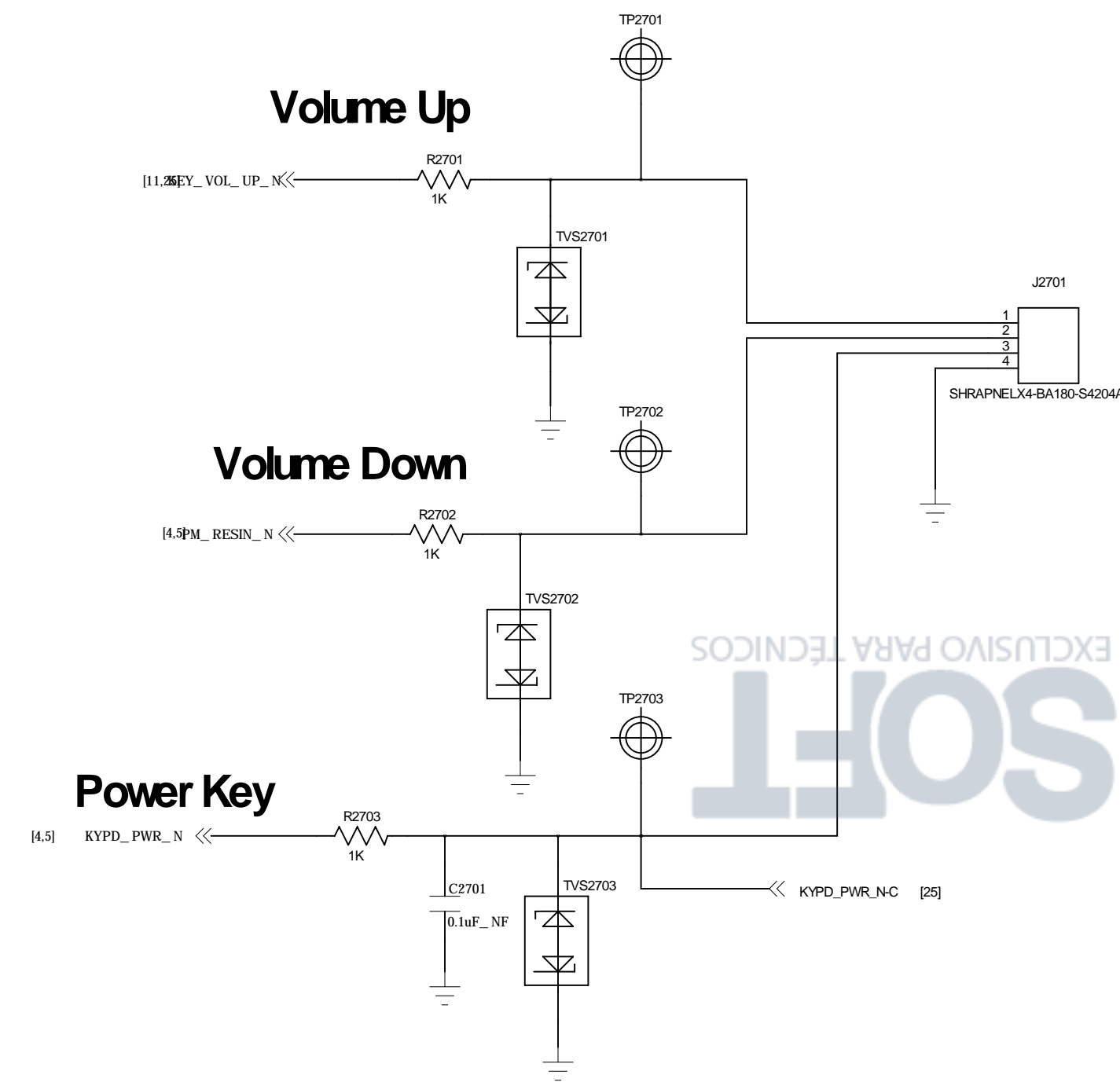


EXCLUSIVO PARA TÉCNICOS

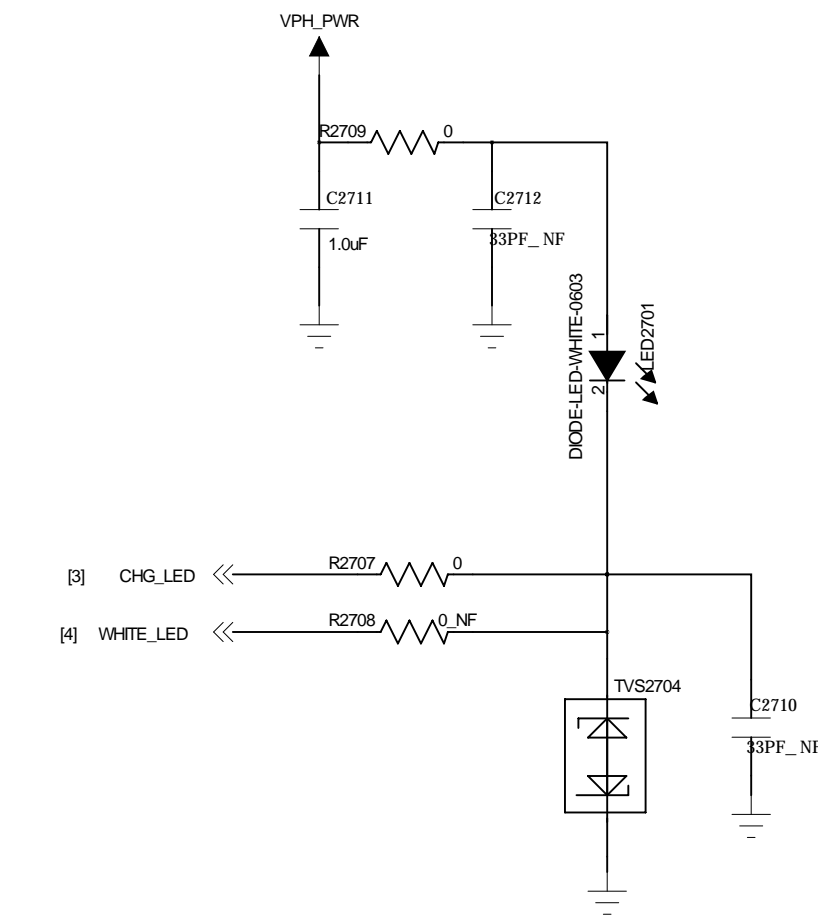
**TransSOFT**

# KEYPAD

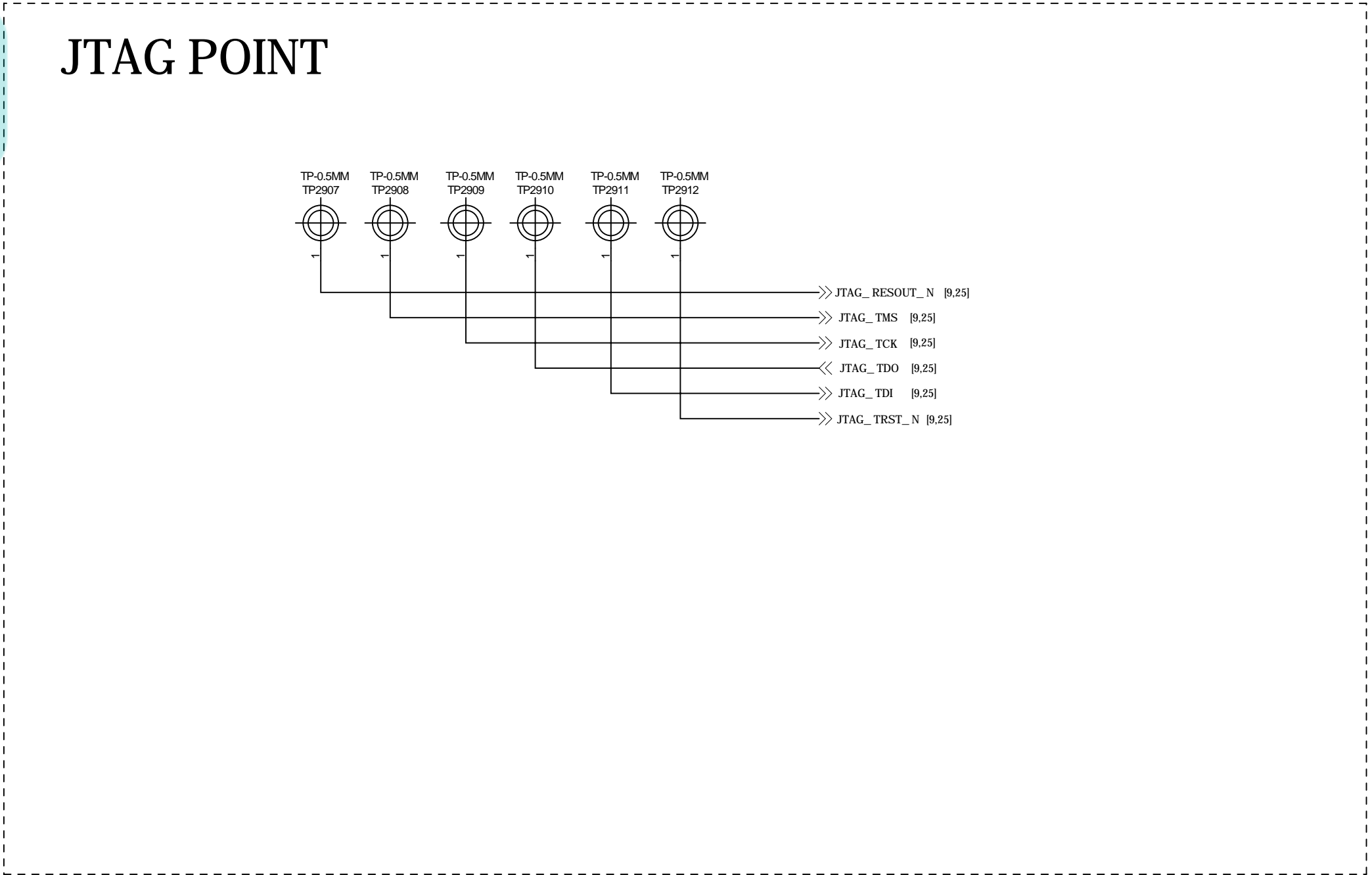
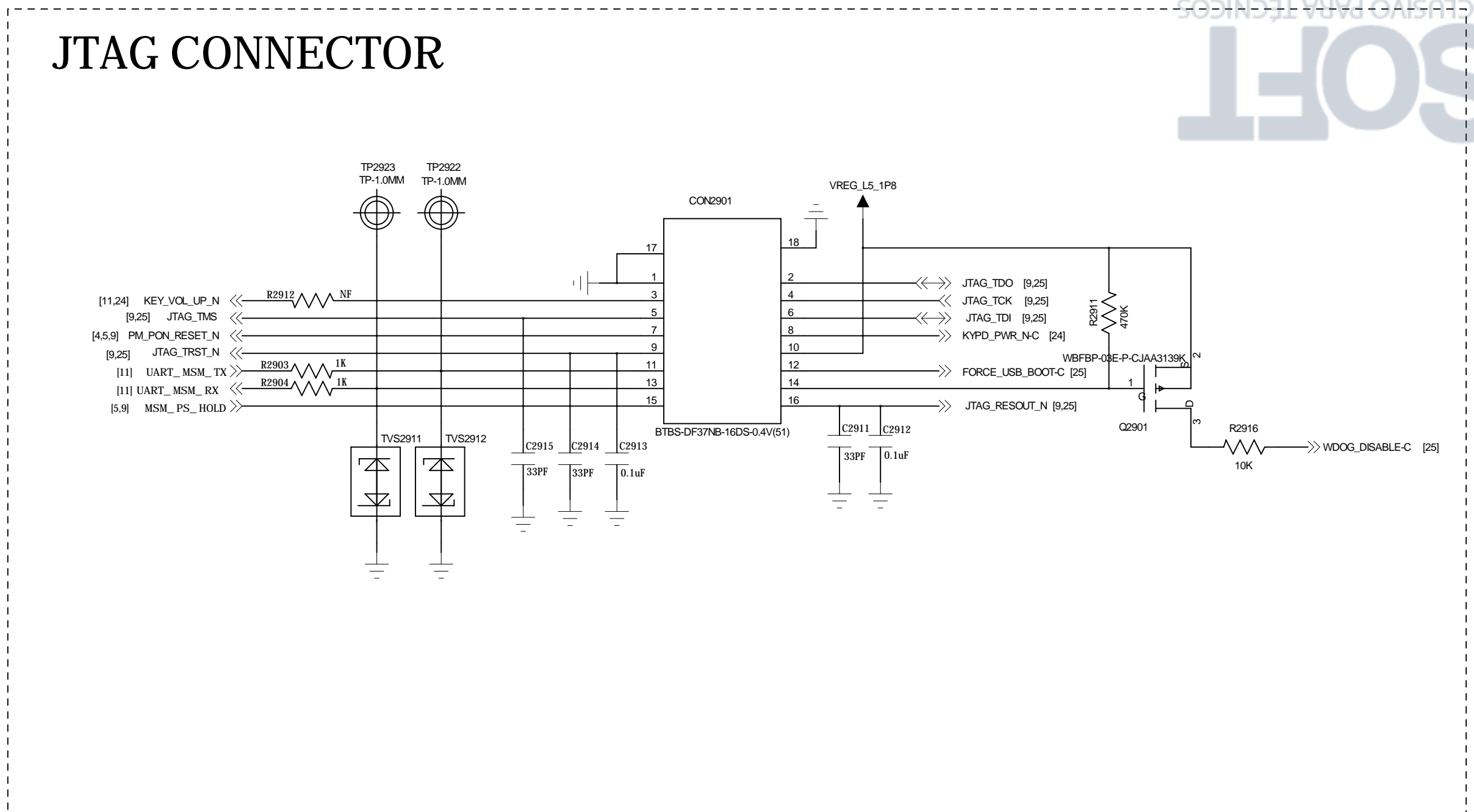
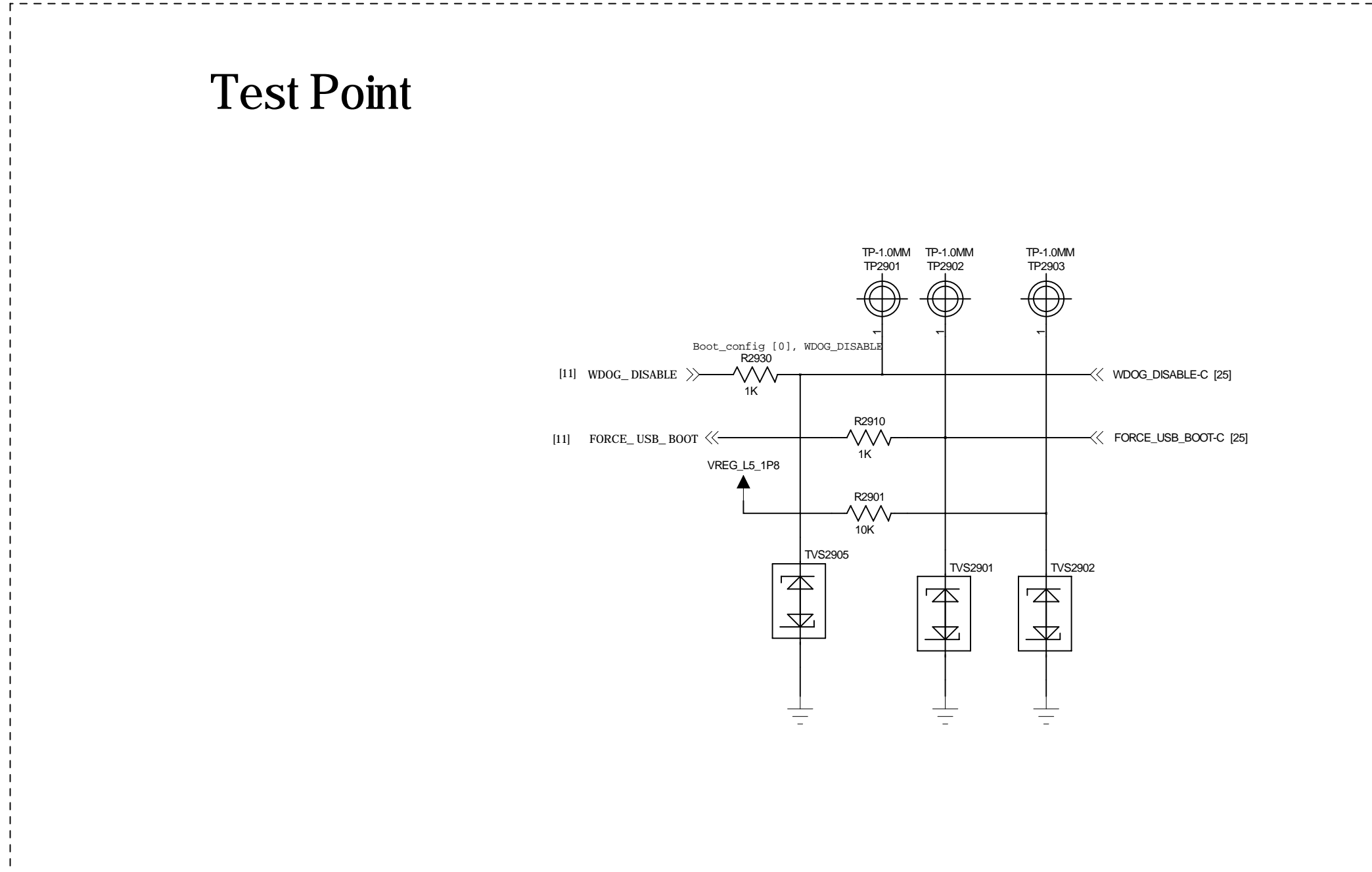
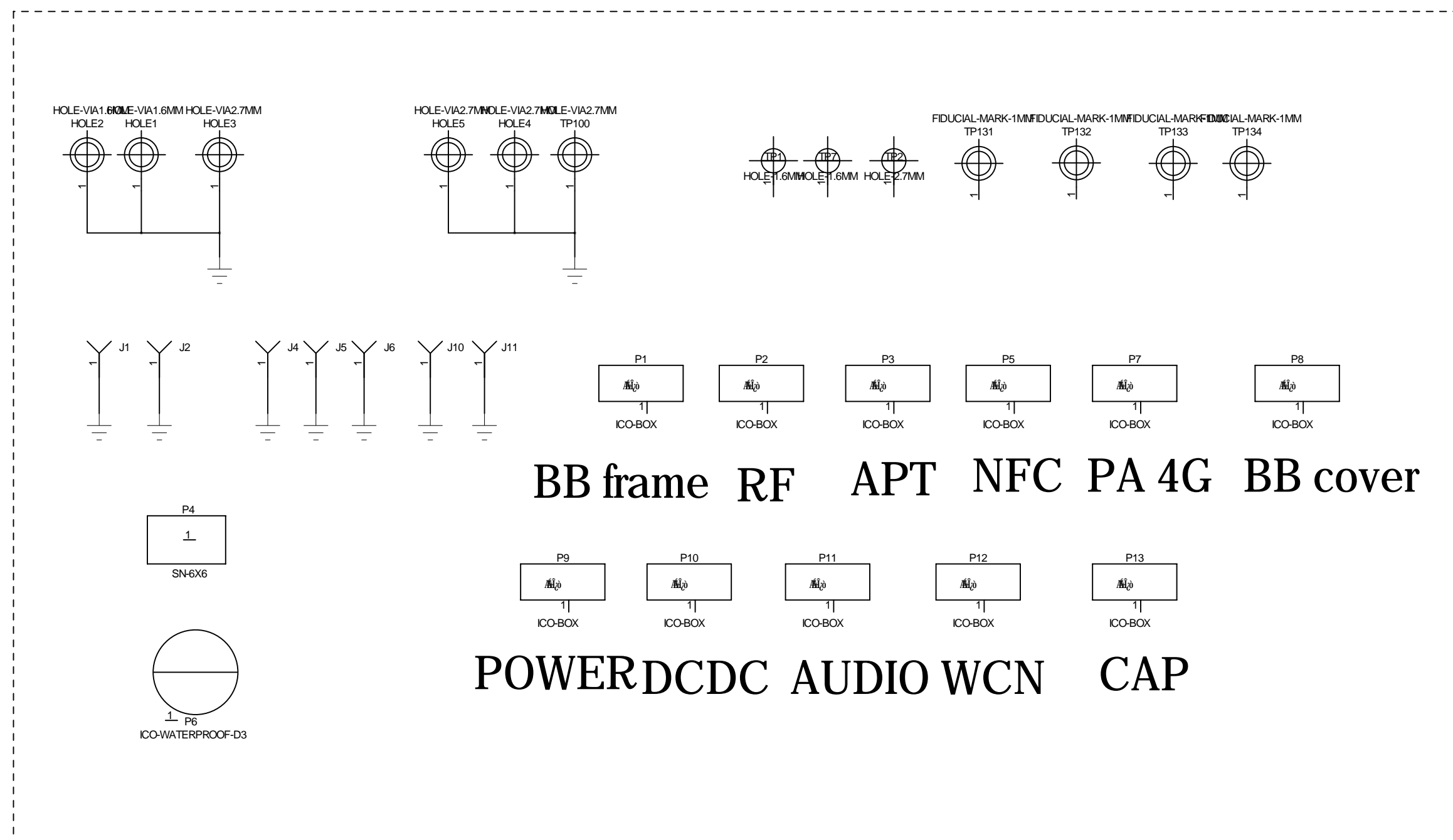
Signal	Description
KEY_VOL_UP_N	Volume Up
PM_RESIN_N	Volume Down
KYPD_PWR_N	POWER_ON
PM_RESIN_N + KYPD_PWR_N	Hardware Reset



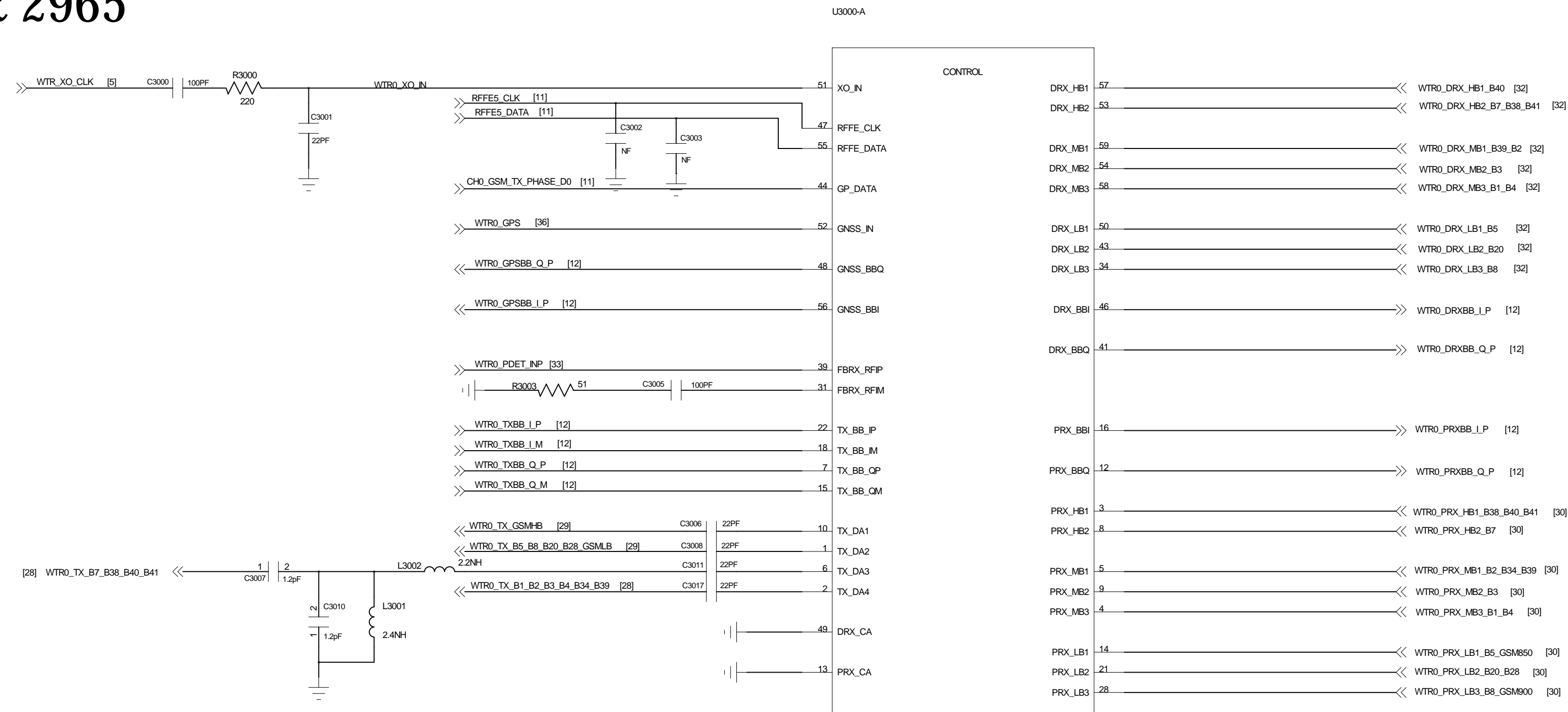
# INDICATOR LED



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**CanSoft**



# WTR 2965



**WTR2965 Tx port mapping**

RF port	GSM	CDMA	WCDMA	LTE-FDD	LTE-TDD	TD-SCDMA
Tx_DA1	850, 900, 1800, 1900	0, 10	8, 11	8, 11, 12, 13, 17, 21, 28	39	34, 39
Tx_DA2	850, 900	0, 10	5, 6, 8, 19	5, 6, 8, 18, 19, 20, 26, 27, 28	7, 30	38, 40, 41
Tx_DA3	1800, 1900	1, 6, 14, 15	1, 2, 3, 4, 9, 10, 11, 25	1, 2, 3, 4, 9, 10, 11, 21, 25, 66	34, 39	
Tx_DA4	1800, 1900					

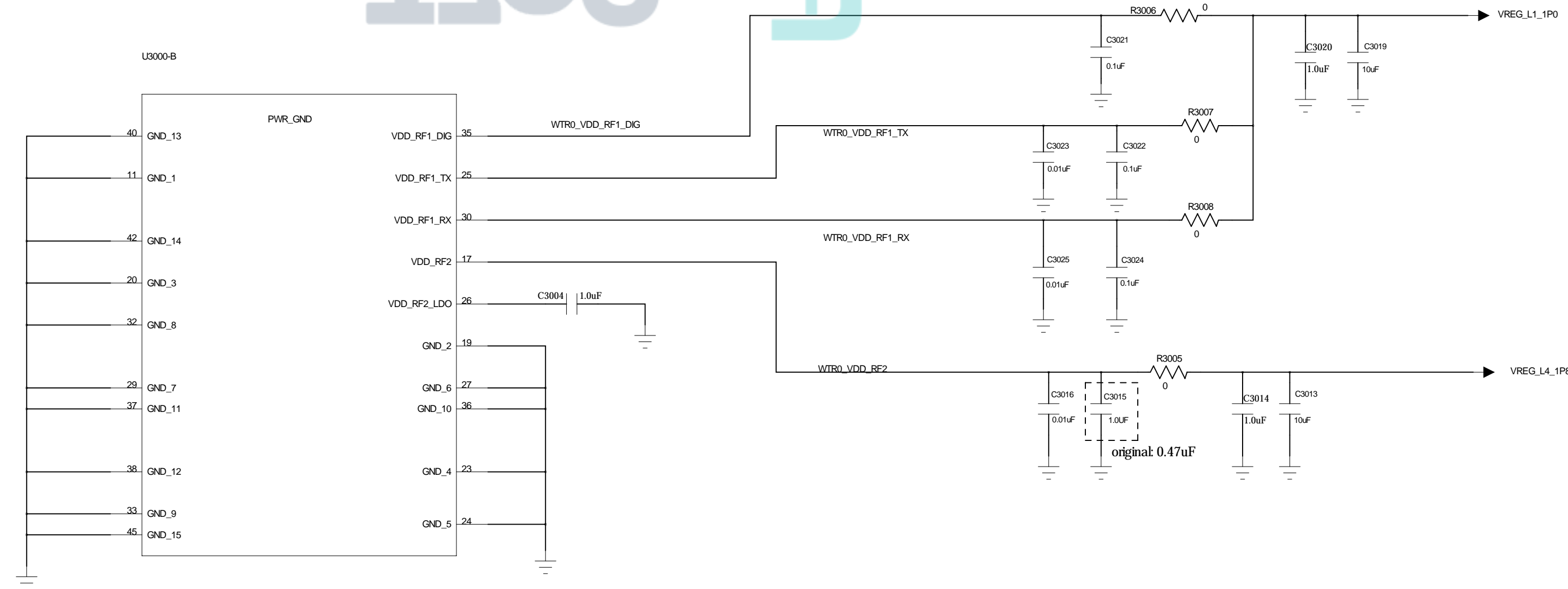
Note:RX ports have DC at the pin, so it need DC block, please make sure there is no DC short to other voltages and GND

## Rx port mapping

WTR2965							Remarks
	CDMA	GSM	WCDMA	LTE-FDD	TD-SCDMA	LTE-TDD	
PRx_LB1	BC0,10	850, 900 850 SAWless, 900 SAWless	5, 6, 8, 19	5, 6, 8, 18, 19, 26, 27			SAWless and SAW mode is not supported at the same time
PRx_LB2		1900		12, 13, 17, 20, 28			
PRx_LB3	BC0,10	850, 900	5, 8	5, 6, 8, 13, 18, 19, 20, 26, 27, 28, 29			
PRx_MB1	BC15, BC1,14	1800 SAWless, 1900 SAWless	2, 4, 10, 11, 25	2, 4, 10, 11, 21, 25, 32	34 SAW/SAWless 39 SAW/SAWless	34 SAW/SAWless 39 SAW/SAWless	SAWless and SAW mode is not supported at the same time
PRx_MB2	BC1,14	1800, 1900	2, 3, 9, 25	2, 3, 9, 25	34, 39	34, 39	
PRx_MB3	BC6, 15	1800	1, 3, 4, 9, 10	1, 3, 4, 9, 10, 66			
PRx_HB1				30			38, 40, 41
PRx_HB2				7			38, 41

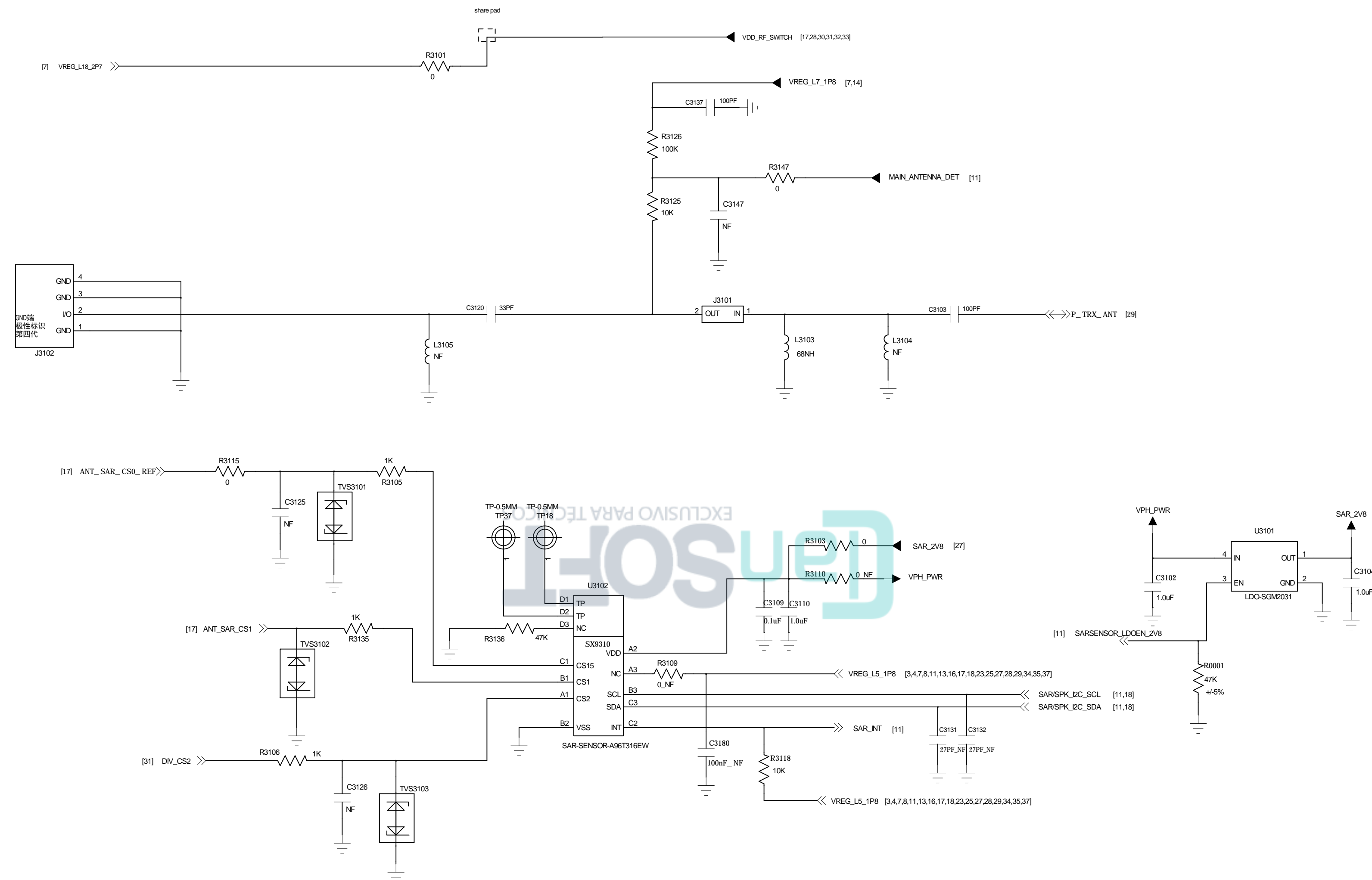
  

	CDMA	GSM	WCDMA	LTE-FDD	TD-SCDMA	LTE-TDD
DRx_LB1	BC0, 10	850, 900	5, 6, 8, 19	5, 6, 8, 18, 19, 26, 27		
DRx_LB2				12, 13, 17, 20, 28		
DRx_LB3	BC0, 10	850, 900	5, 8	5, 6, 8, 13, 18, 19, 20, 26, 27, 28, 29		
DRx_MB1	BC15, BC1,14	1900	2, 4, 10, 11, 25	2, 4, 10, 11, 21, 25, 32	34, 39	34, 39
DRx_MB2	BC1, 14	1800, 1900	2, 3, 9, 25	2, 3, 9, 25	34, 39	34, 39
DRx_MB3	BC6, 15	1800	1, 3, 4, 9, 10	1, 3, 4, 9, 10, 66		
DRx_HB1				30		
DRx_HB2				7		





# PRIMARY\_ANT



3/4G PA

Band7

Band40

Band4

Band3

Band1

Band2

Band5/BC0

Band20/28A

Band8

Band28B

Note: The SAW BW=120MHz

Band38/41

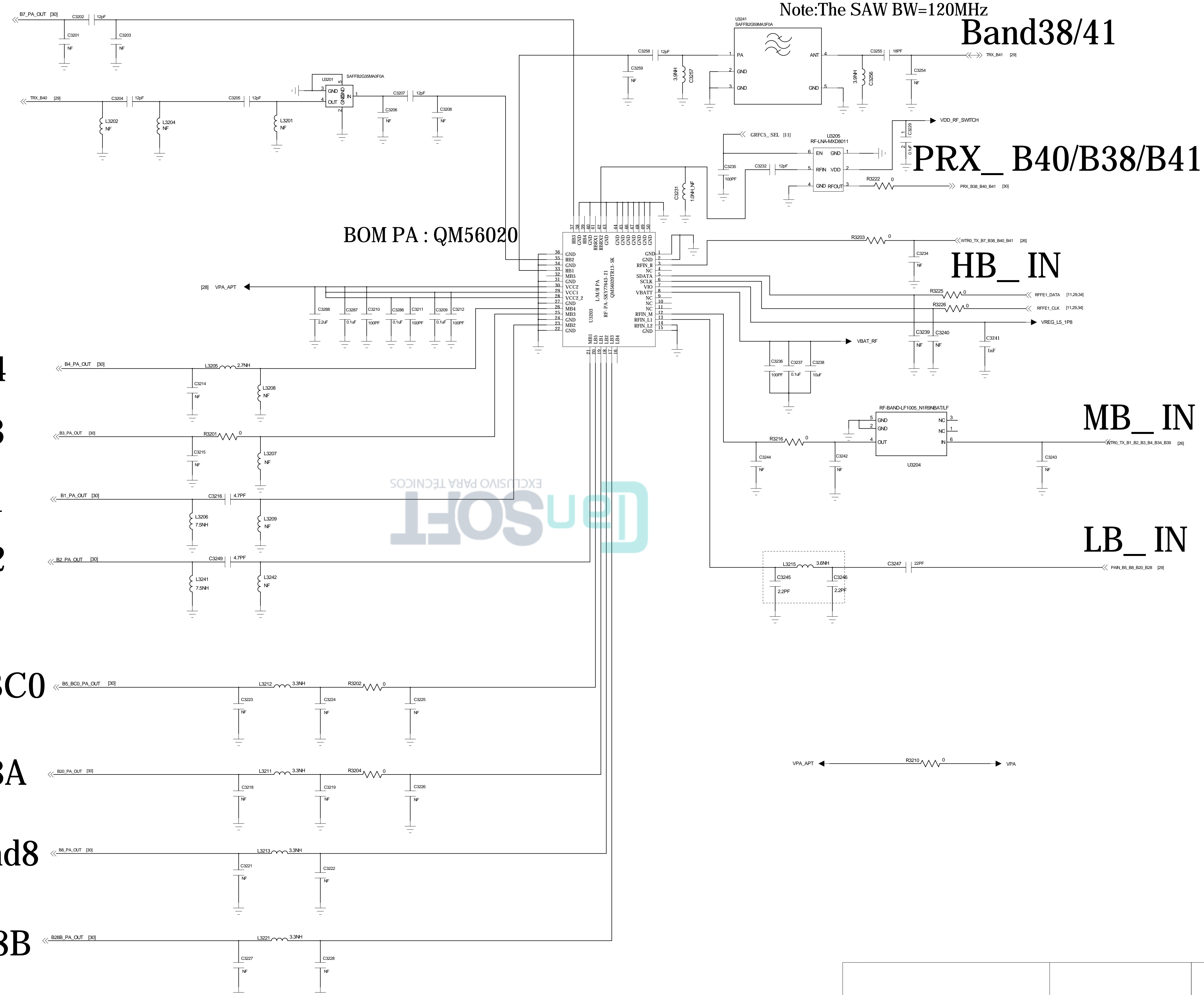
PRX\_B40/B38/B41

HB\_IN

MB\_IN

LB\_IN

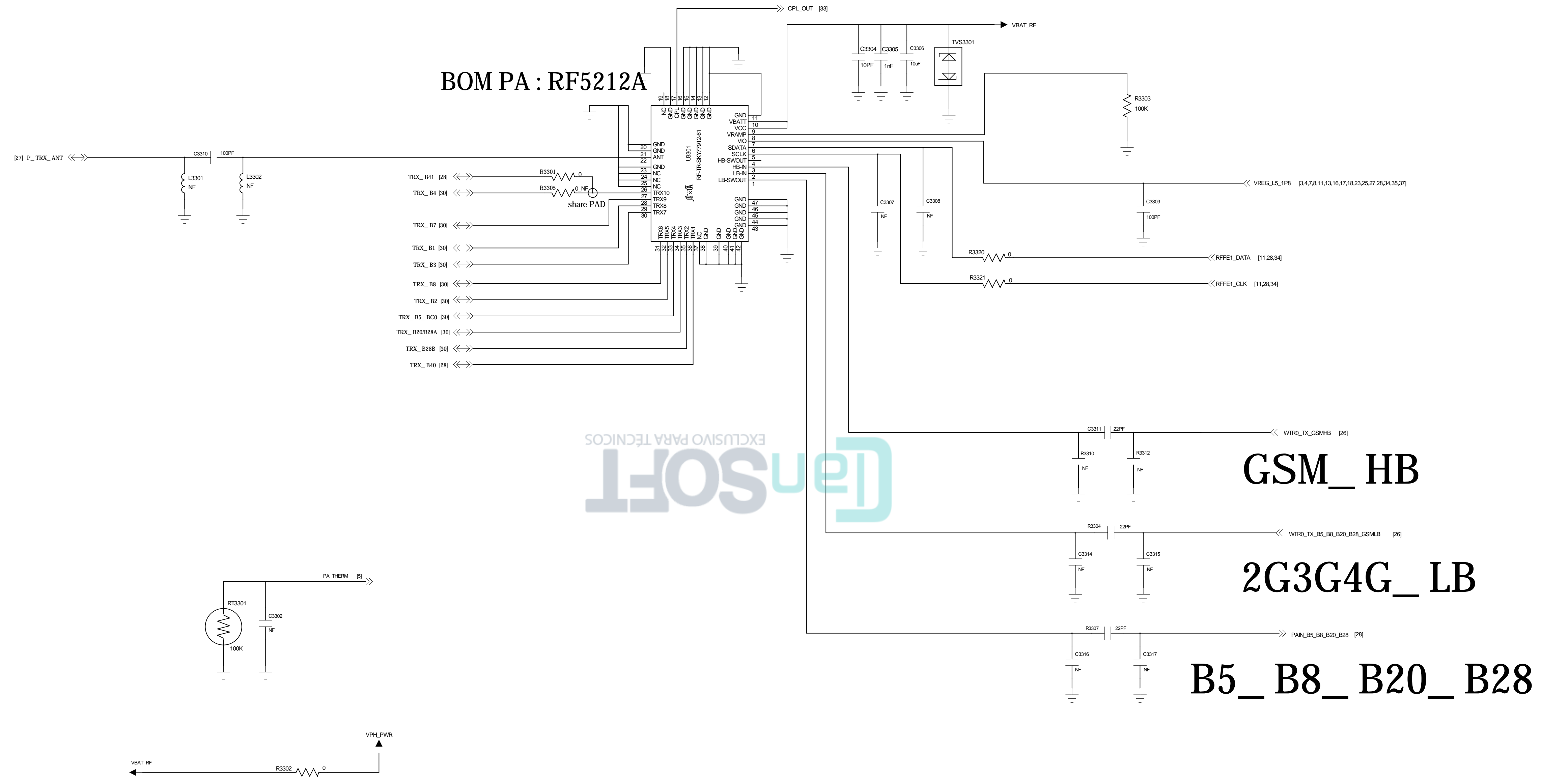
BOM PA : QM56020



Title	
Sheet	Rev
Date:	Sheet of

# 2G PA

## BOM PA : RF5212A



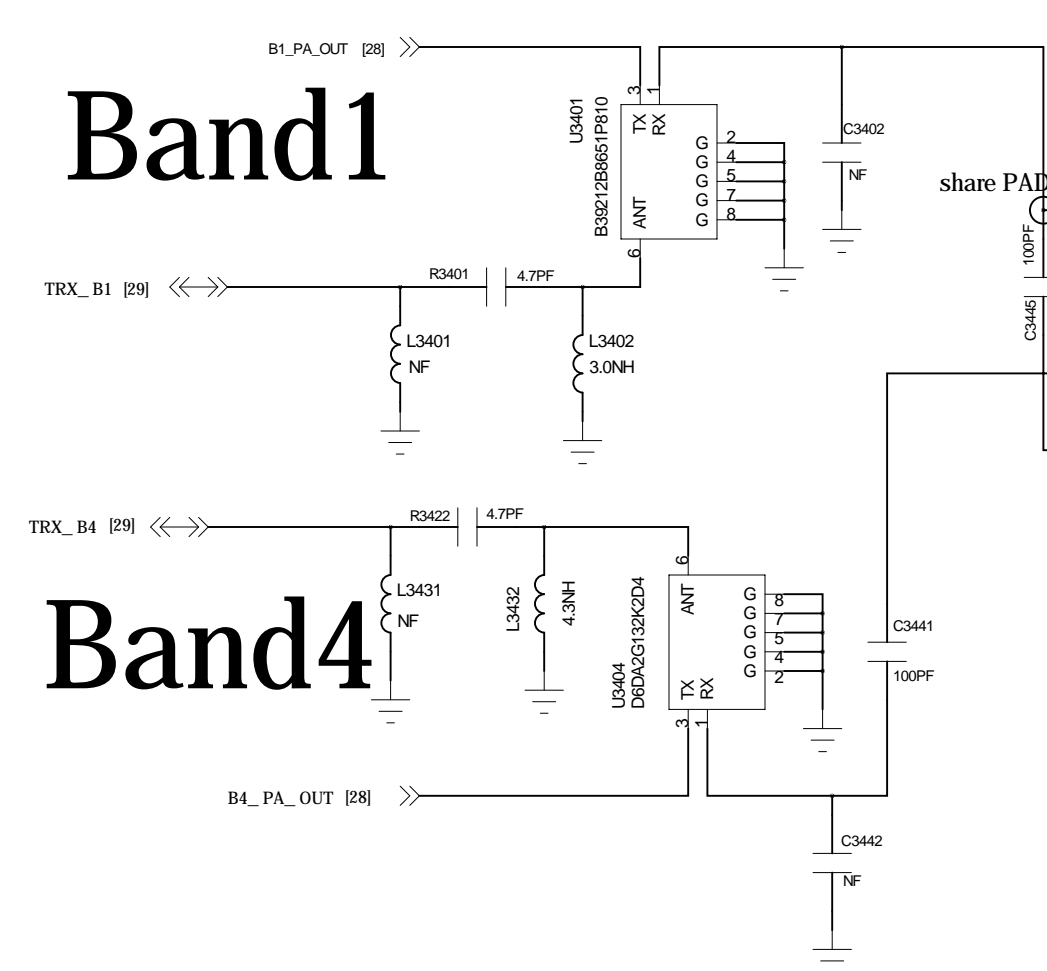
GSM\_HB

2G3G4G\_LB

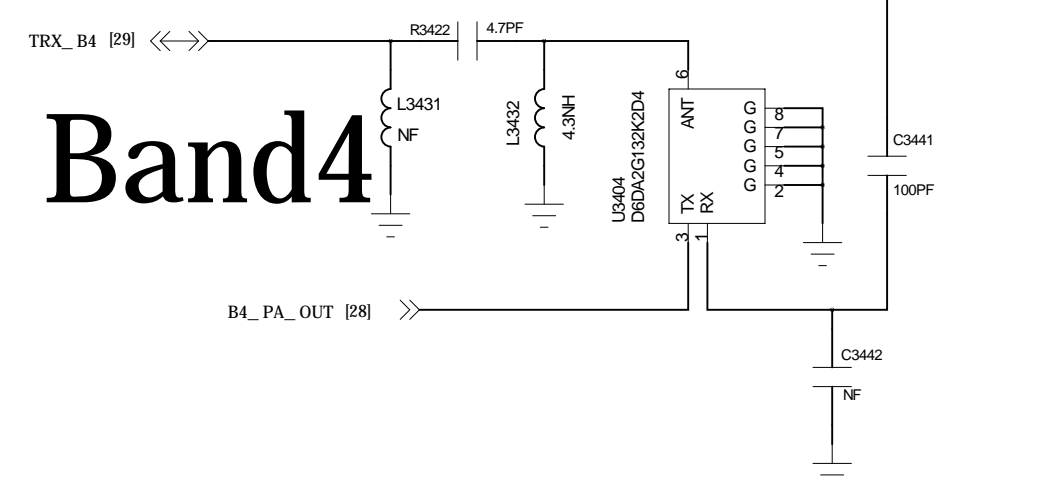
B5\_ B8\_ B20\_ B28

Title		Rev
Sheet	1	
Size	A4	
Date:		Sheet of

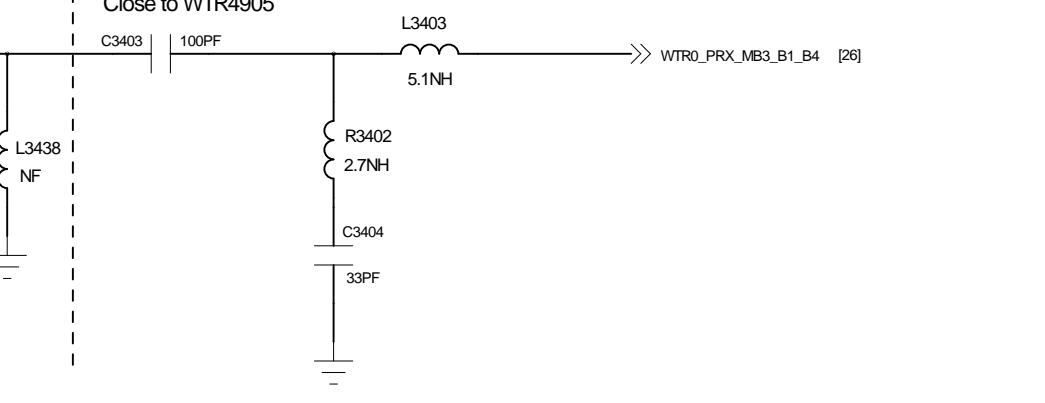
# Band1



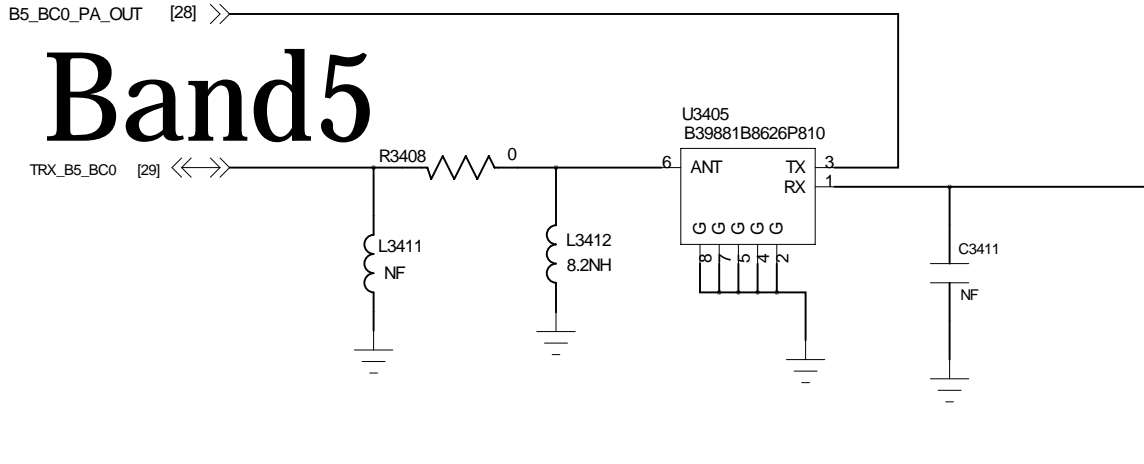
# Band4



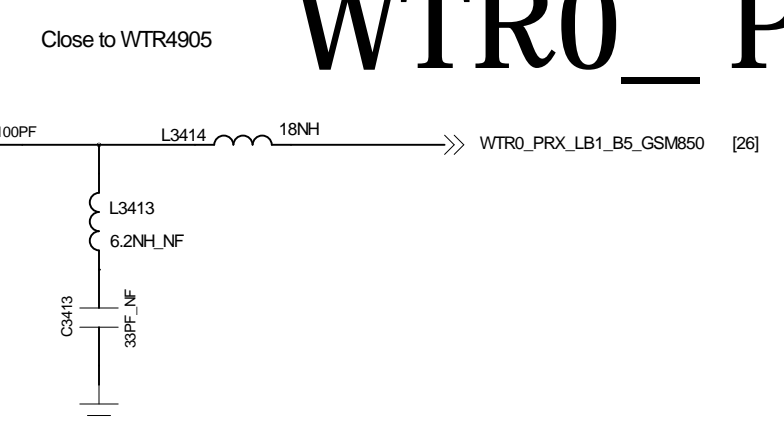
# WTR0\_PRX\_MB3



# Band5

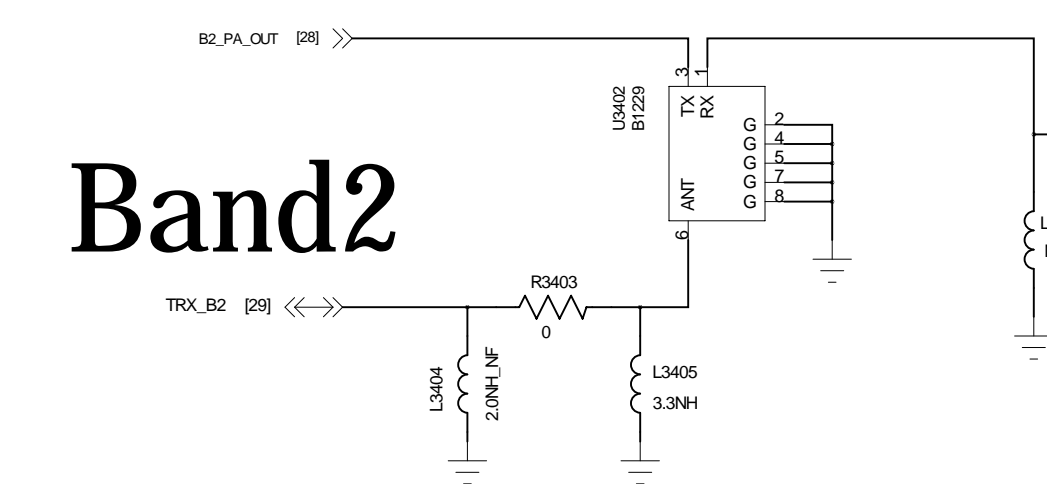


# WTR0\_PRX\_LB1

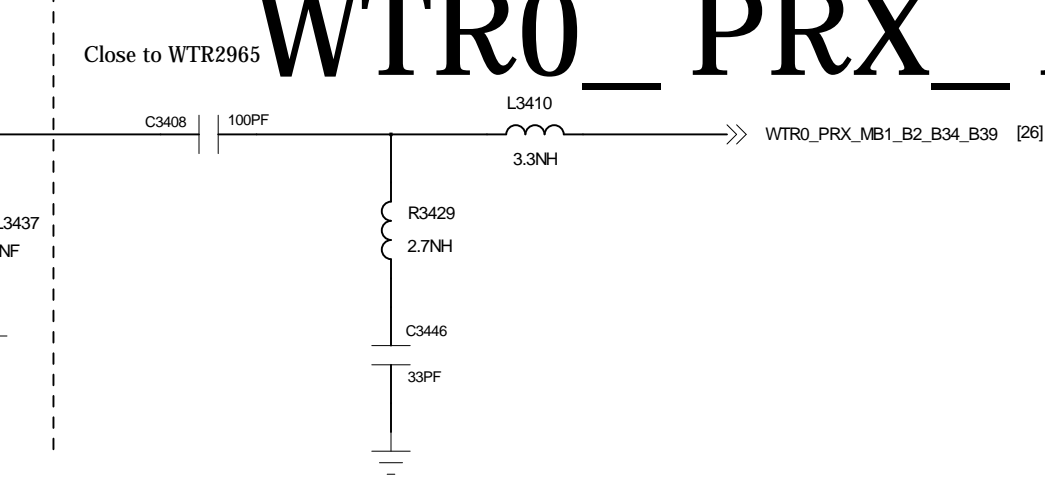


India: GSM1900 SAW 1411 Package for Co-PCB with Band2 1814 DPX

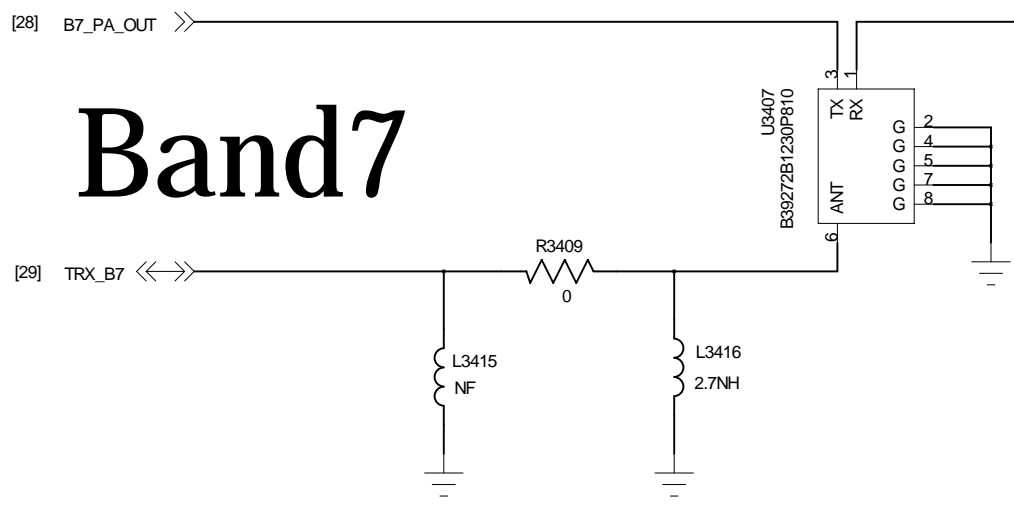
# Band2



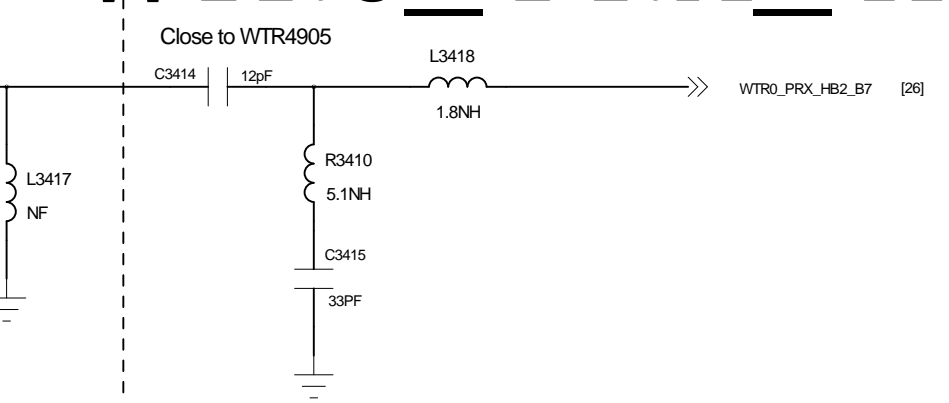
# WTR0\_PRX\_MB1



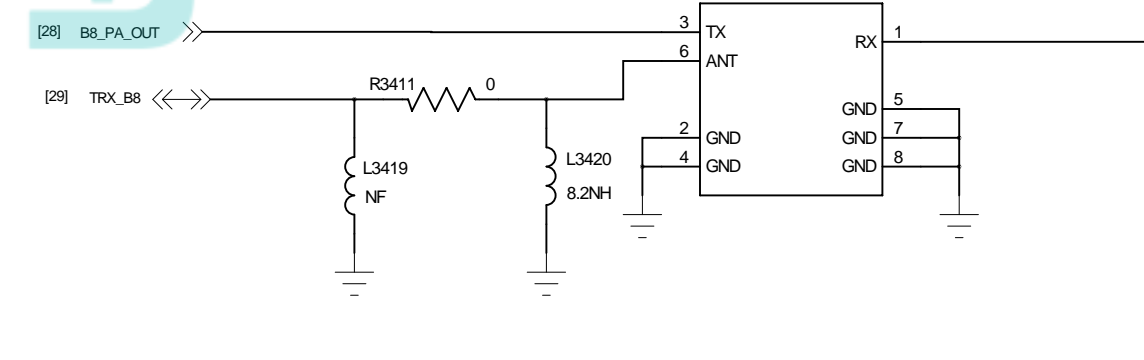
# Band7



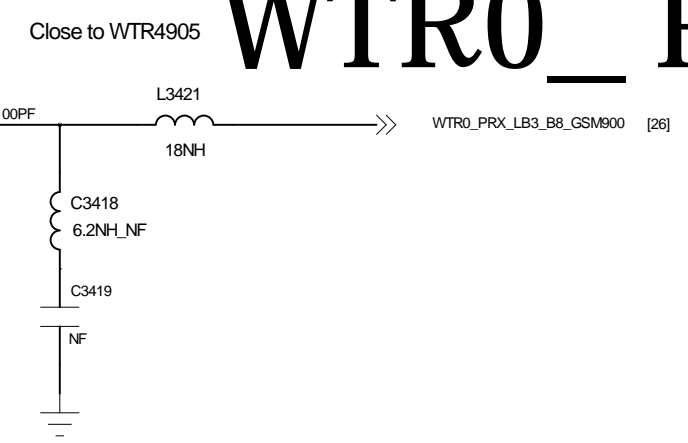
# WTR0\_PRX\_HB2



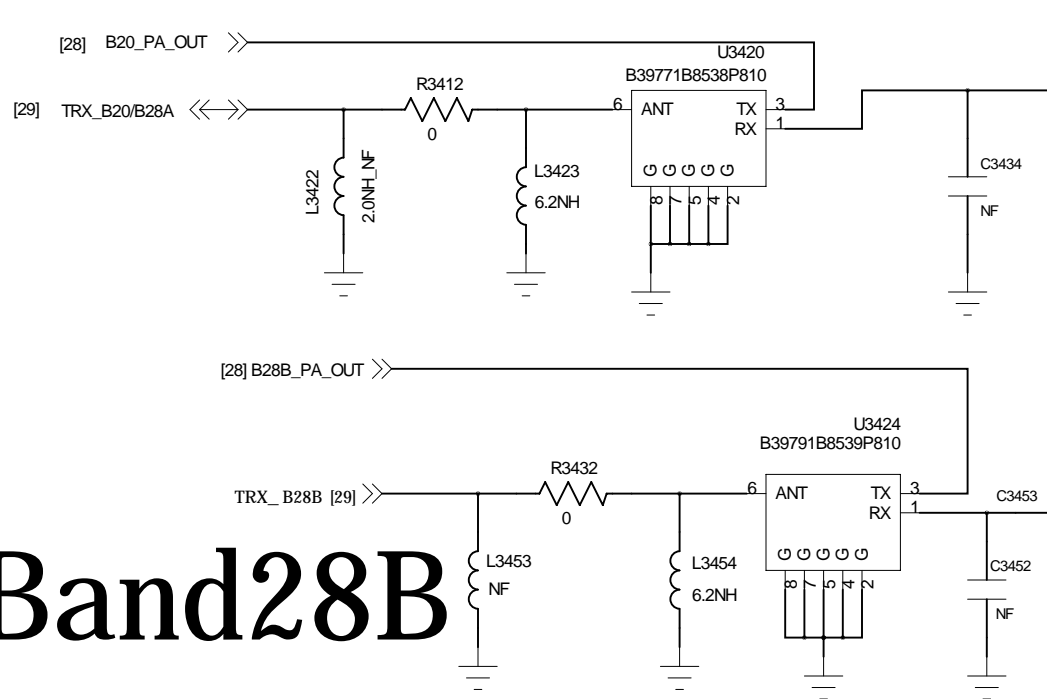
# Band8



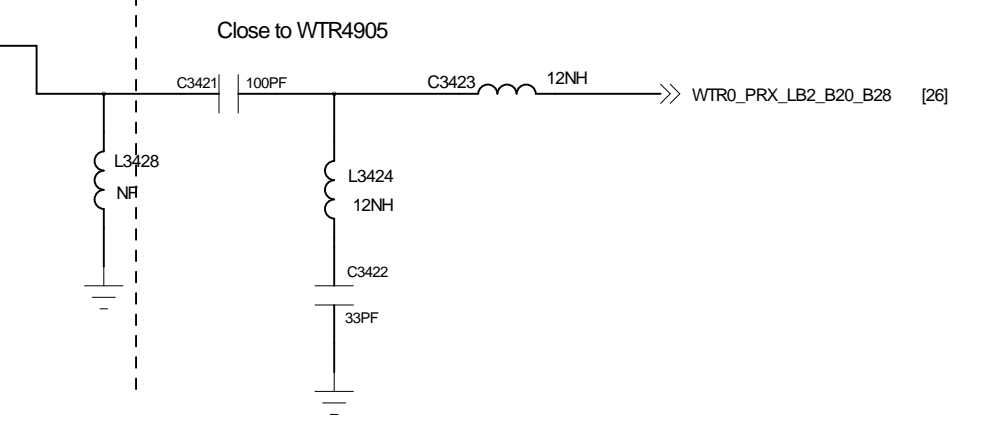
# WTR0\_PRX\_LB3



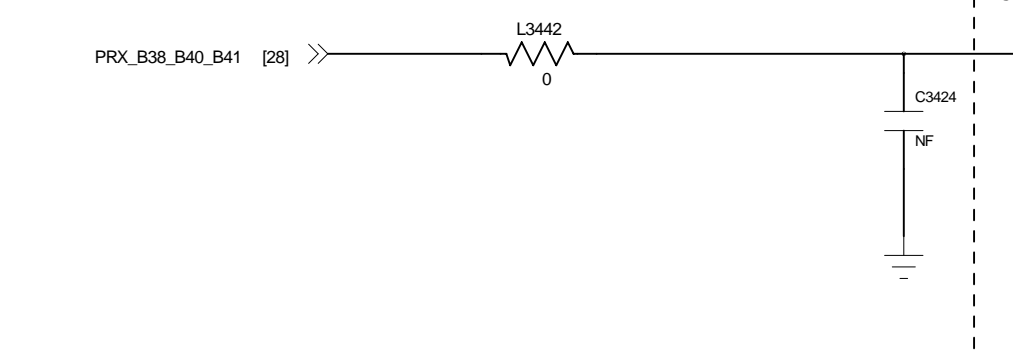
# Band20/28A



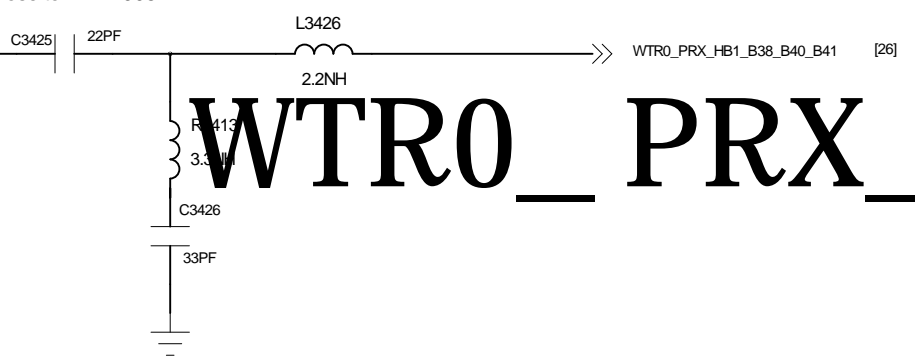
# WTR0\_PRX\_LB2



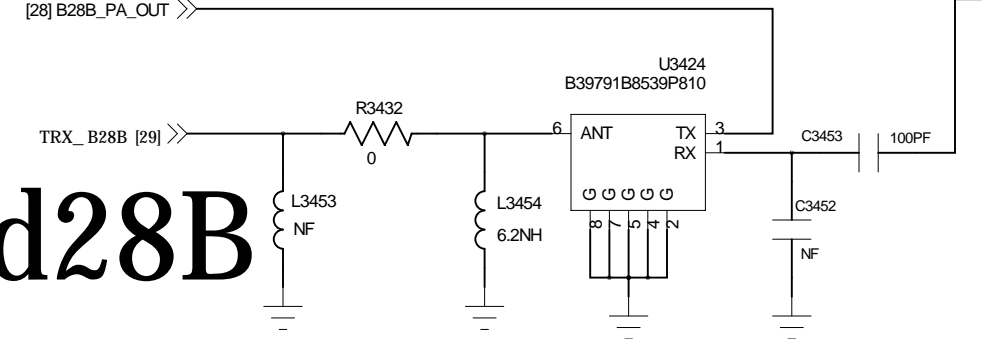
# Band40/38/41



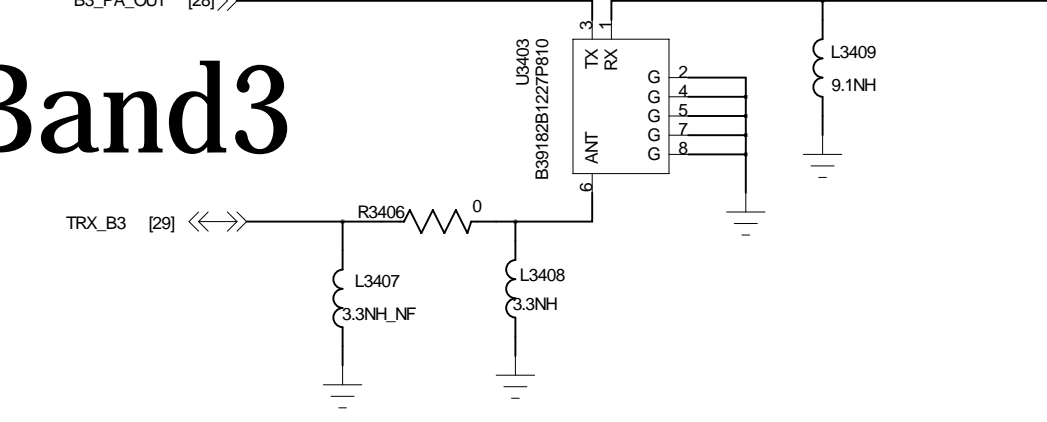
# WTR0\_PRX\_HB1



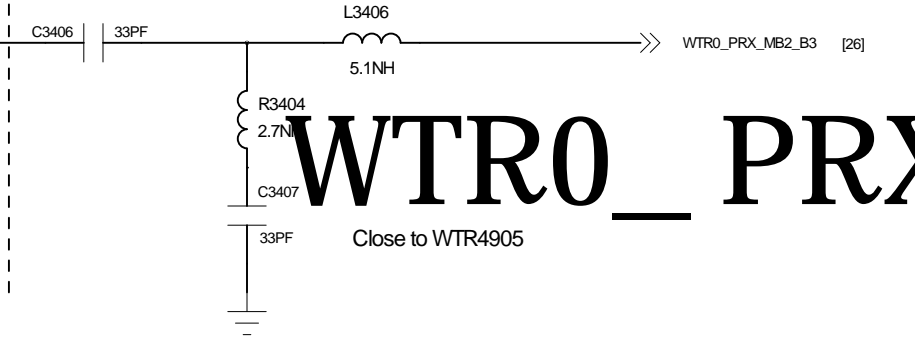
# Band28B



# Band3



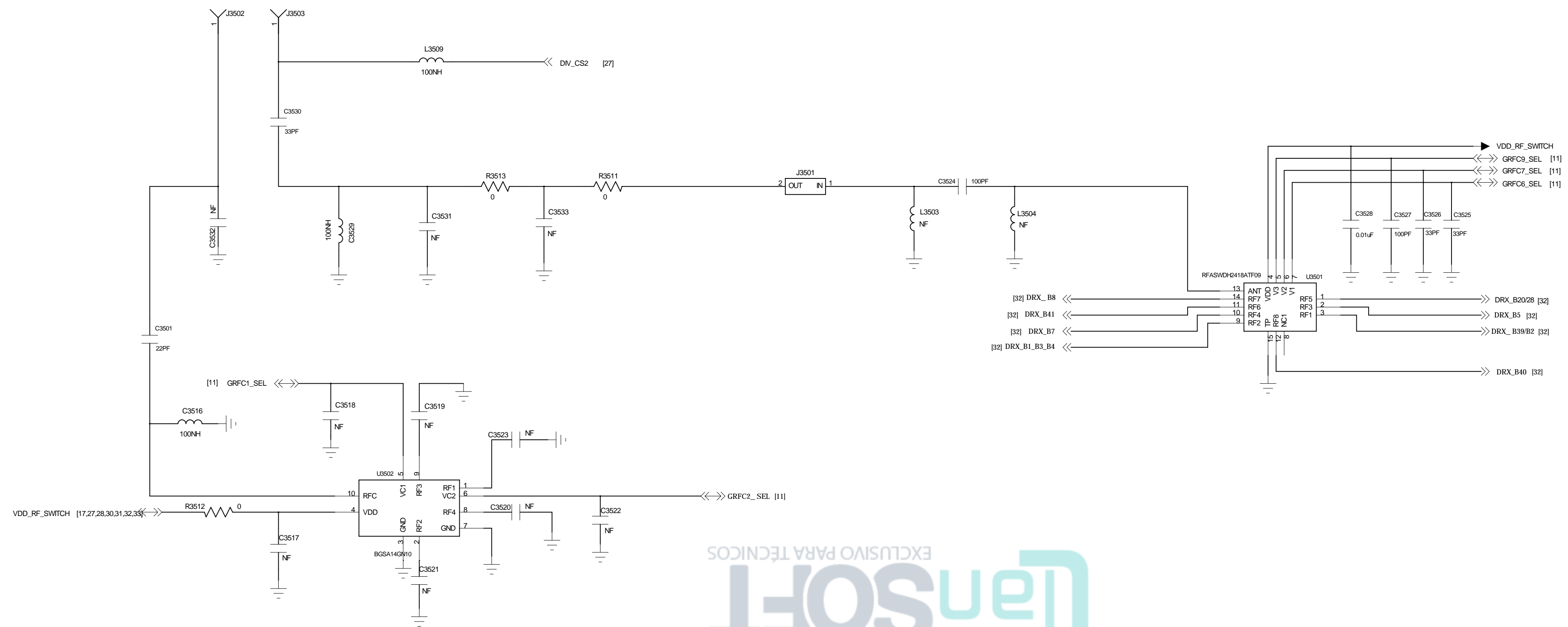
# WTR0\_PRX\_MB2



Note: The matching need close to WTR, RX ports have DC at the pin, so it need DC block,

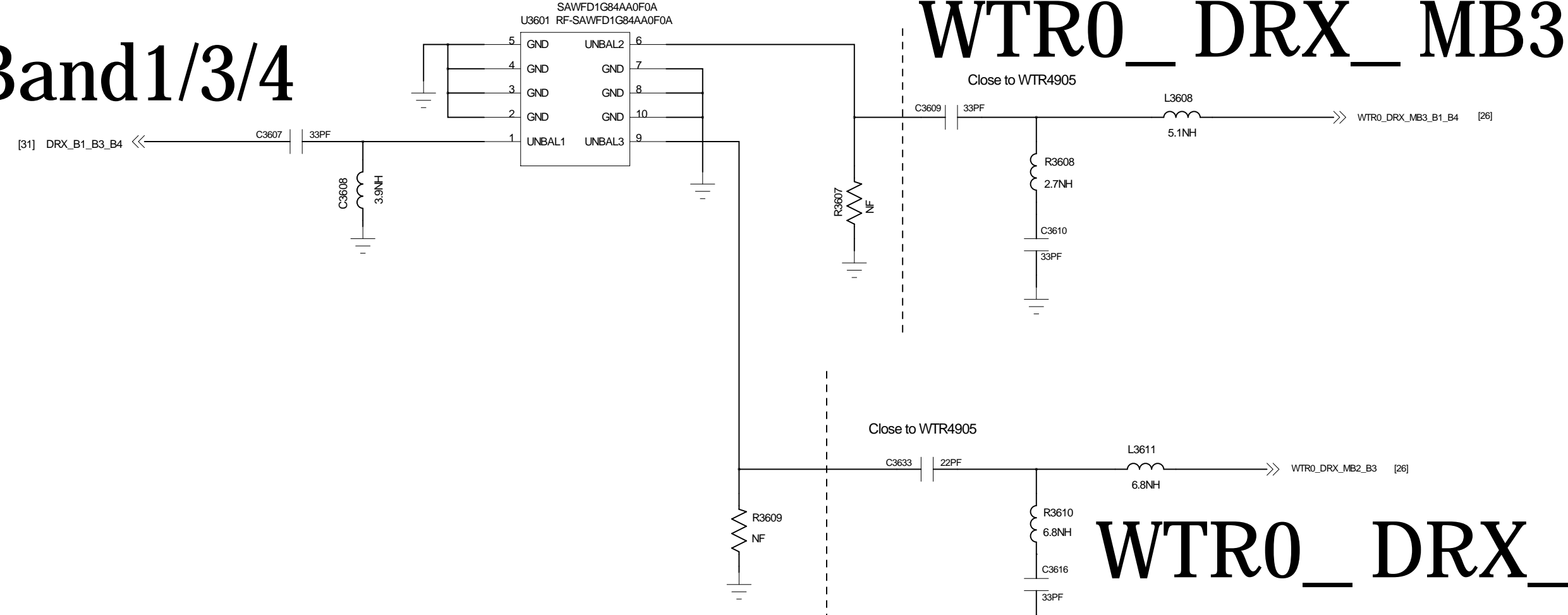
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# DRX\_ANT



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# Band1/3/4



# Band5



# Band20/B28



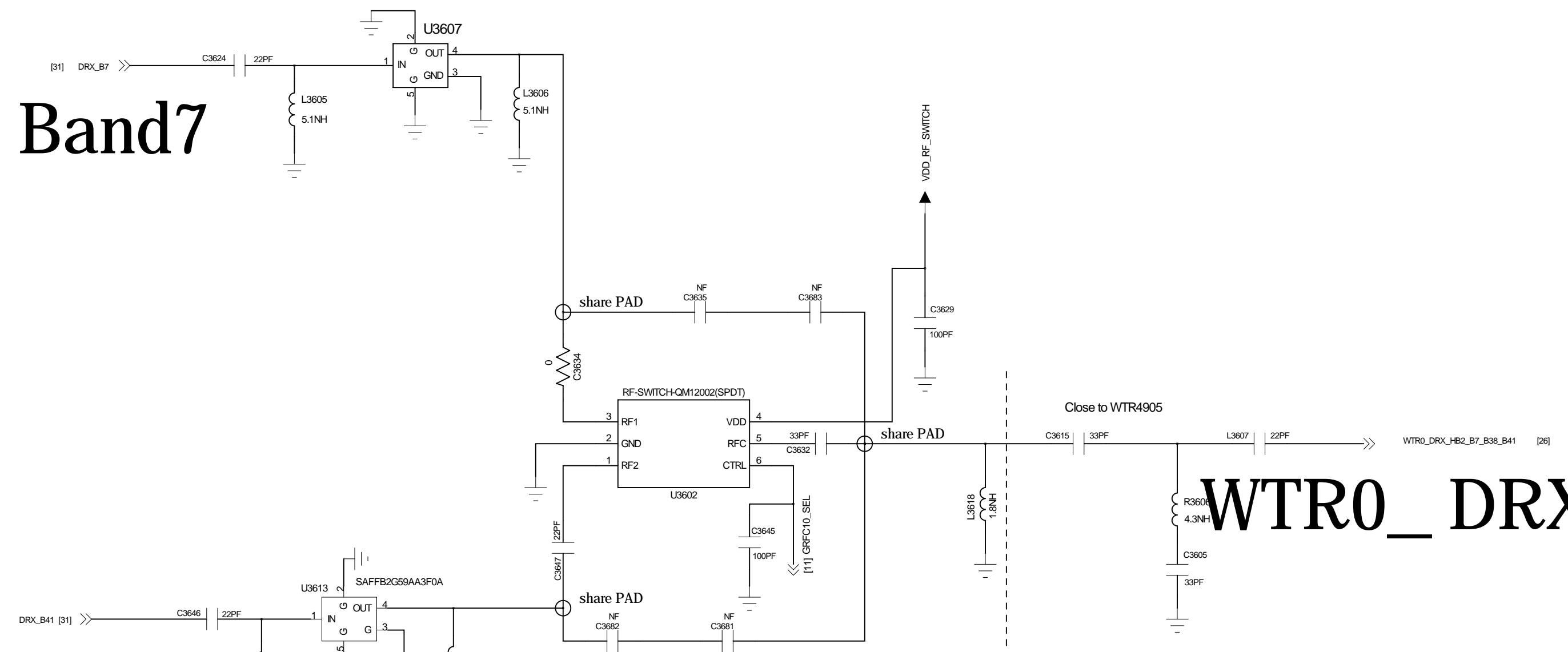
# Band8



# Band2



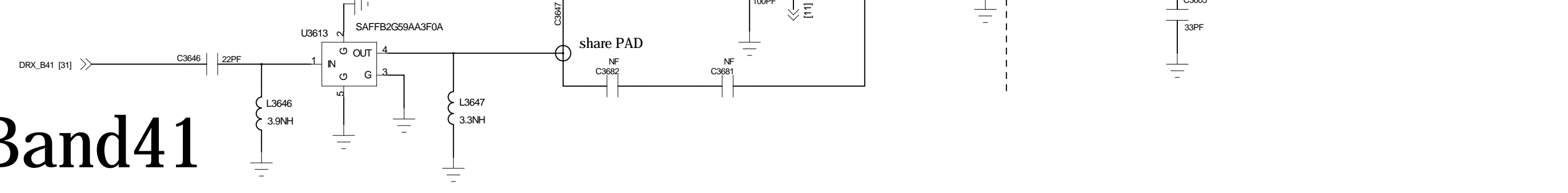
# Band7



# Band40



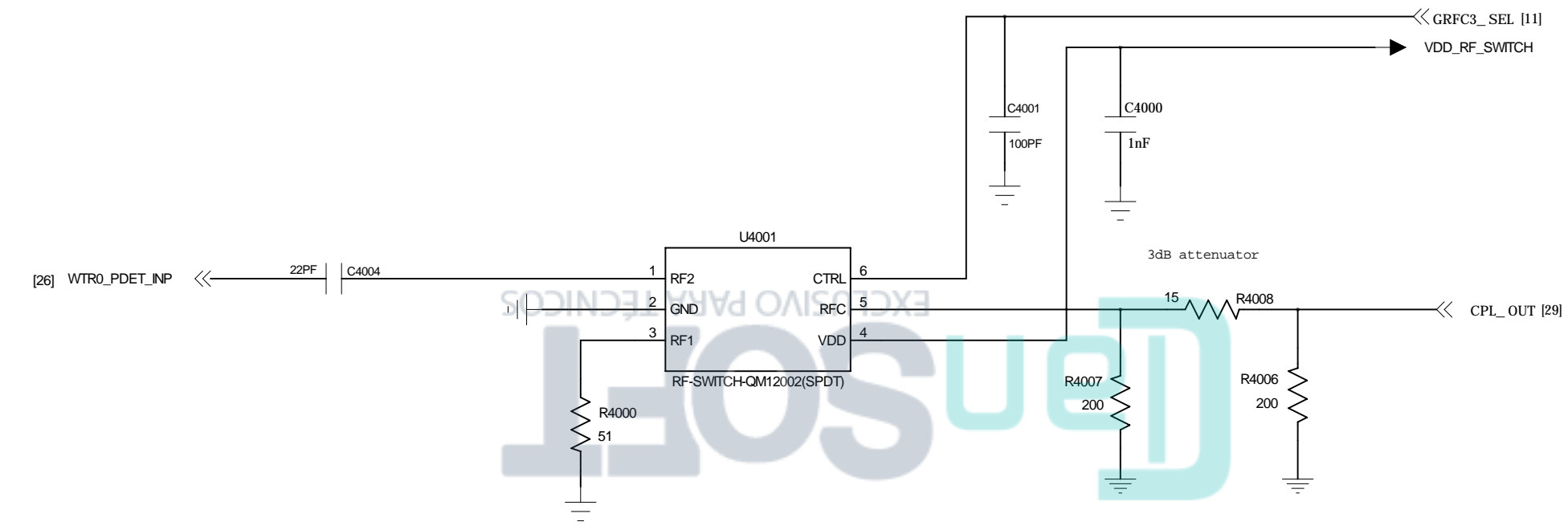
# Band41



Note: The matching need close to WTR, RX ports have DC at the pin, so it need DC block,

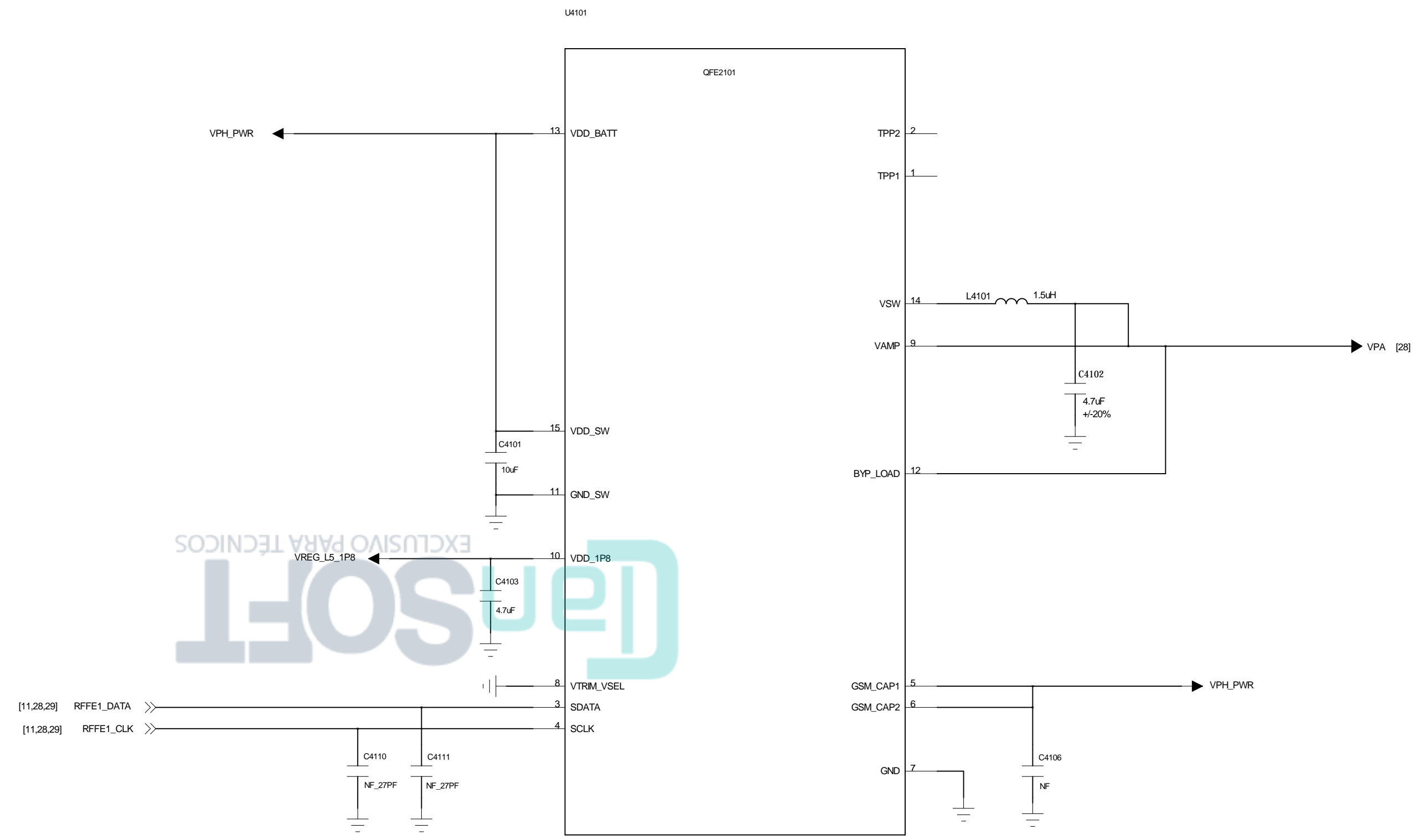
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# SPDT



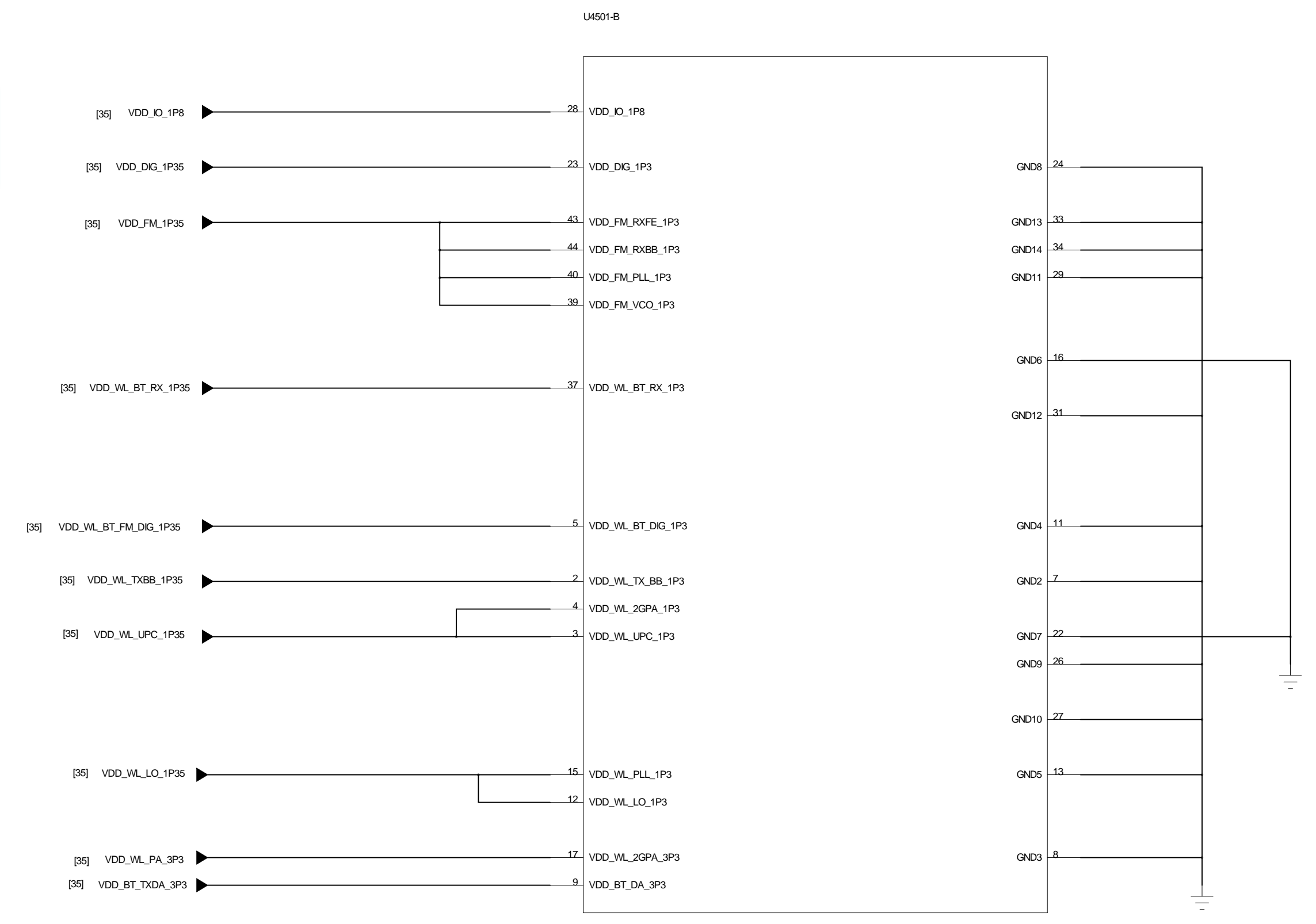
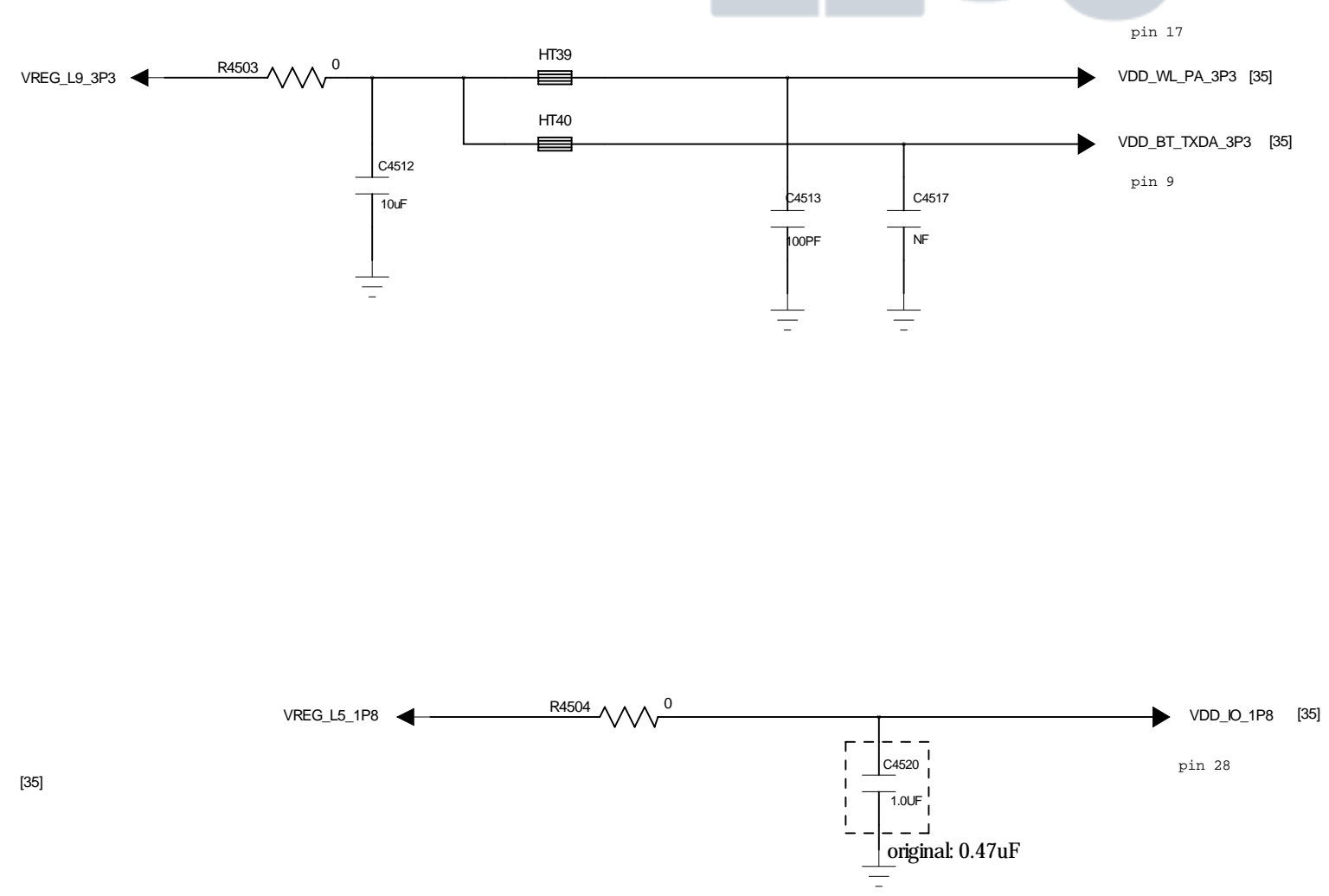
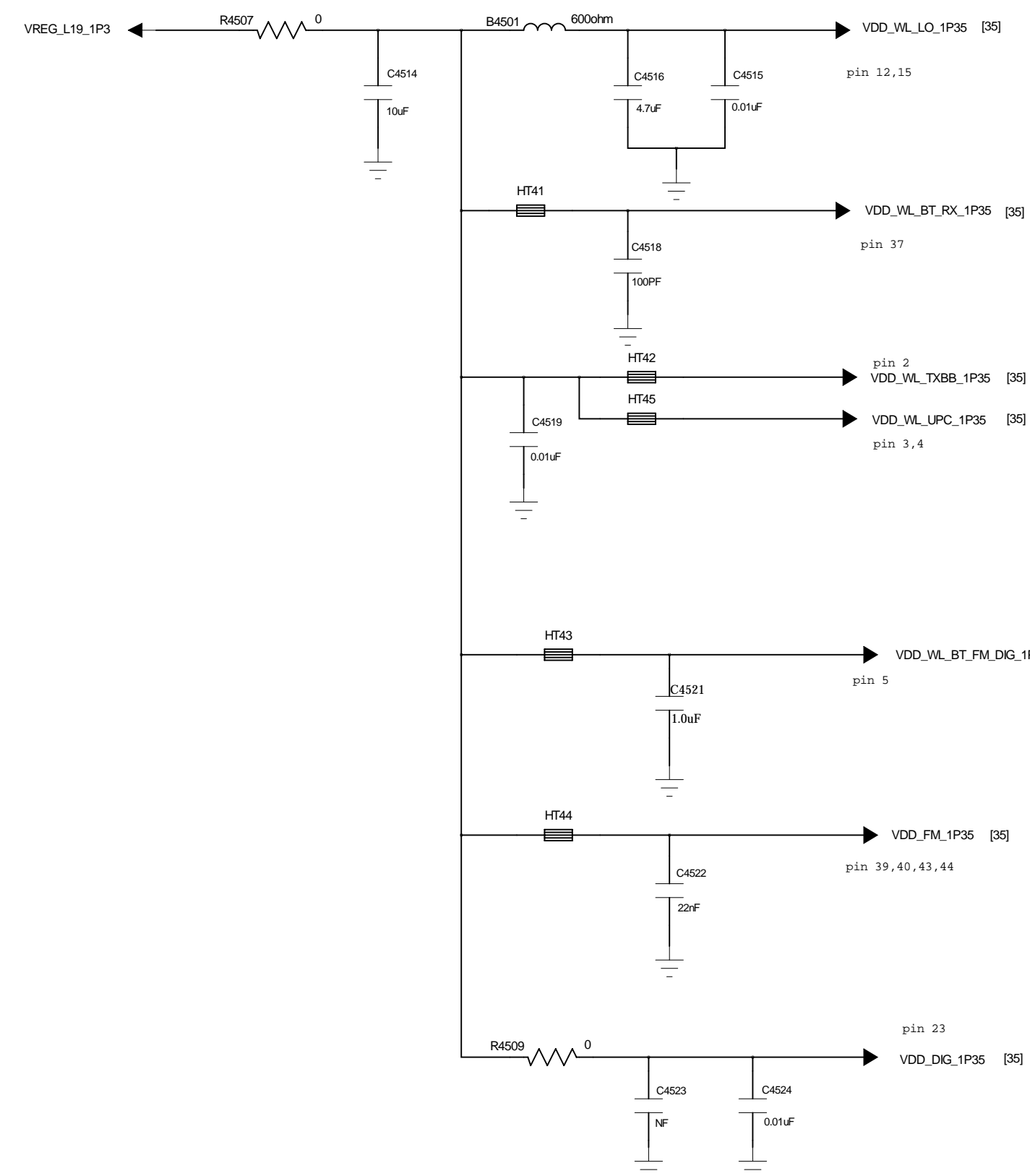
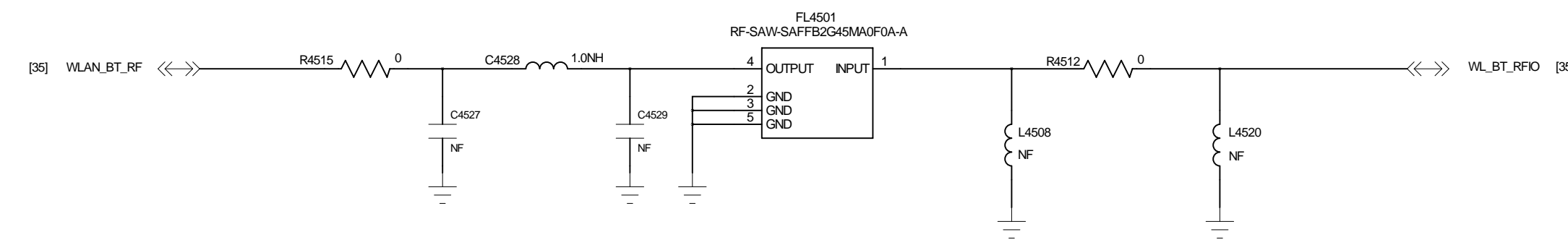
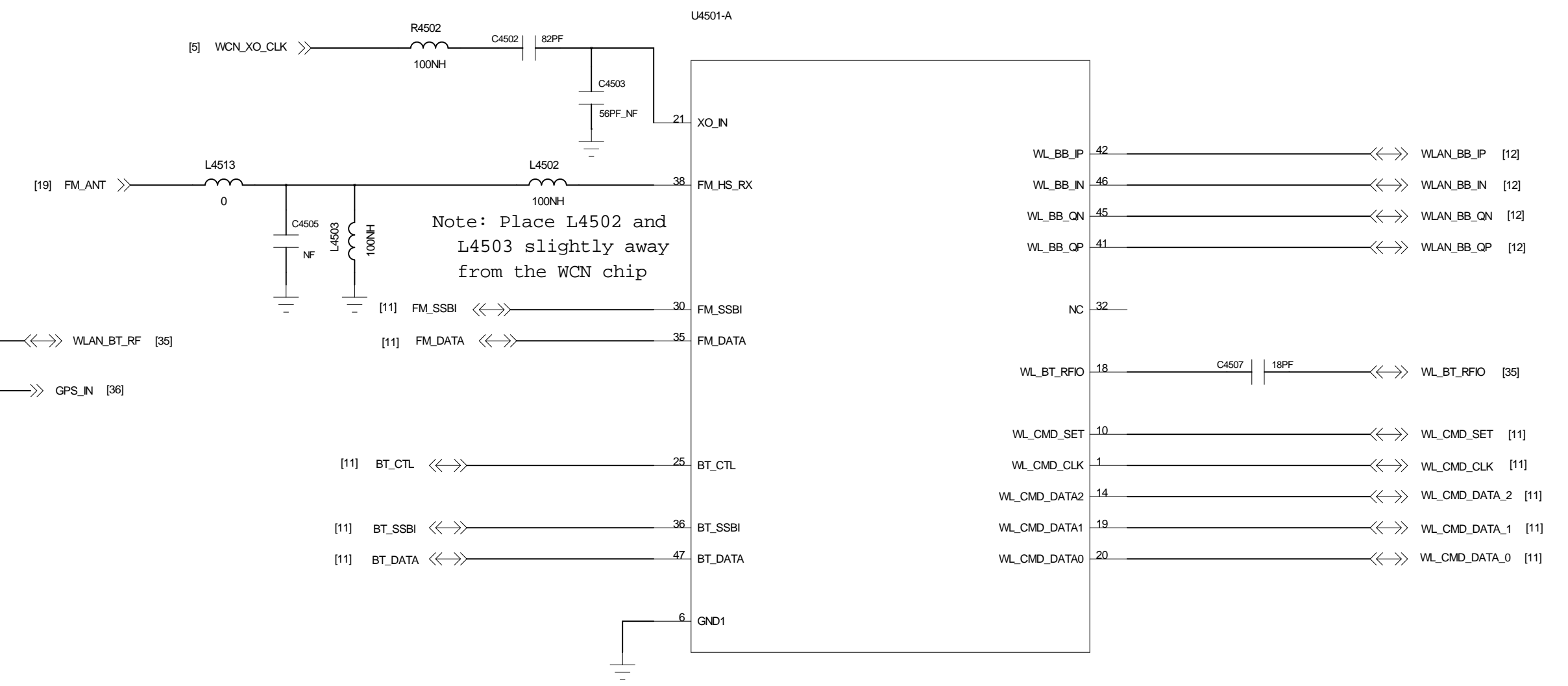
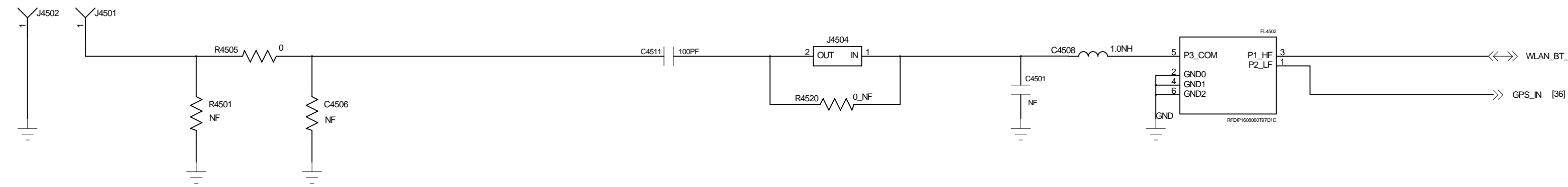
# APT

Note: Use a single low impedance power plane/fill VPA for all ET PA VCC1/VCC2.  
 Refer to 80-NA681-91 rev.B or later revisions for more layout details.

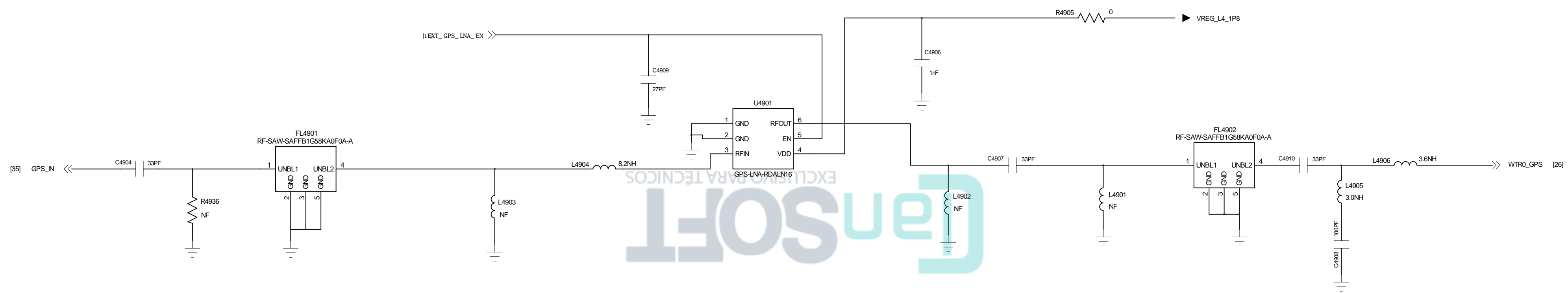




# WCN3615



# GPS



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