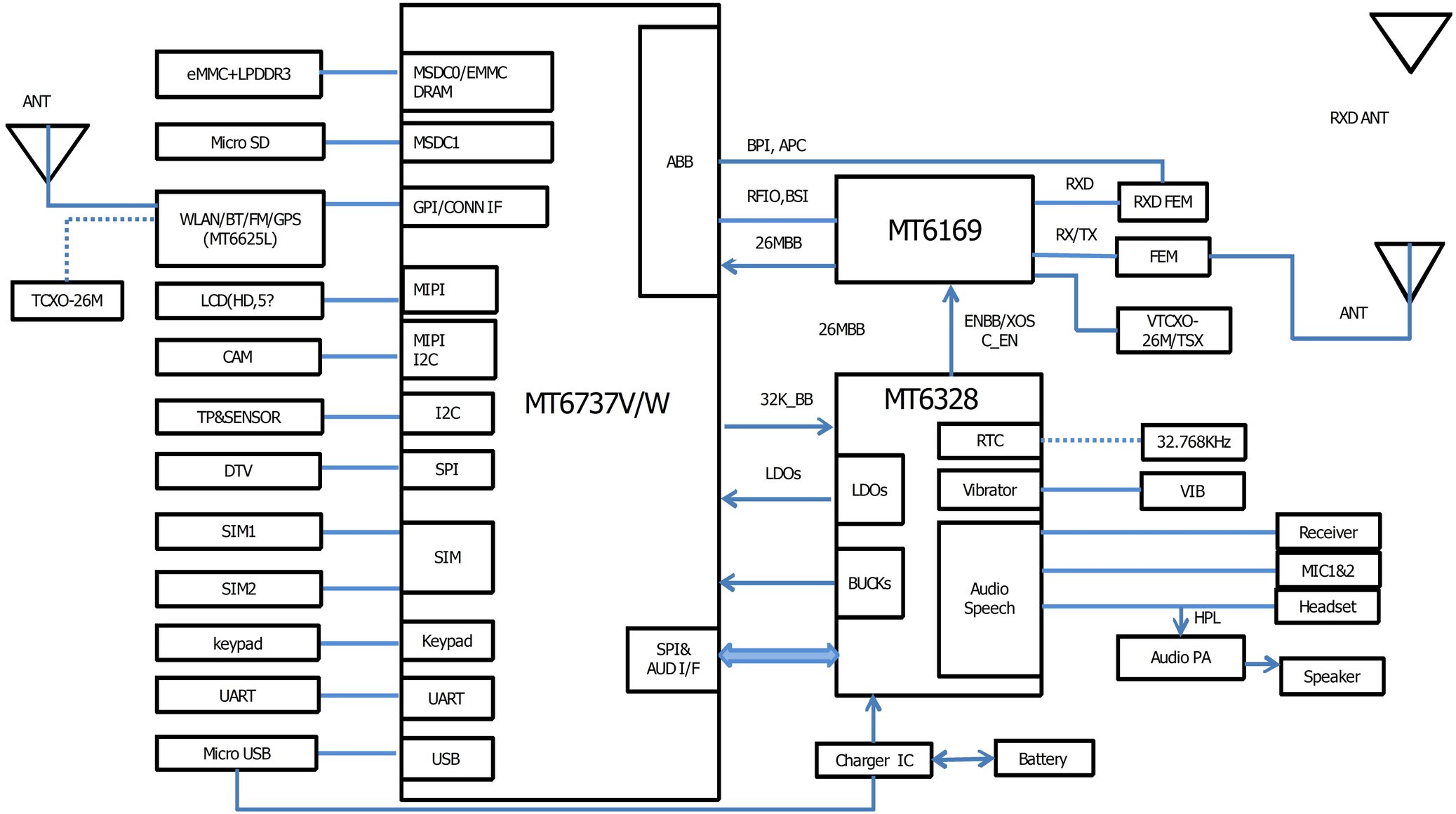

Title	01_BLOCK_DIAGRAM
Size D	Yude Confidential
Data Sep 14,2016	Sheet 11 of 99

I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	Rear Camera - 13M	400 Kbps	Yes.	Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (DW9714A) I2C address: 0x0C (Write:0x18 , Read:0x19)
	Front Camera	400 Kbps	Yes.	Front camera (GC2355) I2C address: 0x3C (Write:0x78, Read:0x79)
I2C-1	CTP	400 Kbps	Yes.	GT1151 / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
I2C-2	M Sensor	2.5 Mbps		AK09911 / M-Sensor I2C Address: 0x0D (Write:0x1A, Read:0x1B)
	Gyro Sensor	400 Kbps	Yes.	ITG1010 / Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Accelerometer	400 Kbps		MC3410 / Accelerometer I2C address: 0x4C (Write:0x98, Read:0x99)
	RGB / PS Sensor	400 Kbps		CM36652 / RGB+PS I2C address: 0X60 (Write:0xC0, Read:0xC1)
	NFC	1.2 Mbps	Yes.	MT6605 / NFC I2C address: 0X28 (Write:0x50, Read:0x51)
	Flashlight Driver	400 Kbps		LM3642 / Flashlight Driver I2C address: 0X63 (Write:0xC6, Read:0xC7)
I2C-3				

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Title	02_I2C_ID_OVERVIEW	
Size D	Yude Confidential	
Data Sep 14,2016		Sheet 11 of 99

C1014 should be 47uF
for MT6753 and MT6753T

Note: 10-1

Note: 10-1

Note: 10-1

C / 47 / uF / 0805 can be replaced
by 2pcs C / 22 / uF / 0603

C1051 close to AVDD18_MEMPLL(E1 ball) & DVDD18_MC1(F3 ball)
and keep trace length < 150mils

C1060 close to DVDD18_MC0 and keep trace length < 150mils

C1052 close to DVDD28_MC1 and keep trace length < 150mils

Schematic design notice of "10_BB_POWER" page.

Note 10-1: 4 mil GND trace with good shielding to PMIC
(Differential)

Note 10-3: FSOURCE_P(EFUSE)
(1)FSOURCE_P EFUSE power(VEFUSE) should be
only for EFUSE usage(not share with other application)
(2)W/I EFUSE program, VEFUSE need 1uF bypass cap
(pls refer to ¡§LDO output voltage/current table¡¨)
(3)W/O EFUSE program, VEFUSE bypass cap should be NC.

Title	10_BB_ POWER
Size D	Yude Confidential
Data Sep 14,2016	Sheet 10 of 99

This circuit muse be reserved

NC

[3,4,5,7,8] [11,12,13,15,16] [18,19,21,24]

VIO18_PMU

R1102 47KR 1% NC

R1112 47KR 1% NC

[5] BOARD_TYPE_ID

BOARD_TYPE_ID[4]

R1103 47KR 1% NC

R1111 47KR 1% NC

GND

MT6737-SBS

PMU_IF

[7,23] SYSRSTB — AC2 SYSRSTB

[7] WATCHDOG — U4 WATCHDOG

[7] SRCLKENA0 — V4 SRCLKENA0

[7] SRCLKENA1 — AC30 SRCLKENA1

[7] RTC32K1V8 — AC1 RTC32K_CK

[7] PWRAP_SPI0_CSN — Y6 PWRAP_SPI0_CSN

[7] PWRAP_SPI0_CK — Y3 PWRAP_SPI0_CK

[7] PWRAP_SPI0_MO — AB2 PWRAP_SPI0_MO

[7] PWRAP_SPI0_MI — AB3 PWRAP_SPI0_MI

[7] AUD_CLK_MOSI — Y1 AUD_CLK_MOSI

[7] AUD_DAT_MOSI_1 — Y2 AUD_DAT_MOSI

[7] AUD_DAT_MISO_1 — W3 AUD_DAT_MISO

AA2 PWRAP_INT

PLLS Test Pin

REXT0 — F2 EXTR0 — R1101 36R 1% need 1% — GND

VREF — F16 — EVREF [4,16]

JTAG

AJ31 JTMS

AJ30 JTCK

AJ29 JTDI

AK29 JTDO

Misc

AK36 TESTMODE — GND

NC

A1 A2 A30 A31 B1 B2 B31 C1 C2 C30 C31 D1 D2 D30 D31 NC

U1601_A

MT6737_12.6X12.6

MT6737V/W

DRAM_IF

DVDD12_EMI [3,16]

R1105 8.06K 1%

C1101 0.1uF

[4,16] EVREF

R1106 8.06K 1%

C1102 0.1uF

C1103 1uF

GND

R1109: 47K,Ext. Buck for LTE VSRAM: Enable

R1109: NC, Ext. Buck for LTE VSRAM: Disable

[3,4,5,7,8] [11,12,13,15,16] [18,19,21,24]

VIO18_PMU — 470K — VLTE_SRAM_EN — ADC_PA [4]

GND — 47KR — R1110

[19] LCD_ID0

MT6737-SBS

SIM

[15] SIM1_SCLK — K3 SIM1_SCLK

[15] SIM1_SIO — J3 SIM1_SIO

[15] SIM1_SRST — J4 SIM1_SRST

[15] SIM2_SCLK — L6 SIM2_SCLK

[15] SIM2_SIO — K5 SIM2_SIO

[15] SIM2_SRST — K4 SIM2_SRST

BPI-L/C

[14] BPI_BUS20 — AK28 BPI_BUS20

[14] BPI_BUS19 — AH12 BPI_BUS19

[14] BPI_BUS18 — AK27 BPI_BUS18

[4] BOARD_TYPE_ID — AL27 BPI_BUS17

[14] BPI_BUS16 — AF27 BPI_BUS16

AG28 BPI_BUS15

AF28 BPI_BUS14

AG27 BPI_BUS13

AF27 BPI_BUS12

[14] BPI_BUS11 — AH28 BPI_BUS11

[14] BPI_BUS10 — AK26 BPI_BUS10

[13] BPI_BUS9 — AG26 BPI_BUS9

AH26 BPI_BUS8

[13] BPI_BUS7 — AJ26 BPI_BUS7

[13] BPI_BUS6 — AK25 BPI_BUS6

AL25 BPI_BUS5

RFI_C

[11] LTE_RFIC0_BSI_EN — AG17 RFIC0_BSI_EN

[11] LTE_RFIC0_BSI_CK — AG16 RFIC0_BSI_CK

[11] LTE_RFIC0_BSI_D2 — AK16 RFIC0_BSI_D2

[11] LTE_RFIC0_BSI_D1 — AL17 RFIC0_BSI_D1

[11] LTE_RFIC0_BSI_D0 — AK17 RFIC0_BSI_D0

AG15 C2K_TXBPI

AH16 RFIC1_BSI_EN

AJ16 RFIC1_BSI_CK

AL16 RFIC1_BSI_D0

AK15 RFIC1_TX_BSI_EN

AK14 RFIC1_TX_BSI_CK

AJ14 RFIC1_TX_BSI_D0

BPI - L

[11] LTE_TXBPI — AH5 LTE_TXBPI

AD3 BPI_BUS27

AG3 BPI_BUS26

AG2 BPI_BUS25

AE3 BPI_BUS24

[8] CHG_STAT — AF3 BPI_BUS23

[22] GPIO_AUSPDTEN — AG1 BPI_BUS22

AE4 BPI_BUS21

[19] BPI_BUS4 — AF1 BPI_BUS4

[19] BPI_BUS3 — AE2 BPI_BUS3

[19] BPI_BUS2 — AG4 BPI_BUS2

[22] GPIO120_APANT — AE1 BPI_BUS1

[9] LCM_BIAS_EN — AH4 BPI_BUS0

U1601_B

MT6737_12.6X12.6

MT6737V/W

ABB_IF

C2KX26M_IN — AF13

C2K_TX_BBIP — AK14

C2K_TX_BBIN — AK13

C2K_TX_BBQP — AL12

C2K_TX_BBQN — AK12

C2K_RX1_BBIP — AH13

C2K_RX1_BBIN — AH13

C2K_RX1_BBQP — AG13

C2K_RX1_BBQN — AG14

C2K_RX2_BBIP — AL15

C2K_RX2_BBIN — AL14

C2K_RX2_BBQP — AH14

C2K_RX2_BBQN — AH14

APC1 — AH10 — APC1 [13]

APC2 — AJ10

LTEX26M_IN — AE10 — LTE_LTEX26M_IN [11]

LTE_TX_BBIP — AK2 — RF_TX_BBIP [11]

LTE_TX_BBIN — AK3 — RF_TX_BBIN [11]

LTE_TX_BBQP — AL3 — RF_TX_BBQP [11]

LTE_TX_BBQN — AL4 — RF_TX_BBQN [11]

LTE_RX1_BBIP — AH7 — RF_RX1_BBIP [11]

LTE_RX1_BBIN — AH7 — RF_RX1_BBIN [11]

LTE_RX1_BBQP — AK6 — RF_RX1_BBQP [11]

LTE_RX1_BBQN — AK6 — RF_RX1_BBQN [11]

LTE_RX2_BBIP — AK7 — RF_RX2_BBIP [11]

LTE_RX2_BBIN — AK8 — RF_RX2_BBIN [11]

LTE_RX2_BBQP — AJ8 — RF_RX2_BBQP [11]

LTE_RX2_BBQN — AH8 — RF_RX2_BBQN [11]

RFIC_ET_EN — AH5

RFIC_ET_CK — AH4

MISC BSI

RFIC_MIPI0_SCLK — AC2 — MIPI0_SCLK [12]

RFIC_MIPI0_SDATA — AC5 — MIPI0_SDATA [12]

RFIC_MIPI1_SCLK — AC3 — MIPI1_SCLK [13]

RFIC_MIPI1_SDATA — AC4 — MIPI1_SDATA [13]

LTE_PAVM — AD4

LTE_PAVP — AC4

AUX IN

ADC_PA [4]

C1108 100PF — GND

AUXIN_AH11 — AH11 — AUX_IN1_NTC [12]

AUXIN_AG12 — AG12

AUXIN_AG11 — AG11 — AUX_IN0_NTC [21]

C1104 0.1uF

C1106 0.1uF — GND — C1105/C1106 close to BB

REF POWER

REFP — AL10 REFP

AVSS_REF — AK10

C1107 0.01uF — GND — Close to AP IC.

VIO18_PMU [3,4,5,7,8,11,12,13,15,16,18,19,21,24]

R1104

ADC_PA [4]

R1107

GND

Title	11_BB_1	
Size D	Yude Confidential	
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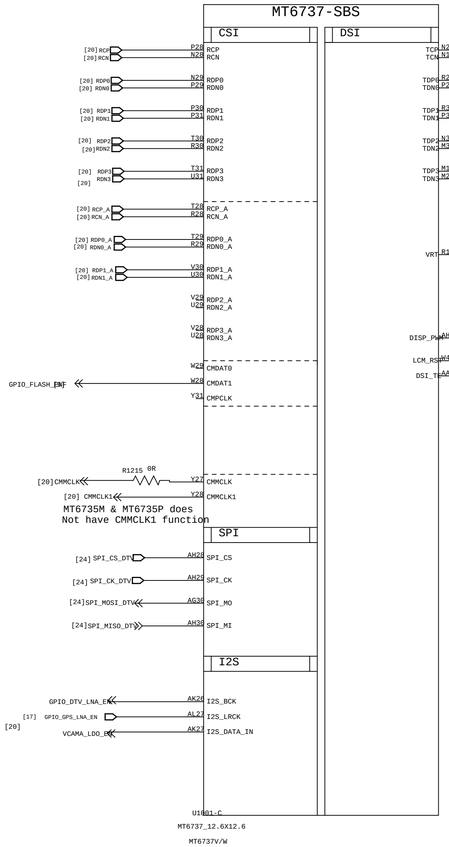
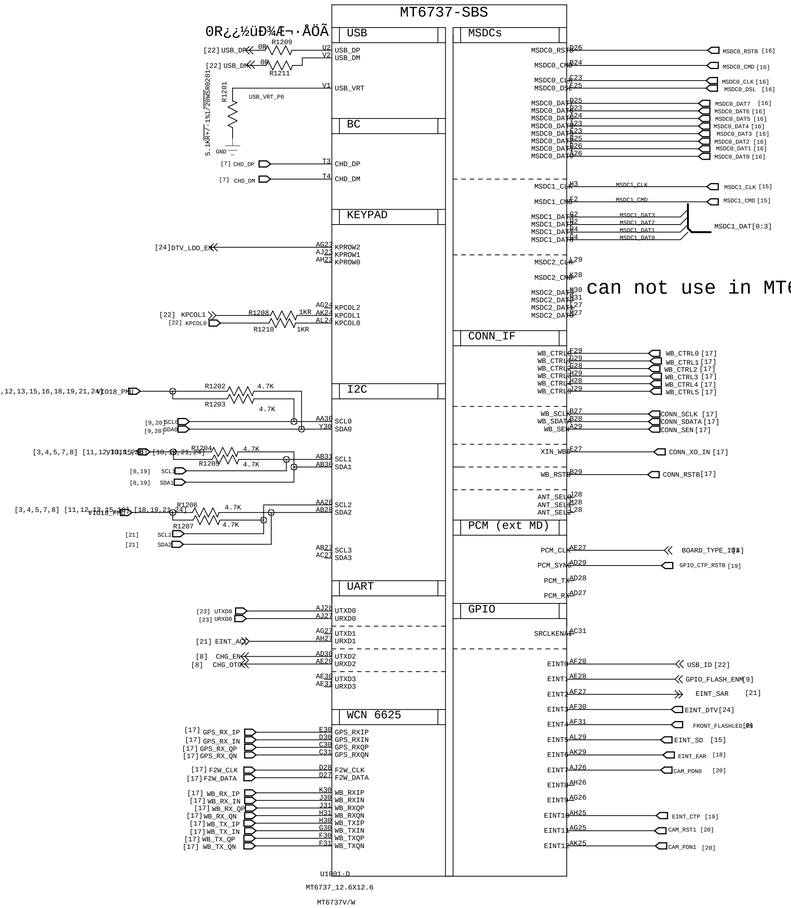




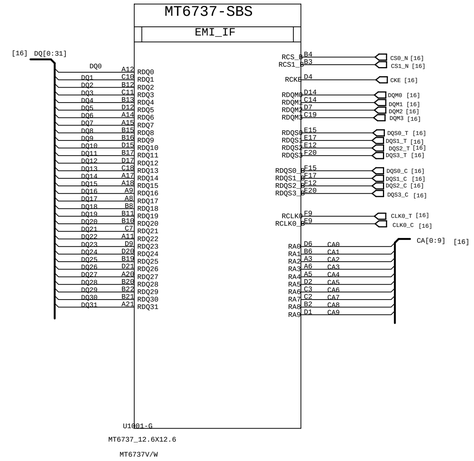
Schematic design notice of "12_BB_2" page.

Note 12-1:MSDC2 Pin should be NC (No Connection) for MT6735M

Note 12-2: MT6735M does Not have CMMCLK1 function

Please refer to MT6735M Design Notice for details

Title	12_BB_2	
Size D	Yude Confidential	
Data Sep 14,2016	Sheet 11 of 99	



Title	13_BB_3	
Size D	Yude Confidential	
Data Sep 14,2016		Sheet 11 of 99

Audio

1. VBAT_Buck input cap should connect to its individual GND first, then go to main GND.
2. Buck controller power trace (AVDD45_SMPS) must use single trace connected to system (battery) power directly, and can¡t merge with others.
3. Please refer to latest MMD design

Add Zenar Diode
Place on the path
from VBAT to IC
(Battery connector
or test point or IO
connector)

500mW
VF : 4.85V~5.36V
Between IC and IO port

Please refer to latest MMD design

UVLO_VTH R RANGE:
200KOHM ~ 250KOHM

Close to MT6328

C2040 close to AVDD22_LDO1/2/3/4 balls

Close to MT6328

Please refer to latest MMD design

Close to PMIC

VCDT rating: 1.268V

Close to MT6328

32k less , C2034 0R.

C2027/ C2038/ C2058 flying cap & holding cap :
4.7uF for 16ohm reciver
2.2uF for 32ohm reciver

single via to GND plane directly

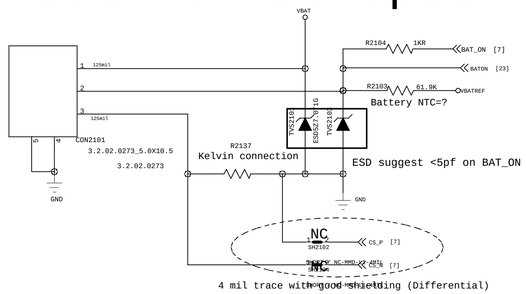
To improve noise level, connect to audio jack first, and then connect to GND R2000 placed near PMU

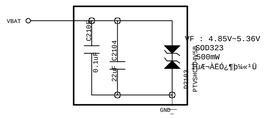
Title	20_POWER_MT6328
Size D	Yude Confidential
Data Sep 14,2016	Sheet 20 of 99

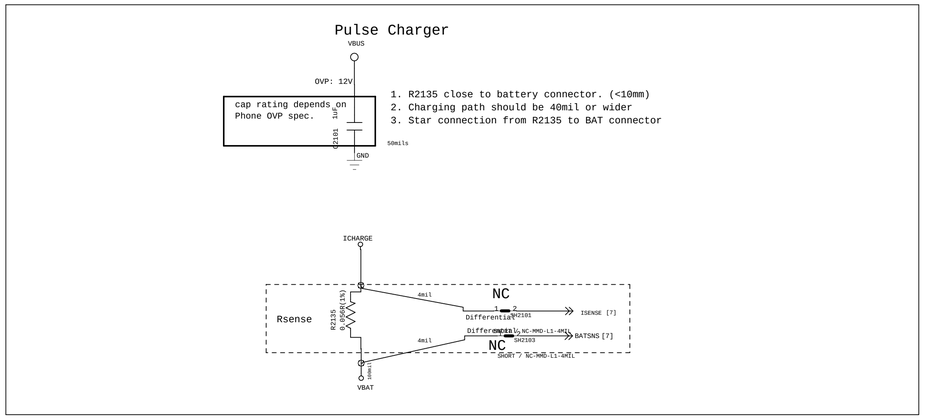
BATTERY CONNECTOR

Battery NTC=10K, R2103 select 16.9K, 1% 10K--16.9K
Battery NTC=47K, R2013 select 61.9K, 1% from MT6328 61.9K--47K

Need creat new sch.pcb







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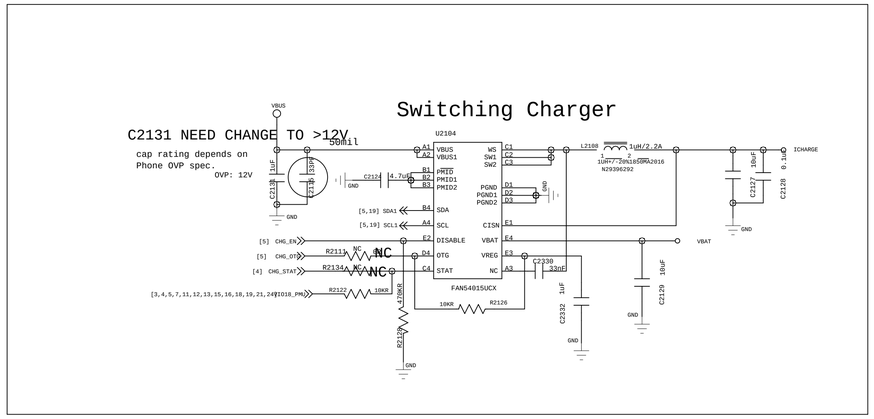

Title	21_POWER_BATTER_CHARGE
Size D	Yude Confidential
Data Sep 14,2016	Sheet 21 of 99

Flash LED

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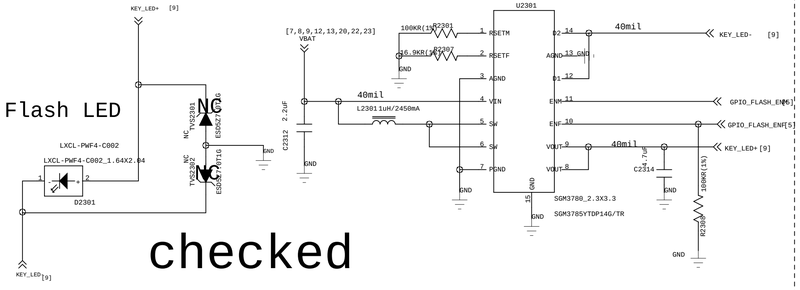
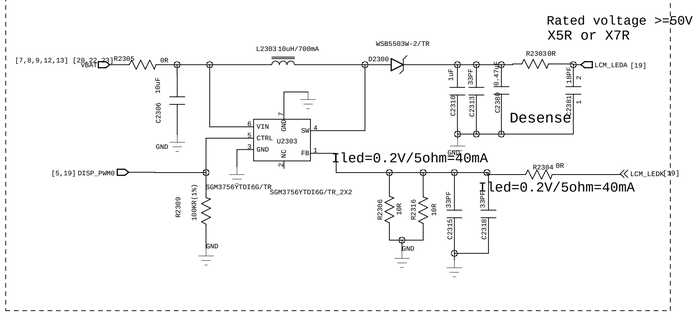
Flash Camera Frontal



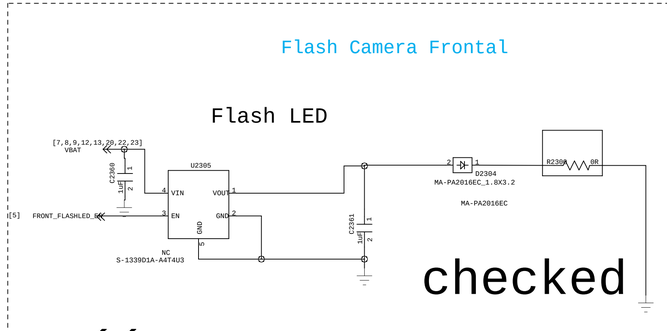
LCM Backlight LED Driver

Led do Display

Rated voltage >=50V
X5R or X7R

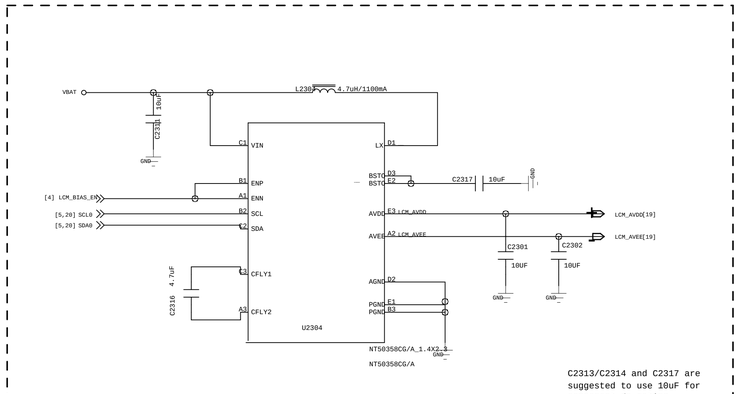


Flash Camera Frontal



LCM Gate Drive

LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)



have checked

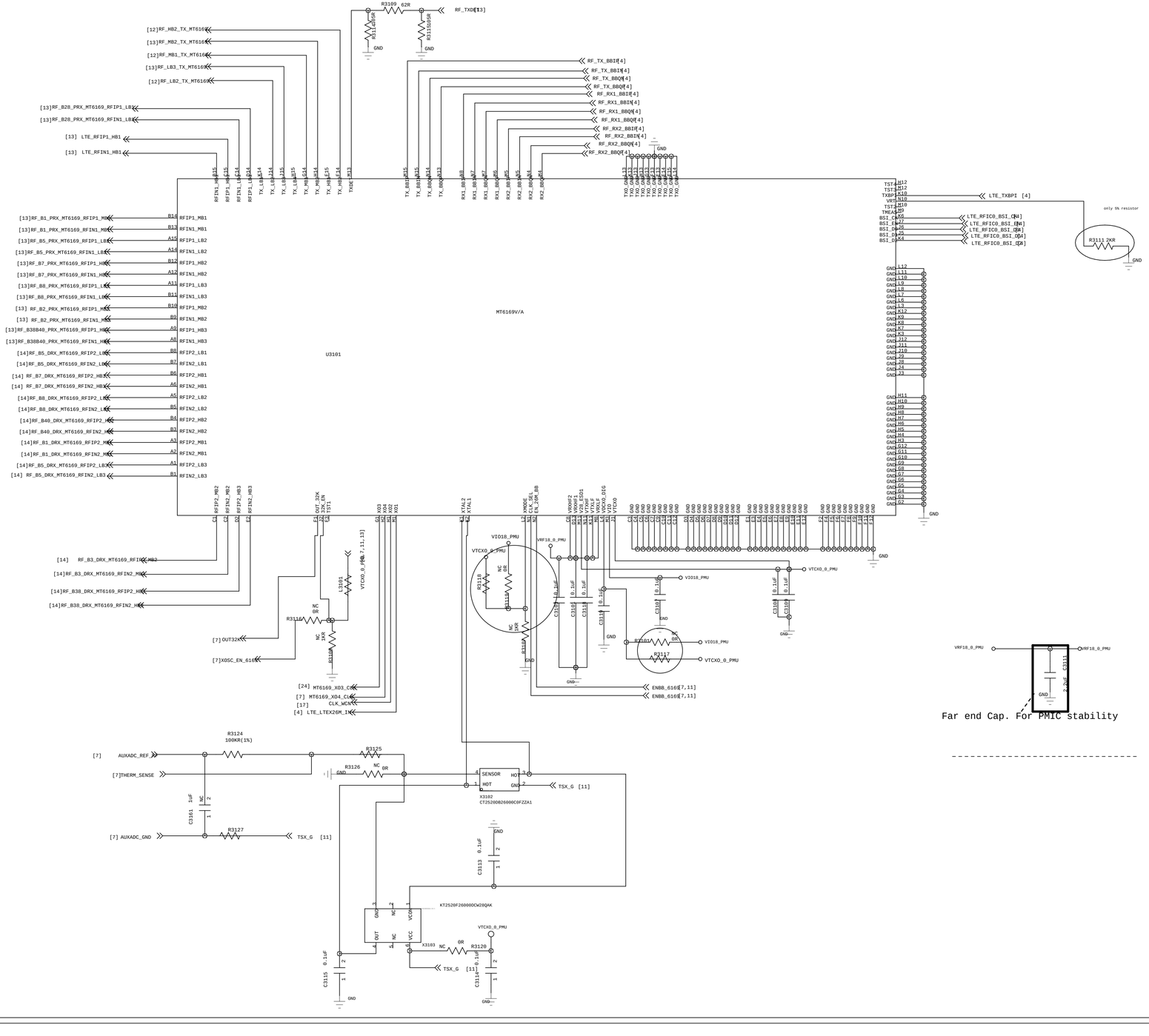
Title	23_POWER_FLASH_LCM BL	
Size D	Yude Confidential	
Data Sep 14,2016	Sheet 11 of 99	

External Buck for DRAM

If using external buck for DRAM application, please refer to "MT6735_53 DRAM External Buck Design Notice":
1. Please add one more 1uF capacitor on PMIC VM output side (Must)
2. Please turn off Fast Transient Function of PMIC VM LDO (Must)

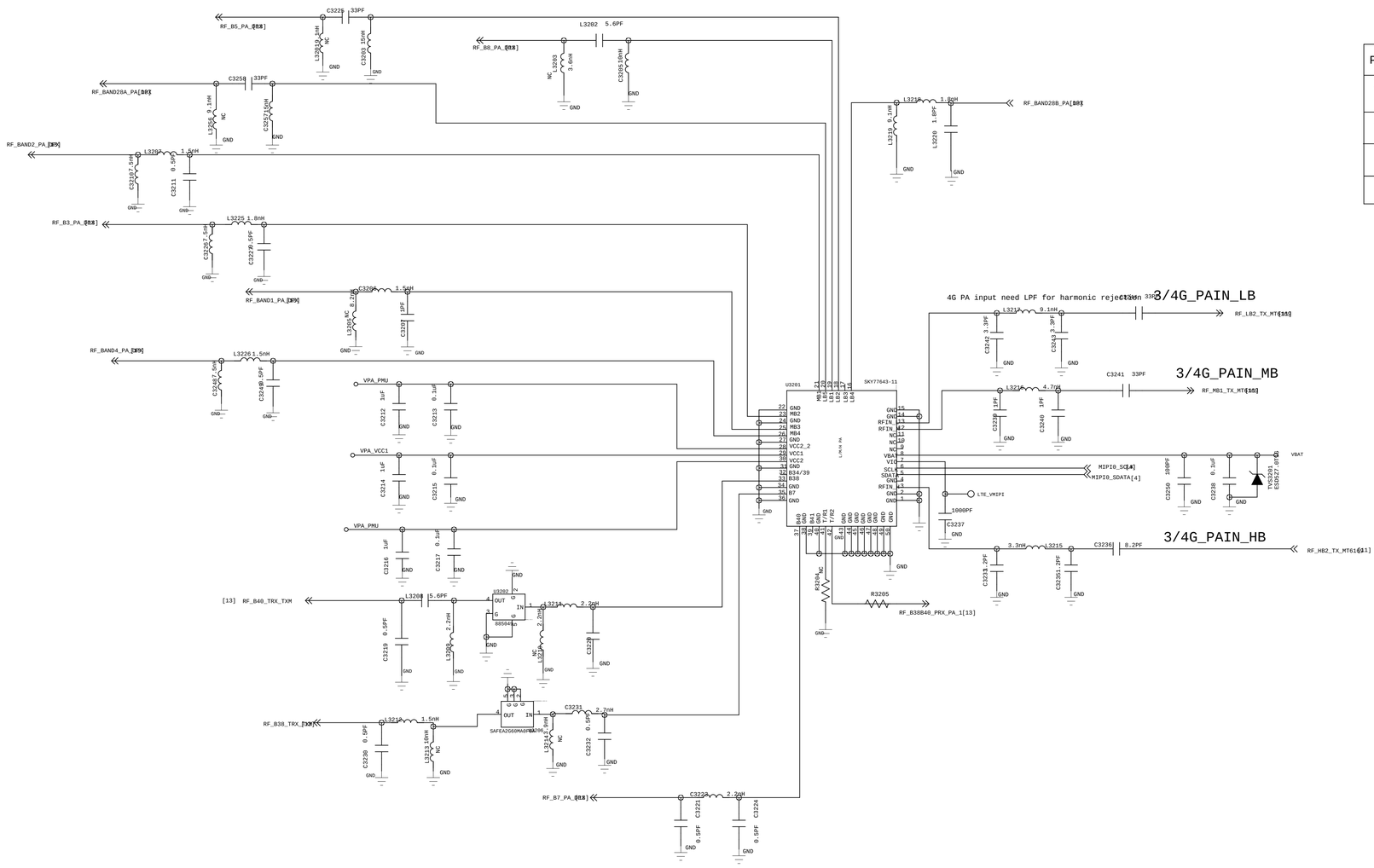
Title	24_NONE	
Size D	Yude Confidential	
Data Sep 14,2016		Sheet 11 of 99

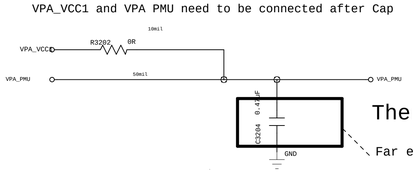
Power trace	PCB line width	MAX current
VRF18_0_PMU	0.4mm	
VIO18_PMU	0.35mm	
VTCXO_0_PMU	0.2mm	

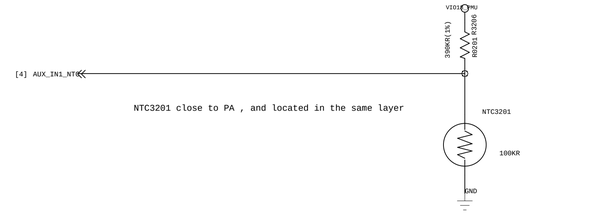


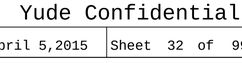
Title	31_RF_MT6169_PIN_OUT	
Size D	Yude Confidential	
Data April 5,2015	Sheet 31 of 99	

Power trace	PCB line width	MAX current
VPA_PMU	1.1mm	
VPA_VCC1	0.5mm	
VBAT	0.15mm	
LTE_VMIPI	0.15mm	





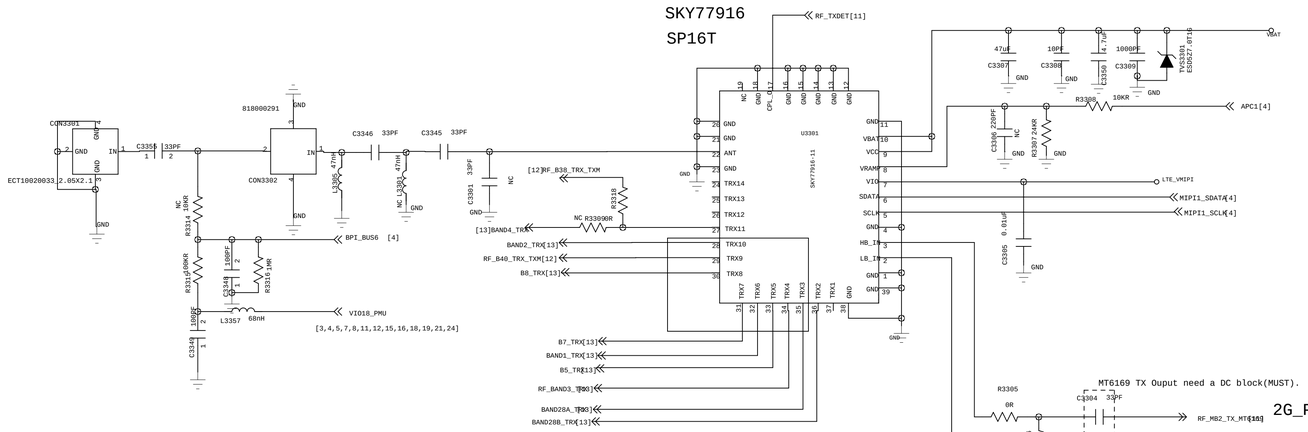




Title	32_RF_MT6169_RF_TX	
Size D	Yude Confidential	
Data April 5,2015	Sheet 32 of 99	

Power trace	PCB line width	MAX current
VBAT	2.5mm (Min 2.0mm)	
LTE_VMIPI	0.15mm	

SKY77916 SP16T



MT6169 TX Ouput need a DC block(MUST).

R3305 0R C3304 33PF RF_MB2_TX_MT6169[11] — 2G_PAIN_HB

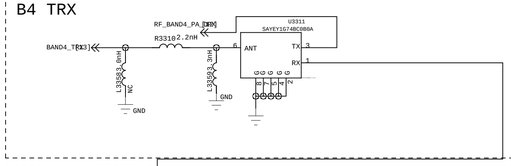
R3306 NC GND

High pass filter for G8 Tx in G7 Rx band noise rejection

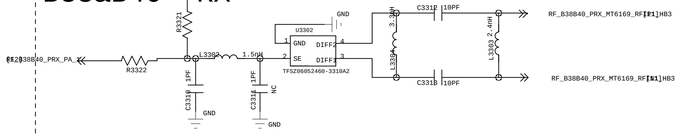
R3303 12R C3303 33PF RF_LB3_TX_MT6169[11] — 2G_PAIN_LB

R3307 440R R3304 440R GND

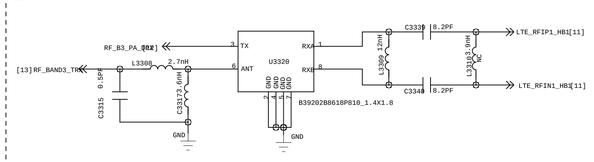
B4 TRX



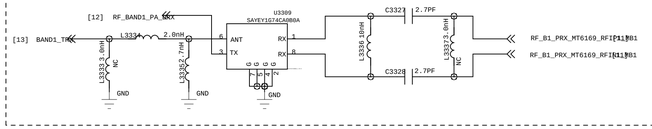
B38&B40 RX



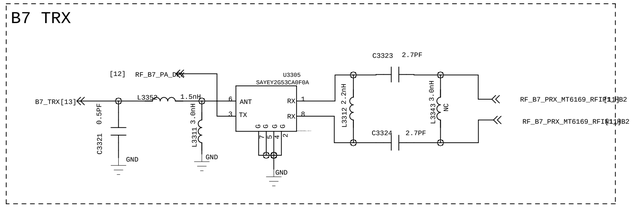
B3 TRX



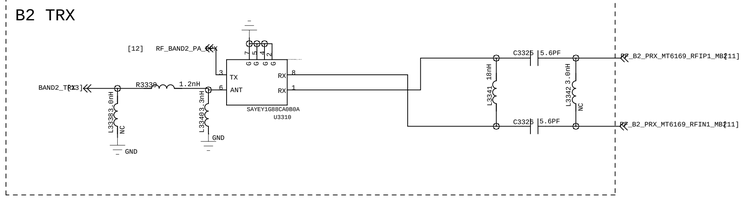
B1 TRX



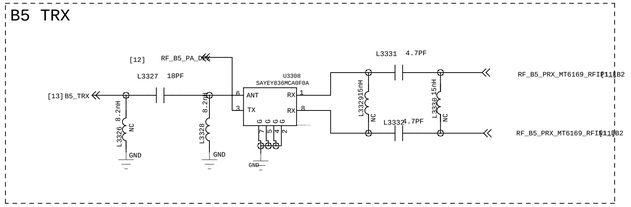
B7 TRX



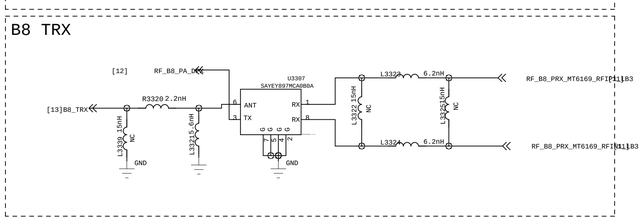
B2 TRX



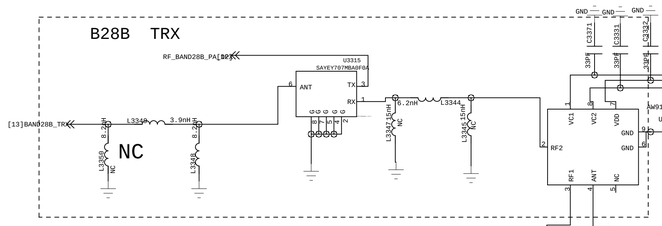
B5 TRX



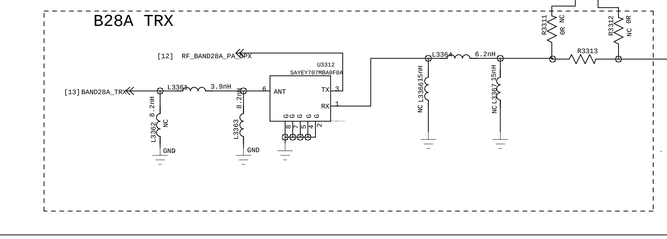
B8 TRX

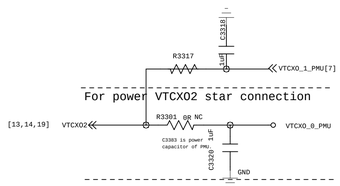


B28B TRX



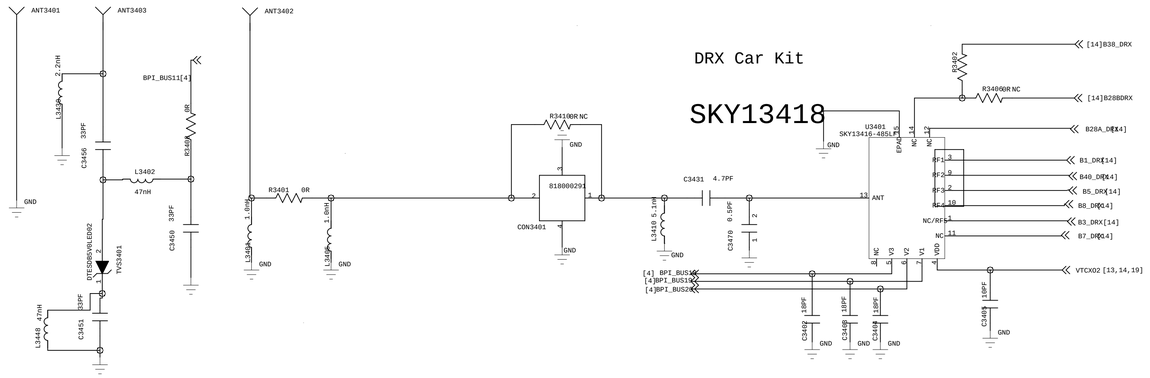
B28A TRX



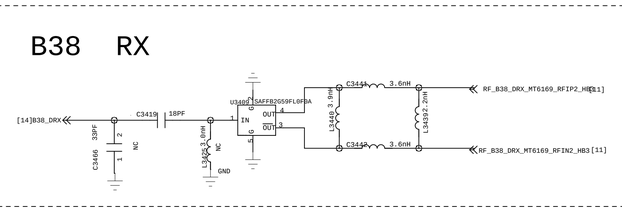


Title	33_RF_MT6169_RF_PRX	
Size D	Yude Confidential	
Data April 5,2015	Sheet 33 of 99	

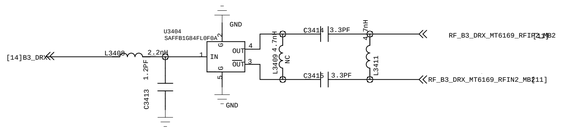
Power trace	PCB line width	MAX current
VTCXO2	0.15mm	50uA



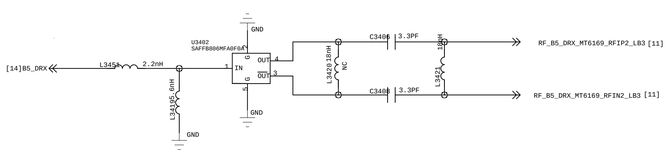
B38 RX



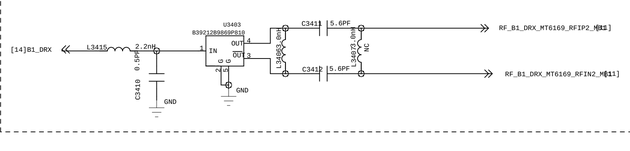
B3 DRX



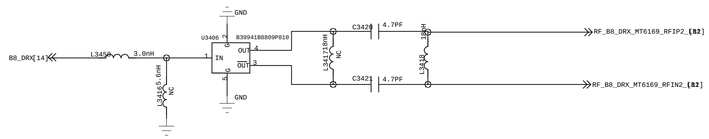
B5 DRX



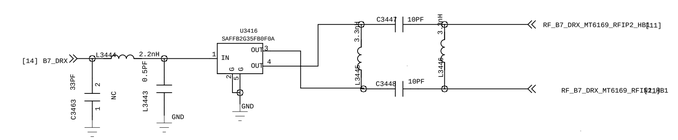
B1 DRX



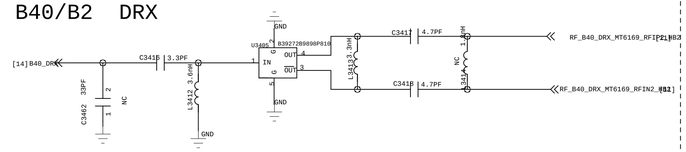
B8 DRX



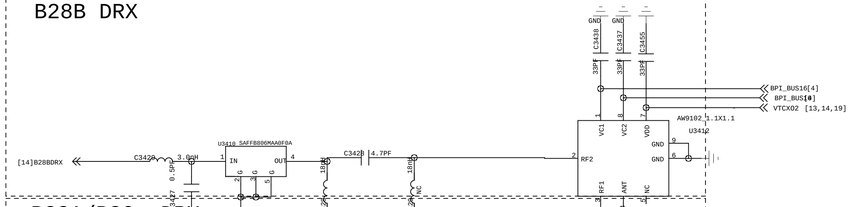
B7 RX



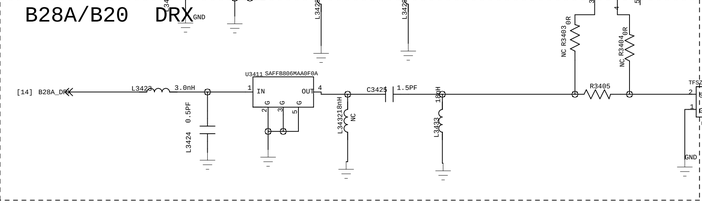
B40/B2 DRX



B28B DRX



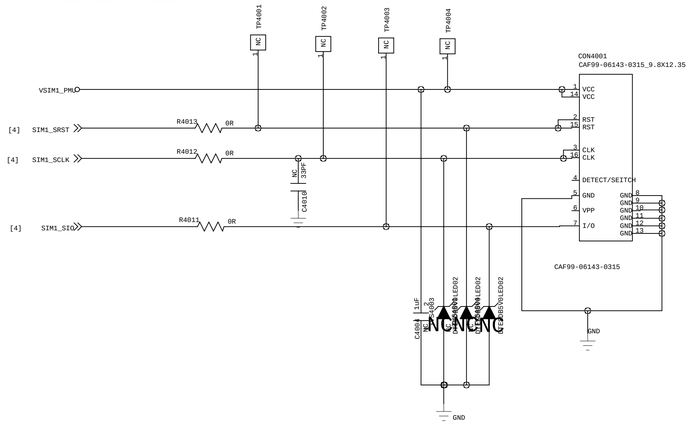
B28A/B20 DRX



Title	34_RF_MT6169_RF_DRX
Size D	Yude Confidential
Data Nov 6,2015	Sheet 34 of 99

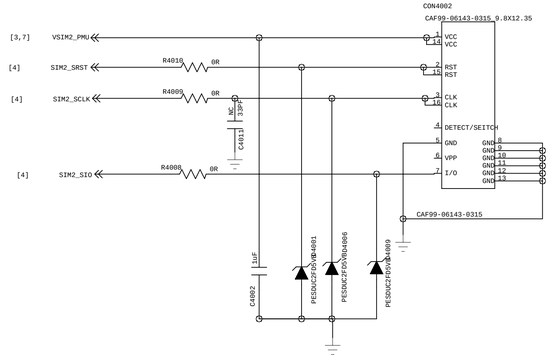
SIM1_sclk & SIM2_sclk sheilding by GND

SIM1



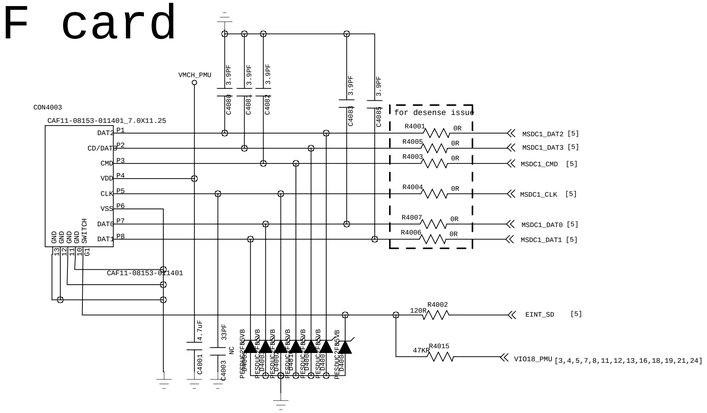
checked

SIM2



checked

TF card



checked

Title	40_MEMORY_SD_CARD_SIMCARD	
Size D	Yude Confidential	
Data Sep 14,2016	Sheet 40 of 99	

eMMC+LPDDR3 16GB eMMC + 8Gb LPDDR3

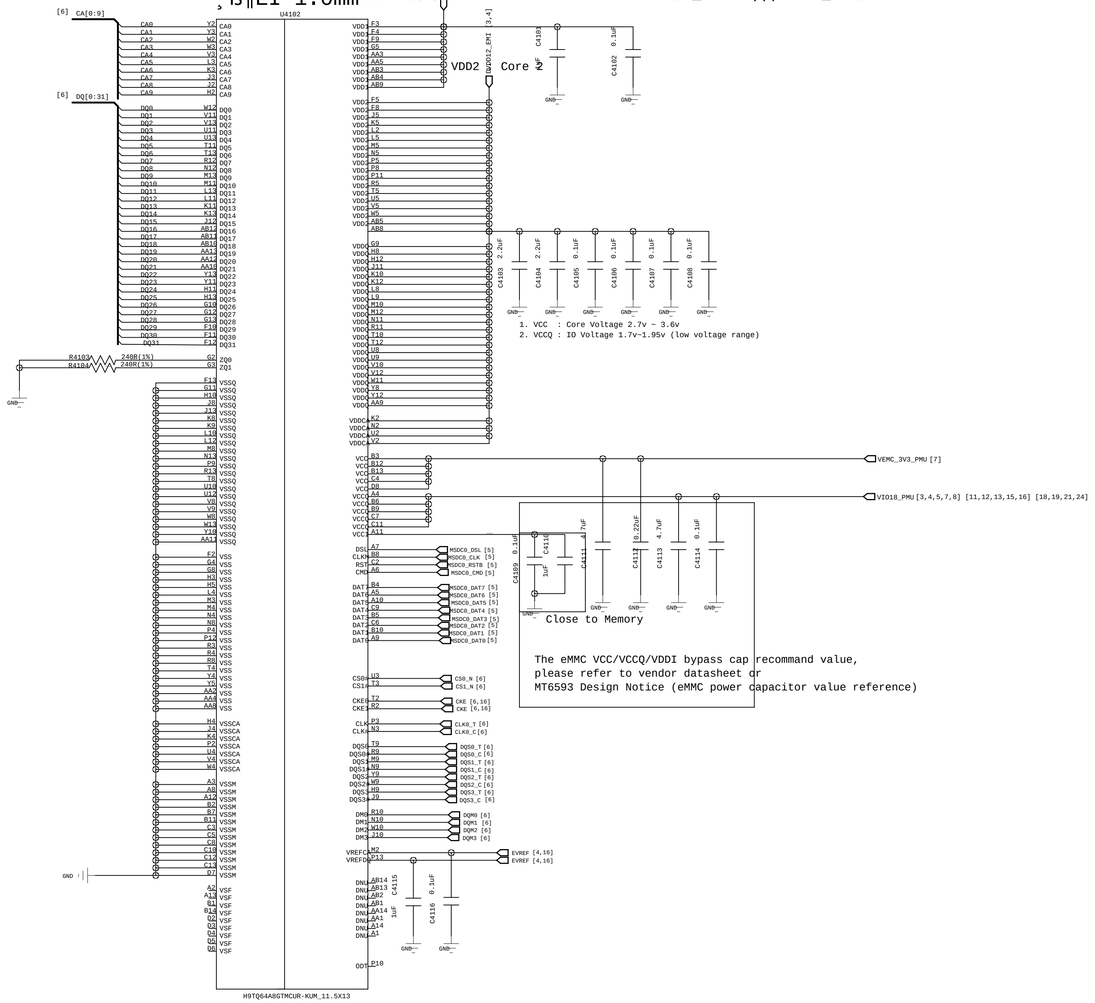
221 Ball, 0.5mm pitch

VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V

ÈýÐÇºÍº£Á¦Ê¿
¸ß¶ÈÎª1.0mm

VDD1 : Core 1

VDD2 Core 2



1. VCC : Core Voltage 2.7v ~ 3.6v
2. VCCQ : IO Voltage 1.7v~1.95v (low voltage range)

Close to Memory

The eMMC VCC/VCCQ/VDDI bypass cap recommand value,
please refer to vendor datasheet or
MT6593 Design Notice (eMMC power capacitor value reference)

Connect to AP	
DQ[0..31]	DQ[0..31]
CA[0..9]	CA[0..9]
CS0_N	CS0_N
CS1_N	CS1_N
CKE	CKE
DQM0	DQM0
DQM1	DQM1
DQM2	DQM2
DQM3	DQM3
DQS0_C	DQS0_C
DQS1_C	DQS1_C
DQS2_C	DQS2_C
DQS3_C	DQS3_C
DQS0_T	DQS0_T
DQS1_T	DQS1_T
DQS2_T	DQS2_T
DQS3_T	DQS3_T
CLK0_T	CLK0_T
CLK0_C	CLK0_C
VREF_CA	VREF_CA
VREF_DQ	VREF_DQ
MSDC0_RSTB	MSDC0_RSTB
MSDC0_CMD	MSDC0_CMD
MSDC0_CLK	MSDC0_CLK
MSDC0_DSL	MSDC0_DSL
MSDC0_DAT0	MSDC0_DAT0
MSDC0_DAT1	MSDC0_DAT1
MSDC0_DAT2	MSDC0_DAT2
MSDC0_DAT3	MSDC0_DAT3
MSDC0_DAT4	MSDC0_DAT4
MSDC0_DAT5	MSDC0_DAT5
MSDC0_DAT6	MSDC0_DAT6
MSDC0_DAT7	MSDC0_DAT7

Power I/F	
VIO18_PMU	VIO18_PMU
VEMC_3V3_PMU	VEMC_3V3_PMU
DVDD12_EMI	DVDD12_EMI

Title	41_MEMORY_EMMC_LPDDR3	
Size D	Yude Confidential	
Data Sep 14,2016	Sheet 11 of 99	

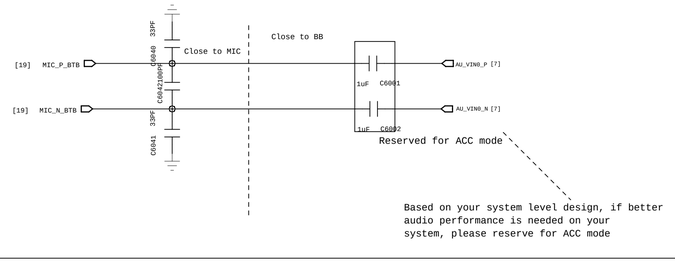
[5,17]
CONN_XO_IN
R5001
NC
R5002
[1] CLK_WCN
U5002
OUT
GND
VCC
NC
VCN28_PMU
C5003
NC
1uF
GND
12/14 by Hank
130514 TW Han modified for removing GPS co-clock
WB_CTRL4[5]
WB_CTRL5[5]
WB_CTRL3[5]
WB_CTRL2[5]
WB_CTRL1[5]
WB_CTRL0[5]
WB_RX_IP[5]
WB_RX_IN[5]
WB_AVDD18
0.1uF C5002
C5005 100PF
U5001
NC
WB_AVDD18
WB_CTRL4
WB_CTRL5
WB_CTRL3
WB_CTRL2
WB_CTRL1
WB_CTRL0
WB_RX_IP
WB_RX_IN
WB_RF_2G
NC
WB_AVDD33
WIFI5G_RF
NC
AVDD28_FM
FM_LANT_N
FM_LANT_P
GPS_RFIN
AVDD18_GPS
DVSS
AVDD28_FSOURCE
HRST_B
FM_DNG
F2W_DATA
F2W_CLK
SCLK
SDATA
SEN
CEXT
XO_IN
MT6625 IPD
[17] VCN33
0402 0R 20150407 SYX
VCN33_PMU
R5015
VCN33_PMU
R1023 can be replaced by bead for FM desense concern
VCN28_PMU
FM_AVDD28
B5001 600R
12/14 by Hank
GPS_AVDD18
R5011
VCN18_PMU
1uF C5010
GND
WB_AVDD18
R5012
WB_RX_QP[5]
WB_RX_QN[5]
WB_TX_IP[5]
WB_TX_IN[5]
WB_TX_QP[5]
WB_TX_QN[5]
GPS_RX_IP[5]
GPS_RX_IN[5]
GPS_RX_QP[5]
GPS_RX_QN[5]
ANT5002
ANT5001
ANT5003
NC 0R R5016
813000291
R5005 0R
L5013 .3nH
L5012 .2nH
CON5001
R5008 2.2PF
DP1608-V1524C
F5001
GND
H.F.
C.P
L.F.
L5011 .8nH
NC R5017 0R
C5004 18PF
R5014 3.6nH
L5008 .5PF
L5009 3.9nH
ACPF-7124/5005
C5014 2.2nH
L5006 8.2nH
L5005 1.5nH
C5006 4.7uF
C5007 100PF
FM_AVDD28
C5008 0.01uF
FM_RX_N_6625 [18]
FM_ANT [24]
L5004 82nH
NC R5018 0R
NC
NC R5006 0R
NC
GPS_AVDD18
C5009 470PF
[5]GPIO_GPS_LNA_EN
VCN28_PMU
1uF C5012
USB03SAFFB1G56KB0F0A
C5011 5.6PF
L5003 12nH
C5013 33PF
NC
AWS015_0.9X1.1
U5004
NC R5007 0R
R5003
USB03SAFFB1G56KB0F0A
R5004
CONN_RSTB[5]
F2W_DATA [5]
F2W_CLK [5]
CONN_SCLK[5]
[5]CONN_SDATA
[5]CONN_SEN
CONN_XO_IN[5,17]
C5018 1uF
C5019 100PF
GND

Speaker NC

Based on your system level design , if better desense performance is needed on your system.

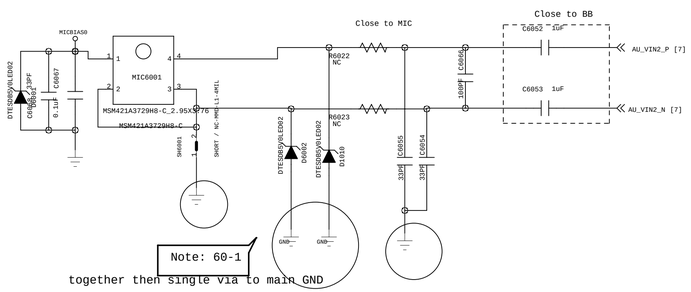
Based on your system level design , if better ESD performance is needed on your system.

Handset Microphone 1



Based on your system level design, if better audio performance is needed on your system, please reserve for ACC mode

Second MIC NC



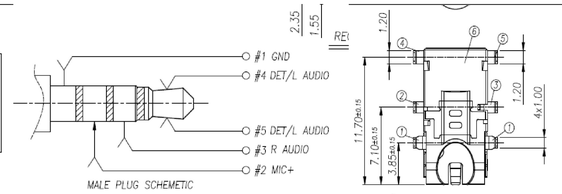
together then single via to main GND

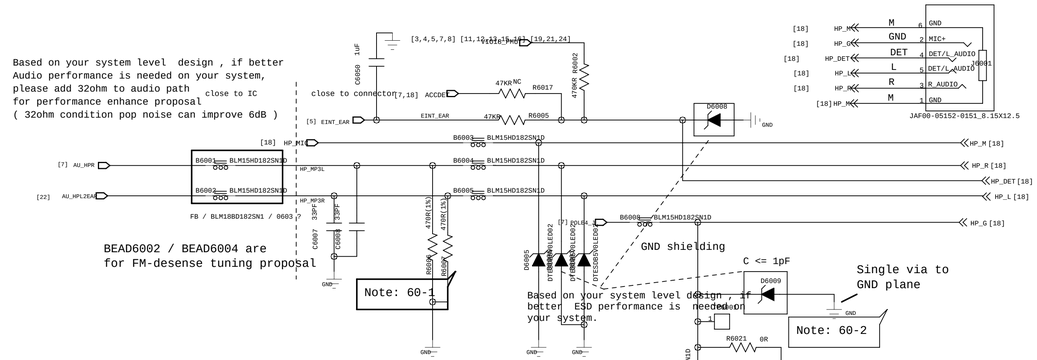
checked

Earphone AudioÃÀ±ê

DIMENSION IN mm	LCN Shenzhen Linkconn Electronics Co.,Ltd.	
TOLERANCE UNLESS OTHERWISE SPECIFIED	APR.	TITLE: ø3.5 AUDIO JACK (DIP) INSERT TYPE
.X±0.35 .X.±5'	CHK.	DWG NO. JAF00-05152-0151
.XX±0.25 .X'±3'	PROJ.	CUSTOMER DRAWING
.XXX±0.15 .XX'±1'	DRA. pengzhijun 2015.07.31	SIZE A4 SCALE 3:1 SHEET 1/2 REV. A

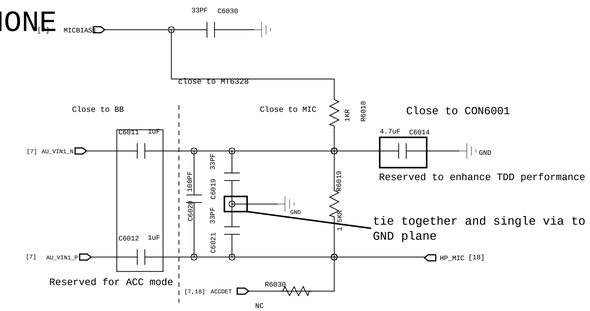
(1) iPhone : L-R-G-M



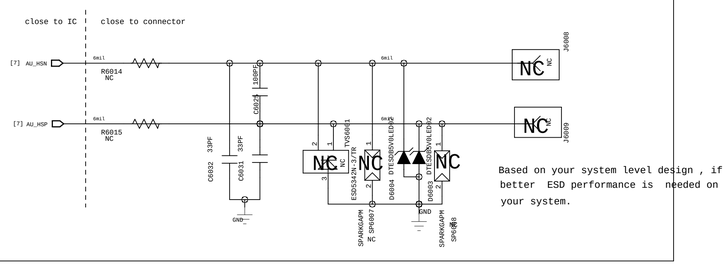


BEAD6002 / BEAD6004 are for FM-desense tuning proposal

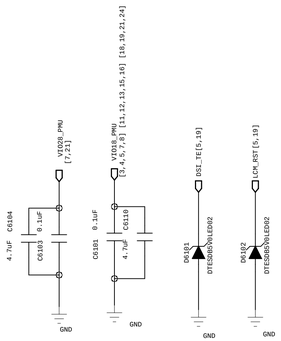
Earphone MICPHONE

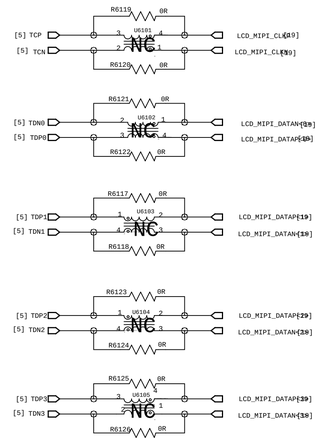


Receiver

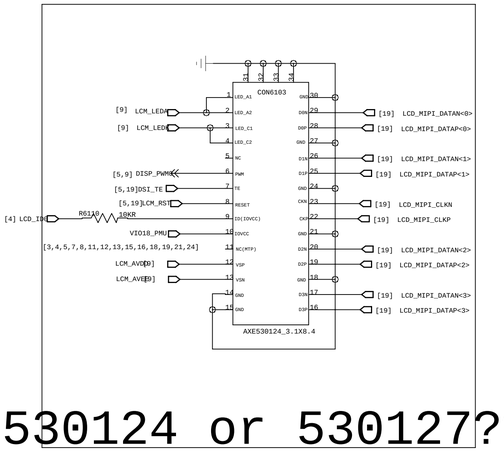


Title	60_PERI_AUDIO_IO
Size D	Yude Confidential
Data Sep 14,2016	Sheet 60 of 99



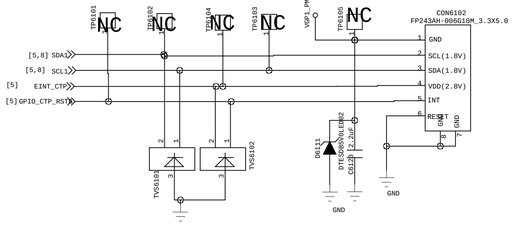


ÆÁÁ¬½ÓÆ÷



530124 or 530127???

define pin accord customer CTP



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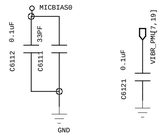
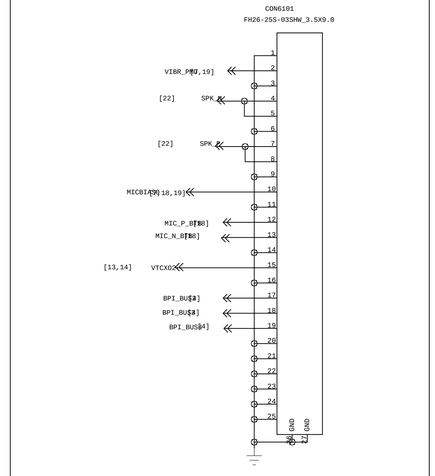
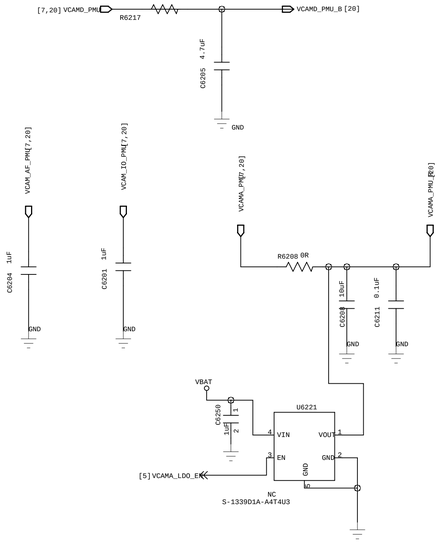


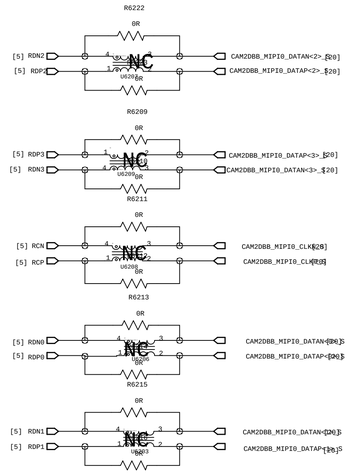
25PIN´óÐ¡°åÁ¬½ÓÆ÷ZIF

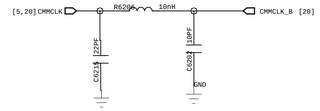


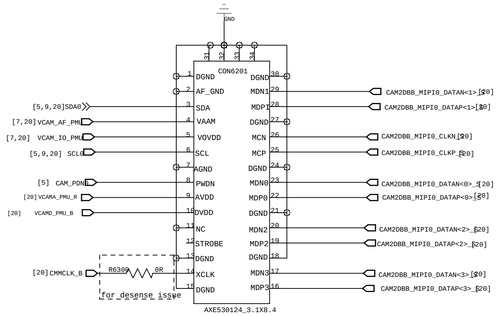
Title	61_PERI_LCD_CTP
Size D	Yude Confidential
Data Sep 14,2016	Sheet 61 of 99

MAIN_CAMERA

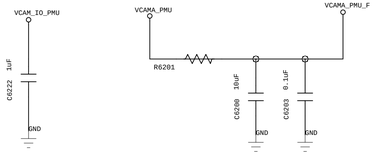


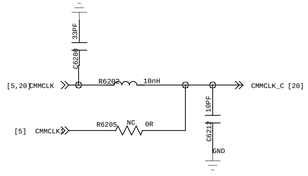


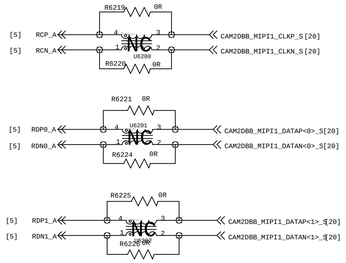


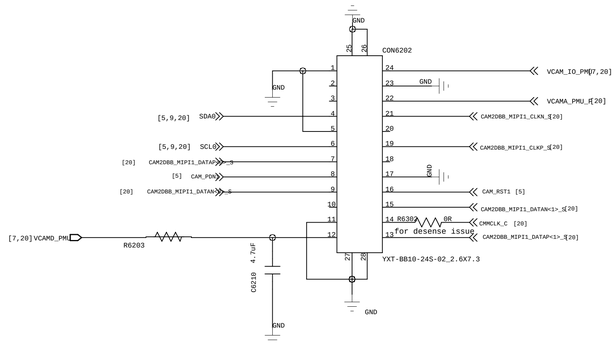


SUB_CAMERA









Need creat new sch,pcb

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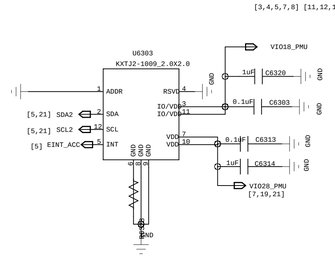
G Sensor-3X



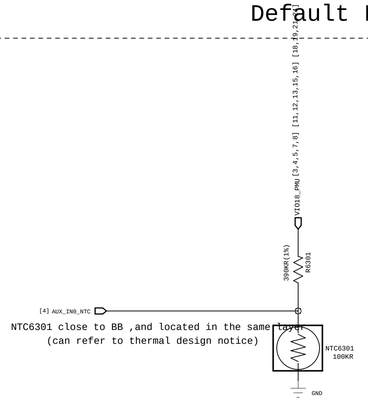
CS=1: IIC

LIS3DHTR : SA0=0: IIC ADDRRSS is 0x18H
KXCJK-1113 : SA0=0: IIC ADDRRSS is 0x1DH
power down(communicating), I = 0.5uA

Configuration VS Chip

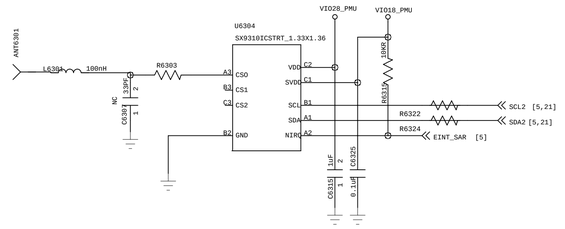
Fuction	U3001	C3004	C3005	C3006	R3003
G-Sensor	LIS3DHTR	NC	NC	NC	0
G-Sensor	KXCJK-1113	NC	NC	NC	0

Default LIS3DHTR



Thermistor / To sense board level temperature

SAR Sensor



have checked

Title	63_PERI_SENSORS
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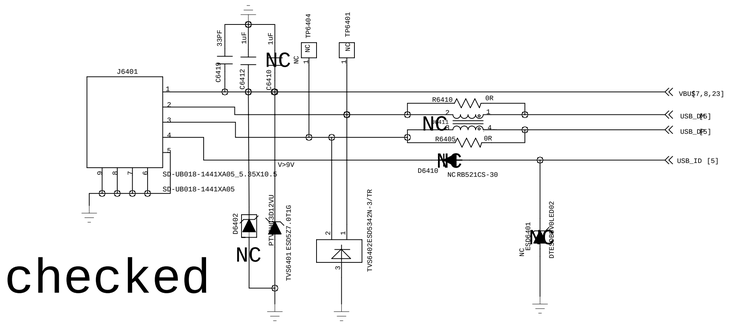

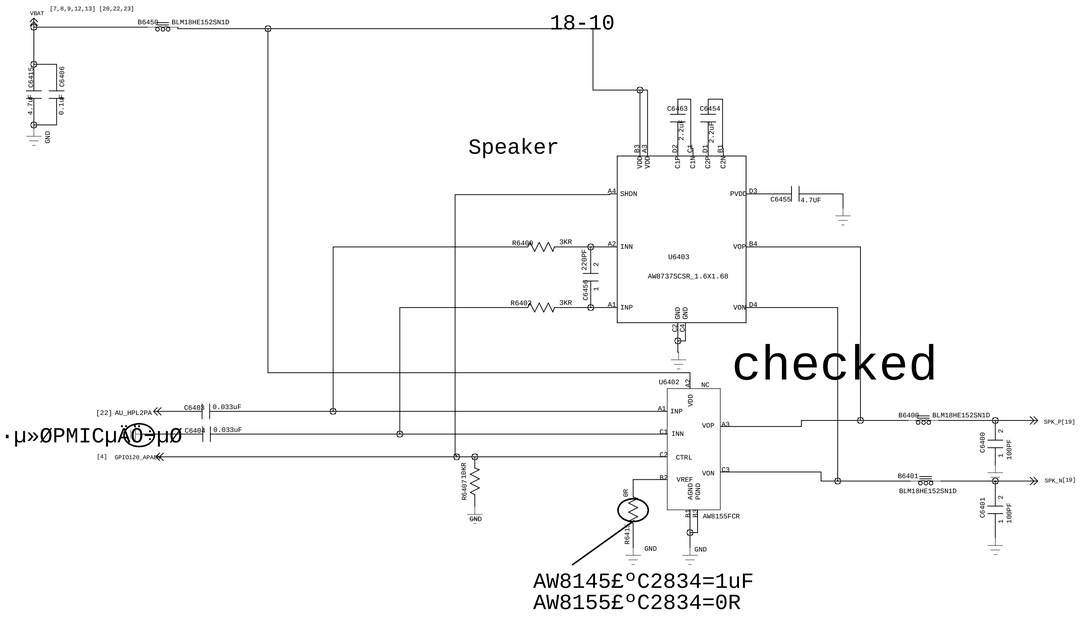

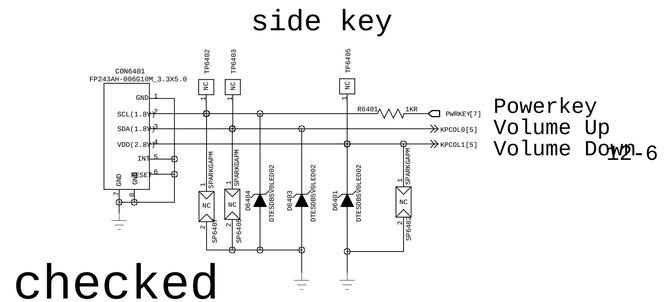

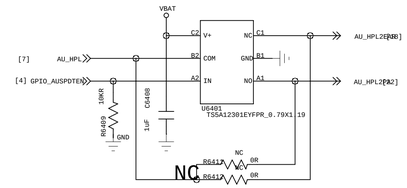

Title	64_PERI_USB_KEYPAD	
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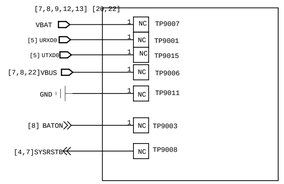
TEST POINTS



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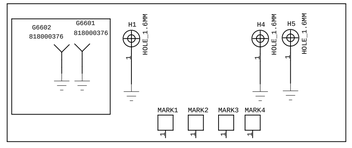

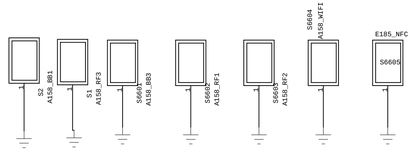

have checked

Title	65_TEST POINT	
Size D	Yude Confidential	
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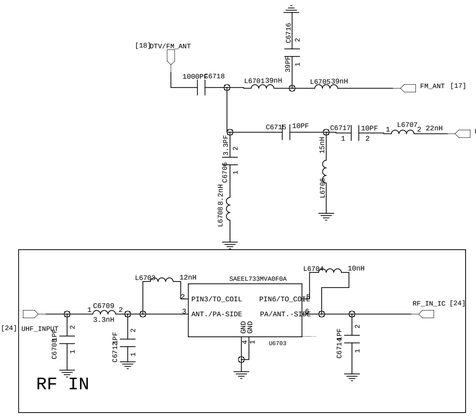
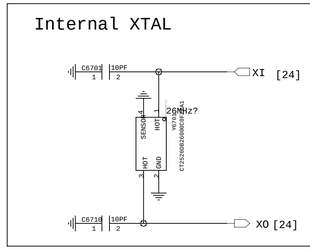
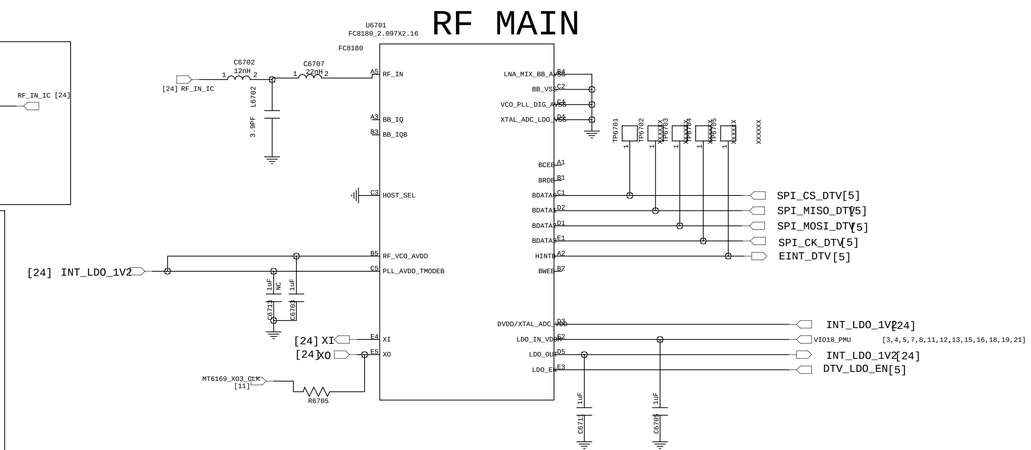
RF MAIN







Title	67_DTV	
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