Pemba

Operational Description / Theory of Operation

1 Introduction

Pemba is a mass market clamshell phone with quad-band capability. A brief description of this product is given below:

Physical & Hardware

- Size 46X99X17.5
- Weight ~ 107g
- Form Factor: Clam
- Modes/Bands: Quad Band, GSM 850/900/1800/1900, EDGE class 12. GPRS class 12
- Chipset/Memory: TransAAM Raptor, LTE2, AUL, ATI 2282 / 512Mb / 128Mb RAM
- Display: 176X220 1.9” TFT , 262K colors, 96X80 1.0” CSTN, 64K CLI
- Battery/TT/SB time): BT50/880mAh, TT: Up to 450mins, SB: 350 hrs

Software

- Messaging/WAP: MMS, SMS, EMS, IM, Email (pop3/SMTP/IMAP4), PTT edge class 12, Java, DI
- Special Features: Progressive download, video streaming, stereo BT, Screen3, Crystal talk

E2E

Audio: MP3, AAC, AAC+, AAC+ Enhanced,
Video: MPEG4 Capture with 4x zoom, QCIF Playback @15fps; H.263 video streaming
Camera: 1.3MP, 8x digital zoom, Fixed focus
Music: MP3/AAC+ Enhanced digital music player (ring tones & music)
Memory: 15MB User Internal memory, external MicroSD™ up to 1GB
Connectivity: Mini-USB, BT Class 2, USB 1.1, PC Synch, Motosynch, Mobile Phone Tools

2 RF Operation

2.1 Functional Block Diagram

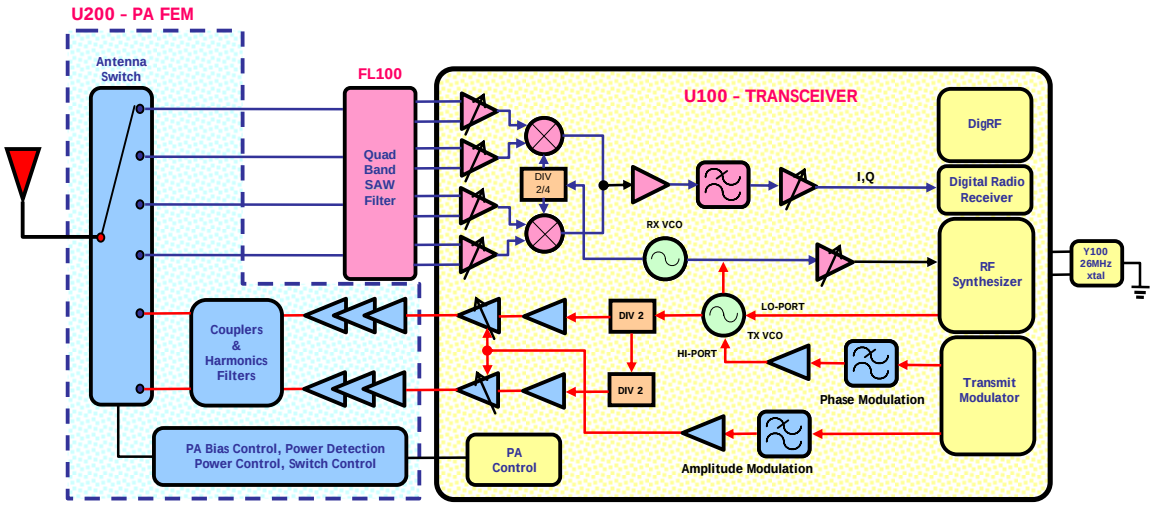

Figure 1. RF Functional Block Diagram

2.2 The Raptor PA FEM (U200)

The Raptor PA FEM is a quad-band GSM, GPRS and EDGE Power Amplifier Front End Module (FEM). It operates over the GSM850, EGSM900, DCS1800, and PCS1900 transmit and receive frequency bands. Power amplification, power coupling, power detection, low-pass filtering, output power control, and antenna switching functions are integrated into this module.

The Raptor module is specified to operate with both GMSK and 8PSK modulation schemes, and is intended to be used in combination with the TransAAM transceiver. Two modes of power control are supported with the Raptor module – bias control for GMSK modulation, and input power control for 8PSK modulation.

The Raptor module includes the following features:

- Quad-Band: GSM850, EGSM900, DCS1800, PCS1900
- Integrated output power control and antenna switching
- EDGE Class 12 operation
- GMSK Power Class 4 operation (GSM850/EGSM900), +33dBm
- GMSK Power Class 1 operation (DCS1800/PCS1900), +30dBm
- EDGE Power Class E2 operation (+27dBm average in LB and +26dBm average in HB)

2.3 Antenna Switch (U200 – Raptor PA FEM)

The antenna switch within the Raptor module routes the transmit or receive signal between the antenna and the respective transmit or receive lineup. This switch is controlled by three control signals – LB_HB, US_EURO, and TX_ANT_SW_EN. The table below shows the truth table for the switching:

LB_HB	US_EURO	TX_ANT_SW_EN	TX / RX	BAND
0	0	0	RX	GSM850
0	1	0		EGSM900
1	1	0		DCS1800
1	0	0		PCS1900
0	0	1	TX	GSM850/EGSM900
1	0	1		DCS1800/PCS1900

Table 1. Antenna Switch Truth Table

2.4 Receiver Operation (U100)

The receiver architecture is digital VLIF/DCR. There are four separate LNAs supporting functionality for GSM850, EGSM900, DCS1800 and PCS1900 frequency bands. The quadrature mixer down-converts the received RF signal to baseband. Filtering at the mixer output then limits out of band signals in the active stages of the baseband section. The I and Q analog baseband signals are passed through low-pass anti-aliasing filters and dc offset correction circuits before being processed by the analog-to-digital converters (in the digital radio receiver block). The outputs of the converters are passed into the RxCPROC, and finally sent serially to the baseband processor via the DigRF interface port.

2.5 Transmitter Operation (U100, U200)

The TX architecture is a polar modulator with direct digital modulation of the VCO. The module can transmit GMSK (phase modulation) or 8PSK (phase and amplitude modulation) mode.

In GMSK mode, the dual port TX VCO is phase modulated by the dual port synthesizer and the signal is fed to the PA input at a fixed level. In 8PSK mode, the additional amplitude modulation is performed via a commuting switch mixer. Two DACs provide signals to the modulator. One DAC is dedicated to the amplitude component of the 8PSK waveform and the other to driving the VCO high port input.

The Raptor and TransAAM modules support two modes of power control operation: Bias Control (GMSK modulation) and Input Power Control (8PSK modulation). The figure below shows the connections between the two modules.

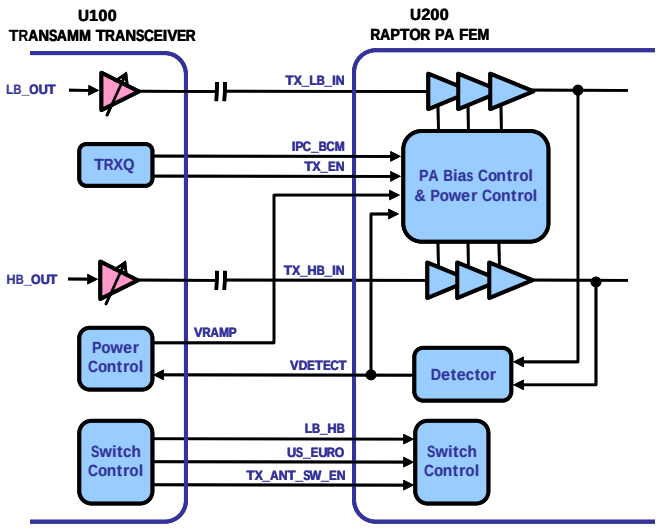

Figure 2. Output Power Control

The TRXQ (transmit/receive sequencer) is a programmable sequencer controlling all the timing of the radio, from power-up sequence through the warm-up of the synthesizer and VCO, calibrations when required, handling of a burst, and finally powering down the radio at the end of a burst if appropriate. It generates appropriate timing events for the transmitter calibration and the EDGE/GMSK transmit/receive burst.

2.6 Frequency Generation

Both the RX and TX VCO run at 3296 to 3820 MHz, and have integrated resonators with 32 states of digital course tuning. The frequency synthesizer is a 24-bit, 3rd order fractional-N synthesizer with digital AFC. A 26 MHz crystal oscillator provides a stable frequency reference.

The VCO output signal runs through a divide-by-two for operation in the DCS/PCS bands and a divide-by-four for operation in the GSM850 and EGSM900 bands.

The 26 MHz reference crystal oscillator provides a stable frequency reference for the major functions in the radio system. The crystal output can also be routed to two auxiliary reference pins to provide a reference clock for RF accessory circuitry such as Bluetooth.

2.7 The DigRF Interface

Interface to the baseband IC using the DigRF standard. The DigRF standard specifies the logical, electrical, and timing details of the RF/Baseband interface. The figure below shows the DigRF standard RF-baseband interface.

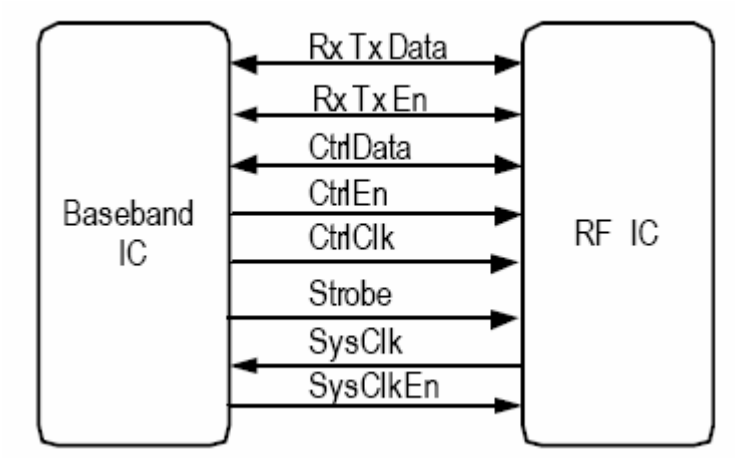

Figure 3. The DigRF Interface

3 Power Management – Atlas UltraLite (AUL)

Atlas Ultra-Lite (AUL) is a highly integrated mixed mode power management and user interface IC. It combines several baseband functions such as general power, audio and lighting management.

A high level diagram of AUL is shown in Figure 4.

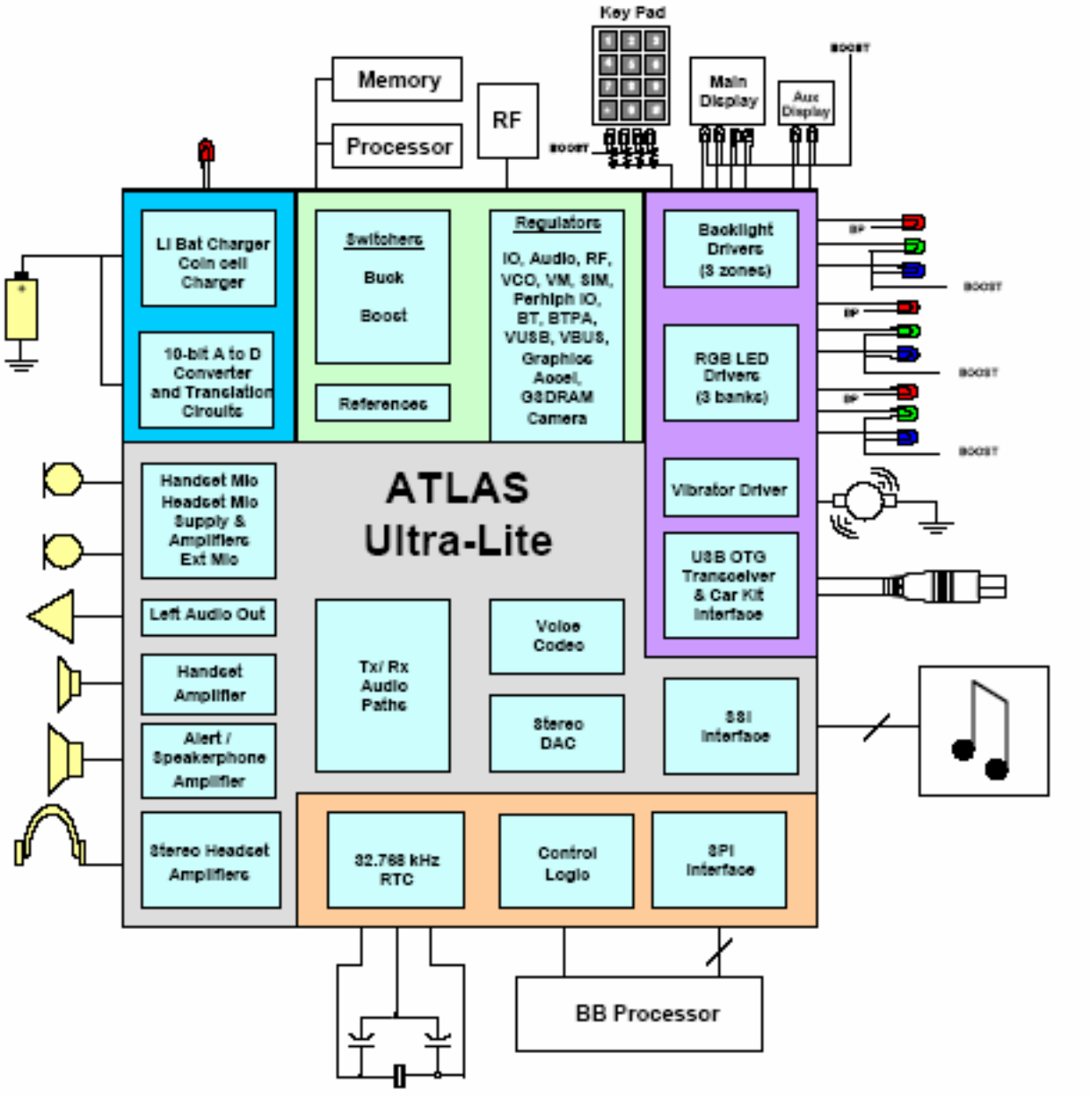

Figure 4. High level diagram of AUL

3.1 AUL to LTE2 Connections

Pins from seven sections in AUL are connected to LTE2. They are:

- Switchers
- Regulators
- USB / RS232
- Control logic
- Oscillator and RTC
- SPI interface
- A to D converter
- Audio bus

The pin-to-pin connections (excluding switchers and regulators) are tabulated in Table 4 below.

AUL Pin	AUL Pin Description	AUL Connection	
		Signal Name	LTE2 Pin
USB / RS232			
URXVM	1. Optional USB receiver processor interface data output (logic level version of D-) 2. Optional RS323 processor interface receive data output	USB_VMIN	USB_VMIN
URXVP	Optional USB receiver processor interface data output (logic level version of D+)	USB_VPIN	USB_VPIN
URCVD	1. Optional USB receiver processor interface differential data output (logic level version of D+/D-) 2. Optional RS323 processor interface request to send output	USB_XRXD	USB_XRXD
UTXENB	1. USB processor interface transmit enable bar 2. Optional RS323 processor interface request to send output	USB_TXENB	EN_USB_TXB
USE0VM	1. USB processor interface transmit single ended zero signal input or transmit minus data input (logic level version of D-) 2. Optional USB processor interface received single ended zero output 3. Optional RS323 processor interface receive data output	USB_VMOUT	USB_VMOUT
UDATPV	1. USB processor interface transmit data input (logic level version of D+/D-) or transmit positive data input (logic level version of D+) 2. Optional USB processor interface receive data output (logic level version of D+/D-) 3. RS323 processor interface	USB_VPOUT	USB_VPOUT
Control Logic			
WDI	Watchdog input	WDOG	WDOG
RESETB	Reset output	RESETB	RESET_IN
INT	Interrupt output	AUL_INT	INT1
STANDBY	Standby input signal from primary processor	STANDBY	STANDBY
Oscillator and RTC			
CLK32K	32kHz Clock output to the processor	CLK_32KHZ	CLK_IL
SPI Interface			
CS	SPI Chip Select	AUL_CS	SPI_CS3
SPICLK	SPI clock input	BB_SPI_CLK	CLK_QSA
MOSI	SPI write input	BB_SPI_MOSI	MOSIA
MISO	SPI read output	BB_SPI_MISO	MISOA
A to D Converter			
ADTRIG	ADC trigger input	TX_EN_BM	TOUT11
Audio Bus			
BITCLK	Bit clock for audio bus. Input in slave mode, output in master mode	BB_SAP_CLK	CLK_SA
FSYNC	Frame synchronization clock for audio bus. Input in slave mode, output in master mode	BB_SAP_FS	SC2A
RX	Receive data input for audio bus	BB_SAP_TX	STDA
TX	Transmit data output for audio bus	BB_SAP_RX	SRDA
CLKIN	Clock input for audio bus	CLK_13MHZ	ADC_SYNC

Table 2. AUL to LTE2 Connections

3.2 SPI Interface

It should be noted that AUL has only one SPI read output interface. Therefore, no SPI arbitration is needed for access to audio and ADC. One other point should be noted is that AUL has 64 fields for control bits. The details can be found in **Error! Reference source not found.**.

3.3 Battery and Charger

Pemba supports charging through the EMU interface only, and they will not have the standard charger connector. As such, the charger supplied with the phone and all other charging accessories will have EMU connectors.

AUL supports three charging configuration, and dual path charging configuration has been chosen. This is selected by grounding the CHRGMOD0 pin. This configuration requires four discrete transistors.

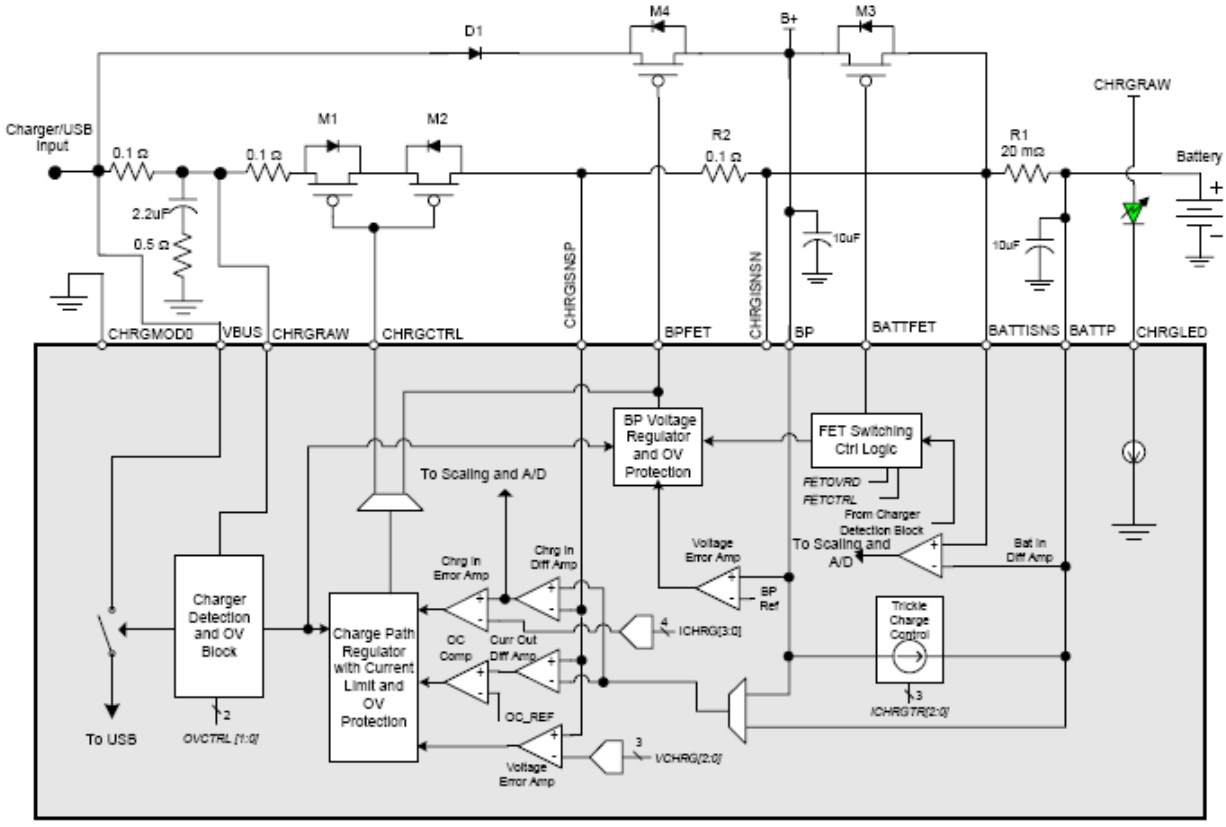

Figure 5. Block Diagram for Dual-Path Charging

In dual path charging, the supply current to B+ and battery is separated to two different paths. This makes it possible to support operation when the battery is dead or absent. From Figure 5, the charging path is controlled by M1 and M2 through CHRGCTRL, and they operate as a voltage regulator with programmable current limit. Transistor M4 controls the supply path from the EMU interface to B+. The fourth transistor M3 is a switch that connects the battery to B+.

3.4 ADC

AUL has a single ADC that supports a total of 8 channels. Of the 8 channels in AUL, 4 of them are able to perform general-purpose measurement, selectable by SPI bits located in SPI register 43. The ADC channel assignment is listed in Table 3.

Channel	SPI Bit (ADC 0 Register 43)	Signal Read	Measurement Connection
0	-	BATSNS	Charging circuit
1	BATICON = 1	BATT_I_ADC	Charging circuit
	BATICON = 0	ADIN1	-
2	-	BPSNS	Charging circuit
3	-	CHRGRAW	Charging circuit
4	CHRGICON = 1	CHGI	Charging circuit
	CHRGICON = 0	ADIN4	-
5	-	BATT_THERM / ADIN5	Thermistor
6	LICELLON = 1	LiCell	RTC battery
	LICELLON = 0	ADIN6	-
7	-	USB_ID / ADIN7	USB ID

Table 3. List of ADC Channels and their Assignment

3.5 ADC

Functional Block	Regulator Used	Voltage Level Used	Current Rating of Regulator Used	Power Input to Regulator
Raptor PA	From B+	B+	-----	-----
	VCO_REG	2.775V	200mA	Input : B+
TransAAM	RF_REG	2.775V	200mA	Input : B+
	VCO_REG	2.775V	350mA	Input : B+
	VM_REG	2.7V	10mA	Input : B+
	IO_REG	2.775V	60mA	Input : B+
	VBUCK	1.875V	350mA	Input : B+
	REF1V2	1.2V	-----	-----
Neptune LTE2				
QVDD	VBUCK	1.875V	350mA	Input : B+
AVDD	VBUCK	1.875V	350mA	Input : B+
BVDD~EVDD	PERIPH_REG	2.775V	200mA	Input : B+
JVDD	IO_REG	2.775V	75mA	Input : B+
FVDD	SIM_REG	2.85V	20mA	Input : B+
LVDD	REF_REG	1.575V	200uA	Input : IO_REG
VDDA	PERIPH_REG	2.775V	200mA	Input : B+
AUL	From B+	B+	-----	-----
TFT-LCD	PERIPH_REG	2.775V	200mA	Input : B+
ATI2282				
VDDC (core)	GRAPH_REG (from LDO switcher U1371 : 5109920D45)	1.5V	350 mA	Input : B+
VDDR1(CPU)	PERIPH_REG	2.775V	200mA	Input : B+
VDDR2 (LCD)	VBUCK	1.875V	350mA	Input : B+
VDDR3(RAM)	PERIPH_REG	2.775V	200mA	Input : B+
VDDR4(VIPO)	VBUCK	1.875V	350mA	Input : B+
VDDR5 (GPIOC)	PERIPH_REG	2.775V	200mA	Input : B+
VDDR6(GPIO)	VBUCK	1.875V	350mA	Input : B+
VDDR7(GPIOD)	PERIPH_REG	2.775V	200mA	Input : B+
PESD	IO_REG	2.775V	75mA	Input : B+
PVDD	GRAPH_REG (from LDO switcher U1371)	1.5V	350mA	Input : B+
VIVDD (EXT RAM CORE)	VBUCK	1.875V	350mA	Input : B+
I_VDDQ(EXT RAM IO)	PERIPH_REG	1.875V	200mA	Input : B+
Memory	VBUCK	1.875V	350mA	Input : B+
Display/ CLI Backlight	VBOOST	5.0V	350mA	Input : B+
EL Backlight	From B+	B+	-----	-----
Not Used	BT_REG	-----	-----	-----
Camera	CAM_REG	2.75V	200mA	Input : B+
	GSDRAM_REG	1.55V	200mA	Input : B+
Tri-Flash	From B+ (Use LDO switcher U970)	B+	-----	-----
SIM/MEGASIM	From B+ (Use LDO switcher U1373)	B+	-----	-----
Vibrator	VIB_REG	1.3V	200mA	Input : B+
Audio Circuit	AUD_REG	2.775V	200mA	Input : B+
Not Used	BT_PA_REG	-----	-----	-----
BT	From B+	B+	-----	-----
	PERIPH_REG	2.775V	200mA	Input: B+

Table 4. Power Tree for Pemba

3.6 Clock Generation

Atlas UL generates the 32 kHz clock from an external crystal. The 32 kHz oscillator will run at all times. It is powered by RTC_BATT, a coin cell battery that is used to maintain the real time clock. The phone will only power up when the 32 kHz becomes stable.

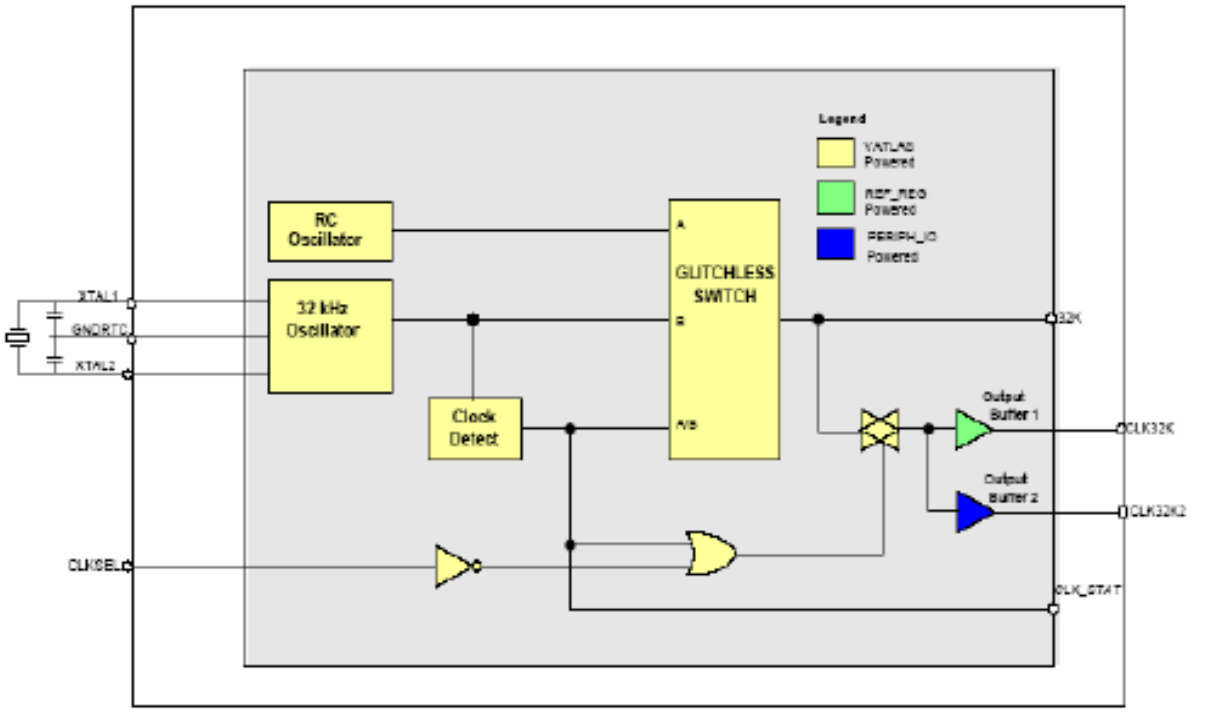

Figure 6. Atlas-UL 32kHz Clock Generation

3.7 Atlas UL – TX Audio

The mobile phone supports an internal microphone (MIC_INM) and an external headset microphone. The input path is identified and selected by the MUX controller and path gain is programmable at the PGA. The internal microphone is a single-ended surface mount part, and is biased by MICBIAS1 of the Atlas-UL IC. The signal is routed to the A3 amplifier. The headset microphone is connected through the EMU connector. The audio input and output paths of D+ and D- meet the requirement of CEA-936.

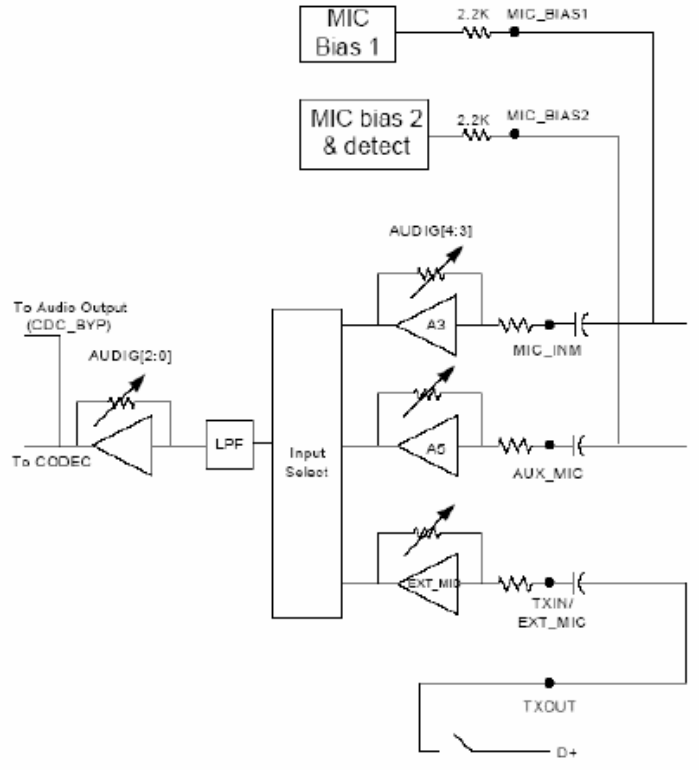

Figure 7. Atlas-UL TX-Audio

3.8 Atlas-UL RX Audio

The mobile phone supports three audio output paths. The output of Atlas-UL's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the three supported outputs via the internal multiplexer. These outputs connect to the SPKR+/SPKR- amplifier (Handset Earpiece Speaker), the ALERT+/ALERT- amplifier (Handset Loudspeaker/Alert Speaker), and the CEA-936 output. All outputs use the same D/A converter, which means that only one output can be activated at one time.

The user can adjust the gain of the audio outputs with the volume control buttons. The Handset Speaker is driven by Atlas-UL's internal SPKR differential amplifier. The headset uses a standard mini-USB connector. The headset may contain a momentary switch, which is normally open and connected to the USB ID line. When the momentary switch is pressed, the ID line is shorted to ground. The phone will detect this action and make an appropriate response, which could be to answer a call, end a call, or dial the last number from scratchpad. The Alert Transducer is driven by Atlas-UL's ALERT/Speakerphone amplifier (A1).

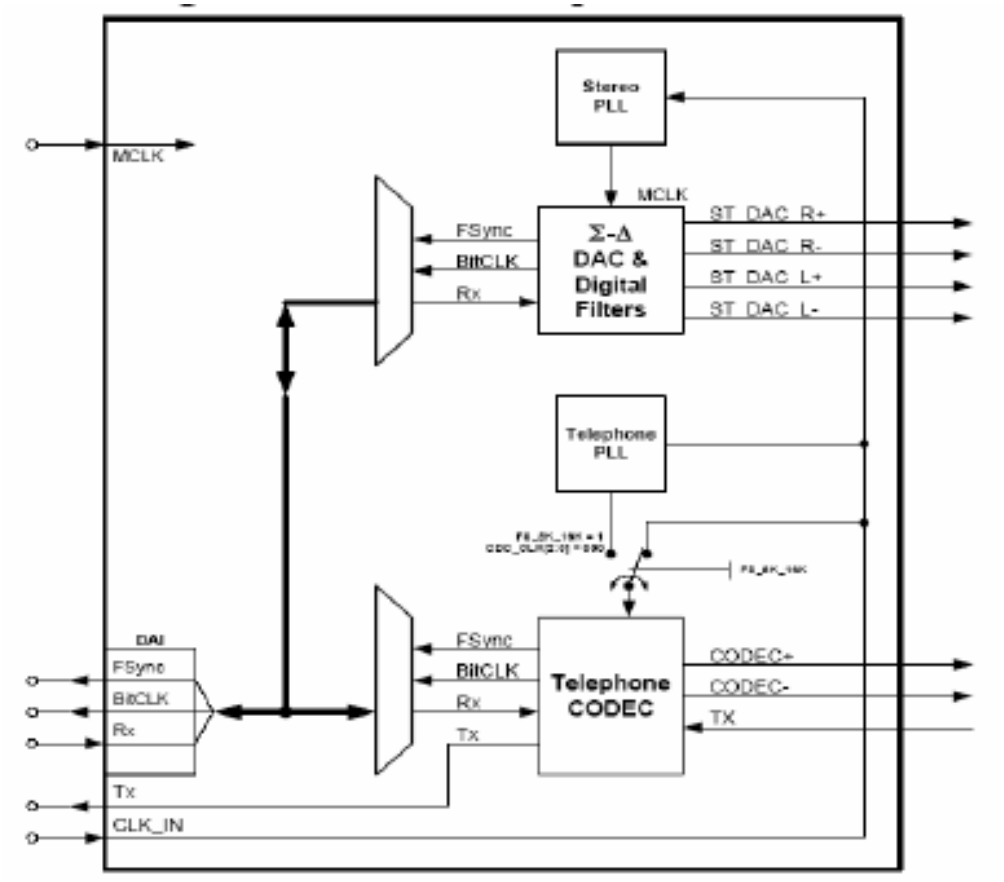

Figure 8. Atlas-UL RX-Audio

4 NEPTUNE LTE2 – MCU/DSP

The Neptune LTE2C90 Baseband IC is a digital baseband processor. The design is derived from HiP7 Neptune LTE with changes to process, memory configuration, and several module enhancements. It is a dual-core processor that contains a Synthesizable Onyx DSP core (56600), an ARM7TDMI-S microcontroller, and custom peripherals. Neptune LTE2C90 is configured for EDGE applications.

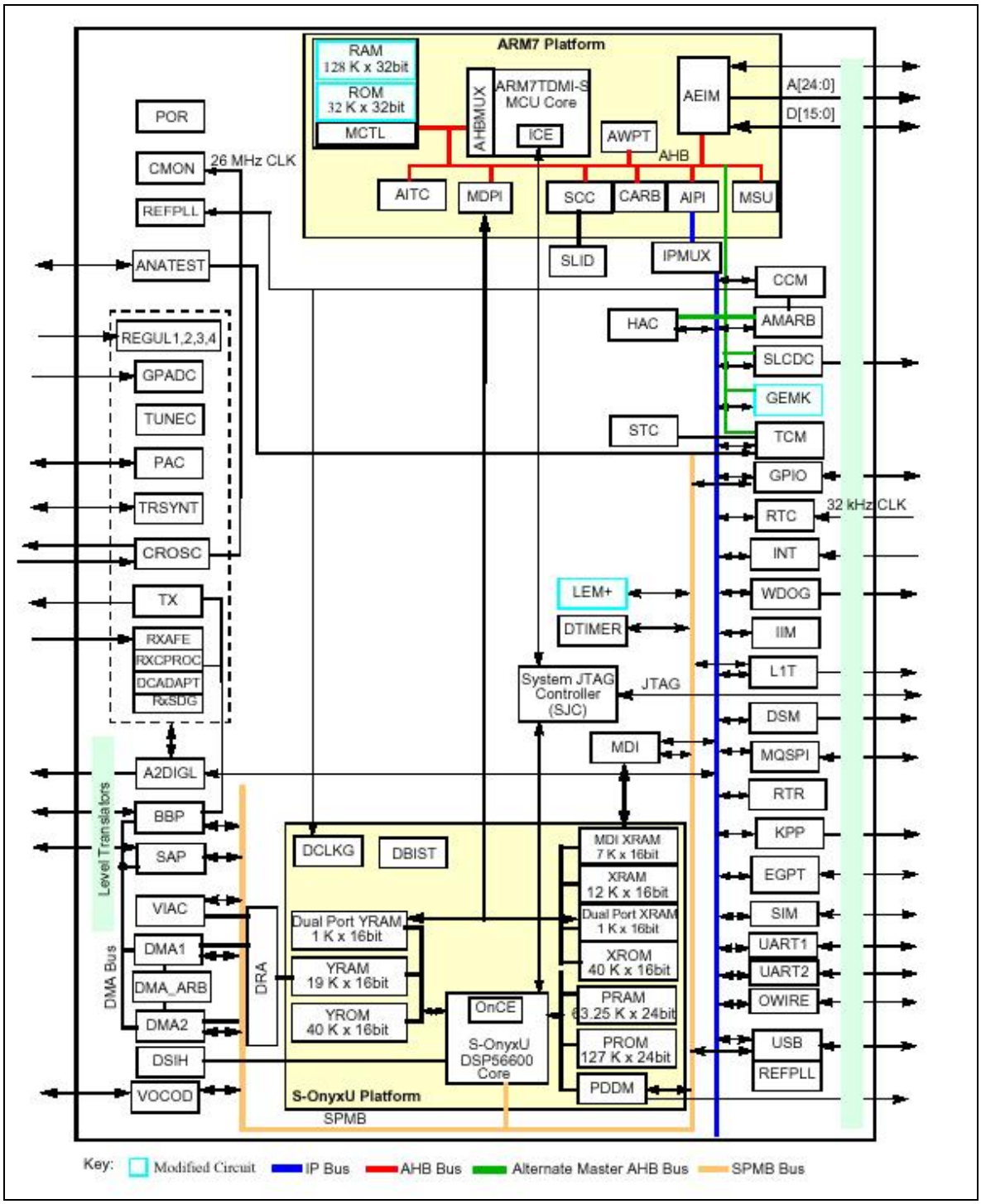

Figure 9. Neptune LTE2 C90 Block Diagram

4.1 Smart Liquid Crystal Display Controller (SLCDC)

Display memory access controller (DMAC) module is replaced by smart liquid crystal display controller (SLCDC) module in LTE2. Apart from the normal functions that DMAC provides, SLCDC can also perform read-back from the LCD through the IP registers. The LCD data bus is now bi-directional. 3 new pins have been added - LCD_OEB, LCD_WEB and LCD_CS. Pin names for LCD_SDATA and LCD_CLK are changed to LCD_DATA[7] and LCD_DATA[6] respectively. The SLCDC can be configured to write image data to an external LCD controller via a 4- line serial, 3-line serial, an 8/16-bit parallel or 6/9/18-bit parallel interface.

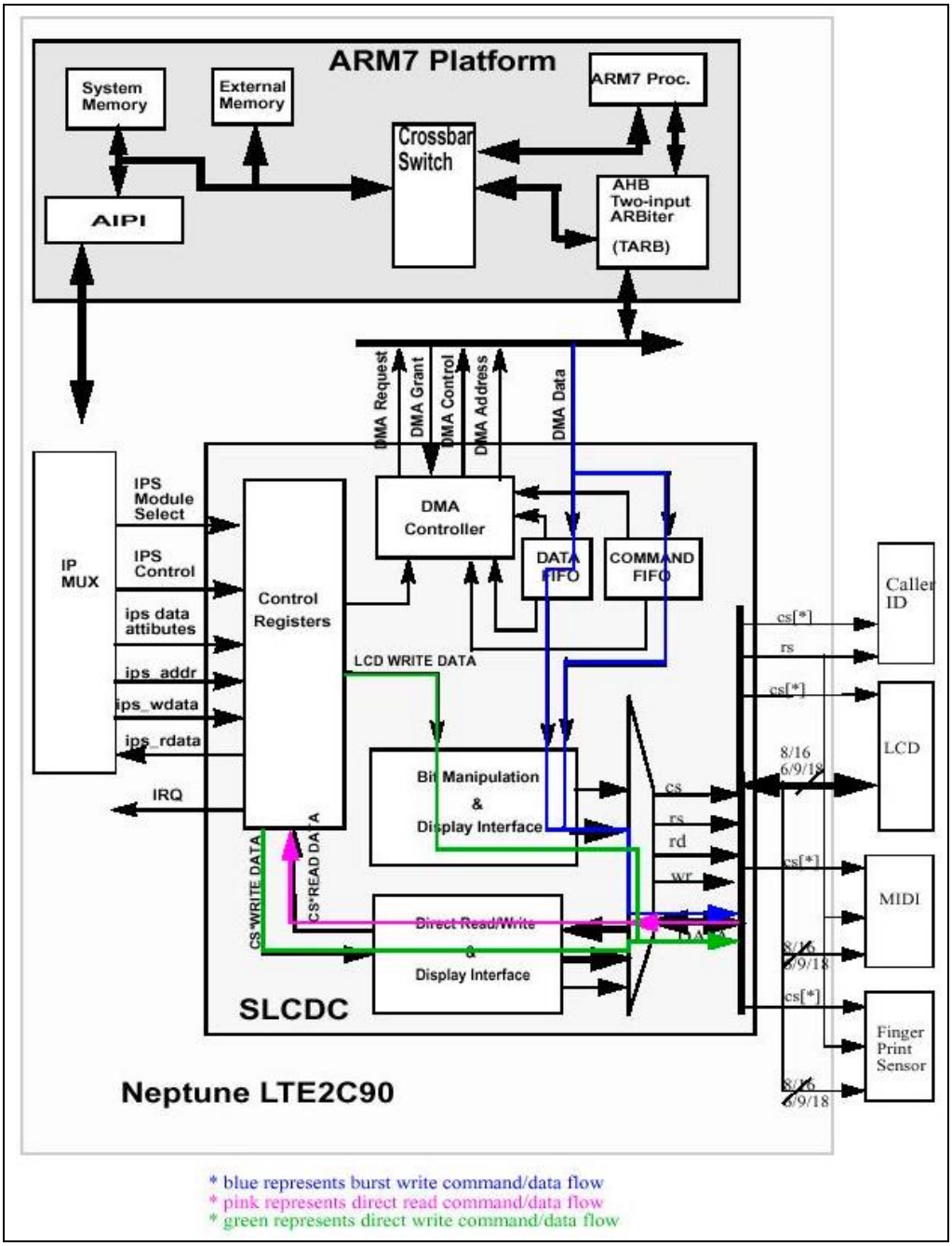

Figure 10. SLCDC System Diagram

4.2 Memory Interface

The external memory is a 512-Mbit (256Mbit + 256Mbit) NOR-Flash memory with 128Mbit PSRAM packaged in a single die stack part.

Neptune LTE2's AEIM will be interfaced to the stacked memory device and consists of the external address lines, data lines, chip selects, and memory control lines.

4.3 Keypad Interface

The Keypad Port is a 16-bit peripheral, used generally for keypad matrix scanning, or as a GPIO port up to 16 bits wide. The keypad matrix can be configured up to 8 rows by 8 columns, with unused pins as GPIO's.

Column #	Col 0	Col 1	Col 2	Col 3	Col 4	Col 5
Keypad Port (GPIO Port)	KPP/CO (PC3)	KPP/C1 (PC4)	KPP/R5 (PC8)	KPP/R6 (PC10)	KPP/R7 (PC11)	No KPP IO (PC13/SJC_MOD)

Row #	Row 0	Row 1	Row 2	Row 3	Row 4
Keypad Port (GPIO Port)	KPP/R0 (PC5)	KPP/R1 (PC6)	KPP/R2 (No PC IO)	KPP/R3 (No PC IO)	KPP/R4 (PC7)

Table 5. Columns and Rows Assignment

In Pemba, all rows will be set as inputs at all times, and the columns will be set as outputs driven low when there are no key presses detected. Pressing a key will short a row to a column, driving the row low and generating an interrupt to the processor. At this point, all columns will be set as inputs and progressively scanned low (set as an output driven low in a sequential fashion with only one column driven low at any point in time) to determine the key that is pressed.

The key mappings used in Pemba are listed in Table 6 below.

	Col 0 (KBC0/PC3)	Col 1 (KBC1/PC4)	Col 2 (KBR5/PC8)	Col 3 (KBR6/PC10)	Col 4 (KBR7/PC11)	Col 5 (SJC_MOD/PC13)	Row 0 (KBR0/PC5)	Row 1 (KBR1/PC6)	Row 2 (KBR2)	Row 3 (KBR3)	Row 4 (KBR4/PC7)
6	X						X				
8	X							X			
7	X								X		
2	X									X	
4	X										X
NAV-RIGHT		X					X				
NAV-DOWN		X						X			
9		X							X		
NAV-UP		X								X	
NAV-LEFT		X									X
VOL DOWN			X				X				
Smart (for PTT). Camera (for Non-PTT Model)			X					X			
VA			X						X		
SEND			X							X	
VOL UP			X								X
NAV-CENTER				X			X				
Message				X				X			
Contacts				X					X		
0				X						X	
#				X							X
5					X		X				
*					X			X			
1					X					X	
3					X	X					X
Carrier 1 / Browse						X	X				
Carrier 2/Clear						X		X			

Table 6. Key Mappings

5 ATI W2282 Multimedia Co-Processor

ATI W2282 is a member of ATI's family of media processors specifically tailored for mobile camera phone applications and the support of multimedia messaging services (MMS) as defined by 3GPP. It integrates stand-alone and high performance video decoding and encoding capabilities, an advanced 2D graphics engine, hardware audio support for a variety of audio codecs, as well as a camera sub-system processing engine to support high resolution sensors. Powered by the highly optimized IMAGEON™ architecture, handheld devices will benefit from ultra low power dissipation and, therefore a much longer battery life.

The IMAGEON™ 2282 offers complete self-contained video and audio processing – an ideal for MMS-capable handsets, and enables multimedia-rich applications, such as high quality video recording or playback, two-way video conference, multimedia audio capabilities, powerful mobile gaming and digital still camera replacement. End-users will enjoy the ultimate visual experience using their IMAGEON™ 2282 powered handsets.

5.1 System Block Diagram

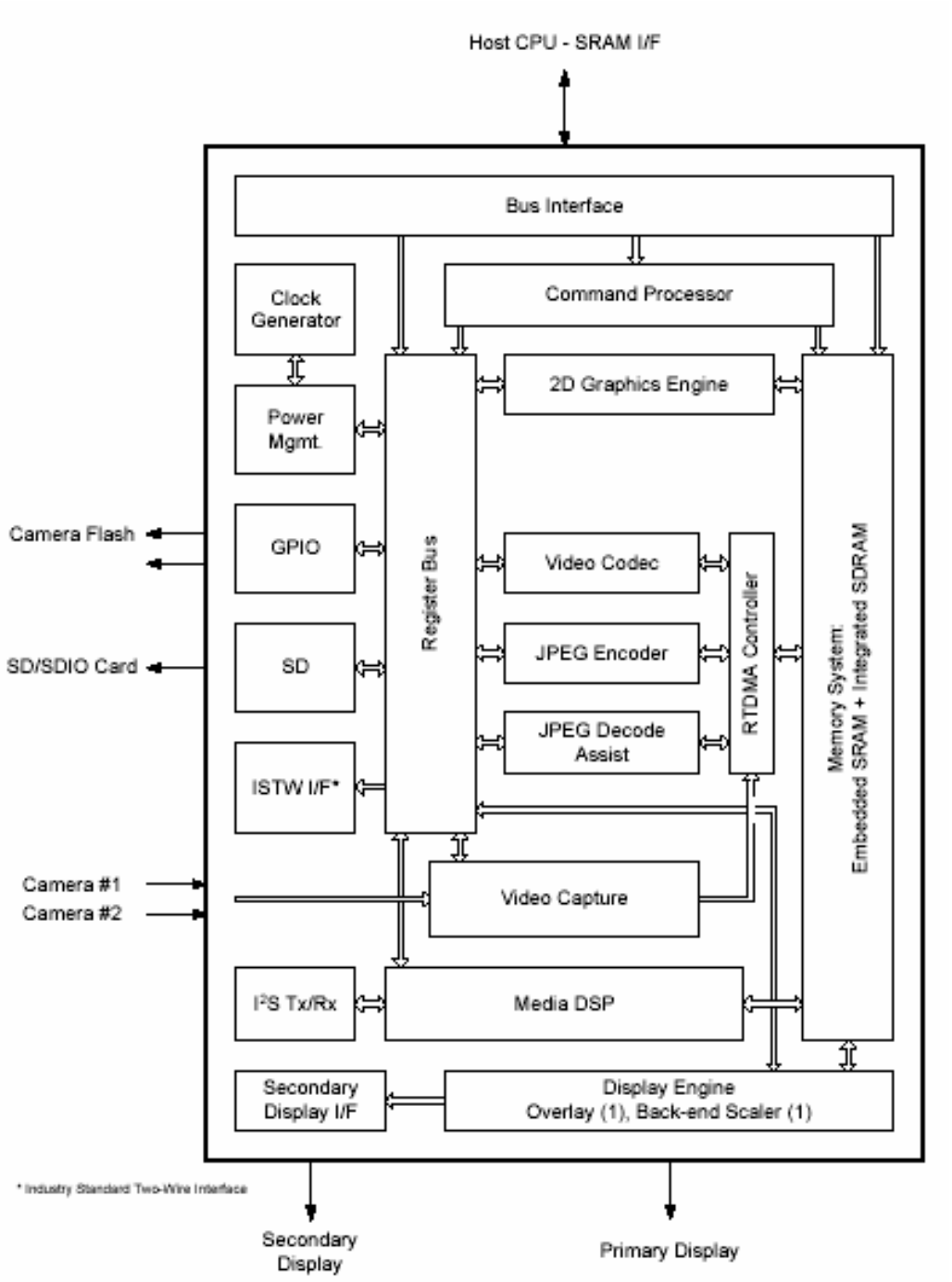

Figure 11. ATI WW2282 System Block Diagram

ATI W2282 supports smart display. Unlike a typical TFT or STN display that requires the image to be refreshed regularly, a smart display is able to self-refresh with an on-board SRAM. The images are transferred only on demand basis under the control of the driver software. As a result, this frees up the main processor for other tasks.

5.2 Port and Display Configurations

The W2282 supports the following display configurations:

- One TFT display, one secondary 1/8-bit CLI port.
- One primary 1/8/16-bit CLI display, one secondary 1/8-bit CLI display.
- One primary 1/8/16-bit CLI display, bypass mode supported on secondary port.

Pemba will be using the TFT configuration, with TFT display as a primary display and adds an external CLI display as a secondary display.

5.3 Display

5.3.1 Main Display

The main display for Pemba will be a 176 x 220 TFT 256K color display. It will be connected to ATI W2282 through the LCD electrical interface (i.e. 18-bit LCD bus+ control). The signal to reset the display is ATI GPIO5. It will assert a LOW signal when resetting the display. To reset ATI2282, PC0 from Neptune need to be asserted to LOW. The TFT Driver will be uPD161981 (SHARP) & S6D2239 (SEC).

5.3.2 CLI Display

The external CLI display for Pemba is a 96x80, 16-bit colour LCD.

6 Backlighting System

6.1 Display Backlight

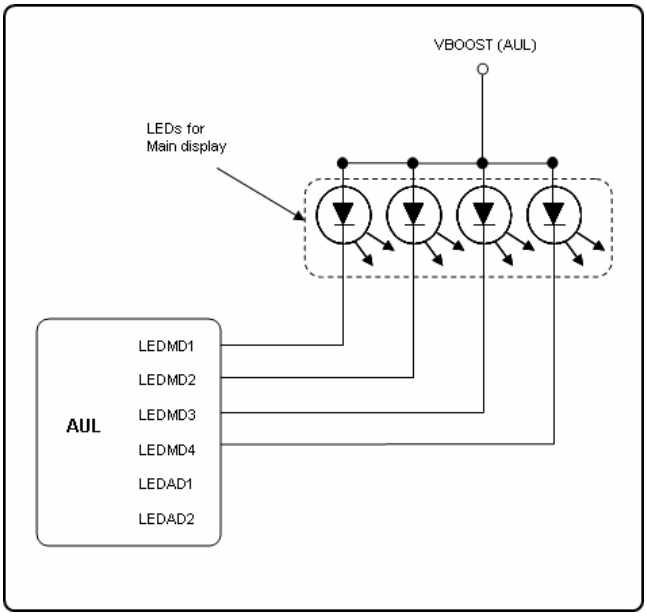

Figure 12. Backlight Configuration

Pemba will have 4 LEDs for display lighting, connected to the backlight drivers of AUL. The LEDs are connected to the backlight main display LED drivers (LEDMD1 to LEDMD4).

The display backlight drivers will be in controlled current mode. The display backlight scheme does not require any PWM drivers.

Currently, when Pemba is either in flip opened or closed mode, the LEDMD1 to LEDM4 drivers are being turned on for backlight leakage to CLI display.

6.2 Keypad Backlight

Pemba will be using EL lamp for keypad backlighting.

The Neptune will enable the EL Driver through TOUT10 (PA7) which is an active high input. The EL driver will light up the EL Lamp.

Figure 13. EL Backlight for Keypad

7 Camera

Pemba uses the 1.3MP camera with Micron sensor SOC1320. The sensor is a color CMOS sensor with RGB pattern filter, It consists of a minimum of 1280 active horizontal pixels & 1024 active vertical pixels. In addition, it supports auto exposure, auto white balance & color conversion. This device can provide images at up to 15fbps for both image & video capture.

8 Removable Memory Storage - MicroSD

Pemba is supporting removable memory storage in the form of SanDisk & Toshiba MicroSD memory card. The SanDisk & Toshiba MicroSD card are hereafter named as MicroSD card. The MicroSD card is a NAND flash based memory card with a form factor of 11mm x 15mm by 1 mm. When used with SD Adapter, the MicroSD card is compatible with all existing SD card applications (i.e. PC, digital camera, MP3 player, etc)

The MicroSD card communication is based on an 8-pin electrical interface and it supports Secure Digital (SD) protocol (the same communication protocol used by SD Cards) as well as SPI protocol. For Pemba, the SD protocol will be used for communication between ATI W2282 and MicroSD card.

Seven different memory capacities are supported, i.e. 32MB, 64MB, 128MB, 256MB, 512MB 1GB & 2GB, with their corresponding Motorola component part number (including adaptor) shown below:

Capacity	Motorola P/N	Capacity	Motorola P/N
32MB	SYN 1401	256MB	SYN1404
64MB	SYN1402	512MB	SYN1405
128MB	SYN1403	1GB	SYN1406

Table 7. MicroSD Part Number

8.1 MicroSD Pin Assignment

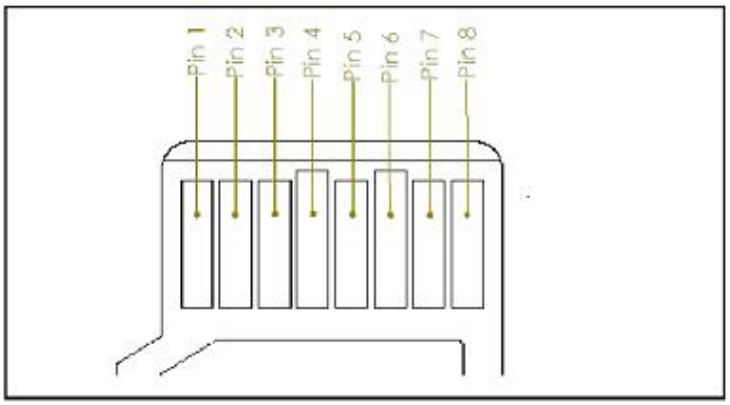

Figure 14. MicroSD Card Pin Asignment

Pin No.	Name	Type1	Description
1	DAT2	I/O/PP	Data Line [Bit 2]
2	CD / DAT3	I/O/PP	Card Detect / Data Line [Bit 3]
3	CMD	PP	Command / Response
4	VDD	S	Supply Voltage
5	CLK	I	Clock
6	VSS	S	Supply Voltage Ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1	I/O/PP	Data Line [Bit 1]

Table 8. MicroSD Protocol Pin Definition

[1]Key: S = Power Supply; I = Input; O=output using push-pull drivers; PP = I/O using push pull driver

8.2 System Interface

Figure 15 below depicts the interface of the MicroSD card to the phone system (Neptune LTE2 and System Memory).

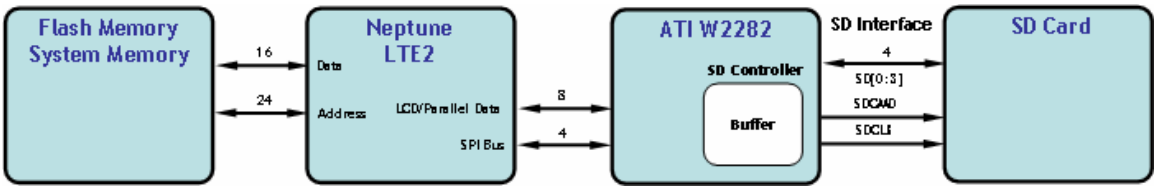

Figure 15. Block Diagram of MicroSD data transfer

8.3 MicroSD Detailed Interface

The LDO (LP3987) supply power for the microSD card. The SYSCLK_EN (STANDBY of AUL) can set the LDO into standby mode. The A12 signal from LTE2, if software enabled, can be used to shut down the LDO to save another 20uA from standby mode.

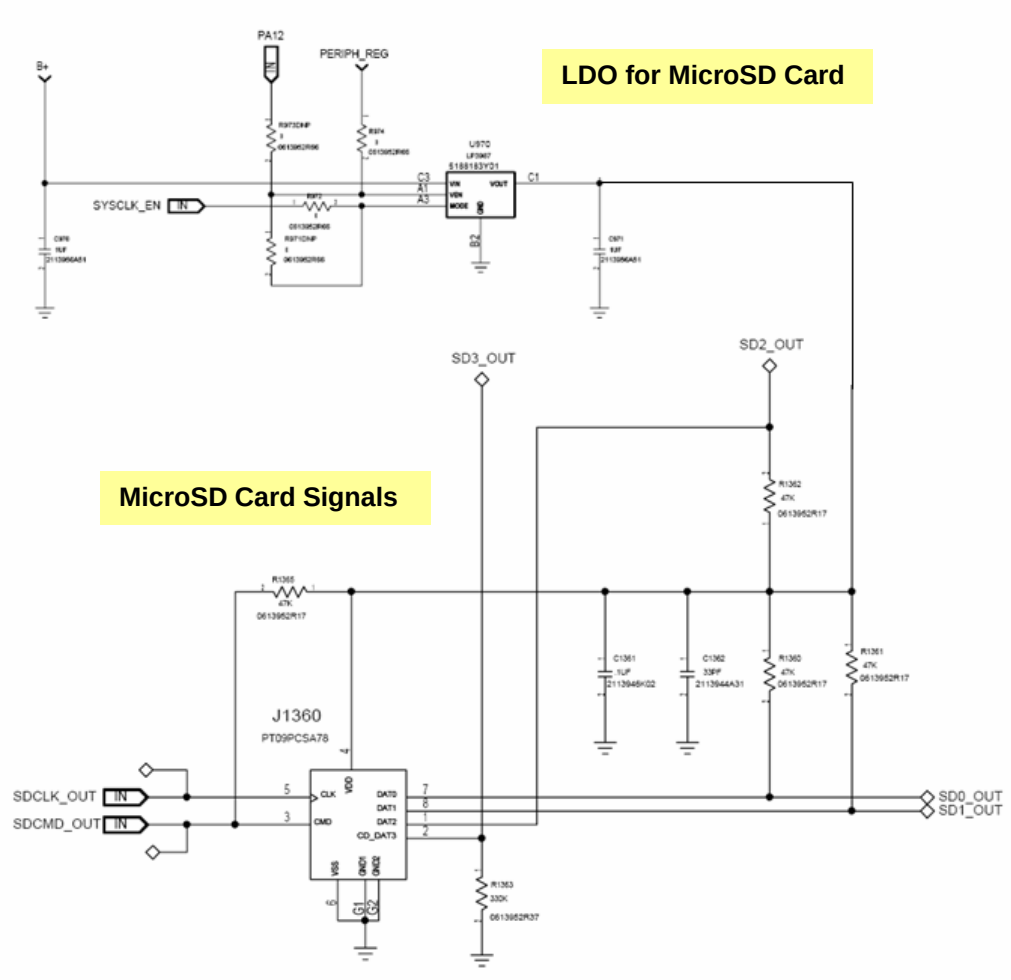

Figure 16. Detailed MicroSD Schematics

8.4 MicroSD Card Detection

Card detection scheme in Pemba is by means of sensing state of Pin2 (DAT3/CD) on the MicroSD interface. By default, after power-up, there is a 10k-90k resistor connected to pin2 and is placed as input mode.

This pull-up resistor on the card can be disconnected / connected by using the SET_CLR_CARD_DETECT (ACMD42) command. When no card is connected, the ATI 2282 will sense a logic “0’ on this pin. When a card is inserted, ATI 2282 will sense the logic “1” on this pin, and if programmed, can send an interrupt to Neptune to indicate card insertion detect. Likewise is for card removal.

Card detection can bring the ATI 2282 out of suspend mode.

9 SIM / MMSIM Interface

Pemba hardware (PCB layout) has made provision for a MegaSIM card holder (though not supporting it), to allow easier migration to support MegaSIM (probably a refresh) should there be a need in future, and when the detailed electrical interfaces to the existing circuitry are locked down or finalized.

Figure 17 below shows the differences between a conventional SIM and MegaSIM signals.

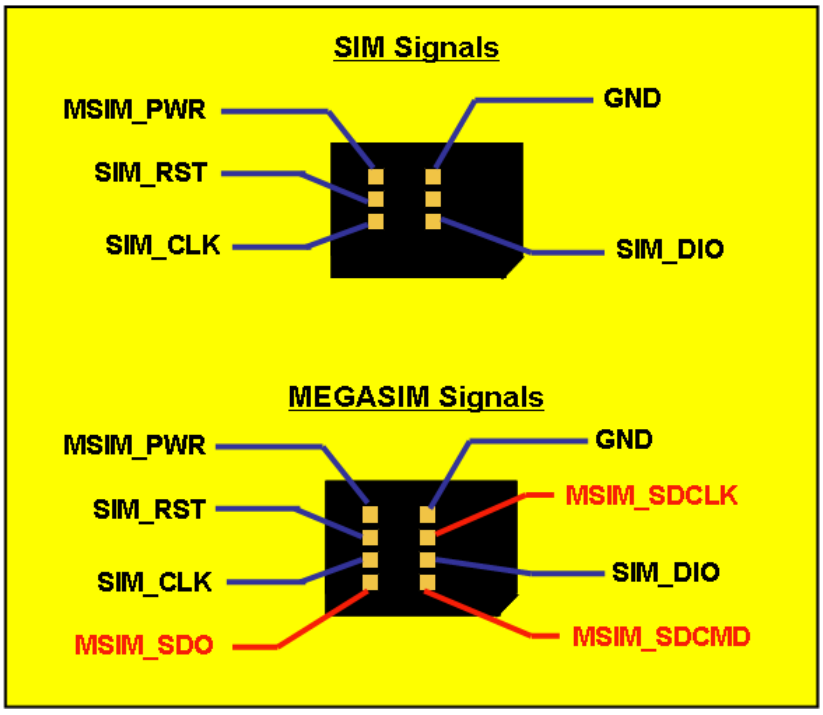

Figure 17. Normal SIM and MegaSIM Differences

*** MegaSim has normal SIM plus MMC interface*

Pin No	Name	Description
1	GND	Ground
2	SDCLK	SD Clock
3	SIM_DIO	SIM Data I/O
4	SDCMD	SD Command/Response
5	SD0	SD Data Line[Bit 0]
6	SIM_CLK	SIM Clock
7	SIM_RST	SIM Reset Line
8	MSIM_PWR	Supply

Table 9. Signal Description

*** MMC Clock: 13MHz to 20MHz*

10 TI6150 Bluetooth Chipset

Pemba incorporates the TI Bluetooth solution into the overall hardware design, instead of BCM2035. This design is based upon a Texas Instruments (TI) BRF-6150 single-chip 0.13-µm CMOS Bluetooth solution. This solution will utilize an embedded ARM7 base-band microprocessor and an on-chip Digital Radio Processor (DRP) functioning as the integrated 2.4GHz transceiver. The IC will also comply with Bluetooth Core Specification v1.2 and will function as a Power Class II (+4 dBm) Bluetooth device.

The TI solution brings the following advantages to the program over the BC solution:

- Lower power consumption
- Lower cost
- Smaller size

10.1 System Block Diagram

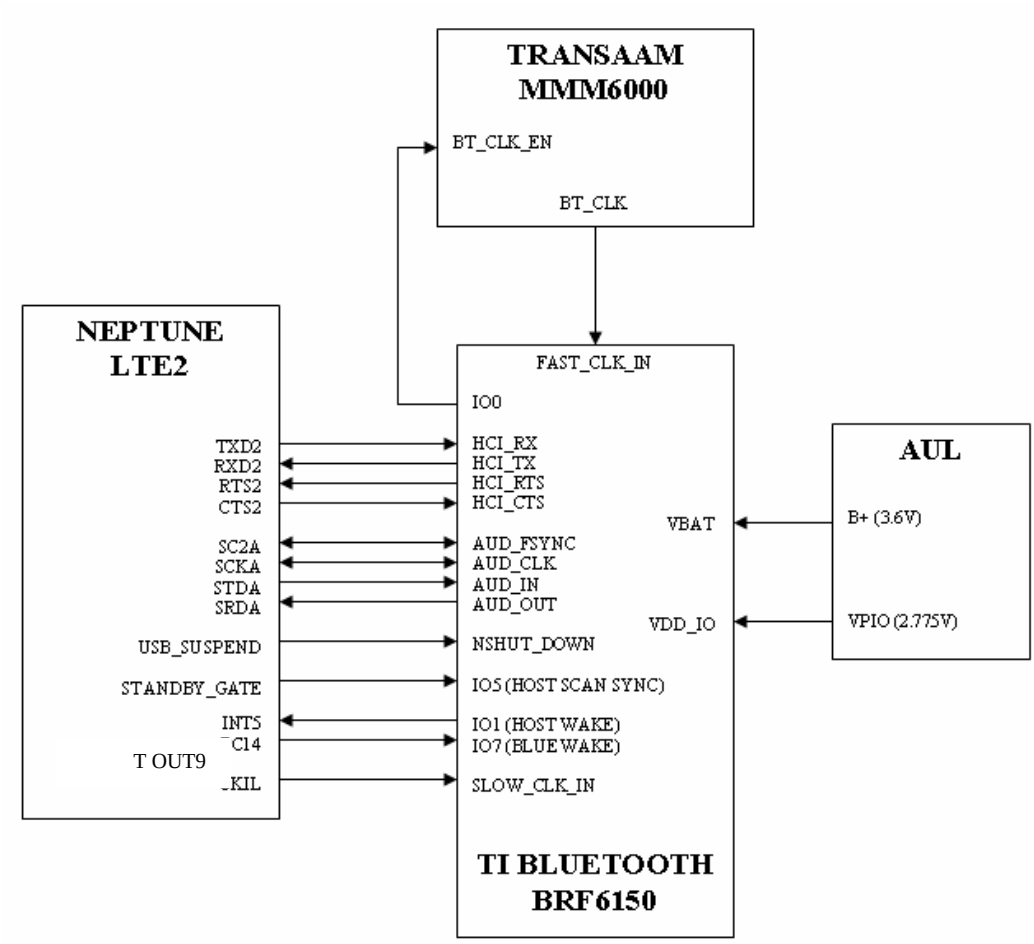

Figure 18. System Block Diagram for Bluetooth

10.2 Bluetooth v1.2 Support

The new features of BT v1.2 which are supported by TI BRF6150 are:

- Faster connection
- Adaptive frequency hopping including master and slave classification
- Extended SCO - all new packet types
- Synchronization
- LMP improvements
- Quality of service improvements

10.3 Bluetooth Reference Clock

The BT reference clock signal is 26MHz from TransAAM, MMM6000

10.4 Six Wires Interfaces

Apart from the standard UART interface which consists of TX, RX and flow control lines RTS, CTS there are extra lines for BLUE_HOST_WAKEB and BLUE_WAKEB. The BLUE_HOST_WAKEB line indicates to the Host device that the BRF6150 device wishes to communicate. The BLUE_WAKEB line indicates to the BRF6150 device that the host wishes to communicate.

This new interface between BRF6150 device and the host will allow each side to go to sleep independently and thereby save the extra current consumption in situations where there is no need to send data to host such as page scan or inquiry scan.

New sleep protocol includes

- Host wakes up BT controller to transmit
- BRF6150 device wakes up without data to send to host
- BRF6150 device wakes up and wishes to transmit to host
- BRF6150 device & host awake & communicate, host ends transmit sequence