Service Manual

Level 3

Draft 1.0

MOTOROLA

DIGITAL WIRELESS TELEPHONE

Model V975/V980

UMTS 2100MHz/PCS 1900MHz/DCS 1800MHz/GSM 900MHz

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3G Flash Procedures

Introduction

This document is intended to describe the flashing (firmware upgrade) procedures for 3G terminals. The 3G terminal described in this document will be limited to the V975, V980, C975, and C980.

Firmware upgrades need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the firmware upgrade application database is up-to-date.

Firmware upgrades allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific circumstances, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the 3G terminal.

Power Hardware

1. Fully Charged battery (SNN5743A or equivalent)

2. Full-rate Charger (SPN5049 or equivalent)

Interface Options

1. USB Data Kit (S8951)
   USB Cable (SKN6311A)
   Data Software CD

Software Requirements

The RSD (Remote Software Download) General Release is used to allow functions such as firmware upgrade, Phone Swap, and Multi-refurbish. Contact your local Motorola service representative to receive download information for the RSD and related support files. Also insure that the RSD database has the latest update.

Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1-1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a nonfunctional (Bricked) 3G terminal.

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery
2. Full-Rate Charger w/battery (recommended)

If the user decides on using the battery only solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the flash process. This action may cause unrecoverable failures to the 3G terminal.

RSD Firmware Upgrade Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal.

1. Launch the RSD General application
2. Connect the unit as illustrated in figure 1-1.
3. Power up the 3G terminal
4. If the 3G terminal doesn't power up, refer to the Force Flash section.
5. Once the phone is fully powered up, the Radio Information Panel will be updated.
7. In the Utilities Panel, select Firmware Upgrade.
8. In the Main information Panel, select desired restore and logging options
9. In the Main information Panel, click on the Start button to begin Firmware upgrade.

NOTE: DO NOT interrupt any hardware connections during the flash process. Connection interruptions may cause the flashing process to fail and render the 3G terminal non-operational.

10. When the process is complete, the Main Information Panel will indicate whether the process was successful. At this time you may safely disconnect the 3G terminal.
11. Power up the 3G terminal to insure that the flash procedure was successful.

Figure 1-1. RSD Hardware Configuration

Figure 1-2. RSD General Release GUI

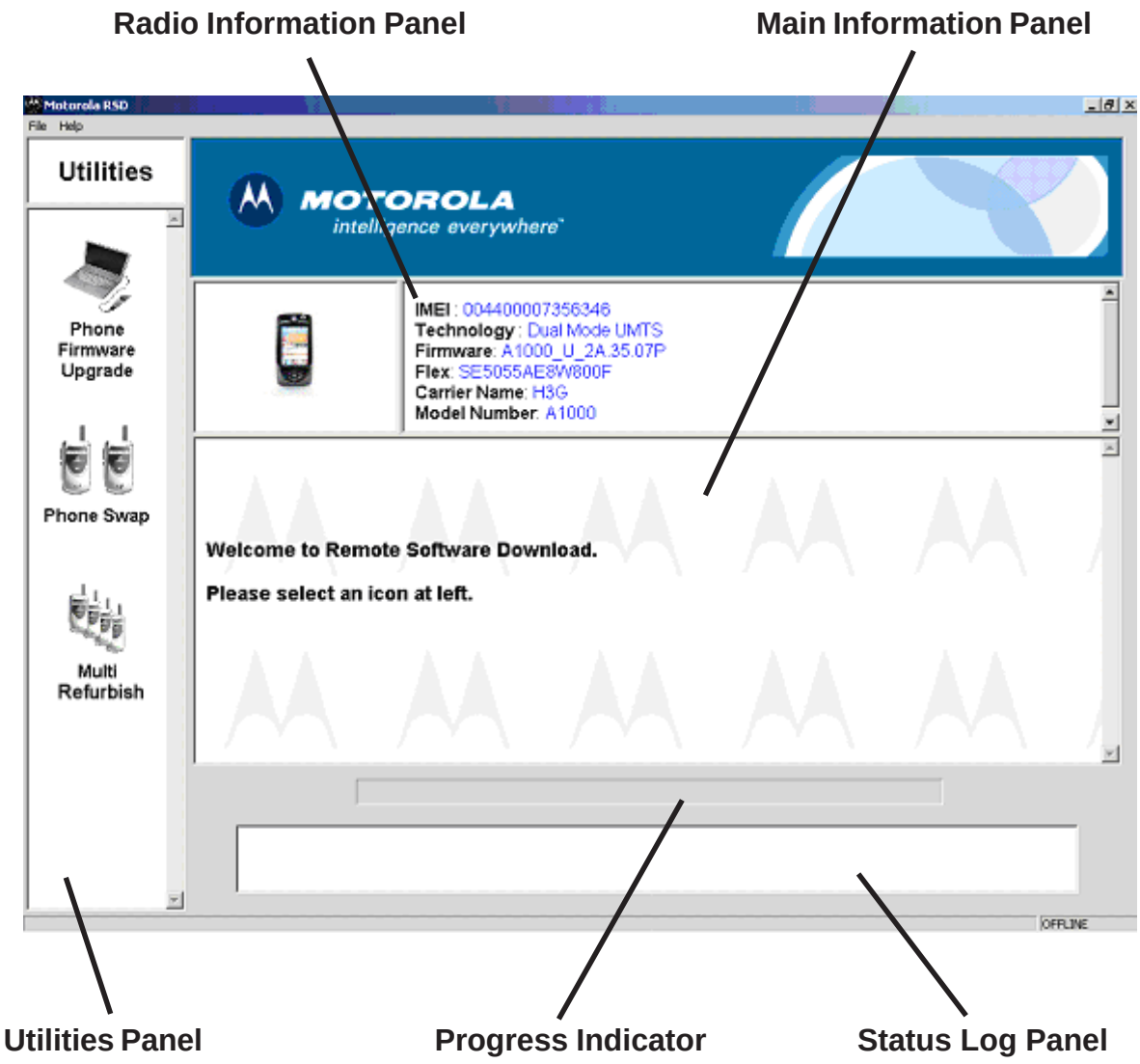
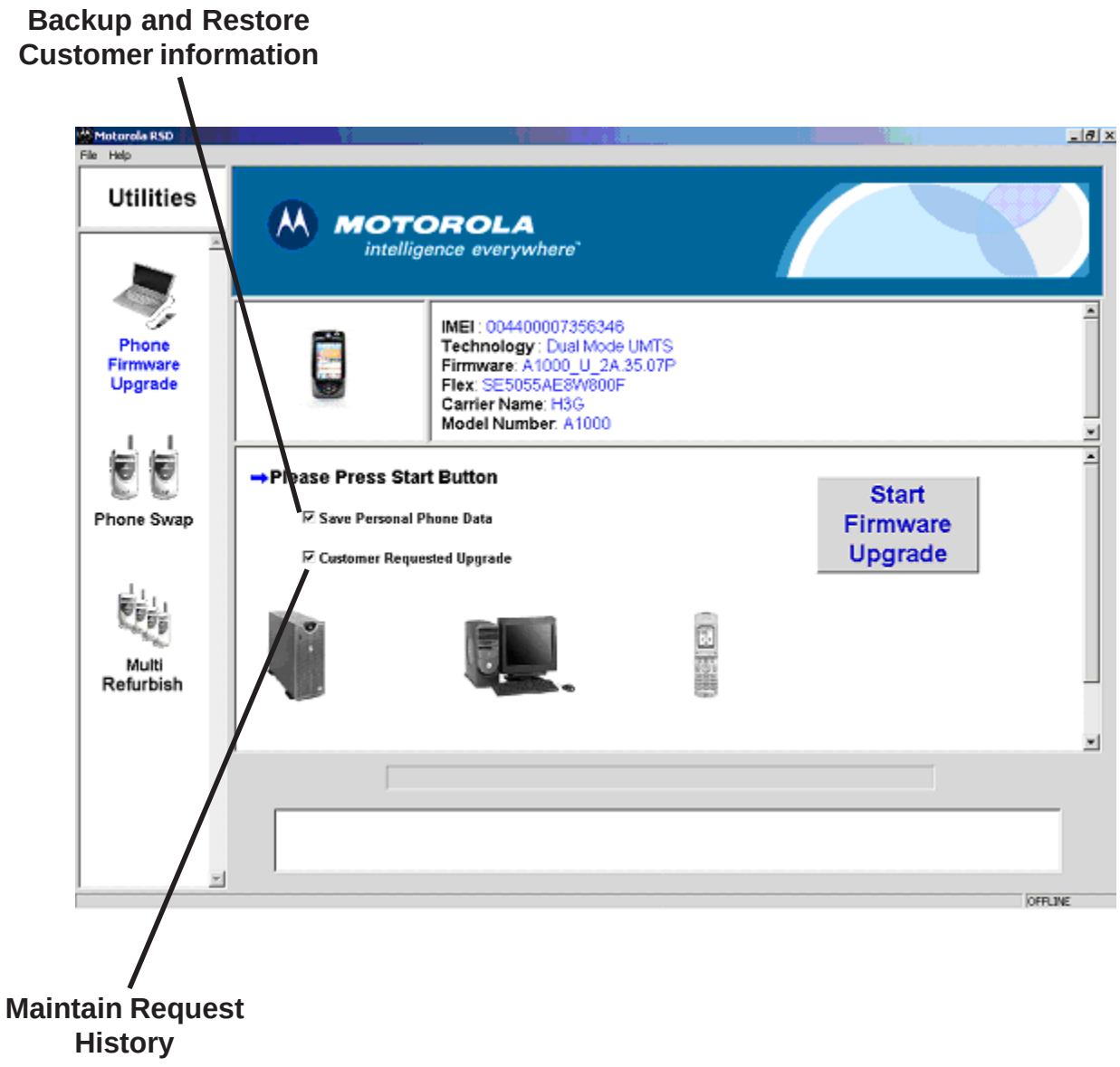


Figure 1-3. Firmware Upgrade



Force Flash Procedures

The procedures described in this section apply only to situations where the 3G terminal will not initiate it's normal power up sequence, but may recover functionality by a repeat flash procedure.

There are two possible alternatives to place the 3G terminal in force flash mode.

Key Hold Solution

Hardware: Refer to Figure 1 (USB solution)

Step 1. Remove the battery from the 3G terminal

Step 2. Prior to connecting the USB cable, press and hold "#" and "*" keys from the 3G terminal

Step 3. Attach the USB cable

Step 4. Verify that the RSD application detects the 3G terminal, if it's not detected, press and hold the gaming keys once again.

Force Flash USB Cable Solution

Hardware: Refer to Figure 1-1 (USB solution), except, replace USB cable (SKN6311A) with force flash cable (SKN6168A)

Step 1. Connect the force flash cable in the same manner described in Figure 1-1.

Step 2. The 3G terminal will automatically be placed in force flash mode. There's no need to press the power key. The RSD application will now detect the 3G terminal

Manual Test Procedures

Introduction

The phone allows computer controlled testing of various test parameters.

This chapter includes the computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

Non-Signaling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signaling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The phasing parameters are stored in an EPROM in the transceiver board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted (phased) with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5743A[1] or equivalent)
- Full-Rate Power Supply (SPN5049A[1])
- Battery Eliminator (5-00-3Y-12000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

RF Interface

- RF Adapter (2-00-4E-10000[2])
- SMA/N type Adapter (0-00-00-40042)
- SMA Cable 0.5m (0-00-00-40047[2])
- USIM (0-00-00-40810[2])

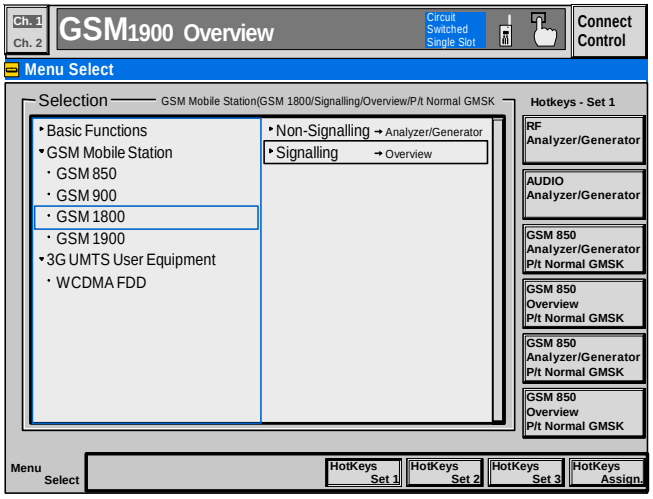
[2]Contact AMS Software and Elektronik GmbH for ordering

Call Origination

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

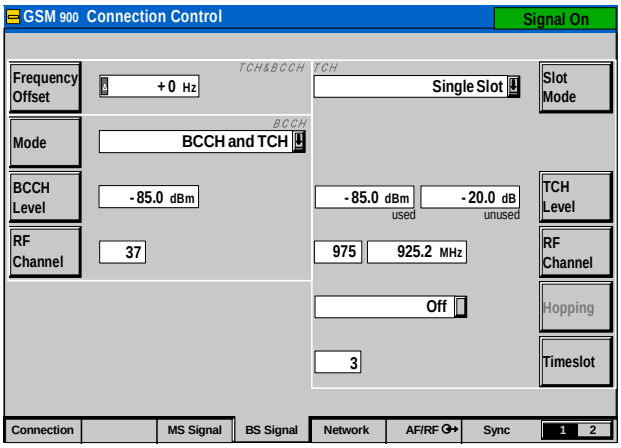
1. Install the test USIM in phone.
2. Connect hardware as illustrated in figure 2-5.

Figure 2-1. GSM Signaling Setup



3. Setup up the test box for GSM, DCS, or PCS Signaling
4. Set Broadcast Channel (BCH) to 120 (GSM), 700 (DCS), or 661 (PCS)
5. Set Broadcast channel level to -85dBm
6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS/PCS)
7. Set Traffic channel level to -85dBm
8. Wait until the phone indicates a receive signal

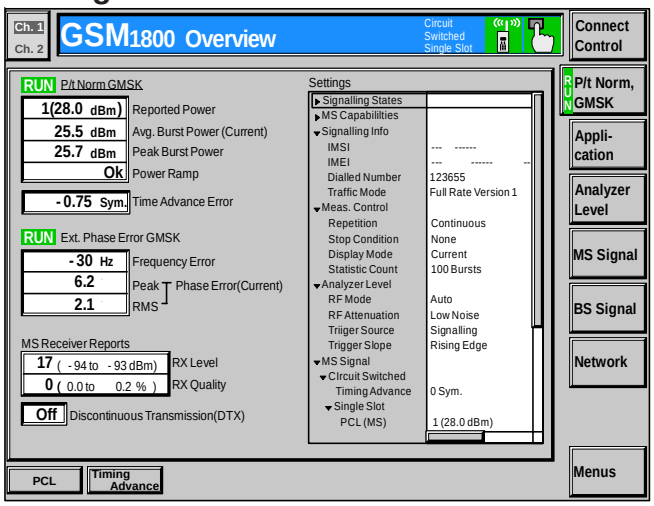
Figure 2-2. GSM Connection Control



9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 2-3. GSM Call Connected



Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-1. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	27	31	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 2-2. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

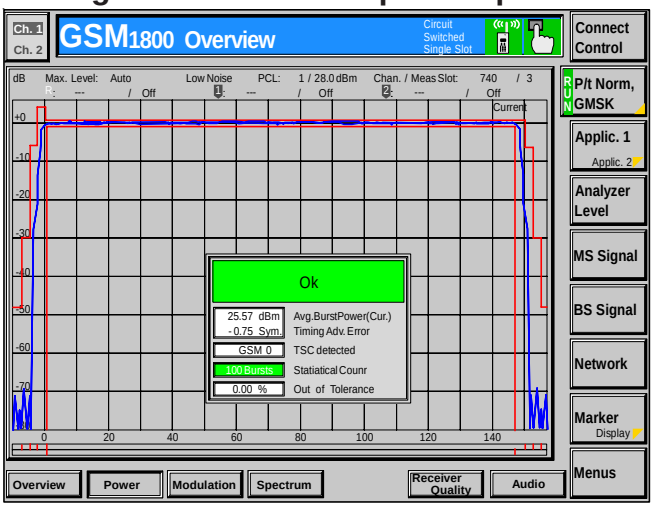
[1]Power Level = 15
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 2-3. PCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 15
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Figure 2-4. Burst Output Shape



Burst Output Shape should fall within the standard limits of the Power Ramp.

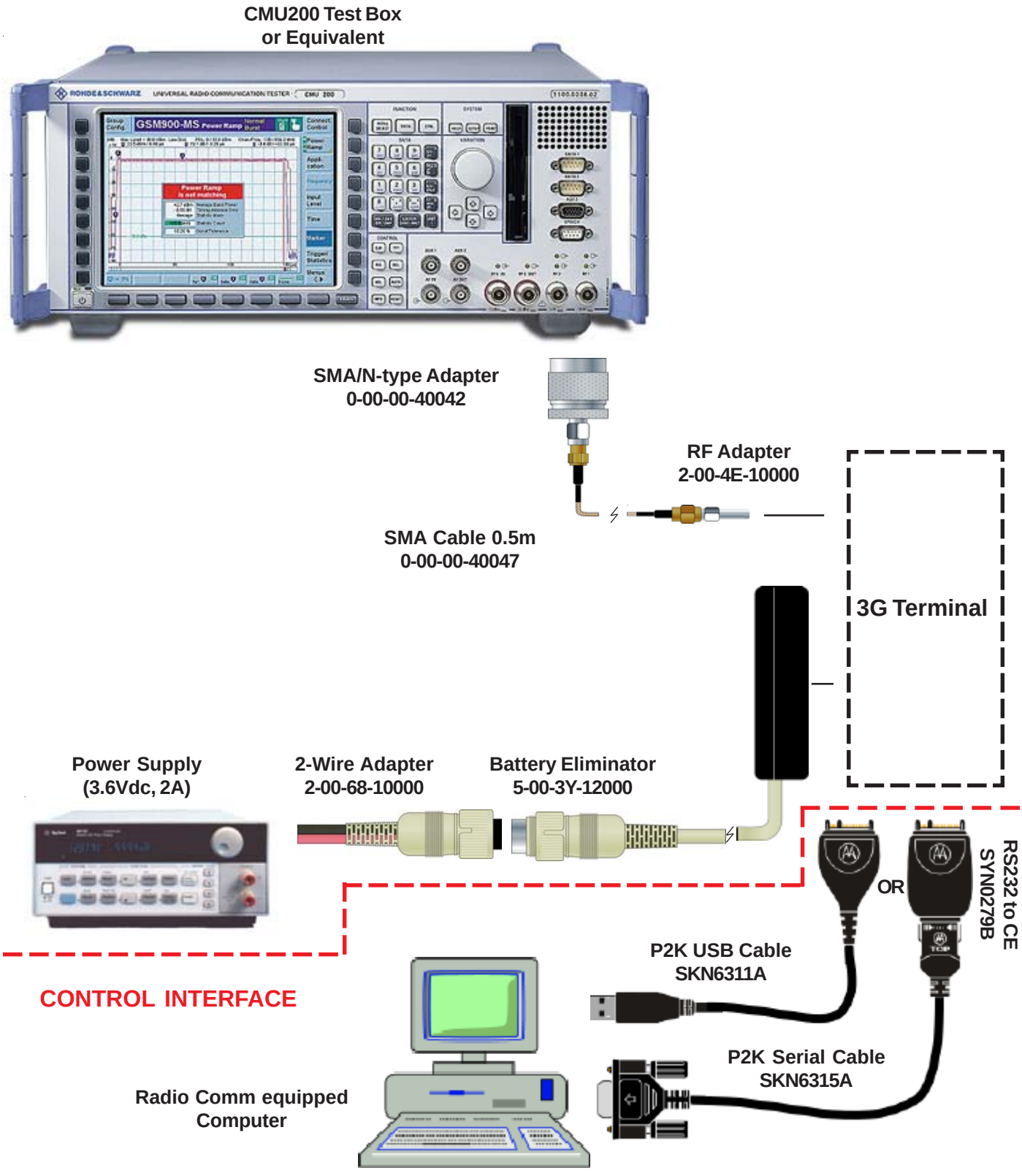
BER measurements is only required if RX Quality reads a value of 4 or greater.

It is recommended that handover procedures be performed as shown in the following table.

Table 2-4. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

Figure 2-5. Manual Test Hardware Configuration



WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 2-5.

Software Requirements

None.

Call Origination (WCDMA)

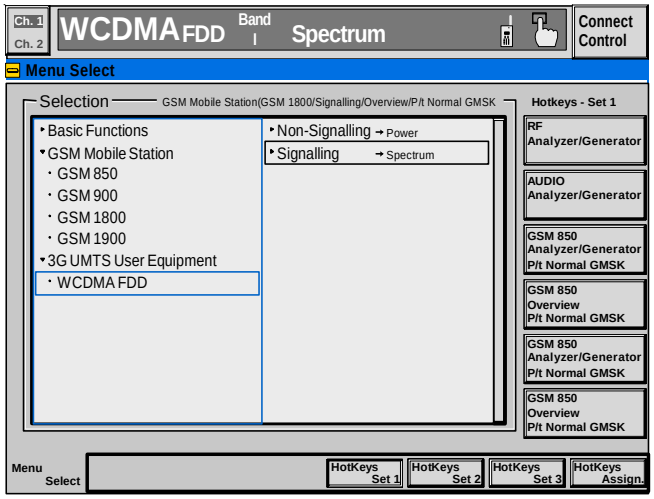
Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signaling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

Figure 2-6. WCDMA Signalling Setup

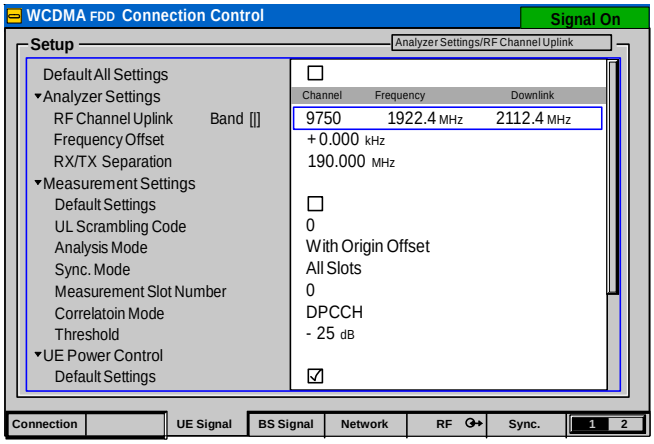


3. Setup up the test box for WCDMA FDD Signaling

4. Set UE Signal, RF Channel Uplink to 9400

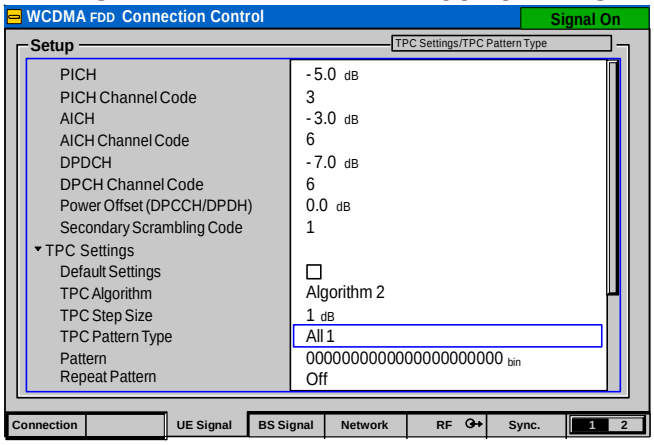
5. Set UE Signal, RF Channel Downlink to 9800

Figure 2-7. Channel Uplink(UE Signal)



6. Set TPC Pattern Type to All 1

Figure 2-8. TPC Pattern Type(UE Signal)

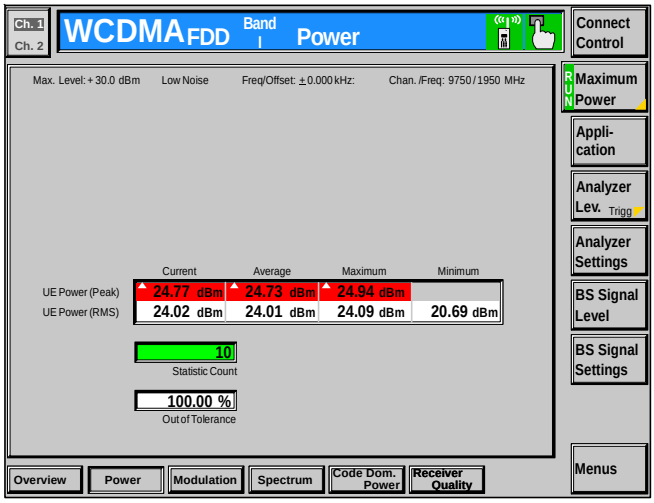


7. Wait until the phone indicates a signal

8. Dial a number from the phone and press the send button.

9. The phone is now connected.

Figure 2-9. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-5. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 2-10. WCDMA Modulation

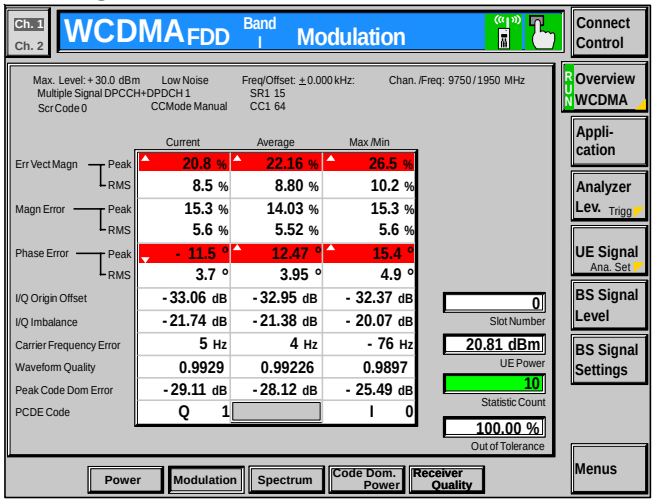
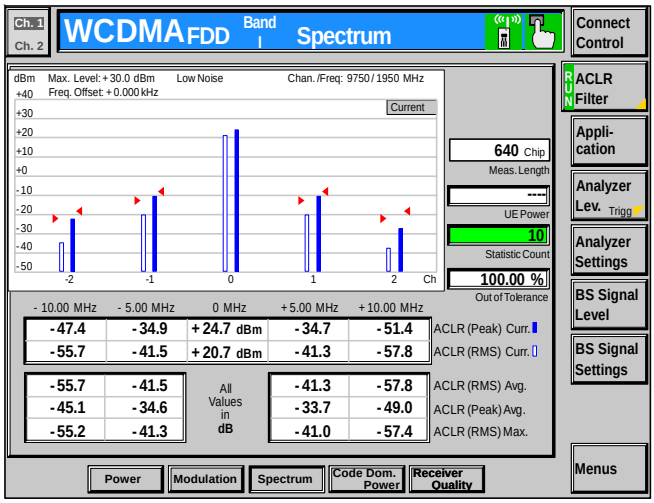


Figure 2-11. ACLR Screen



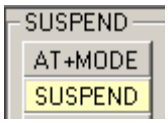
Non-Signaling Test Procedures (GSM/DCS/PCS)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands are sent using a computer.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)

Click SUSPEND (USB Only)



Hardware Requirements

Control Interface Options

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

[1]Contact your local Motorola dealer for ordering

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

Verify TX Power Output (GSM/DCS/PCS)

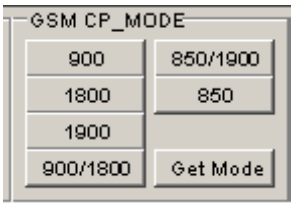
Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-6. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28.2	30	dBm
PCS TX Power Out	28.2	30	dBm

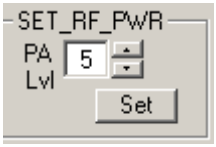
[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

Click on 900/1800 (GSM/DCS) or 1900 (PCS)

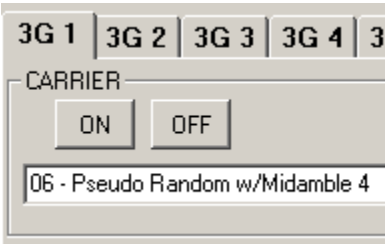


Enter 38 (GSM), 700 (DCS), or 661 (PCS) and then click Set

Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



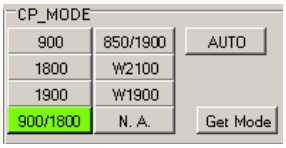
NOTE: Set Training Sequence to 4 on the test equipment.

GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

Broadcast Channel (BCH): 38
Broadcast Channel (BCH) Level: -105 dBm

Click on 850/1900 (GSM/DCS) or 1800 (DCS)



Enter Channel 38
Click INIT

Click Execute

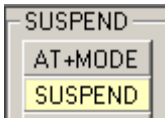
Verify return data is approximately -105 dBm

Non-signaling Test Procedures (WCDMA)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Hardware Requirements

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

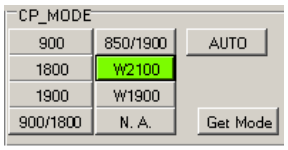
Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-7. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	19.5	22	dBm

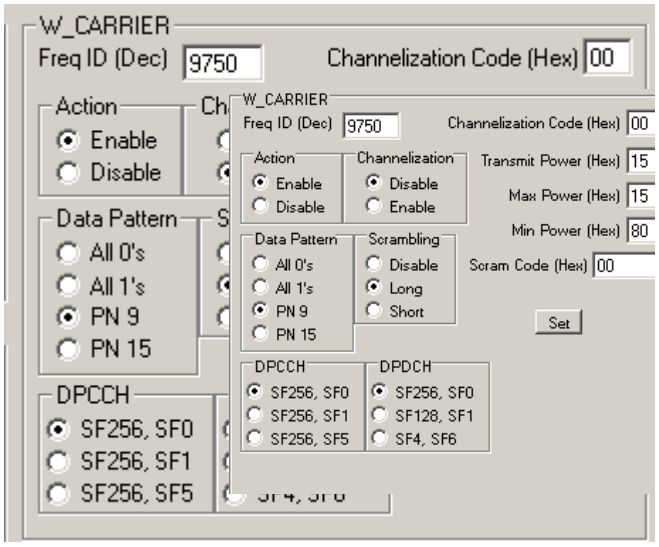
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)

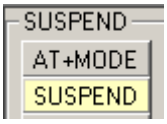


Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

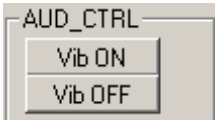
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Vibrator Test

Enable or Disable Vibrator



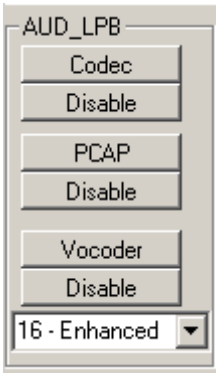
Verification

Verfiy vibration function when enabled.

Handset Mic/Speaker test

Set as illustrated.
Click Set

Select Enhanced Full Rate and click Vocoder



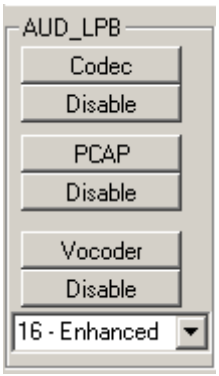
Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

Mono Headset Mic/Speaker test

Set as illustrated
Click Set

Select Enhanced Full Rate and click Vocoder

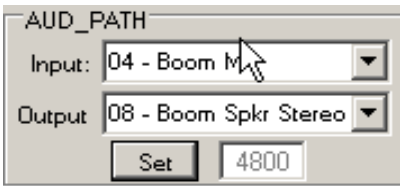


Verification

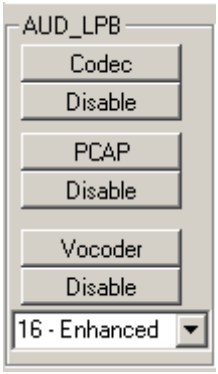
Speak into the headset mic and listen for undistorted speech in the headset speaker.

Stereo Headset Mic/Speaker test

Set as illustrated
Click Set



Select Enhanced Full Rate and click Vocoder



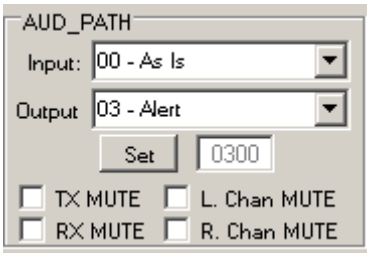
Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

Set AUD_TN_GEN as illustrated and click Start Tones

Set AUD_PATH as ilustrated and Click Set



Verification

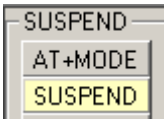
Listen for undistorted audio on the Alert.

Display Test Procedures

This section will describe the proper test procedures to determine the functionality of the color display.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Display Backlight Test

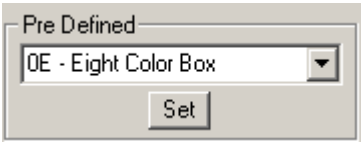
Click "FL Off" to disable backlight
Click "FL On-Full" to enable backlight

Verification

Verify that the backlights respond for each issued command.

Display Color Test

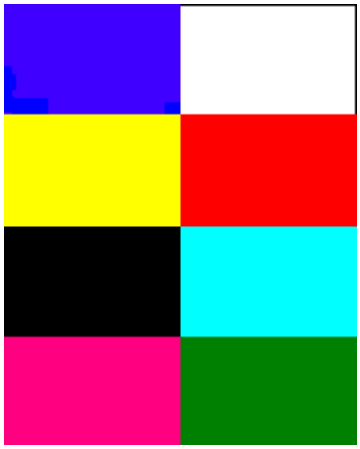
Select Eight Color Box and click "Set"



Verification

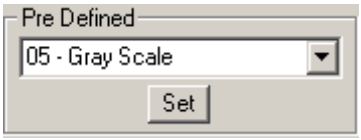
Verify that the color pattern on the phone's display matches the color box in figure 23. Also verify edges (uniform/smooth).

Figure 20. Eight Color Box Pattern



Display Linearity Test

Select Grey Scale and click “Set”



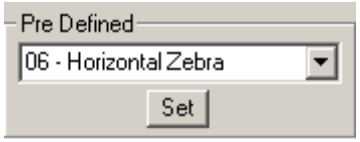
Verification

Verify that the Grey scale block on the phone’s display matches the Grey scale block in figure 14. This test can also be used to confirm that the color intensity is linear.

Figure 21. Grey Scale Block

Display Flicker Test

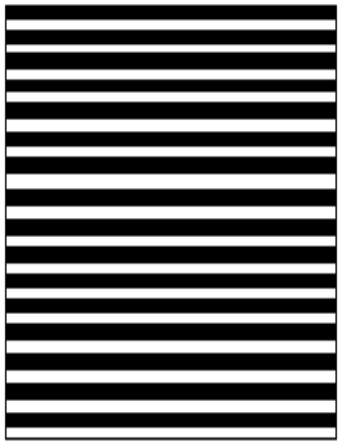
Select Horizontal Zebra and click “Set”



Verification

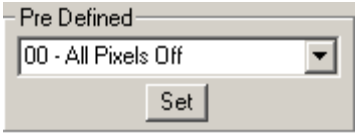
Verify that no noticable flicker exists.

Figure 22. Zebra Pattern



Display Pixel Defect (Bright)

Select All Pixels Off and click “Set”

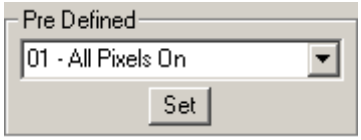


Verification

Verify that no greater than two pixels are off.

Display Pixel Defect (Dark)

Select All Pixels On and click “Set”



Verification

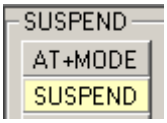
Verify that no greater than two pixels are on.

LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

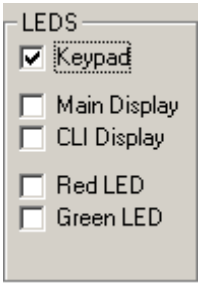
In order to successfully send test commands to the phone under test, the phone doesn’t need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Click AT+MODE (Serial Only)



Keypad Backlight

Select Keypad to enable. Deselect Keypad to disable.



Verification

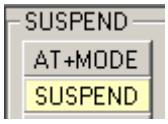
Verify that all keypad backlight LEDs activate.

Camera Testing

This section is intended to describe the procedures that will determine whether the camera function of a Motorola terminal is under normal operating conditions.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

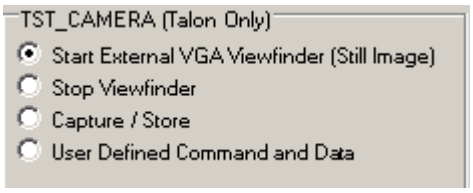
Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



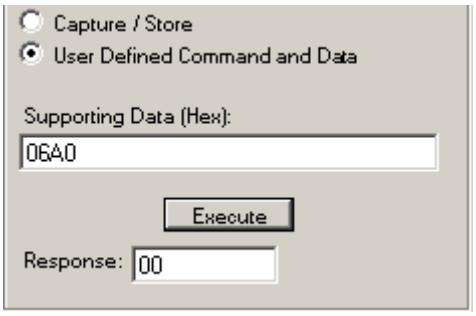
Data Line Integrity Check

When performing this test, RadioComm needs to be switched to GSM for proper responses. Go to the Menu bar and select Main>MA>GSM.

Select Start External Viewfinder



Select User Defined Command, enter 06A0 for data, and click Execute

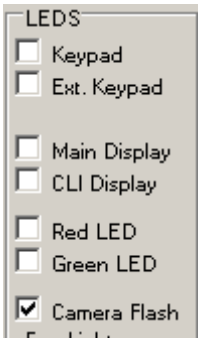


Verification

Verify that the response data returned 00.

Camera Flash Check

Select Camera Flash to enable. De-select Camera Flash to disable.



Verification

Verify that Camera Flash LED activates.

Theory of Operation

V975/V980 Overview

Motorola V975 and V980 telephones deliver 3G features in a smalle and lightweight package. These Global System for Mobile communications (GSM) General Packet Radio Service (GPRS) Wireless Application Protocol (WAP)-enabled mobile phones incorporate an icon based User Interface (UI) for easier operation, allows Short Message Service (SMS) text messaging, Multi-media Messaging Services (MMS), and includes Personal Information Manager (PIM) functionality. V975 and V980 are tri-band phones that allow roaming within the GSM 900 MHz, 1800 MHz Digital Cellular System (DCS), the GSM 850 MHz, and PCS 1900 MHz bands, in addition to the UMTS WCDMA 2100 MHz band.

V975 and V980 telephones have a clam form factor. They feature an externally viewable 96 x 80 4K color STN CLI display for caller identification with date/time, and an internal 167 x 220 65K TFT color display located in the flip. The bottom part of the clam (front housing) contains the keypad, transceiver printed circuit board (PCB), microphone, flex connection, external accessory connector, smart button, volume buttons, and voice button. The standard 820 mAh Lithium Ion (Li Ion) battery fits behind a removable back cover.

The phone accepts both 3V Subscriber Identity Module (SIM) cards that fit into the SIM holder under the battery. The antenna is a fixed stub type antenna. Inexpensive direct connection to a computer or handheld device through USB for data and fax calls, and for synchronizing phonebook entries with Motorola mobile Phone Tools™ software, can be accomplished using the optional data cable and soft modem.

V975 and V980 telephones use advanced, self-contained, sealed, custom integrated circuits to perform the complex functions required for GSM/WCDMA communication.

Features available in this family of telephones include:

- WCDMA 2100 MHz, GSM/GPRS 900/1800/1900 MHz
- Volume 105 cc
- 176 x 220, 1.9”, 65K TFT color display
- 96 x 80, 1”, 4K color STN CLI display
- VGA image capture w/ 4X zoom and lighting solution
- CIF camera for video conferencing
- 5 way navigation key

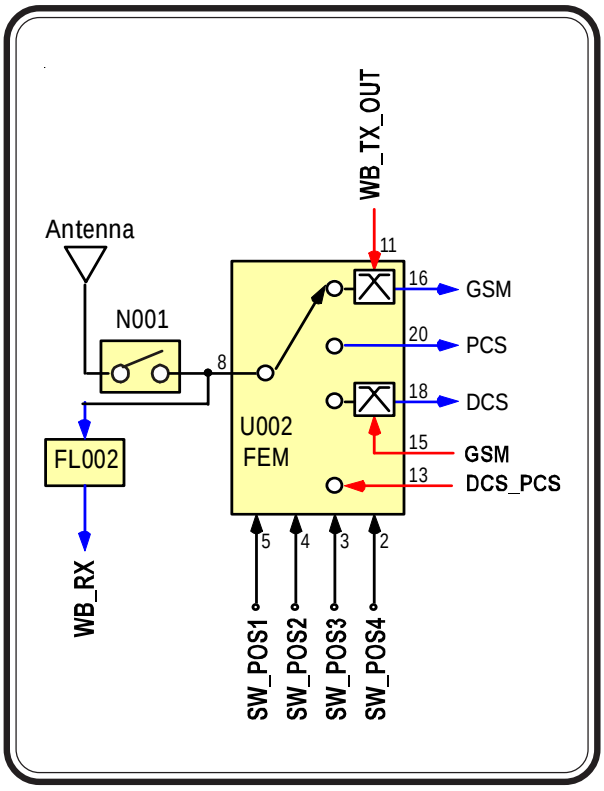
Figure 3-1. V975 Transceiver

- Dedicated camera key
- Accepts removable TransFlash memory (16, 32 64, 128, or 256MB) modules
- Talk time: up to 215 minutes (WCDMA, CS)
- Standby time: up to 260 hours
- Video clip playback
- 2MB user memory-V980
- 8MB user memory-V975

Front End Module

GSM receive signals from the antenna are fed into the FEM (Front End Module) through an antenna matching network and RF connector (N001). The WCDMA receive signal is directly tapped into the antenna matching network. This WCDMA receive configuration allows the mobile transceiver to receive WCDMA and GSM signals simultaneously, facilitating the ability to handover from a GSM network to UMTS network and vise-versa.

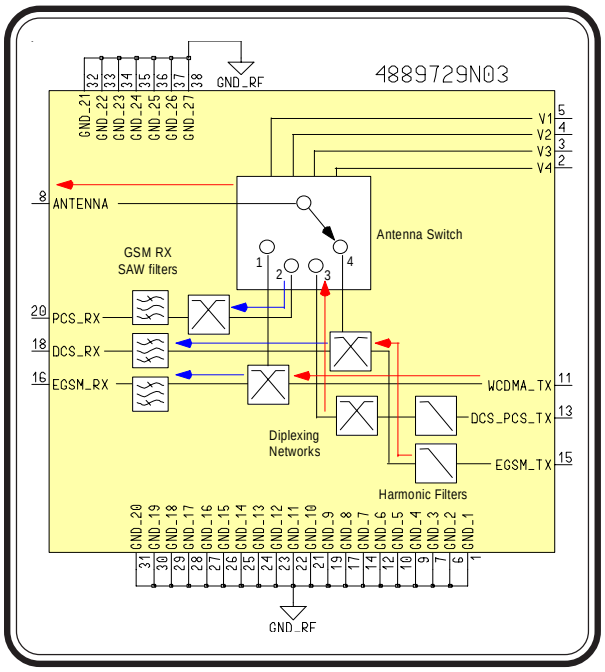
Figure 3-2. RF Top



WCDMA and GSM (all bands) transmit signals are passed through the FEM and fed into the antenna for transmission. If N001 is used, all WCDMA and GSM signals are fed into N001. Also, the internal antenna path will be in an open state when N001 is used.

The FEM integrates a 4-position GaAs antenna switch, diplexers, transmit harmonic filters, SAW filters and matching components on a multilayer low-temperature cofired ceramic (LTCC) module. The module provides band selection and filtering between the EGSM, DCS, PCS, and WCDMA (UMTS) receive and transmit bands in the 3G terminal.

Figure 3-3. FEM Module (FL001)



There is a network on each port of the antenna switch that serves several functions. The primary function is to make each switch path behave as an open circuit to incoming signals in the WCDMA receive band (2110 – 2170 MHz). Signals in the WCDMA Rx band are thereby reflected back to the WCDMA receiver. Received signals in the EGSM, DCS or PCS bands are allowed to pass through the switch and undergo some pre-filtering, then pass through SAW filters before leaving the module.

Signals from the WCDMA transmitter are diplexed with EGSM Rx, sharing switch position 1. Similarly, signals from the EGSM transmitter are diplexed with DCS Rx, sharing switch position 4. Switch position 3 is used solely by the DCS/PCS transmitter, and switch position 2 is used only by PCS Rx.

Band Selection in the Front End Module follows the Truth Table shown in table 3-1.

Table 3-1. FEM Truth Table

Band Selected	V1	V2	V3	V4
WCDMA Rx	x	x	x	x
WCDMA Tx, EGSM Rx	1	0	0	0
PCS Rx	0	1	0	0
DCS/PCS Tx	0	0	1	0
EGSM Tx, DCS Rx	0	0	0	1

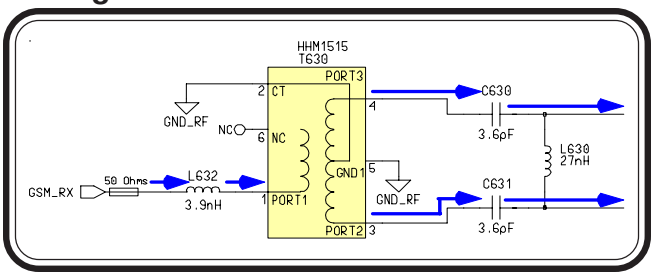
WCDMA Rx is available in any switch position.
Logic “1” is defined as 2.5 volts minimum.
Logic “0” is defined as 0 volts.

RF GSM Receiver

BALUN

From the FEM, the GSM singled-end, unbalanced received signals are fed into the Algae MB section of the Blue Module (900). Since the Algae MB expects a balanced differential receive input signal, the EGSM, PCS, and DCS signals must first pass through a differential conversion. Balun transformers provide the conversions from an unbalanced to a balanced line condition.

Figure 3-4. Balun Transformer

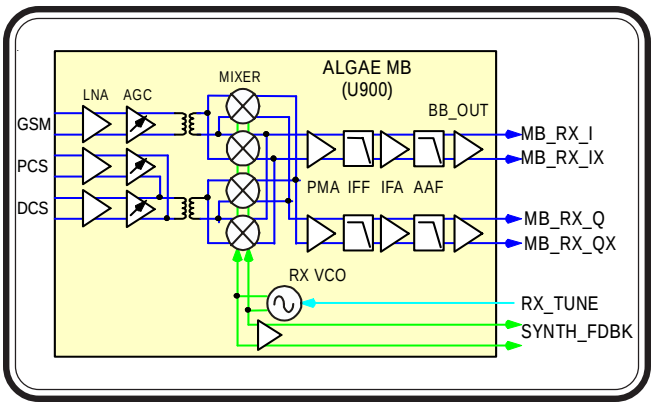


Each GSM band will contain a Balun transformer for differential conversions. The expected insertion loss for the Balun transformer is approximately 0.6 dBm.

BLUE MODULE IC (ALGAE)

Three LNAs are used for each receiver frequency band. Two hi-band LNAs are used for DCS and PCS frequencies and one low-band LNA is used for EGSM. Both hi-band LNAs are grouped together to share the same impedance matching transformer at the output. The low-band EGSM LNAs uses a separate impedance matching transformer at the the output.

Figure 3-5. ALGAE MB (Receiver)



Automatic gain control is provided by an AGC current steering differential pair. This current steering stage diverts current from the LNA load to supply in order to reduce the gain. The current steering differential pair alone would not have the desired transfer function, therefore an AGC linearizer is needed to provide a response that is linear in dB/V.

The LNAs drive AGC current steering stages that feed integrated transformer matching networks. The transformer drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q.

The downmixer converts the RF signal to baseband so that the signal can pass through a low-pass antialiasing filter and be converted to a digital format.

The output of the mixer connects directly to the post-

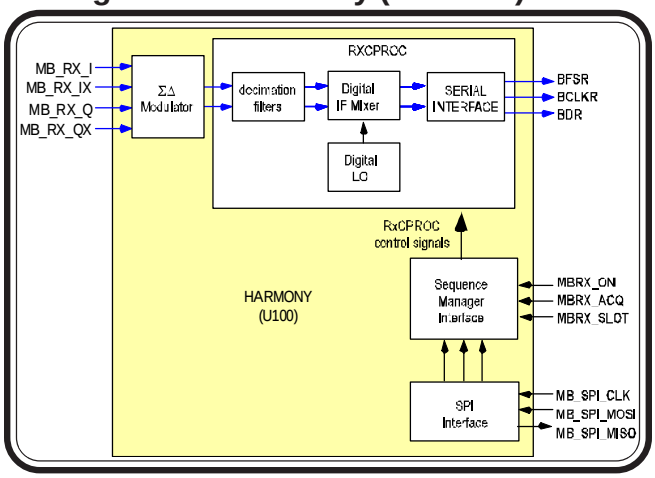
mixer amplifier. Large integrated capacitors are used to provide a low-frequency, low-pass corner at the output of the mixer. The signal then passes through baseband amplification and anti-aliasing filtering. The output of ALGAE MB will be balanced RXI and RXQ signal. It will have a 100kHz Very Low Intermediate Frequency (VLIF) signal that will be sent to the Harmony for Analog to digital conversion.

The LO signal is provided by a fully integrated VCO that drives either a divide-by-two or divide-by-four quadrature generator. In addition, a divide-by-3or5 circuit is used to feed back the LO signal to the synthesizer. The divide-by-3or5 circuit drives a differential output stage that provides the appropriate power level to the synthesizer. This output stage is shared with the TX path and provides the synthesizer feedback signal in both transmit and receive.

HARMONY GSM_RX (U100)

The RXI and RXQ VLIF signal entering the Harmony is sent to the Sigma-Delta modulator which transforms the slow moving analog signal into a high speed digital output. The Sigma-Delta modulator is set as an Analog-to-Digital Converter (ADC). The output of the Sigma-Delta modulator is then fed into the Receive Coprocessor (RxCPROC).

Figure 3-6. Harmony (GSM RX)



The RxCPROC includes the digital signal processing hardware required for the receive transceiver (Rx) after the initial conversion done by the sigma-delta modulator. It's configured to be used in the very low intermediate frequency mode (VLIF). The RxCPROC supports the GSM and EDGE standards.

The RxCPROC is represented by blocks listed as "decimation filters", "digital IF mixer", "digital LO" and "serial interface". The RxCPROC decimates and filters the I and Q quadrature input signals and converts them to baseband. Processed signals are sent serially to the Base Band Port (BBP) to be further handled by the DSP and VIAC.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data to the BBP module in the POG. SDFS is a framing signal which marks the beginning of an I,Q transfer. SDRX is the serial data. The clock used for the serial transfer is SCLK.

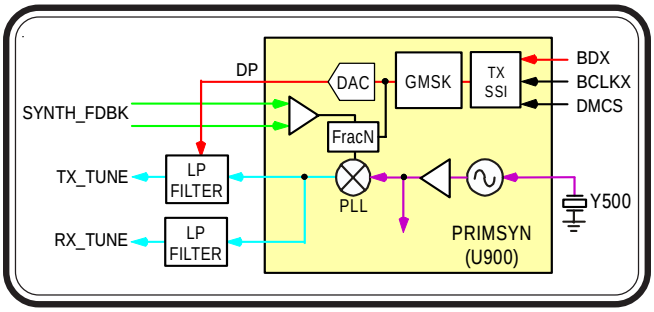
The RxCPROC is controlled via the SEQUENCE MANGER or SPI. Each control line of the Seq. Manager can be overridden by a corresponding line from the SPI (MB_SPI_CLK, MB_SPI_MOSI). Layer One timer signals (MB_RX_ON, MBRX_ACQ, MBRX_SLOT) from POG control the start of major sequences of events.

RF GSM Transmitter

BLUE MODULE IC (PRIMSYN GSM_TX)

The PRIMSYN receives SSI TX data at *DMCS* (digital input to start Tx modulation), *TXCLK* (clock for serial transfer) and *SDTX* (serial Tx data) from POG. This data pattern input to a fractional N synthesizer with a 24-bit resolution. For EGSM the synthesizer output is 880 – 915MHz, DCS is 1710 – 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

Figure 3-7. PRIMSYN (GSM TX)

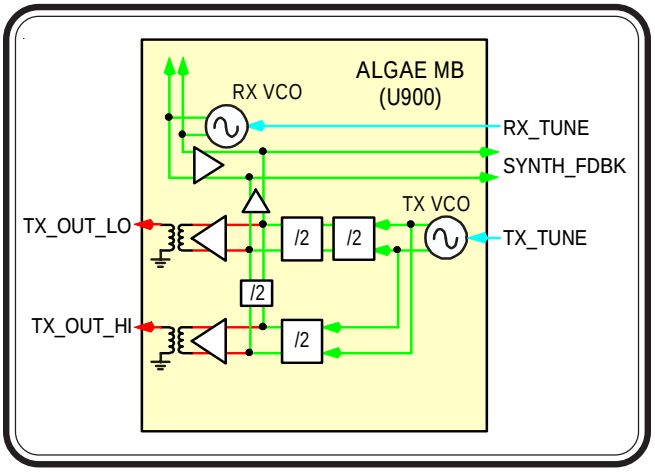


BLUE MODULE (ALGAE)

TRANSMIT SECTION

An integrated VCO is used for the transmit path. A single VCO is used for transmit. A low noise floor divide-by-2 stage drives the high band output. The low band output is driven by a divide-by-4 stage.

Figure 3-8. ALGAE MB (Transceiver)



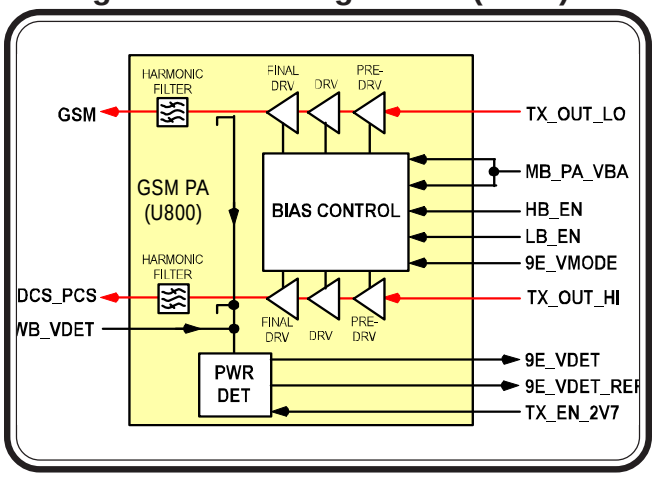
Two transmit output stages are provided. Both stages have integrated output matches in order to reduce the required number of discrete components. The integrated matches are implemented as differential to single-ended transformers.

The transmit signal is fed back to the synthesizer through a differential output stage that is shared with the receiver.

GSM PA (U800)

The TX VCO output signal from the ALGAE MB is injected in the Durango 9E3G via the TX_OUT_LO (Low Band) and TX_OUT_HI (Hi Band). Durango

Figure 3-9. Durango 9E3G (U800)



9E3G is a quad band PA Module for GSM applications in 3G phones. The module uses a dual amplifier lineup which operates in the three separate EGSM, DCS1800, and PCS1900 bands. It is compatible with GSM/GPRS operating modes. The integrated module incorporates coupler/detector for power control, Low pass filtering for harmonic rejection, and is internally input and output matched to 50 ohms.

This Transmit module is to be used as the final amplification stages in the A1000 for the EGSM (900 MHz), DCS (1800 MHz) and PCS (1900 MHz).

The nominal expected maximum gain is ~30dB.

The *VDET* (output) is the RF feedback along the DC reference *V_REF_DET* (output) are used in backend PA Control (PAC) processing by the HARMONY.

VBA_1 and VBA_2 are inputs from HARMONY that controls the PA output level. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases.

The power detector is internal to the PA and is shared among all GSM bands as well as WCDMA. WB_VDET connects WCDMA TX to the power detector

HB_EN enables the high band (DCS/PCS) amplifier lineup. LB_EN enables the low band (EGSM) amplifier lineup. TX_EN_2V7 enables the detector.

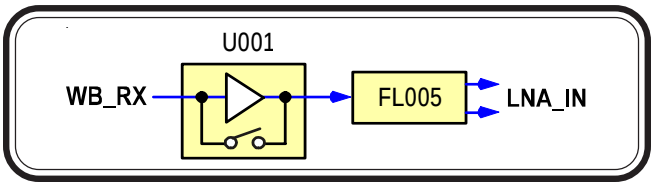
9E_VMODE sets the operating mode of the PA. GMSK and EDGE modes are supported, but only GMSK mode is used in this design. 9E_VMODE is set high during GMSK TX mode. 9E-VMODE is set low when the transmitter is in standby mode. This line is also enabled in WCDMA mode to allow proper WCDMA power detection.

RF WCDMA Receiver

MC13820 (U001)

The first IC in the WCDMA Rx line up is U001 (MC13820), which is a Low Noise Amplifier. The RX frequency will be amplified and passed on to OneLife WB through FL005. The LNA is controlled by Harmony (U100) through two enable lines. MBC_EN1 enables gain for the LNA while MBC_EN2 enables the IC. Both lines can be probed at testpoints located near Harmony (TP120 and TP121).

Figure 3-10. WCDMA LNA

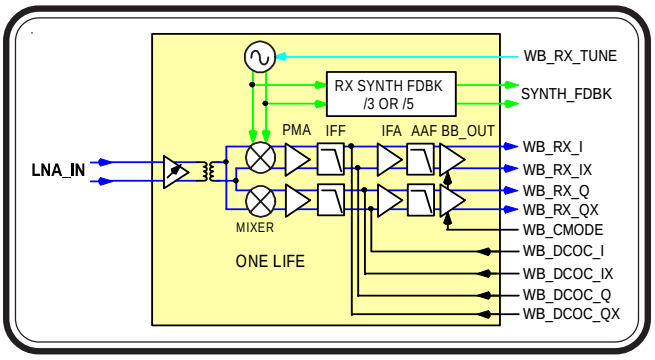


BLUE MODULE (ONELife)

ONELife is a full custom mixed signal BiCMOS IC with the SiGe option with electroplated copper inductors. This IC is a fully differential direct-conversion front-end IC and is comprised of a multiband RF section and a single path baseband section. The RF section is comprised of three Low Noise Amplifiers, two sets of quadrature mixers and an integrated 4GHz VCO with a divided prescaler output. Only one LNA is used in this design to cover the WCDMA/UMTS band (2110-1710). The LNA has two gain states; a high gain state and a bypass state with no reverse isolation. The LNA drives the quadrature mixers, via an integrated transformer matching network, that convert the RF signal to baseband, quadrature I and Q. The LO signal is provided by fully integrated VCOs that drives a divide-by-two quadrature generator. In addition, a divide-by-three/five circuit is used to feed back the LO signal to the synthesizer via an open collector output stage.

The baseband section is comprised of two separate I and Q paths each containing a PMA, an anti-aliasing filter made up of an IFA with an active pole and DCOC, two bi-quad sections, and an output buffer. The baseband signal path has six poles of baseband filtering distributed between mixer pole, the active IFA pole, and the two bi-quad blocks. The PMA has pseudo-continuous gain capability and is part of the AGC system along with the LNAs. The PMA AGC is controlled through five dedicated IC pins. At the output of the PMA stage, a baseband detector circuit provides broadband, strong signal information to the baseband part. DC Offset correction is provided through external differential pins to provide offset corrections to the internal IFA stage. The output buffer receives an input voltage via feedback from the Harmony WB_CMODE line so that OneLifeWB's output signal drives the A/D with the correct common mode voltage.

Figure 3-11. ONELife



Control and programming are done through a SPI interface from Harmony. Two supplies are required to power the IC, VRF_DIG_1.875V for SPI lines and VRF_2.775V for RF portions.

Harmony WCDMA_RX (U100)

The RX I an Q baseband signals are fed into the Sigma-Delta modulator of the Harmony. The Sigma-Delta modulator is an A/D converter that converts the I and Q baseband inputs to noise shaped 6-bit digital outputs. These outputs are then next decimated by a ratio of 3 using 3-stage cascaded comb type filters to a sampling rate of 15.36 MHz.

DC offset correction is performed next immediately to minimize the amount of delay in this mixed mode control loop to achieve rapid DC acquisition during *normal mode warmup sequences*. The DC offset correction unit has feedback to the OneLife-WB IC to be able to correct for DC offsets at the inputs to IF amplifier stage.

The matched selectivity filter is designed such that it provides the desired selectivity to meet adjacent channel and blocker specifications in the 2100 and 1800 MHz frequency bands.

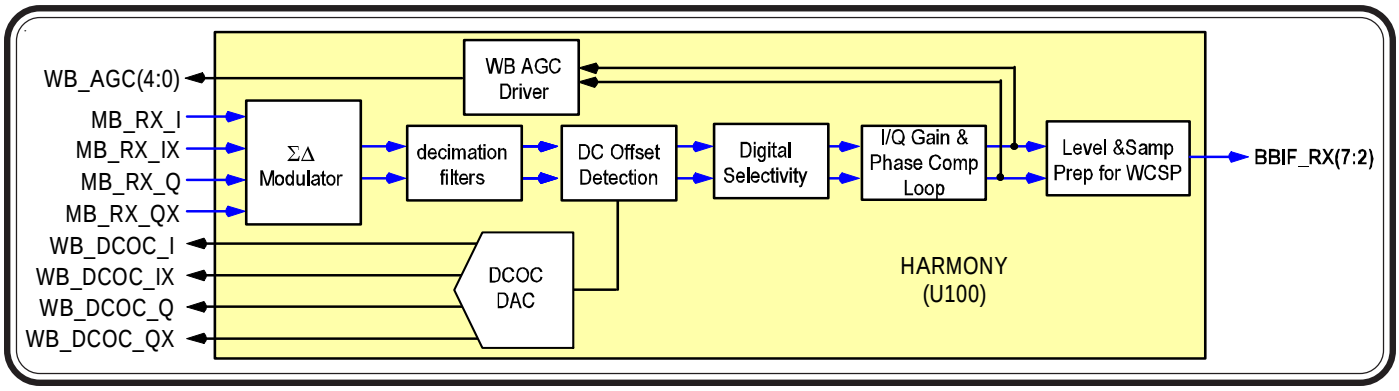
I/Q gain and phase imbalance equalization units located next in the lineup is used to correct for I/Q mismatches due to both the base station transmitter as well as the mobile device.

Next, the outputs of the I/Q gain equalization unit feed into the RF/IF AGC as well as the digital gain compensation control units. These outputs from the I/Q gain equalizer are used by the AGC unit for on-channel power detection. In addition, the AGC unit also receives off-channel power indication from a 2-bit SOS detector data bus from OneLife-WB IC. The on-channel and off-channel power levels are used by the RF/IF AGC unit to control internal and external LNA step attenuator stages as well as the variable gain PMA stage in OneLife-WB IC.

Two bit control lines are used to control each of the external LNA step attenuator stages. Alternately, a 1-bit control line is employed to control the internal LNA in the OneLife IC. In addition, a 5-bit parallel digital bus is employed to control the PMA variable gain control stage in OneLife-WB IC. The AGC unit also supplies the detected RSSI level to the external host device (e.g. POG IC) based upon the current RF, IF, and digital baseband gain control settings as well as the on-channel RSSI detected.

Following the I/Q gain equalization stage, a digital gain compensation unit is located next. The purpose of this gain compensation unit is to provide a 6-bit gain compensated output signal to the WCSP unit given that the input signal's dynamic range is 13 bits. The 15.36 MHz rate I and Q outputs are then interleaved in the BBIF (baseband interface) unit to generate the output I/Q data at a 30.72 MHz rate on a single 6-bit data bus to the external host device.

Figure 3-12. Harmony WCDMA RX (U100)



RF WCDMA Transmitter

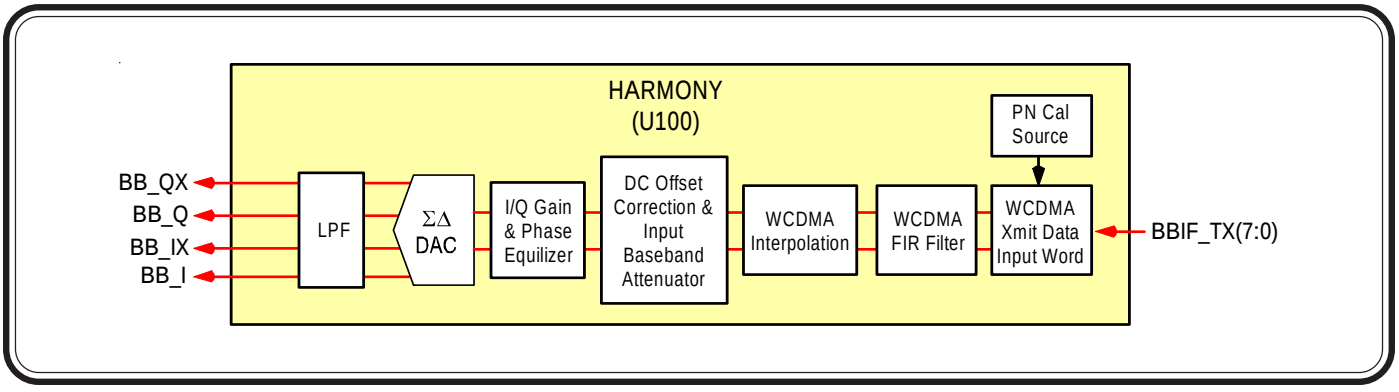
Harmony WCDMA TX (U100)

The Harmony provides pulse shaping and modulation of the 8-bit interleaved TX data coming from the POG. RF carrier suppression and baseband DC offset, I/Q gain and phase equilization will be then be performed. Finally, the I/Q signal is passed through a DAC and fed into the Rattler IC.

An 8-bit parallel interleaved data interface (BBIF_TX) is used to load the I and Q chip data from POG into the WCDMA signal path. Alternately, a PN calibration signal may also be loaded into this signal path for correction of baseband DC offsets and I/Q imbalances during transmitter warmup sequences. The parallel I and Q data from POG is first pulse shaped at a 7.68 MHz sampling rate using 31-tap SRRC FIR filters for the I and Q channels. These filters' outputs are then interpolated to a 30.72 MHz sampling rate using two stages of halfband interpolation filters.

The 12-bit outputs from the baseband pulse shaping and modulation system are fed into this DC and I/Q correction system. The specified 12 bit inputs first pass through the DC offset, I/Q phase and gain equalization blocks. The output samples from the gain equalizer are then fed into the sigma delta DACs at a higher sampling rate to minimize anti-aliasing filtering requirements. Following the DACs, there is an analog gain stage with 5 attenuation settings available for the baseband gain control system. Following this stage, a 2-pole passive filter and a 4th order Butterworth filter is employed in the quadrature signal path to eliminate the shaped noise from the sigma delta D/A's. The outputs of these reconstruction filters feed into the RF modulator IC (Rattler).

Figure 3-13. Harmony WCDMA TX (U100)



MC13786 (U200)

The MC13786 is an integrated I/Q modulator, IF and RF variable gain amplifier, UHF frequency synthesizer with a fully integrated VCO, image-reject upconverter mixer, and linear PA driver.

The synthesizer or phase locked loop (PLL) consists of a buffer amplifier, multi-modulus prescaler (divide by 4, 5, 6, and 7), a sixbit programmable post divider, reference divider, phase detector, and charge pump. The PLL uses a reference frequency of 15.36 MHz. One frequency synthesizer/VCO provides both the main and offset LO functions. The VCO operates over a frequency range of 2114 MHz to 2263 MHz and is fully integrated.

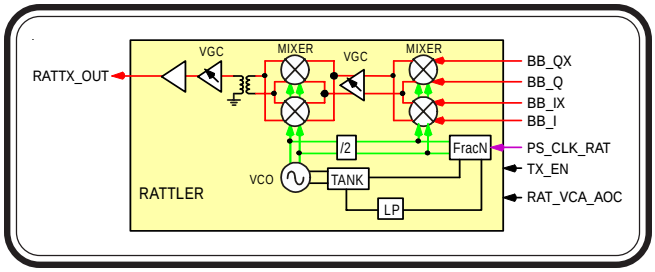
The I/Q Modulator consists of a quadrature generator and two Gilbert Cell active mixers. Using the offset LO and quadrature generator, the active mixers modulate the differential baseband I/Q signals onto a TXIF signal. Depending on the channel selection, the TXIF frequency will range from 274 MHz to 283 MHz.

From the active mixers, the TXIF signal is fed into a IF Variable Gain Amplified (IF VGA). The IF VGA has 70 dB of total typical gain control range and is controlled by the VGC line. The output of the VGA shall have a single pole bandpass tank circuit to provide attenuation to far-out noise.

The upconverter has an image-reject configuration so that the unwanted sideband is rejected to decrease the linearity requirements of the VGA stage. An input polyphase filter shall provide the necessary phase shift for the IR mixer. The TXIF signal is upconverted to a TX carrier frequency ranging from 1920MHz to 1980MHz. An on-chip copper balun shall provide the differential to single ended conversion necessary for the following stages.

The VGA provides a reduction in gain and current to optimize the TX lineup for lower output power levels. The PA driver amplifies the signal to provide sufficient drive for the radio power amplifier.

Figure 3-14. Rattler (U200)

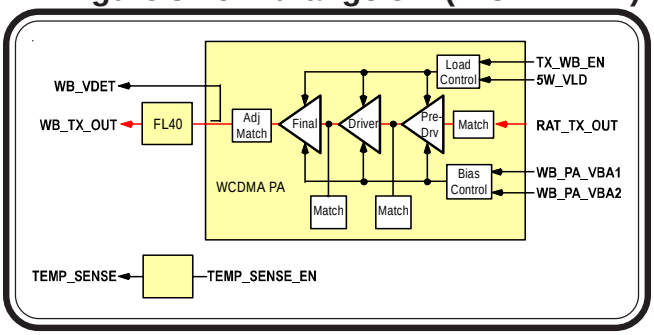


WCDMA PA (U850)

Durango5W is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 – 1980MHz. The nominal expected maximum gain is ~30dB.

A Motorola proprietary high power / low power efficiency enhancement load switch (5W_VLD) is included in the output match. VLD adjusts the output load for optimum efficiency from low power to high power out.

Figure 3-15. Durango 5W (WCDMA PA)



In conjunction with VLD, bias control (WB_PA_VBA1/WB_PA_VBA2) is performed between high and low power ranges.

The amplified WCDMA carrier is fed into a RF coupler device which has an integrated RF detector. An RF detect will pass through the Durango 9E3G (GSM PA) before being fed to the Harmony for power detection.

U880 is used to measure temperature. Its linear output is a voltage signal that corresponds to its physical device temperature. TEMP_SENSE is measured by PCAP and the MCU (POG) retreives the temperature readings every 5 seconds and passes it to the DSP (POG) so that the temperature compensation tables are updated.

The isolator provides a stable 50 ohm PA load. It also protects the PA from interfering with other frequency bands. Finally, it guards against IM products being produced by the transmitter and affecting receiver circuits.

RF Interface

Harmony

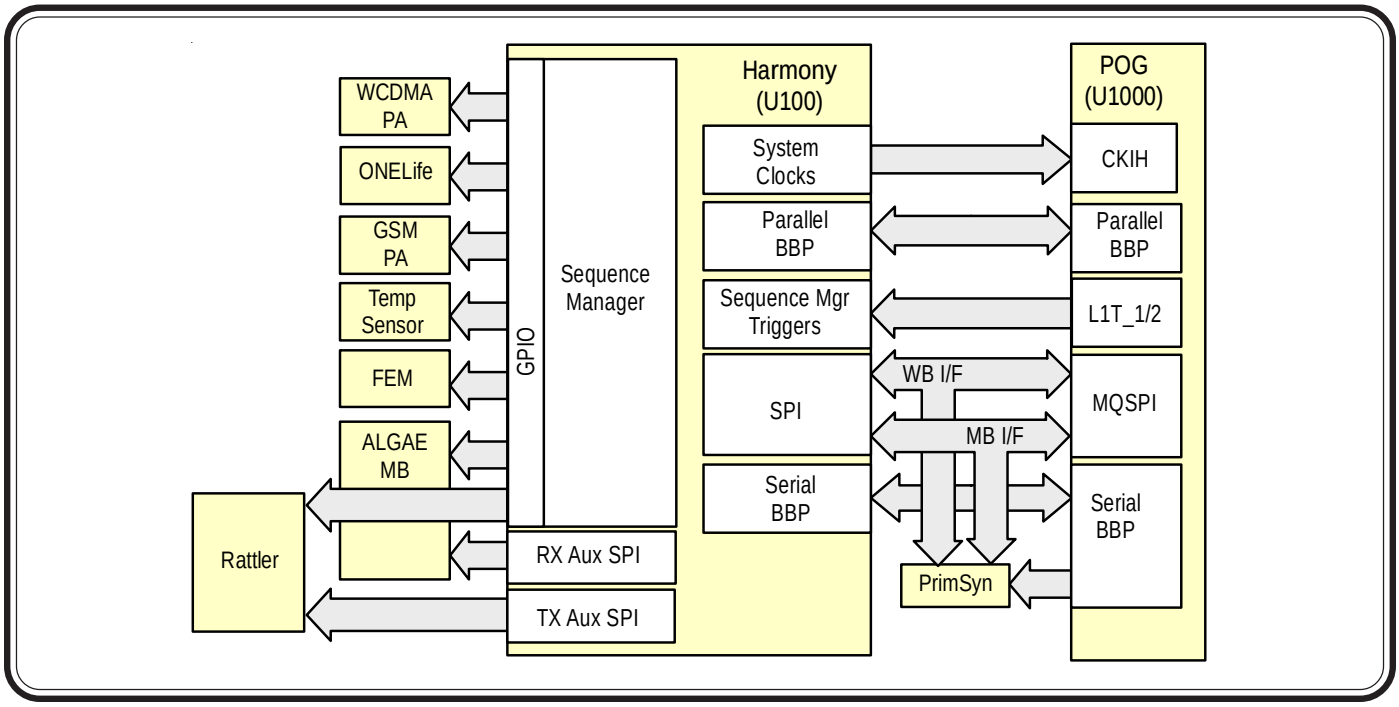
The Harmony IC is a mixed-signal transceiver backend IC intended to support GSM, EDGE and WCDMA services. It includes 2 receive paths: a medium-band path and a wideband path. The medium-band path is intended for GSM and EDGE and is configured to support VLIF receiver architecture. The wideband path is intended for WCDMA and is designed to operate in a direct conversion receiver architecture. Both of these receive signal paths are optimized for non-compressed mode. The transmitter path is designed to operate in a direct-launch transmitter architecture. The IC also includes dual clock synthesizers, as well as general support circuit such as sequence manager and SPI.

The Harmony IC and Base-Band (POG) IC interface consists of two independent sets of SPI lines (WB I/F, MB I/F); 2 chip-enable inputs, 2 clock inputs, 2 data inputs, and 2 data outputs. Harmony interfaces to the Base-band IC as a slave IC, however, it is also a master to two auxiliary ICs (Algae MB and Rattler) using two independent sets of SPI lines (TX AUX, RX AUX). The two auxiliary ICs are programmed by the Base-Band via Harmony.

In order to decrease the overall area required for controlling the sequences, a sequential access strategy was developed. The sequence manager would consist of controllers that would access an SRAM device sequentially. These controllers run of a set of programs that are pre loaded in to an SRAM memory device. In order to eliminate the need for a stack and interrupts each controller is dedicated to a single task. In the sequence manager there exists a controller per task, where the number of maximum tasks would be equivalent to the number of input TIMER lines.

A serial bus consisting of SDFS and SDRX will transmit the GSM RXI and RXQ data in 2's complement format to the Serial BBP module. The RXI and RXQ data will then be handled by the DSP integrated in the

Figure 3-16. RF Interface Block Diagram



POG. The Serial BBP module for TX is not used in this design.

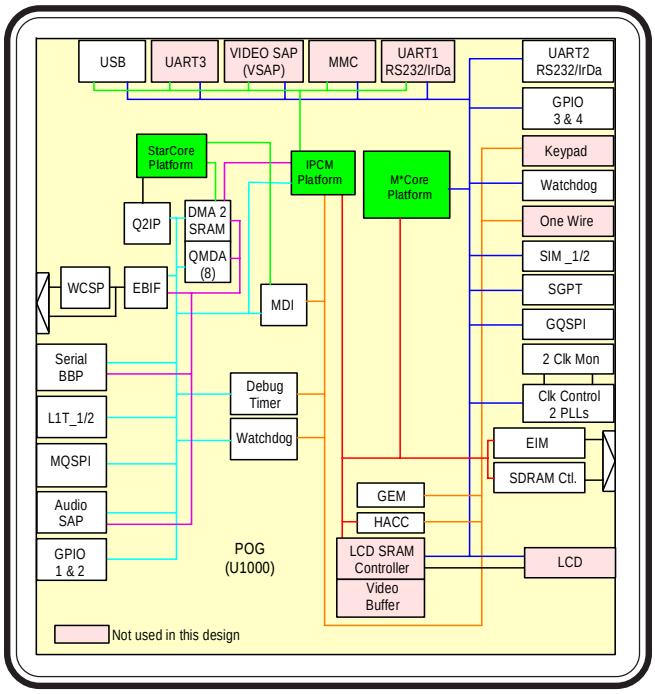
The WCDMA path receive path has a parallel BBP interface to send data to the Base Band processor. The interface is programmed to run at 15.36mhz. An 8-bit parallel interleaved data interface (Parallel BBP) is used to load the TX I and Q chip data from the external host processor (POG) IC into the WCDMA signal path of Harmony.

Baseband Electrical (Digital)

POG (U1000)

POG is the baseband processor IC of the 3G chipset solution. POG is crafted to provide a high performance embedded solution at low power for 3G mobile devices. POG is a TriCore processor IC integrating a powerful DSP core, a 32bit MCU RISC core with unified cache and a custom 32bit RISC engine for data movement across the processing domains.

Figure 3-18. POG Block Diagram



The DSP core is a high performance StarCore with four parallel ALUs, the SC140, with a novel Variable Length Execution Set (VLES) architecture which maximizes the execution of multiple instructions in a single clock cycle. The SC140 is assisted by 3G specific hardware accelerators and timers to optimize performance and power. As part of the 3G support, the Wideband CDMA Signal Processor (WCSP) module implements modem functions required by the CDMA subscriber unit in accordance with the 3GPP specifications.

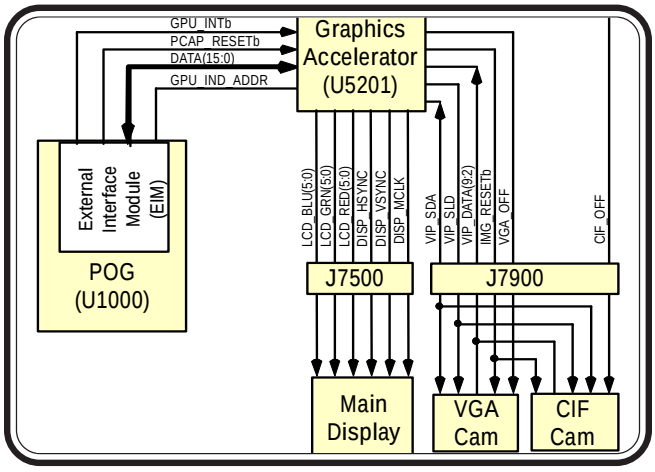
The 32bit MCU RISC core is the M*Core M341 designed for high performance and low power embedded systems. The M341 embodies an 16K unified cache, integer multiplier and MMU in support of virtual memory management OSes.

Data communication across the cores is handled by a flexible 32bit RISC machine, the Inter Processor Communication Module (IPCM). The IPCM supports flexible data flow between the MCU, DSP and the multimedia peripherals.

Graphics Accelerator

U5201 is a high performance, low power, Graphics/ Media Processor IC (GPU) that supports advanced multimedia applications for W-CDMA, UMTS, and GSM. This IC enables the user to capture, view, and share high quality images and video. A hardware-based

Figure 3-19. GPU Interface



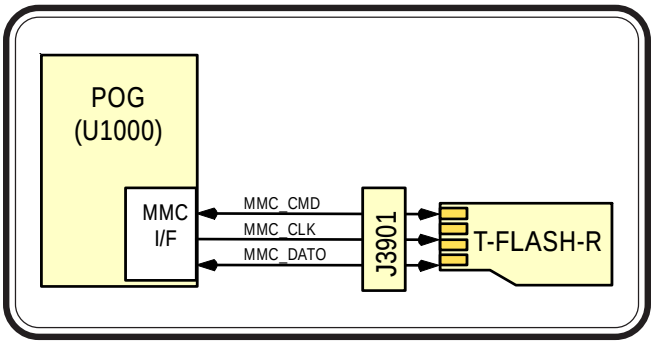
MPEG-4 encoder captures video at up to CIF resolution at 30fps. A hardware-based video decoder allows playback of the video recorded, or any other MPEG-4 clip or streaming video. A full hardware codec is uti-

lized for video conferencing – QCIF image size at up to 30fps. Support of VGA (680x480) resolution LCD at 16 and 18-bpp (with dithering) using only an embedded frame buffer and up to 3MP cameras with resolutions up to 2048x1536 image capture with a 10fps preview and 2MP cameras with a 15fps preview. The video processing engine is coupled with a JPEG encoder capable of encoding still images with 3MP resolution and a JPEG decoder capable of playback motion JPEG at up to 30fps at VGA resolution. The host interface bus provides an 8, 16, or 32-bit asynchronous interface that supports both direct and indirect addressing modes.

MMC/SD Flash Interface

The MMC/SD host controller provides an interface between the POG and Triflash-R memory card.

Figure 3-20. MMC Interface

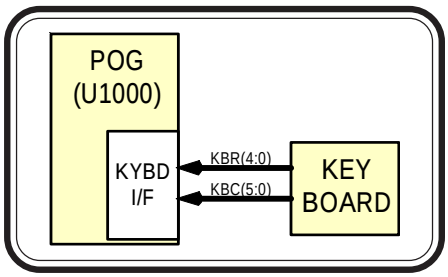


The MMC/SD host controller handles MMC/SD protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for syntactical correctness.

Keypad Interface

The keypad provides the primary physical user interface for the radio. The 5-way NAV joystick has a center keypress in addition to the four primary directions. White LED's will be used for backlighting. The keypad implementation to be used is the 2-contact, 1-pole keypad scanning architecture.

Figure 3-21. Keyboard Interface



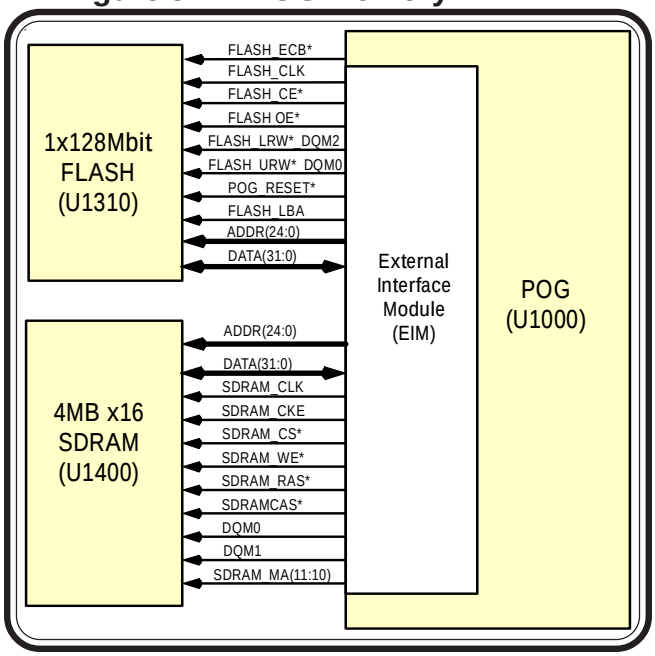
The Keypad Port (KPP) of POG decodes keypad presses. The Keypad Port is a 16-bit peripheral which is used for keypad matrix scanning. Keypad matrix uses 5 rows and 4 columns for key scanning. The KPP on POG can support up to an 8 x 8 row-by-column keypad matrix. The KPP will use a 32.768 KHz clock.

The Power/End key will not be part of the matrix but instead will connect directly to PCAP2.

POG Memory

The POG flash memory uses a 128 (128 Mbit) 1.8 Volt wireless memory which delivers high density flash memory in a single package. Individually erasable memory blocks are optimally sized for code and data storage. Four 16-Kword blocks and seven 64-Kword blocks are located in the parameter partition. The rest of the flash memory is divided into fifteen partitions of eight 64-Kword main blocks. By dividing the flash memory into partitions, program or erase can take place simultaneously during read operations. The device is available in a 56-ball vfBGA* package with 0.75 mm ball pitch.

Figure 3-22. POG Memory



The POG SDRAM device is a JEDEC standard SDRAM with 1.8V core supply, 1.8V I/O supply, four banks, and density of 4Mb x 16 (64 Mb). It is low power with special function support including partial array self refresh and temperature compensated refresh. It has a max frequency of 104MHz with CAS latency of three.

Power Supply Architecture

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are illustrated below.

Table 3-1. Power Distribution 1

Physical name	Logical name(s)	Voltage	Supplies
SW1	VLVIO_1.875	1.875	AP/BP Flash cores, AP flash I/O
SW2	Not Used	1.725	
SW3	VBOOST_5.5V	5.5	V10, Keypad backlights
V1	V1	1.875	Camera processors
V2	VA_2.775V	2.775	Audio
V3	Not Used	1.875	
V4	VPOG_VLVIO_1.875V	1.875	Low voltage I/O
V5	VHVIO_2.775	2.775	PCAP internal components
V6	VRF_TX_2.775V	2.775	Harmony, Rattler, RF TX
V7	Not Used	2.775	

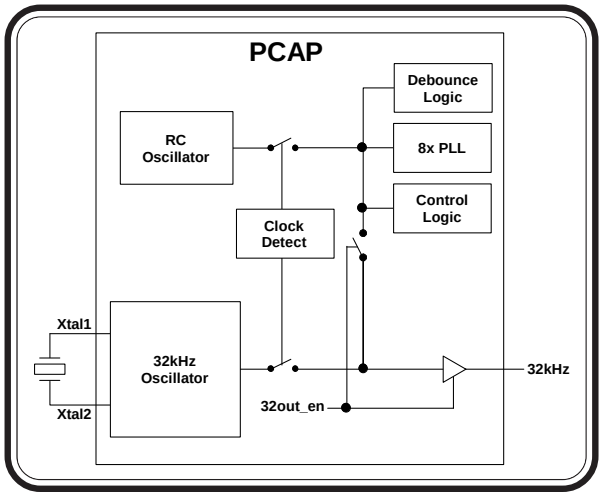
Table 3-2. Power Distribution 2

Physical name	Logical name(s)	Voltage	Supplies
V8	VMMC_2.775	2.775	MMC
V9	VRF_REF_2.475V	2.775	RF Reference
V10	VRF_HV_5V	5	RF HV
VAUX1	Not Used	2.775	
VAUX2	VRF_RX_2.775V	2.775	Harmony, Algae, RF RX
VAUX3	VCAM_2.6	2.6	Transflash
VAUX4	Not Used	3	
U3206	VMAIN_1.55V	1.55	POG Core

Clock Generation

PCAP can generate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Rainbow requires for optimal performance, therefore, an external 32.768kHz crystal is used.

Figure 3-24. RTC Clock



The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Audio Circuits

PCAP (U3000)

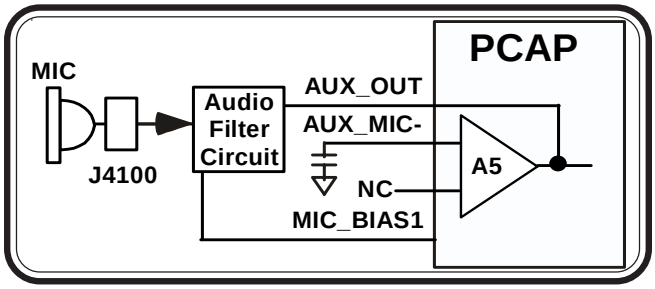
The PCAP2 IC is an ASIC intended for use in Colorado platform mobile phones. It integrates several functional modules:

- Voltage regulators of both linear and switching types designed for use in the Colorado power scheme
- Audio codecs and amplifiers
- RS-232 and USB transceivers
- LED controllers for the service light and display/keypad backlights
- Digital interfaces for two controlling processors.

TX Audio

The 3G termianl supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single-ended with respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

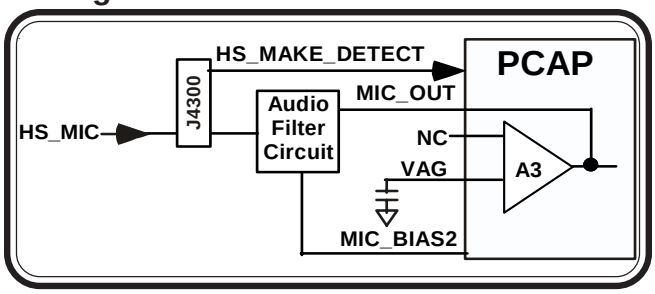
Figure 3-25. Internal Mic Path



The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 and R4101 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R4102 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

The headset microphone path is biased through R4396, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by using R4399 as a pull-up resistor and detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

Figure 3-26. Headset Mic Path



The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight/ALeft Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R34003 and R34002 respectively, and then connected to the transducer. Off the Speaker-path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

Figure 3-28. Handset Speaker Path

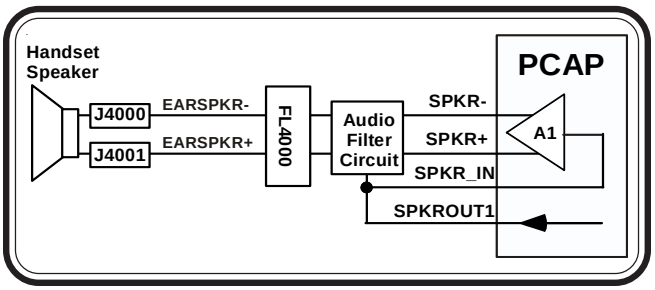
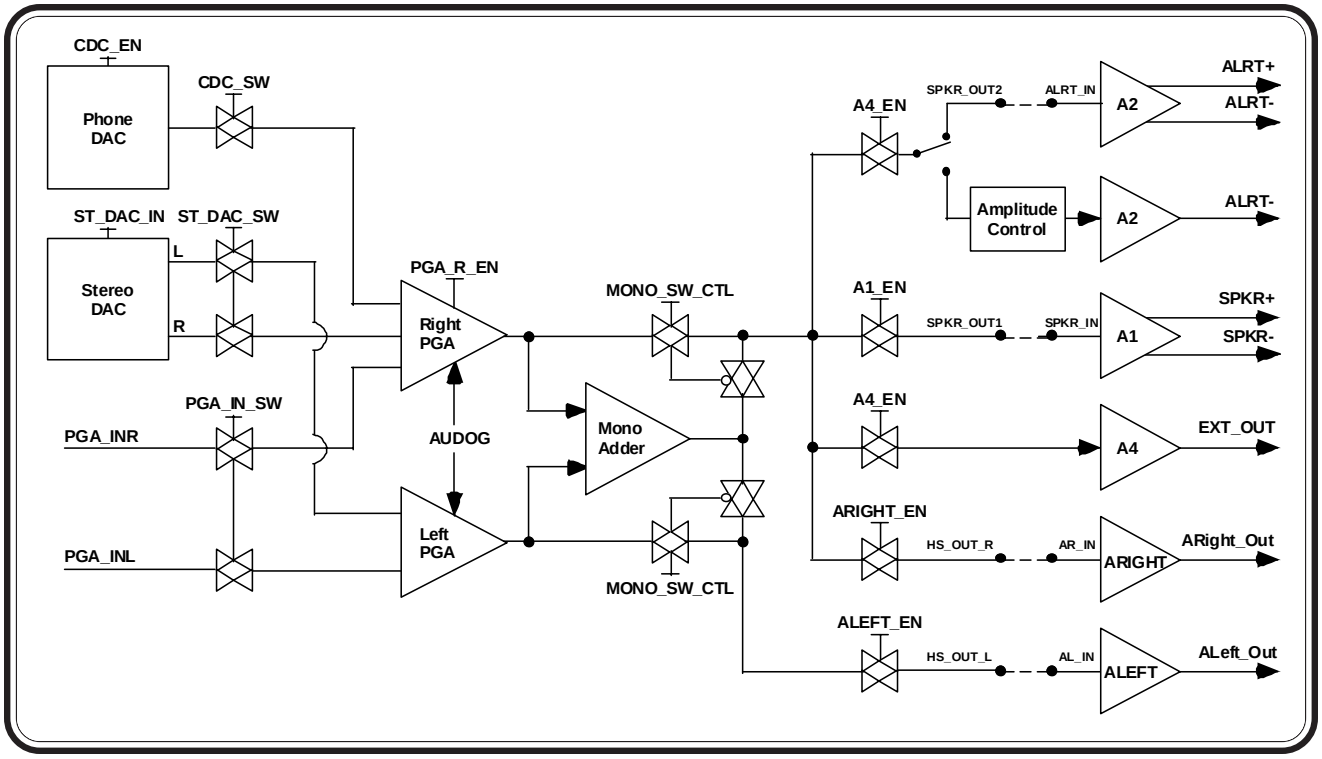
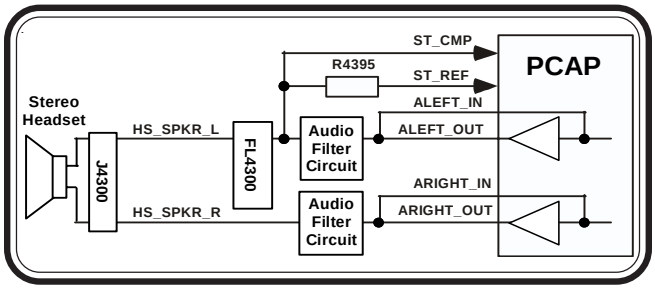


Figure 3-27. RX Audio Block



The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

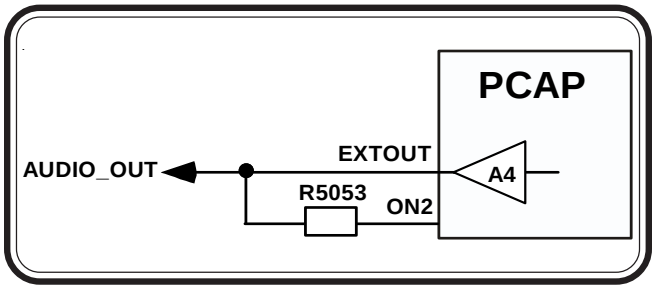
Figure 3-29. Headset Speaker Path



The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R34304 and C4306, R34303 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ARight_Out path, AL_IN is tapped off through C4354 for the inverting input of the audio amp ALEFT.

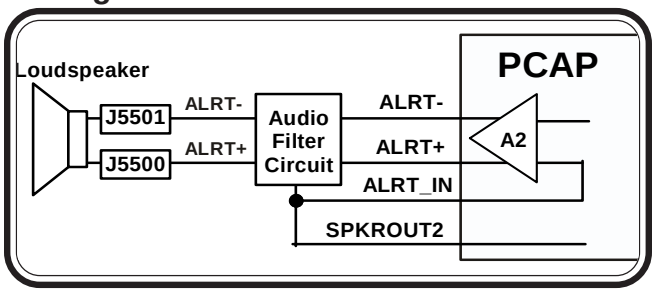
The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

Figure 3-30. External Speaker Path



The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

Figure 3-31. Alert Path



Battery Interface

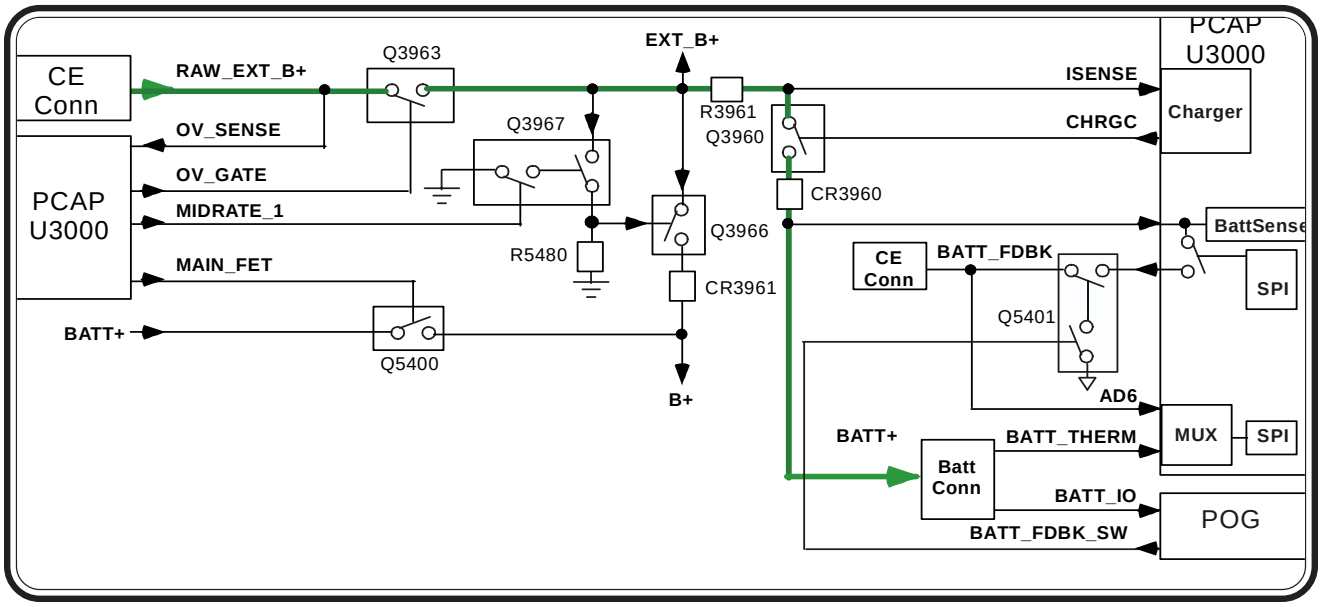
Batteries interface to the main transceiver board via a 4-pin connector (J5400). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q5400 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U3000) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J5000). During full rate charging, Q3966 is turned ON so that current can be supplied from the external source to B+. Q5400 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q3960. A sense resistor (R3961) provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J5000). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 3-32. Battery Interface Block



V975 Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the V975 UMTS/GSM handset.

Table 4-1. Electrical Parts List - A1 to C400

Reference Number	Part Number	Description
A1	3989013L05	CONTACT
B5400	0990107N01	CONN_J
C001	2113944A02	CAP, 1.2pF
C004	2189687Y06	CAP, 0.3pF
C007	2113945B02	CAP, .01uF
C008	2113944A25	CAP, 10pF
C003DNP	2113944A63	CAP, 1pF
C005DNP	2113944A63	CAP, 1pF
C010	2113944A63	CAP, 1pF
C011DNP	2113944A05	CAP, 1.5pF
C020	2113944A31	CAP, 33pF
C021	2113944A31	CAP, 33pF
C022	2113944A31	CAP, 33pF
C023	2113944A31	CAP, 33pF
C100	2113946F03	CAP, 4.7uF
C101	2113946F03	CAP, 4.7uF
C102	2113944A31	CAP, 33pF
C103	2113946D02	CAP, 1.0uF
C104	2113946D02	CAP, 1.0uF
C105	2113946D02	CAP, 1.0uF
C106	2187893N01	CAP, 1.0uF
C110	2113944A41	CAP, 120pF
C111	2113945B02	CAP, .01uF
C112	2113945A10	CAP, 1500pF
C113	2113945B02	CAP, .01uF
C115	2113944A32	CAP, 39pF
C114DNP	2113946K02	CAP, 0.10uF
C200	2113946F03	CAP, 4.7uF
C201DNP	2113944A25	CAP, 10pF
C202DNP	2113944A25	CAP, 10pF
C203DNP	2113944A25	CAP, 10pF
C212	2113944A11	CAP, 2.7pF
C221	2113944A26	CAP, 12pF
C222DNP	2113944A26	CAP, 12pF
C3911DNP	2113946D02	CAP, 1.0uF
C3971DNP	2113946K02	CAP, 0.10uF
C3985DNP	2113946K02	CAP, 0.10uF
C400	2113946F03	CAP, 4.7uF

Table 4-2. Electrical Parts List - C401 to C908

Reference Number	Part Number	Description
C401	2113946D02	CAP, 1.0uF
C402	2113946D02	CAP, 1.0uF
C403	2113945B02	CAP, .01uF
C404	2113944A25	CAP, 10pF
C406	2113944A32	CAP, 39pF
C407	2113946D02	CAP, 1.0uF
C408	2113944A63	CAP, 1pF
C4000DNP	2113944A31	CAP, 33pF
C4003DNP	2113944A31	CAP, 33pF
C409DNP	2113944A63	CAP, 1pF
C4101DNP	2113944A31	CAP, 33pF
C4102DNP	2113944A31	CAP, 33pF
C4308DNP	2113944A31	CAP, 33pF
C4402DNP	2113944A31	CAP, 33pF
C4500DNP	2113944A31	CAP, 33pF
C4504DNP	2113944A31	CAP, 33pF
C501	2113945B02	CAP, .01uF
C5501DNP	2113944A25	CAP, 10pF
C5502DNP	2113944A25	CAP, 10pF
C5505DNP	2113944A25	CAP, 10pF
C800	2113946F05	CAP, 10uF
C801	2113946B04	CAP, 0.1uF
C802	2113946B04	CAP, 0.1uF
C803	2113946B04	CAP, 0.1uF
C804	2113946B04	CAP, 0.1uF
C806	2113946B04	CAP, 0.1uF
C807	2113944A25	CAP, 10pF
C808	2113944A25	CAP, 10pF
C809	2113944A08	CAP, 2.0pF
C810	2113944A08	CAP, 2.0pF
C811	2113944A32	CAP, 39pF
C812	2113944A09	CAP, 2.2pF
C813	2113944A25	CAP, 10pF
C815DNP	2113944A25	CAP, 10pF
C816DNP	2113944A25	CAP, 10pF
C881	2113945B02	CAP, .01uF
C882	2113945B02	CAP, .01uF
C901	2113946F03	CAP, 4.7uF
C902	2113946F03	CAP, 4.7uF
C903	2113946F03	CAP, 4.7uF
C904	2113946F03	CAP, 4.7uF
C906	2113944A08	CAP, 2.0pF
C907	2113945B02	CAP, .01uF
C908	2113945B02	CAP, .01uF

Table 4-3. Electrical Parts List - C909 to C3002

Reference Number	Part Number	Description
C909	2113945B02	CAP, .01uF
C915	2113944A32	CAP, 39pF
C916	2113944A32	CAP, 39pF
C917	2113944A32	CAP, 39pF
C918	2113944A32	CAP, 39pF
C921	2113944A32	CAP, 39pF
C1000	2113944A32	CAP, 39pF
C1002	2113947H01	CAP, 0.1uF
C1003	2113947H01	CAP, 0.1uF
C1004	2113947H01	CAP, 0.1uF
C1005	2113946K02	CAP, 0.10uF
C1007	2113947H01	CAP, 0.1uF
C1008	2113947H01	CAP, 0.1uF
C1009	2113946K02	CAP, 0.10uF
C1012	2113947H01	CAP, 0.1uF
C1013	2113947H01	CAP, 0.1uF
C1014	2113947H01	CAP, 0.1uF
C1015	2113946K02	CAP, 0.10uF
C1016	2113947H01	CAP, 0.1uF
C1017	2113947H01	CAP, 0.1uF
C1018	2113947H01	CAP, 0.1uF
C1020	2113946K02	CAP, 0.10uF
C1021	2113947H01	CAP, 0.1uF
C1023	2113947H01	CAP, 0.1uF
C1024	2113947H01	CAP, 0.1uF
C1025	2113946K02	CAP, 0.10uF
C1026	2113946K02	CAP, 0.10uF
C1028	2113946K02	CAP, 0.10uF
C1031	2113947H01	CAP, 0.1uF
C1032	2113946K02	CAP, 0.10uF
C1038	2113946K02	CAP, 0.10uF
C1300	2113947H01	CAP, 0.1uF
C1301	2113947H01	CAP, 0.1uF
C1302	2113947H01	CAP, 0.1uF
C1303	2113947H01	CAP, 0.1uF
C1305	2113946K02	CAP, 0.10uF
C1402	2113946K02	CAP, 0.10uF
C1403	2113946K02	CAP, 0.10uF
C1404	2113946K02	CAP, 0.10uF
C1405	2113946K02	CAP, 0.10uF
C1406	2113946K02	CAP, 0.10uF
C3000	2113946F05	CAP, 10uF
C3001	2113946F05	CAP, 10uF
C3002	2113946K02	CAP, 0.10uF

Table 4-4. Electrical Parts List - C3050 to C4208

Reference Number	Part Number	Description
C3050	2113946D02	CAP, 1.0uF
C3100	2113946F05	CAP, 10uF
C3101	2113946F05	CAP, 10uF
C3102	2113946K02	CAP, 0.10uF
C3150	2113946D02	CAP, 1.0uF
C3151	2113944A31	CAP, 33pF
C3200	2113944A34	CAP, 56pF
C3201	2113946F05	CAP, 10uF
C3202	2113944A42	CAP, 150pF
C3205	2113946F05	CAP, 10uF
C3250	2113946K02	CAP, 0.10uF
C3300	2113946D02	CAP, 1.0uF
C3350	2113946F03	CAP, 4.7uF
C3400	2113946F08	CAP, 22uF
C3401	2113946K02	CAP, 0.10uF
C3500	2113946F08	CAP, 22uF
C3501	2113946K02	CAP, 0.10uF
C3550	2113946D02	CAP, 1.0uF
C3600	2113946D02	CAP, 1.0uF
C3654	2113946D02	CAP, 1.0uF
C3800	2113946D02	CAP, 1.0uF
C3801	2113946D02	CAP, 1.0uF
C3850	2113946D02	CAP, 1.0uF
C3851	2113946D02	CAP, 1.0uF
C3906	2113944A31	CAP, 33pF
C3910	2113946K02	CAP, 0.10uF
C3951	2113946F03	CAP, 4.7uF
C3960	2113946F05	CAP, 10uF
C3961	2113946F05	CAP, 10uF
C3962	2113946K02	CAP, 0.10uF
C3965	2113946K02	CAP, 0.10uF
C3970	2113946D02	CAP, 1.0uF
C3983	2113944A25	CAP, 10pF
C3984	2113944A25	CAP, 10pF
C3990	2113946K02	CAP, 0.10uF
C4001	2113945A10	CAP, 1500pF
C4002	2113946B04	CAP, 0.1uF
C4100	2113946B04	CAP, 0.1uF
C4103	2113944A31	CAP, 33pF
C4104	2113944A25	CAP, 10pF
C4105	2113946D02	CAP, 1.0uF
C4203	2113944A31	CAP, 33pF
C4204	2113944A31	CAP, 33pF
C4208	2113944A31	CAP, 33pF

Table 4-5. Electrical Parts List - C4209 to C5200

Reference Number	Part Number	Description
C4209	2113944A31	CAP, 33pF
C4210	2113946F03	CAP, 4.7uF
C4211	2113944A31	CAP, 33pF
C4212	2113945A07	CAP, 680pF
C4213	2113946B04	CAP, 0.1uF
C4214	2113944A31	CAP, 33pF
C4300	2113944A31	CAP, 33pF
C4301	2113945B02	CAP, .01uF
C4302	2113945B02	CAP, .01uF
C4304	2113946B04	CAP, 0.1uF
C4305	2113946B04	CAP, 0.1uF
C4306	2113946F08	CAP, 22uF
C4310	2113946B04	CAP, 0.1uF
C4356	2113946F08	CAP, 22uF
C4392	2113944A32	CAP, 39pF
C4393	2113944A32	CAP, 39pF
C4400	2113946D02	CAP, 1.0uF
C4401	2113946B04	CAP, 0.1uF
C4403	2113946D02	CAP, 1.0uF
C4501	2113946B04	CAP, 0.1uF
C4502	2113946D02	CAP, 1.0uF
C4503	2113946B04	CAP, 0.1uF
C4550	2113945A13	CAP, 4700pF
C4551	2113946B04	CAP, 0.1uF
C4901	2113946B04	CAP, 0.1uF
C4902	2113945B02	CAP, .01uF
C4903	2113945B02	CAP, .01uF
C5000	2113946K02	CAP, 0.10uF
C5001	2113944A31	CAP, 33pF
C5002	2113944A31	CAP, 33pF
C5003	2113946D02	CAP, 1.0uF
C5111	2113944A31	CAP, 33pF
C5112	2113944A31	CAP, 33pF
C5113	2113944A31	CAP, 33pF
C5114	2113944A31	CAP, 33pF
C5115	2113944A31	CAP, 33pF
C5116	2113944A31	CAP, 33pF
C5118	2113944A31	CAP, 33pF
C5119	2113944A31	CAP, 33pF
C5120	2113944A31	CAP, 33pF
C5121	2113944A31	CAP, 33pF
C5122	2113944A32	CAP, 39pF
C5123	2113945B02	CAP, .01uF
C5200	2113946K02	CAP, 0.10uF

Table 4-6. Electrical Parts List - C5201 to L002

Reference Number	Part Number	Description
C5201	2113946K02	CAP, 0.10uF
C5202	2113946K02	CAP, 0.10uF
C5203	2113947H01	CAP, 0.1uF
C5204	2113946K02	CAP, 0.10uF
C5205	2113947H01	CAP, 0.1uF
C5206	2113946K02	CAP, 0.10uF
C5207	2113944A31	CAP, 33pF
C5208	2113944A31	CAP, 33pF
C5400	2113946F03	CAP, 4.7uF
C5503	2113944A25	CAP, 10pF
C5508	2113944A25	CAP, 10pF
C910DNP	2113945B02	CAP, .01uF
C911DNP	2113945B02	CAP, .01uF
C912DNP	2113945B02	CAP, .01uF
C913DNP	2113944A25	CAP, 10pF
C914DNP	2113944A25	CAP, 10pF
C919DNP	2113743N15	CAP, 3.6pF
C920DNP	2113743N15	CAP, 3.6pF
CR3000	4809924D29	BAS52
CR5401	4888722V02	RB751V-40FTE17
D901	4809948D52	BA892
D3100	4809653F10	MBRM120ET3
D3961	4809653F10	MBRM120ET3
D3962	4809653F10	MBRM120ET3
E501	SHORT_RES0402	SHORT
E800	SHORT_RES0201	SHORT
E801	SHORT_RES0201	SHORT
FL001	4889729N03	FEM3203_ES6D
FL002	9109674L25	CF61A4203
FL003	9188736Y01	CF61A6001
FL004	9109674L17	74L17
FL100	9188695K05	CSPRC032AG
FL900	9109239M38	SAFSD2G14
FL4300	4889526L14	CSPEMI202AG
FL5200	9188916Y01	NFA21SL
FL5201	9188916Y01	NFA21SL
J3901	3989655N02	CONTACT
J4100	0909195E05	CONN_J
J4300	0989675N03	CONN_J
J5000	0988794Y02	CONN_J
J5100	0987817K06	CONN_J
J5212	0989851N01	CONN_J
J5500	0185923C01	CONN_J
L002	2488090Y09	IDCTR, 4.7nH

Table 4-7. Electrical Parts List - L003 to R113

Reference Number	Part Number	Description
L003	2488090Y08	IDCTR, 3.9nH
L004	2489711L11	IDCTR, 10nH
L005	2488090Y05	IDCTR, 2.2nH
L006	2415427H01	IDCTR, 1.0nH
L009	2488090Y17	IDCTR, 22nH
L007DNP	2488090Y08	IDCTR, 3.9nH
L008DNP	2488090Y17	IDCTR, 22nH
L800	2487996L04	EXCML16
L801	2488090Y07	IDCTR, 3.3nH
L802	2488090Y12	IDCTR, 8.2nH
L803	2488090Y12	IDCTR, 8.2nH
L901	2488090Y09	IDCTR, 4.7nH
L3000	2588079Y03	IDCTR, 10uH
L3100	2590031N05	IDCTR, 6.8uH
L3206	2588079Y03	IDCTR, 10uH
L4399	2414017G14	IDCTR, 39nH
L4400	2414017G14	IDCTR, 39nH
M100DNP	1188983Y01	1188983Y01
M101DNP	1188983Y01	1188983Y01
M102DNP	1188983Y01	1188983Y01
M103DNP	1188983Y01	1188983Y01
M3000	5987774N01	MR-2561
M5400	3987697Y02	CONTACT
N001	0987378K01	SWITCH
Q3401	4813973M76	NSL12AW
Q3501	4813973M76	NSL12AW
Q3960	4805585Q23	SI8401DB
Q3961	4805585Q23	SI8401DB
Q3963	4888585Y01	SI8405DB
Q3964	4805585Q23	SI8401DB
Q3974	4809579E67	2SK3019FTL
Q5001	5186626U10	LM619
Q5100	4813973A13	73A13
R001	0613952R66	RES, 0
R002	0613952Q87	RES, 3.9K
R003	0613952Q80	RES, 2K
R006	0613952R66	RES, 0
R103	SHORT_RES0402	SHORT
R104	SHORT_RES0402	SHORT
R105	SHORT_RES0402	SHORT
R106	SHORT_RES0402	SHORT
R1032DNP	0613952R66	RES, 0
R111	0613952Q77	RES, 1.5K
R113	0613952Q77	RES, 1.5K

Table 4-8. Electrical Parts List - R114 to R1404

Reference Number	Part Number	Description
R114	0613952R25	RES, 100K
R200	0613952Q39	RES, 39
R201	0613952R66	RES, 0
R203	0613952R66	RES, 0
R204	0613952R66	RES, 0
R206	SHORT_RES0402	SHORT
R207	SHORT_RES0402	SHORT
R208	SHORT_RES0402	SHORT
R209	SHORT_RES0402	SHORT
R217	0613952R66	RES, 0
R3250DNP	0613952R66	RES, 0
R3970DNP	0613952R66	RES, 0
R406	0613952R66	RES, 0
R407	0613952R66	RES, 0
R801	SHORT_RES0402	SHORT
R802	0613952R66	RES, 0
R804	0613952R66	RES, 0
R803DNP	0613952R66	RES, 0
R812	0613952R66	RES, 0
R813	0613952Q49	RES, 100
R830DNP	0613952R66	RES, 0
R882	0613952Q65	RES, 470
R901	SHORT_RES0402	SHORT
R902	0613952R66	RES, 0
R903	SHORT_RES0402	SHORT
R904	0613952Q33	RES, 22
R906	SHORT_RES0402	SHORT
R907	SHORT_RES0402	SHORT
R908	SHORT_RES0201	SHORT
R909	SHORT_RES0201	SHORT
R910	SHORT_RES0402	SHORT
R913	0613952R66	RES, 0
R914	0613952R66	RES, 0
R915	0613952R01	RES, 10K
R916	SHORT_RES0402	SHORT
R917	0613952R66	RES, 0
R1010	SHORT_RES0402	SHORT
R1011	SHORT_RES0402	SHORT
R1034	SHORT_RES0402	SHORT
R1035	SHORT_RES0402	SHORT
R1038	0613952R66	RES, 0
R1300	SHORT_RES0402	SHORT
R1301	SHORT_RES0402	SHORT
R1404	SHORT_RES0402	SHORT

Table 4-9. Electrical Parts List - R1405 to R5101

Reference Number	Part Number	Description
R1405	SHORT_RES0402	SHORT
R3001	0687874L02	RES, 0.1
R3100	SHORT_RES0402	SHORT
R3101	0687874L02	RES, 0.1
R3150	SHORT_RES0402	SHORT
R3210	0613952P43	RES, 274K
R3211	0613952P09	RES, 121K
R3350	SHORT_RES0402	SHORT
R3650	0613952Q77	RES, 1.5K
R3651	0613952Q33	RES, 22
R3652	0613952Q33	RES, 22
R3654	0613952R17	RES, 47K
R3900	0613952R01	RES, 10K
R3901	0613952R22	RES, 75K
R3902	SHORT_RES0402	SHORT
R3960	0687874L01	RES, 0.24
R3961	0688044N02	RES, 20m
R3962	0613952Q91	RES, 5.6K
R3963	0613952R32	RES, 200K
R3965	SHORT_RES0402	SHORT
R3971	0613952R66	RES, 0
R3975	SHORT_RES0402	SHORT
R4100	0613952Q89	RES, 4.7K
R4300	0613952R17	RES, 47K
R4301	0613952R17	RES, 47K
R4302	0613952Q89	RES, 4.7K
R4303	0613952N34	RES, 22.1K
R4304	0613952P02	RES, 102K
R4306	0613952P43	RES, 274K
R4400	0613952Q49	RES, 100
R4401	0613952Q73	RES, 1K
R4402	0613952R08	RES, 20K
R4550	0613952Q91	RES, 5.6K
R4901	0613952R17	RES, 47K
R4902	0613952P42	RES, 267K
R4903	0613952N34	RES, 22.1K
R4904	0613952P51	RES, 332K
R4905	0613952N01	RES, 10K
R4906	0613952N58	RES, 39.2K
R4907	0613952N01	RES, 10K
R5000	0613952R25	RES, 100K
R5001	0613952R17	RES, 47K
R5100	0613952R01	RES, 10K
R5101	0613952Q03	RES, 1.2

Table 4-10. Electrical Parts List - R5102 to U880

Reference Number	Part Number	Description
R5102	SHORT_RES0402	SHORT
R5117	0613952R25	RES, 100K
R5270	0613952Q37	RES, 33
R5271	0613952Q37	RES, 33
R5272	0613952Q37	RES, 33
R5273	0613952Q37	RES, 33
R5274	0613952Q37	RES, 33
R5275	0613952Q37	RES, 33
R5279	0613952R25	RES, 100K
R5401	0613952Q89	RES, 4.7K
R5402	0613952Q49	RES, 100
R5501	0613952Q91	RES, 5.6K
R5502	0613952R66	RES, 0
R5503	0613952R66	RES, 0
R5504	0613952R66	RES, 0
R5505	SHORT_RES0402	SHORT
SH1	2687855Y01	SHIELD
SH2	2687854Y01	SHIELD
SH3	2688505Y02	SHIELD
SH4	2687859Y01	SHIELD
SH5	2687856Y01	SHIELD
SH6	2687858Y01	SHIELD
SH7	2687857Y01	SHIELD
SH8	2687860Y01	SHIELD
SH9	2688064Y01	SHIELD
SW5100	4087635K01	SWITCH
SW5101	4087635K01	SWITCH
SW5102	4087635K01	SWITCH
SW5103	4087635K01	SWITCH
T901	5885949K04	HHM1515
T902	5885949K06	HHM1526
T903	5885949K06	HHM1526
TP4200	TPSM2_032SQ	TEST_POINT
TP4201	TPSM2_032SQ	TEST_POINT
U001	5109944C61	MC13820
U100	5188450M23	50M23
U1019DNP	5114007M39	NL17SZ08
U101DNP	5113837M44	NL17SZ16
U1020DNP	5109522E82	NC7SB3157
U200	5188450M21	50M21
U3971DNP	5109522E90	NC7SP125
U400	5189552N01	MMM5092
U800	5188220Y02	20Y02
U880	5109768D12	LM20BIM

Table 4-11. Electrical Parts List - U900 to Y3982

Reference Number	Part Number	Description
U900	4889717N03	17N03
U1000	5199169K06	DSPIO
U1300	5199187J01	PF48F4400L0YBP0
U1305	5114007M44	NL17SV08
U1306	5114007M44	NL17SV08
U1400	5199188J01	HYB18L128160BF
U3000	5185941F02	TWL93010DGZGR
U3200	5188128Y01	TPS62021
U3650	5164751E03	MC74VHC1GT50
U5000	4889526L12	CSPEMI306AG
U5001	4889526L13	CSPEMI307AG
U5100	4889526L12	CSPEMI306AG
U5101	4889526L12	CSPEMI306AG
U5104	4889526L14	CSPEMI202AG
U5200	5114007M40	74VCXH245MNR2G
U5201	5114007M40	74VCXH245MNR2G
U5202	4889526L12	CSPEMI306AG
U5203	4889526L12	CSPEMI306AG
U5204	4889526L12	CSPEMI306AG
VS4200	4809948D49	CSPESD304G
VS4300	4809788E21	MM3Z6V8ST1G
VS4301	4809788E22	MM3Z8V2ST1G
VS5001	4888581Y01	SD15C_TCT
VS5002	4813979M40	SD05T1G
VS5003	4809948D49	CSPESD304G
VS5100	4809948D49	CSPESD304G
VS5101	4813979M41	NZQA6V8AXV5T1
VS5102	4813979M41	NZQA6V8AXV5T1
VS5103	4809948D49	CSPESD304G
VS5104	4809948D49	CSPESD304G
VS5201	4813979M41	NZQA6V8AXV5T1
VS5202	4813979M41	NZQA6V8AXV5T1
VS5400	4809788E21	MM3Z6V8ST1G
Y500	4809718L24	18L24
Y3982	4809995L20	MC146

V980 Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the V980 UMTS/GSM handset.

Table 4-1. Electrical Parts List - A1 to C501

Reference Number	Part Number	Description
A1	3989013L05	CONTACT
B5400	0990107N01	CONN_J
C001	2113743N05	CAP, 1.2pF
C004	2186463Z07	CAP, 0.3pF
C007	2113743L41	CAP, .01uF
C008	2113743N26	CAP, 10pF
C003DNP	2113743N03	CAP, 1pF
C005DNP	2113743N03	CAP, 1pF
C010	2113743N03	CAP, 1pF
C011DNP	2113743N07	CAP, 1.5pF
C020	2113743N38	CAP, 33pF
C021	2113743N38	CAP, 33pF
C022	2113743N38	CAP, 33pF
C023	2113743N38	CAP, 33pF
C100	2113928C04	CAP, 4.7uF
C101	2113928C04	CAP, 4.7uF
C102	2113743N38	CAP, 33pF
C103	2113928P04	CAP, 1.0uF
C104	2113928P04	CAP, 1.0uF
C105	2113928P04	CAP, 1.0uF
C106	2113928P04	CAP, 1.0uF
C110	2113743L21	CAP, 1500pF
C111	2113743L41	CAP, .01uF
C112	2113743L21	CAP, 1500pF
C113	2113743L41	CAP, .01uF
C115	2113743N40	CAP, 39pF
C114DNP	2113743M24	CAP, 0.1uF
C200	2113928C04	CAP, 4.7uF
C221	2113743N28	CAP, 12pF
C400	2113928C04	CAP, 4.7uF
C401	2113946D02	CAP, 1.0uF
C402	2113946D02	CAP, 1.0uF

Table 4-2. Electrical Parts List - C800 to C1020

Reference Number	Part Number	Description
C403	2113743L41	CAP, .01uF
C404	2113743N26	CAP, 10pF
C406	2113743N40	CAP, 39pF
C407	2113946D02	CAP, 1.0uF
C408	2113743N03	CAP, 1pF
C501	2113743L41	CAP, .01uF
C800	2113928C12	CAP, 10uF
C801	2113743E20	CAP, 0.1uF
C802	2113743E20	CAP, 0.1uF
C803	2113743E20	CAP, 0.1uF
C804	2113743E20	CAP, 0.1uF
C806	2113743E20	CAP, 0.1uF
C807	2113743N26	CAP, 10pF
C808	2113743N26	CAP, 10pF
C809	2113743N09	CAP, 2pF
C810	2113743N09	CAP, 2pF
C811	2113743N40	CAP, 39pF
C812	2113743N10	CAP, 2.2pF
C813	2113743N26	CAP, 10pF
C881	2113743L41	CAP, .01uF
C882	2113743L41	CAP, .01uF
C901	2113928C04	CAP, 4.7uF
C902	2113928C04	CAP, 4.7uF
C903	2113928C04	CAP, 4.7uF
C904	2113928C04	CAP, 4.7uF
C906	2113743N15	CAP, 3.6pF
C907	2113743L41	CAP, .01uF
C908	2113743L41	CAP, .01uF
C909	2113743L41	CAP, .01uF
C915	2113743N40	CAP, 39pF
C916	2113743N40	CAP, 39pF
C917	2113743N40	CAP, 39pF
C918	2113743N40	CAP, 39pF
C921	2113743N40	CAP, 39pF
C1000	2113743N40	CAP, 39pF
C1002	2113947H01	CAP, 0.1uF
C1003	2113947H01	CAP, 0.1uF

Table 4-3. Electrical Parts List - C1021 to C3401

Reference Number	Part Number	Description
C1004	2113947H01	CAP, 0.1uF
C1005	2113743M24	CAP, 0.1uF
C1007	2113947H01	CAP, 0.1uF
C1008	2113947H01	CAP, 0.1uF
C1009	2113743M24	CAP, 0.1uF
C1012	2113947H01	CAP, 0.1uF
C1013	2113947H01	CAP, 0.1uF
C1014	2113947H01	CAP, 0.1uF
C1015	2113743M24	CAP, 0.1uF
C1016	2113947H01	CAP, 0.1uF
C1017	2113947H01	CAP, 0.1uF
C1018	2113947H01	CAP, 0.1uF
C1020	2113743M24	CAP, 0.1uF
C1021	2113947H01	CAP, 0.1uF
C1023	2113947H01	CAP, 0.1uF
C1024	2113947H01	CAP, 0.1uF
C1025	2113743M24	CAP, 0.1uF
C1026	2113743M24	CAP, 0.1uF
C1028	2113743M24	CAP, 0.1uF
C1031	2113947H01	CAP, 0.1uF
C1032	2113743M24	CAP, 0.1uF
C1038	2113743M24	CAP, 0.1uF
C1300	2113947H01	CAP, 0.1uF
C1301	2113743M24	CAP, 0.1uF
C1302	2113743M24	CAP, 0.1uF
C1304	2113947H01	CAP, 0.1uF
C1306	2113743M24	CAP, 0.1uF
C1307	2113743M24	CAP, 0.1uF
C1308	2113743M24	CAP, 0.1uF
C1310	2113743M24	CAP, 0.1uF
C1402	2113743M24	CAP, 0.1uF
C1403	2113743M24	CAP, 0.1uF
C1404	2113743M24	CAP, 0.1uF
C1405	2113743M24	CAP, 0.1uF
C1406	2113743M24	CAP, 0.1uF
C201DNP	2113743N26	CAP, 10pF
C202DNP	2113743N26	CAP, 10pF

Table 4-4. Electrical Parts List - C3500 to C4300

Reference Number	Part Number	Description
C203DNP	2113743N26	CAP, 10pF
C222DNP	2113743N28	CAP, 12pF
C3000	2113928C12	CAP, 10uF
C3001	2113928C12	CAP, 10uF
C3002	2113743M24	CAP, 0.1uF
C3050	2113928P04	CAP, 1.0uF
C3100	2113928C12	CAP, 10uF
C3101	2113928C12	CAP, 10uF
C3102	2113743M24	CAP, 0.1uF
C3150	2113928P04	CAP, 1.0uF
C3151	2113743N38	CAP, 33pF
C3200	2113743N44	CAP, 56pF
C3201	2113928C12	CAP, 10uF
C3202	2113743N54	CAP, 150pF
C3205	2113928C12	CAP, 10uF
C3250	2113743M24	CAP, 0.1uF
C3300	2113928P04	CAP, 1.0uF
C3350	2113928C04	CAP, 4.7uF
C3400	2113928Z11	CAP, 22uF
C3401	2113743M24	CAP, 0.1uF
C3500	2113928Z11	CAP, 22uF
C3501	2113743M24	CAP, 0.1uF
C3550	2113928P04	CAP, 1.0uF
C3600	2113928P04	CAP, 1.0uF
C3654	2113928P04	CAP, 1.0uF
C3800	2113928P04	CAP, 1.0uF
C3801	2113928P04	CAP, 1.0uF
C3850	2113928P04	CAP, 1.0uF
C3851	2113928P04	CAP, 1.0uF
C3906	2113743N38	CAP, 33pF
C3910	2113743M24	CAP, 0.1uF
C3911DNP	2113928P04	CAP, 1.0uF
C3951	2113928C04	CAP, 4.7uF
C3960	2113928C12	CAP, 10uF
C3961	2113928C12	CAP, 10uF
C3962	2113743M24	CAP, 0.1uF
C3965	2113743M24	CAP, 0.1uF

Table 4-5. Electrical Parts List - C4300 to C5203

Reference Number	Part Number	Description
C3970	2113928P04	CAP, 1.0uF
C3971DNP	2113743M24	CAP, 0.1uF
C3983	2113743N26	CAP, 10pF
C3984	2113743N26	CAP, 10pF
C3985DNP	2113743M24	CAP, 0.1uF
C3990	2113743M24	CAP, 0.1uF
C4001	2113743L21	CAP, 1500pF
C4002	2113928N01	CAP, 0.1uF
C4000DNP	2113743N38	CAP, 33pF
C4003DNP	2113743N38	CAP, 33pF
C409DNP	2113743N03	CAP, 1pF
C4100	2113928N01	CAP, 0.1uF
C4103	2113743N38	CAP, 33pF
C4104	2113743N26	CAP, 10pF
C4105	2113928P04	CAP, 1.0uF
C4101DNP	2113743N38	CAP, 33pF
C4102DNP	2113743N38	CAP, 33pF
C4203	2113743N38	CAP, 33pF
C4204	2113743N38	CAP, 33pF
C4208	2113743N38	CAP, 33pF
C4209	2113743N38	CAP, 33pF
C4210	2113928C04	CAP, 4.7uF
C4211	2113743N38	CAP, 33pF
C4212	2113743L13	CAP, 680pF
C4213	2113928N01	CAP, 0.1uF
C4214	2113743N38	CAP, 33pF
C4300	2113743N38	CAP, 33pF
C4301	2113743L41	CAP, .01uF
C4302	2113743L41	CAP, .01uF
C4304	2113928N01	CAP, 0.1uF
C4305	2113928N01	CAP, 0.1uF
C4306	2113928Z11	CAP, 22uF
C4308DNP	2113743N38	CAP, 33pF
C4310	2113928N01	CAP, 0.1uF
C4356	2113928Z11	CAP, 22uF
C4392	2113743N40	CAP, 39pF
C4393	2113743N40	CAP, 39pF

Table 4-6. Electrical Parts List - C5204 to J5100

Reference Number	Part Number	Description
C4400	2113928P04	CAP, 1.0uF
C4401	2113928N01	CAP, 0.1uF
C4403	2113928P04	CAP, 1.0uF
C4402DNP	2113743N38	CAP, 33pF
C4501	2113928N01	CAP, 0.1uF
C4502	2113928P04	CAP, 1.0uF
C4503	2113928N01	CAP, 0.1uF
C4500DNP	2113743N38	CAP, 33pF
C4504DNP	2113743N38	CAP, 33pF
C4550	2113743L33	CAP, 4700pF
C4551	2113928N01	CAP, 0.1uF
C4901	2113928N01	CAP, 0.1uF
C4902	2113743L41	CAP, .01uF
C4903	2113743L41	CAP, .01uF
C5000	2113743M24	CAP, 0.1uF
C5001	2113743N38	CAP, 33pF
C5002	2113743N38	CAP, 33pF
C5003	2113928P04	CAP, 1.0uF
C5111	2113743N38	CAP, 33pF
C5112	2113743N38	CAP, 33pF
C5113	2113743N38	CAP, 33pF
C5114	2113743N38	CAP, 33pF
C5115	2113743N38	CAP, 33pF
C5116	2113743N38	CAP, 33pF
C5118	2113743N38	CAP, 33pF
C5119	2113743N38	CAP, 33pF
C5120	2113743N38	CAP, 33pF
C5121	2113743N38	CAP, 33pF
C5122	2113743N40	CAP, 39pF
C5123	2113743L41	CAP, .01uF
C5200	2113743M24	CAP, 0.1uF
C5201	2113743M24	CAP, 0.1uF
C5202	2113743M24	CAP, 0.1uF
C5203	2113947H01	CAP, 0.1uF
C5204	2113743M24	CAP, 0.1uF
C5205	2113947H01	CAP, 0.1uF
C5206	2113743M24	CAP, 0.1uF

Table 4-7. Electrical Parts List - J5212 to R105

Reference Number	Part Number	Description
C5207	2113743N38	CAP, 33pF
C5208	2113743N38	CAP, 33pF
C5400	2113928C04	CAP, 4.7uF
C5503	2113743N26	CAP, 10pF
C5508	2113743N26	CAP, 10pF
C5501DNP	2113743N26	CAP, 10pF
C5502DNP	2113743N26	CAP, 10pF
C5505DNP	2113743N26	CAP, 10pF
C815DNP	2113743N26	CAP, 10pF
C816DNP	2113743N26	CAP, 10pF
C910DNP	2113743L41	CAP, .01uF
C911DNP	2113743L41	CAP, .01uF
C912DNP	2113743L41	CAP, .01uF
C913DNP	2113743N26	CAP, 10pF
C914DNP	2113743N26	CAP, 10pF
C919DNP	2113743N15	CAP, 3.6pF
C920DNP	2113743N15	CAP, 3.6pF
CR3000	4809924D18	RB520S-30
CR5401	4809948D42	RB751V40
D901	4809948D37	BA892
D3100	4809653F07	MBRM120ET3
D3961	4809653F07	MBRM120ET3
D3962	4809653F07	MBRM120ET3
D5000DNP	4809948D42	RB751V40
E501	SHORT_RES0402	SHORT
E800	SHORT_RES0201	SHORT
E801	SHORT_RES0201	SHORT
FL001	4889729N03	FEM3203_ES6D
FL002	9109674L20	S0351
FL003	9109674L21	CF61A5601
FL004	9109674L17	74L17
FL100	9188695K05	CSPRC032AG
FL900	9109239M38	SAFSD2G14
FL4300	4889526L14	CSPEMI202AG
FL5200	9188916Y01	NFA21SL
FL5201	9188916Y01	NFA21SL
J3901	3989655N02	CONTACT

Table 4-8. Electrical Parts List - R106 to R1404

Reference Number	Part Number	Description
J4100	0909195E05	CONN_J
J4300	0989675N03	CONN_J
J5000	0987636K07	CONN_J
J5100	0987817K06	CONN_J
J5212	0989851N01	CONN_J
J5500	0185923C01	CONN_J
L002	2488090Y09	IDCTR, 4.7nH
L003	2488090Y08	IDCTR, 3.9nH
L004	2489711L11	IDCTR, 10nH
L005	2488090Y05	IDCTR, 2.2nH
L006	2487319K01	IDCTR, 1.0nH
L009	2488090Y17	IDCTR, 22nH
L007DNP	2488090Y08	IDCTR, 3.9nH
L008DNP	2488090Y17	IDCTR, 22nH
L201	2488090Y17	IDCTR, 22nH
L800	2487996L04	EXCML16
L801	2488090Y07	IDCTR, 3.3nH
L802	2488090Y12	IDCTR, 8.2nH
L803	2488090Y12	IDCTR, 8.2nH
L901	2488090Y09	IDCTR, 4.7nH
L3000	2588079Y03	IDCTR, 10uH
L3100	2590031N05	IDCTR, 6.8uH
L3206	2588079Y03	IDCTR, 10uH
L4399	2409646M13	IDCTR, 39nH
L4400	2409646M13	IDCTR, 39nH
M100	1188983Y01	1188983Y01
M101	1188983Y01	1188983Y01
M102	1188983Y01	1188983Y01
M103	1188983Y01	1188983Y01
M3000	5987774N01	MR-2561
M5400	3987697Y02	CONTACT
N001	0987378K01	SWITCH
Q3401	4813824M88	NSL12AW
Q3501	4813824M88	NSL12AW
Q3960	4805585Q23	SI8401DB
Q3961	4805585Q23	SI8401DB
Q3963	4888585Y01	SI8405DB

Table 4-9. Electrical Parts List - R1405 to R5001

Reference Number	Part Number	Description
Q3964	4805585Q23	SI8401DB
Q3974	4809579E02	2SK1830
Q5001	5109817F58	17F58
Q5100	4813824A17	MMBT3906
R001	0662057M01	RES, 0
R002	0662057M88	RES, 3.9K
R003	0662057M81	RES, 2K
R006	0662057M01	RES, 0
R103	SHORT_RES0402	SHORT
R104	SHORT_RES0402	SHORT
R105	SHORT_RES0402	SHORT
R106	SHORT_RES0402	SHORT
R111	0662057M78	RES, 1.5K
R113	0662057M78	RES, 1.5K
R114	0662057N23	RES, 100K
R200	0662057M40	RES, 39
R203	0662057M01	RES, 0
R204	0662057M01	RES, 0
R206	SHORT_RES0402	SHORT
R207	SHORT_RES0402	SHORT
R208	SHORT_RES0402	SHORT
R209	SHORT_RES0402	SHORT
R212	0662057M62	RES, 330
R217	0662057M01	RES, 0
R406	0662057M01	RES, 0
R407	0662057M01	RES, 0
R801	SHORT_RES0402	SHORT
R802	0662057M01	RES, 0
R804	0662057M01	RES, 0
R812	0662057M01	RES, 0
R813	0662057M50	RES, 100
R882	0662057M66	RES, 470
R901	SHORT_RES0402	SHORT
R902	0662057M01	RES, 0
R903	SHORT_RES0402	SHORT
R904	0662057M34	RES, 22
R906	SHORT_RES0402	SHORT

Table 4-10. Electrical Parts List - R5100 to U200

Reference Number	Part Number	Description
R907	SHORT_RES0402	SHORT
R908	SHORT_RES0201	SHORT
R909	SHORT_RES0201	SHORT
R910	SHORT_RES0402	SHORT
R913	0662057M01	RES, 0
R914	0662057M01	RES, 0
R915	0662057M98	RES, 10K
R916	SHORT_RES0402	SHORT
R917	0662057M01	RES, 0
R1010	SHORT_RES0402	SHORT
R1011	SHORT_RES0402	SHORT
R1034	SHORT_RES0402	SHORT
R1035	SHORT_RES0402	SHORT
R1038	0662057M01	RES, 0
R1032DNP	0662057M01	RES, 0
R1300	SHORT_RES0402	SHORT
R1303	SHORT_RES0402	SHORT
R1404	SHORT_RES0402	SHORT
R1405	SHORT_RES0402	SHORT
R3001	0687874L02	RES, 0.1
R3100	SHORT_RES0402	SHORT
R3101	0687874L02	RES, 0.1
R3150	SHORT_RES0402	SHORT
R3210	0662057V41	RES, 270K
R3211	0662057V29	RES, 120K
R3250DNP	0662057M01	RES, 0
R3350	SHORT_RES0402	SHORT
R3650	0662057M78	RES, 1.5K
R3651	0662057M34	RES, 22
R3652	0662057M34	RES, 22
R3654	0662057N15	RES, 47K
R3900	0662057M98	RES, 10K
R3901	0662057N20	RES, 75K
R3902	SHORT_RES0402	SHORT
R3960	0687874L01	RES, 0.24
R3961	0688044N02	RES, 20m
R3962	0662057M92	RES, 5.6K

Table 4-11. Electrical Parts List - U3971 to Y3982

Reference Number	Part Number	Description
R3963	0662057N30	RES, 200K
R3965	SHORT_RES0402	SHORT
R3971	0662057M01	RES, 0
R3975	SHORT_RES0402	SHORT
R3970DNP	0662057M01	RES, 0
R4100	0662057M90	RES, 4.7K
R4300	0662057N15	RES, 47K
R4301	0662057N15	RES, 47K
R4302	0662057M90	RES, 4.7K
R4303	0662057V11	RES, 22K
R4304	0662057V27	RES, 100K
R4306	0662057V41	RES, 270K
R4400	0662057M50	RES, 100
R4401	0662057M74	RES, 1K
R4402	0662057N06	RES, 20K
R4550	0662057M92	RES, 5.6K
R4901	0662057N15	RES, 47K
R4902	0662057V41	RES, 270K
R4903	0662057V11	RES, 22K
R4904	0662057V43	RES, 330K
R4905	0662057V02	RES, 10K
R4906	0662057V17	RES, 39K
R4907	0662057V02	RES, 10K
R5000	0662057N23	RES, 100K
R5001	0662057N15	RES, 47K
R5100	0662057M98	RES, 10K
R5101	0662057M03	RES, 1.2
R5102	SHORT_RES0402	SHORT
R5117	0662057N23	RES, 100K
R5270	0662057M38	RES, 33
R5271	0662057M38	RES, 33
R5272	0662057M38	RES, 33
R5273	0662057M38	RES, 33
R5274	0662057M38	RES, 33
R5275	0662057M38	RES, 33
R5279	0662057N23	RES, 100K
R5401	0662057M90	RES, 4.7K