MOTOROLA

Personal Communications Sector

GSM
Service Support
Level 3 Authorized

GSM Service Support

Training - Documentation - Engineering

Level 3
Circuit Description
12 / 10 / 00
V1.0

RF: Receive

1) The RF Signal from the base station is received through the Antenna A1 on the antenna board, which is contained within the flip Assembly, to **J3** on the transceiver board, or from the Auxiliary Phasing Connector J2. It is then fed to **Pin 10** or **Pin 3** respectively of the RF Switch U150, the switch acts as isolation between TX and RX. The RF Switch control is provided by U151.This decides whether the Switch is opened for TX or RX and if the RF is passed to the Aux RF port or the Antenna. This is managed by the following signals:

TX_EN	RX_EN	SW_RF (50W Load)	Result
H	L	Loaded	TX through J2
L	H	Loaded	RX through J2
H	L	Not Loaded	TX through Antenna
L	H	Not Loaded	RX through Antenna

2) **TX_EN** and **RX_EN** are produced by Whitecap U800, **Pins C1** and **E3** respectively.U151 is supported by the voltages **FILTERED –5V**(From **–5V** (U903)) and **RF_V1**(Q201)

3) Once the received signal is present (using GSM 900 as the example) in the RF switch. Provided **RX275_GSM_PCS** (Q2101) is high, then the received signal will be passed to the band pass filter FL400, GSM900received frequency will be filtered through, *Note **RX275_GSM_PCS** also selects the PCS 1900 frequency passed through FL2400. The DCS 1800 frequency is selected by **RX275_DCS** (Q110) and passed through FL1400

4) For the PCS 1900 and DCS 1800 frequencies the signal is then fed onto the DCS/PCS Select switch U400. The signal **RVCO_PCS** and **RVCO_DCS** (Q1100) will then select the appropriate signal; with output tuning being provided by L1411 and C1411 for DCS and C2411 for PCS.

5) Once selected the signal will be fed into a Low noise Amplifier Circuit, this part of the circuit is critical in the achievement of a very low signal to noise ratio, therefore as can be seen around the actual amplifiers Q400 for GSM (supported by **RX275_GSM** (Q110)) and Q1400 for DCS / PCS (supported by **RX275_DPCS** (Q2102)), a large amount of external frequency matching and noise reduction circuitry is involved.

6) The appropriate signal is then fed onto FL1401 (For GSM 1800 / 1900) or FL401 (For GSM 900) where any existing harmonics or other unwanted frequencies are removed.

7) The amplified signal is now injected to the base of the dual transistor mixer Q450. Both mixers are supported by **RX275** (Q112).The tuned emitter biasing voltage is provided by **RX275_GSM** (Q110) and **RX275_DPCS** (Q2102)

8) The RX VCO U250 is now an integrated circuit and is controlled firstly from the Whitecap using the **MQ SPI** bus to program the MAGIC and then MAGIC drives the RX VCO IC using the **CP_RX** signal **Pin A1**. The power is supplied by **RVCO_275** (**SF_OUT** + **GPO4** through Q1102).
Approximate CP_RX readings are: Channel 975 – 2.08V (EGSM Low Channel)
Channel 062 – 2.40V
Channel 124 – 2.60V

9) The generated RX VCO signal is then split, with a part going back to the MAGIC IC – U200. **Pin A3** to serve as the feedback for the RX VCO Phase lock loop. The other part is firstly amplified through a Tuned Transistor Amplifier Q252, before being used to mix with the received frequencies through the emitters of the dual mixer transistor Q450.

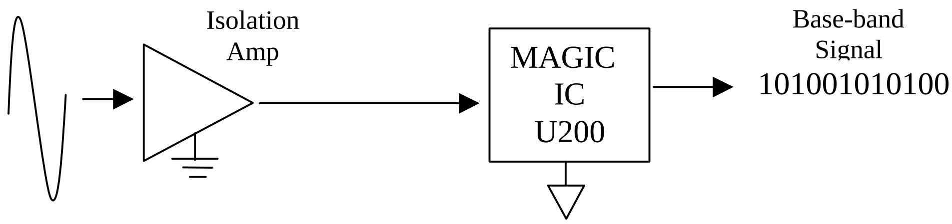
10) The mixer will produce sum and difference signals i.e. RX'ed frequency + RX VCO frequency and RX'ed frequency - RX VCO frequency. It will be the difference signal that is now fed to the SAW Filter FL457 (Surface Acoustic Wave), this filter is the same as was used in previous 400MHz products. The purpose of the SAW filter is to provide comprehensive removal of harmonics created during the mixing process.

11) The IF signal fed to the SAW filter will be 400Mhz. The reason for the change to 400Mhz from 215Mhz is to limit the span of the RX VCO e.g.

Description	IF	Channel	Received Frequency	RX VCO Frequency	Difference
EGSM L Channel	400Mhz	975	925.2Mhz	1325.2Mhz	264.6Mhz
PCS H Channel	400Mhz	810	1989.8Mhz	1589.8Mhz	
EGSM L Channel	215Mhz	975	925.2Mhz	1140.5Mhz	634.6Mhz
PCS H Channel	215Mhz	810	1989.8Mhz	1774.8Mhz	

As can be seen if the IF was kept at 215Mhz, the frequency span would have to be an extra **370Mhz.** This is turn assists in reducing the part count.

12) The 400Mhz IF signal is then passed to the Isolation Amplifier Q480
The purpose of an Isolation Amp is to couple an analogue signal to adjoining parts of a circuit that use 2 different grounds. Also to protect the base band signals from any stray RF. The Isolation Amp is supported by **SW_VCC** (MAGIC U200 **Pin C7**)



13) The signal is then passed to the MAGIC IC U200 **PRE IN Pin A7**

14) The signal is then demodulated internally using an external 800 MHz Varactor diode CR249, RX Local Oscillator set up, which is driven by **LO2 CP Pin A9** of MAGIC U200.

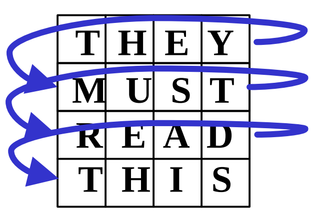
15) Where in earlier products, we used to have **RX RXQ, and I** these signals are now only used in digital form within the MAGIC and can only be measured using a specific set up. The demodulated signal is now converted internally to a base band digital form to be passed along an RX SPI bus to the Whitecap.

16) The **RX SPI** signal is made up of **BDR** (Base band Data Receive), **BFSR** (Base band Frame Synch Receive) and **BCLKR** (Base band Clock Receive, fed from MAGIC **Pins G8, G9 and F7** respectively.

17) The Whitecap U800 receives these signals on **Pins A3, D4 and B4,** within the Whitecap the signal is digitally processed.
Some of the processor functions are as follows:

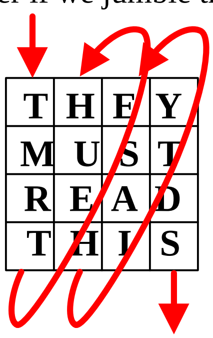
- De-Interleaving: Interleaving is a way in which the information that is to be transmitted is jumbled around before it is sent i.e.

If we wish to send the information 'They must read this'



And we lose the information during the time that 'must' is being sent. Then we will lose a whole word.

However if we jumble the bits around that make up the words, i.e. transmit in a different order.



If now during the same time frame we lose the same amount of information, then we will only lose a small part of each word

- Channel De-Multiplexing – this is where we decode the signal that was transmitted, encryption at the transmitter ends is usually done by X-ORing the information.
- Forward Error Correction Decoding – This is where the redundant bits of data that were added in the transmitter are removed, and the information that is received can be processed. The redundant bit are added in various quantities dependant upon the signal quality. This means if some data is lost whilst travelling OTA then, for example, instead of 8 bits of speech data being lost, only 4 bits of speech and 4 bits of redundant data.
- De-Segmentation and CRC Attachment analysis. – During the transmission process the data is broken into packets of various lengths (N^o of bits). These packets are then processed to give a checksum of what should be expected at the receiver. Once in the Whitecap the information received is processed, and the two checksums compared. From the analysis, the correct algorithm for repairing any data corruption can be implemented.

18) The resultant digital signal is now fed down the **DIG_AUD_SPI** bus to the GCAP II U900, internally to the GCAP, the digital signal is converted to analogue and distributed to the correct outputs:

19) The Alert is generated within the Whitecap, given the appropriate data from the incoming signal, SMS, call etc… and is fed to the Alert Pads LS1. This signal is supported by the signal **ALRT_VCC**, which is generated from B+ through Q903.

20) For the headset only the **SPKR-** signal is used from GCAP II **Pin H6**.The output is then fed out to the Headset Jack socket J504. **Pin 3.**

RF: Transmit

1) Analogue voice will be fed from the Aux Mic attached to the headset and will be routed from **Connection 1** of the Headset Jack J504, through to GCAP II, **Pin H3**.

2) Within the GCAP II the analogue audio will be converted to digital and clocked out onto the **DIG_AUD** SPI bus to the Whitecap U800.

3) It is within the Whitecap that all information about the transmission burst is formulated i.e. The timing of the burst / The channel to transmit on / The error correction protocol / In which frame the information will be carried to the base station, (see Receive, Note 17 for transmission processing).

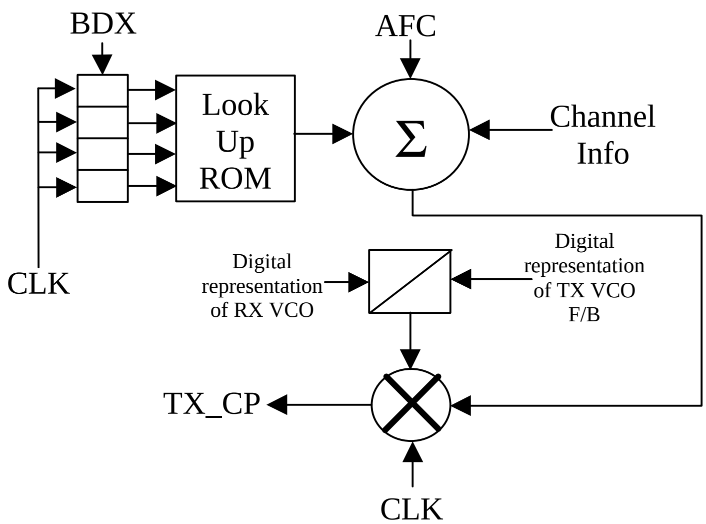
4) All this information is then added to the digitised audio and is transferred to the MAGIC U200 along a TX SPI bus. The bus is made up of **BCLKX** (Base band Clock Transmit) **Pin B3** and **BDX** (Base band Data Transmit) **Pin B6**. The timing for this data is already decided for the transmission burst, and therefore a frame synch is not required.

5) The SPI comes into the MAGIC at **Pin G7** (**BCLKX**) and **Pin J2** (**BDX**)

6) The operation of the MAGIC is very complex and with respect to the transmit path, integrates the functions of the Modem and its function of performing GMSK (Gaussian Minimum Shift Keying) and also the functions of the TIC (Translational Integrated Circuit).

7) A very basic block view of how the transmit path works within the MAGIC is demonstrated in: Fig 8.1

<u>Internal MAGIC Operation **Fig 8.1**</u>



8) The data is transmitted from Whitecap to MAGIC on TX SPI bus **BDX**, within the MAGIC each bit of data is clocked into a register. The clocked bit and the 3 preceding bits on the register are then clocked into the look up ROM, which looks at the digital word and from that information downloads the appropriate GSMK digital representation. Channel information and AFC information from MAGIC SPI is then added to this new digital word, this word is then representative of the TX IF frequency of GIFSYN products. As in the case of the TIC, the TX frequency feedback and the RX VCO frequency are mixed to give a difference signal, this is digitally phase compared with the 'modulation' from the look up ROM. The difference creates a DC error voltage **TX_CP** that forms part of the TX Phase locked loop.

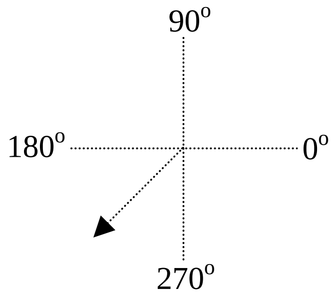
<u>Gaussian Minimum Shift Keying</u>

GMSK - Uses the idea that we always change the <u>current</u> phase of the carrier by + or - 90^{o}, the Gaussian part of the title refers to the use of a Gaussian filter that reduces the side-bands that are created during the Minimum shift keying process.

Below is a very simplistic view, of the GMSK process:
1) Firstly, we have the data to be sent = 001011
2) This is then split into the TXI & TXQ paths.
The ‘I’ Path will implement the phase change by 0^{o} or 180^{o}.(Dependant on logic level)
The ‘Q’ Path will implement the phase change by 90^{o} or 270^{o}. (Dependant on logic level)

0	1	1	TXI
0	0	1	TXQ

Therefore if we now apply the first bit of I data and the first bit of Q data. We get



I Data = 0 which is equivalent to 180^{o}
Q Data = 0 which is equivalent to 270^{o}
Therefore resultant phase shift = -135^{o}

9) The error correction voltage **TX_CP** is then fed from **Pin B1** of MAGIC to **Pin 4** of the TX VCO IC U350, adjoining this line is the loop filter (See Loop Filter document, http://gsm-service.fle.css.mot.com → Kramer → Level 4 → Other Related Documents → Block Diagram Loop Filter. This explanation is not an exact depiction of the V100 Loop filter but identifies the basic operation).

10) The Loop filter comprises mainly of U360 / Q360 / Q361 and C367 and it’s main function is to ‘smooth’ out any overshoots when the channel is changed, see Fig 11.1. If this overshoot were fed to the TX VCO the resulting burst would not meet the world standards for GSM with respect to bandwidth, see Fig 11.2.

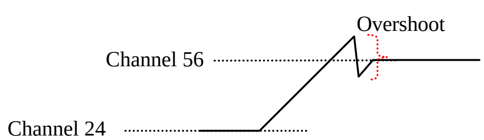


Fig 11.1

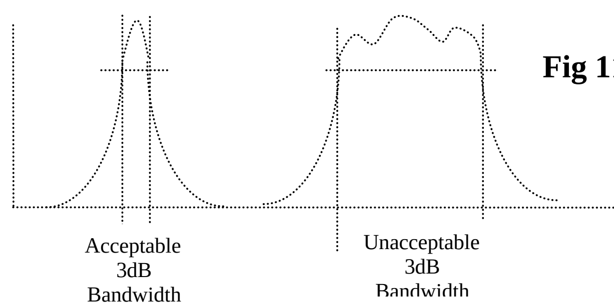


Fig 11.2

11) The Loop filter basically acts then as a huge capacitor and resistor to give a long CR time for smoothing. It uses a small capacitor and the very high input impedance buffer Op-Amp. During the **TX_EN** (Whitecap) period when the transmitter is preparing to operate the capacitor charges, then on receipt of **DM_CS** (Whitecap) when the Transmitter actually fires; the capacitor discharges through the Op-Amp giving a smooth tuning voltage, carrying modulation to the TX VCO. The support voltage for the Loop filter is **V1_FILT** (**V2** from GCAP II through Q913, then creates **V1_SW** which creates **V1_FILT**).

12) The TX VCO IC now creates our required output frequency with the support signals
TX_DCS (**TX275 + *DCS_SEL** through (U1101).
TX275_GSM (***GSM_SEL + RX275**) (Q110)
TX275_DPCS (***GSM_SEL + RX275**) (Q2102)
These signals configure the VCO for correct mode of operation i.e. GSM 900 / 1800 / 1900.
Support Voltage being **SF_OUT** (MAGIC **Pin C1**

13) The signal is then fed out through a buffer amplifier Q330, which is supported by **TX275.** The signal is also split with a sample of the output frequency being directed back to the MAGIC IC **Pin A3**, for use within the TIC part of the MAGIC as part of the TX Phase Locked Loop.

14) To prevent the output frequency from the TX VCO before stabilisation has occurred, being amplified and transmitted, there is an Isolation Diode CR330 placed. This is biased 'on' by the exciter voltage from the PAC IC U390 (Power Amplifier Control IC) **Pin 7**; this allows the TX output frequency through to the Exciter Amplifier Q331 and at same time gives more or less drive to the exciter stage.

15) The signal is then fed to a wide bandwidth PA U300, this is driven by the exciter voltage from the PAC IC, and supported by a –ve biasing voltage created and timed by **TX275** (**RF_V2 + TX_EN** through Q120), **Filtered –5V** (**-5V**) and **DM_CS** (Whitecap U800 **Pin E2**). Also supported by the voltage **PA B+** (**DM_CS + B+** through Q390)

16) PA matching is provided using the signals **TX_GSM** (**TX275 + *GSM_SEL** through Q1101) and TX_DCS (**TX275 + *DCS_SEL** through Q1101) to switch on or off the diodes CR300 through CR306 to match the PA between GSM and DCS / PCS using the inductive strips on the PCB.

17) The amplified signal is then fed back to the RF switch U150, as discussed in **Receive**, then either transmitted through J3 to the Antenna Board and onto the Antenna A1 or the Auxiliary Phasing Port J2. The Antenna is matched to the GSM 1800 / 1900 frequency and mismatched to the GSM 900 frequency, due to the extra power that is generated over the GSM 900 frequency range

RF: Power Control Operation

1) The PAC IC U390 (Power Amplifier Control Integrated Circuit) controls the power control of the transmitter. Below is a list of the main signals associated with the PAC IC and their purposes.

2) The RF detector (**RF_IN Pin 2**) provides a DC level proportional to the peak RF voltage out of the power amplifier, this is taken via an inductively coupled strip from the output of the PA U300.

3) **DET_SW Pin 11**. This pin controls the variable gain stage connected between the RF detector and the integrator. The gain of the variable stage will be unity when **DET_SW** is low and will be 3 when **DET_SW** is high (floating).

4) **TX_KEY Pin 10**. This signal is used to 'pre-charge' the Exciter and P.A. and occurs 20µS before the start of the transmit pulse.

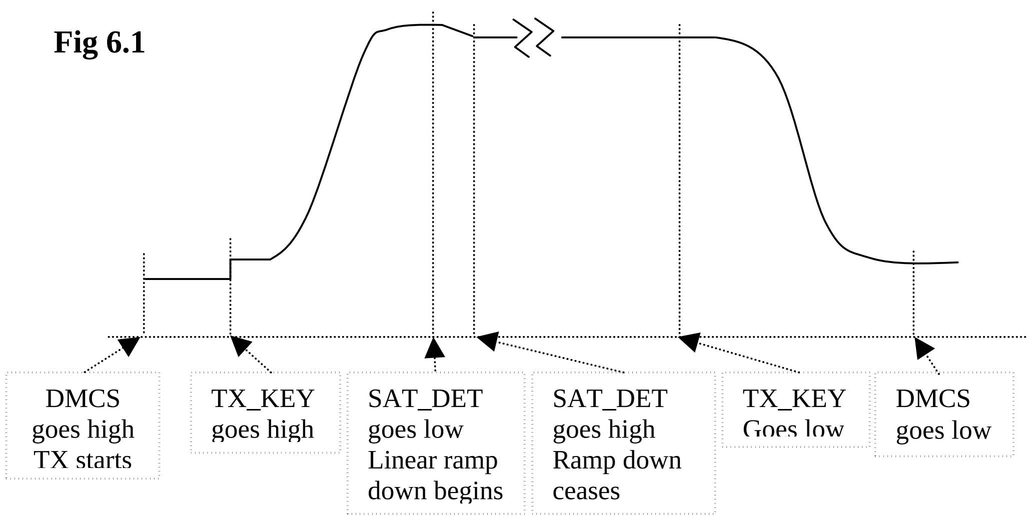
5) **EXC Pin 7**.This output drives the power control port of the exciter. An increase of this voltage will cause the exciter to increase its output power.

6) **SAT_DET Pin 12**. If the feedback signal from the RF detector lags too far behind the AOC signal then this output will go low, indicating that the loop in at or near saturation. This signals the DSP to reduce the **AOC_DRIVE** signal until **SAT_DET** rises. See **Fig 6.1**

7) **AOC_DRIVE Pin 8**. The voltage on this pin will determine the output power of the transmitter. Under normal conditions the control loop will adjust the voltage on EXC so that the power level presented to the RF detector results in equality of the voltage present at INT and AOC. The input level will be between 0 and 2.5V.

8) **ACT Pin 9**. This pin will hold a high voltage when no RF is present. Once the RF level increases enough to cause the detector to rise a few millivolts then this output will go low. In the GSM radio a resistor is routed between this point and the AOC input to cause the radio to ramp up the power until the detector goes active.

Fig 6.1



Logic: Power Up sequence

1) Three power sources are available, battery, External Power via Fast Charger and External Power via Mid-rate charger. **(Battery must be present to power up)**

2) Battery Power Source: The V100 uses the 3.6V Lithium Ion battery .The power from the battery is taken from **BATT +** (Battery contacts J604) and is routed through the Battery FET Q901. Once **B+** is available the unit carries out the following checks

- The battery temperature is monitored to establish whether rapid charge is required, (J604 **Pin 2 BATT_THERM_AD** to GCAP II **Pin B3**)
  -40 deg C – 2.75V 25 deg C – 1.39V 40 deg C – 0.96V
- Charger sensed (J600 Pin 5 **MANTEST_AD** to GCAP II **Pin A1**) This is achieved using different sense resistors within the accessory.
  For DHFA Charger - 2.75V For Fast Charger – 2.13V
  For Mid Rate Charger – 1.38V
- Senses battery voltage (GCAP II **Pin F7** – **BATTERY**)
- Senses input B+ level GCAP II **Pin E10** – **B+**)

3) Charger Power Source
When the charger is connected into the accessory plug J600, **EXT B+** will be available at **Pin 14**. This will be sensed at GCAP II U900 **Pin D10 MOBPORTB**. Once sensed the power will then be passed through the protection diode CR903 and output to the EXT B+ FET Q905. The output will be controlled by the **Mid-rate 1** signal and power will be made available at **B+**
NB. The charger supports the phone in conjunction with the batteries, therefore the batteries are charged as **B+** is supplied.

4) The GCAP II is programmed to Boost mode (5.6V) by **PGB0 Pin G7** and **PGM1 Pin G8** both being tied to Ground. Once **B+** is applied to GCAP II **Pin K5**, all the appropriate voltages to supply the circuit are provided. These are:

- **V1** – Programmed to 5.0V. **V1** is at 2.775V at immediate power on, but is ‘boosted’ to 5.0V through the switch mode power supply L901 / CR902 and C913. See Fig 6.1 for basic operation. **V1** supplies the DSC bus drivers, negative voltage regulators and MAGIC. **V1** is created from GCAP II **Pin A6** and can be measured on C906.

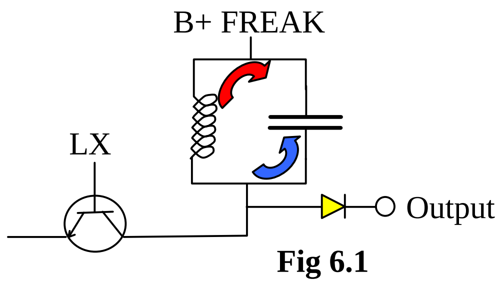


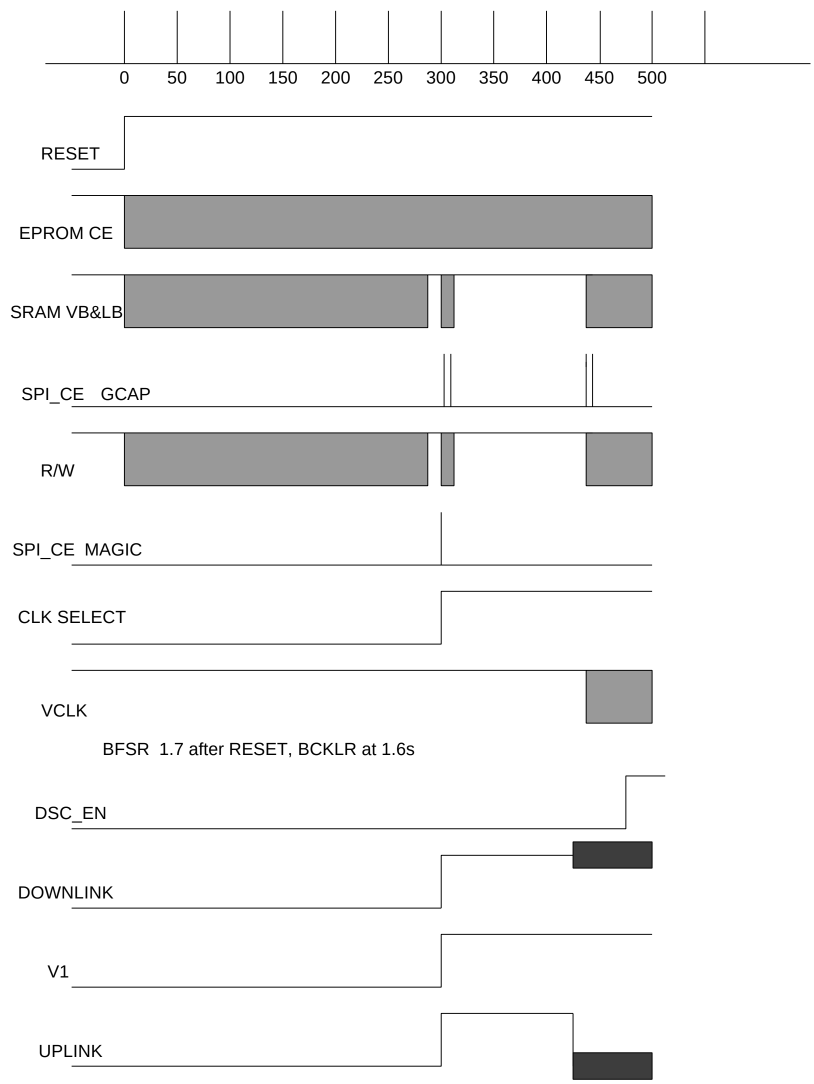
Fig 6.1

The basic circuit operation for the Boost circuit is as follows the **LX** signal (GCAP II **Pin B10**) allows a path for **B+** to charge the capacitor, when the switch is on, the capacitor then discharges through the inductor (switch off), setting up an electric field. The field then collapses setting up a back EMF to charge the capacitor, and so on and so on. The back EMF created by the inductor is greater than **B+** with the +ve half of the cycle passing through the diode to charge a capacitor from where the **V_BOOST** voltage is taken. The frequency of the switching signal **LX** decides the duty cycle of the output wave and therefore the resultant voltage. **V_BOOST** is fed back into the GCAP.

- **V2** – Programmed to 2.775V, available whenever the radio is on and supplies most of the logic side of the board. **V2** is supplied out of GCAP II **Pin J2** and can be measured on either C939 or C941.
- **V3** – Programmed to 2.003V to support the Whitecap, but does support the normal 2.75V logic output from the Whitecap, it originates from GCAP II **Pin B5** and can be measured on C909 or C910.
- **VSIM1** – Used to support either 3V or 5V SIM cards. Will dynamically be set to 3V upon power up, but if the card cannot be read then the SIM card is powered down and an attempt to read the card at 5V is tried. VSIM1 can be measured on C905 and is distributed from GCAP II **Pin C6** (For further information, see SIM Card Operation).
- **VREF** – Programmed as **V2** i.e. 2.775 and provides a reference voltage for the MAGIC IC, distributed from GCAP II **Pin G9** and can be measured on C919.
- **-5V –** Used to drive display and **–10V** – Used for RF GSM / DCS selection signals through Q160. Both voltages produced by **V1** through U903 and U904.
- **SR_VCC** – **Power Cut Circuit -** Used to buffer the SRAM U702 voltage with a built in soft reset within the unit's software. The reason for this is to protect the user from any accidental loss of power up to 0.5 seconds i.e. If the unit is knocked, causing a slight battery contact bounce, the **SR_VCC** will, to the user, keep the unit running normally, whilst internally the unit resets itself. During this loss of power the unit takes it's power from **RTC BATTERY+** and is originated from GCAP II **Pin E1**
- **V1_SW –** See **Deep Sleep Mode**

5) Once the power source has been selected to power the phone on the **PWR_SW** must be toggled low. This can be done by pressing the Power Key S500 to create **ON_2**, which is supported by **PWR_SW** (GCAP II **Pin C8**). Alternatively by plugging in an external fast charger, if a battery is present, then again the **ON_2** line will be pulled low.

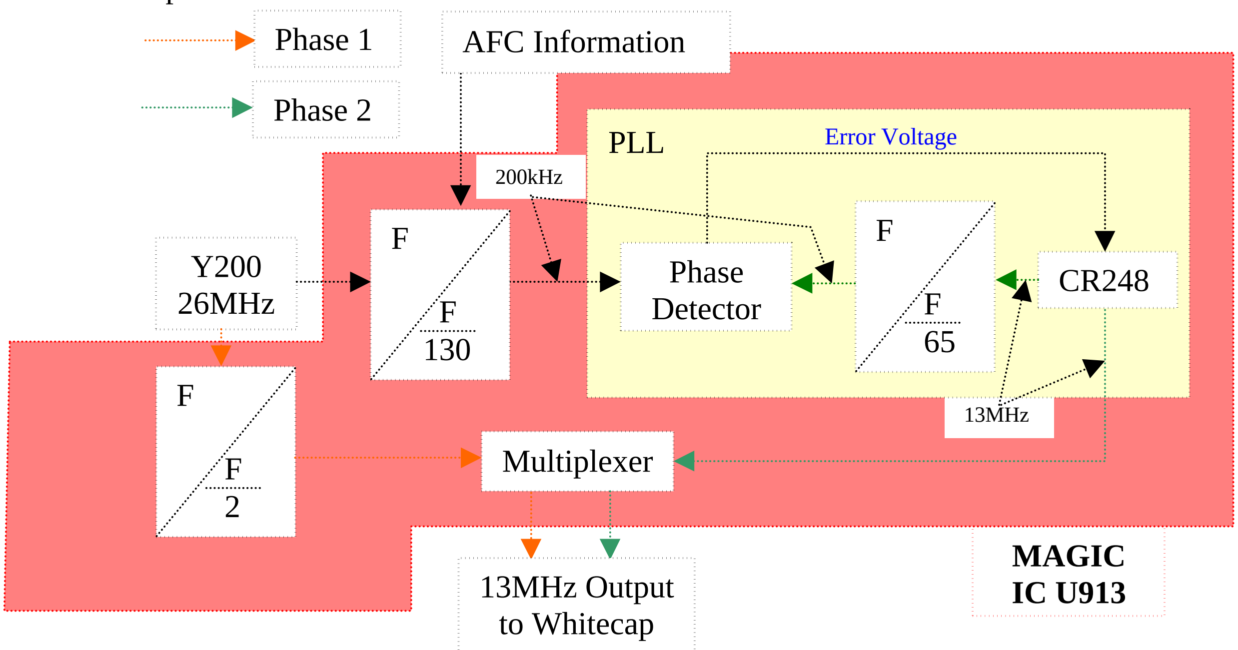
6) The unit will then follow on as in the sequence below:



On initial power up, all the keypad backlights (DS500 – DS509 and DS512 to DS522), and display backlights DS504 – DS510 will be on. They are supported from the signal **ALRT_VCC** (B+ through Q903) and switched by **BKLT_EN** (Whitecap **Pin K3**) through Q907.

7) **13 MHz clock**. On Power Up there are 2 different reference clocks produced. Initially, as soon as power is applied to the MAGIC IC the crystal, Y200, supported by the **CRYSTAL_BASE** (MAGIC **Pin E1**) will emit a 26MHz signal to the MAGIC IC, which will internally be divided by 2 to give our external 13MHz clock.

This is then fed out of the MAGIC on **Pin J6** (**MAGIC_13MHz**) and distributed to Whitecap **Pin H10** (**CLKIN**), then from Whitecap **Pin B7** to GCAP II **Pin F5** as **GCAP_CLK**. At the same time the 13MHz Varactor Diode CR248 is producing an output. This output is controlled in the following way: The 26MHz from Y200 is divided down to 200 kHz (this 200Khz is kept absolutely stable by AFC information that is derived from the feedback from the RX VCO) and is fed to a phase comparator within the MAGIC. The 13MHz from CR248 is also divided down and fed in to the phase comparator, the difference in phase produces an error voltage that is fed onto the cathode of the Varactor CR248. Which regulates the output to a stable 13MHz clock. Once the software is running and the logic side of the board has successfully powered up, the **CLK_SELECT** signal from Whitecap **Pin A1** is fed to MAGIC **Pin G6**. This in turn then switches the Multiplexer from the output of Y200 to the CR248 output.



Logic: SIM Card Interface

1) Once powered up, the SIM card is interrogated. The SIM interface is part of the Whitecap U800 and it supports both 'synchronous' (Prepay card) and asynchronous, serial data transmission. Although the T2288 is programmed only for asynchronous. **VSIM1** (**SIM_VCC**) is originally programmed to 3V but if the card is 5V then the SIM card will be powered down and **VSIM1** will be reprogrammed to 5V. The signal levels for in and out of the SIM are now required to be level shifted within GCAP II U900 to 3V.these signals are:

- **Reset** (Whitecap Pin E9 – **RST0**) in to GCAP II **Pin K7 – LS1_IN_TG1A**. This signal is then level shifted to the required voltage and fed out to SIM Contacts J803 **Pin 2** from **Pin J7** - **LS1_OUT_TG1A**.
- Clock: This is a 3.25MHz signal from Whitecap **Pin E9** – **CLK0** **Pin E7** to GCAP II **Pin G6 – LS2_IN**. This signal is then level shifted to the required voltage and fed out to SIM Contacts J803 **Pin 1** from **Pin F6** – **LS2_OUT**.

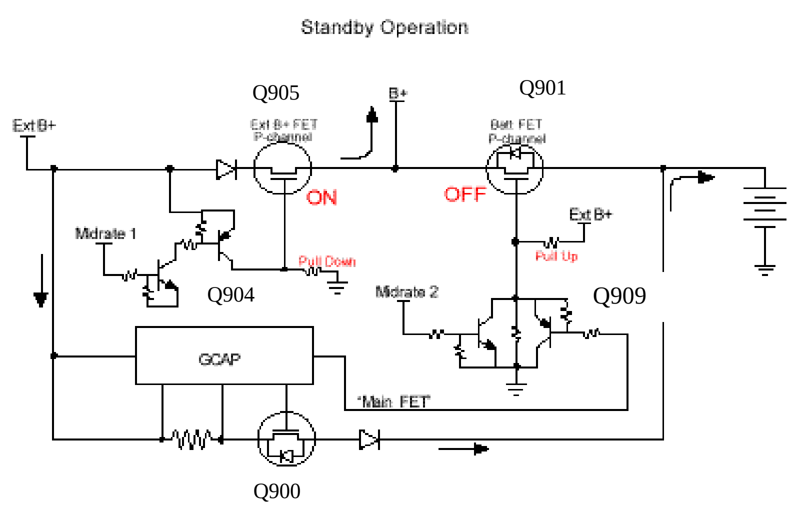
- **SIM I/O** – Data transmission to and from SIM card. For TX, from SIM card contact **SIM I/O Pin 6** through to GCAP II **Pin J8 SIM I/O**. Through level shifter to desired voltage and out through **Pin K10** (**LS3_TX_PA_B+**) to Whitecap **Pin F3 DAT0_TX**. For RX data from Whitecap **Pin B5 DATA0_RX** to GCAP II, **Pin H8 – LS3_RX** where the signal is level shifted to desired voltage and outputted on **Pin J8 SIM I/O** to SIM contacts **Pin 6 SIM I/O**.
- **SIM_PD** – This signal is provided by using the **BATT_THERM** contact of the battery. If there are no batteries present then the unit will not power up. If batteries are present, but colder than –15 deg C and no card is inserted then the output of the comparator Q905 will stay high and the unit will display ***'Insert Card'***. Once the battery temperature goes above that, (**BATT_THERM** Voltage approximately 2.51V) but the SIM card is either not inserted or faulty '***CHECK CARD*** ' will be displayed. The reason behind this is to prevent the extra cost of a mechanical SIM presence detect switch and to prevent the SIM card being removed whilst connected to Aux Power.

Logic: Charger Circuit

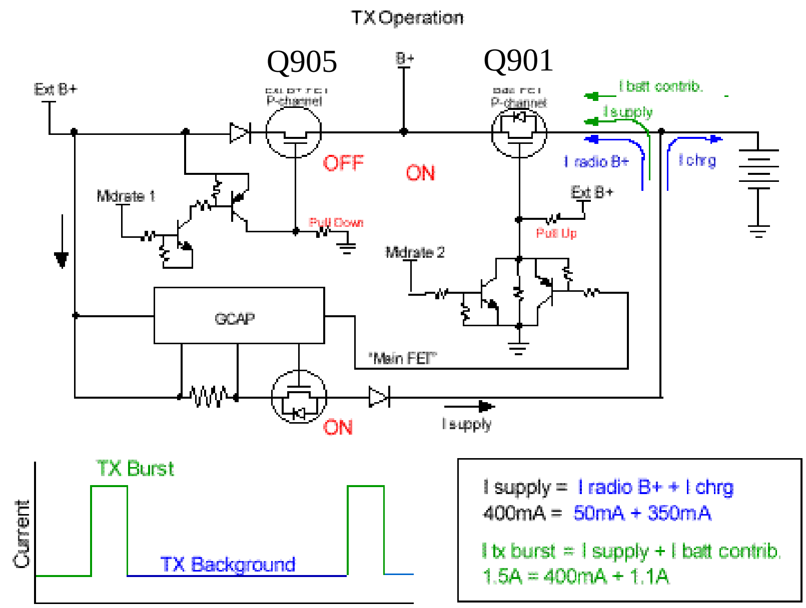
1) As was mentioned earlier for the V100, we use either the mid-rate charger or the full rate charger. The operation of which is as follows:

In standby, the phone requires approximately 50mA for support so Q905 is opened, and as the charger can support 400mA. The phone also opens Q900, controlled by **CHRGC** (GCAP II **Pin E8**). This allows a charge of 350mA to charge the battery. The current is monitored Current Sense Resistor R913; the voltage drop over this resistor is looked at by GCAP II **Pin D9 – I_SENSE**, to monitor the charge being delivered.

Mid-rate 1 = 0 **Mid-rate 2** = 0



Whilst in a Transmit mode of operation, the unit requires up to 1.5A to be supplied during each burst.



Whilst in background mode the phone operates as in standby mode with 50mA supporting the phone and 350mA charging the battery, but this time the EXT B+ FET Q905 is switched off and therefore the charger current is directed through the charging FET Q900. In this state **Mid-rate 1** = 0 **Mid-rate 2** = 1
During a TX pulse the full 400mA from the charger supports **B+** with addition to approximately 1.1A from the battery.
For this state **Mid-rate 1** = 1 **Mid-rate 2** = 1

Logic: Deep Sleep Mode

Deep sleep mode is there to provide a facility to save battery life by intermittently shutting off part of the PCB. This is achieved in the following way. The signal **STBY_DL** is generated from Whitecap **Pin F1**, through a standby delay circuit CR912 and U906. The logic gate U906 and diode CR912 are used to provide a short delay between the time of activation of the **STBY_PC5** signal and to the **STBY_DL** signal. This is a hardware patch for timing issues related to the Whitecap's Deep Sleep Module (DSM). The resultant signal is then passed onto Q834 and Q912. This has the effect respectively of:

1) Grounding **VREF** which makes MAGIC inoperable
2) Grounding **V2** This switches off MAGIC, Front END IC and inhibits the Transmit path through **RF_V2**
3) The shutdown is only for a fraction of a second and during that time the GCAP Clock supports the logic side of the unit. The GCAP clock is generated by Y900, which generates a 32.768MHz clock. This clock is output from Whitecap **Pin C7** and fed directly to Whitecap **Pin P4**. The clock is always monitored by Whitecap and should it fail, the unit will no longer go into deep sleep mode.

Logic: Keypad Operation

1) The keypad works as a matrix supported V2. The signals inform the Whitecap upon a key press by dropping the signal ‘low’. Below is the Key Matrix.

Function	**Key**	**KBR0**	**KBR1**	**KBR2**	**KBR3**	**KBR4**	**KBC0**	**KBC1**	**KBC2**	**KBC3**	**KBC4**
A	S509	0									0
B	S508	0								0	
C	S507	0							0		
D	S506	0						0			
E	S505	0					0				
F	S504	0				0					
G	S503	0			0						
H	S502	0		0							
I	S501	0	0								
J	S517		0								0
K	S516		0							0	
L	S515		0						0		
M	S514		0					0			
N	S513		0				0				
O	S512		0			0					
P	S511		0		0						
Q	S510		0	0							
R	S524			0							0
S	S523			0						0	
T	S522			0					0		
U	S521			0				0			
V	S520			0			0				
W	S519			0		0					
X	S518			0	0						
Y	S530				0						0
Z	S529				0					0	
,	S528				0				0		
.	S527				0			0			
?	S526				0		0				
Alt	S525				0	0					
;	S534					0					0
Shift	S533					0				0	
Fast access	S548					0			0		
Smart	S532					0		0			
Voice Notes	S531					0	0				
Left	S538						0				0
Right	S537						0			0	
Up	S536						0		0		
Down	S535						0	0			
Menu	S541							0			0
Space	S539							0		0	
OK / Enter	S540,S545							0	0		
Mail	S543								0		0
Cancel	S542								0	0	
Editor	S547									0	0

Logic: Display

1) The display is a 126 X 64 pixel graphics display and is connected to the PCB via a 27 Pin ZIF connector J902. It is made up of glass with polarizers, a display driver and transflector. It is connected to the PCB with a ribbon cable that uses the 'hot-bar' sealing process. The LCD is controlled by:

- **CS1** Chip Select which originates from **DP_EN_L**, Whitecap **Pin A11** to J902 **Pin 1**.
- **RES** which originates from **RESET**, Whitecap **Pin P2** to J902 **Pin 2**.
- **R/W** which originates from **R_W**, Whitecap **Pin B11** to J902 Pin 4.
- 8 Data Lines from Whitecap **DO – D7**
- The display is supported by **V2** and **–10V** (originating from U904 and can be measured on C965)
- Also the data / command signal **AO** from Whitecap **Pin B12**.

Logic: Vibrator

The Vibrator M1 is physically attached to the controller board PCB (Soldered). The vibrator is controlled by the signal **VIB_EN** Whitecap IC **Pin K1** and is supported by **B+** through U501.