MOTOROLA
Personal Communications Sector

GSM Service Support
Level 3 Authorized

# T190 / T191

GSM Service Support
Training - Documentation - Engineering


# Level 3
# Circuit Description
# 11 / 08 / 01
# V1.0



by Toko (toko@gsm-free.org)

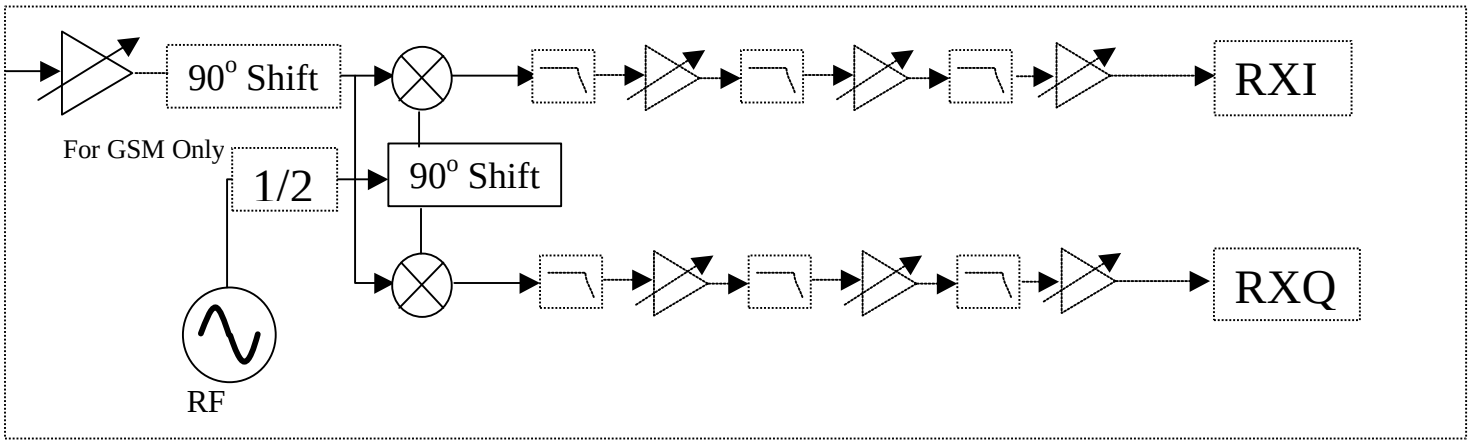
## RECEIVE

1. Received GSM 900 frequency enters the unit at the Antenna ANT1
2. L702 / L701 /C711 provide matching
3. The signal then enters mechanical Auxiliary RF port U72. When a load (50Ω is placed into the socket the RF will be diverted into or out of U72). This socket will be used for phasing, testing purposes.
4. From U72 **Pin 6** to RF Switch U75 **Pin 8** (**ANT**), where through control voltages the Rx path is isolated from the TX path. The following voltages control the RF Switch: **VC1 & VC2**, which are all 0V or 3.6V Low or High respectively.
   **For RX a diplexer is used to separate the GSM and DCS frequencies***
   The controlling input signals for U72 are originated from T/R Switch Controller U73, using the outputs on **Pins 6 & 4**:
   To provide the appropriate switching voltages the following signals are used.
   - **GSM_T/R** this signal puts the phone into GSM Mode when High (originates from Hercules Digital Processor U1 **Pin B10**)
   - **DCS_T/R**, this signal puts the phone into DCS Mode when High (originates from Hercules Digital Processor U1 **Pin E9**)
   - **V_BR**, is the support voltage, it originates from **VBAT** through U90. Voltage range is between 3.3V – 3.6V

   Below are the states of **VC1 & VC2** and the relative states of **DCS_T/R** and **GSM_T/R** for each scenario.

| | **VC1** | **VC2** | DCS_T/R | GSM_T/R |
|---|---|---|---|---|
| GSM RX | 0V | 0V | X | X |
| DCS RX | 0V | 0V | X | X |

5. The appropriate frequency is then fed from the diplexer of U75 from **Pin 10** for GSM and **Pin 1** for DCS
6. The received frequency is then fed into a Dual Band select SAW (Standing Acoustic Wave) filter U66 for GSM (Loss approximately 4dB), and U67 for DCS.
7. The outputs from the SAW filter is 2 balanced outputs that will be fed into the Transceiver IC – U61 on **Pins 4 & 5** for GSM and **Pins 9 & 10** for DCS



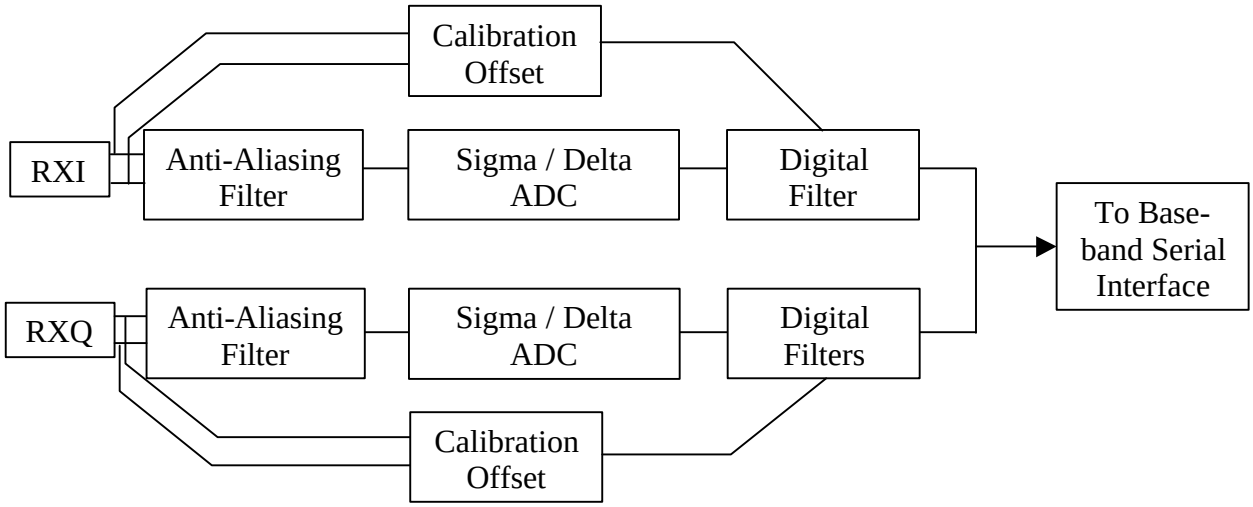

8. U61 is a Dual-Band Transceiver IC; it integrates a direct-conversion receiver vector modulator. (In basic terms Direct conversion allows us to take our incoming frequency and convert that frequency directly to Baseband without the need for expensive IF SAW filters or associated IF components.
9. The signal is firstly passed to an RF Low Noise Amp; this amplifier has 3 variable gain settings that will be programmed via SPI for AGC (Automatic Gain Control) purposes.
   From there the signal is passed in to a pair of Gilbert Cell Mixers, where the received frequency will be mixed with a generated RXVCO reference frequency.
10. The RX VCO frequency is generated by the RF Balun U64, which is fed by the RF Frequency Synthesiser IC, U63, The Charge pump to provide the correct conversion frequency is fed out of the Transceiver IC on **Pin 44**, and is operable between approximately 0.5V and 2.5V dependant on Frequency required. **V_RX** provides the switched supply for U64. This is generated from **V_BAT** through Dual regulator U90, the output on **Pin 1** as **V_SYN**, will then be switched via Q700-2 by **RX_ON_N** to provide **V_RX** at 2.85V
11. The RF signal will then be passed to U64 at 3.6 – 3.84Ghz where the signal will be split into 2 balanced outputs, **Pins 3 & 4**. These outputs will be fed into the Transceiver IC on **Pins 49 & 50** before being fed to the mixers. (The frequency will be divided by 2 for EGSM)
12. Now at Baseband frequencies, the signal will go through a 3-stage amplification process, which has a range of 90dB in 2 dB steps over the 3 amplifiers. The filtering of the Baseband signal is carried out by a first stage R/C Low-pass filter (The capacitor in this filter is external to the IC – C603 and C604).
    This is followed by 2-second stage Butterworth Filters. The IC contains DC offset circuits to remove any unwanted DC values and the signal is fed out as **RXI and RXQ** (Positive and Negative – Still Balanced) on **Pins25 – 28**. These will be passed through a High pass Filter R632

**13.** The Baseband In Phase and Quadrature signals arrive into the Omega IC, U3 on **Pins E7 – E10**, and into the Baseband Codec.

**14.** The Omega IC when combined with Hercules forms a fully integrated DSP. It forms the Base band interface for processing of Voice signals and Base Band signals. It also deals with Supply Voltage Regulation, SIM card, Battery Charging and ON/ Off functionality.

**15.** The Baseband Codec comprises of a Baseband Downlink path, which converts the Baseband Analogue I&Q signals into digital format, where they are filtered through digital FIR to isolate the desired information from the adjacent channels.

**16.** Within the Omega IC the path of the base-band RXI & Q data from the Transceiver IC takes the following route.



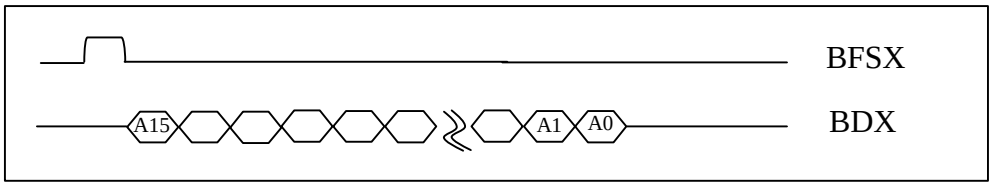

**17.** The RXI and Q signals from the Transceiver IC enter the Omega IC (**BDLIP / BDLIN / BDLQP / BDLQM**) and follow identical paths. The first stage is through a continuous-time second order anti-aliasing filter, which serves 2 functions: 1) to interface between RF logic and on-chip circuitry and 2) to prevent aliasing during the ADC process.

**18.** The signal is then fed into a Sigma – Delta ADC, and is fed out as a 3-bit word. This is then fed into a set of digital filters, that will decimate, (break the signal into piece parts), to give us an overall sampling rate of 270.8KHz (÷24). This allows a low enough frequency for adjacent channel rejection, and therefore channel separation.

**19.** Calibration of the IQ paths is achieved by internally shorting out the 2 input I paths, and then the same again on the 2 input Q paths the digital value measured will then be stored in a register. Once the **RXI** and **Q** paths are reconnected to the circuitry, again the calibration process takes place and the offset value is calculated.

**20.** The digital information is then sent to Hercules via the Baseband serial port on pins on **BDX** (Baseband Data Transmit) and **BFSR** (Baseband Frame Sync Transmit) **Pins G5 & F5** respectively, this information is clocked out at 270Khz.

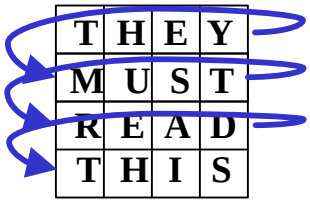
**21.** See below for timing diagram for Transmission of the data.




HERCROM200 (Hercules U1) is a chip implementing the digital Base Band processing of a GSM mobile product.
This chip combines a DSP M16L80 Mega-Module (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE) and an internal 2M bit RAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM.
The chip supports the GSM full-level test approval (FTA) for both Full-Rate, Half-Rate and Enhanced Full-Rate speech coding when using the appropriate GSM protocol stack S/W.
Hercules implements dedicated voice features (voice memo, voice recognition).

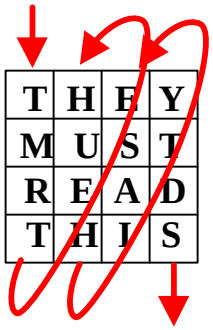
**22.** Within Hercules general GSM processing takes place, such as:

- **De-Interleaving**: Interleaving is a way in which the information that is to be transmitted is jumbled around before it is sent i.e.
  If we wish to send the information 'They must read this'




And we lose the information during the time that 'must' is being sent. Then we will lose a whole word.

- However if we jumble the bits around that make up the words, i.e. transmit in a different order.




If now during the same time frame we lose the same amount of information, and then we will only lose a small part of each word

- **Channel De-Multiplexing** – this is where we decode the signal that was transmitted; encryption at the transmitter ends is usually done by X-ORing the information.

- **Forward Error Correction Decoding** – This is where the redundant bits of data that were added in the transmitter are removed, and the information that is received can be processed. The redundant bits are added in various quantities dependent upon the signal quality. This means if some data is lost whilst travelling OTA then, for example, instead of 8 bits of speech data being lost, only 4 bits of speech and 4 bits of redundant data.

- **De-Segmentation and CRC Attachment analysis**. – During the transmission process the data is broken into packets of various lengths ($N^o$ of bits). These packets are then processed to give a checksum of what should be expected at the receiver. Once in the Hercules the information received is processed, and the two checksums compared. From the analysis, the correct algorithm for repairing any data corruption can be implemented.

**23.** The processed digital audio from the Hercules is then returned to the Omega IC on the Voice-band serial interface **VDR** (Hercules **H12** to Omega **K7**) clock, **VCLKRX** and Frame synchronisation signal, **VFSRX**.

**24.** The processed digital audio is received from the Hercules and fed into the Voice Band Codec of the Omega IC, from here the signal is interpolated within a speech-digital infinite duration impulse response filter (IIR) (i.e. that is, for the data coming in, the adjacent bits of the data being looked at are all synchronised and an average taken. From this a prediction of events can be calculated) also the sampling rate is increased, and the speech bandwidth is limited by high and Low pass responses.

**25.** The signal is then fed into a D/A converter and will be output to the appropriate analogue audio devices. Other functions performed by the Voice band Codec are:
- Programmable Gain for setting Audio Output Levels (Internally set)
- Volume Controls (Externally set gain)
- Side Tone production

**26.** The converted speech can then take 1 of 2 paths.

**27.** Path 1 to the Internal speaker LS1, the audio is fed out of the Omega on **Pins H8 & H9**, and fed directly to the speaker, voltage suppressers T3 and T4 are responsible for ESD protection. The speaker is situated in the front housing of the unit and is connected to the main PCB through an elastomeric contact.

**28.** Path 2 to the Headset Connector, the audio is fed out from the Omega IC on **Pin J9 AUXOP**, from here the audio will be passed to the Headset Socket J3.

**J3 is also used as a serial data entry port for Test / Flashing and Flexing, therefore data switches are required to correctly route the data**.

**29.** The analogue Audio is routed from Omega to an Analogue Switch U8, where a decision will be made to see if Audio or Data (**TXD0**) needs to be selected. This is done using the signal **I03DATA_HP_SEL**. This signal originates from Hercules **Pin M**5. This signal will be a Positive pulse for Data Cable download, that is active Low and will be active high for Earpiece.

For Data Cable  For Earpiece 

**30.** However to originate these control signals, the unit needs to know what is connected, i.e. either Headset or Data cable. This is achieved by using the **EARPHONE_IN** signal to detect the type of accessory. This will provide a voltage of between 2.8V – 2.6V for the Data Cable and 2.4V – 0V for the headset. The signal is fed to the ADC input of the Omega IC **Pin C6**. The signal **I013ACCIN** will detect when an accessory has been plugged into the headset socket and provide a wakeup signal.

**31.** Once the Processor knows what that an earpiece is connected, the Audio will be passed through U8, (supported by **VR2B_SW**, this is **VR2B** passed through a 0O Resistor). Then passed through a Noise Suppressor U9 and into the Headset Socket J3

## TRANSMIT

**32.** There are 2 sources of input audio:

**33.** Auxiliary Microphone is fed from the Headset Connector J3 on **Pin 4**, through Noise Suppressor U9 and into Analogue Switch U10, which will decide if the output will be for **RXD0** (Data Cable) or Analogue Audio. See **Points 30 & 31** for operation. The audio will then be routed to the Omega IC, **Pin H7** as **AUXI**

**34.** The Internal Microphone X2, uses the signal **MICBIAS** to provide correct microphone biasing conditions, the biasing support voltage being fed from the Omega IC, **Pin K9**. Voltage suppressers U14 provides ESD protection to the circuit. The signal is then passed as **MICIP** & **MICIN**

**35.** If both inputs are active then, output signal from the internal microphone will be used.

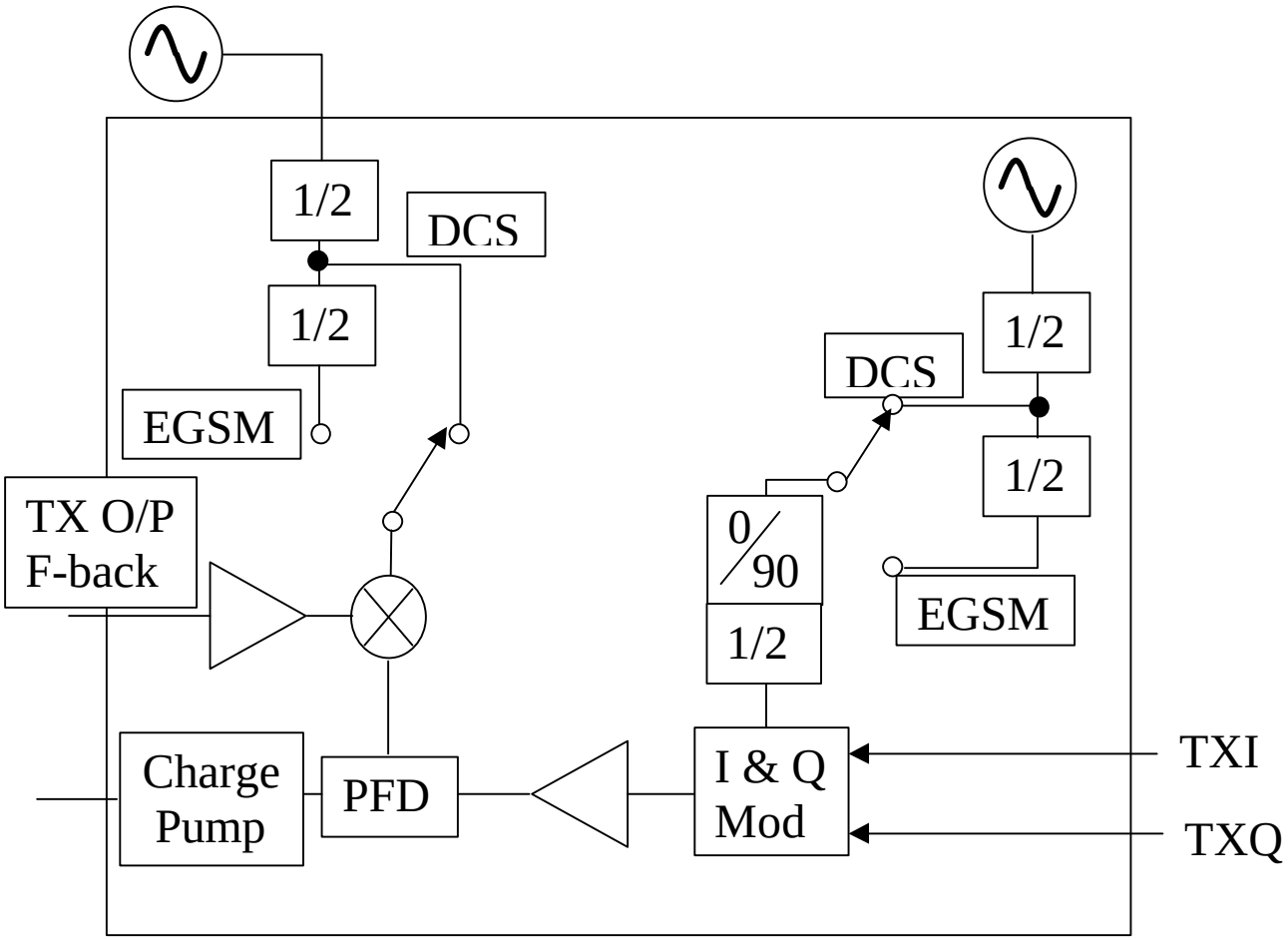
**36.** The input analogue audio is then routed to the Voice Band Codec of the Omega IC **Pins K8 & J8**. Within the Omega IC the analogue signal will be driven through a PGA (Programmable Gain Amplifier), and the information will be passed through an A/D converter.

**37.** Once again, as in **RECEIVE**, the loop between the Omega IC and the Hercules IC is put in place for standard data processing.

**38.** The transmitted signal is sent to the Hercules IC over the Voice-band **VDX** Line Omega **Pin G6** and is clocked by **VCLKRX Pin H6**. The signal is then received by the Hercules IC on **Pins H13 & G11** respectively. Synchronisation is achieved using the frame synch signal **VFSRX** (Omega **Pin G7** / Hercules **Pin H11**.

**39.** After processing, the Base-band signal information is transferred back to the Omega IC using the base-band lines, **BFSR / BDR /** (Omega **Pins J5, K5**and Hercules **Pins F12, F13** respectively)

**40.** Within the Omega IC, the received information will now be passed to the Base Band Codec, where the signals from the DSP will be modulated in accordance with GSM Specifications and will output the analogue **TXI** and **TXQ** signals to the Transceiver IC (Omega **Pins C9 / C10 / D8 / D9**) then through a low pass filter R624/ C621 / C622, entering U61 on **Pins 19 - 22**



**41.** The Transceiver IC U61 generates a modulated signal using a Quadrature Modulator and then converts to the final frequency using an OPLL (Offset Phase Locked Loop.

**42.** OPLL is basically a normal PLL, however it incorporates a down converter mixer, which has the advantage of having a different comparison frequency to that of the transmitted frequency and therefore broadband noise created in the modulator will be outside the spectrum.

**43.** Once generated the modulated word will be superimposed upon the TX IF frequency created by the internal synthesiser. This runs at between 376Mhz and 384Mhz. The signal will then be divided down (by 4 for DCS and 8 for EGSM). This generates signals at 90Mhz for DCS and 45Mhz for EGSM

**44.** The phase-modulated carrier is now forwarded through an amplifier and into the OPLL, the OPLL consists of a Gilbert Cell Down Converter, phase detector, off chip passive loop filter and VCO.

**45.** Within the OPLL, the Feedback from the TX VCO will be fed back into Omega on **Pin 14** and will be mixed (Down Converted) with the RF VCO, which will be divided down by 2 for DCS and 4 for EGSM. This will then be phase compared with the modulated signal to give a difference error signal that when fed into the Charge Pump will create an error voltage that will drive the TX VCO to the correct frequency.

Worked Example.

- Internal TX IF VCO for EGSM = 360Mhz
- Divide / 8 = 45Mhz
- TX Feedback for EGSM = 880.2Mhz
- RF VCO for EGSM = 3700.8Mhz
- Divide / 4 = 925.2
- **RF VCO – TX F/Back = 925.2 – 880.2 = 45Mhz**

**46.** The analogue VCO drive information, is now sent from OMEGA **Pins** 17 to the Passive Loop Filter, consisting of C614 / C615 / C617 & R619 / R621. The charge pump voltage is approximately 0.5V – 2.5V.

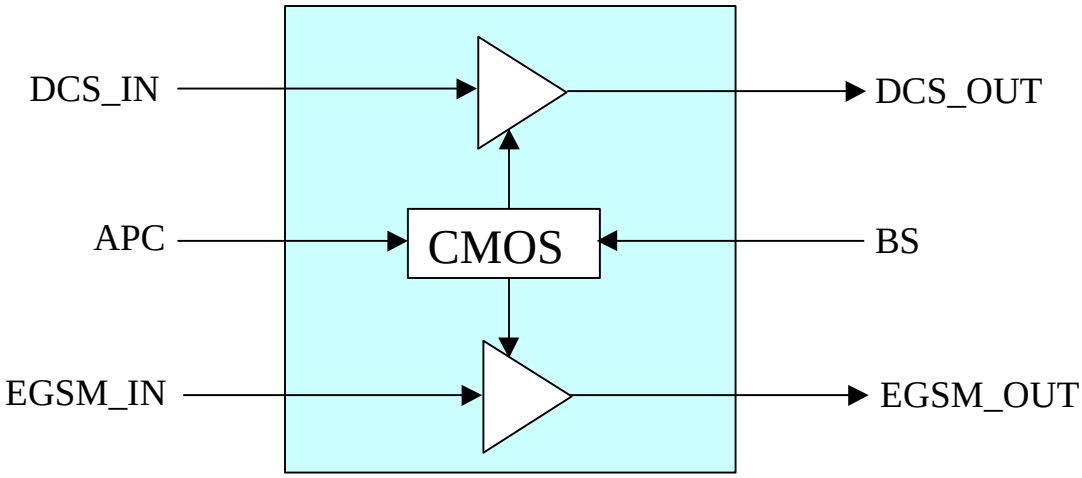
**47.** The charge pump voltage enters the TX VCO on **Pins 10** for GSM and **Pin 6** for DCS. U65 is supported by 2.85V V_TX which is generated by Q700 – 1 (Combination of **V_BR** (U90) and **TX_ON_N**. (**VBAT** switched through U86 by **TX_ON**)

**48.** The control signals **BS1** and **BS2** are used to provide the band switching controls, and are originated from Hercules **Pins B13** & **D11** respectively

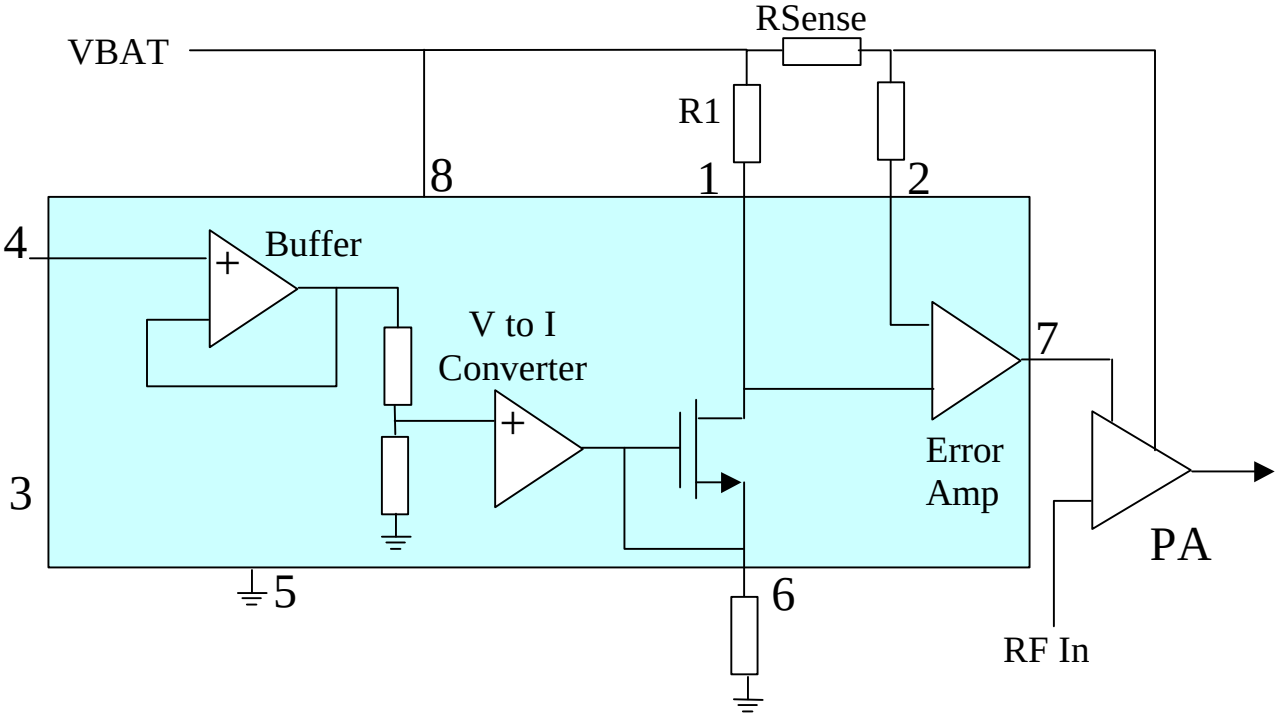
**49.** The appropriate Transmit frequency will now be generated according to channel selection and Band, with the EGSM outputting from U65 **Pin 1** and DCS from **Pin 5**.

**50.** At the output of the TX VCO is a 30dB attenuator to take a sample of the transmitted frequency for use in the Transceiver IC within the OPLL.

**51.** The transmit frequency signal is then pushed to the PA U71 for amplification. U71 is a Dual Band Power Amplifier containing 2 Bipolar Transistor blocks for each band.




**52.** The inputted frequency in inputted into the Transistor stage amplifiers with the signal BS1 controlling the band select. The signal APC (Analogue Power Control) fed in on Pin 6 & 8 (VCC) will allow more or less amplification by providing more or less current to the IC.



**53.** APC is provide by Power Control IC U74
The PAC IC uses a closed Loop bias control voltage system to control the output power of the PA. In normal operation the current driving the PA from **VBAT** will flow through the current sense resistor. When stable the voltage drop across R1 should be = to that across the current sense resistor. The larger the voltage drop over R1, the greater the current delivered to the PA.
When the transmitter needs to deliver more power, the signal **RAMP** from Omega **Pin F9** goes higher. This is fed directly to the U74 **Pin 4** and into the buffer amp; within here the signal is divided by 4 in a ratio of 3:1. The scaled down voltage is now fed to the V to I converter. This switches on the FET allowing a current flow between Pins 1 and Pins 6, therefore setting the R1 Voltage level, and as mentioned previously, the Error Amplifier will output a voltage signal to the PA to drive harder, until R1 and I Sense PD's are the same.
The signal **PC**, from Omega **Pin B12,** acts as an enable.
**VBAT** is switched by **TX_ON** through U86, as a safety feature to remove **VBAT** during receive to ensure no transmission

**54.** The **RAMP** signal is controlled via SPI programming, however a Thermister, TR1 connected to Omega **Pin D6** which is supported by **VR3** feeds temperature information back to the Omega IC, which in turn back down the PA via the **RAMP** signal if the unit is getting too hot.

**55.** Once the transmit power is achieved, the **PA** will transmit in accordance with the GSM Burst specifications. The burst will then be fed through the T/R switch U75, through the mechanical switch U72 and out of the Antenna, ANT 1

**Power up Sequence**

**56.** There are 3 methods by which the product can be switched on, these are:

- On button depressed – On pressing the Power Key (S19) for + 2 seconds, this signal will then be sent to Omega **Pin B10**
- Software wake up – If the user has programmed his unit to wake up at a certain time and Power on, the signal **RTCINT**, will be originated from Hercules **Pin B6** and will be sent to Omega **Pin D7**
- Charger is plugged in – When the charger is plugged in at the Power Jack J1, Power will be sourced from **Pin 1**, through Fuse F1, through U17, and output to Omega **Pin E4**, at a time when **VCHG** > than **VBAT**, Omega **Pin E5**, constitutes the conditions for Power on.

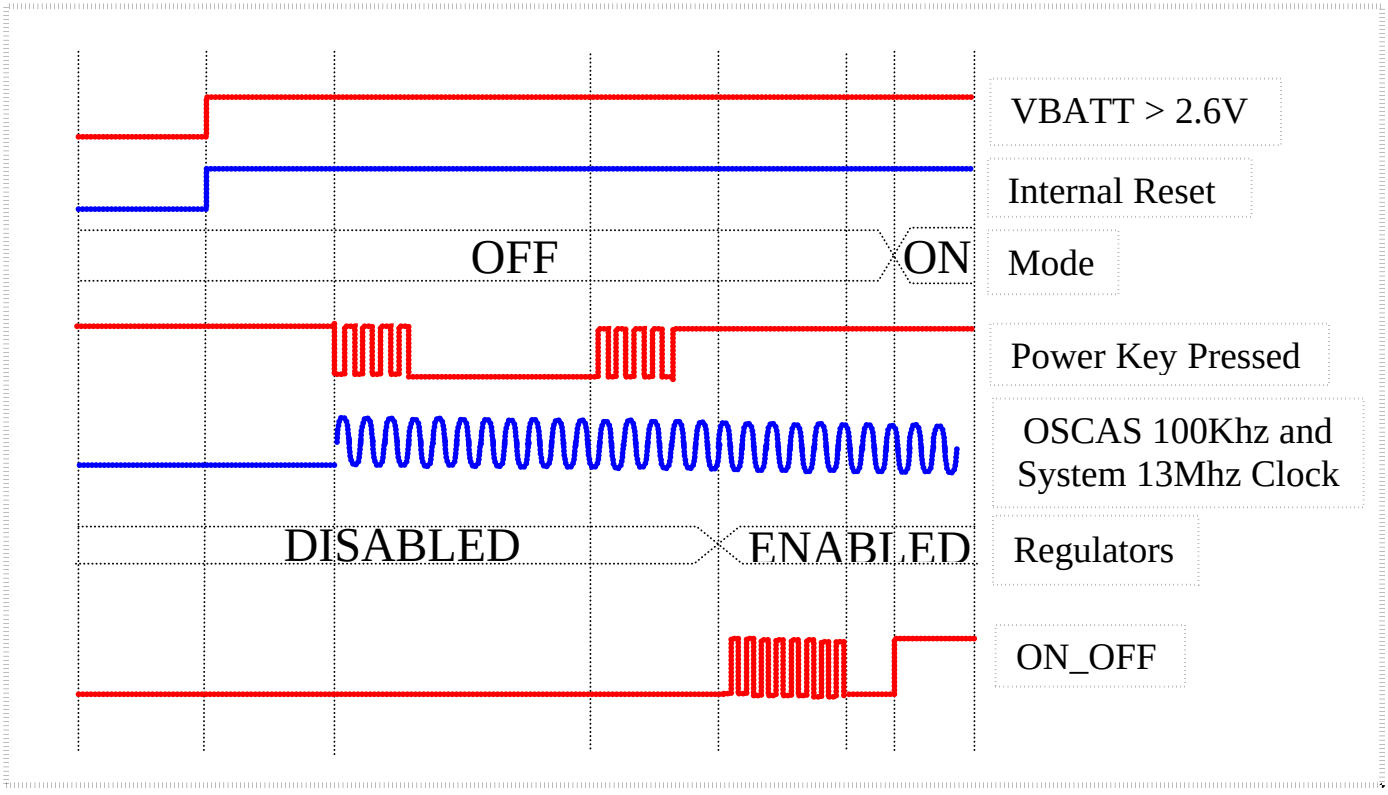
**57.** Once one of the scenarios has taken place, the unit will then begin to power up, the Power up sequence is as follows: (For On/off key pressed)

- Battery power made available from Battery Connector JP1 as **VBAT**, and also a signal is sent to Omega **Pin F1**, as **VBATBB**.

- Power Key, S19 is depressed, which creates an interrupt within the Omega.
- **NRESET** is pulled low, Omega **Pin F6**
- **VREF** and **IBIAS**, set up a reference voltage Band-gap within Omega, using the capacitor and resistor C24 and R23 **Pins F4 and G1** respectively
- This will start the internal 100Khz Internal Clock.
- Regulators now begin to output necessary Voltages, these are:
  - **VR1** – Pin H1 – 1.8V @ 120mA – Supplies Hercules and RTC Battery.
  - **VR2** – Pin E1 – 2.85V @ 120mA – Supplies Hercules 13Mhz Clock Output and Flash and Ext RAM
  - **VR2B** – Pin D1 – 2.85V @ 50mA - Support Omega / Hercules communication and also 3V peripheral devices
  - **VR1B** – Pin C1 – 2.0V @ 50mA – Supplies Omega Internal circuits
  - **VR3** – Pin H10 – 2.85V @ 80mA – Supplies Analogue Voltages

**58.** Once all the necessary voltage have been produced, Hercules will supply the signal **TCXOEN** along with Omega originated **VR3**, this will be fed into RF side U84 and will be used in conjunction with U85 to create the 26Mhz Clock, which is fed into the Transceiver IC **Pin 40**. This is then used as internal system clock within the Transceiver IC, but will also be divided by 2 to create the 13Mhz system clock, Omega Pin 37, Into Hercules **G14**, out on **Pin L14** to Omega **Pin A4.**

**59.** Once all the Power supplies and clock are running, the signal **ON_OFF** from Omega is output to Hercules **Pins D10 / D6**



**Memory**

**60.** The memory consists of a 32Mbit Flash part U5, and a 1Mbit SRAM U6; both are supported by **VR2**. The chip select for the Flash is provided by the signal **NROMCS1** from Hercules **Pin P6** and from **P7** for the SRAM

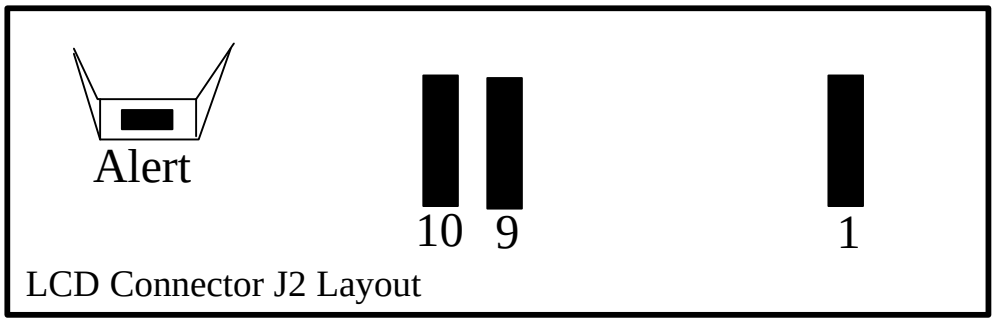
**61.** Contrast control is achieved by the variation in voltages, which are stored in C40 through C44 and DC / DC LCD driving voltages provided by C45 through C48.

**62.** Data to and from the LCD is though the data bus **D0 – D7**, U24 **Pins 16 – 24**

**63.** Chip select is sent from Hercules **Pin 48** to LCD Connector **Pin 28**, with the **Reset** on connector on **Pin 27**.

**LCD**

**64.** The LCD Connector J2 is a 98 X 64 Graphic, Black and White COG (Chip on Glass) type. It uses Serial Data input instead of Parallel data input as Topaz. The LCD Module is supported, with the voltages **VR2** on **Pins 8 & 7**, with 8V being provided by C34. The LCD uses the reset signal from Hercules, **Pin K11**. The data to the display is provided by the SPI bus **I2C_SDA** (data) and **I2C_SCL** (Clock). These are originated from Hercules **Pins C4 and F4** respectively; these are both supported by **VR2B**.



LCD Connector J2 Layout

**Vibrator and Alert**

**65.** The vibrator is driven by the signal **IO0VIBRATOR** which originates from Hercules **Pin J1**, this signal is applied to the base of Transistor BQ4, this then gives the vibrator support voltage **VBAT** a path to earth through Vibrator Motor M1. D14 allows a discharge path for remnant energy after the vibrator has switched off

**66.** The buzzer / alert is operated, using the signal **BU** from Hercules **Pin C2**, this signal can be programmed to variable frequencies. It forces BQ3 to conduct creating the current path for the Buzzer U13 support voltage **VBAT** to earth.

## Keypad and Back lights

**67.** The backlights are split into 2 for the LCD (D4 / D3 / D13) and the keypad backlights of which there are 8 (D5 – D12). The backlights are switched on using the signal **BL** This is generated from Hercules **Pin B1**. When **BL** goes high**,** U7 **Pin 6** goes low, which in turn, forces BQ2 to conduct. This allows **VBATBB** to supply the backlights. Approximately 1.9V will be made available for each set of LED's with approximately 36mA being drawn through R40 and 60mA being drawn through R35

**68.** The keypad is made up of a 4 column x 4 Row matrix, with the signals **KBR3 – KBR0** being generated from Hercules **Pins B2 / D4 / B4 / A4** respectively. The column signals, **KBC4 – KBC1** Hercules **Pin E5 / D5 / B5** / **A5**. Each key has its own unique combination of Column and Row

**69.** The keypad matrix is as follows

| Function | **Key** | **COL 0** | **COL 1** | **COL 2** | **COL 3** | **COL 4** | **ROW 0** | **ROW 1** | **ROW 2** | **ROW 3** |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |
| **1** | S3 | X | | | | | | | X | |
| **2** | S2 | X | | | | | | X | | |
| **3** | S1 | X | | | | | X | | | |
| **4** | S7 | | X | | | | | | X | |
| **5** | S6 | | X | | | | | X | | |
| **6** | S5 | | X | | | | X | | | |
| **7** | S10 | | | X | | | | | X | |
| **8** | S9 | | | X | | | | X | | |
| **9** | S12 | | | X | | | X | | | |
| **0** | S13 | | | | X | | | X | | |
| **Down** | S4 | X | | | | | | | | X |
| **SEL** | S8 | | X | | | | | | | X |
| **Up** | S11 | | | X | | | | | | X |
| **#** | S16 | | | | X | | X | | | |
| ***** | S15 | | | | X | | | | X | |
| **Menu** | S15 | | | | X | | | | | X |
| **Send** | S17 | | | | | X | | | X | |
| **Quit** | S18 | | | | | X | | | | X |

## Charger Function

**70.** There are 3 modes of operation for the T191 charge these are:

- Normal charge

- Trigger of Full rate Charge
- Over Voltage Protection

**71. Normal Charge** – During normal operation, once the charger has been plugged into the Power Jack J1, power will be distributed from **Pin 1** and will be passed through Fuse F1.
The signal **ACCID** is not used, instead a resistor is placed on the **ACCID** line to make a potential divider with R75 and this will be used for the Product 'ID' to establish if the unit is from EMEA or ASIA.
Once through the fuse the charging voltage will be fed into **Source 1** of U17, the left side of this dual FET is biased on by the Over Voltage FET U16. The voltage is then fed through to the **Drain**. It will then be fed back into **Source 2** of U17 before being fed out as **VBAT** and **VBATBB**.
During this time the right side of U17 is biased on by the signal **ICTL**, from Omega **Pin E3**, this signal controls the charging profile.

**72. Trigger or Full Rate Charge** – When the battery is completely flat, a quick charge at full current is required, to do this we initially have U18 right side grounded, i.e ON.(this has the effect of fully opening the charge 'gate' of U17)
The right side of U18 is initially 'OFF' as the charging current begins to flow, a biasing voltage will be formed at G2 of U18 ensuring it stays on, at the same time C48 will begin to charge. After 2 seconds, the potential on C47 will be sufficient to switch on U18 left side, this will put a ground onto the **Gate** of U18 Right side, which will turn this side off, thus allowing the controlling signal **ICTL** to take control of the charging current.

**73. Over Voltage Mode** – The Over Voltage Mode is set at a threshold of 7.8V, if the voltage on the Charge input line should exceed this then the voltage between R62 & R65 will go above 0.73V and will switch the left side of OVIC U16 'ON' the will provide a path to Earth, grounding the inputted Charger Voltage.

**SIM Circuit**

**74.** Both 3 and 5V SIM cards are supported by the Omega. The 5V is achieved by using a charge pump circuit, consisting of C5 and C6, along with the 2.85V **SVDD** (Omega **Pin A2**). This will be fed onto the SIM Block U2 on **Pins 4 and 5**.

**75.** Other signals are:

- **Reset**, Omega **Pin D5**, U2 **Pin 3**
- **Clock**, Omega **Pin B4**, U2 **Pin 1**
- **I/O** (data to and from the SIM Card) Omega **Pin D4**, U2 **Pin 2**, again this can be transposed from 3V to 5V if necessary)