L2/L6 Block Diagram Signal Description

	Signal	From	To	Description
1	AG_REG	Q901	U50, U150	2,775V supply Voltage for U50, U150
2	ALERT-	U900	J1403	ALERT Out Negatve (-) from Alert amplifier to Alert speaker
3	ALERT+	U900	J1403	ALERT Out Positive (+)from Alert amplifier to Alert speaker
4	ANT_DETB	M3	U800	Antenna Detect low active indication for an extern connected antenna
5	AOC_DRIVE	U800	U50	Bias control signal to U300 TX amplifier (Automatic Output Control Driver)
6	AUD_REG	U900	U900	AUDio 2,775V support voltage for U900 internal functions
7	AUL_CS	U800	U900	BaseBand SPI Bus Chip Select from U800 to Atlas (Neptune /Atlas Control Communication)
8	AUL_INT	U900	U800	INTerupt to indicate the end of conversation on Communication Bus
9	B+	U900	U900, U50	Main Source for the Phone supporting U900 power supply, PA power support
10	BATT+	M1	R911, U900	BATTery (+) output/input to Battery switch Q904 and U900 AD converter input
11	BATTFET	U900	Q904	Enables / Disables Battery BATT+ Switch to support B+ as Main source for the device with Battery power
12	BATTISNS	R910	U900	Negative AD converter input to Atlas to mesure the votage drop over R910 as Current flow indicator of charge mode
13	BB_I	U150	U800	positive In phase baseband signal from receiver in Algae to A/D converter in Netune
14	BB_IX	U150	U800	negative In phase baseband signal from receiver in Algae to A/D converter in Netune
15	BB_Q	U150	U800	positive Quadratur-phase signal from receiver in Algae to A/D converter in Netune
16	BB_QX	U150	U800	negative Quadratur-phase signal from receiver in Algae to A/D converter in Netune
17	BB_SAP_CLK	U800	U300, U900	Base Band Serial Audio Port CLocK to Clock Audio Data Flow (Audio SPI Bus)
18	BB_SAP_FS	U800	U300, U900	Base Band Serial Audio Port Frame Synchronisation to syncronize the Audio Frames (Audio SPI Bus)
19	BB_SAP_RX	U300, U900	U800	Base Band Serial Audio Port Receive signal to U800 (Audio SPI Bus)
20	BB_SAP_TX	U800	U300, U900	Base Band Serial Audio Port Transmitt signal to U900 and U301 (Audio SPI Bus)
21	BB_SPI_CLK	U800	U900, U1301	BaseBand SPI Bus CLocK to Clock Data Flow (Neptune /PCAP Control Communication)
22	BB_SPI_MISO	U900, U1301	U800	BaseBand SPI Bus Master (U800) Input, Slave (U900) Output (Neptune /PCAP Control Communication)
23	BB_SPI_MOSI	U800	U900, U1301	BaseBand SPI Bus Master (U800) Output, Slave (U900) Input (Neptune /PCAP Control Communication)
24	BLUE_CLK_ENB	U900	U300	Orginal CLK_32KHz from Pcap as Enable indication to the Bluetooth Chip
25	BLUE_HOST_WAKEB	U300	U800	Communication WAKEup signal from U301 to U800
26	BLUE_WAKEB	U800	U300	Communication WAKEup signal from U800 to U301
27	BPFET	U900	Q903	OverVoltage control interface output to Enable / Disable BATT+ Switch to support B+ as Main source for the device with external power
28	BT_REG	U900	U300	1,8 Volt regulator output from Atlas to support the BT Chipset U300
29	BURSTCLK	U800	U700	BURST CLocK to clock U700 to syncronize the loading of addresses and delivery of burst read data
30	CAM_CAMCLK	U1301	J1401	CAMera CLlocK, operation clock for camera circuit
31	CAM_D0 - D9	J1401	U1301	CAMera Data Bus to Graphic Processor
32	CAM_HSYNC	J1401	U1301	CAMera Horizontal SYNChronization
33	CAM_PCLK	J1401	U1301	CAMera Period ClocK
34	CAM_PWRDWN	J1401	U1301	CAMera Mos Circuit Power down
35	CAM_REG	U900	J1401	2,775V supply Voltage for Camera module
36	CAM_RESET	U1301	J1401	CAMera RESET

37	**CAM_SDA**	J1401	U1301	**CAM**era **S**erial **D**ata cimmunication to Camera circuit
38	**CAM_SLC**	U1301	J1401	**CAM**era **S**erial **C**lock, clock for serial data communication
39	**CAM_VSYNC**	J1401	U1301	**CAM**era **V**ertical **SYNC**hronization
40	**CHRGCTRL**	U900	Q905,Q906	Analog Tuning Voltage to drive /control the current flow of the Charge Transistor's Q905/Q906 into the Battery
41	**CHRGISNSP**	R910	U900	Positive AD converter input to Atlas to mesure the votage drop over R910 as Current flow indicator of charge mode
42	**CHRGRAW**	J2003	U900	Voltage sense from External Power VBUS
43	**CLK_32KHZ**	U900	U800, U1301	**32KHZ CL**oc**K** output to RTC timer interface in Neptune and J1300
44	**CLK_32KHZ_2_7V**	U900	U1301	**32Khz CL**oc**K** 2,7V to support the Graphic Processor with system Clock
45	**CLK_13MHZ**	U800	U900	**13 MHz** Core **CL**oc**K** to PCap
46	**CM_IN**	U150	U800	Decoupled Ground Connection for RX BaseBand signals
47	**CS0B**	U800	U700	**C**hip **S**elect **0** - active low output is used as external Flash Memory chip select
48	**CS1B**	U800	U700	**C**hip **S**elect **1** - active low output is used as external Flash Memory chip select
49	**CTS2**	U800	U300	**C**lear **T**o **S**end Data indication from U800 To U301 (InterChip Communication)
50	**D-**	U900/ J2003	J2003/ U900	USB **D**ata**-** line in/output passing the RV923 ESD protection Fliter, EMU mode: Audio out left or Microphone in
51	**D+**	U900/ J2003	J2003/ U900	USB **D**ata**+** line in/output passing the RV922 ESD protection Fliter, EMU mode: Audio out right
52	**DISP_LED1 - LED3**	J1403	U900	**DISP**lay backlight **LED** driver input, backlight enabled by short to ground
53	**EB0_B**	U800	U700	Used as write **E**nable to partition of SRAM
54	**EB1_B**	U800	U700	Used as write **E**nable to partition of SRAM
55	**ECBB**	U800	U700	**E**nd **O**ff **C**urret **B**urst-active low(**B**)- to indicate to FLASH the end of current burst sequence.
56	**EURO_US**	U800	U50	Band Selection Signal from Neptune to RX/TX Switch in Eagle IC U50
57	**EXC_EN**	U800	U50, U150	**EXC**iter **EN**able active high to drive the Switch Control Circuit to TX mode and TX indication to Eagle IC
58	**EXTAL**	Y805	U800	26MHz reference clock differential input
59	**GA_INT**	U800	U1301	**INT**erupt to indicate the end of conversation on Communication Bus
60	**GA_SPI_CS**	U800	U1301	**G**raphic **A**ccelerator **SPI C**hip **S**elect Orginal **BB_SPI_CS6**
61	**GND**	PCB	PCB	**GrouND** connection
62	**GRAPH_REG**	U900	U1301	**1,275V** Supply Voltage for **GRAPH**ic Procesor
63	**HAND_SPKR-**	U900	P1000	Audio amplifier output (-) to Flip connector to support the Earpeace **SP**ea**K**e**R** through FL1200
64	**HAND_SPKR+**	U900	P1000	Audio amplifier output (+) to Flip connector to support the Earpeace **SP**ea**K**e**R** through FL1200
65	**IO_REG**	U900	U800,,U1301	2,775 Volt supply for different sources like Neptune, Graphic processor ...
66	**KBC0-1**	U800	Keypad	**K**eypad (**B**oard) **C**olum Strobe
67	**KBR0-7**	U800	Keypad	**K**eypad (**B**oard) **R**ow Sense
68	**LBAB**	U800	U700	**L**oad **B**urst **A**ddress active low- causing that U701 is loading a new starting burst address
69	**LCD_CLK_DATA(6)**	U800	U1301	Serial **CL**oc**K** output to **LCD** driver to clock the **DATA** Bus. The **(6)** stands for Data Line 6.
70	**LCD_CS**	U800	U1301	**C**hip **S**elect for LCD driver
71	**LCD_DATA (0-5)**	U800	U1301	LCD DATA Bus Lines from Neptune Display Interface to Display Driver
72	**LCD_RS**	U800	U1301	**R**egister **S**elect indicates if display data or control datas are written
73	**LCD_SDATA_DATA(7)**	U800	U1301	**S**erial **DATA** output from Neptune Display SPI interface. The (**7**) stands for Data Line 7.
74	**LCDC_CS**	U1301	J887	**C**hip **S**elect for LCD
75	**LCDC_DATA (0-7)**	U1301	J887	**LCD DATA** Bus Lines from Graphic Processor Display Interface to Display
76	**LCDC_Reset**	U1301	J887	**LCD** Reset
77	**LCDC_RS**	U1301	J887	**R**egister **S**elect indicates if display data or control datas are written

78	**LEDKP**	J1403	U900	**K**ey**P**ad **LED** diver input, backlight enabled by short to ground
79	**LOBATTI**	U900	U800	Low Battery Voltage indication from Atlas control circuit
80	**LOWB_HIGH**	U800	U50	**LOW /HIGH** Band selection signal from U800. Active low in Low Band modus.
81	**LT_SNS_CTL**	U800	U1000	**L**igh**T** **S**e**NS**or enable/supply from Neptune to DS805
82	**MIC_BIAS1**	U900	Mic Audio Line	**BIAS** Voltage output to support the **INT**ernal **MIC** Audio line
83	**MIC_INM**	J1403	U900	analog **INT**ernal **MIC**rophone signal as input to microphone amplifier
84	**OEB**	U800	U700	**O**utput **E**nable-active low (**B**)- is indicating that the bus access is a read and enables slave devicesto drive the bus with read data.
85	**ON1B**	J1403	U900	if pulled to GND (powerkey) indicates the On /OFF logic in U900 to power on or off the unit
86	**OWB**	M1	U800	**O**ne **W**ire **B**us signal line from Battery EEProm to Neptune. Used to download Battery Recharge information to Neptune
87	**PA_DET**	U50	U800	Antenna power detect feedback from Eagle power amplifier, refers to output power level typically 50mV without transmitter power
88	**PA_REF**	U50	U800	Reference feedback from Eagle power amplifier, typically 60 mV and does not vary with transmitter power level
89	**PC13**	S1401	U800	additional Keyboard signal from PTT / Camera switch
90	**PE14**	U800	U1301	Reset from Neptune for Graphic Processor
91	**R_WB**	U800	U700	**R**ead **W**rite, active low in Write. Indicates the bus acces type.
92	**REF_REG**	U900	U900	**REF**erence **REG**ulator Supply only for internal Pcap use 1,575V
93	**RESET_OUT**	U800	U700	**RESET** from Neptune for U700
94	**RESETB**	U900	U800.U300	active low **RESET** for U800 and U300
95	**RF_5V_REG**	U900	U800	**5V** support Voltage **REG**ulator from U900 to support the RX/TX Charge Pumps, supported by VBOOST
96	**RF_CLK**	U800	U150	SPI **CL**oc**K** output to U150 (**RF** Interface)
97	**RF_CS**	U800	U150	SPI **C**hip **S**elect output to U150 (**RF** Interface)
98	**RF_DATA**	U800	U150	SPI Serial **DATA** to U150 (**RF** Interface)
99	**RF_REG**	U900	U800	2,775 Supply for Synthesyzer, super filter **REG**ulators , **RF** and analog functions
100	**RF_REG**	U900	U800	2,775V supply **V**oltage for RF circuits of Neptune IC
101	**RTC_BATT**	J1400/U900	U900/J1400	RTC Backup Battery + Supply to RTC Timer Interface interface. RTC Battery will be recharged
102	**RTS2**	U300	U800	**R**equest **T**o **S**end Indication from U301 to U800
103	**RX_CP**	U800	U150	Bias/ tuning voltage from the **RX C**harge **P**ump to the RX VCO in Algae
104	**RX_EN**	U800	U150	RX Enable signal for the Algae Frontend and VCO
105	**RXD2**	U300	U800	**R**eceive Data Communication from U301 to U800 (InterChip Communication)
106	**SIM_CLK**	U800	J1000	output **CL**oc**K** from Sim Card Interface to SIM Card
107	**SIM_DIO**	U800/J1403	J1403/U800	**D**ata **I**n and **O**utput from and to SIM Card / Interface
108	**SIM_PD**	U900	U800	**S**IM **P**resence **D**etect signals the insertion or removel of Phone Battrey to Neptune organated by **BATT_DETB** output from PCAP
109	**SIM_REG**	U900	U800/ J1403	**SIM** Card support voltage **V**CC 1.8 or 3V from Atlas
110	**SIM_RST**	U900	J1403	active low **R**e**S**e**T** signal from SIM interface

111	**STANDBY**	U800	U900	Deep Sleep Signal from Neptune to Pcap to indicate Low Power State
112	**SYNTH_FD_N**	U150	U800	downconverted negative differential RX/TX VCO **F**ee**D**back to Neptune **SYNTH**esizer
113	**SYNTH_FD_P**	U150	U800	downconverted positive differential RX/TX VCO **F**ee**D**back to Neptune **SYNTH**esizer
114	**THERM**	M1	U900	Analog Referece voltage Biased by THERM_BIAS to Indicate the Battery Temperature to Pcap Charger Interface.
115	**THERMBIAS**	U900	M1	Analog Bias Votage to Thermistor line from Battery
116	**TRK_CLK**	U800	U150	**TR**ac**K**ing **CL**oc**K** signal from Neptune to Algae to calibrate the internal digital filters
117	**TX_CP**	U800	U150	Filtered **C**harge **P**ump output from PLL phase detect to bias the **TX** VCO
118	**TX_EN**	U800	U50	**TX EN**able is enabling the TX signal path in U50
119	**TX_MOD**	U800	TX_C P- TXVCO	High Pass filter output contains the GSMK Modulation package to modulate the TX VCO via TX_CP Line
120	**TX_OUT_HB**	U150	U50	**TX H**igh frequency **B**and **OUT**put to PA in U50
121	**TX_OUT_LB**	U150	U50	**TX L**ow frequency **B**and **OUT**put to PA in U50
122	**TXD2**	U800	U301	**T**ransmitt Data Communication from U800 To U301(InterChip Communication)
123	**UID**	J2003	U900	**U**SB **ID** line used as accessory detection
124	**USB_TXENB**	U800	U900	**USB T**ransmitt **Enable**- active low- signals to USB device when to transmit dataon USB bus.
125	**USB_VMIN_RXD**	U900	U800	**USB- (MIN**us) data from U900 to U800
126	**USB_VMIN_RXD**	U900	U800	RS232 **R**eceive data from U900 to U800
127	**USB_VMOUT**	U800	U600	**USB**- (**MIN**us) data from U800 to U600
128	**USB_VPIN**	U900	U800	**USB+ (P**ositive) data from U900 to U800 for internal Pcap Neptune Communication
129	**USB_VPOUT_TXD**	U800	U900	**USB+ (P**ositive) data from U800 to U900
130	**USB_VPOUT_TXD**	U800	U600	RS232 **T**ransmitt data from U800 to U900
131	**USB_XRXD_RTS**	U900	U800	CMOS logic value of value received from USB wires
132	**USB_XRXD_RTS**	U800	U900	**R**equest **T**o **S**end signal for RS232 communication between U800 and U900
133	**V_BUCK**	U900	U800, U700	Supply for Neptune (U800) core and logic and U700(FLASH)
134	**VBOOST**	U900	U800, J1403	5,6 Volt regulator output of Atlas to support Atlas internal USB Interface and V10 Regulator for U800 Charge Pumps. Supply for Backlight LED´s
135	**VIB_REG**	U900	PCB contacts	**VIB**rator **REG**ulator OUTput to vibrator motor contacts
136	**VM_REG**	U900	U800	2,775V supply **V**oltage for Neptune IC
137	**VSIM_EN**	U800	U900	**EN**able signal from Neptune to Seaweed for the **SIM V**CC regulator
138	**WDOG**	U800	U900	**W**atch**DOG-** active low signal to U900 to indicate power down of the unit
139	**XTAL**	Y805	U800	26MHz reference clock differential input