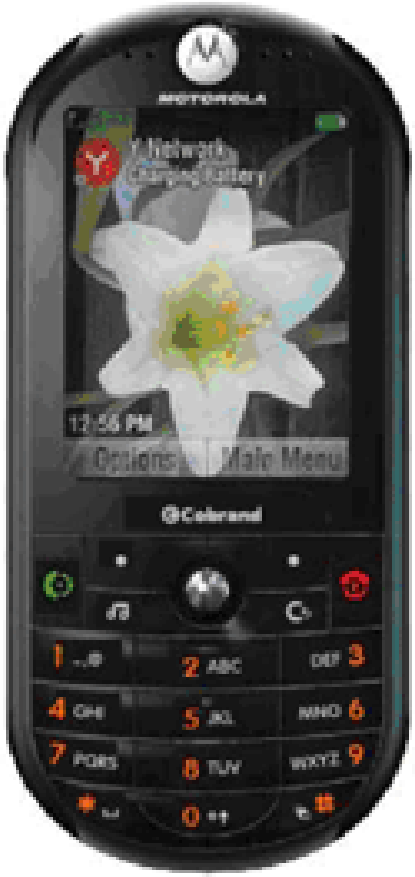
E2 Quad-Band GPRS / EDGE Smart Phone

LEVEL 3 CIRCUIT DESCRIPTION



Service Engineering & Optimization

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1 Revision History

Revision	Date	Section	Author
1.0	22th Dec 2005	STD	STD

2 Introduction and Purpose

The purpose of this document is to list and define the hardware system interfaces for E2 cellular phone. This phone is based out of EZX platform which consisting Neptune-LTE2 IC (base band call processor), Bulverde IC (adjunct application processor), PCAP2 (Platform Audio Interface and Power Control) IC, EMU Bus One-Chip IC, as well as the RFMD chips such as RF6025 IC and RF3178 power amplifier IC.

In this document, the major chipset features and functionality will be introduced as well as the dedicated usage in E2 phone design. The interconnections between Neptune-LTE2 and Bulverde will be introduced in detail. The control signals from Neptune-LTE2 to RF6025 and RF3178 will also be introduced.

3 PCAP2 Hardware Overview

This section describes the general features of the PCAP2 (Platform Control/Audio/Power) IC. The PCAP2 architecture is derived from previous devices such as GCAP-III and GCAP1, with feature enhancements as needed to support requirements of next-generation mobile terminals.

The system-level requirements that have created the need for a new PCAP2 device include the following:

- Improved Power Cut/Power Power supply and control for external
- Stereo Audio capability for Multimedia support
- Dedicated Transceiver power supply
- The PCAP2 will also include additional features to improve system efficiency and reduce external component count such as:
- Dual SPI control interface to allow access from two independent base band processors
- Multiple Switch mode power supply controllers for buck and/or boost conversion
- Additional independent, configurable voltage regulators
- Enhanced touch screen interface
- Improved backlight controller capability

Certain functions that were available on previous devices such as GCAP-II, GCAP-III will NOT be carried over to the PCAP2 parts due to changes in system requirements or lack of use on previous products.

These include:

- Internal over voltage protection / clamp as implemented in CCAP
- Negative voltage generation charge pump
- Negative voltage linear regulators
- DSC serial communication interface

3.1 Power Management

3.1.1 Regulator Usage Description

Regulators of PCAP2 were assigned as dedicated power supplies for Neptune-LTE or Bulverde side. The functions were listed as below.

1) V1 Linear Regulator

For E2, V1 is programmed to 2.775V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 2.775V as default. V1 supplies Neptune-LTE2 analog modules and RF6025 SPI port. V1 is also used to provide I/O voltages to Bulverde sub-system. Some external level shifters power supplies were also provided by V1. V1 was assigned as label AP_IO_REG in E2 schematic.

2) V2 Linear Regulator

For E2, V2 is programmed to 2.775V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 2.775V as default. V2 supplies Neptune internal CODEC circuitry power supply and PCAP2 internal audio related circuitry such as audio amplifiers, microphone bias etc. V2 was assigned as label AUD_REG in E2 schematic.

3) V3 Linear Regulator

For E2, V3 is programmed to 1.275V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 1.275V as default. V3 supplies the power for Bulverde VCC_SRAM power. V3 was assigned as label VCC_SRAM in E2 schematic. This regulator can be switched off when Bulverde entering into sleep mode, the control signal for this is PWR_EN of Bulverde.

4) V4 Linear Regulator

For E2, V4 is programmed to 2.775V as default. V4 supplies the power for PCAP2 internal circuitry such as SPI module and Neptune-LTE2 IO supply. V4 was assigned as BB_IO_REG in E2 schematic.

5) V5 Linear Regulator

For E2, V5 is programmed to 2.775V as default. V5 supplies the power for PCAP2 internal circuitry such as SPI module and RF2025 related circuitry etc. V5 was assigned as VCO_REG in E2 schematic.

6) V6 Linear Regulator

For E2, V6 is used as Bluetooth RF power supply.

7) V7 Linear Regulator

For E2, V7 is programmed to 2.775V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 2.775V as default. V7 supplies to RF6025 related circuitries. V7 was assigned as label RF_REG in E2 schematic.

8) V8 Linear Regulator

For E2, V8 is programmed to 1.275V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 1.275V as default. V8 supplies the power for Bulverde VCC_PLL power. V8 was assigned as label VAP_PLL in E2 schematic. This regulator can be switched off when Bulverde entering into sleep mode, the control signal for this is PWR_EN of Bulverde.

9) V9 Linear Regulator

For E2, V9 is programmed to 1.575V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 1.575V as default. V9 supplies to Neptune LVDD1 as Neptune internal reference voltage. V9 was assigned as label REF_REG in E2 schematic.

10) V10 Linear Regulator

.V10 is not used in E2 design.

11) VAUX1 Linear Regulator

VAUX1 is not used in E2.

12) VAUX3 Linear Regulator

For E2, VAUX3 is programmed to 2.800V and is supplied directly by B+. This regulator is off when the radio is turned on, and the initial power-up level is 0V as default. VAUX3 supplies power to Trans-Flash card. VAUX3 was assigned as label VCC_TRANSFLASH in E2 schematic.

13) VAUX4 Linear Regulator

VAUX4 is not used in E2.

14) SW1 Switching Regulator

For E2, SW1 is programmed to 1.2V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 1.20V as default. SW1 supplies power to Bulverde VCC_CORE domain. SW1 was assigned as label AP_CORE in E2 schematic.

15) SW2 Switching Regulator

For E2, SW2 is programmed to 1.875V and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 1.875V as default. SW2 supplies power to Bulverde memory system and Neptune-LTE2 memory interface. SW2 was assigned as label VBUCK in E2 schematic.

16) SW3 Switching Regulator

For E2, SW3 is programmed to 5.5V as default and is supplied directly by B+. This regulator is on whenever the radio is turned on, and the initial power-up level is 5.50V as default. SW3 supplies power to EMU Bus One-Chip and Fun-Light LEDs. SW3 was assigned as label VBOOST_EMU in E2 schematic.

3.1.2 Power Distribution Tree

PCAP2 provides all the regulated power supplies to Neptune-LTE subsystem, Bulverde adjunct processor sub-system, Bluetooth system and other system etc.

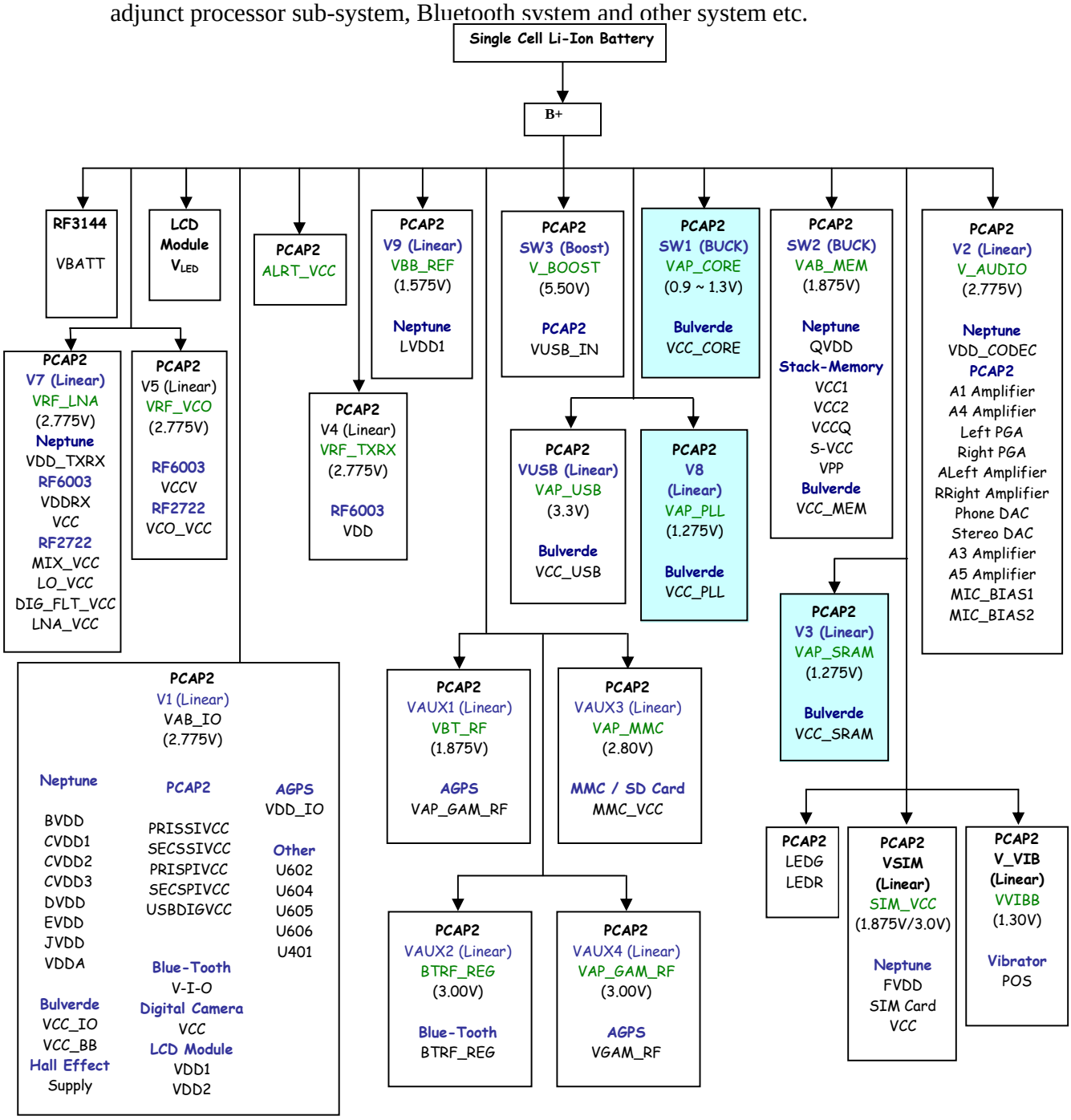


Figure 1 - Power Distribution Tree

3.1.3 E2 Power Management Control

There are two standby control signals in PCAP2, which is different from PCAP design. In E2 power management design, one standby control pin of PCAP2 is connected to Neptune-LTE standby pin and another standby control pin is connected to Bulverde PWR_EN pin. (It needs to be inverted as PCAP2 required).

During the period of Neptune-LTE in standby mode, Neptune-LTE asserts its STANDBY pin and PCAP2 shutdown the power supplies to Neptune-LTE subsystem needed to be for power saving purpose. The power supplies need to be switched off for Neptune-LTE standby mode are V7, V4 & V5.

In E2 adjunct processor power saving mode, Bulverde needs to enter into Sleep mode for achieving minimum power consumption. That needs the power supplies provided to Bulverde Core, PLL and internal SRAM power domain to be switched off after Bulverde entered into sleep mode. The pin PWR_EN of Bulverde will be changed from logic HIGH to logic LOW after Bulverde entering into Sleep mode. The inverted PWR_EN (nPWR_EN) was connected with PCAP2 STANDBY2 pin in E2, so when STANDBY2 of PCAP2 was changed from logic LOW to logic HIGH, the power supplies to Bulverde Core, PLL and internal SRAM can be shutdown. Two types of power supplies involved into Bulverde sleep mode operation, one is a linear regulator and another one is switching mode regulator.

Fehler! Verweisquelle konnte nicht gefunden werden. illustrates the waveform of control sequence for VCC_SRAM, VCC_PLL, and VCC_CORE with PWR_EN.

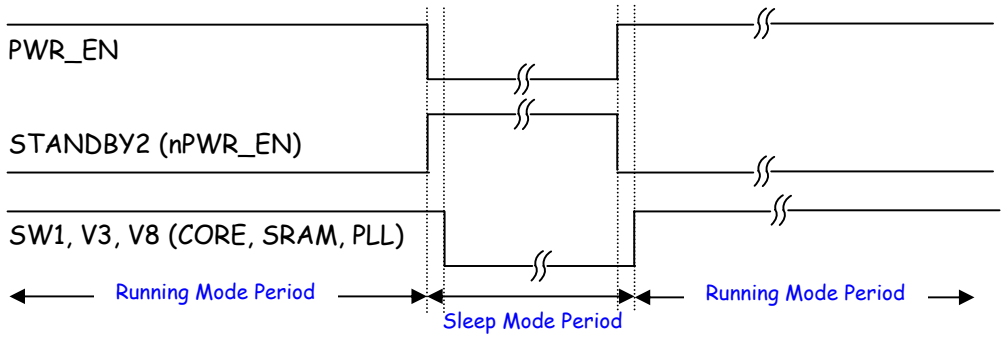


Figure 2 – E2 Bulverde Sleep and Operation Mode Power Supply Control

The state of PWR_EN signal of Bulverde will change from high to low automatically after software entering into sleep mode and can automatically change back to high from low while triggered by wakeup events settled by software. There is a small delay for SW1, V3 and V8 to setup after STANDBY2 pin changed from high to low. But that is within the timing requirement of Bulverde.

3.1.4 E2 Audio Routing and SPI Control

The audio system of E2 composed of Neptune, Bulverde and PCAP2. Neptune and Bulverde control the PCAP2 audio portion through the SPI port. E2 audio routing and SPI control connection block diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

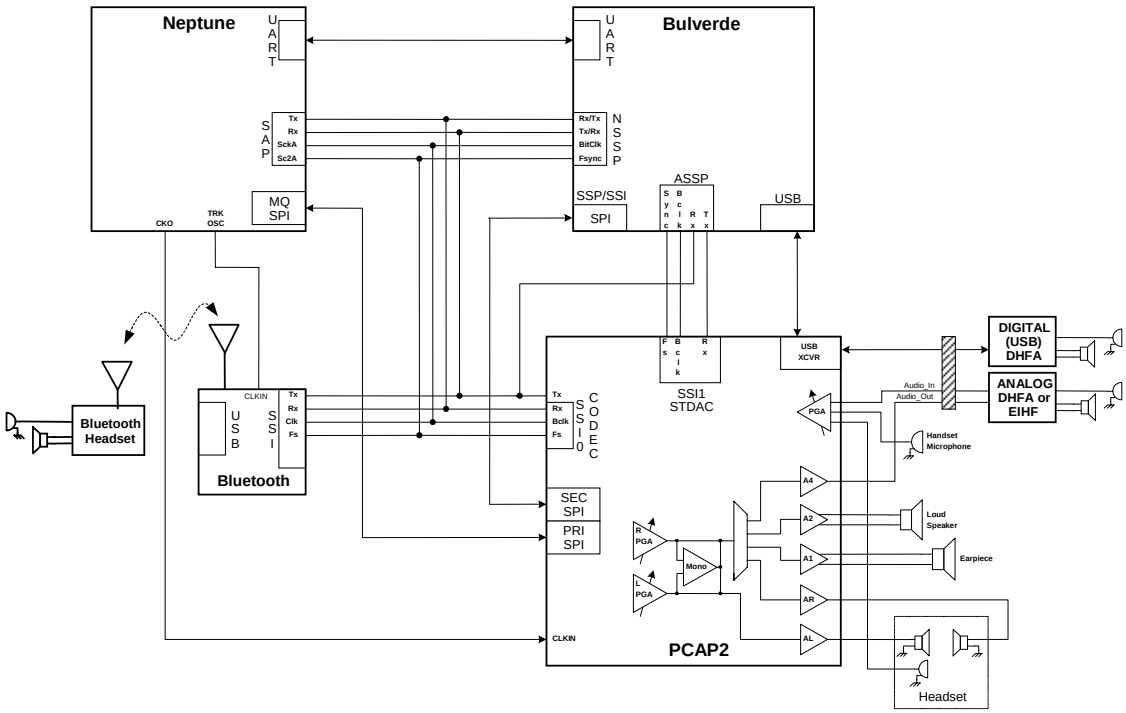


Figure 3 – E2 Audio Routing and SPI Control Block Diagram

3.2 E2 Audio System and PCAP2 Audio Section

3.2.1 E2 Audio System Architecture Block Diagram

AE2 phone design supports the voice audio, stereo audio and Bluetooth audio as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**-10. The RX path is shown in Blue, the TX path is shown in Red. Clock and Frame Synchronisation are highlighted in thick black lines.

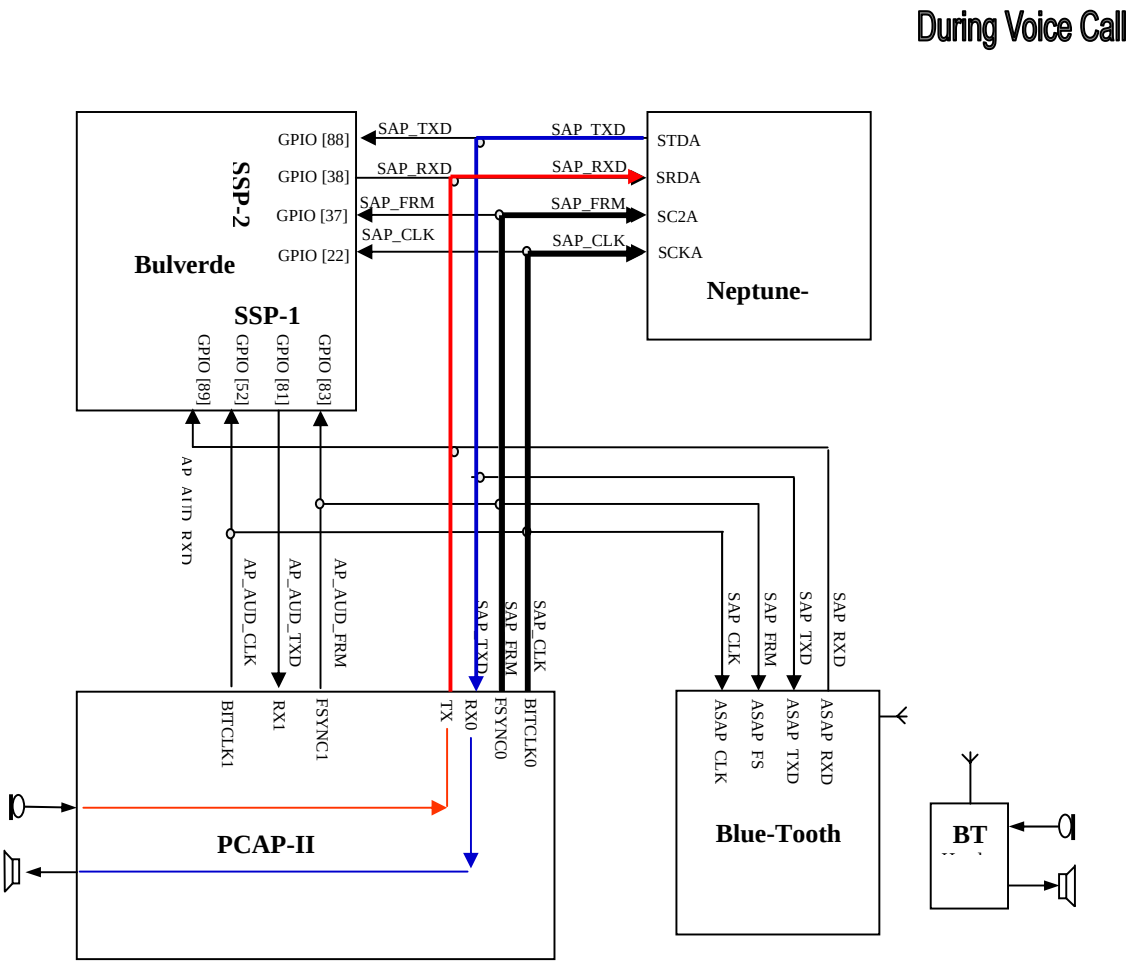


Figure 4 – E2 Audio System Architecture Block Diagram – SAP communication - during Voice Call-

During Blue-Tooth Voice Call

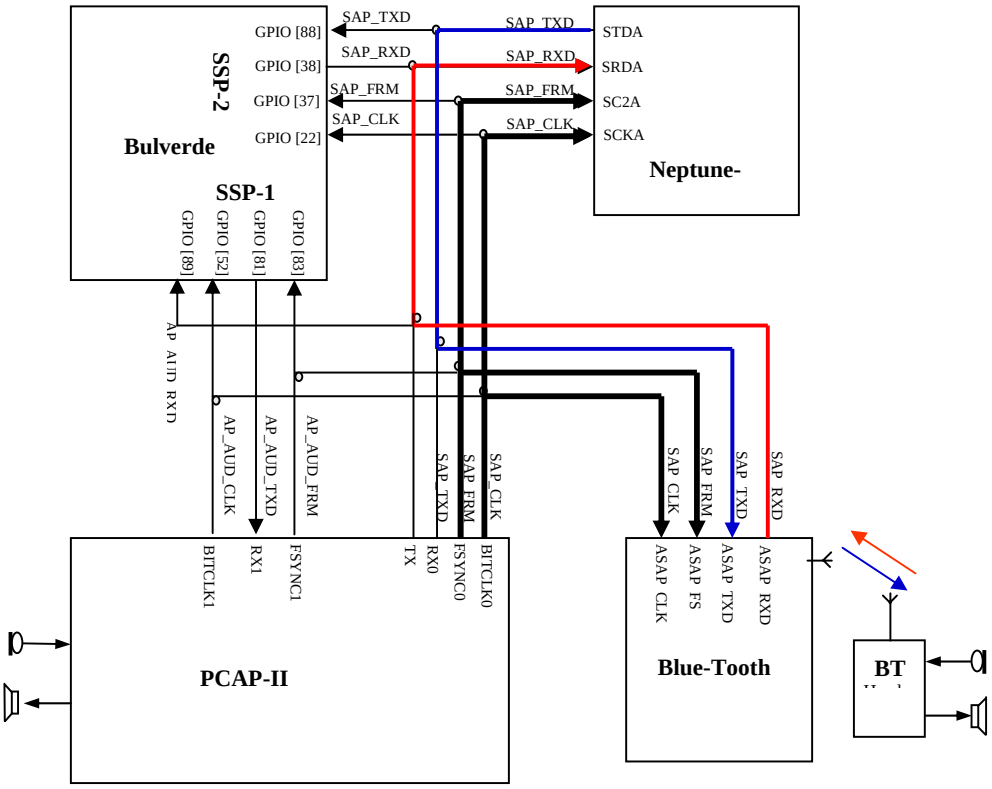


Figure 5 – E2 Audio System Architecture Block Diagram – SAP communication - during Blue-Tooth Voice Call-

Voice Record During Call

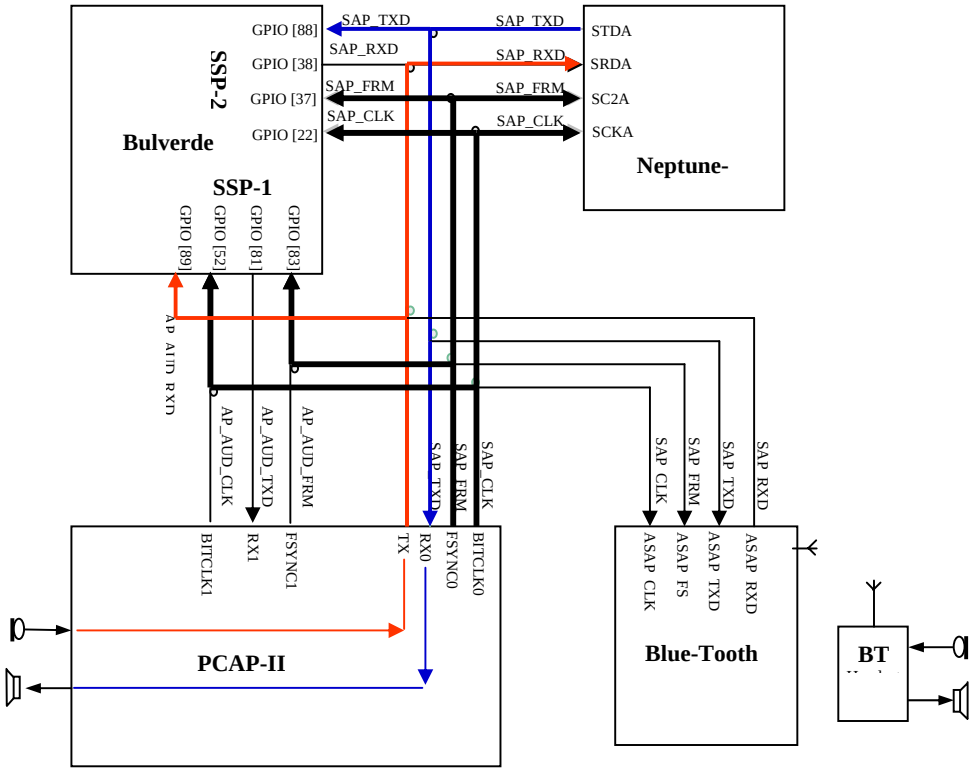


Figure 6 – E2 Audio System Architecture Block Diagram – SAP communication – Voice Record During Call-

Voice Record During Blue-Tooth Call

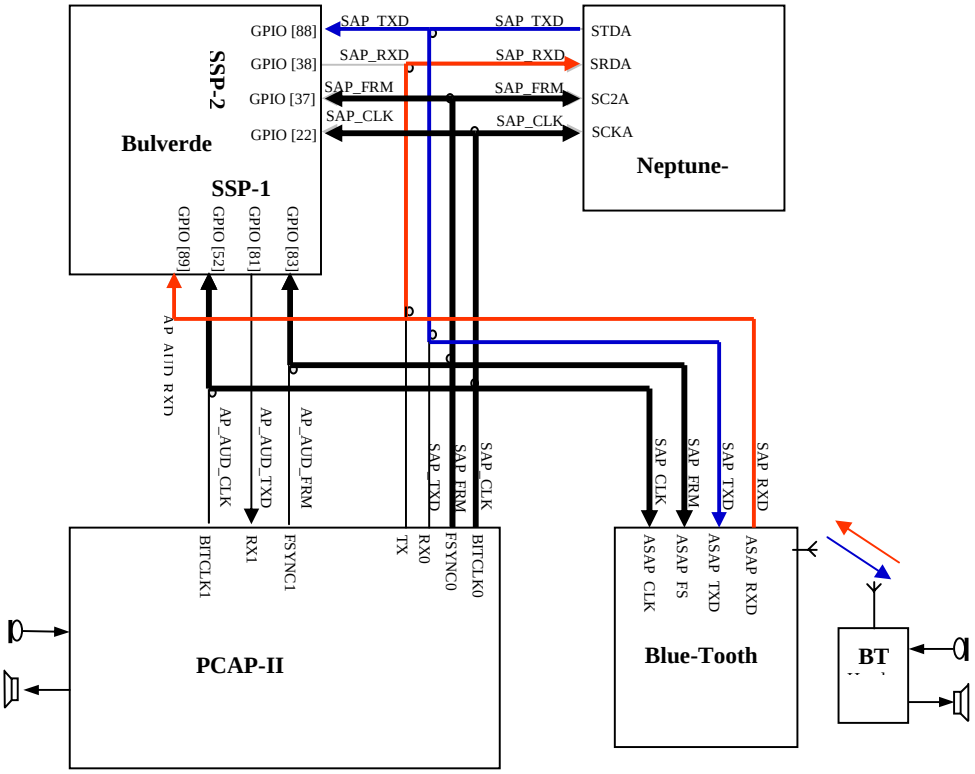


Figure 7 – E2 Audio System Architecture Block Diagram – SAP communication – Voice Record During Blue-Tooth Call-

Local Audio Record

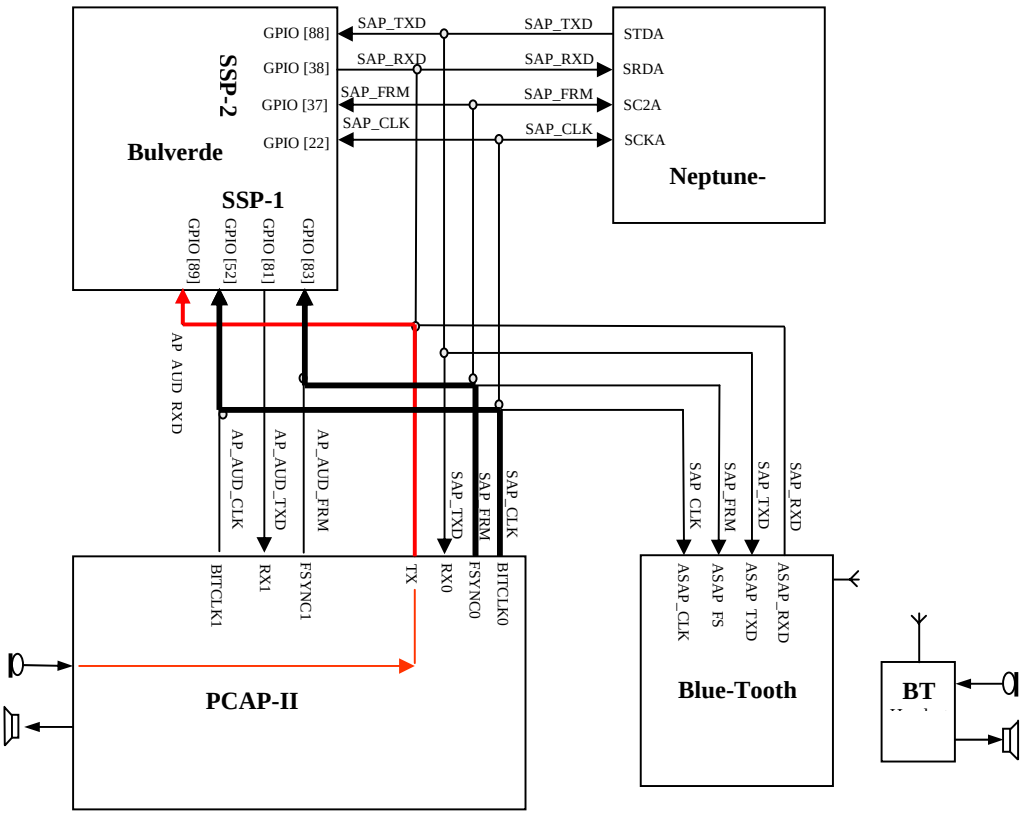


Figure 8 – E2 Audio System Architecture Block Diagram – SAP communication – Local Audio Record-

Local Audio Playback

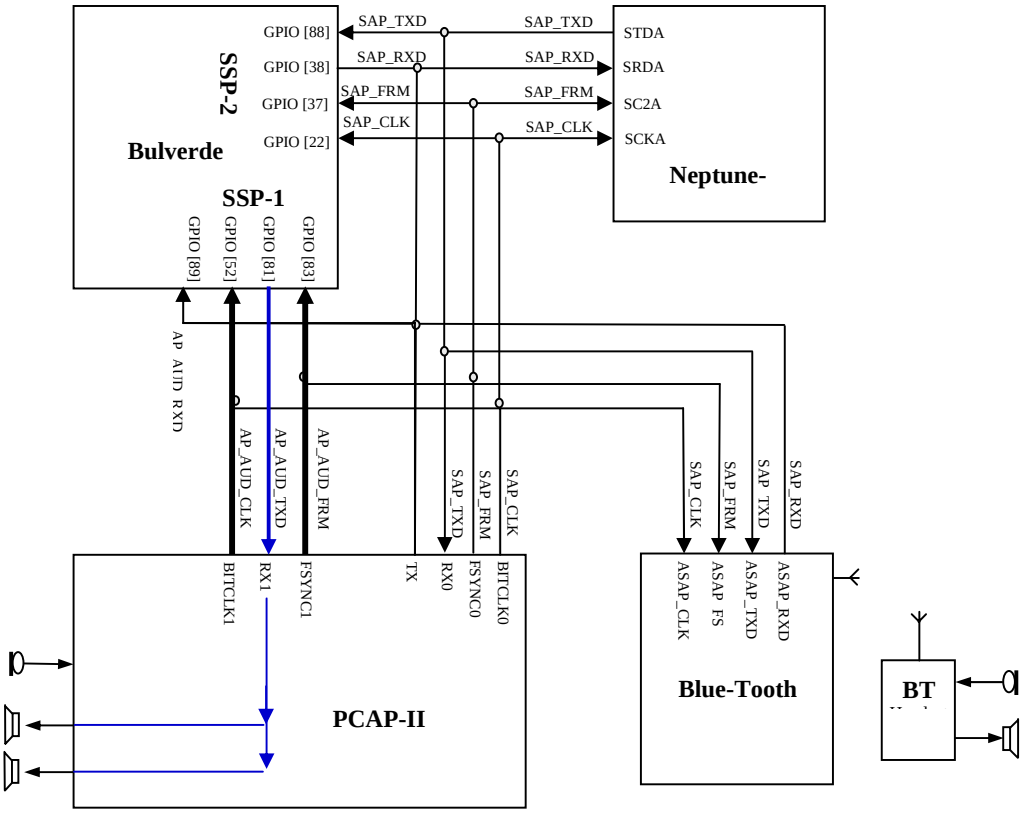


Figure 9 – E2 Audio System Architecture Block Diagram –SAP communication – Local Audio Playback (MP3, FM Receiver, Voice Notes, Sounds)-

3.2.2 Audio Input Section

PCAP2 Audio Input Section block diagram shows in Figure11. Any one of three equivalent microphone inputs can be selected. These inputs are MIC_OUT (**HJACK_MIC**) , AUX_OUT (**INT_MICP**) and EXT_MIC (**AUDIO_IN**). These three inputs are single ended. The differential input microphone amplifier A3 and A5 are not in use.

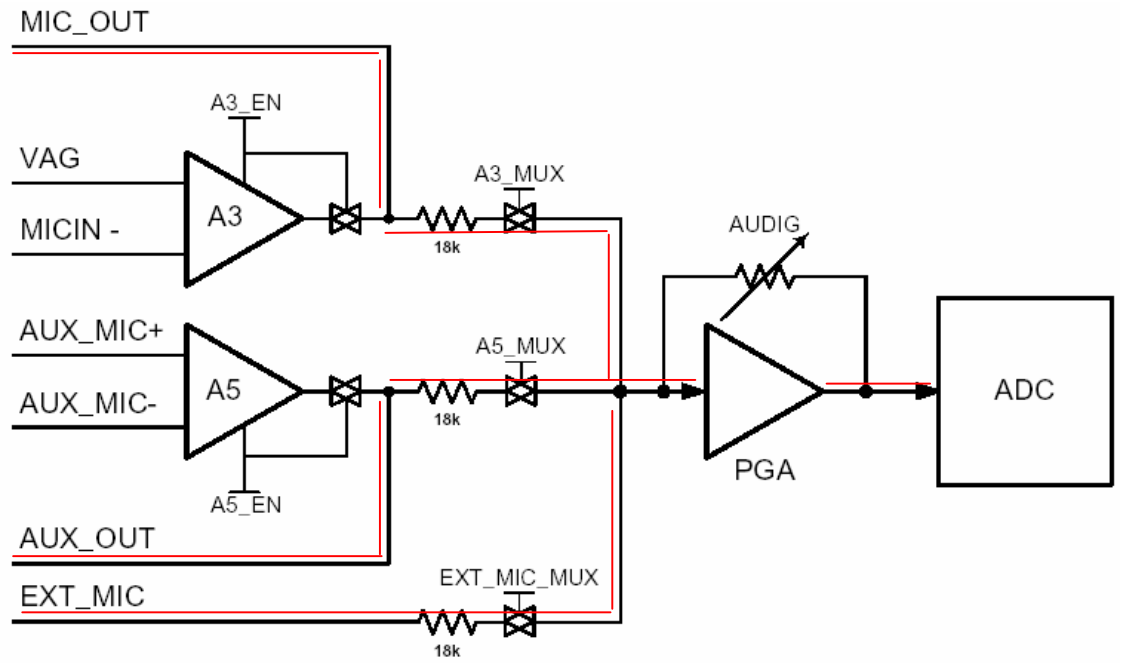


Figure 10 - PCAP Audio Input Section

3.2.3 Audio Output Section

PCAP2 Audio Output section block diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

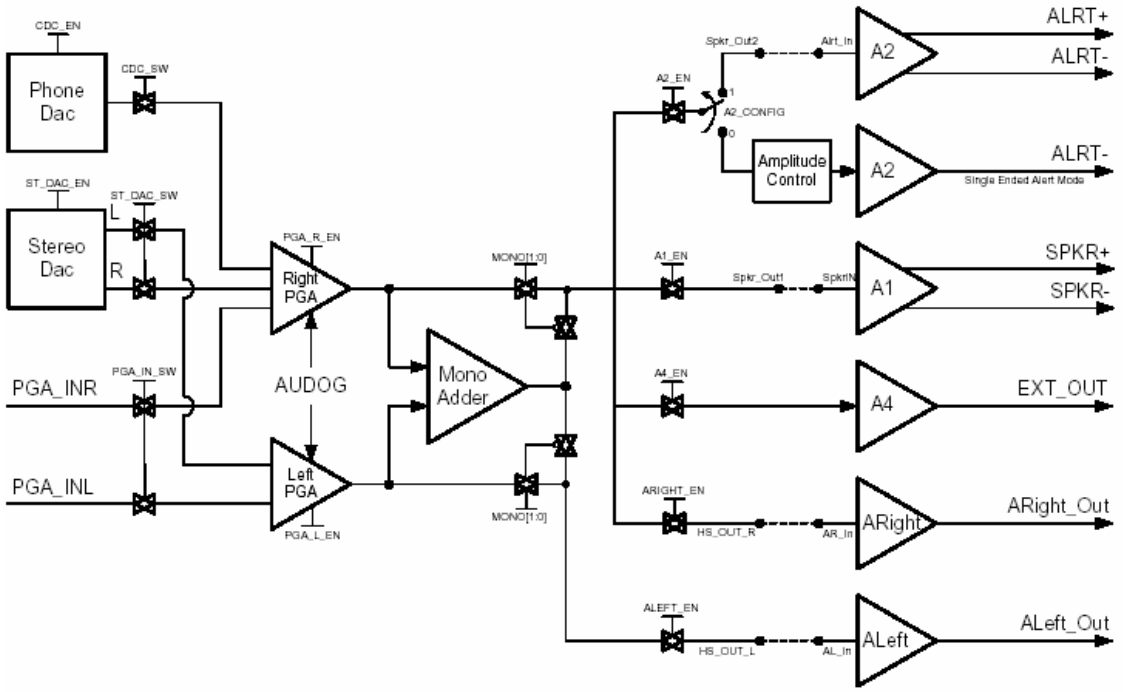


Figure 11 - PCAP2 Audio Output Section Block Diagram

It shows that the audio out of the telephone CODEC or the right channel of the stereo DAC can be routed via the right PGA to any one of four outputs. These outputs are: the internal earpiece speaker amplifier, A1, the alert amplifier, A2, the external speaker amplifier, A4, or the dedicated headset right channel speaker amplifier, ARight. The Mono adder can be used to sum the left and right channels of the stereo DAC or signals supplied to the left and right PGA inputs. The Mono adder can then attenuate the summed signals by 0dB, 3dB or 6dB and an identical monophonic signal to any of output amplifiers mentioned above.

3.3 A/D Conversion And Channel Allocations

The A/D conversion functions are performed by PCAP2 chipset through the connections between PCAP2 and Neptune-LTE, PCAP2 and Bulverde via read & write accessing SPI port. The A/D converter of PCAP2 is a 14-Channel, 10-bit converter with a state machine to control the various modes of operation. That 14-channel input is split into two groups and each one with 7-channel.

AD_SEL (internal signal) selects between two groups of 7 input signals. If set to Zero then LiCell, BATSENSE, B+SENSE, MPBSENSE, AD4, AD5, and AD6 are read and stored into the PCAP2 registers when the conversion finished. If AD_SEL is set to One then AD7, AD8, AD9, TSX1, TSX2, TSY1, and TSY2 are read and stored. This is done to shorten the total read time and to reduce the required storage of converted values.

This is shown in the **Fehler! Verweisquelle konnte nicht gefunden werden.** for AD_SEL = 0.

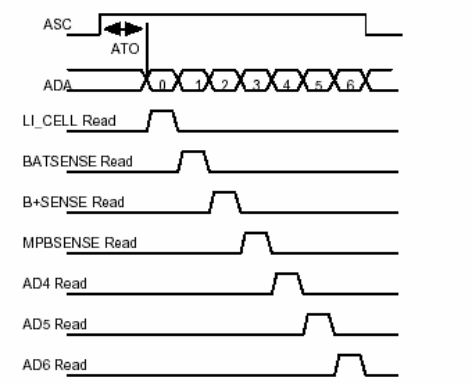
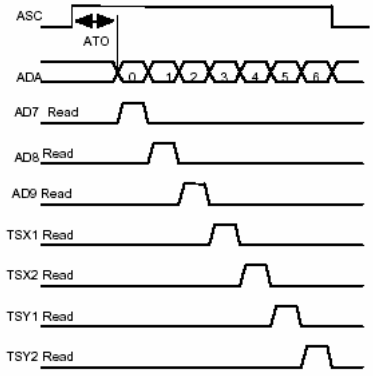


Figure 12 - PCAP2 A/D Conversion Timing Diagram with AD_SEL = 0

If AD_SEL = 1 then the channels converted are as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**.



3.3.1.1.1.1.1

Figure 13 - PCAP2 A/D Conversion Timing Diagram with AD_SEL = 1

E2 A/D converter allocation listed in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

		Address			
Input	Internal / External	**Signal**	**Purpose**	**Condition**	**A/D Voltage**
AD1	Internal	Li-Cell	Backup cell voltage monitoring	1.5V ~ 4.5V	0.4V ~ 2.3V
AD2	Internal	BATT_SENSE	Battery terminal voltage monitor for charge & discharge control	2.0V ~ 5.5V	0.4V ~ 2.3V
AD3	Internal	B+_SENSE	B+ terminal voltage monitor for charge & discharge control	2.5V ~ 6.5V	0.4V ~ 2.3V
AD4	Internal	MPBSENSE	EXT_B_ terminal voltage monitor for charger type identification and charge control	2.7V ~ 6.5V	0.4V ~ 2.3V
AD5	External	BATT_THERM	Connect with battery thermo voltage for battery pack temperature monitor during charge and discharge	25°C	1.28V
AD7	External	/	Not used in E2 design	N/A	
AD6	External	CHRG_ID	Connect with Mini-USB connector and functions as accessory ID identify	Mid-Rate	1.254V
				Full-Rate	1.955V
AD9	External	/	Not used in E2 design	N/A	N/A
AD8	External	/	Not used in E2 design	N/A	N/A
AD10	External	/	Not used in E2 design	N/A	N/A
AD11	External	TSX1	Connect with resistive touch panel for X - position reading	Position dependence	0.4V ~ 2.3V
AD12	External	TSX2	Connect with resistive touch panel for X - position reading	Position dependence	0.4V ~ 2.3V
AD13	External	TSY1	Connect with resistive touch panel for Y - position reading	Position dependence	0.4V ~ 2.3V
AD14	External	TSY2	Connect with resistive touch panel for Y - position reading	Position dependence	0.4V ~ 2.3V

Table 1 – E2 A/D Converter Allocation Table

3.3.2 Detailed Description Of Each A/D Channel

1) (AD1 internal PCap) (LICELL)

The coin cell battery voltage can be monitored at this channel of A/D converter. This can be used to do the decision for power cut, user off etc functions.

2) (AD2) (BATTI)

This A/D converter input directly is connected with battery positive pin for terminal voltage monitoring for both charge & discharge battery gas-gauge display. This A/D input comes from PCAP2 pin **BATTI** with which battery positive pin internally connected.

3) (AD3) (PCAP_BP)

This A/D converter input is connected with B+ and is used to do the voltage monitoring during discharge. Software can use this A/D channel to do the software shutdown when the battery voltage is too low to provide the power to the whole phone. The threshold of shutdown is stored in the battery EPROM and was read back during the phone power up.

5) (AD4) (THERM)

This A/D channel is used to do the monitoring of battery pack temperature. There is a thermo-resistor built into the battery pack, which can be used to do the temperature measurement for battery charge and discharge safety use purpose. This A/D channel is internally connected with AD4 of PCAP2 with which battery pack thermo-resistor connected. The connection block diagram shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**.During standby mode operation period, the Standby signal will disconnect the V2 from the thermo-resistor for power saving. The voltage input to AD4 should be within 0.4V ~ 2.3V.

The characteristic of the thermo-resistor is in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

There is a capacitor connected at AD5 with ground for interference proof.

At room temperature, the nominal resistance of RT is 10KΩ. And the voltage at AD5 is 1.28V.
When the battery pack is removed from the board, the voltage at AD4 is 2.70V roughly.

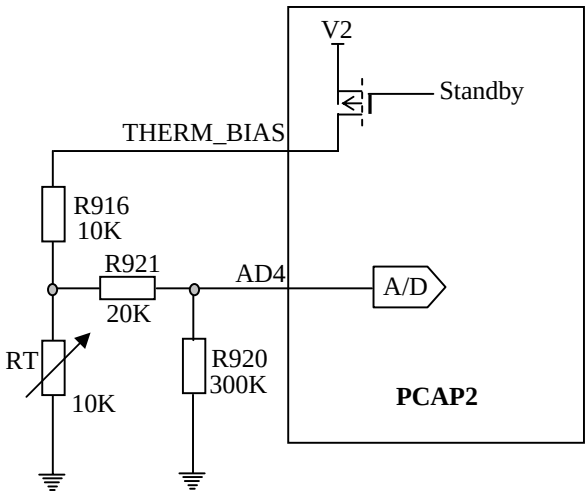


Figure 14 - Battery Thermistor Connection Block Diagram

Temperature	$R_{Thermistor}$	Voltage
°C	KΩ	V
No Battery	Infinity	2.52
-40	336.60	2.45
-35	242.80	2.43
-30	177.00	2.39
-25	130.40	2.35
-20	97.12	2.29
-15	92.98	2.28
-10	55.34	2.15
-5	42.34	2.05
0	32.66	1.95
5	25.40	1.83
10	19.90	1.7
15	15.71	1.56
20	12.49	1.42
25	10.00	1.28
30	8.06	1.15
35	6.53	1.02
40	5.33	0.89
45	4.37	0.78
50	3.60	0.68
55	2.99	0.59
60	2.49	0.52
65	2.08	0.45
70	1.75	0.39
75	1.48	0.33
80	1.26	0.29

Table 2- Battery Thermistor Readings Over Temperature

5) (AD5) (ACC_ID)

This channel A/D connected internally with EXT_B+. This A/D can be used to monitor the charger's /accessory type prior to charging.

4 Neptune-LTE Logic Interfaces

E2 Quad-band design decided to use Neptune-LTE 257-PIN as its base band call processor chipset IC. Neptune-LTE IC is a digital base band processor for the 2.5 / 2.75G GSM market. It is a dual-core processor that contains a Synthesizable Onyx DSP core (566xx), an ARM7TDMI-S micro-controller, and custom peripherals.

Neptune-LTE is available in two packages; 257-Pin Neptune-LTE chipset is used in E2 Quad-band final design.

Neptune-LTE connects with Bulverde, PCAP2, RF6025 etc to build the E2 system architecture.

4.1 Neptune LTE IC Description

The Neptune IC is a digital baseband processor. It is a dual-core processor that contains a Synthesizable Onyx DSP core (566xx), an ARM7TDMI-S micro controller, and custom peripherals. The Neptune IC is optimized for 2.5G GSM based applications. The Neptune IC will be ROM-based using mainly internal memory and an external flash. The Neptune IC is optimized for GSM based applications.

4.2 Neptune Functional Summary

4.2.1 DSP

The DSP56600 S-ONYXU core in Neptune operates at a maximum output frequency of 104 MHz. This performance will be utilized to support General Packet Radio Service (GPRS), High Speed Circuit Switched Data (HSCSD), extended Voice Annotation (VA), Voice Recognition (VR), and other features.

4.2.2 ARM7 MCU

The ARM7TDMI-S is a member of the ARM family of general-purpose 32-bit microprocessors. The ARM family offers high performance for very low power consumption and gate count.
The ARM7 MCU core in Neptune operates at a frequency up to 52 MHz. The increase in processor frequency will increase performance of critical routines located in internal memory.

4.2.2.1 MCU Memory

Neptune has 901K x32 of internal memory accessible by the MCU. A 792Kx32 block of internal memory will be implemented as ROM, while the remaining 109Kx32 block will be implemented as RAM.

4.2.2.2 MCU Peripherals

The functions of the MCU peripherals for the Neptune IC are summarized below. Each peripheral provides the ability to disable the clock at the input to the module. Each peripheral provides a software reset capability. The software reset must reset the peripheral in the same way as a system reset. Neptune includes some clock control logic outside of the peripheral blocks. The Clock Control Module handles this supplemental clock control.

1) Multiple Queue Serial Peripheral Interface (MQSPI)

The MQSPI provides two (2) independent QSPI channels which performs the serial programming operations to configure the RF subsystem and selected peripherals. It is designed to minimize the amount of MCU interaction by automating multiple and repetitive serial data transfers. The module has multiple queues to hold these transfers. Module transfers can be triggered by the Layer 1 Timer.

2) SIM Interface Modifications (SIM)

The SIM module is a customized UART with additional features allowing for communication with SmartCards and conforming to the ISO 7816 specification.

2) Universal Asynchronous Receiver Transmitter (UART)

A UART module performs all normal operations associated with “start-stop” asynchronous communications. The UART transmit and receive buffer sizes are 32 bytes each. The UART modules will operate at 115.2Kbps, 460Kbps, and 920Kbps based on a 13MHz input reference clock.

3) Deep Sleep Module (DSM)

The Deep Sleep Module allows for optimal power savings in idle modes by allowing the Neptune IC to synchronize to the frame timing automatically even though the timing reference has been removed from the part during the idle time.

4) Watchdog Timer (WDOG)

The Watchdog Timer is used to protect against system failures by providing a means to escape from unexpected events or application errors. Once started, the timer must be serviced by the core on a periodic basis. If servicing does not occur, the module time out and asserts the reset signal.

5) Keypad Port (KPP)

The Keypad port is a module that is used for keypad matrix scanning.

6) Real Time Clock (RTC)

The real time clock (RTC) module consists of counters and registers used to maintain the day, time of day and alarm values. The RTC operates even when the phone is powered down and the alarm function can turn it on and alert the processor. If the phone is already on, the processor is interrupted. The RTC uses a frequency reference generated on the PCAP2 using a low-cost crystal and inaccuracies in the frequency may be compensated for by trimming the modulus register value. The RTC module also provides power cut logic, and keep-alive memory that activates when a low battery condition is detected.

20) Display Memory Access Controller (DMAC)

The DMAC (display memory access controller) module is designed to transfer data from the display frame buffer in system memory to an external LCD display device.

21) Clock Control Module (CCM)

The Clock Control Module handles all intermodule clock routing, the selection of multiple input clock sources for the cores and various peripherals, manage MCU low power modes (DOZE, STOP and WAIT) by disabling peripheral clocks and other clock related features. This module also includes the control logic for asserting soft and hard chip-level system resets.

22) External Interrupt Module (INT)

This module provides control for five of the eight external interrupt sources. Each pin is individually configurable as a level-sensitive interrupt, an edge-detecting (rising, falling, or both) interrupt, or a general purpose I/O. Each pin has a dedicated interrupt line.

4.2.3 Shared Peripherals

Shared peripherals are peripherals that can be accessed by both the DSP and MCU cores. The functionality of these peripherals is detailed below.

4.2.3.1 Universal Serial Bus Module (USB)

The USB module provides the required buffering and protocol to communicate on the Universal Serial Bus. The module is provided with an access port for the DSP and for the MCU. The module will act as a USB device only. Host functionality will not be supported. All four types of USB data transfers are supported: control, isochronous, interrupt, and bulk

4.2.3.2 General Purpose I/O (GPIO)

The GPIO module is a stand alone module that serves as the all-in-one communication link between the outside world, the MCU module, and the DSP module. The GPIO module will be implemented as a stand-alone module. The GPIO module will provide the following functionality:

- Standard GPIO functionality
- Multiplexed output functionality
- Alternate input functionality
- Shared Access for DSP and MCU
- MCU, DSP interrupt capability
- Interrupt visibility

4.2.3.3 MCU / DSP Interface (MDI)

The MDI is the communication interface between the DSP and MCU cores. Through this module, each core can access shared memory, messaging registers, and flags. This module also allows each core to interrupt the other, monitor the low power state of the other core, and other useful functions.

4.2.3.4 Layer 1 Timer (L1T)

The Layer 1 Timer module allows for control of all the radio channel timings. Its main function is to unload the MCU from having to schedule events associated with the radio air interface. The timer provides the user a great deal of flexibility in scheduling and executing events using the programmable event tables and macros.

4.3 Neptune GPIO Summary

Neptune GPIO module is a stand alone module that serves as the all-in-one communication link between the outside world, the MCU module and the DSP module. The GPIO communicates with the MCU through the IP Bus and to the DSP through the DSP Peripheral Bus. The GPIO module houses five 16 pin bi-directional Ports.

4.4 Neptune-LTE Memory Interface

Although Neptune has internal ROM and RAM, it still needs external memory chipsets for its operation. One 32Mbit Flash and one 4Mbit SRAM can access by Neptune via the 16-bit parallel data bus. Each of these devices is assigned a specific chip enable(s) from the Neptune-LTE.

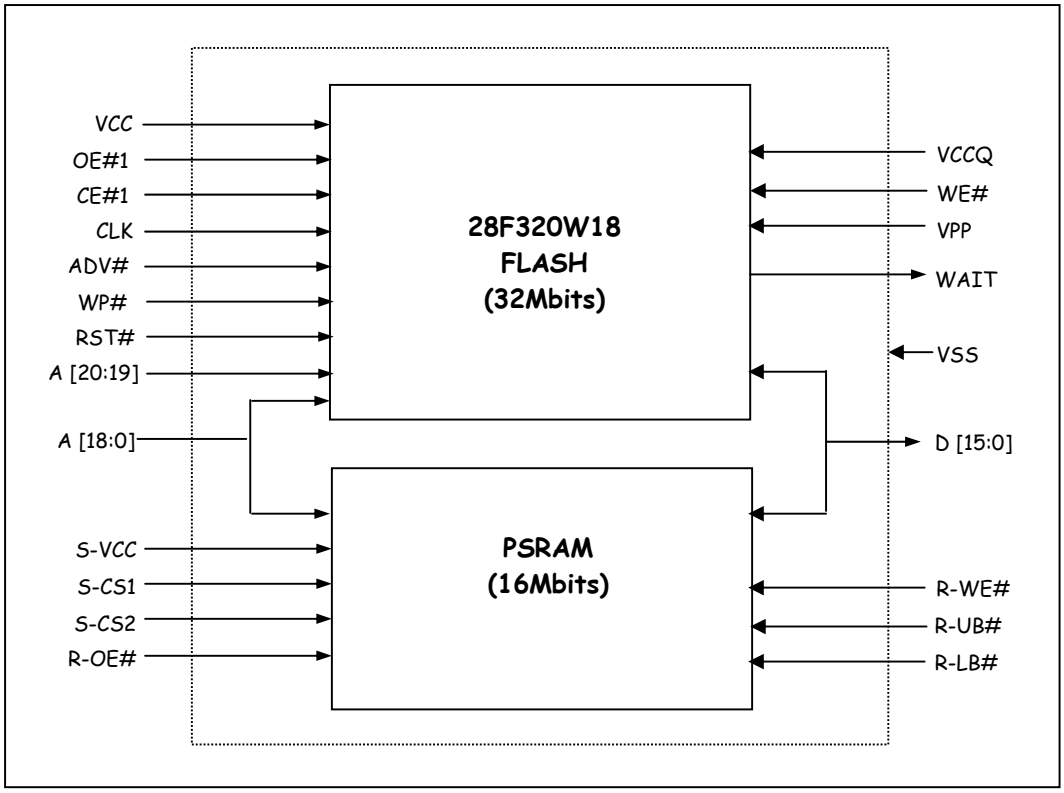


Figure 15 – E2 Baseband 32W18 + 16Mb SRAM Stacked-CSP Block Diagram

The detailed information of Flash and SRAM is described as following.

4.4.1 Flash

The Flash used in E2 phone design is Intel W18 series Flash product. The 1.8 Volt Intel® Wireless Flash memory provides RWW/RWE capability with high performance synchronous and asynchronous reads on package-compatible densities with a 16-bit data bus.

4.4.2 PSRAM

The memory size used in E2 phone design is 16 Mega bits (2 Mega bytes).

4.4.3 Neptune-LTE Chip Select Assignments

The ARM External Memory Interface Module (handles the interface to devices external to an ARM architecture based chip, including generation of chip selects for external peripherals and memory.

The six Chip Selects assigned as in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

Pin Name	Pin #	Type	Active H/L	Description
CS0	P15	O	L	Flash Chip Selection
CS1	R15	O	L	SRAM Chip Selection

Table 3 - Neptune-LTE Chip Select Assignment

EB0 * and EB1 * are assignment as the Byte selection for SRAM access. EB0 * is for SRAM lower byte and EB1 * is for SRAM upper byte access.

The memory connection with Neptune-LTE shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

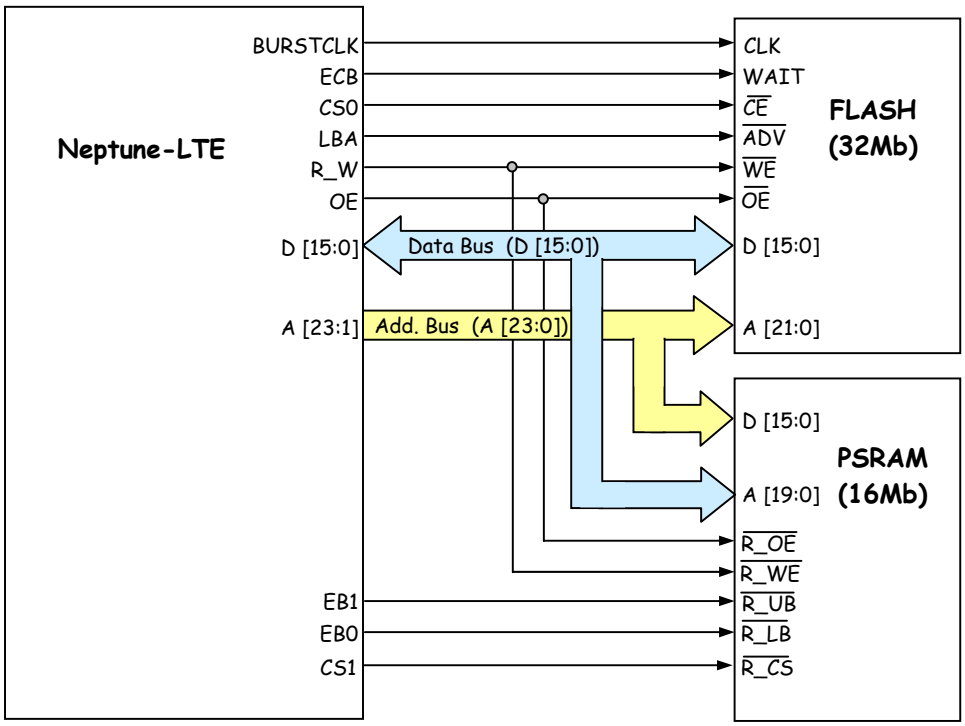


Figure 16 – E2 Baseband Neptune-LTE and Memory Connection Block Diagram

4.5 Neptune MQSPI Module

The MQSPI (Multiple Queue Serial Peripheral Interface) performs the serial programming operations to configure radio subsystems and selected peripherals. In this dual SPI configuration, the system is typically partitioned into RF and baseband functions. This peripheral is designed to minimize the amount of MCU interaction necessary for multiple serial data transfers. The MQSPI module in Neptune has the following features:

- Full-Duplex, Three-Wire Synchronous Transfers
- Half-Duplex, Two-Wire Synchronous Transfers
- Programmable Bit Rates
- Programmable Inactive Clock Polarity
- Programmable Chip Select Polarity
- Ten Chip Select Pins
- 256 X 16 bit of RAM for Data I/O Storages sharable by both SPIs
- Programmable Transfer Length - from 1 to 32 Bytes
- Programmable Multiple Message - from 1 to 64 Messages
- Each SPI functions only as a master SPI
- Dual Independently Functioning SPIs
- 32 Configurable Control Queues/Triggers
- 64 Programmable Control Data Registers (32 Mode and 32 Pointer Registers)
- Four FIFO Queues - a High and Low Priority Queue for Each SPI
- 32 One-Cold Trigger Signals From the Layer 1 Timer
- MCU Controlled Trigger Register
- Two Interrupt Lines - One for Each SPI
- Programmable Data Change on Rising/Falling Clock Edge
- Programmable Data Latch on Rising/Falling Clock Edge
- Separate Read/Write Data I/O Storage Pointers
- Burst and multiple message transfers
- Programmable 128 Clock Delay Before First Clock Edge
- Programmable 128 Clock Delay After Transfer
- Transmit and receive Data is LSB/MSB Selectable
- DOZE Mode Capability
- Serial Display Interface

E2 quad-band EDGE / GPRS GSM uses a dedicated RF SPI port for RF6025 data writing. And one MQSPI port is used to access with PCAP2 and the chip selection is SPI_CS3. The connection between Neptune-LTE and PCAP2, RF6025 shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

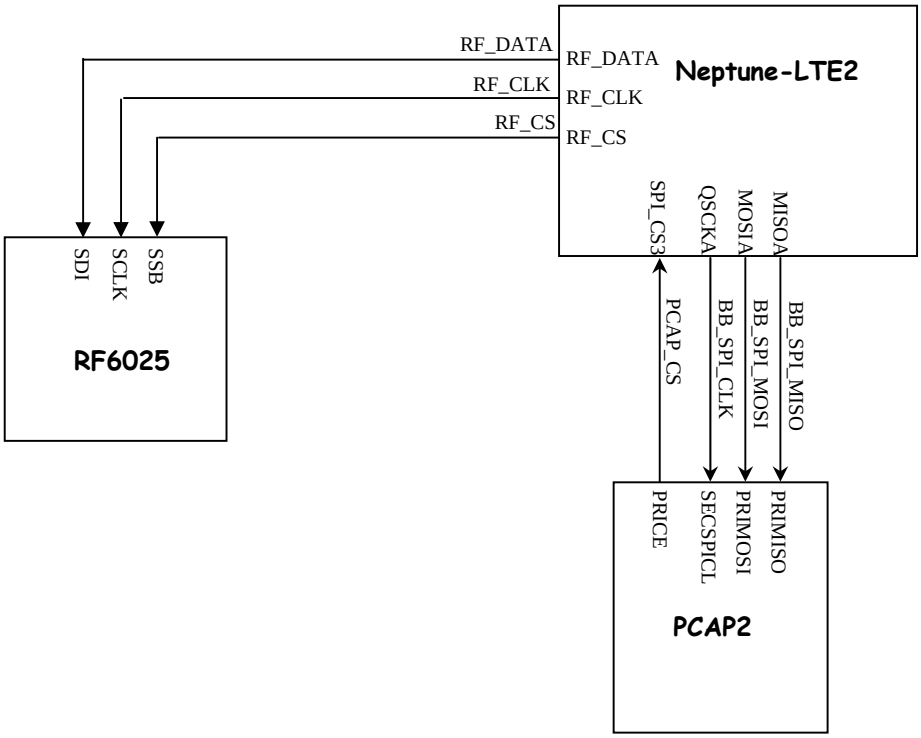


Figure 17 - Neptune MQSPI Connection with PCAP2 and RF6025 Block Diagram

4.6 SIM Interface

The SIM Interface Module (SIM) is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards. The SIM module has two ports that can be used to interface with the various cards. The SIM connection in E2 shows in **Fehler! Verweisquelle konnte nicht gefunden werden.** diagram.

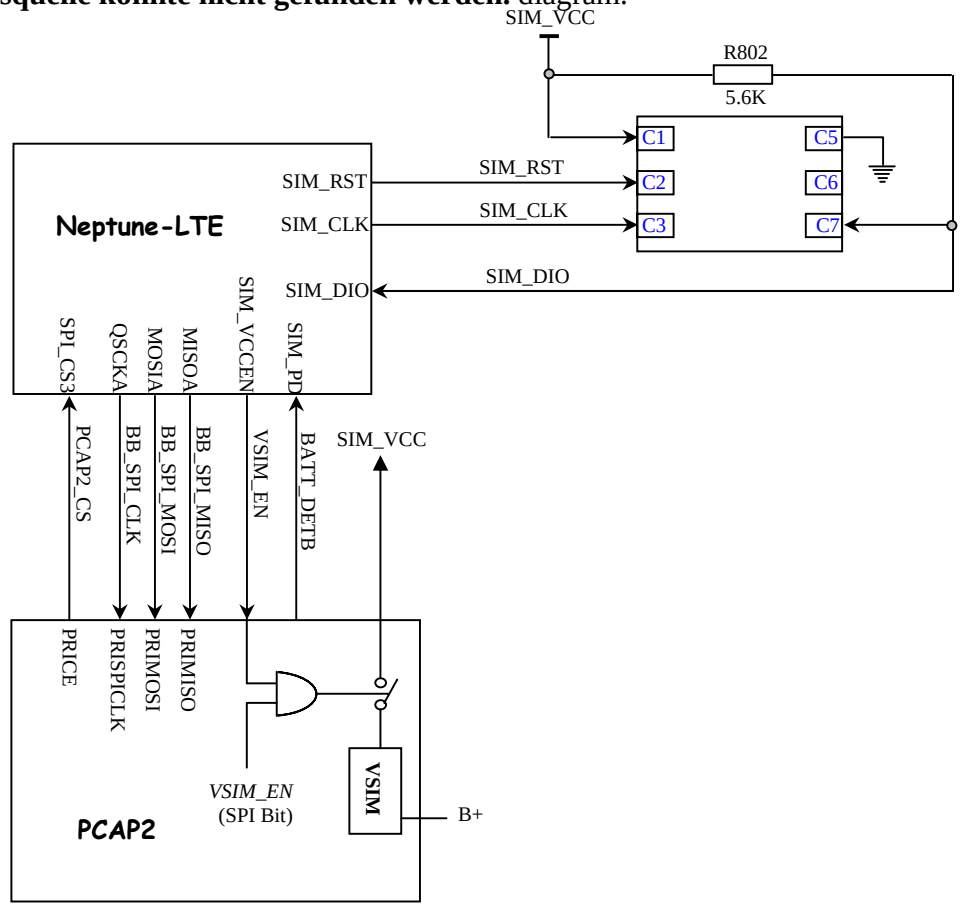


Figure 18 – E2 SIM Connection Block Diagram

E2 doesn't use PCAP2 internal level shifters for 5V SIM card support due to the fact that Neptune-LTE multiplexed the SIM data input and output together. E2 can only support 3V SIM card and no 1.8V & 5V SIM support.

The SIM detect circuit is actually a battery detection circuit in E2 design. When one of the following conditions occurs, the BATT_DETB output asserted logic 0 to indicate battery presence.

- A thermistor (with effective resistance < 38K approx) is connected to the AD4 input
- The BATT+ (battery) voltage exceeds REF2 threshold
- MOBPORTB is present AND the BATT_DET_IN signal is grounded

The PCAP2 battery detection circuit block diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

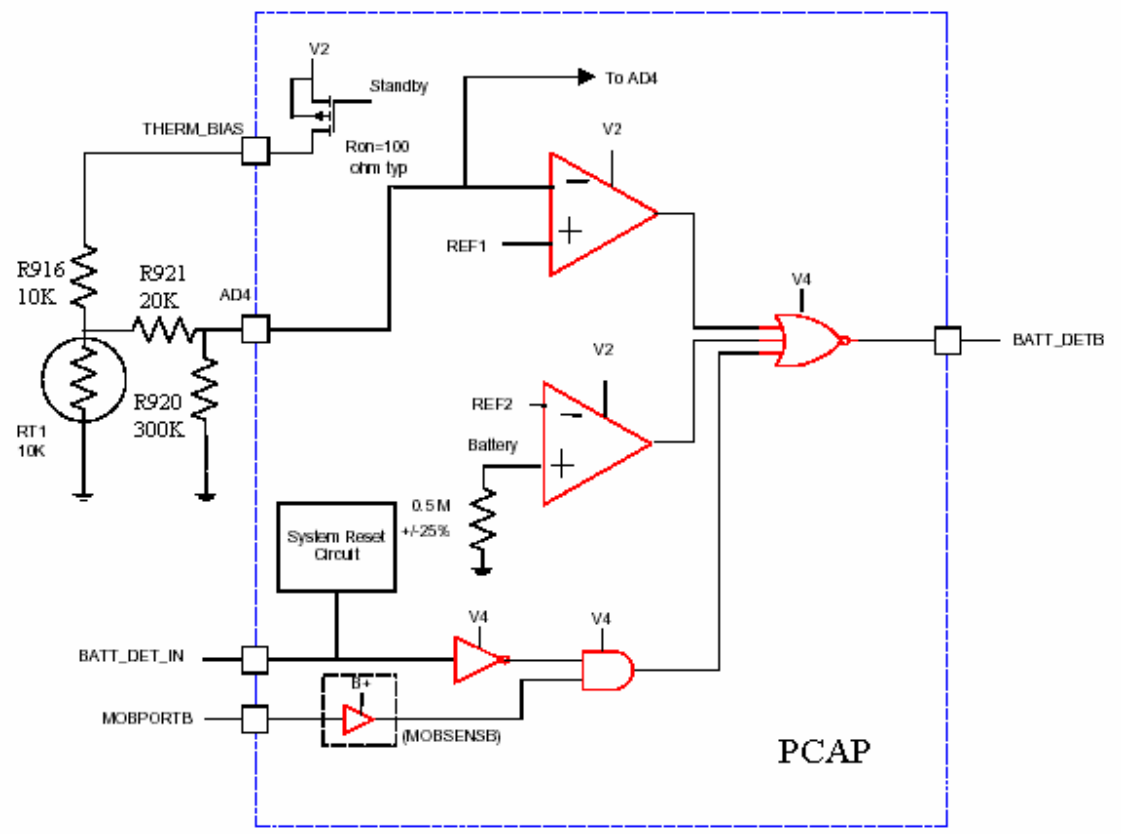


Figure 19 – E2 SIM Present Detection Circuit Logic Block Diagram

A battery must be inserted to pull the BATT_DETB (Neptune pin name is SIM_PD) line low. Software shall check to see if this line is low. If it is not low then that indicates that a battery is not present and software shall write “Insert Battery” to the display. When a battery is not present, BATT_DETB is pulled high with V2 (2.775 V). If a battery is present, then BATT_DETB is pulled low and software shall then attempt to read from the SIM card. If it does not read any data from the SIM on the SIM_I/O line then that indicates that a card is not present and software writes “Check Card” to the display.

Battery Present	SIM Card Present	Display Message	Comment
No	No	"Insert Battery"	Phone may be powered via EXT_B+
No	Yes	"Insert Battery"	Phone may be powered via EXT_B+
Yes	No	"Check Card"	Phone may be powered via battery or EXT_B+
Yes	Yes		Allow fulll phone functionality to user

Table 4 - SIM Card Presence Detect Matrix

Fehler! Verweisquelle konnte nicht gefunden werden. shows the SIM card presence detection matrix.

A battery, whether it is good (above software voltage threshold for shutdown) or bad (below software voltage threshold for power up), must be inserted to the phone to pull BATT_DETB low. If the user cannot power the phone up with the battery alone, then he or she must insert the AC Adapter as well a battery with internal thermistor to use the phone. In all the above cases, EMERGENCY CALLS are allowed.

5 Neptune-LTE RF Interface

E2 RF interface includes two separate ICs.

This section describes the interface between the Neptune LTE2 and the RF section (RFMD PRiME 2 chipset). There are two chipsets for RFMD GPRS / EDGE solutions. A brief descriptions for those chips functions etc are introduced below.

5.1.1 RF6025 Functional Description

The Polaris RF6025 transceiver module is a highly integrated transceiver intended for quad-band GSM/GPRS/EDGE applications. Included, in the module, are integrated RX SAW filters, integrated TX power VCOs and a RX VCO, a GMSK modulator; a 8PSK modulator; PA ramp control and reference oscillator circuitry for an off-module crystal oscillator.
Configuration of the transceiver is accomplished by setting internal registers via a 3-wire serial interface that connects directly to the baseband controller (Neptune). In receive, the RF6025 accepts four inputs from the switchplexer (one for each RX band) and after down-conversion and filtering sends RX I/Q data to the baseband. The output format may be either analog or digital. In transmit, the RF6025 module takes either analog I/Q data or the TX symbol data from the baseband, uses this to modulate the TX VCO and control the PA ramping signal to the PA or transmit module. The switchplexer may also be controlled with the general purpose output lines in the module.
The fractional-N synthesizer section is multiplexed between transmit and receive functions, creating two sets of PLL parameters. The PLLx0 register determines the state in which the PLL is working. Each PLL configuration has a fully integrated loop filter.
The RF6025 module has a buffered oscillator output that provides either a 13MHz or 26MHz reference output for use by the baseband. The frequency of this buffered output is user selectable.
The internal power VCO's are designed for use in the following frequency ranges: VCO1 has a frequency range of 824MHz to 915MHz; and, VCO2 has a frequency range of 1710MHz to 1910MHz. Each VCO is buffered and has a +4dBm minimum output power.

Downconversion from VLIF to baseband, and all necessary baseband filtering for GSM/GPRS/EDGE reception, is implemented digitally, with programmable bandwidths ranging from 80kHz to 135kHz.

The polar modulator used for EDGE transmit is shown below. In EDGE mode, both digital and analog interfaces are available. The RF6025 performs all of the necessary pulse shaping, and maps the data bits into amplitude and phase components for the required modulation. The phase component is pre-distorted to account for the PLL loop filter roll off and then combined with the channel selection word of the Fractional-N (FN) synthesizer, which is directly modulated onto the internal VCO. The amplitude components are scaled according to the PA ramping control signal and directly applied to the PA collector voltage control system (in the RF3144). The amplitude component in this way is directly modulated onto the PA output. **Fehler! Verweisquelle konnte nicht gefunden werden.** shows the RF6025

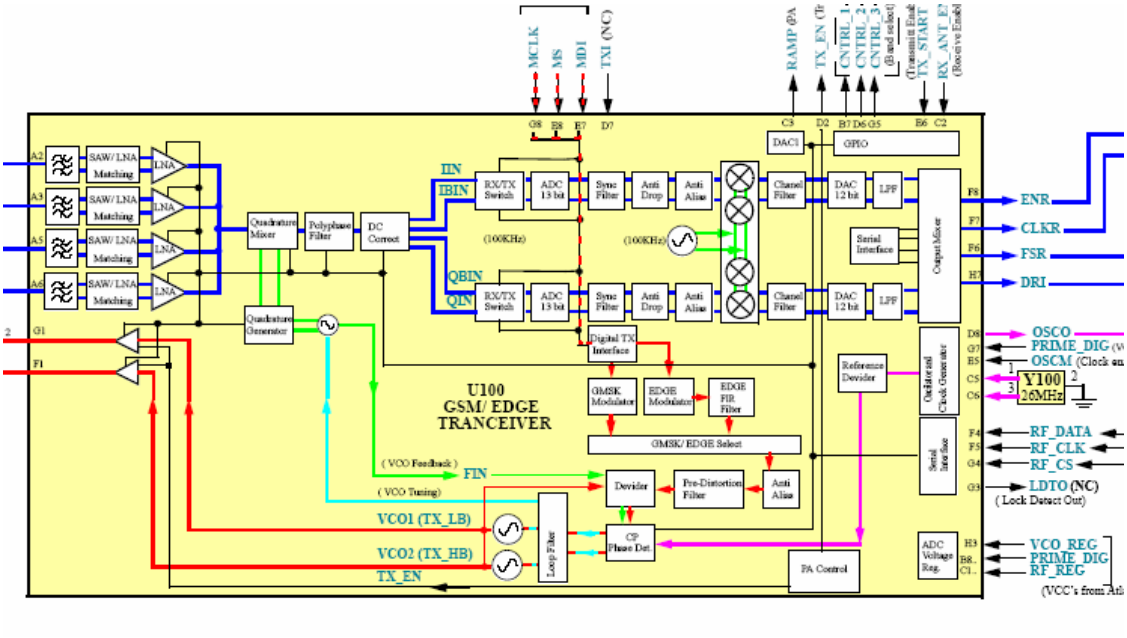


Figure 20 - RF6025 Functional Block Diagram

The GSM receive and transmit baseband interfaces can be configured to work with standard analog differential I/Q signals or fully digital signals depending on SDI programming. The GMSK modulator necessary for GSM signaling is also provided and feeds into the transmit FN synthesizer for direct modulation of the VCO's. There are two D/As (DAC1/DAC2) provided: DAC1 is configured to provide programmable ramp control for the PA; and, DAC2 for generalpurpose DC tuning voltage applications. An automatic PA ramp control function is provided, ramp shaping and timing and is the same for both GMSK and 8PSK modulation types.

5.1.2 RF6025 Serial Data Interface and Device Control

A three wire serial data interface allows user programming of the internal control registers in the RF6025. The serial data interface consists of the serial select (SSB), serial data in (SDI) and serial clock (SCLK) pins. The lock detect/test out (LDTO) pin is by default configured as an output from the serial interface, but may be used to monitor various internal PLL signals, as well.

5.2 RF3178 (Quad-Band Power Amplifier Module) Chipset

The 3144 module is a 50W input/output, quad-band, dual-mode, GMSK/8PSK(EDGE) PA module intended for 2.75G radio applications. The module consists of a dual line-up power amplifier, harmonic filter, and antenna switch. The antenna connects the antenna to any one of four receiver ports or either low band power amplifier output or high band power amplifier output. The module contains two RF dies using HBT technology, a silicon die for the power control and antenna switch controller, a harmonic filter, an DC blocks at all RF ports. The module incorporates an indirect closed loop method for power control. Output power is controlled by varying the collector voltage. The module does not have any filters/coupler/detector.

This PA module is used in the final amplification stages in a GSM portable telephone operating in either GMSK or EDGE mode. For the EDGE mode, this PA is best suited for systems employing Polar Modulation method where in the amplifier operates compression all the time.

No serial interface needs to provide control to this chipset during its operation

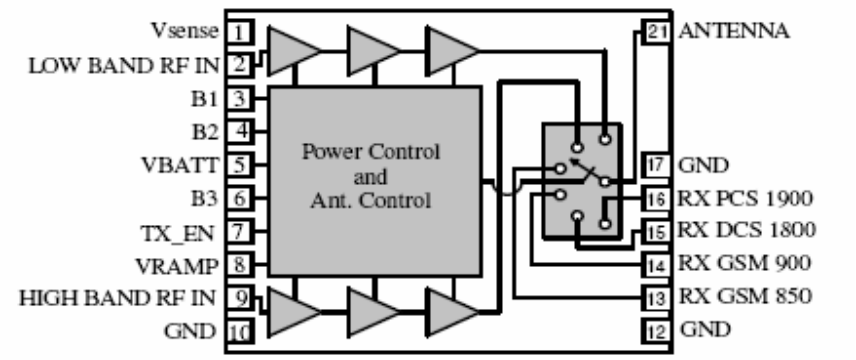


Figure 21 - RF3178 Functional Block Diagram

The band , receiver and transmit control true table shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

TX module mode	Control Pins			
	TX_EN	B1	B2	B3
Low power standby mode	0	0	0	0
RX850	0	0	0	1
RX900	0	1	0	x
RX1800	0	0	1	x
RX1900	0	1	1	x
TX low band, low output power range (VCC3 OFF)	1	x	0	0
TX low band, high output power range	1	x	0	1
TX high band, low output power range (VCC3 OFF)	1	x	1	0
TX high band, high output power range	1	x	1	1

Table 5 - RF3178 Antenna Switch Control True Table

6 Application Processor (Bulverde)

6.1 Bulverde Functional Overview

The Bulverde processor is an integrated system-on-a-chip microprocessor for high performance, dynamic, low-power portable handheld and handset devices. It incorporates the Intel® XScale™ microarchitecture with voltage and frequency scaling and sophisticated power management to provide excellent MIPs/mW performance. The processor complies with the ARM* version 5TE instruction set (excluding floating-point instructions) and follows the ARM* programmer's model. The Bulverde processor also provides Intel® Wireless MMX™ media enhancement technology, which supports integer instructions to accelerate audio and video processor.

Bulverde has the following features:

- Core frequencies supported
- 200 MHz for the PXA261 processor
- 200 - 300 MHz for the PXA262 processor
- System memory interface
  - 100MHz SDRAM
  - 4 MB to 256 MB of SDRAM memory
  - Support for 16, 64, 128, or 256Mbit DRAM technologies
  - 4 Banks of SDRAM, each supporting 64 MB of memory
  - Clock enable (CKE) – provides 1 CKE pin to put the entire SDRAM interface into self refresh
  - Supports as many as 5 external static memory devices (SRAM, flash, or VLIO) and 1 internal flash device

- PCMCIA/Compact Flash card control pins
- LCD Controller pins
- Full-function UART
- Bluetooth UART
- Hardware UART
- MMC Controller pins
- SSP pins
- Network SSP
- Audio SSP
- USB Client pins
- AC'97 Controller pins
- Standard UART pins
- I2C Controller pins
- PWM pins
- 20 dedicated GPIOs pins
- Integrated JTAG support
- Single-Ended USB client

6.2 Bulverde Memory Interface

E2 uses Intel 64MB Flash + 48MB SDRAM stack memory as application memory chipset.

The connection of Bulverde and memory shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

6.2.1 Bulverde SDRAM Interface

The processor supports an SDRAM interface at a maximum frequency of 100 MHz. The SDRAM interface supports four 16-bit or 32-bit wide SDRAM partitions. Each partition is allocated 64 MBytes of the internal memory map. However, the actual size of each partition is dependent on the particular SDRAM configuration used. The four partitions are divided into two partition pairs: the 0/1 pair and the 2/3 pair. Both partitions within a pair (for example, partition 0 and partition 1) must be identical in size and configuration; however, the two pairs can be different. For example, the 0/1 pair can be 100 MHz SDRAM on a 32-bit data bus, while the 2/3 pair can be 50 MHz SDRAM on a 16-bit data bus.

E2 assigns 32MB SDRAM in pair 0 and 16MB SDRAM in pair 1.

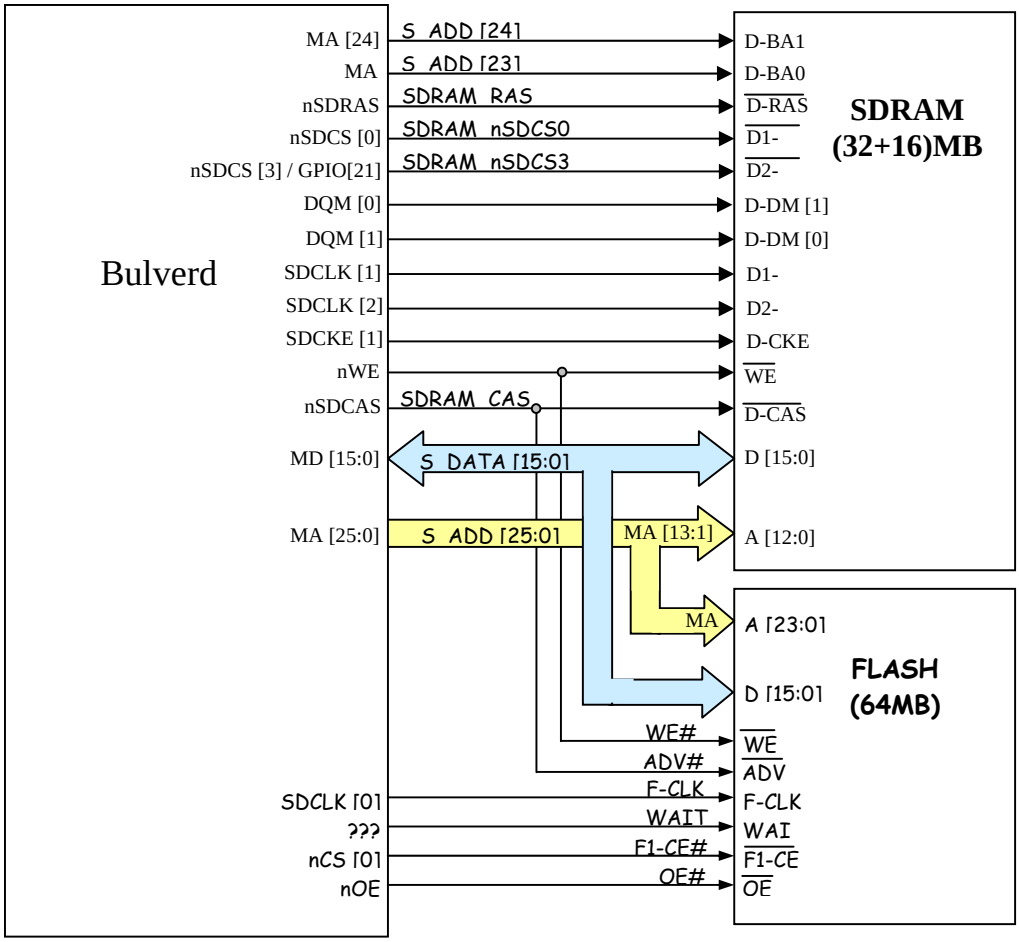


Figure 22 - Bulverde Memory Connection Block Diagram

In this diagram, each SDRAM signal functions as below:

- **S_DATA [15:0]** – Data Input / Output pins.
- **S_ADD [12:0]** – During a Bank Activate command cycle, those signals define the row address (RA0 – RA12) when sampled at the rising clock edge. During a Read or Write command cycle, S_ADD [0] – S_ADD [n] define the column address (CA0 – CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organization. In addition to the column address, S_ADD [10] (=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If S_ADD [10] is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If S_ADD [10] is low, autoprecharge is disabled. During a Precharge command cycle, S_ADD [10] (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.
- **S_ADD [23] & S_ADD [24]** – Bank Select Inputs. Selects which bank is to be active.
- **SDRAM_RAS & SDRAM_CAS** – When sampled at the positive rising edge of the clock, those two signals and SDRAM_nWE define the command to be executed by the SDRAM. SDRAM_LDQM & SDRAM_UDQM – The Data Input / Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQMx has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. LDQM and UDQM control the lower and upper bytes in x16 SDRAM.
- **SDRAM_CLK1** – The system clock input. This clock input is for 32MB SDRAM die. All of the SDRAM inputs are samples on the rising edge of the clock.
- **SDRAM_CLK2** – The system clock input. This clock input is for 16MB SDRAM die. All of the SDRAM inputs are samples on the rising edge of the clock.
- **SDRAM_CKE1** – Activates the clock signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
- **SDRAM_nSDCS0** – This signal enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This input is for 32MB SDRAM die chip-select .
- **SDRAM_nSDCS3** – This signal enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This input is for 16MB SDRAM die chip-select . GPIO[21] of Bulverde needs to be configured as SDRAM chip-selection alternative function.

6.2.2 Bulverde Flash Interface

The embedded 256 Mega-bit Flash in Bulverde is Intel ™ 1.8V StrataFlash® L18 flash memory. The Flash related signals function illustrated in **Fehler! Verweisquelle konnte nicht gefunden werden.** are described as below.

- **A [23:0] –** Address signal. It's a global device signals. Share inputs for all memory die address during read and write operations with SDRAM.

- **D [15:0]** – Data Input / Output signals. Inputs data and commands during write cycles, outputs data during read cycle. Flash data signals are high-Z when chip selection and / or output enable signals are de-asserted.

- **ADV#** – Address Valid. Low true input. It indicates valid address presence on address inputs of the selected Flash die. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge, whichever occurs first. Flash asynchronous mode, addresses are latched on the rising edge ADV#, or are continuously flow-through when ADV# is kept asserted.

- **F1-CE#** – Flash Chip Enable. Low true input. When it becomes low, it enable Flash write / read operation.

- **F-CLK** – Flash Clock. Synchronizes the selected memory die to the system's bus clock in synchronous operations.

- **OE#** – Output Enable. OE# low enables the output driver of the Flash. OE# high places the output drivers of the selected Flash in high-Z.

- **WAIT** – Device wait. WAIT indicates invalid data (asserted) in synchronous read mode. WAIT is active (driven) when F1-CE# is asserted and is high-Z when F1-CE# or OE# is deasserted.

- **WE#** – Write Enable. Low true input. WE# low selects the associated memory for write operation. WE# high deselect the associated memory and data are placed in high-Z state.

6.3 Bulverde GPIO Assignment

The Bulverde processor provides 121 highly-multiplexed general-purpose I/O (GPIO) pins for use in generating and capturing application-specific input and output signals. Each pin may be programmed as an output, an input, or as bi-directional for certain alternate functions (which override the value programmed in the GPIO direction registers). When programmed as an input, a GPIO can also serve as an interrupt source. All GPIO pins are configured as inputs during the assertion of all resets, and they remain inputs until configured otherwise. In addition, select special function GPIO pins serve as bi-directional pins where the I/O direction is driven from the respective unit (overriding the GPIO direction register).

6.3.1 Bulverde GPIO Operation as Application-specific GPIO

Use the GPIO Pin Direction Register GPDR0/1/2/3 to program the GPIO pins as inputs or outputs. For a pin configured as an output, write to the GPIO Pin Output Set Register GPSR0/1/2/3 to set the pin high; write to the GPIO Pin Output Clear Register GPCR0/1/2/3 to clear the pin to a low-level. Writes to GPDRx and GPSRx may take place whether the pin if configured as an input or an output. If a pin is configured as an input, the programmed output state occurs when the pin is reconfigured as an output.

To validate the state of a GPIO pin, read the GPIO Pin Level Register GPLR0/1/2/3. Software may read this register at any time to confirm the state of a pin, even if the pin is configured as an output.

To detect either a rising or a falling edge on each GPIO pin, use the GPIO Rising Edge Detect Enable registers GRER0/1/2/3 and GPIO Falling Edge Detect Enable registers GFER0/1/2/3. Use the GPIO Edge Detect Status Register GEDR0/1/2/3 to read edge state.

GPIO [35], GPIO [15:0], GPIO [4:3] and GPIO [1:0] can generate wake-up events to bring the processor out of sleep and deep-sleep modes, in addition to the keypad, USB and MSL wakeup events.

When the processor enters sleep mode, the contents of the Power Manager Sleep State registers PGSR0/1/2/3 are loaded into the output data registers. If the particular pin is programmed as an output, then the value in the PGSR is driven onto the pin before entering sleep mode. When the Bulverde processor exits sleep mode, these values remain driven until the GPIO pins are reprogrammed by writing to the GPDR, GPSR or GPCR, and setting the GPIO bit in the Power Manager Sleep Status Register PSSR to indicate that the GPIO registers have been re-initialized after sleep mode. This is necessary since the GPIO logic loses power during sleep mode.

6.3.2 Most GPIO pins are multiplexed with alternate-functions of the Bulverde processor. Certain modes within the serial controllers and LCD controller require extra pins. These functions are externally available through specific GPIO pinsBulverde GPIO Operation as E2 Function

E2 Bulverde GPIO assignment listed in **Fehler! Verweisquelle konnte nicht gefunden werden. ~ Fehler! Verweisquelle konnte nicht gefunden werden.**.

Bulverde GPIO		E2 Usage (From GPIO [0] to GPIO [34])		
GPIO	Name	Function Description	Input / Output	From / To
GPIO[0]	GPIO[0]	BP_READY	Input	Neptune
GPIO[1]	GPIO[1]	AP_PCAP_INT	Input	PCAP2
GPIO[2]	GPIO[2]	RESERVED	/	/
GPIO[3]	PWR_SCL	BB_WDOG	Input	Neptune
GPIO[4]	PWR_SDA	AP_WDOG	Output	PCAP2
GPIO[5]	PWR_CAP0	0.1 uF cap tied to both pins	/	/
GPIO[6]	PWR_CAP1		/	/
GPIO[7]	PWR_CAP2	0.1 uF cap tied to both pins	/	/
GPIO[8]	PWR_CAP3		/	/
GPIO[9]	CLK_PIO	MM_13MHz	Output	PCAP2
GPIO[10]	CLK_TOUT	EMU_INT	Input	EMU One-Chip
GPIO[11]	EXT_SYNC0	NC	/	/
GPIO[12]	EXT_SYNC1	CAM_DATA(7)	Input	Digital Camera
GPIO[13]	CLK_EXT	BLUE_HOST_WAKEB	Input	Bluetooth
GPIO[14]	L_VSYNC	BB_SAP_FS	Input	Neptune
GPIO[15]	nCS1	FLIP_INT	Input	Hall-Effect Switch
GPIO[16]	PWM_OUT0	BKLT_PWM	Output	LCD
GPIO[17]	PWM_OUT1	NC	/	/
GPIO[18]	RDY	LCD_ID1	Input	LCD
GPIO[19]	L_CS	NU	/	/
GPIO[20]	GPIO[20]	NU	/	/
GPIO[21]	GPIO[21]	SD_nSDCS3	Output	SDRAM
GPIO[22]	SSPEXTCLK2	BB_SAP_CLK	Input	Neptune / PCAP2 / Blue Tooth
GPIO[23]	SSPSCLK	CAM_CLKIN	Output	Digital Camera
GPIO[24]	SSPSFRM	AP_PCAP_CS	Output	PCAP2
GPIO[25]	SSPTXD	AP_SPI_MOSI	Output	PCAP2
GPIO[26]	SSPRXD	AP_SPI_MISO	Input	PCAP2
GPIO[27]	SSPEXTCLK	CAM_DATA(0)	Input	Digital Camera
GPIO[28]	BITCLK	I2C_RESET	Output	Digital Camera
GPIO[29]	SDATA_IN	AP_SPI_CLK	Output	PCAP2
GPIO[30]	SDATA_OUT	BUL_ICL_TXENB	Input	Neptune
GPIO[31]	SYNC	BUL_ICL_VPOUT	Input	Neptune
GPIO[32]	MMCLK	TFLASH_CLK	Output	Trans-Flash
GPIO[33]	nCS5	NU	/	/
GPIO[34]	FFRXD	BUL_EMU_TXENB	Output	PCAP2

Table 6 – E2 Bulverde GPIO Assignment (GPIO [0] ~ GPIO [34])

Bulverde GPIO		E2 Usage (From GPIO [35] to GPIO [69])		
GPIO	Name	Function Description	Input / Output	From / To
GPIO[35]	FFCTS	BUL_EMU_XRXD	Input	PCAP2
GPIO[36]	SSPSCLK2	BUL_EMU_SE0	Output	PCAP2
GPIO[37]	SSPSFRM2	BT_RESETB	Output	Blue Tooth
GPIO[38]	SSPTXD2	BB_SAP_TX	Output	Neptune / PCAP2 / Blue Tooth
GPIO[39]	FFTXD	BUL_EMU_VPOUT	Output	EMU One-Chip
GPIO[40]	SSPRXD2	BUL_EMU_VPIN	Input	EMU One-Chip
GPIO[41]	FFRTS	BP_FLASH_MODE_EN	Output	Neptune switch for OPT1 & OPT2
GPIO[42]	BTRXD	BT_RXD	Input	Blue Tooth
GPIO[43]	BTTXD	BT_TXD	Output	Blue Tooth
GPIO[44]	BTCTS	BT_RTS	Input	Blue Tooth
GPIO[45]	BTRTS	BT_CTS	Output	Blue Tooth
GPIO[46]	ICP_RXD	STUART_RX	/	/
GPIO[47]	ICP_TXD	STUART_TX	/	/
GPIO[48]	BB_OB_DAT1	CAM_DATA(5)	Input	Digital Camera
GPIO[49]	nPWE	NC	/	/
GPIO[50]	BB_OB_DAT2	CAM_EN	Output	Digital Camera
GPIO[51]	BB_OB_DAT3	CAM_DATA(2)	Input	Digital Camera
GPIO[52]	BB_OB_CLK	AP_SAP_CLK	Input	PCAP2
GPIO[53]	BB_OB_STB	BUL_EMU_VMIN	Input	EMU One-Chip
GPIO[54]	BB_OB_WAIT	CAM_CLKOUT	Output	Digital Camera
GPIO[55]	BB_IB_DAT1	SYS_RESTART	Output	PCAP2
GPIO[56]	BB_IB_DAT2	BUL_ICL_SE0	Input	Neptune
GPIO[57]	BB_IB_DAT3	BLUE_WAKEB	Output	Bluetooth
GPIO[58]	L_DD0	L_DD(0) B0	Output	LCD (B0)
GPIO[59]	L_DD1	L_DD(1) B1	Output	LCD (B1)
GPIO[60]	L_DD2	L_DD(2) B2	Output	LCD (B2)
GPIO[61]	L_DD3	L_DD(3) B3	Output	LCD (B3)
GPIO[62]	L_DD4	L_DD(4) B4	Output	LCD (B4)
GPIO[63]]	L_DD5	L_DD(5) B5	Output	LCD (B5)
GPIO[64]	L_DD6	L_DD(6) G0	Output	LCD (G0)
GPIO[65]	L_DD7	L_DD(7) G1	Output	LCD (G1)
GPIO[66]	L_DD8	L_DD(8) G2	Output	LCD (G2)
GPIO[67]	L_DD9	L_DD(9) G3	Output	LCD (G3)
GPIO[68]	L_DD10	L_DD(10) G4	Output	LCD (G4)
GPIO[69]	L_DD11	L_DD(11) G5	Output	LCD (G5)

Table 7 – E2 Bulverde GPIO Assignment (GPIO [35] ~ GPIO [69

Bulverde GPIO		E2 Usage (From GPIO[70] to GPIO[104])		
GPIO	Name	Function Description	Input / Output	From / To
GPIO[70]	L_DD12	L_DD(12) R0	Output	LCD (R0)
GPIO[71]	L_DD13	L_DD(13) R1	Output	LCD (R1)
GPIO[72]	L_DD14	L_DD(14) R2	Output	LCD (R2)
GPIO[73]	L_DD15	L_DD(15) R3	Output	LCD (R3)
GPIO[74]	L_FCLK_RD	LCD_VSYNC	Output	LCD
GPIO[75]	L_LCLK_A0	LCD_HSYNC	Output	LCD
GPIO[76]	L_PCLK_WR	LCD_MCLK	Output	LCD
GPIO[77]	L_BIAS	LCD_OE	Output	LCD
GPIO[78]	nCS2	LCD_SD	Output	LCD
GPIO[79]	nCS3	LCD_CM	Output	LCD
GPIO[80]	nCS4	LCD_ID0	Input	LCD
GPIO[81]	BB_OB_DAT0	AP_SAP_TX	Output	PCAP2
GPIO[82]	BB_IB_DAT0	BB_SAP_RX	Output	Neptune
GPIO[83]	BB_IB_CLK	AP_SAP_FS	Input	PCAP2
GPIO[84]	BB_IB_STB	CAM_VSYNC	Output	Digital Camera
GPIO[85]	BB_IB_WAIT	CAM_HSYNC	Output	Digital Camera
GPIO[86]	L_DD16	L_DD(16) R4	Output	LCD (R4)
GPIO[87]	L_DD17	L_DD(17) R5	Output	LCD (R5)
GPIO[88]	USBHPWR0	BB_SAP_RX	Input	Neptune / PCAP2 / Blue Tooth
GPIO[89]	USBHPEN0	NU	/	/
GPIO[90]	URST	BUL_ICL_VPIN	Output	Neptune
GPIO[91]	UCLK	BUL_ICL_XRXD	Output	Neptune
GPIO[92]	MMDAT0	MMC_D0	Input / Output	Trans-Flash
GPIO[93]	KP_DKIN0	CAM_DATA(6)	Input	Digital Camera
GPIO[94]	KP_DKIN1	NC	/	/
GPIO[95]	KP_DKIN2	CAM_DATA(4)	Input	Digital Camera
GPIO[96]	KP_DKIN3	AP_READY	Output	Neptune
GPIO[97]	KP_DKIN4	KBR3	Input	Keypad
GPIO[98]	KP_DKIN5	KBR4	Input	Keypad
GPIO[99]	KP_DKIN6	USB_READY	Output	EMU One-Chip
GPIO[100]	KP_MKIN0	KBR0	Input	Keypad
GPIO[101]	KP_MKIN1	KBR1	Input	Keypad
GPIO[102]	KP_MKIN2	KBR2	Input	Keypad
GPIO[103]	KP_MKOUT0	KBC0	Output	Keypad
GPIO[104]	KP_MKOUT1	KBC1	Output	Keypad

Table 8 – E2 Bulverde GPIO Assignment (GPIO [70] ~ GPIO [104])

Bulverde GPIO		E2 Usage (From GPIO[105] to GPIO[120])		
GPIO	Name	Function Description	Input / Output	From / To
GPIO[105]	KP_MKOUT2	KBC2	Output	Keypad
GPIO[106]	KP_MKOUT3	KBC3	Output	Keypad
GPIO[107]	KP_MKOUT4	KBC4	Output	Keypad
GPIO[108]	KP_MKOUT5	KBC5	Output	Keypad
GPIO[109]	MMDAT1	MMC_D1	Input / Output	Trans-Flash
GPIO[110]	MMDAT2	MMC_D2	Input / Output	Trans-Flash
GPIO[111]	MMDAT3	MMC_D3	Input / Output	Trans-Flash
GPIO[112]	MMCMD	MMC_CMD	Input	Trans-Flash
GPIO[113]	AC97_nRESET	BUL_ICL_VMIN	Output	Neptune
GPIO[114]	UVS0	CAM_DATA(1)	Input	Digital Camera
GPIO[115]	nUVS1	CAM_DATA(3)	Input	Digital Camera
GPIO[116]	nUVS2	BP_RESETB	Output	Neptune
GPIO[117]	SCL	I2C_SCL	Output	Digital Camera
GPIO[118]	SDA	I2C_SDA	Input / Output	Digital Camera
GPIO[119]	USBHPWR[1]	RESERVED	/	/
GPIO[120]	USBHPEN[1]	RESERVED	/	/

Table 9 – E2 Bulverde GPIO Assignment (GPIO [105] ~ GPIO [120])

6.4 E2 Keypad Design

6.4.1 Keypad Interface

There are total 27 keypads on E2 phone design. One is connected with PCAP2 On pin as power up control key and another 26 keypads connected with Bulverde keypad control module. The pin definitions on E2 phone housing shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

There are two types of keypad selected in E2 phone design. One is the single press button that used for CAMERA, VA / VR, POWER_KEY, HOME, Music keys. Another one is a five-position navigation switch.

Table 10 – E2 Matrix Scan Key Assignment

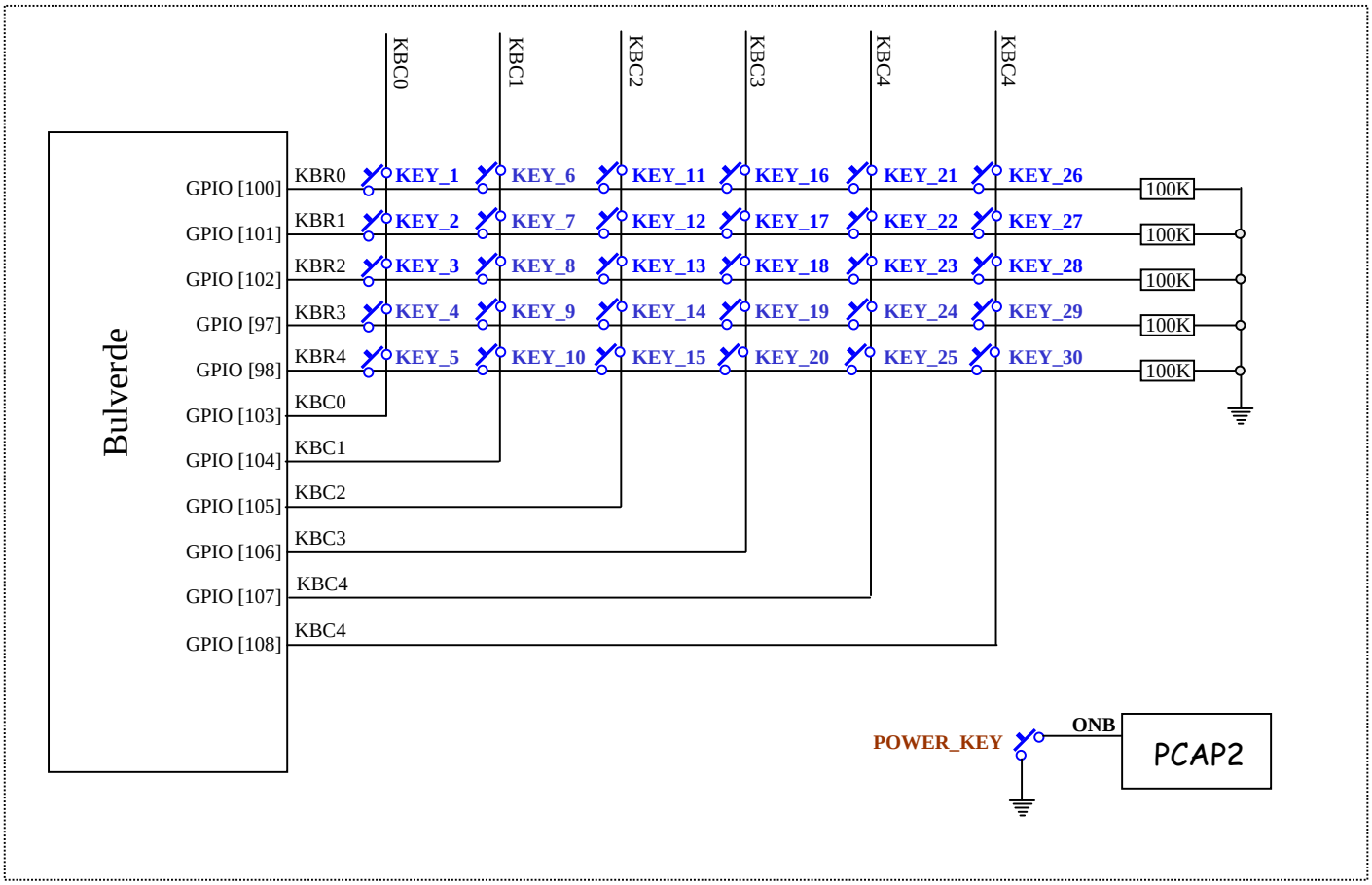


Figure 23 – E2 Keypad Interface Block Diagram

For navigation 5-way switch selected by E2 is of 5 dedicated single key. When press at one direction, only one switch is closed.

Column / Row		Key Pad	Row (Input)				
			KBR0	KBR1	KBR2	KBR3	KBR4
			GPIO[100]	GPIO[101]	GPIO[102]	GPIO[97]	GPIO[98]
Column (Output)	KBC0	GPIO [103]					
	KBC1	GPIO [104]	NAV_RIGHT	NAV_DOWN	NAV_SELECT	NAV_UP	NAV_LEFT
	KBC2	GPIO [105]	JOG_DIAL_DOWN	CAMERA	VA	HOME	JOG_DIAL_UP
	KBC3	GPIO [106]					
	KBC4	GPIO [107]					
	KBC5	GPIO [108]			JOG_DIAL_MID		

Table 11 – E2 Bulverde GPIO Assignment of Keypad Controller

6.5 E2 LCD Module Interface

E2 LCD Display Module is a color Active Matrix Liquid Crystal Display (AMLCD) module of glass construction with black pixels on a white background. The display consists of 240 (x RGB Stripe) x 320 pixels with 262K colors.

This display module is constructed of:

- The Liquid Crystal Display Glass consisting of the top glass plate, top and bottom polarizers and compensation films, color filter, liquid crystal, internal transflector, a poly-Si backplane containing the pixel transistors, and row and column driving circuitry integrated onto the glass.
- Auxiliary Backlighting System consisting of white LEDs, lightguide, and LED driving circuitry
- Mechanical support system with top and bottom metal frame.
- FPC with LCD controller and other necessary passive components.

The LCD module electrical block diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

The timing diagram of LCD horizontal reading / writing shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**. And Vertical reading / writing timing shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

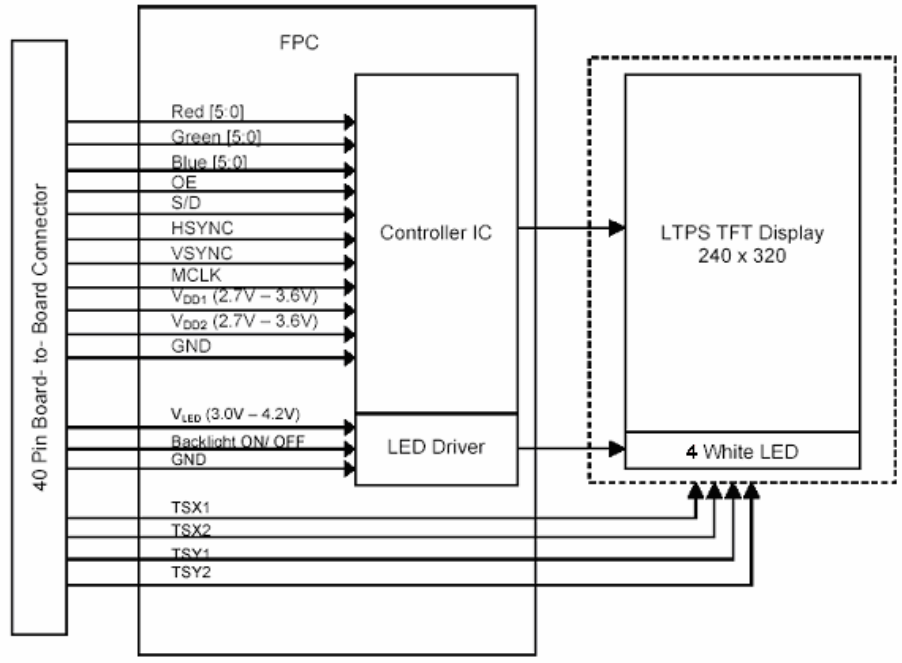


Figure 24 – E2 LCD Module Electrical Block Diagram

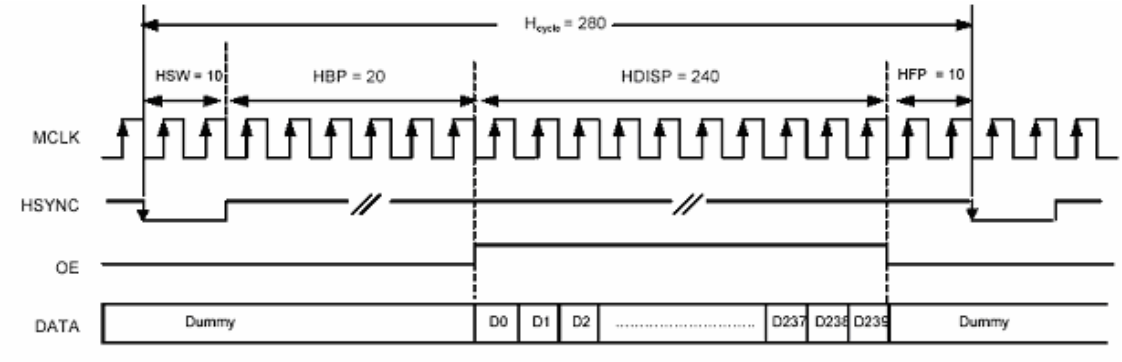


Figure 25 – E2 LCD Module Horizontal Reading / Writing Timing Diagram

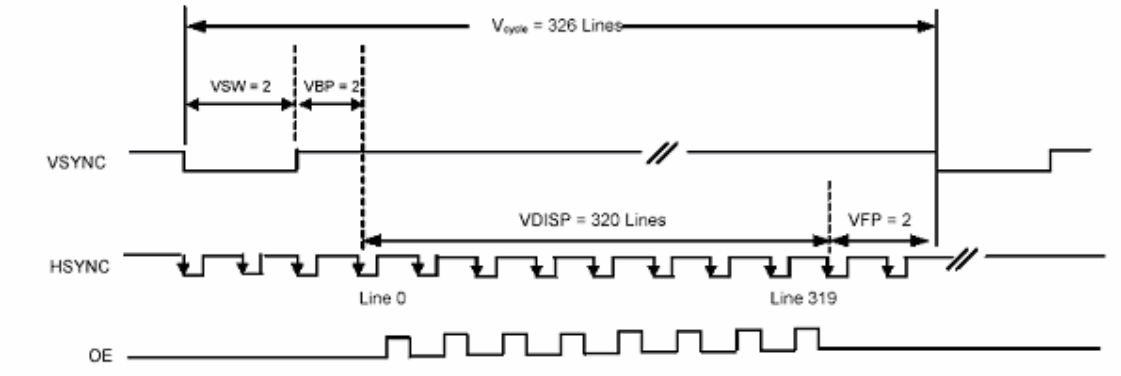


Figure 26 – E2 LCD Module Vertical Reading / Writing Timing Diagram

The S/D pin of LCD module is used to turn on or off the display. The power up and power down timing diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.** & **Fehler! Verweisquelle konnte nicht gefunden werden.**. And the corresponding timing parameters listed in **Fehler! Verweisquelle konnte nicht gefunden werden.** and **Fehler! Verweisquelle konnte nicht gefunden werden.**.

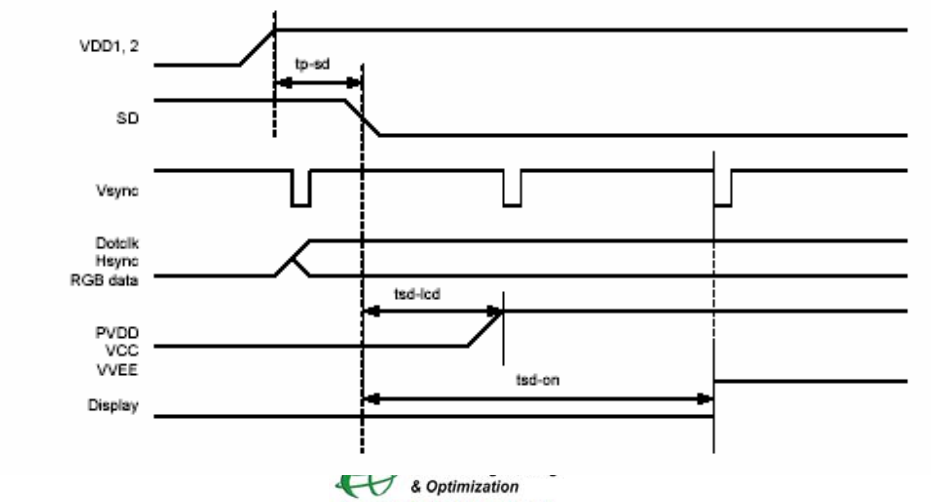


Figure 27 – E2 LCD Power Up Timing Diagram

Characteristics	Symbol	Minimum	Typical	Maximum	Units
VDD-On to rising edge of S/D	tp-sd	1	-	-	usec
Rising edge of S/D to LCD power on	tsd-lcd	-	-	128	msec
Rising edge of S/D to display start		-	-	185	msec
(MCLK = 5.44MHz)		-	-	11	frame

Table 12 – AE2 LCD Power up Timing Figures

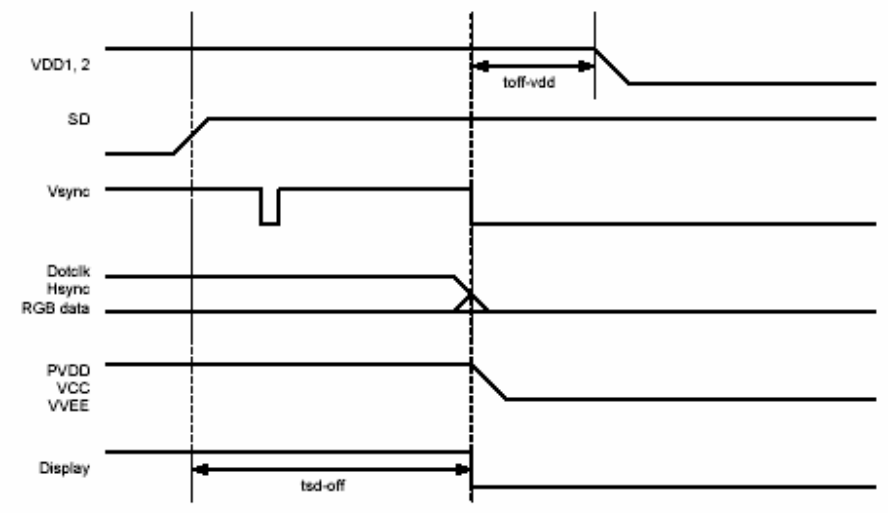


Figure 28 – E2 LCD Power Down Timing Diagram

Characteristics	Symbol	Minimum	Typical	Maximum	Units
Falling edge of S/D to display off (MCLK = 5.44MHz)	tsd-off	16.7 1	- -	33.4 2	msec frame
Falling edge of Vsync to VDD off	tsd-lcd	-	-	-	usec

6.5.1.1.1.1

Table 13 – E2 LCD Power Down Timing Figures

The connections between Bulverde and LCD module diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

Bulverde GPIO settings for LCD module to work shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.The alternative function for those GPIOs as LCD function were marked with RED.

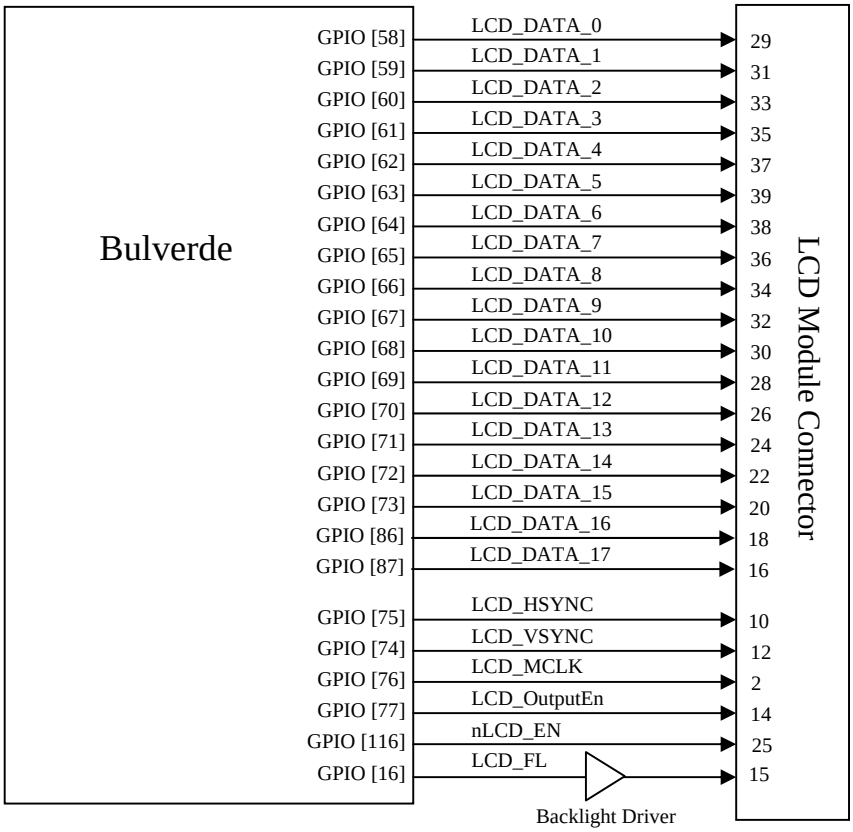


Figure 29 – E2 Connection Block Diagram Between Bulverde and LCD Module

An external DC-DC boost converter drives E2 LCD front-light LED. The control pin for this converter comes from Bulverde GPIO with PWM functionality. GPIO [16] of Bulverde is selected as LCD front-light LED brightness control.

Bulverde has 4 independent PWM outputs from PWM-OUT [0] to PWM-OUT [3] – E2 GPIO [16] PWM is PWM-OUT [0]. Each PWM outputs, once programmed, output a specified waveform until the value in any associated register is altered. The PWMs use three registers to configure the output of each PWM <x> signal: PWMCRx, PWMDCRx and PWMPCRx.

6.6 Bulverde Peripherals Interface

Several peripherals are connected with Bulverde to form the application system. This includes Blue-Tooth and Digital Camera. Bulverde Bluetooth UART modules control Bluetooth peripherals. The connection block diagram shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

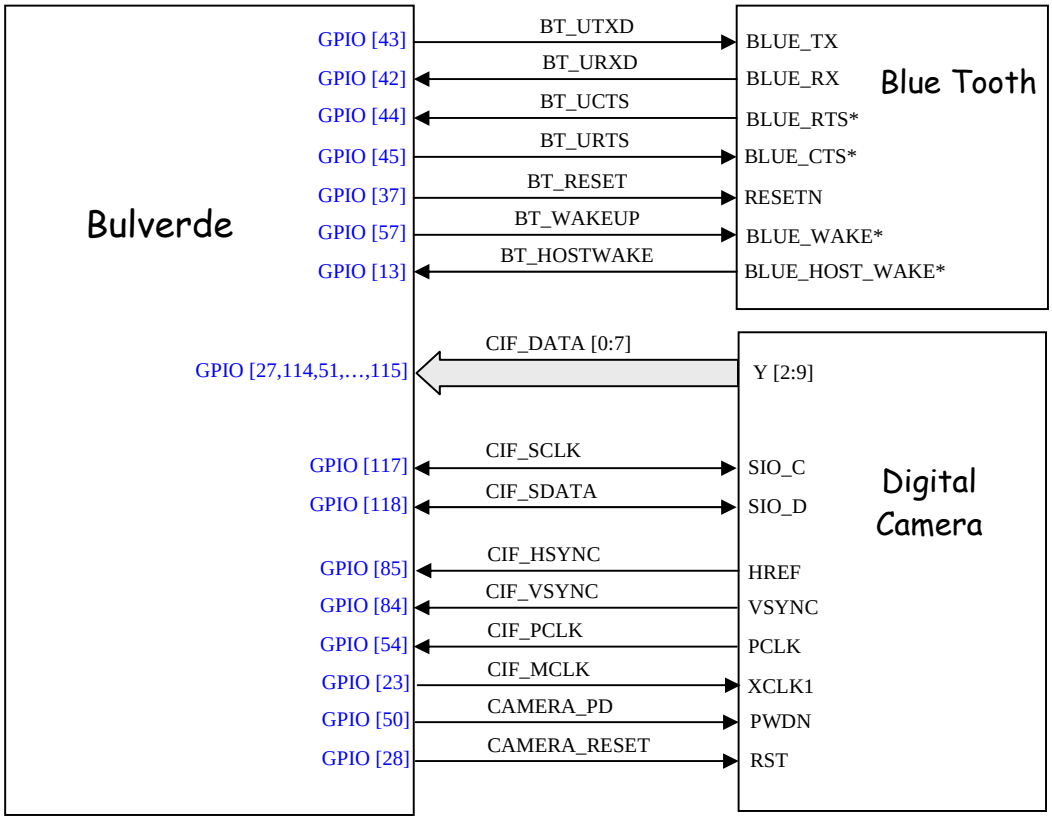


Figure 30 – E2 Bulverde Peripherals Connections Block Diagram

6.6.1 Blue Tooth Module

E2 uses a blue-tooth module for its Blue-Tooth application. The core chip set of the Blue-Tooth Module is **BROADCOM ™** BCM2045. The Broadcom BCM2045 is a monolithic single-chip, Bluetooth 1.2 compliant, stand-along baseband processor with an integrated 2.4GHz transceiver. It eliminates the need for external Flash memories and active components by integrating critical external components into the device, thus minimizing the footprint and system cost of implementing a Bluetooth solution.

The BCM2035 has the following features:

- Bluetooth Specification version 1.2 compliant
- ROM based internal memory with patch RAM
- Automatic on-chip calibration optimizes performance and eliminates tuning during manufacturing
- Programmable output power control meets Class 2 or Class 3 requirements
- Fractional-N synthesizer supports frequency references from 12MHz to 40MHz
- Automatic frequency detection for standard crystal and TCXO values
- Standard HCI USB and UART interface

The Functional Block Diagram shows in Figure 32.

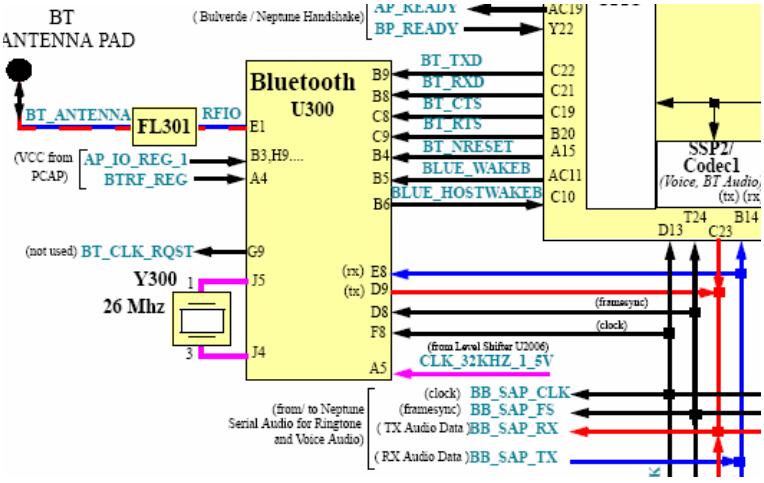


Figure 31 - BCM2045 Functional Block Diagram

6.6.2 Digital Camera

The digital camera sensor used in E2 phone is Micron's MT9D111, which is a 1/3 Inch 1.3 Megapixel Digital Image Sensor.

Micron™ Imaging MT9D111 is a 1/3-inch 1.3-megapixel CMOS image sensor with an integrated advanced camera system. The camera system features a microcontroller (MCU) and a sophisticated image flow processor (IFP) with a real-time JPEG encoder. It also includes a programmable general purpose I/O module (GPIO), which can be used to control external auto focus, optical zoom, or mechanical shutter.

The microcontroller manages all components of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 1280x1024 pixels, programmable timing and control circuitry including a PLL and external flash support, analog signal chain with automatic offset correction and programmable gain, and two 10-bit A/D converters (ADC). The entire system-on-achip (SOC) has ultra-low power requirements and superior low-light performance that is particularly suitable for mobile applications.

6.6.2.1 Micron™ 1.3-MegaPixel Module Features

The key features of MT9D111 DigitalClarity™ listed as below:

- DigitalClarity™ CMOS Imaging Technolog
- Superior low-light performance
- Ultra-low power, low cost
- Internal master clock generated by on-chip phase-locked loop oscillator
- Electronic rolling shutter (ERS), progressive scan
- Automatic image correction and enhancement, including lens shading correction
- Arbitrary image decimation with anti-aliasing
- Integrated read-time JPEG encoder
- Integrated microcontroller for flexibility
- Two-wire serial interface providing access to registers and microcontroller memory (I2C- Bus)
- Selectable output format: ITU-R BT.601 (YCbCr), 565RGB, 555RGB, 444RGB, JPEG 4:2:2, JPEG 4:2:0, and raw 10-bit
- Output FIFO for data rate equalization
- Programmable I/O slew rate
- Xenon and LED flash support with fast exposure adaptation
- Flexible support for extenal auto focus, optical zoom, and mechanical shutter

6.6.2.2 MT9D111 Functional Description

Fehler! Verweisquelle konnte nicht gefunden werden. shows the functional block diagram of the MT9D111 image sensor.

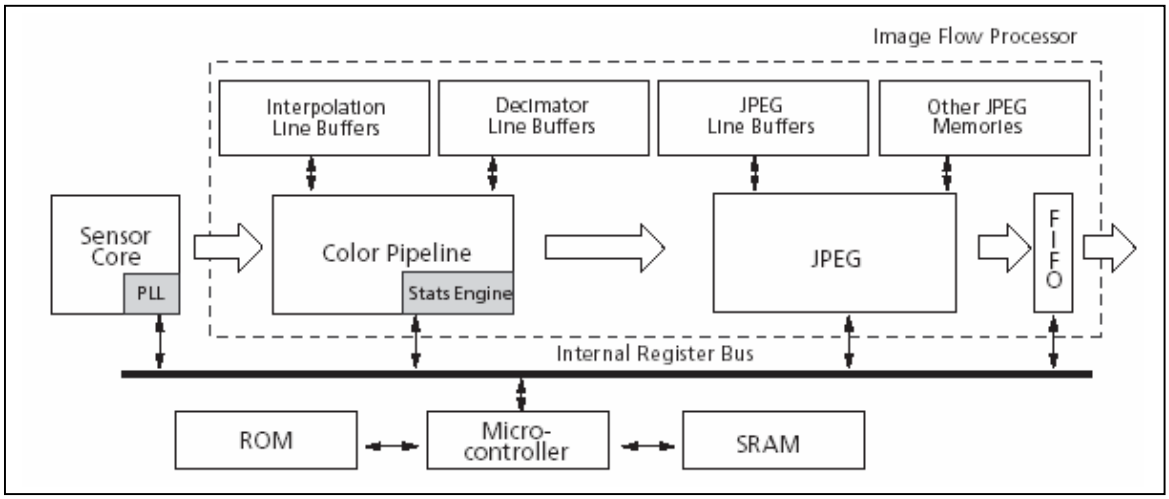


Figure 32 - MT9D111 Functional Block Diagram

The MT9D111 image sensor includes the following function block.

- Image sensor Core
- Color Pipeline
- JPEG Encoder and FIFO
- JPEG Line Buffers
- JPEG Memories
- Interface FIFO

6.6.2.3 E2 Digital Camera Hardware Architecture

E2 camera hardware can be divided into four parts: controller, camera module, flash and power supplier. **Fehler! Verweisquelle konnte nicht gefunden werden.** shows their relationship.

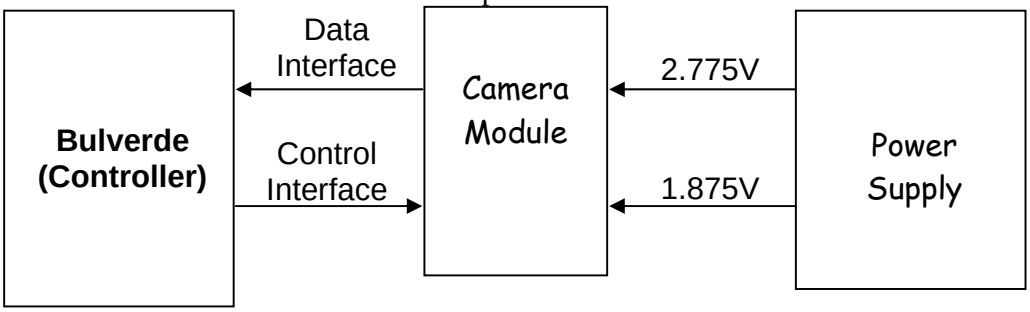


Figure 33 – E2 Digital Camera System Architecture Block Diagram

The functions for each signal shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

The GPIO assignment of Bulverde for Digital camera operation shows in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

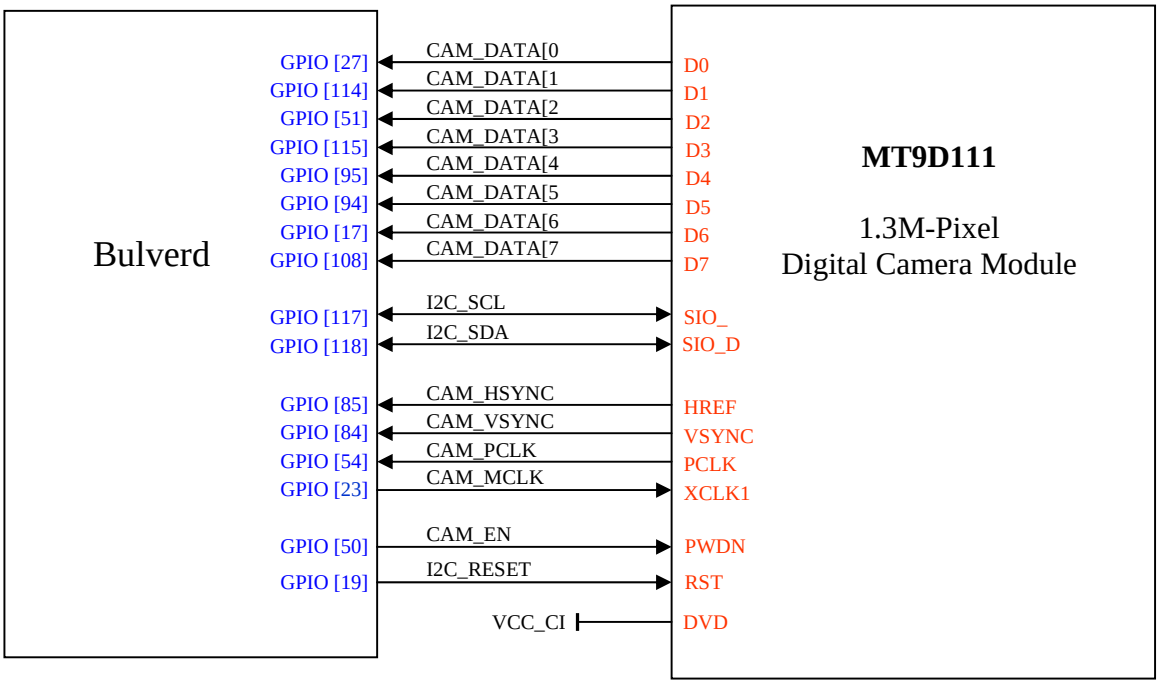


Figure 34 – E2 Digital Camera Detailed Connection With Bulverde

Signal	Bulverde GPIO	Camera Signal	Function Description
CAM_DATA [0]	GPIO [27]	D0	Data Line from Camera to Bulverde
CAM_DATA [1]	GPIO [114]	D1	Data Line from Camera to Bulverde
CAM_DATA [2]	GPIO [51]	D2	Data Line from Camera to Bulverde
CAM_DATA [3]	GPIO [115]	D3	Data Line from Camera to Bulverde
CAM_DATA [4]	GPIO [95]	D4	Data Line from Camera to Bulverde
CAM_DATA [5]	GPIO [48]	D5	Data Line from Camera to Bulverde
CAM_DATA [6]	GPIO [93]	D6	Data Line from Camera to Bulverde
CAM_DATA [7]	GPIO [12]	D7	Data Line from Camera to Bulverde
I2C_SCL	GPIO [117]	SIO_C	I2C Control Clock signal
I2C_SDA	GPIO [118]	SIO_D	I2C Control Data Signal
CAM_HSYNC	GPIO [85]	HREF	Line Signal from Camera to Bulverde
CAM_VSYNC	GPIO [84]	VSYNC	Frame signal from Camera to Bulverde
CAM_PCLK	GPIO [54]	PCLK	Pixel clock from Camera to Bulverde
CAM_MCLK	GPIO [23]	XCLK1	Programmable clock to Camera
CAM_EN	GPIO [50]	PWDN	Camera Power Down Signal – Active High
I2C_RESET	GPIO [19]	RST	Camera Reset Signal – Active High

Table 14 – E2 Digital Camera Signal Function Description

6.6.3 SD Card

E2 is a high tier multimedia phone, a removable multimedia file storage media is required. Flash is the ideal storage medium for portable, battery powered devices. It features low power consumption and is non-volatile, requiring no power to maintain the stored data. It also has a wide operating range for temperature, shock and vibration.

SD-Flash is well suited to meet the needs of small, low power, electronic devices. With a form factor as small as 24mm by 32mm and 2mm thickness, SD-Flash can be used in a wide variety of portable devices like mobile phones, digital audio players, car navigation devices, and voice recorders.

There are 9-pin on a SD-Flash card as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**. Each pin as defined in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

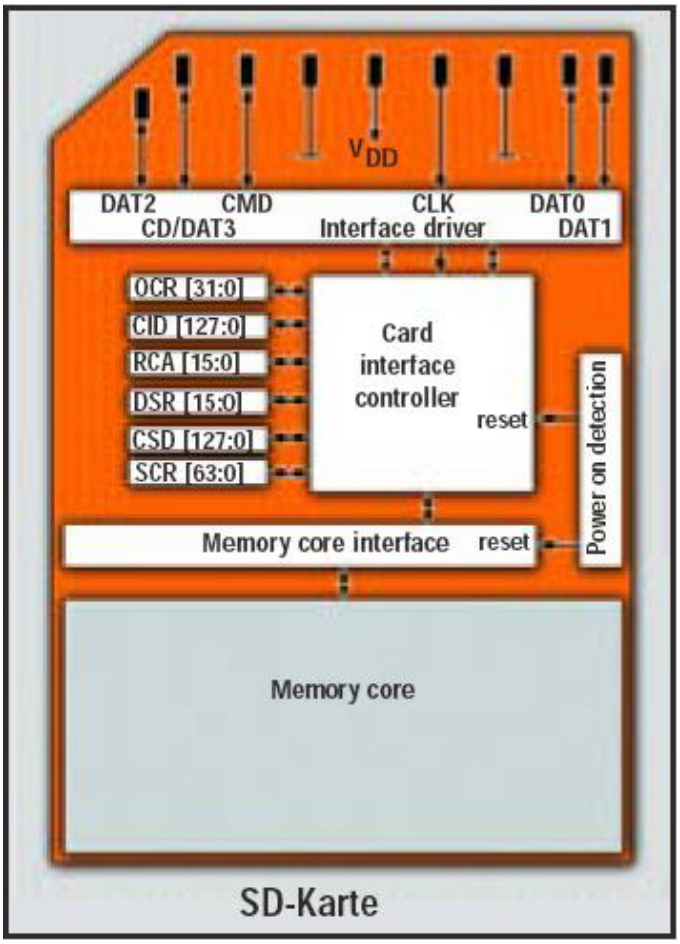


Figure 35 - SD-Flash Card Outline Diagram

	SD Mode			SPI Mode		
Pin #	Name	Type	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [Bit 2]	RSV		
2	CD/DAT3	I/O/PP3	Card Detect / Data Line [Bit 3]	CS	I	Chip Select (Negative True)
3	CMD	PP	Command / Response	DI	I	Data In
4	VSS1	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
5	VDD	S	Supply Voltage Ground	VDD	S	Supply Voltage
6	CLK	I	Clock	SCLK	I	Clock
7	VSS1	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
8	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
9	DAT1	I/O/PP	Data Line [Bit 1]	RSV		

Table 15 - SD-Flash Card Pin Definition

SD-Flash can be accessed with MMC and SPI mode interface. 37 illustrates the architecture with a SD-Flash card and it's MMC / SPI interface with application processor.

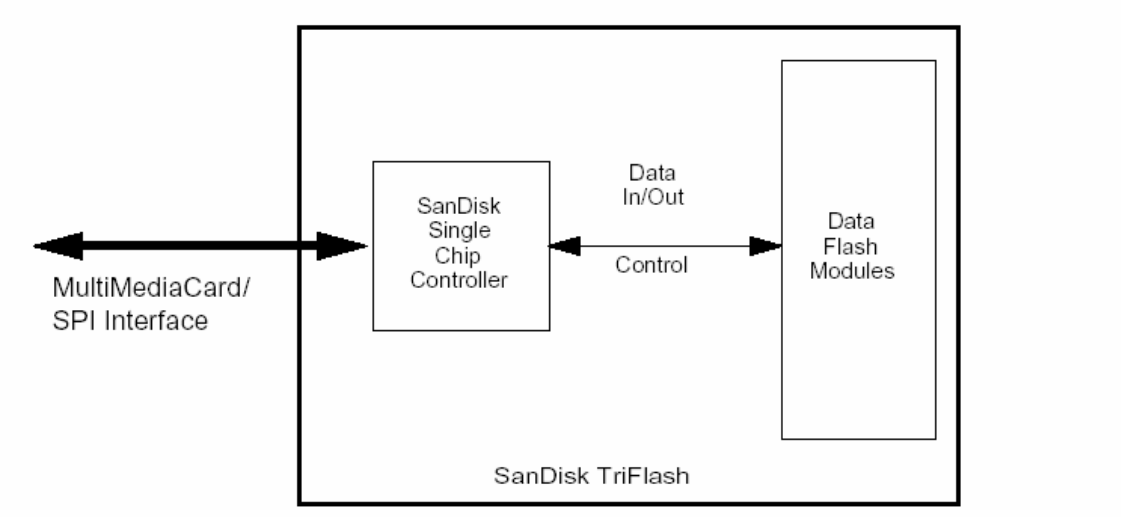


Figure 36 - SD-Flash With MMC and SPI Interface Block Diagram

SD-Flash Using MMC Bus	SD-Flash Using SPI Bus
Three-Wire serial data bus (Clock, Command, Data)	Three-wire serial data bus (Clock, Data-In, Data-Out) and device specific CS signal (hardwired device selection)
Up to 64K devices addressable by the bus protocol	Device selection via a hardware CS signal
Error-Protected data transfer	Optional. A non-protected data transfer mode is available
Sequential and single / multiple block oriented data transfer	Single or multiple block oriented data transfer

Table 16 - Tri-Flash Card MMC Bus and SPI Bus Comparison

E2 design connect Bulverde with SD-Flash as SD / MMC bus for data and command exchange. **Fehler! Verweisquelle konnte nicht gefunden werden.** illustrated the connection between Bulverde and Tri-Flash.

The power supply to SD-Flash is provided by PCAP2 VAUX3 (VAP_MMC), which is default OFF after power up. VAP_MMC can be switched ON through secondary SPI connected with Bulverde.

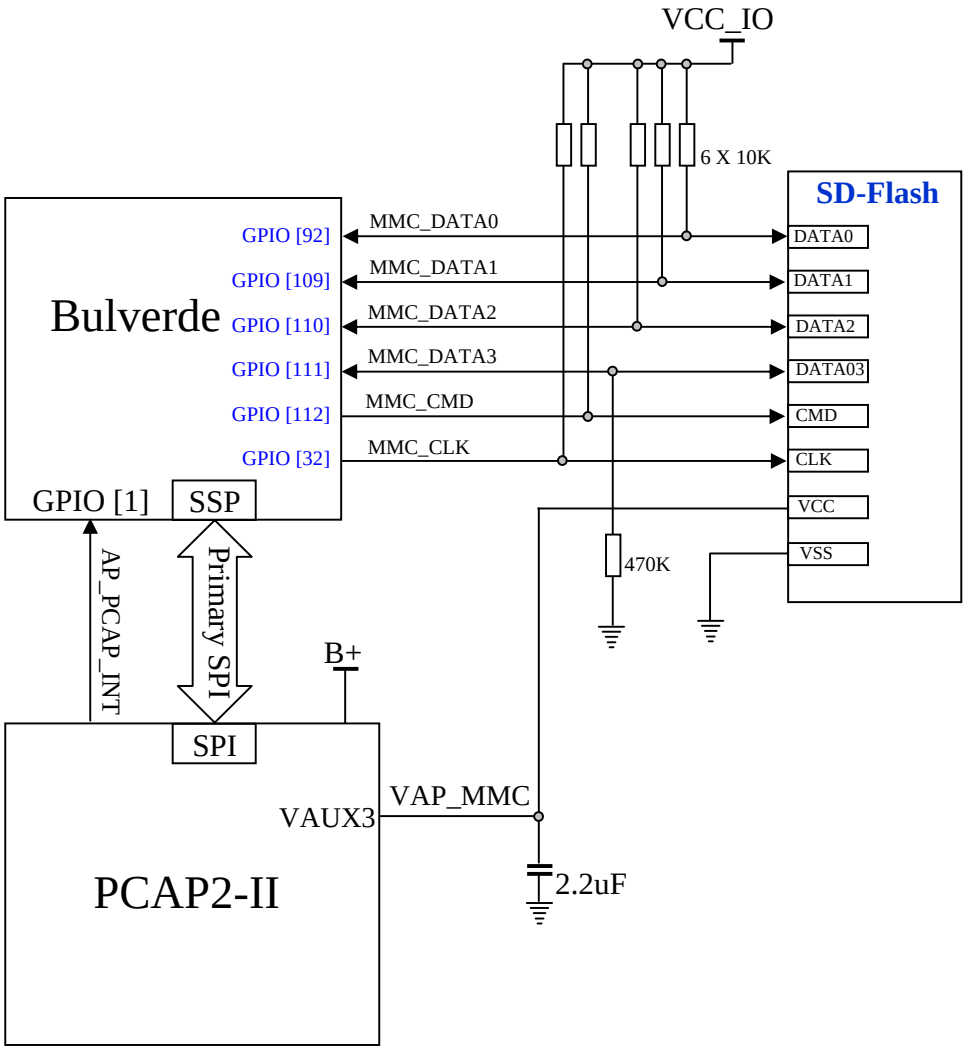


Figure 37 – E2 SD-Flash Card Control Block Diagram

E2 locates the Trans-Flash card holder under battery, doesn't need to support hot-plug. MMC_DATA3 is used as card detection when power up. If MMC_DATA3 (GPIO[111]) is logic High, the card is inserted in the holder, otherwise, no card existed.

6.6.4 FM Radio Design

E2 phone design uses Philips TEA5764 FM radio chipset.

The TEA5764 is a single chip electronically tuned FM stereo radio with RDS/RBDS demodulator and RDS/RBDS decoder for low voltage application with fully integrated IF selectivity and demodulation.
The radio is completely adjustment free and does only require a minimum of small and low cost external components.
The radio can tune the European-, US- and Japan FM bands. The Radio does not meet all of the requirements from EN55020 a trade off was done to make possible the previously stated features. The IC is available in HVQFN package and in Chip Scale Package.

6.6.4.1 TEA5764 Features and Description

The function block diagram of TEA5764 illustrated in Figure 39.

The key features of TEA5764 lists as below:

- Chip Scale Package
- High sensitivity due to integrated low noise RF input amplifier
- FM mixer for conversion of the US/Europe (87.5MHz to 108MHz) and Japanese FM band (76 MHz to 90MHz) to IF Preset tuning to receive Japanese TV audio up to 108MHz, raster 100kHz
- RF Automatic Gain Control circuit
- LC tuner oscillator operating with low cost fixed chip inductors
- Fully integrated FM IF selectivity
- Fully integrated FM demodulator, no external discriminator
- Crystal reference frequency oscillator. The oscillator operates with a 32768Hz clock crystal.
- PLL synthesizer tuning system
- Signal depending mono/stereo blend (SNC, stereo noise canceling)
- Soft mute, SNC can be switched off via the bus
- Adjustment free stereo decoder
- Autonomous search tuning function
- Stand-by mode
- Fully integrated RDS/RBDS demodulator in accordance with EN50067
- RDS/RBDS decoder with memory for two RDS data blocks provides block synchronization and error correction. Block data and status information are available via the I2C-bus.
- Audio Pause Detector
- Interrupt flag

6.6.4.2 FM Radio Connection Block Diagram

The FM radio and audio related system connection block diagram shows in Figure 39.

FM radio audio outputs are input to PCAP2 **PGA_INL** and **PGA_INR**.

The control to TEA5764 is through **I2C** interface of Bulverde.

The interrupt signal didn't used by Bulverde processor in E2 design.

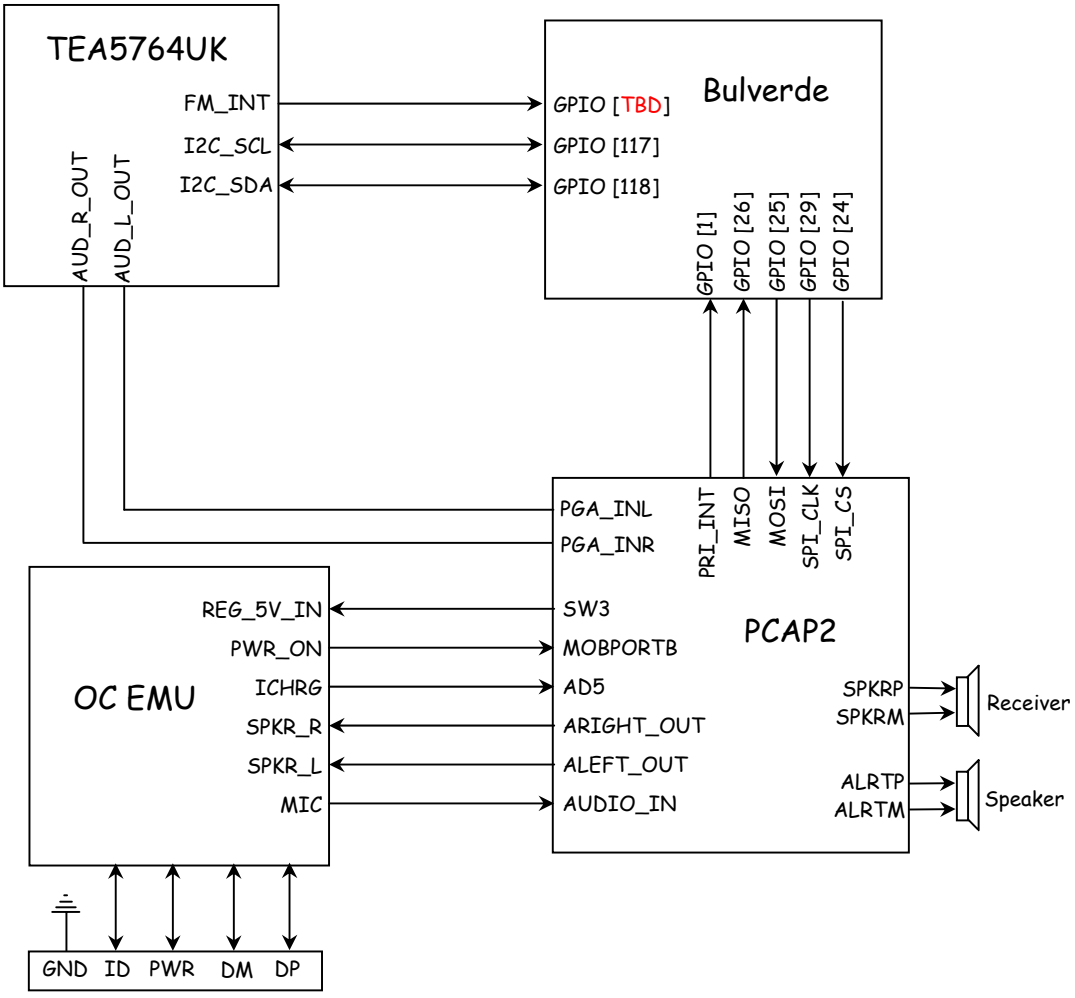


Figure 38 – E2 FM Radio and Audio Related Signal Block Diagram

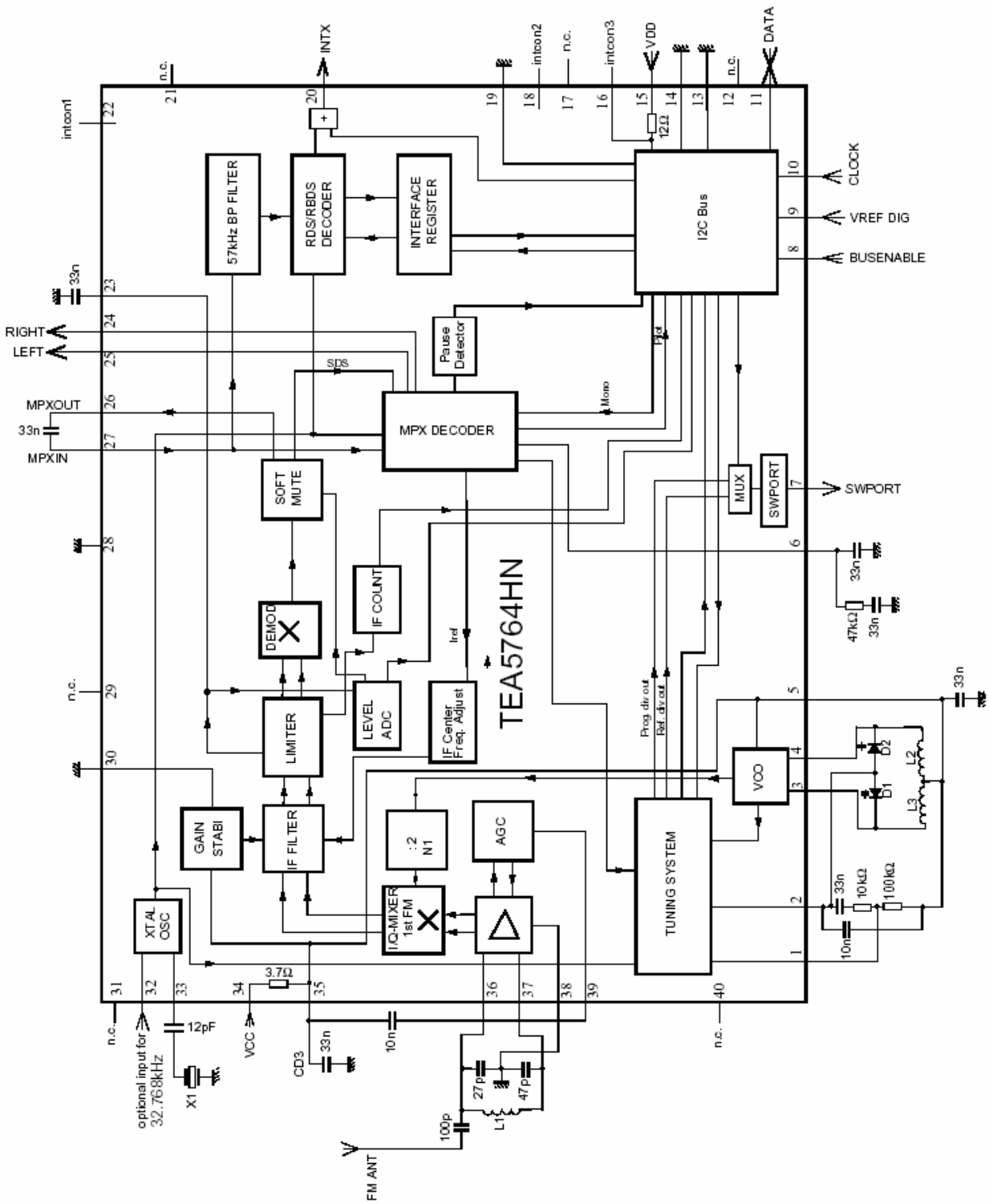


Figure 39 - Phillips TEA5764 Function Block Diagram

7 E2 System Architecture Description

7.1 E2 System architecture block diagram

E2 Quad-band system architecture block diagram shows in Figure 41.

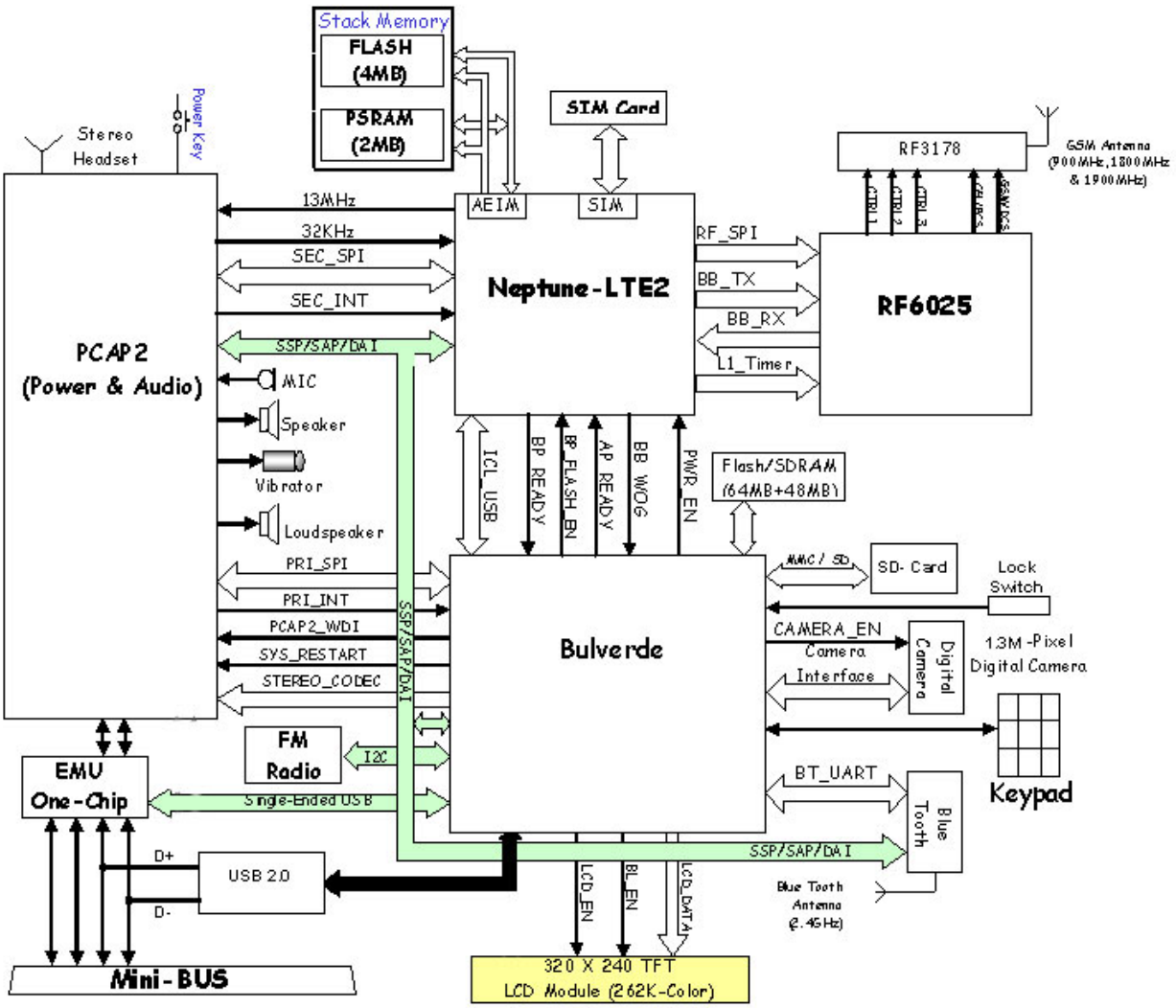


Figure 40 – E2 Quad-band System architecture block diagram

7.2 E2 Interconnection Link between Neptune-LTE & Bulverde (ICL)

A block diagram **Fehler! Verweisquelle konnte nicht gefunden werden.** shows all the inter-connection between Neptune-LTE, Bulverde, PCAP2, EMU One-Chip and USB 2.0 IC. In E2 design, these inter-connection signals are classified as ICL signals.

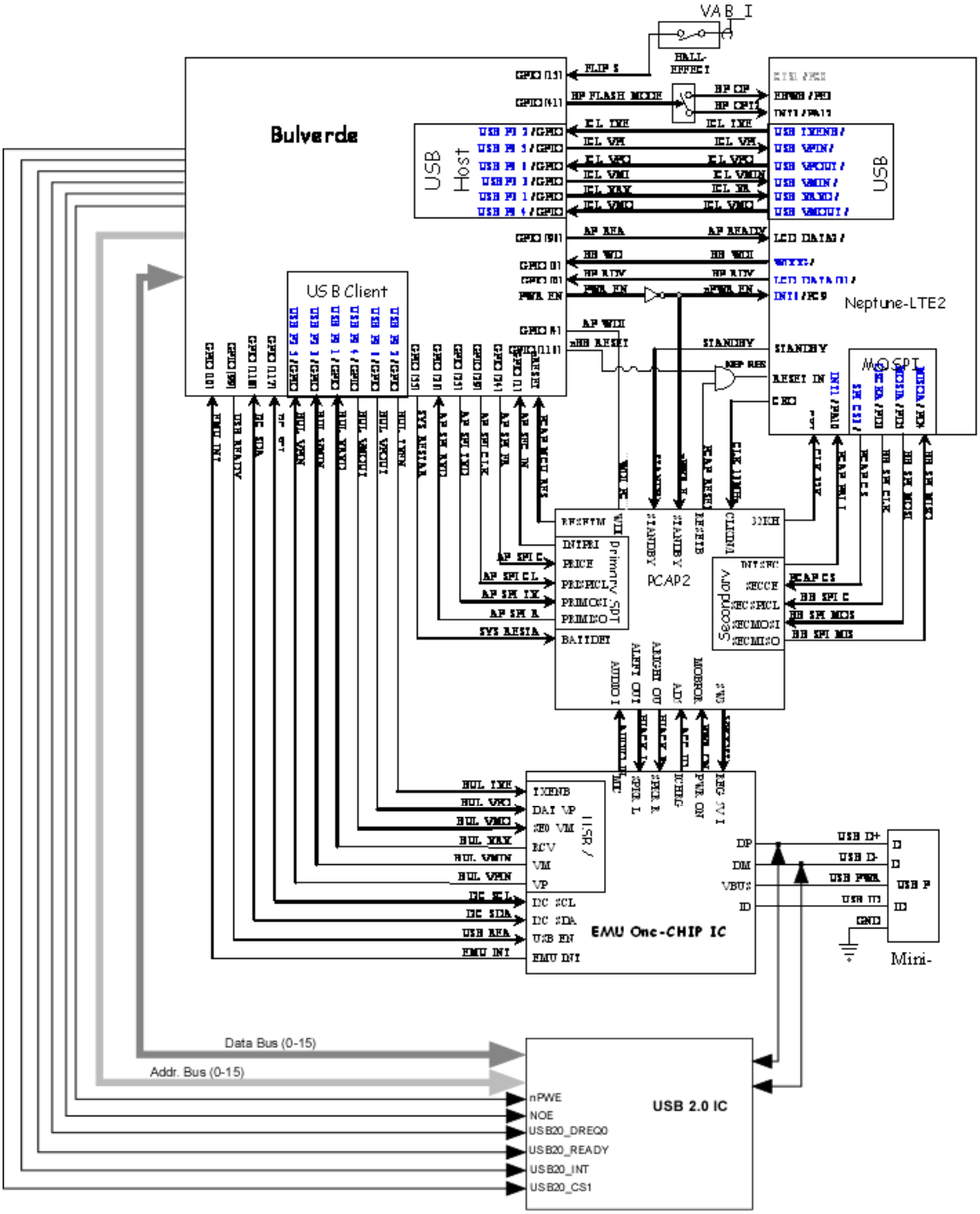


Figure 41 – E2 Interconnection Link between Neptune,Bulverde & EMU

All the ICL signals function descriptions are summarized in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

	Signal Direction		
Signal	**Output / GPIO**	**Input / GPIO**	**Function Description**
FLIP_SW	Hall-Effect Switch	Bulverde	Hall-effect switch - Logic Low when Flip is closed
ICL_TXENB	Neptune / PD10	Bulverde / GPIO[30]	USB transmit enable signal
ICL_VPIN	Bulverde / GPIO[90]	Neptune / PD11	USB positive input signal
ICL_VPOUT	Neptune / PD14	Bulverde / GPIO[31]	USB positive output signal
ICL_VMIN	Bulverde / GPIO[113]	Neptune / PD12	USB negative input signal
ICL_XRXD	Bulverde / GPIO[91]	Neptune / PD13	USB differential signal
ICL_VMOUT	Neptune / PD14	Bulverde / GPIO[56]	USB negative output signal
EMU_INT	EMU One-Chip	Bulverde / GPIO[10]	EMU interrupt signal to Bulverde
BB_WDOG	Neptune / PA14	Bulverde / GPIO[13]	Neptune WDI signal - Bulverde will shutdown the power supplies when this signal asserted
BP_READY	Neptune / PC7	Bulverde / GPIO[0]	Hand-Shake signal with Bulverde during power up. Wakeup signal when Neptune waked from standby mode
PWR_EN	Bulverde	Neptune / PA9	Asserted when Bulverde enters into sleep mode for power saving - Active Low
BP_FLASH_MODE_EN	Bulverde / GPIO[41]	Neptune / PE3	Neptune Flash mode control
AP_WDOG	Bulverde / GPIO[4]	PCAP2	Power off control signal from Bulverde - Active Low
nBB_RESET	Bulverde / GPIO[82]	Neptune	Neptune reset signal from Bulverde. Bulverde can reset Neptune - Active Low
PCAP_CS	Neptune / PD9	PCAP2	Second SPI chip-select signal of Neptune - Active High
BB_SPI_CLK	Neptune / PD3	PCAP2	Second SPI clock input signal to PCAP2 from Neptune
BB_SPI_MOSI	Neptune / PD5	PCAP2	Second SPI MOSI signal to PCAP2 from Neptune
BB_SPI_MISO	PCAP2	Neptune / PD4	Second SPI MISO signal to Neptune from PCAP2
PCAP_PRI_INT	PCAP2	Neptune / PA10	Second SPI interrupt signal to Neptune from PCAP2
BUL_TXENB	Bulverde / GPIO[34]	EMU One-Chip	Bulverde USB TX enable signal to EMU. Bulverde USB P2_2
BUL_VPOUT	Bulverde / GPIO[39]	EMU One-Chip	Bulverde USB Positive output to EMU. Bulverde USB P2_6
BUL_VMOUT	Bulverde / GPIO[36]	EMU One-Chip	Bulverde USB Negative output to EMU. Bulverde USB P2_4
BUL_XRXD	EMU One-Chip	Bulverde / GPIO[35]	Bulverde USB differential intput from EMU. Bulverde USB P2_1
BUL_VPIN	EMU One-Chip	Bulverde / GPIO[40]	Bulverde USB positive input from EMU. Bulverde USB P2_5
BUL_VMIN	EMU One-Chip	Bulverde / GPIO[53]	Bulverde USB negative input from EMU. Bulverde USB P_3
CLK_13MHz	Neptune	PCAP2	13MHz clock from Neptune to PCAP2 for voice codec operation
PCAP_RESET*	PCAP2	Neptune	Neptune reset signal from PCAP2. AND together with nBB_RESET to perform
PCAP_MCU_RESET*	PCAP2	Bulverde	Bulverde reset signal from PCAP2.
AP_SEC_INT	PCAP2	Bulverde / GPIO[1]	Primary SPI interrupt signal to Bulverde from PCAP2
AP_SPI_FRM	Bulverde / GPIO[24]	PCAP2	Primary SPI chip-select signal to PCAP2 from Bulverde. Inverter is added.
AP_SPI_TXD	Bulverde / GPIO[25]	PCAP2	Primary SPI MOSI signal from Bulverde to PCAP2
AP_SPI_RXD	PCAP2	Bulverde / GPIO[26]	Primary SPI MISO signal from PCAP2 to Bulverde
AP_SPI_CLK	Bulverde / GPIO[29]	PCAP2	Primary SPI clock input signal to PCAP2 from Bulverde
SYS_RESTART	Bulverde / GPIO[55]	PCAP2	System re-start control signal to PCAP2 from Bulverde - Active 100ms pulse

Table 17 – E2 ICL Signals Function Description

7.3 E2 Clock System Control

E2 clock system block diagram shows in Figure 43. The signal with dash line is an optional selection for its corresponding connected clock signal. This may give parts saving opportunities. The clock input amplitude to each module can't be unified due to not every module required the same amplitude signal, so level shifter is needed for modules required.

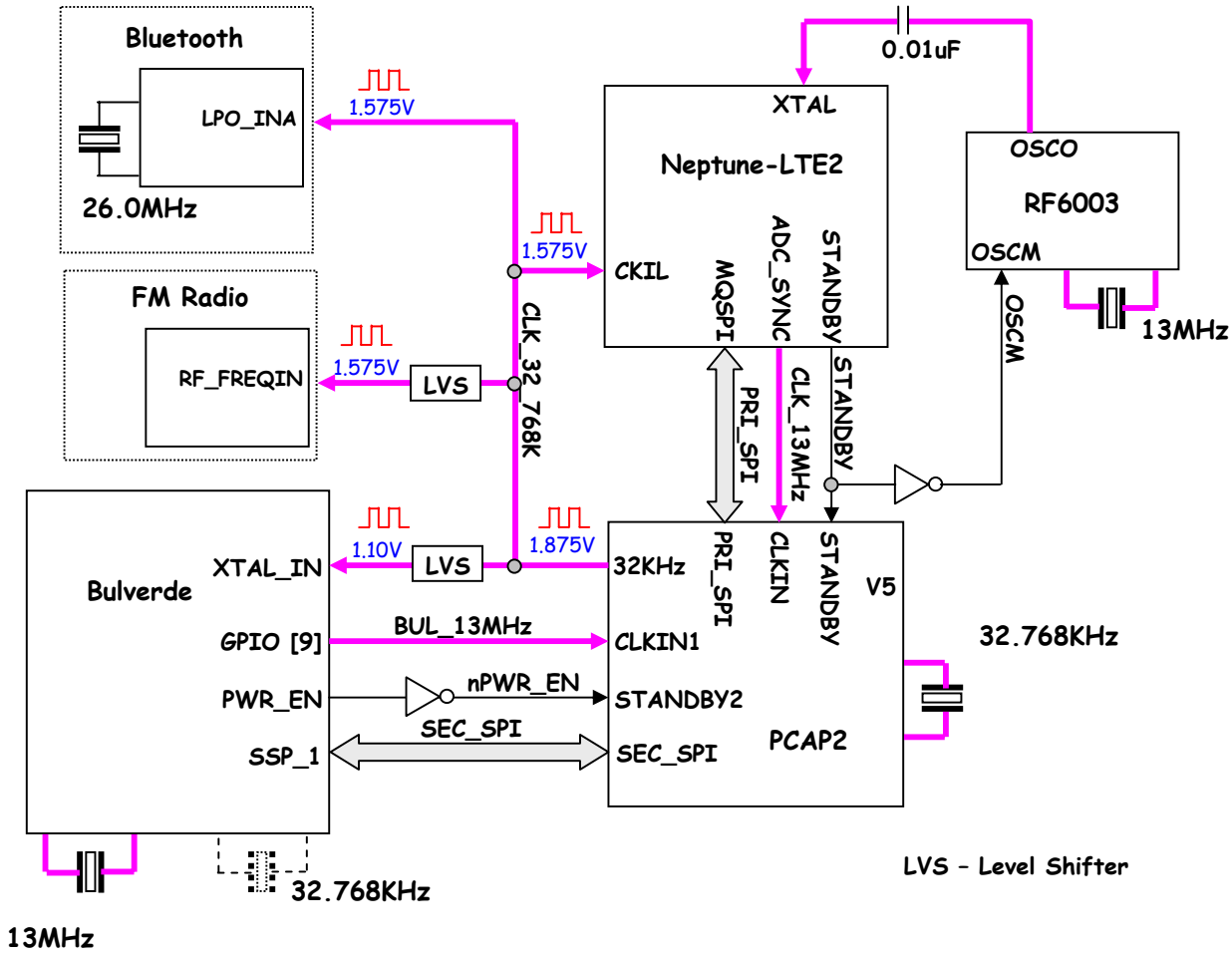


Figure 42 – E2 Clock System Control Block Diagram

7.3.1 Neptune-LTE Related Clock Signal

There are two clock input signals needed for Neptune-LTE. Neptune-LTE clock oscillator generates 26MHz clock signal by connecting a 26MHz crystal to its systems. A low frequency (32KHz) clock input is required, which can be used as wakeup events detection after Neptune-LTE enters into deep sleep mode. This clock signal is provided by PCAP2 32KHz generator. The amplitude required for 32KHz clock signal is 1.575V, and this signal provided by PCAP2 is powered by V9, so the amplitude from PCAP2 can meet the requirement of Neptune-LTE, no level shifter is needed. 13MHz clock signal can be output to PCAP2 for voice CODEC operation. Neptune-LTE 13MHz clock connects with PCAP2 CLKIN input. There are two high frequency input pins on PCAP2 chipset; this kind of architecture can avoid the situation encountered in E2 phone design. For E2 phone, adjunct processor must first request Neptune to provide 13MHz clock signal to PCAP2 before multimedia application such as MP3 player etc to begin. Such a clock request prevents baseband side from actually entering into deep sleep mode for power saving purpose.

7.3.2 RFMD Related Clock Signal

RF6003 26MHz clock input signal is provided by an external oscillator. It can also be provided by Neptune-LTE TRK_CLK_OUT, but need to do evaluations. The buffered 26MHz clock signal of RF6003 provides to RF2722 clock input pin for its operation.

7.3.3 Bulverde Related Clock Signal

Bulverde chipset needs two clock input signal for its operation. For normal operation, a 13MHz clock is required for its core to operate. During Bulverde in sleep mode, a 32KHz clock is required for wakeup events detection purpose. A 13MHz crystal is connected with Bulverde clock generator module. 32KHz clock can be generated by connecting a 32KHz crystal or providing by PCAP2, but need to be scaled to fit the 1.10V requirement. GPIO [9] can output a 13MHz clock signal to PCAP2 pin CLKIN1 during MP3 etc multimedia playback operation.
E2 doesn't need Neptune-LTE to provide 13MHz to PCAP2 anymore during Bulverde playing multimedia application etc.

7.3.4 Bluetooth Related Clock Signal

E2 Bluetooth module reuse A760 class-2 module that a 15.36MHz crystal is wrapped into its package. The 32KHz low frequency clock input can be provided directly by PCAP2 as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

7.3.5 PCAP2 Related Clock Signal

One 32.768KHz crystal is connected with PCAP2 clock generator module. 13MHz clock can input from CLKIN and CLKIN1 from Neptune-LTE and Bulverde GPIO [9] pin respectively and PCAP2 use those two different clock input for voice CODEC PLL and stereo CODEC PLL accordingly as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

Voice CODEC PLL clock will input from CLK_IN0 if CLK_IN_SEL is clear to logic 0 and input from CLK_IN1 if CLK_IN_SEL is set to logic 1 through writing to Register 11 of PCAP2 by primary or secondary SPI port.
Stereo CODEC PLL clock will input from CLK_IN0 if ST_DAC_CLK_IN_SEL is clear to logic 0 and input from CLK_IN1 in ST_DAC_CLK_IN_SEL is set to logic 1 through writing to Register 13 of PCAP2 by primary or secondary SPI port.

8 Bus and E2 Accessories

As PD required, E2 phone need to support EMU Bus. EMU (Enhanced Mini-USB) is intended o support connection to accessories, personal computers, and test systems. The bus connector has a total of 5 pins, 4 of which have multiple functions.

The bus has 5 basic features: Charging, Power Out to an accessory, USB Functionality, Analog Audio and simple Serial for communicating to intelligent accessories.

As shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**, E2 is a dual-microprocessor system. E2 EMU system architecture is different from single-microprocessor system phone's design.

8.1 E2 EMU Bus System Architecture

E2 EMU system uses EMU One-Chip to implement all EMU related functions. EMU One-Chip block diagram shows in Figure 44. Detailed informations about EMU One-Chip, please refer to "EMU One-Chip IC Specification".

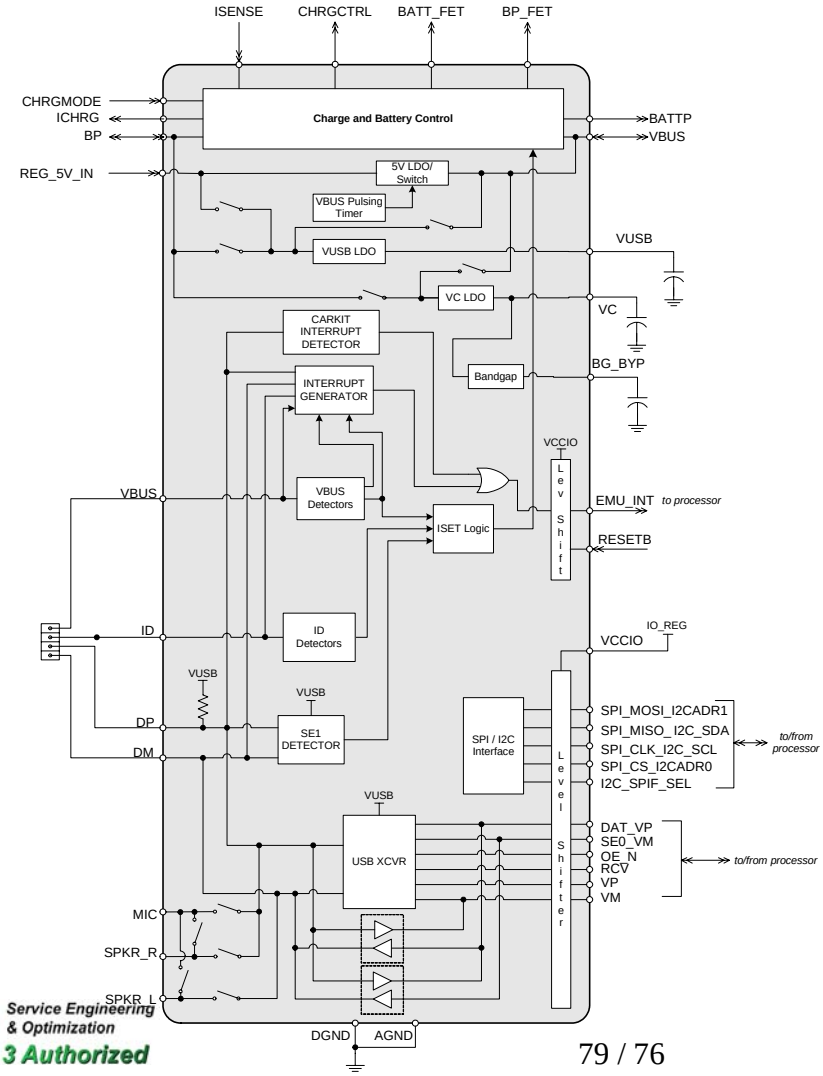


Figure 43 – E2 EMU Bus Support System Architecture Block Diagram