Motorizr Z9 (NA)

Motorola Motorizr Z9 telephone delivers 3G features in a slider form factor. It supports quad-band GSM and WCDMA band II and V. As a 3G product, the Motorizr Z9 complies with all key specifications defined by the 3GPP.

Key product features are:
Form Factor: Slider
Finish: VM
Bands/Modes: WCDMA 850/1900 MHz and GSM 850/900/1800/1900 MHz
OS: P2K
Weight: 110g
Antenna: FJA (cellular bands) and printed ground coupled IFA (Bluetooth)
Color: Mahogany

Figure 1 Motorizr Z9

Key Points and Features

- 240 x 320 262K TFT 2.4" Display
- Large 2.4” QVGA color Display
- Wireless Broadband (HSDPA 3.6)
- Integrated 2.0 Mega-pixel digital camera with 8x digital zoom
- Single Imager AT&T Video Share
- MPEG4, H.263, WMV v9, Real Video 9
- Moto Sync – Phonebook, Calendar, Email
- Music player with stereo micro-USB and Stereo BT headset support. Supports
- MP3, MIDI, AMR-NB/WB, AAC, AAC+, Enh AAC+, WMA v9, WMA DRM 10,
- RealAudio 8, XMF
- Up to 45MB User memory/ Hot swappable MicroSDHC card up to 8GB
- Speaker independent name & digit dialing
- Integrated Bluetooth™ - Stereo headset and printing profiles
- GPS receiver with built-in antenna (North America model only)

Overview

The Bute reference platform was the source of the Z9 NA schematic. V3xx is a predecessor handset which is available on the market that utilizes the Bute reference architecture as well. Figure 2 is a block diagram of Z9.

Z9 NA is the 3G handset in a trilogy of handsets using the same slider assemblies. Other designs using the Z9 slider assembly include Z6 (GSM) and Z6m (CDMA). The interface to the imager flex through the keypad flex is the same between all programs. However, the keypad flex is unique for Z9.

The Z9 design utilizes a folded J antenna (FJA) in the base housing of the phone. It is co-located in the chin of the phone with the Bluetooth antenna and polyphonic speaker.

The remainder of this document will provide an explanation of both RF and Baseband functional blocks.

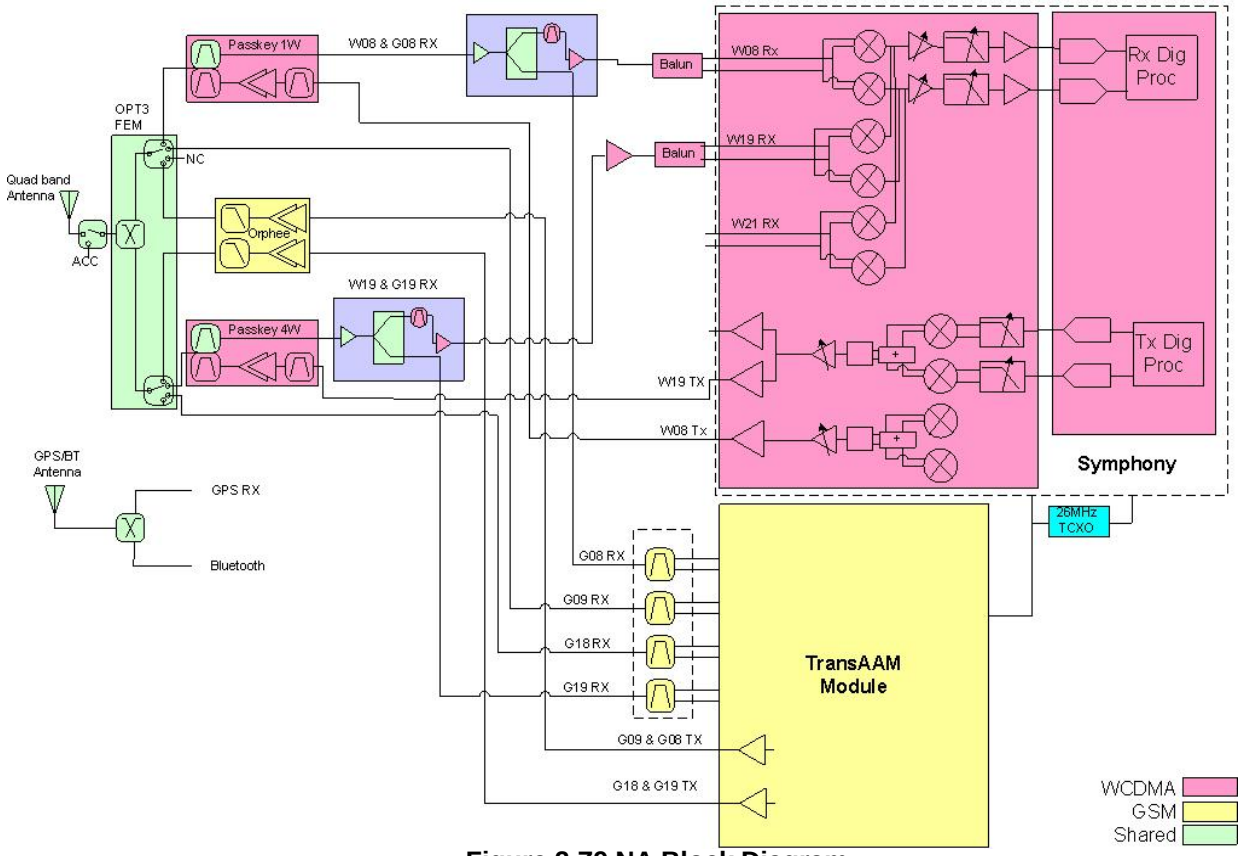

Figure 2 Z9 NA Block Diagram

GSM Receiver

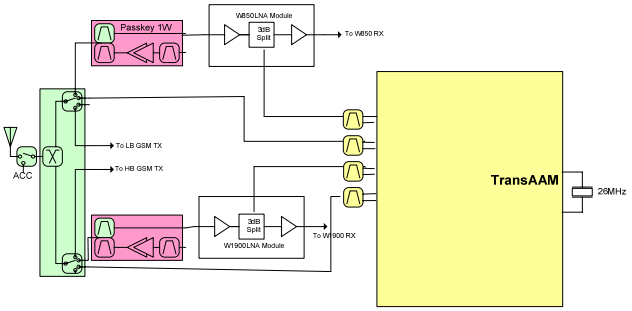

Figure 3 GSM Receiver Functional Block

Rizr Z9 supports GSM850/1900 and GSM900/1800 bands. Figure 3 shows the GSM receiver line-up. The GSM receive signal from the antenna is fed into the antenna switch through a matching circuit and an auxiliary RF connector. The antenna switch provides band selection and filtering between different bands. The RX signal from the switch is fed into the WCDMA PA module (Passkey4W or Passkey1W). The Rx signal from the duplexer inside the WCDMA PA module is fed into the Low Noise Amplifier (LNA) module for amplification. The LNA has two stages of amplification. The GSM signal is then fed into the GSM transceiver for signal processing after one stage of amplification.

Co-band LNA (U300, U350)

Rizr Z9 has two co-band LNAs. They are called co-band because same LNA is shared between GSM and WCDMA bands. U350 (Passkey1W) is shared between GSM850 and WCDMA850 bands. U300 (Passkey4W) is shared between GSM1900 and WCDMA 1900 bands. The co-band LNA is a two stage LNA where GSM signal goes through one stage of amplification and WCDMA signal goes through two stages of amplification.

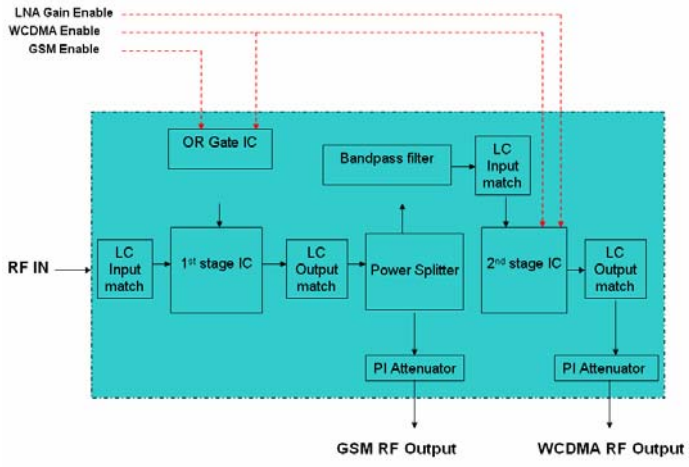

Figure 4 Co-band LNA Functional Block

The co-band LNA module has WCDMA enable, GSM enable and LNA gain pins. In WCDMA high gain mode, the WCDMA enable signal and LNA gain signal are high. In WCDMA bypass mode, WCDMA enable is high and LNA gain signal is low. The LNA operates in GSM mode when the GSM enable signal is high.

TransAAM (U500)

The TransAAM receiver is a quad-band receiver, built around a Superheterodyne-infradyne architecture. The receive signal is down-converted to a VLIF of 122.7 kHz, after the LNA and is then passed through a poly-phase filter in order to suppress the image frequency. The VLIF signal is then digitally converted to baseband and passed through a digital filter with a bandwidth of 90 kHz. The filter selected is suitable for the Downlink Advanced Receiver Performance (DARP) feature (2X, 14th order).

GSM Transmitter

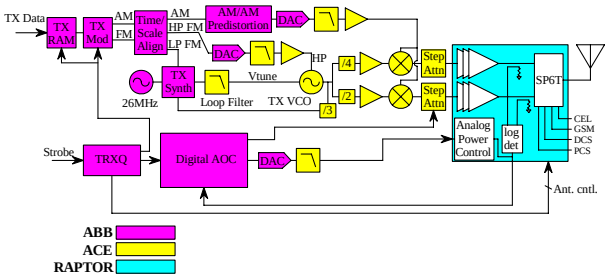

Figure 5 GSM Transmitter Functional Block

The TransAAM transmitter architecture is shown in the diagram above. It consists of the EDGE/GMSK TX modulator, Time/Scale Alignment circuit, TX synthesizer as part of a dual port modulated PLL, a TX VCO, an AM modulator, step attenuators, TRXQ, Digital Power control system, a 3 stage power amplifier, and a single pole six through RF antenna switch. The diagram is color coded to indicate block location.

TransAAM uses polar modulation for EDGE mode. TransAAM performs all of the necessary pulse shaping, and maps the data bits into amplitude and phase components for the required modulation. The AM component is corrected for AM to AM distortion. No correction is required for AM/PM distortion since the AM modulator does not produce significant AM/PM distortion.

On TransAAM, POR programming initializes registers. The values are directly derived from permanent data storage.

The EDGE/GMSK Digital Transmit Module (TXM) supports two modulation schemes (GMSK and 8-PSK) and supports the Amplitude/Frequency polar modulator. This is done by having two different modulators, a digital CORDIC algorithm and a phase derivative block. The modulator supports GMSK and 8-PSK modulation per GSM specification 05.04. The output drivers can support AM/FM and AM/PM polar transmission. The symbols enter the modulator at a rate of ~270.8333 kHz (13 Hz/48). Each GMSK symbol contains 1 bit of information and each 8-PSK symbol contains 3 bits of information. For GMSK modulation, the initial state of the modulator and the final state of the modulator is assumed to consist of an infinite series of logic “1” data bits. For 8-PSK modulation, the initial and final state of the modulator is an infinite series of logic “111” symbols/data bits This is marked ‘not defined’ in the GSM specification.

The first 3 and last 3 symbols within a burst are called “tail bits.” These 3 symbols are always “0” for GMSK and “7”, i.e. 1,1,1), for 8-PSK. The start of the burst is defined as the center of the first symbol and the end of the burst is defined as the center of the 148th symbol. The useful part of the burst is therefore 147 symbol periods, even though 148 symbols are sent to the modulator.

TransAAM supports GMSK and 8PSK modulations. The modulator is accessed by Argon LV through the digital interface described in Figure 6.

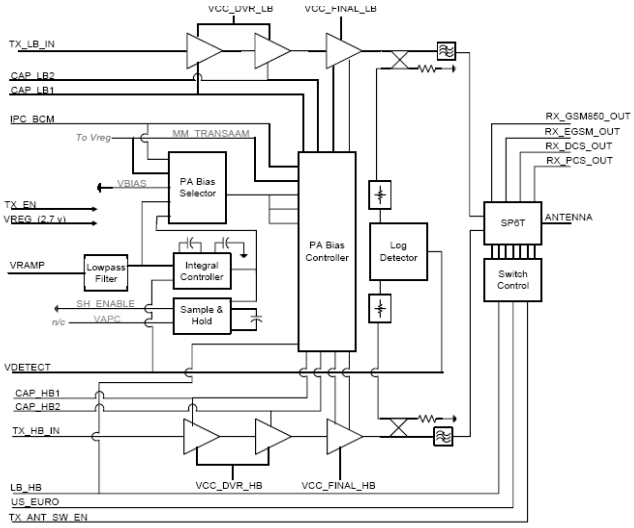

Figure 6 TransAAM Transmitter Block Diagram

WCDMA Transceiver Overview

Block Diagram

Rizr Z9 supports both WCDMA 850 and WCDMA 1900 bands. Figure 7 shows the WCDMA block diagram for Rizr Z9. The WCDMA receive signal from the antenna is fed into the antenna switch (U001) through a matching circuit and an auxiliary RF connector (M001). The antenna switch provides band selection and filtering between different bands. The RX signal from the switch is fed into the WCDMA PA. The PA has a duplexer inside it which provides isolation between WCDMA Tx and Rx paths. The Rx signal from the duplexer is fed into the Low Noise Amplifier (LNA) for amplification. From the LNA the signal goes into the WCDMA transceiver module (Symphony).

The WCDMA transmit signal path from Symphony is connected to the WCDMA PA through a transmission line. From the PA the signal is fed into the antenna through the antenna switch and auxiliary RF connector. If RF connector is used all RF signals are fed into the connector and the internal antenna path will be in an open state.

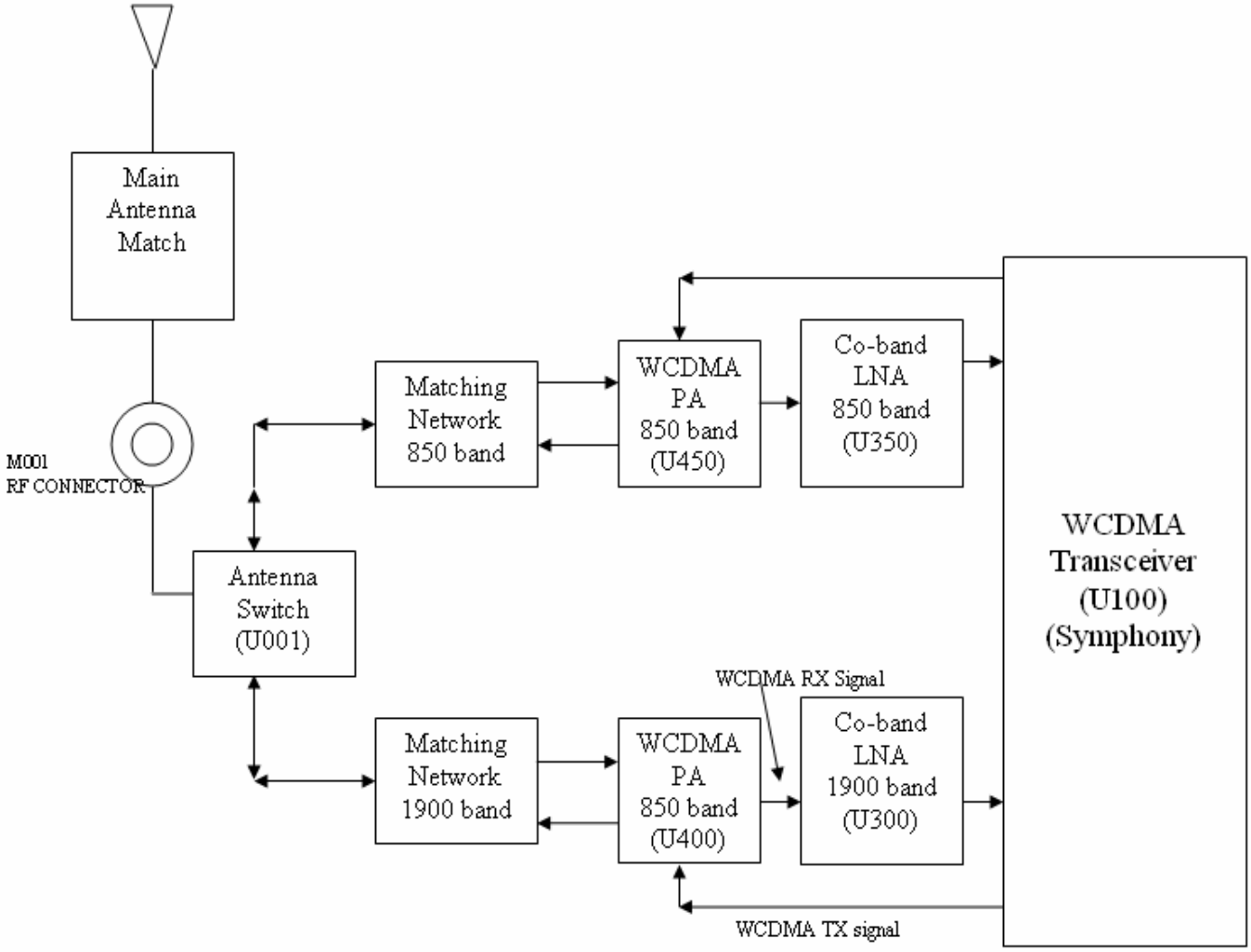

Figure 7 WCDMA Block Diagram for RizrZ9

Antenna Switch (U001)

The antenna switch provides band selection and filtering between CEL (850), EGSM (900), DCS (1800), PCS (1900), WCDMA (850, 1900) transmit and receive paths to a single antenna port. This switch consists of two GaAs FET switches, a diplexer and a three line control decoder. Figure 8 shows the block diagram of the antenna switch.

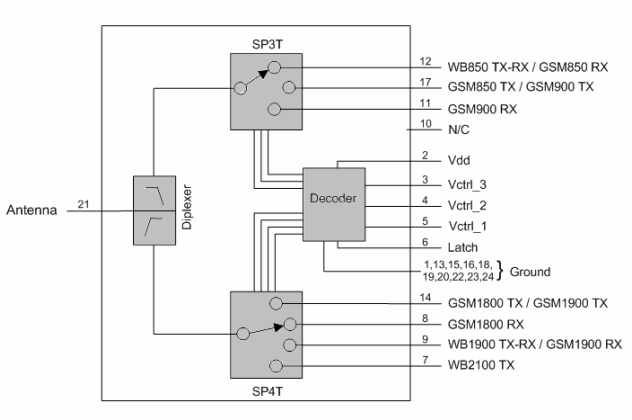

Figure 8 Block Diagram of Antenna Switch

The switch has three control pins, one supply pin, and one latch pin. The band selection in the antenna switch is controlled by the voltages on the control pins. The switch mode changes only at the rising edge of the latch. The diplexer arrangement in the module is such that when in a WCDMA call, the other end of the diplexer is connected to GSM and vice-versa. This is required to support non- compressed handovers between GSM and WCDMA.

WCDMA Receiver

Co-band LNA (U300, U350)

Rizr Z9 has two co-band LNAs. They are called co-band because same LNA is shared between GSM and WCDMA bands. U350 is shared between GSM850 and WCDMA850 bands. U300 is shared between GSM1900 and WCDMA 1900 bands.

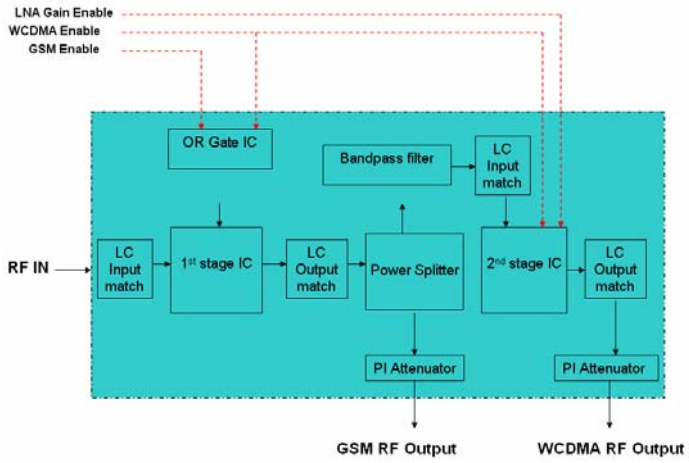

Figure 9 Block Diagram for Co-band LNA

Each LNA module has WCDMA enable, GSM enable and LNA gain pins. In WCDMA high gain mode, the WCDMA enable signal and LNA gain signal are high. In WCDMA bypass mode, WCDMA enable is high and LNA gain signal is low. The LNA operates in GSM mode when the GSM enable signal is high.

Symphony Rx (U100)

Symphony (U100) is a programmable mixed-signal quad band exciter (Tx) and receiver back-end (Rx) for a UMTS W-CDMA cellular radio (UE) operating in FDD mode. The functional interface of this part is RF at the carrier frequency and digital baseband. The four bands supported are UMTS (Band I), North American PCS (Band II), North American 800 (Band V), and Japan 800 (Band VI). Band I, V and VI are used for M702IS.

The frequency generation within the part supports variable duplex frequency spacing (Rx/Tx) per 3GPP requirements though the intention at this time is to use the part in fixed duplex mode. Because of this requirement, the Rx and Tx have separate VCO's and PLL's, and their operation is independent of the other. Loop filters are internal to the module.

The SPI (serial programming interface) is used to setup the part for operation and is programmed by the baseband processor. The SPI supports read and write operations to/from the internal programmable registers. In addition to static

operational modes defined by some of the register values, the part also includes “sequence managers” that utilize a pre-programmed sequence of instructions to dynamically enable, control, and disable the transceiver. The sequence managers are triggered by layer 1 timed control signals from the baseband processor.

The receiver architecture is a direct conversion receiver (DCR). The inputs drive three sets of differential quadrature mixers, one for each frequency band. Pre-selection filters, LNAs, and inter-stage filters must be provided externally to the inputs. The mixer inputs are internally matched to pre-defined inter-stage filter output impedances.

The mixer zero-IF outputs are low pass filtered and amplified internally with a variable gain amplifier, also known as the post-mixer amplifier (PMA). The dynamic range of the PMA is driven by the AGC system requirements. Finally, the I/Q signals are digitized, digitally filtered, and output in a serial fashion to the DSP demodulator in the baseband processor.

This particular module is a Multi-Chip Module (MCM) integrated on an organic High Density Interconnect (HDI) substrate. The module contains two IC’s named internally as “Melody” (RF/baseband interface IC) and “Viper” (RFIC). Supporting discrete components are placed inside the module such as impedance matching networks, PLL loop filters, and supply bypass capacitors. Melody is paired with Argon (U1000), which is the baseband processor. Argon includes the DSP core known as “WAMMO”.

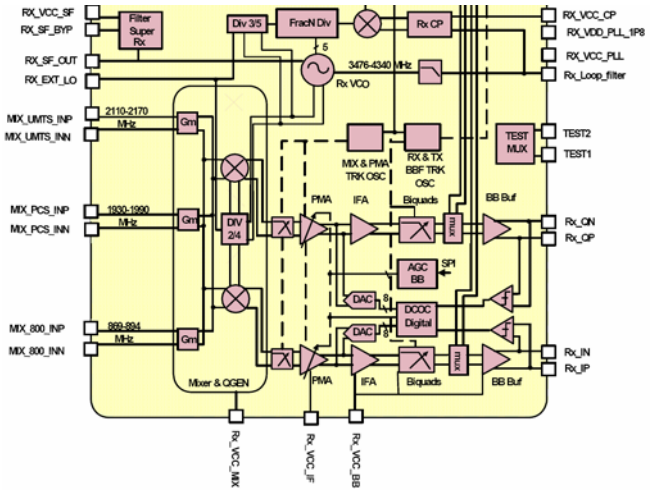

Figure 10 Symphony Rx

WCDMA Transmitter

WCDMA PA (U400, U450)

Rizr Z9 has PA for both WCDMA 850 and WCDMA 1900 bands. Figure 4 shows the block diagram for the WCDMA PA (Passkey 1W and 4W).

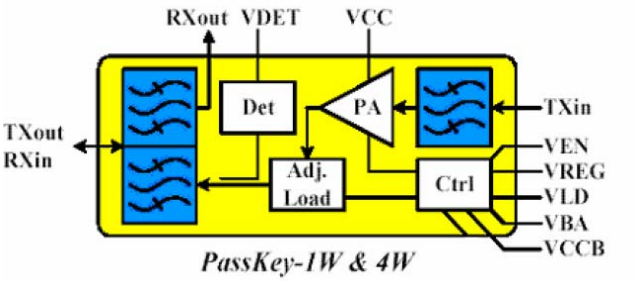

Figure 11 Block Diagram for WCDMA PA

Passkey 1W & 4W are single-band, single-mode, PA modules intended for 3G radio applications. These modules integrate inter-stage filter, power amplifier, coupler, power detector, and duplex filter for the 850 and 1900 MHz respectively. The duplexer inside the Passkey provides isolation between WCDMA Tx and Rx paths.

Symphony Tx (U100)

The transmitter architecture is direct launch. The inputs are serial digital baseband I/Q from the

DSP modulator in Argon. They are digitally filtered and then converted to baseband analog signals. After filtering, the I/Q signals are quadrature modulated and upconverted directly to the carrier frequency. The RF signal is input to a variable gain amplifier (VGA) that is controlled by the AOC feedback system for precise power control.

Finally, the RF is routed to a set of three PA driver stages, one for each frequency band, that serves as the module's output. Provided externally to this part are pre-PA filtering, PA amplification, power detection, and final Tx filtering.

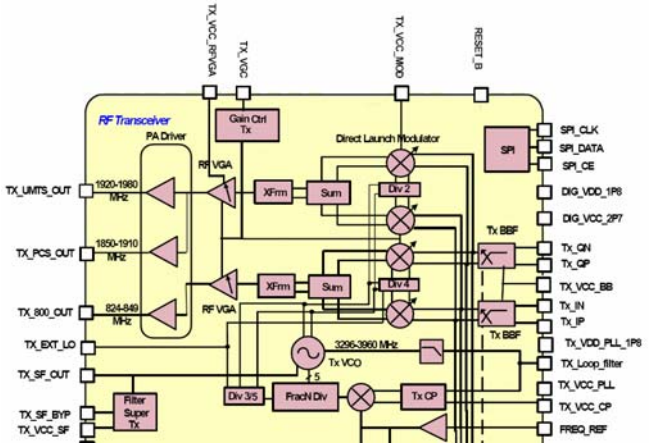

Figure 12 Symphony (Tx)

WCDMA PA (U440, U400)

Z9 has two WCDMA power amplifiers:
PASSKEY-1W PA (U450) for W850 band
PASSKEY-4W PA (U400) for the W1900 band.

PASSKEY-1W PA (U450) and PASSKEY-4W PA (U400) are 50 ohm, single-band, single-mode, WCDMA PA modules intended for 3G radio applications. The module integrates an inter-stage filter, power amplifier, coupler and power detector. The 1W and 4W modules represented by the block diagram in Figure 13 includes a Tx bandpass input filter and a full-band duplexer at the output.

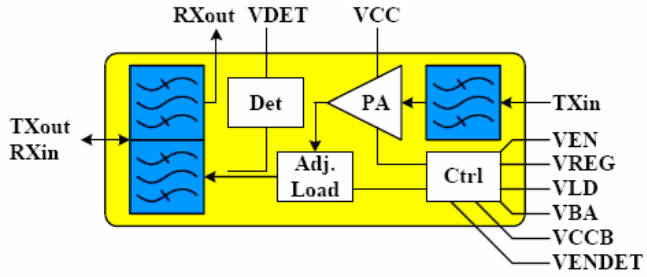

Figure 13 PASSKEY-1W and PASSKEY-4W

A Motorola proprietary high power / low power efficiency enhancement load (EE Ld) switch is included in the output match. For the EE Ld switch, VMODE voltage level changes the output load for optimum efficiency from low power to high power out. A bias line (Vba) is available for band/mode optimization for ACLR and current.

Both PA have an internal RF detector which is used for feedback to the AOC system.

The PA can be set in two modes, the High Power Mode (HPM) and the Low Power Mode (LPM). The modes are selected by setting WB_PA_VLD (Vmod) line. When VLD is set high (2.4V), the PA is in LPM. When VLD is set low (0V), the PA is in HPM. In LPM, the gain of the PA is variable. The PA gain can be varied by applying different PA biases on the WB_PA_VBIAS (VBA) line. The range for LPM is from 16dBm to below -50dBm.

In HPM the gain of the PA is the highest (20 to 23 dB). HPM is any power above 16dBm to 23 dBm at the antenna port. The PA bias, VBA is set to about 2.2V.

The WCDMA TX lineup can also be operated in a Open Loop or Closed Loop Mode. The Open Loop mode is generally from below -50 to +3dBm, below the operating range of the RF detector. The Tx power is set by calibration tables. The AOC system calculates the required TX index for the required power level and applies any channel LPM correction. Since the detector feedback is not used, the AOC system is not aware of the actual transmitted power.

The Closed Loop Mode is power levels above 3dBm, within the range of the RF detector. The Tx power is dynamically adjusted based on RF detect feedback. The detector within the PA is used to provide feedback to Symphony (AOC system) about the current output power level from the PA.

Digital Baseband Interface

ArgonLV (U1000) provides digital interfaces to WCDMA. ArgonLV utilizes BBIF bus to transmit/receive Tx and Rx I&Q data from Symphony and SPI bus for configuring Symphony's control registers. ArgonLV also uses other control signals which are mapped to GPIO control registers and Layer 1 Timer to directly control and manage RF components and their control sequence.

The interface block diagram in Figure shows the low pin count interface between the Symphony module and ArgonLV IC. To minimize the pin count, WCDMA interfaces operating at 46.08 MHz are employed. These receive and transmit interfaces employ independent I and Q channel serial data pins (RX_I, RX_Q, TX_I, and TX_Q) operating at a 46.08 MHz serial data rate, in addition to a frame control signal (RX_FRM and TX_FRM) to distinguish the first data bit in a received or transmitted data word.

In the receive path, the word rate of the 6-bit I and Q words is 7.68 MHz. After conversion to a serial format, these words are provided to the baseband at a 46.08 MHz bit rate. Alternately, in the transmit path, the word rate of the 8-bit I and Q words is at the chip rate of 3.84 MHz. After conversion to a serial format in addition to some zero padding bits, the transmitter words are also transmitted at a 46.08 MHz bit rate in this baseband interface.

The RX_WARMUP and TX_WARMUP signals from the Layer 1 timer in the baseband indicate when to initiate the RF/IF receiver and transmitter warm-up sequences, respectively. The zero-to-one transition of these signals also initiate preamble sequences in the serial Rx/Tx data interfaces. The purpose of these preamble sequences is to allow bit synchronization to the serial Rx/Tx data in the Symphony module and the baseband ICs, respectively, using internally generated 184.32 MHz (= 4 x serial date rate) clocks prior to any actual data reception or transmission. The 184.32 MHz oversampled clock is generated using independent internal

clock synthesizers in both these ICs using the 26 MHz reference clock from the crystal.

Also shown in Figure are the RX_ACQ and TX_RAMP signals which are generated from the receive and transmit sequence managers, respectively, and then fed into the receive and transmit BBIF (Baseband Interface) units. These signals are asserted after fixed programmed delays following the assertions of the RX_WARMUP and TX_WARMUP signals, respectively. The assertions of the RX_ACQ and TX_RAMP signals indicate to the receive and transmit BBIF units when to start sending actual receive and transmit data, respectively, over the Rx/Tx serial interfaces shown. The RX_SLOT and TX_SLOT signals from the Layer 1 timer to the receive and transmit sequence managers notify of Rx/Tx slot events which initiate particular internal sequencing events. The TX_AOC_UPDWN signal indicates whether to ramp up or ramp down the PA output power by a fixed programmed amount at the next TX_SLOT pulse assertion. This signal is supplied to the transmit AOC unit in the Symphony module.

In addition, the serial SPI interface lines (SS_B, SDI, SDO, and SCK) are used for bi-direction control and status information to and from the transceiver module ICs. It should also be noted that the transceiver module's SPI interface supports a write-through mode which allows the baseband to directly write to the SPI through the transceiver module.

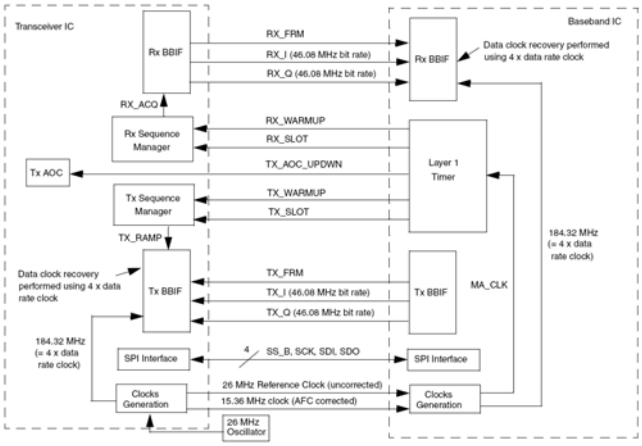

Figure 14 Symphony-ArgonLV Interface

Baseband

ArgonLV

ArgonLV is the main processor used for all system and user applications.

The Argon IC integrates the following three main cores:

- Microcontroller Unit (MCU): 385.5 MHz ARM11 used for operating system, user applications and call control.
- Digital Signal Processor (DSP): 208MHz Motorola StarCore used for call and audio data processing.
- Smart DMA (SDMA): 100MHz Direct Memory Access Controller used to assist communications between the MCU and DSP.

ArgonLV contains built in interfaces for all phone peripherals, such as MMC/SD Card (TransFlash), USIM, USB (EMU), keypad, Bluetooth and a Dedicated Smart Display interface for communicating with graphics processor on the board.

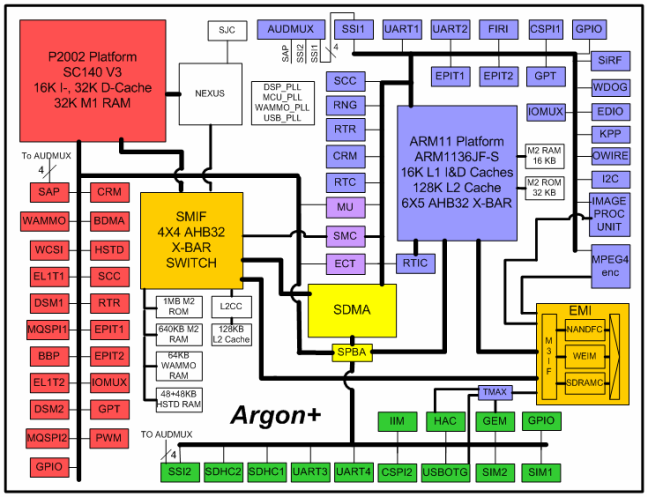

Figure 15 ArgonLV Block Diagram

Memory

Three types of memory are used with ArgonLV:

- NOR Flash: 512Mbit used for code storage. This is programmed at the factory flash and CFC stations. Code is executed from these parts directly.
- NAND Flash: 512Mbit used for the phone file system. This space is intended for user storage of songs, videos, etc. This space will be formatted at the factory flash station.
- SDRAM: 512Mbit of DDR memory.

The NOR Flash and DDR memory share address lines and the NOR Flash and the NAND Flash share data lines.

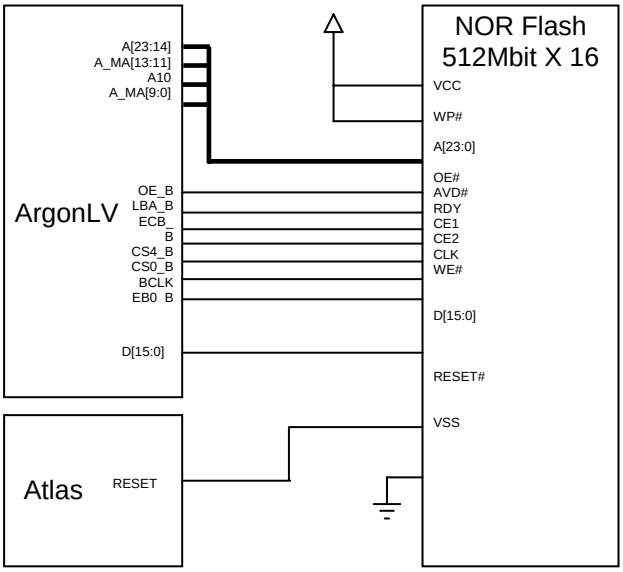

Figure 16 NOR Flash Interface

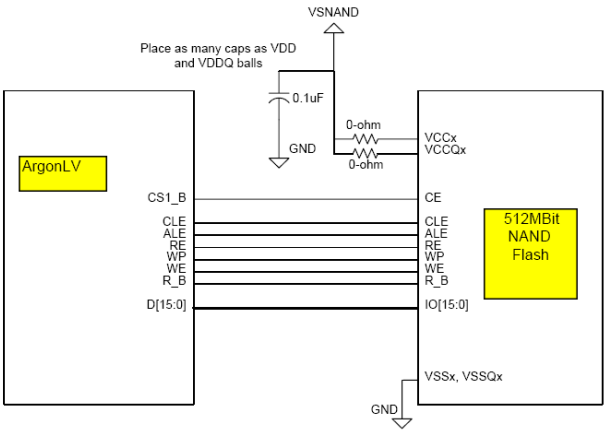

Figure 17 NAND Flash Interface

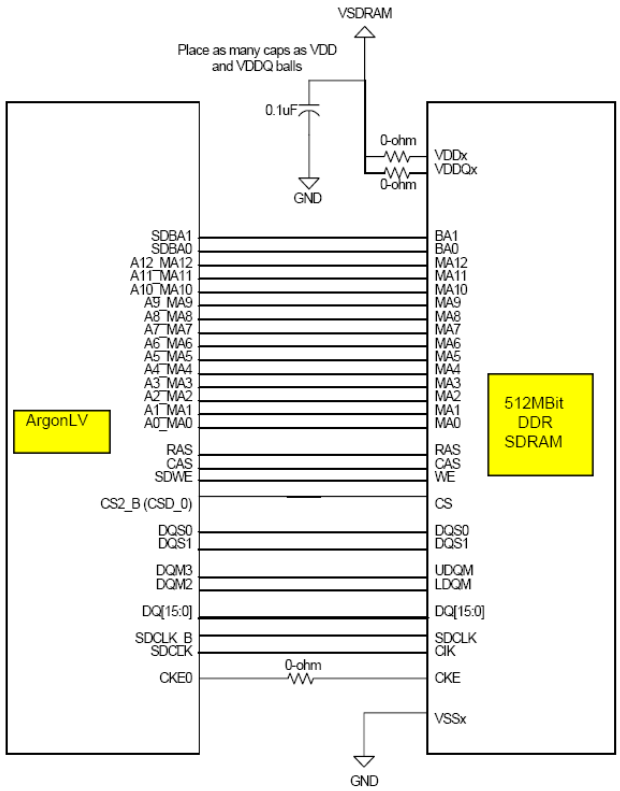

Figure 18 SDRAM Interface

ArgonLV PoP

U1000 is the ArgonLV Package on Package (PoP), which has with the memory interface pinned out on the top of the Argon microprocessor. The memory is combined into a single 15x15 MCP (multi chip package) to be placed on top of ArgonLV PoP. The parts are shipped discretely and are placed and reflowed together on the production line.

ArgonLV PoP provides significant reduction in board space by combining discrete memories into a single MCP and stacking on top of the processor.

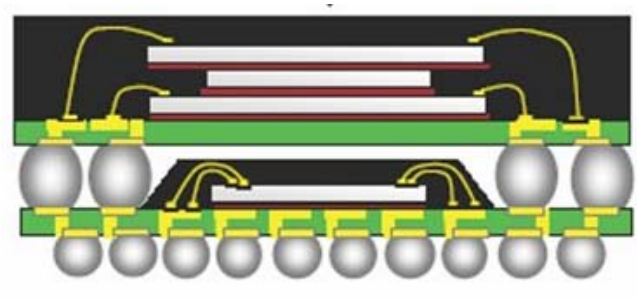

Figure 19 ArgonLV PoP

Atlas

The Atlas IC is an ASIC intended for use in Argon/Atlas platform mobile phones. It integrates several voltage regulators of both linear and switching types designed for use in the power scheme, audio codec and amplifiers, serial and USB transceivers, back- and service-light LED controllers and digital interfaces to one or two controlling processors.

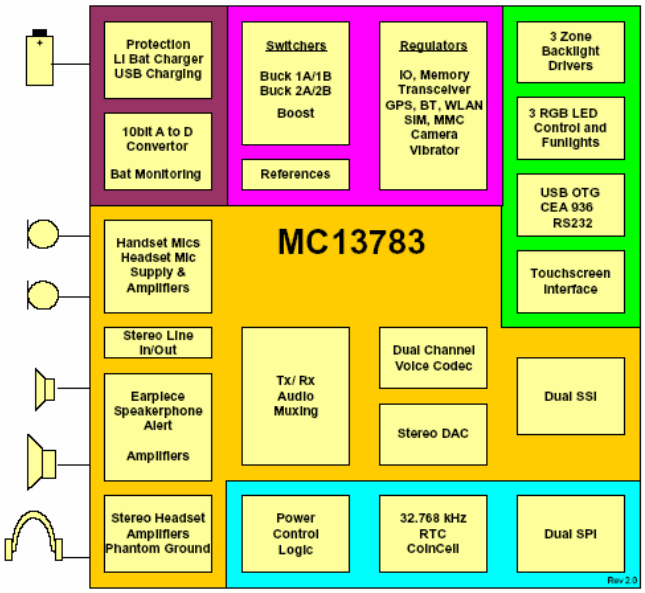

Figure 20 Atlas Block Diagram

Atlas Power Supply Architecture

The main battery voltage range is from 3.1V to 4.2V. Atlas regulates the main battery voltage to power the ICs in the phone. Some typical voltages are as follows:

- 1.5V: Argon (Turbo mode) and Graphics Processor cores
- 1.2V: ArgonLV core
- 1.8V: Memory cores, many I/O supplies
- 2.775V: Some peripheral cores, I/O supplies
- 3.3V: USB transceiver, Argon eFusing
- 5.0V: Backlight LED
- 5.0V: Used to generate 3.3V

Some voltages are provided by more than one regulator. There are three switching regulators (1.2V, 1.8V, and 5.0V) and many linear regulators.
Atlas also handles battery charging.

The regulators and power distribution are listed below:

Table 1 Power Distribution-1

Input	Reg Name	Net Name	Operating Voltage	Power up Default	Supplies
B+	SW1	VARGON_CORE	1.2V	1.6V	ArgonLV Core
B+	SW2	VLVIO, VDIG	1.8V	1.8V	Memory Cores, Low voltage I/O
B+	SW3	VBOOST	5.0V	5.5V	eFuse regulator, USB transceiver
B+	VAUDIO	VAUDIO	2.775V	2.775V	Audio circuits
B+	VIOLO	VIOLO	1.8V	1.8V	Atlas internal circuit, GPS
B+	VHVIO	VHVIO	2.775V	2.775V	High voltage I/O
B+	VRFREF	VRFREF	2.775V	2.775V	WCDMA TCXO

Table 2 Power Distribution-2

Input	Reg Name	Net Name	Operating Voltage	Power up Default	Supplies
SW2	VDIG	VMELODY_CORE, VARGON_PLL	1.5V	1.5V	Melody Core, Argon PLL
SW2	VGEN	VGPU_CORE	1.5V	1.5V	GPU
B+	VRF1	VRF_RX_2775V	2.775V	2.775V	Symphony RX, LNA
B+	VRF2	VRF_TX_2775V	2.775V	2.775V	Symphony TX, PA
B+	VRFDIG	VRF_LVIO	1.875V	1.875V	RF low IO
B+	VCAM(ext)	VCAM	2.8V	2.8V	Camera

Table 3 Power Distribution-3

Input	Reg Name	Net Name	Operating Voltage	Power up Default	Supplies
B+	VSIM	VSIM	1.8/3.0V(card inserted)	off	SIM card
B+	VMMC(ext)	VMMC_EXT	2.9V	2.9V	Transflash
VBOOST	external	VARGON_FUSE	3.3V/1.8V	1.8V	Argon Fusing

Atlas Audio

Atlas also provides the audio functions for the phone. Atlas has the analog connections to all the transducers such as Microphone, Earpiece speaker, Loudspeaker and EMU headset microphone and speakers.

Atlas also handles the digital to analog conversion of all audio, in both directions. There are two digital paths. One handles bidirectional AMR audio, which occurs during phone calls. The ASAP interface carries this traffic between Argon, Atlas and Bluetooth. The second (MMSAP) handles multimedia audio. This path is output only but can play both stereo and mono audio. Usually this is used by the MP3 and movie players.

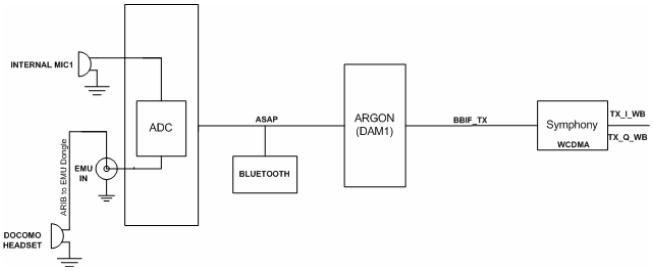

Figure 21 Audio Tx Path Block Diagram

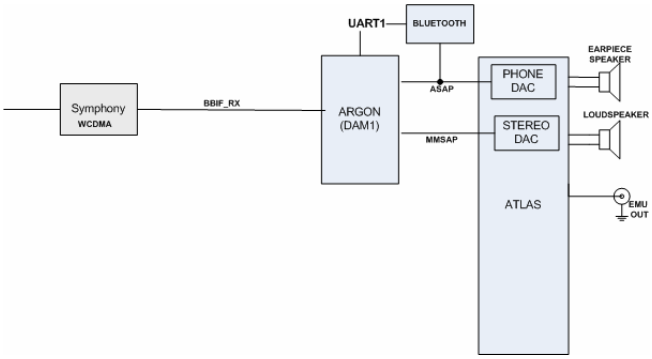

Figure 22 Audio Rx Path Block Diagram

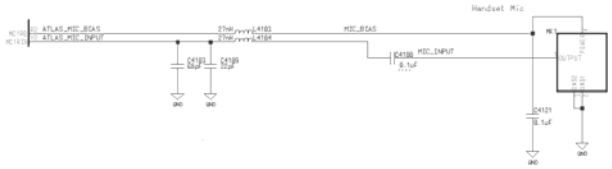

Figure 23 Handset Internal Mic Circuit

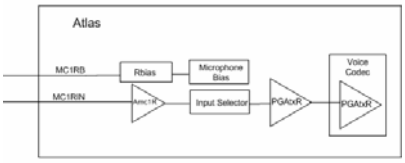

Figure 24 Atlas Mic Path

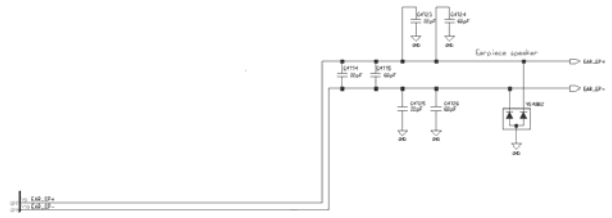

Figure 25 Handset Earpiece Speaker Circuit

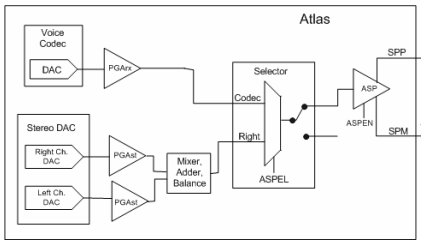

Figure 26 Atlas Speaker Path

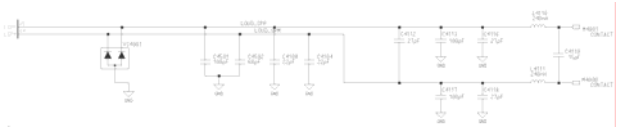

Figure 27 Handset Loudspeaker Circuit

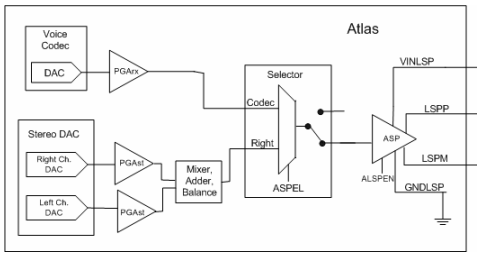

Figure 28 Atlas Loudspeaker Path

Charging Control

Dual path charger mode is being used. Figure shows Dual Path charging architecture.

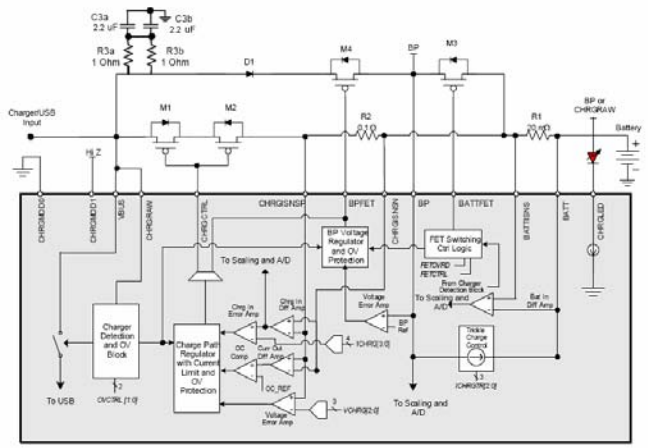

Figure 29 Dual Path Charging Architecture

Figure This Diagram below shows how the power paths lead to the battery within a phone using Atlas.
The BP regulator limits the voltage going to BP from the Charger Input to between 4.1 and 4.5 volts.
The Main FET is a switch used to selectively connect the BATTP to BP.
The Charging Regulator is a hardware circuit which limits the voltage going to BATTP and limits the maximum current from the Charger Input going to BATTP.
The Internal Trickle Charge Circuit is entirely enclosed in the Atlas IC. Its purpose is to charge dead batteries up by passing current from BP to BATTP.

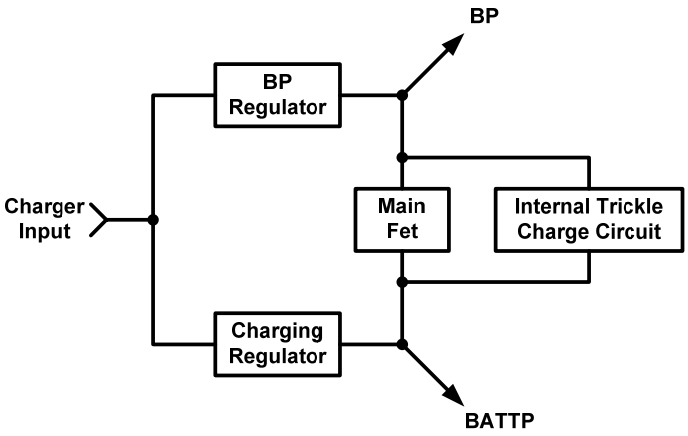

Figure 30 Charging Block Diagram

Bluetooth

The Bluetooth section is based on the Broadcom BCM2045 integrated baseband and RF IC working in conjunction with Argon LV running Motorola's Bluetooth host controller stack. Z9 uses the BCM2045 packaged in a 36-pin LGA (6mm x 6mm x 1.1mm) module (4888735Y03).

The Broadcom BCM2045 is a monolithic single-chip stand-alone baseband processor with an integrated 2.4GHz transceiver. It is 2.0-compliant and has Enhanced Data Rate (EDR) support. The baseband section controls all Bluetooth functionality from the physical layer radio HCI layer. The radio section incorporates the complete receive and transmit paths, including PLL, LNA, PA, upconverter, downconverter, modulator, demodulator, and channel select filtering. Fractional-N synthesizer can support multiple reference frequencies, from 12MHz to 40MHz.

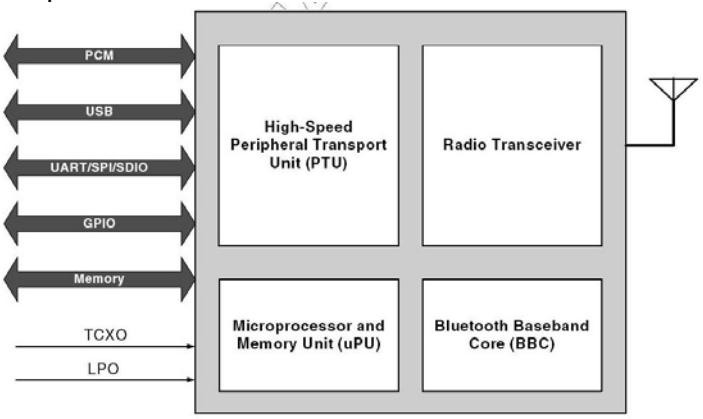

Figure 31 BCM2045 Block Diagram

The control and data messages will be transported via a 6 wire UART interface (see figure 20-2). The 6 wire mode is activated by a vendor specific command. PCM audio will be transferred between Argon and Bluetooth via Argon audio port DAM1. The Bluetooth IC requires a 26MHz RF clock (fast clock) which is generated by the Symphony module. The Bluetooth IC will use an active low clock request signal connected to SYN_TCX0_EN_IN_0 (CLK_EN_B_0) on Symphony to enable the clock when it requires a clock.

The RF and logic core will be powered by an internal LDO in the IC. VLVIO_1_8V from switcher 2 will be used to supply the LDO. The signal BT_REG_CTL will be used to enable the LDO. The chip can be reset via SW or it can also be reset by de-asserting the BT_REG_CTL signal for 250ms. The I/O voltage will also be powered by VLIVO_1_8V. The solution will be compliant with Bluetooth Specification v2.0.

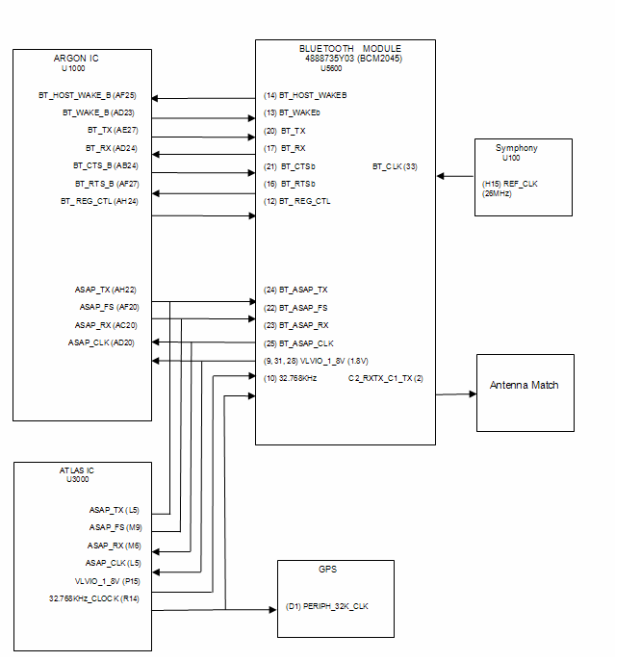

Figure 32 Bluetooth Pin Connections

Note: The Atlas ASAP_CLK pin in the diagram above should read M7 not L5.

USIM Interface

For 3G, the traditional SIM card is being called the USIM (Universal Subscriber Identity Module). The USIM will be contained on a UICC (Universal Integrated Circuit Card), which will be a removable module. The USIM shall contain an identity that unambiguously identifies a subscriber. The USIM will also provide storage for subscription and subscriber-related information. It will need to be resident in the radio for a call to be initiated. If it is not present, the user will be informed that the USIM is missing by a message on the display. If the USIM is removed during a call, the call will be terminated. Access to 3G services without a UICC containing a valid USIM will be available only for emergency calls.

The USIM will allow roaming from 3G (UMTS) networks onto GSM (pre-UMTS) networks. The phone will also allow calls to be made on pre-UMTS networks if a SIM card is inserted into the radio.

The SIM Interface Module (SIM) in ArgonLV will provide support for T=1 type SIM cards. Of the two ports available in the Argon SIM, only Port 0 will be used.

According to the 3GPP specifications, USIM support should be available over at least the following ranges: 3.0V ±10% and 1.8V ±10%. In specifications such as TS 31.101, the 1.8V supply voltage range is called “Class B” while the 3V supply voltage range is called “Class C.” Both the 1.8V and 3V ranges will be supported by Z9. USIM cards will contain an identification coded into bits 5-7 of their status information that will identify them as the appropriate technology USIM. USIM communicates with Z9 via the SIM (Smartcard Interface Module) of the Argon.

According to ISO 7816, GSM 11.12, and GSM 11.18, the clock going to the USIM should be between 3 to 4 MHz. The exact frequency will be 3.25 MHz. The SIM module in Argon contains a block designed specifically for generating the clocks used internal to the SIM module, and the clocks provided to the SIM cards.

Even if an external charger is being used, a battery will always have to be present in the phone in order to make a call. The USIM presence detect line will be active low. If a USIM is not present, the display will show a USIM insertion error. If the battery is detected, ArgonLV will try to initiate communications with the USIM. If there is no response, an “Insert USIM” error will result.

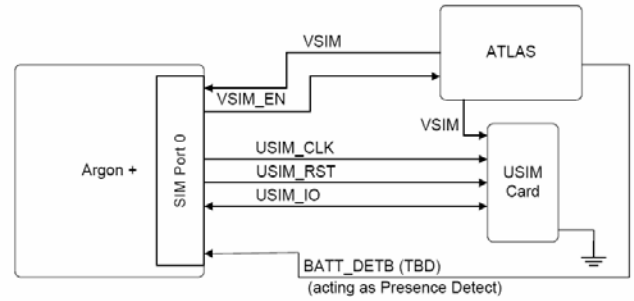

Figure 33 USIM Interface Block Diagram

TransFlash Memory Card Interface

The Argon based platforms will interface with a type of NAND flash memory card known as TransFlash (formerly known as Triflash-R). This type of card is capable of Multimedia Card (MMC), Secure Digital (SD) card, and SPI modes. The TransFlash contains a high-density flash memory as well as a controller that gives the user the ability to store personal files and use them in low-bandwidth applications.

For Argon based platforms, the Secure Digital Host Controller (SDHC) module will provide the necessary signals for communication with TransFlash cards. Because of the TransFlash connector's small size, the larger MMC and SD cards will not be supported. However, a TransFlash to SD "adaptor card" will be available that will allow users to access files with their PC using a USB-based SD card reader.

The Argon based platforms (Z9 included) will interface with TransFlash cards via the SD interface. Due to size constraints, these memory cards will not have write-protect switches. The push/push connector will utilize a mechanical presence detect switch, which will interface to GPIO #17 (Argon).

The VMMC_2.9V supply will provide power to the Vdd pin on the card. The maximum clock frequency for SD devices is 25 MHz. The SDHC module of Argon supports a maximum operating frequency of 25MHz and its base clock is the MCU peripheral clock divided by 5. The final clock rate will be determined by the value of the CLK_RATE register in Argon. Argon versions 2.1 and later have internal pull-ups.

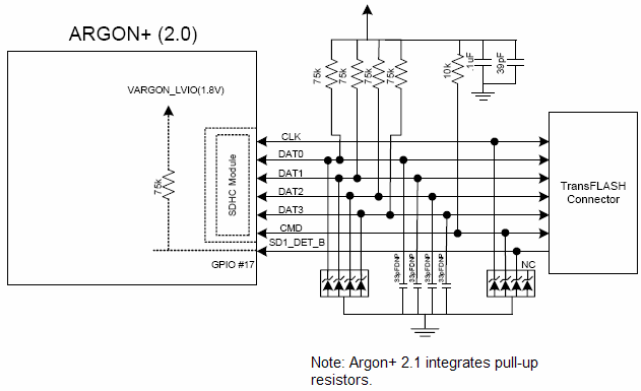

Figure 34 TransFlash Interface Block Diagram

EMU Interface

The EMU (Enhanced Mini-USB) bus is an interface that incorporates support for the CEA-936A carkit specification, charging from a variety of sources, USB connectivity, as well as support for phone-powered accessories. The EMU Bus does not provide support for JTAG.

External adapter provides compatibility with ARIB Charger and Data Cable.

The EMU Accessory connector is a standard micro USB connector with a total of 5 pins and is directly connected to the Atlas IC. The Atlas IC is a custom IC designed to provide standard signaling modes. Atlas provides audio support through EMU for accessories. In addition to the signaling modes, Atlas integrates all necessary logic to take on the task of controlling the dual path charging lineup.

When a device is connected to the EMU bus, Atlas will identify the device based on the states of the VBUS, D+, D-, and ID pins. Atlas utilizes three different detectors to determine which type of device is connected. A change in status on any of the following 3 detectors will generate an interrupt and the status can be read from the appropriate status register.

- Vbus Detector - Three comparators are used to detect the voltage level on VBUS. USBDET4V4 detects a valid VBUS while USBDET2V0 and USBDET0V8 support the USB OTG session request protocol. Each have a sense bit (USB4V4S, USB0V8S, and USB2V0S) located in the interrupt sense register. These sense bits are 1 when the VBUS level is above the detected threshold. On any rising or falling edge of the comparator outputs, a USBI interrupt is generated. VBUS can be connected to the charger input pin for joint charging and USB signaling.
- SE1 Detector - To distinguish different phone accessories, an SE1 detector checks to see if the signal on D+ and D- are above a positive threshold. If so, the SE1S bit will be set high. Any change in SE1S generates an SE1I interrupt.
- ID Detector - Used primarily to distinguish between A type and B type plugs being inserted into the micro USB connector. However, the ID pin supports two additional modes outside of USB standards: factory test mode and non USB accessory mode. The state of the ID detector can be read by SPI via the IDFLOATS and the IDGNDS sense bits. An IDI interrupt is generated when one of these sense bits changes. The ID voltage can be read out via the ADC channel ADIN7.

Finally, the exact states of D+ and D- can be read through the USBOTG module in Argon through GPIO4 and 6. However, to get D+ and D- to pass through the USB transceiver on Atlas, USB must be suspended by setting bit 1 in SPI register 49. The GPIOs are read using capture mode. Therefore GPIO4 and GPIO6 must be reserved for this feature. Although they will not be physically connected to VPIN or VMIN on the PCB, we must reserve them for this function because the control of the pins shifts between the MCU and DSP when reading the states of the lines.

USB is a serial bus that uses 5 lines (VBUS, D+, D-, ID, and GND) though the ID pin is used only for detection purposes. Each pin is connected directly to Atlas' USB transceiver through which it forwards the signals to Argon. The USB transceiver is enabled when the SPI bit USBXCVREN is set high. The USB transceiver data formatting operates in four modes, defined by the DATSE0 and BIDIR SPI bits.

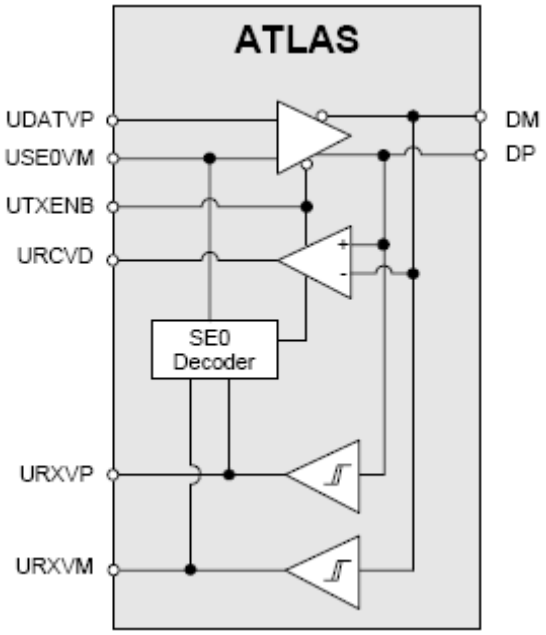

Figure 35 USB Transceiver

In all data modes, when UTXENB is high, the transmitter will be disabled while the receiver remains active. When UTXENB is low, the receiver is disabled.

The EMU Bus supports both full speed and low speed operation. The USB transceiver in Atlas controls the speed configuration through the SPI bit FSENB. Via this SPI bit, an internal 1.5kOhm pull up resistor can be connected to UDP to indicate full speed or to UDM to indicate low speed.

USB suspend mode can be enabled through the SPI bit USBSUSPEND. When it's set, the USB transceiver enters a low power mode which reduces the transceiver current drain to below 500 uA.

The USB employs NRZI (Non-Return-to-Zero-Inverted) data encoding when transmitting. In NRZI encoding, a "1" is represented by no change in level and a "0" is represented by a change in level. A string of zeros causes the NRZI data to toggle each bit time, and a string of ones causes long periods with no transitions in the data. USB also utilizes bit stuffing, where a zero is inserted after every six consecutive ones in the data stream before the data is NRZI encoded, to force a NRZI transition. The data is sent differentially over D+ and D-.

Atlas provides mono and stereo audio modes in which audio signals are multiplexed on the USB D+ and D- data lines.

After detection of any headset, the software will detect whether the headset is mono or stereo by attempting to force stereo mode. This entails enabling bit 8 in SPI Register 50 to switch in a 100kOhm pull up resistor on the ID line. Inside of a stereo headset, this increase in voltage will enable 2 analog switches which change the headset from dual mono mode to stereo mode. Along with this switch, the logic on D+ will drop from high to low. This drop in voltage can be read out of the USBOTG module in Argon using GPIO capture mode. Software will set the proper path for mono or stereo audio based on the drop in logic on D+.

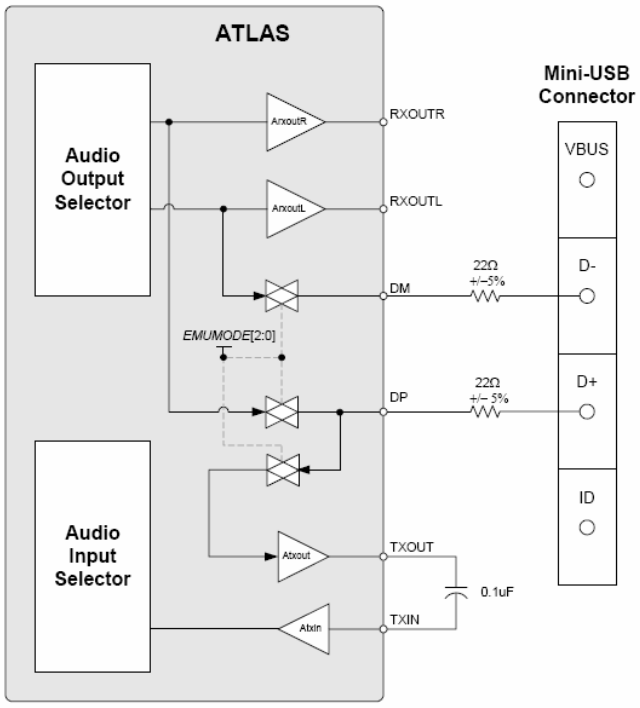

Figure 36 EMU and Atlas Audio Implementation

GPU/Serializer

The main Baseband processor, ArgonLV, interfaces to the nVidia SC12 through a parallel bus. The interface between ArgonLV and the GPU is performed using a 1 bit indirect addressing mode where the first bit on the bus specifies the bit stream as either data or as an address. The SC12 receives a 13 MHz clock from Symphony for its internal PLL. The SC12 PLL generates an output clock of 53.95MHz that is used as the input clock to the 2MP imager (Micron SOC2020). The GC module and display are driven by a relaxation oscillator which is provided by a 200K (1% tolerance) pull-up resistor to CVDD (1.5V). Argon LV will switch between relaxation oscillator and PLL when Imager is used.

The GPU supports the following:

- 3D Graphics Engine
- MPEG-4 / H.263 Hardware Codec
- JPEG Hardware Codec
- SD/SDIO Host Controller
- High Resolution COLOR Display
- Video Input
- 64-bit 2D Graphics Acceleration
- Flat Panel (LCD) Interface
- Graphics Controller
- Integrated 1280KB 128-bit SRAM
- 32-BIT Flexible Host Bus Interface
- Clock Options
- Advanced Power Management

The nVidia (SC12) GPU along with the Fairchild FIN670 serializer is used to reduce the number of lines going from the transceiver to the flip assembly. There are a total of 24 signals between nVidia and the FIN670 device. There are 6 control lines plus the 18 RGB lines from SC12 that are connected to the serializer. Using FIN670 enables the product to use the 70 pin connector that connects the flip to the transceiver, otherwise the connector pins would significantly higher.

FIN670 is a 24 bit serializer/deserializer and can be configured as master or slave. The serializer resides on the transceiver board and is configured as master. The deserializer resides in the display module is configured as slave.

Below is the table of the GPU to FIN670 pin mapping.

nVidia	Emerald Signal Name	Fin670 PIN
FSCLK	DISP_MCLK	STRB1_WCLK0
FDE	DISP_OE	CNTL2
FHSYNC	DISP_HSYNC	CNTL0
FVSYNC	DISP_VSYNC	CNTL1
FGP6	SER_STBY_B	EN_STBY_RSLEW
FGP7	SER_RST_B	RES
FD0	LCD_BLU[0]	DP0
FD1	LCD_BLU[1]	DP1
FD2	LCD_BLU[2]	DP2
FD3	LCD_BLU[3]	DP3
FD4	LCD_BLU[4]	DP4
FD5	LCD_BLU[5]	DP5
FD6	LCD_GRN[0]	DP6
FD7	LCD_GRN[1]	DP7
FD8	LCD_GRN[2]	DP8
FD9	LCD_GRN[3]	DP9
FD10	LCD_GRN[4]	DP10
FD11	LCD_GRN[5]	DP11
FD12	LCD_RED[0]	DP12
FD13	LCD_RED[1]	DP13
FD14	LCD_RED[2]	DP14
FD15	LCD_RED[3]	DP15
FD16	LCD_RED[4]	DP16
FD17	LCD_RED[5]	DP17

Listed below are the four signals from the serializer outputs connected to the display via the 70-pin connector.

Emerald Signal Name	Fin670 PIN
DISP_CLK_POS	CKS_POS_DS_POS
DISP_CLK_NEG	CKS_NEG_DS_NEG
DISP_DATA_POS	DS_POS_CKS_POS
DISP_DATA_NEG	DS_NEG_CKS_NEG

There is also a high speed serial interface (HSSI) from the GPU to the display module for communicating to the display module.

Below is the block diagram of the Flip to GPU/Serializer and Argon Interface

Slider

The Slider Module has the following functions:

- Main display
- Display backlights
- Indicator LEDs
- Navigation keys
- Earpiece Speaker
- Microphone

Display

This display module is comprised of a color Active Matrix Liquid Crystal Display (AMLCD) of glass construction with White pixels on a Black background. The display module consists of 240 (x RGB Stripe) x 320 pixels with 262144 colors. The display is a 2.4" transmissive main display. The interface method is HSS with read/write SPI interface.
This display module is constructed of
• A Liquid Crystal Display Glass assemblies consisting of the top glass plate, top and bottom polarizers and compensation films, color filter, liquid crystal,, and Poly-Si backplane containing the pixel transistors.
• Chip-on-glass (COG) with the driver ("chip") located on the front of the sub panel; with flex interconnect to main display.
• FPC with the necessary passive components.
• 6 LEDs on flex for parallel backlighting.
• HSS de-serializer for RGB decoding use case
• SPI command channel for RGB HSS use case.

Displays Backlight

There are six parallel LEDs used for the lighting of display module. The display module backlight LEDs are by Atlas. Below is the block diagram of the display module backlight.

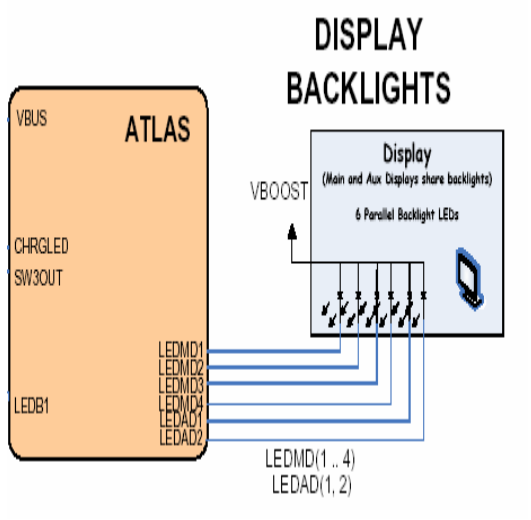

Figure 37
Display backlight block diagram

Indicator LEDs

There are two LEDs in the slider. A green LED controlled by Atlas (CHRGLED). This LED is used to indicate charging status and phone events (incoming call, voice mail, etc). A blue LED controlled by Atlas (LED_BT) that indicates an active Bluetooth connection. Below is the block diagram of the indicator LEDs.

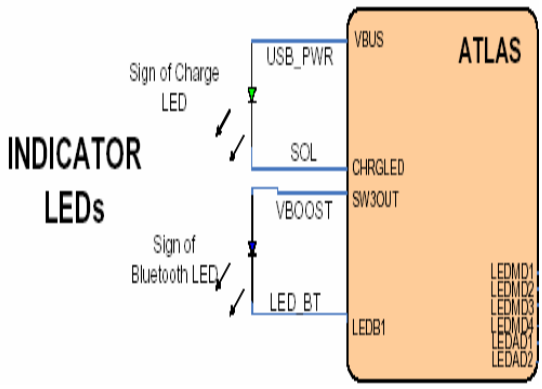

Figure 38
Indicator LEDs Block Diagram

External camera

The following External and Internal Cameras are in the flip module:

- Sensor Resolution: 2.0 MP CMOS
- Number of Pixels: 1600 x 1200
- Optical Format: ¼ inch (4:3)
- Maximum frame rate:
  15 fps at full resolution
  24 fps in preview mode
  30 fps in video mode
- Diagonal Field-of-View: 60 degree nom.
- Pixel Size: 2.2 um x 2.2 um
- Sensor Vendor and Model: Micron (MI–SOC2020)
- Dimensions: 8.5x8.5x6mm.

Keypad Backlight

The Keypad lighting is done using 8 LEDs, two LED drivers and a thin, silicon sheet light guide. The LEDs are powered by Vboost, which comes from Atlas. The LED drivers are enabled by the Argon signal Vcontrol.

Keypad

The power key is connected directly to Atlas. All other key presses are detected by keypad press port (KPP) on ArgonLV.
The KPP on ArgonLV can support up to an 8 x 8 row-by-column keypad matrix. The KPP will use a 32.768 KHz clock.

GPS

The Z9 design includes the SiRF GSCi-5000 that is a standalone integrated GPS receiver packaged in a 4mm x 6mm BGA carrier. The GSCi-5000 package consists of a custom digital processor die fabricated in 90nm CMOS technology and a custom RF receiver die fabricated in 0.18um SiGe BiCMOS technology. The RF receiver includes an LNA, fractional-N synthesizer with integrated VCO, integrated IF filter, AGC circuitry and a serial port interface. The digital processor will consists of a GPS acquisition engine with 32,768 correlators, high-speed SRAM, an instruction ROM, ARM7S processor and DUART interface.

The GSCI-5000 will receive and decode GPS signals at 1575.42 MHz. It is a self contained GPS receiver capable of producing a final position solution including full tracking and data decode capability. The hardware architecture will support assisted and autonomous operation. A patch RAM memory is available for software updates to the ROM version.

The AGPS IC requires a 26MHz RF clock (fast clock) which is generated by a dedicated TCXO as shown in Figure 2. The AGPS IC also requires a 32.768kHz clock generated by the Atlas.

The AGPS IC will use an active low signal connected to GPS_CLK on Symphony to enable the clock when it requires a clock.

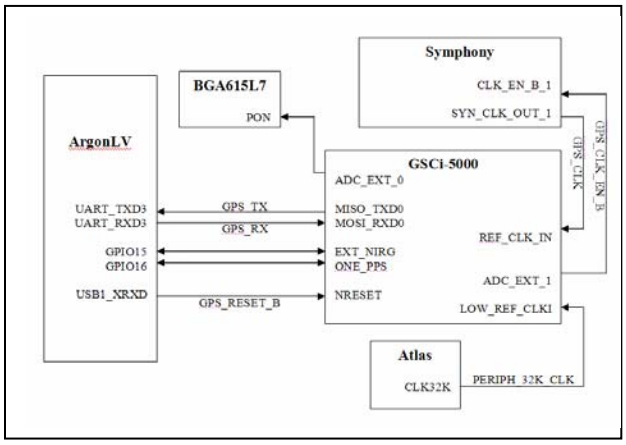

Figure 40 GPS Block Diagram