Service Engineering & Optimization

Level 3 Authorized

RAZR06 CR EDGE
Operational Description

Table of Contents

Features available in this family of cell phones include:

- GSM 850/900/1800/1900 MHz GPRS/EGPRS (2U/4D)
- Built in VGA Camera (640x480 pixels)
- 256K TFT Active Color Display
- External Vertical CLI Display
- Polyphonic Speaker
- Speaker Phone
- Bluetooth™ Class 2
- Metal Housings

Antenna Circuit

In order for the phone to report accurate receive level of an incoming signal, the efficiency of the antenna must be taken into account. Note that RAZR V3 does not support any RF cabled accessories. The connector located on the rear of the phone near the bottom, underneath the battery door and it is not accessible to end-users, is designed to be used only for factory testing, type acceptance, and repair center personnel. When a cabled connection is made the plane of reference is shifted to the connector and RX level measurements need to be adjusted accordingly. The signal ANT_DETB is normally low when a connection to the antenna is present. This signal alerts the software to account for a phased offset to accurately reflect the power of an incoming signal at the antenna. When a cabled connection is established, the path to ground is broken and a pull-up resistor to VDD asserts the ANT_DETB line and signals that the plane of reference is now the accessory port. Since the signal is normally low and is shunted to ground via a resistive path, the 69 kohm pull-up resistor inside the Neptune LTS / LTE maintains a steady state current drain that is unacceptable for deep sleep requirements. Therefore the ANT_DETB line is configured as a bidirectional line, where it is an input during the time it is begin polled to determine if an antenna is present, and then switched to an output that is always asserted low to eliminate current drain.

Figure 2. Radiated RF
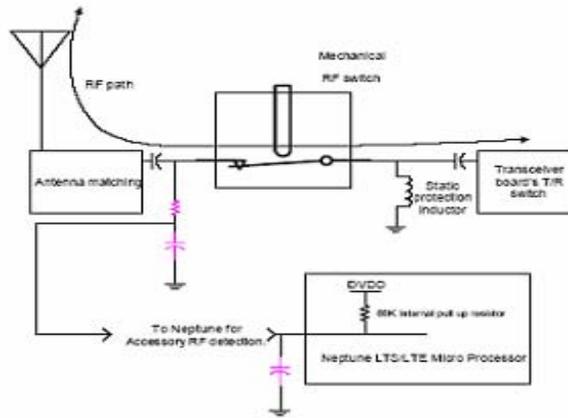
Figure 3. Conducted RF
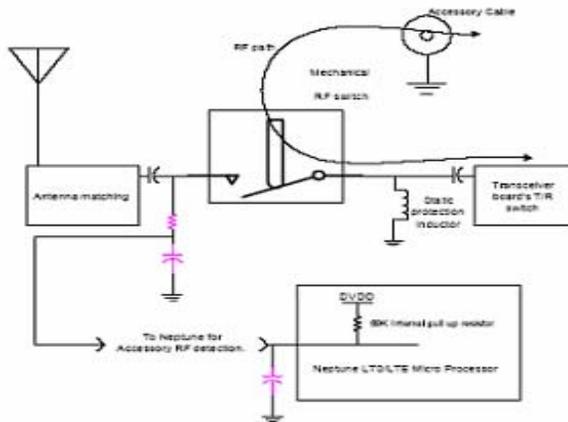
Features of RF6029 (Receiver and Synthesizer IC)

• EDGE Polar Modulator
• Frac-N Digital GMSK Modulator
• Integrated VCO's, Loop Filters, 4 RX SAW Filters, Matching, Bypass Caps
• On-Chip Reference Oscillator Outputs (26MHzor 13MHz to Baseband)
• Analog I/Q and Digital Baseband Interfaces
• VLIF and DCR RX Modes
• SAIC Capable
• Two DACs: Power Amplifier Ramp and Frequency Control
• 10mmx10mm Leadless Package

Applications

• Multi-Band GPRS Handsets
• Multi-Band EDGE Handsets

Function Description:

The transceiver, RF6029, is a highly integrated 10mmx10mm module supporting quad-band GSM, GPRS and EDGE cellular standards in the GSM850, EGSM, DCS, and PCS bands. The module includes the die with integrated VCO's and
Fractional-N synthesizer, RX SAW filters and surface-mounted passive components, mounted on an HDI substrate over-molded
to a total height of 1.7mm. The RX path includes four RX SAW filters matched to dedicated LNA's, an integrated VCO, an image rejection down-converting mixer, automatic gain control (AGC), and the necessary channel filtering to meet blocking and IMD requirements. The down-converted baseband I and Q signals can be configured for either analog or digital operation.
Module functionality is controlled through a three-wire SDI bus and dedicated TX/RX control signals.
The RF6029 transceiver module is for quad-band GSM/GPRS/EDGE applications. Included, in the module, are integrated RX SAW filters, integrated TX power VCOs and a RX VCO, a GMSK modulator; a 8PSK modulator; PA ramp control and reference oscillator circuitry for an off-module crystal oscillator. Configuration of the transceiver is accomplished by setting internal registers via a 3-wire serial interface that connects directly to the baseband controller. In receive; the RF6029 accepts four inputs from the switchplexer (one for each RX band) and after down-conversion and filtering sends RX I/Q data to the baseband. The output format may be either analog or digital. In transmit, the RF6029 module takes either analog I/Q data or the TX symbol data from the baseband, uses this to modulate the TX VCO and control the PA ramping signal to the PA or transmit module. The switchplexer may also be controlled with the general purpose output lines in the module.
The fractional-N synthesizer section is multiplexed between transmit and receive functions, creating two sets of PLL parameters. The PLLx0 register determines the state in which the PLL is working. Each PLL configuration has a fully integrated loop filter.
The RF6029 module has a buffered oscillator output that provides either a 13MHz or 26MHz reference output for use by the baseband. The frequency of this buffered output is user selectable.
The internal power VCO's are designed for use in the following frequency ranges: VCO1 has a frequency range of 824MHz to 915MHz; and, VCO2 has a frequency range of 1710MHz to 1910MHz. Each VCO is buffered and has a +4dBm minimum output power.

Figure 4. Detailed Functional Block Diagram

Tranceiver Blcok Diagram
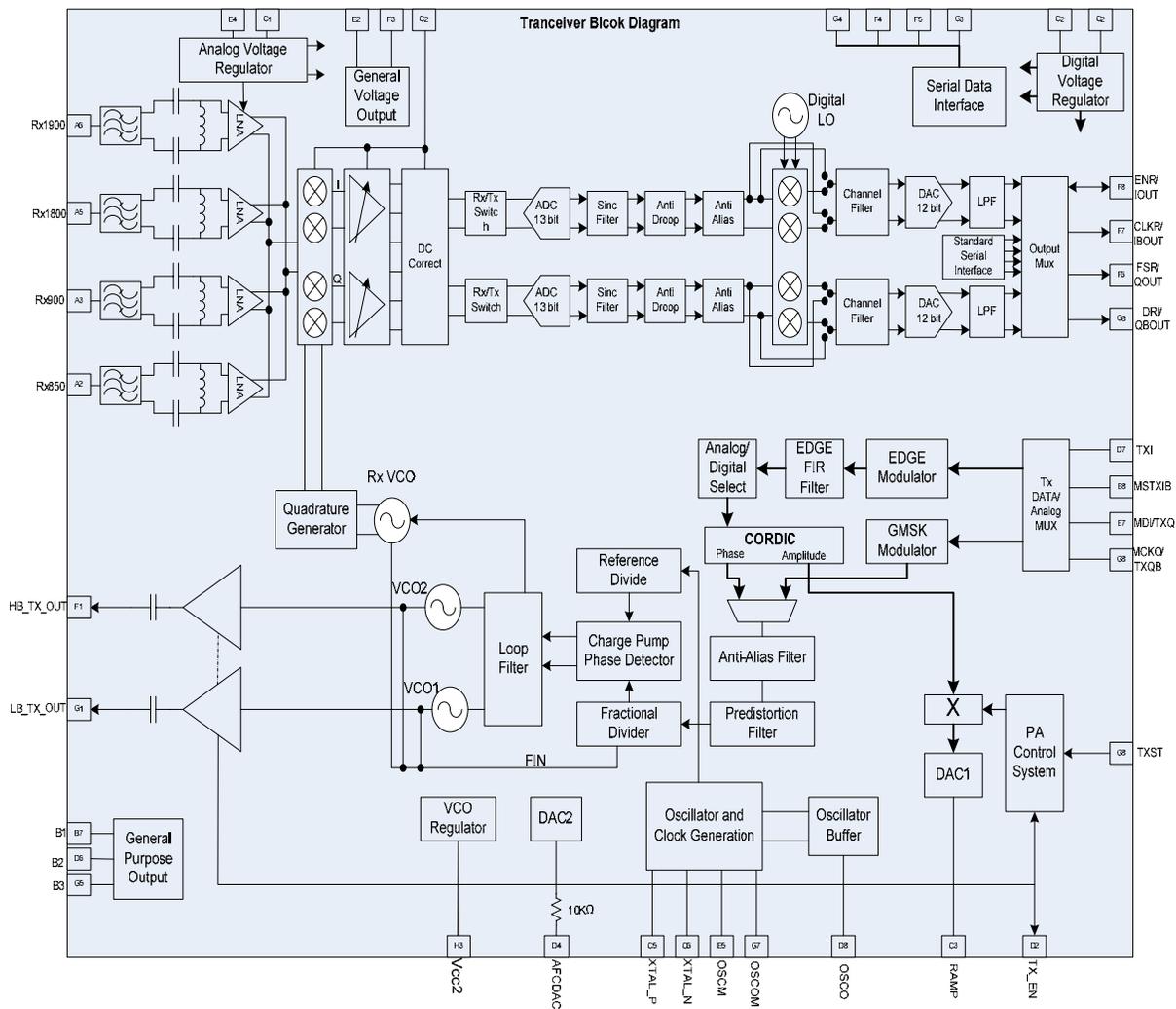
Transmitter Theory of Operation

I. RF3178EA

RF3178EA is a 2W TX front end module. It is capable to transmit and receive quad-band which consists of GSM850/900, DCS1800 and PCS1900 and is compatible with GSM/GPRS/EGPRS operating modes. The module consists of two 3-stages power amplifier line-ups, matching/harmonic filter circuits, a controller and an antenna switch. This integrated module includes two separate GaAs dies for PA line-ups, one single CMOS die for the controller to control output power and RF switch and a single PHEMT die for the RF switch.

RF3178EA uses Collector Voltage Control Method to vary PA output power. This is done by regulating the collector voltage of the PA to a reference voltage. Besides controlling output power, the controller also consists of decoder circuit to control RF switch. The single throw, six pole switches is used to select among Tx850/900, Tx1800/1900, Rx850, Rx900, Rx1800 and Rx1900.

Figure 5. RF3178EA Block Diagram
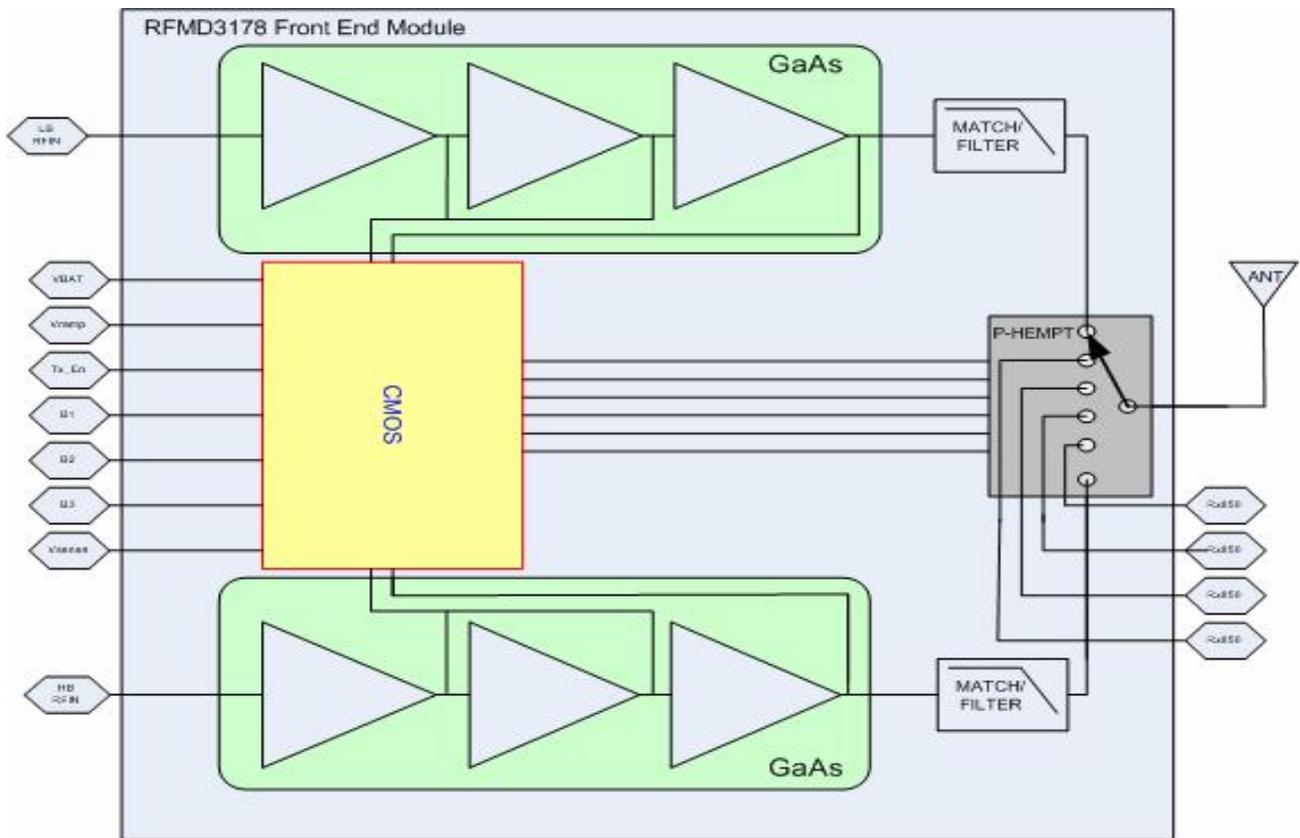
II. Antenna Switch Truth Table

Table below shows the truth table for the RF3178EA antenna switch. The antenna switch routes the appropriate band transmit or receive signal between the antenna and respective IC. The switch is controlled by VTxLB, VTxHB, VRx850, VRx900, VRx1800 and VRx1900 inside the RF6029. These controlled signals are decoded from **B1**, **B2** and **B3**, output from the RF6029. B1, B2 and B3 are connected to GPO1, GPO2, and GPO3 inside the RF6029. These 3 lines are programmed through the SPI interface in register CFG3 on the RF6029.

Table: Antenna Switch Truth Table for RF3178EA

TX_EN	B3	B2	B1	PA Module Mode	VTx LB	VTx HB	VRx 850	VRx 900	VRx 1800	VRx 1900
0	0	0	0	Low power standby mode	0	0	0	0	0	0
0	1	0	0	RX850	0	0	1	0	0	0
0	X	0	1	RX900	0	0	0	1	0	0
0	X	1	0	RX1800	0	0	0	0	1	0

0	X	1	1	RX1900	0	0	0	0	0	1
1	0	0	X	TX low band, low output	1	0	0	0	0	0
1	1	0	X	TX low band, high output	1	0	0	0	0	0
1	0	1	X	TX high band, low output	0	1	0	0	0	0
1	1	1	X	TX high band, high output	0	1	0	0	0	0

III. Table: Operating Frequency

The below table shows transmit and receive frequencies of GSM quad-band.

Band	GSM900	DCS1800	PCS1900	GSM850
Tx Frequency	880MHz - 915MHz	1710MHz - 1785MHz	1850MHz - 1910Mhz	824MHz - 849MHz
Rx Frequency	925MHz - 960MHz	1805MHz - 1880MHz	1930MHz - 1990MHz	869MHz - 894MHz

IV. Interface between RF and Base Band

The diagram below describes interface between RF3178EA, RF6029 and Neptune. The connections include RF, analog and digital signals.

- RX signals flow the antenna to RF6029 through RF switch inside the RF3178EA. These signals are filtered, amplified, mixed, converted to IQ and digitized before sending to the Base Band IC. The transmitter IQ is modulated directly into the TxVCO's, buffered then sent to RF3178 for amplification.
- Vramp from RF6029 is used to control PA output power. This signal includes the amplitudes and timings of ramping up, final power level and ramping down of the TX burst. DAC values are programmed through SPI interface in the registers inside RF6029. Vsense from RF3178EA to Neptune is used to monitor the current drain of the PA.
- B1, B2 and B3 of RF3178EA are connected to GPO1, GPO2 and GPO3 of the RF6029. The values of these signals are stored in register inside RF6029. MS, MCLK, and MDI from Neptune to RF6029 are TX modulation sync, clock and TXQ/TXIB analog signals. DRI, FSR and CLKR from RF6029 to Neptune are digital serial RX data interface frame sync or Q analog signal and digital serial RX data interface clock or IB analog signals. OSCO from RF6029 to Neptune is a digital clock. It is used as system clock of the radio. Its frequency is dependent of OSCOM. As stated earlier, SPI from Neptune to RF6029 is used to program the RF6029. TX_START, ENR, RX_ANT_EN are transmit start, digital serial RX data interface enable and receiver enable.

Figure 6. Interface Block Diagram
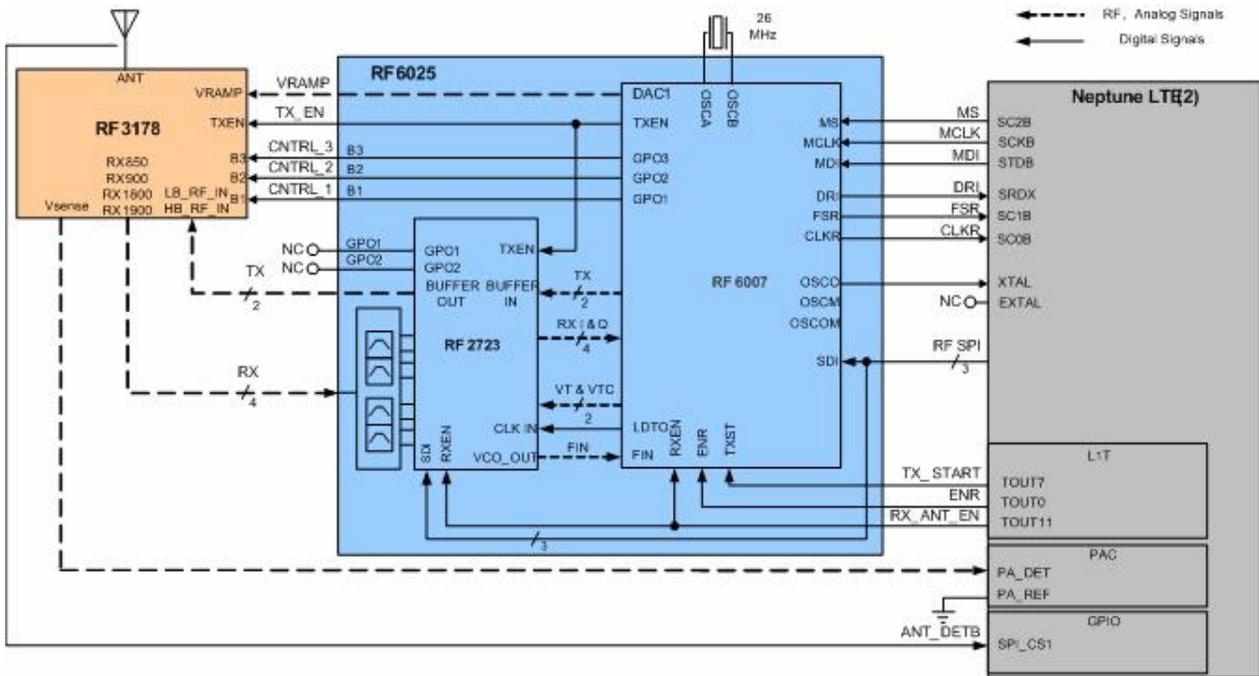
Power Distribution

Voltage regulation is provided by the Atlas Ultra-lite IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are listed below.

Vbuck, 1.875V +/- 3%
>Sources Neptune Core

Vboost 5.0V +/- 5%
>Source for Display backlights

VIO = IO_REG, 2.775V +/- 3%,
>Sources ATI Graphics Accel I/O
>Ring, Camera, SPI interfaces

VREFREG = REF_REG, 1.575V +/-2%
>Provides 1.575V reference to Neptune

VCAM = REG_3V   2.75V SW reprogrammed to 3.1V
>Supply for the camera's analog imager circuitry.

VSIM = VSIM
>Sources SIM circuitry

VAUDIO = AUD_REG, 2.775V +/- 3.6%
>Sources Atlas Ultra-lite audio circuitry

VBT = BTRF_REG, 1.875 V +/- 3%
>Sources blue tooth RF circuitry

VPIO = PERIPH_IO_REG 2.775v +/-3%
>Sources Neptune IO ring, SPI interfaces, RFMD 6027 IO ring

VVCO = VCO_REG 2.775V +/- 2.7%
> Sources RFMD 6027 VCO

VRF = RF_REG 2.775V +/- 3%
> Sources RFMD 6027 circuitry

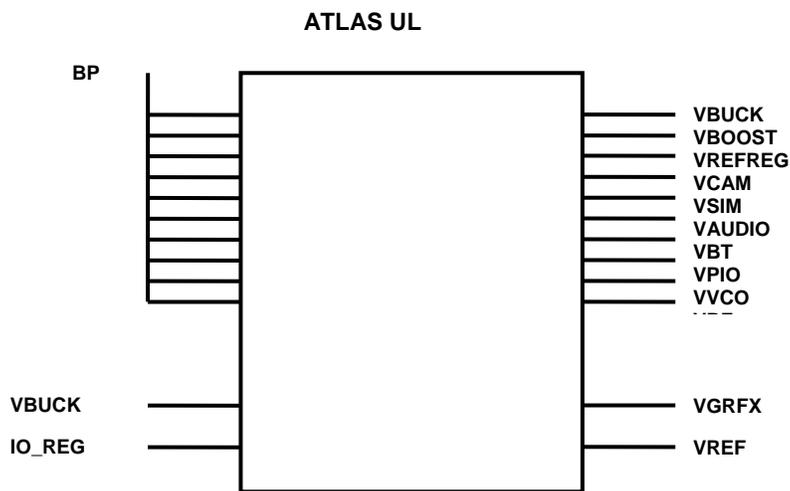**VGRFX = GRAPH_REG 1.275 +/- 3%**
> Sources ATI Graphics Accel Core

**VM Regulator**
> Not connected

VGSDRAM Regulator
> Not connected

Figure 7. ATLAS UL REGULTAORS

ATLAS UL

Clock Generation:

Atlas Ultra Lite can generate a 32 kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Neptune requires for optimal performance, therefore, an external 32.768 kHz crystal is used. The 32 kHz oscillator will run at all times. It is powered by RTC_BATT, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

## Figure 8. Atlas UL 32kHz Clock Generation
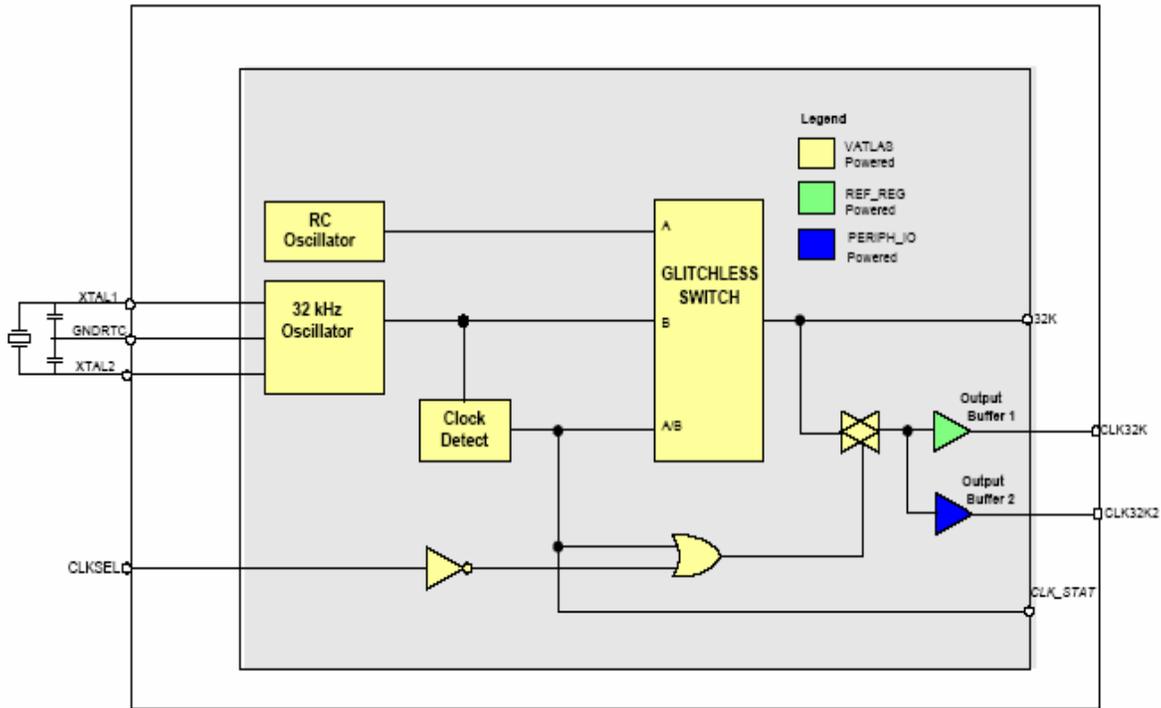
Atlas-UL TX Audio

The mobile phone supports an Internal Microphone (MICINM) and an external (headset microphone). The internal input is single ended with respect to VAG. The proper

The mobile phone supports two microphone input paths identified as Internal Microphone path is selected by the MUX controller and path gain is programmable at the PGA. The internal microphone is a single ended surface mount part the microphone is biased by MICBIAS1 of the Atlas UL IC. The signal is routed to the A3 amplifier. The headset microphone is connected through the EMU connector, the audio input and output paths of D+ and D- meet the requirements of CEA-936.

Figure 9 Atlas UL TX-Audio
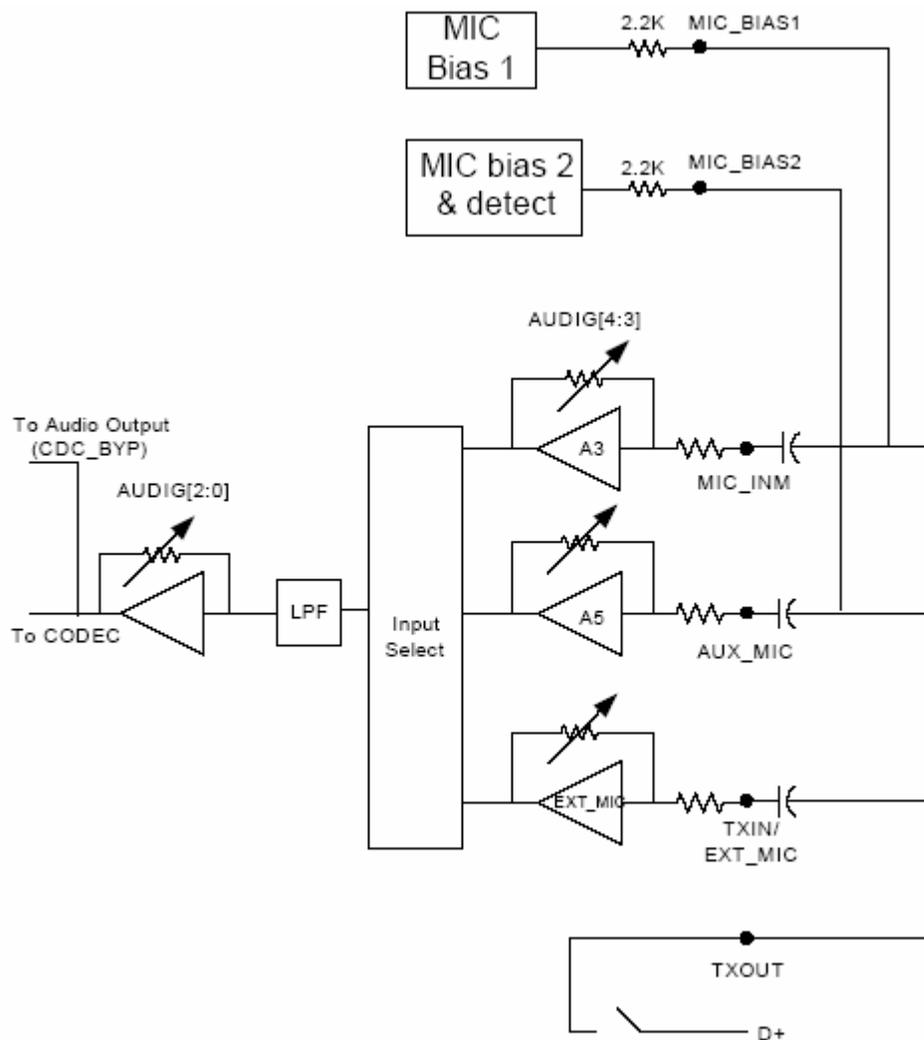
Atlas-UL RX Audio

The mobile phone supports three audio output paths. The output of Atlas-UL's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the three supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), and the CEA-936 output. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons. The Handset Speaker is driven by Atlas_UL's internal SPKR differential amplifier. Following the speaker path from the pins SPEAKERM and SPEAKERP are connected to the transducer. The headset uses a standard mini-USB connector. The headset may contain a momentary switch, which is normally open and connected to the USB ID line. When the momentary switch is pressed, the ID line is shorted to ground. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad. The Headset Speaker is driven by Atlas-US's internal USBAMP. The Alert Transducer is driven by Atlas-UL's ALERT/Speakerphone amplifier (A1). The alert path from the PCAP pins ALRT and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed to the inverting input of the alert amp A1.

Figure 10. Atlas-UL Telephone CODEC
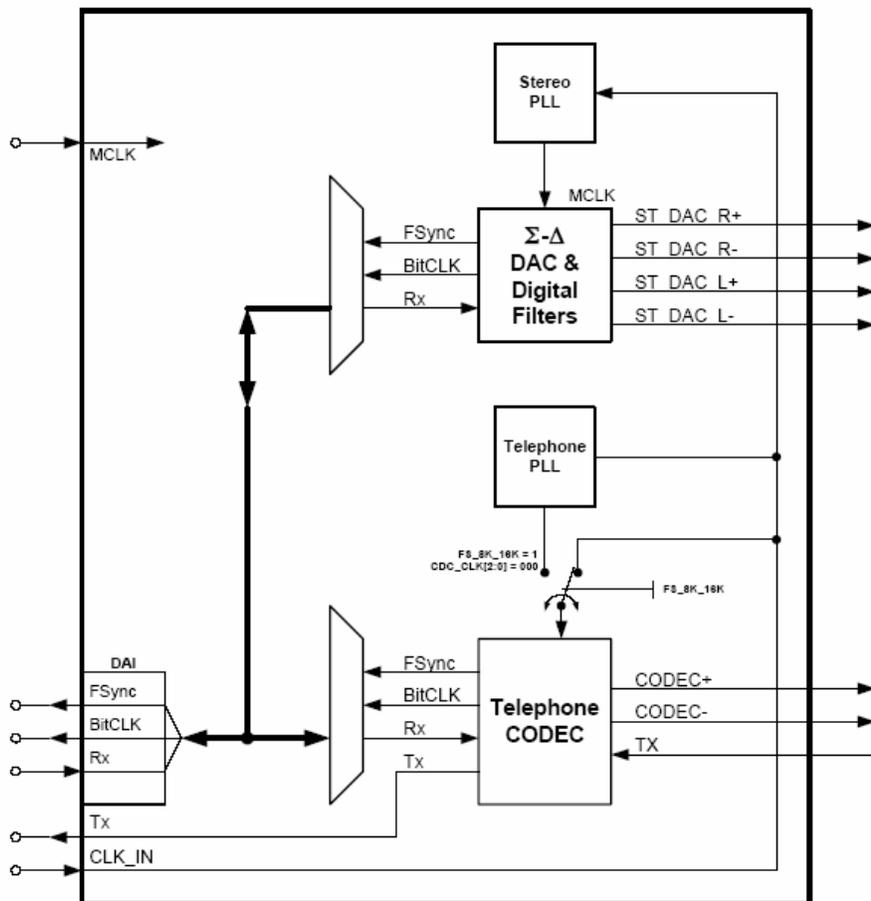
Battery Interface

Batteries interface to the main transceiver board via a 4-pin connector. Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback. During normal phone operation, without a charger attached, Q904 is turned ON so that current can be supplied from the battery to the BP power node on the transceiver board. When the phone is 'ON', the Atlas-UL IC will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the Atlas-UL IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to BP to minimize 'OFF' state leakage current. Lithium Ion/Polymer charging is internally supported in the phone. Mid-rate charging is supported when a valid mid-rate charger is detected on the accessory interface connector. During mid-rate charging, Q905 & Q906 are turned ON so that current can be supplied from the external source to the Battery. Q904 will remain on to allow current flow from the battery terminal to BP, the radio will be operating in "current sharing" mode when a charger is present. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q905 and Q906. A sense resistor provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high. Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface. Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 11. Charger Block Diagram
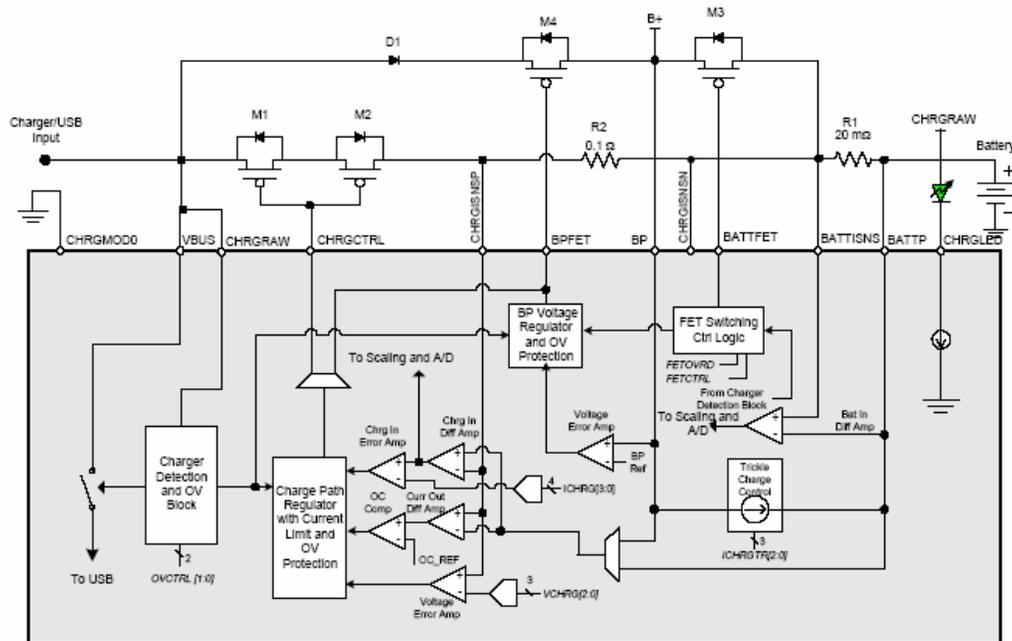
Neptune LTE2

The Neptune LTE2 Baseband IC is a digital baseband processor for the 2.75G GSM Market. The design is derived from Neptune LTE with changes to memory configuration and several module enhancements. It is a dual-core processor that contains a Synthesizable Onyx DSP core (56600), an ARM7TDMI-S microcontroller, and custom peripherals. The Neptune LTE2 IC is derived from the Neptune LTE

IC with the following key changes:

• Addition of Platform Independent Security Architecture (PISA) modules:
     — Security Controller (SCC),
     — Memory Separation Unit (MSU)
     — HASH Accelerator (HAC)

• On-chip memory:
     — Changed MCU RAM size from 436Kbytes to 512Kbytes for GPRS production version, 256Kbytes for EDGE production version
     —Decreased MCU ROM size from 3168Kbytes to 1792Kbytes
     — Increased DSP X, Y, and P RAM and ROM sizes to support new features including EDGE.

• Addition of OWIRE peripheral to support removable battery

• Addition of 2nd UART to support e.g. optional applications coprocessor

• Pin and GPIO muxing changes including
     — parallel DMAC
     — dedicated BBP transmit pins for interface to external EDGE transmit IC

• DSP subsystem changes to support 130MHz required for EDGE

• Neptune LTE2 MCU "PIG" peripheral bus has been omitted. All "PIG" peripherals are now accessed through the "IP" peripheral bus, and their base addresses have been changed (internal register organization remains the same).

Figure 12. Neptune LTE Functional Block
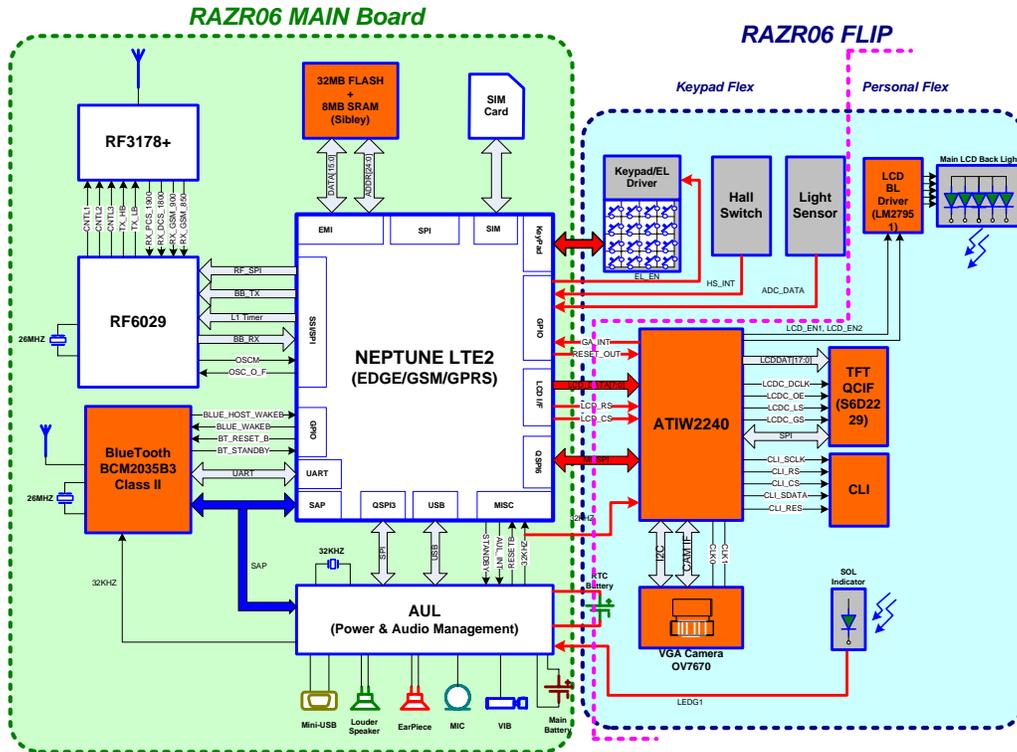
Memory Interface

The portable will be using a memory stacked part containing a 256Mbit Burst Flash die and a 64Mbit PSRAM die. The portable products will be operating at 1.8V core voltages and will have a 1.8V interface to Neptune LTE2.

Neptune LTE2's AEIM will be interfaced to the stacked memory device and consists of the external address lines, data lines, chip selects, and memory control lines.

Keypad Interface

The Keypad Port is a 16-bit peripheral, used generally for keypad matrix scanning, or as a GPIO port up to 16 bits wide. The keypad matrix can be configured up to 8 rows by 8 columns, with unused pins as GPIO's. For this phone, the keys are mapped as specified in the Synergy keypad matrix. All rows shall be set as inputs at all times. Columns shall be set as outputs driven low when there are no key presses detected. Pressing a key will short a row to a column driving the row low and generating an interrupt to the processor. At this point, all columns will be set as inputs and progressively scanned low (set as an output driven low in a sequential fashion with only one column driven low at any point in time) to determine the key that is pressed.

SIM Interface

The SIM interface block is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards. The card itself stores important information including the subscriber telephone number, phone numbers, the users' PIN, and other information to be able to complete a phone call. The card holds all this information for the user and therefore must be protected from electro-static discharge that could destroy the card. We prevent this event by also requiring the user to attach a battery. Batteries on Motorola product are arranged in such a way to fully cover the SIM block. The SIM block has two ports that can be used to interface with the various cards. The interface with the MCU is a 16-bit connection via the AIPI Controller and the IP-Bus Interface. Figure 13 shows the signals and direction of propagation between the different device modules.

ATLAS UL can supply the SIM block with either 1.875 V or 3.0 V. The bit VSIM_0 determines the voltage. This is bit number 18 in the AUX_VREG register (location 07). The 5 V SIM cards are not supported with this architecture. The VSIM regulators on and off state will be controlled by one SPI bit (VSIM_EN) and one external pin (SIM_VCCEN). SIM_VCCEN is a pin on Neptune that connects to the VSIM_EN pin of ATLAS UL. The SIM regulator will be on only when the SIM_VCCEN pin and the VSIM_EN SPI bit are logic high. The voltage supply to the card must be shut down before the SIM card is removed and the card loses contact with the radio. Because of the nature of the removable SIM card the SIM regulator must be able to withstand a short circuit at its output without sustaining any damage. The SIM module contains a block designed specifically for generating the clocks used internal to the SIM module, and the clocks provided to the SIM cards. There are no interrupt sources generated by the SIM clock generator block. The SIM Transmitter block contains a transmit state machine, transmit shift register, and a transmit FIFO. The SIM Receiver block contains a receive state machine, receive FIFO, and control logic. On power up, the phone checks for connected accessories and for the validity of battery voltage. If the battery voltage is valid then the SIM Card is secure and the phone attempts to read data from the SIM on the SIM_I/O line. If no data is read then that indicates that a card is not present and S/W should write "CHECK CARD" to the display. The SIMPD input allows for detection of the insertion or removal of a SIM card. A mask-able interrupt can be generated when a SIMPD event occurs. An internal 69k pull-up is present on the SIMPD pin for Neptune. This will provide for a high to low transition on the SIMPD pin when a SIM card is removed. The SIM port control block contains hardware that provides the correct sequence to power down a SIM card. The software must perform the power-up sequence.

The power down sequence is:

RST transitions from high to low

CLK is turned off to a low

I/O transitions from tri-state to low

SIM Vcc is turned off

The SIM module is capable of forcing a SIM card power down. It is similar to the auto power down feature, except that it is not dependent upon either the state of the SIM card auto power down enable bit, or triggering of a presence detect event.

Figure 13 SIM Interface
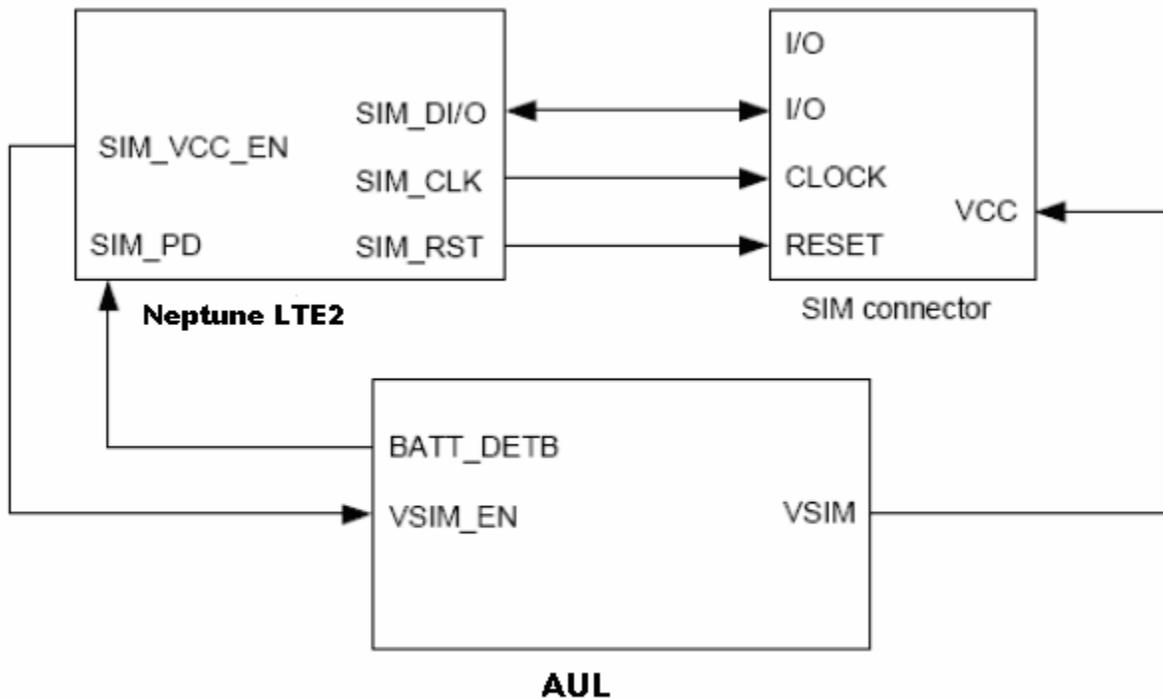
Flip Interface

The Flip Display Module functions as a core display subassembly that also supports an external Caller ID (CLI) display in 96 x 80 4K CSTN LCD format. The Camera interface is a board to board connector designed to mate with the VGA camera module. Four white LEDs provide the backlight for the main display..The Bluetooth LED is sourced by VBOOST and sunk by LEDB1. The Sign Of Life/Charger LED is sourced by VBUS and sunk by LEDG. The flip is connected to the topside of PCBA via the flex , using board to board connector.

FIGURE 14. FLIP INTERFACE MODULE
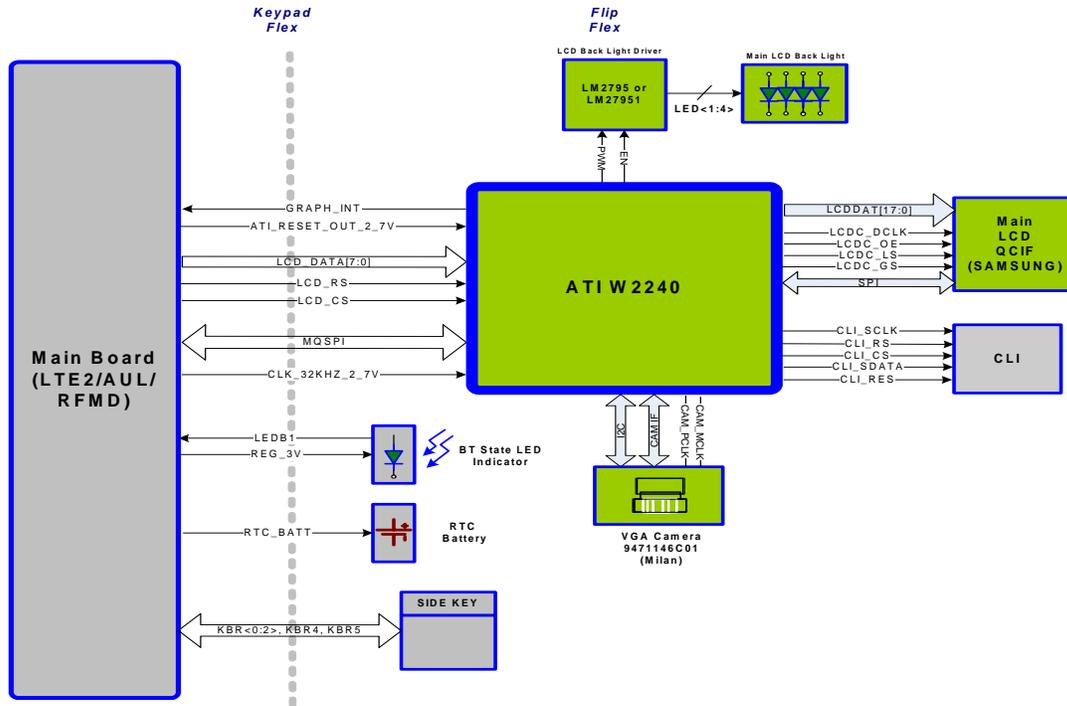
Bluetooth version 1.2 Class 2 Module

The HCI interface will utilize an UART. There are two data signals (TXD and RXD) and two flow control signals (RTS and CTS). The BT module assumes a role as DTE and the Neptune LTE2 acts as a DCE. Therefore when the BT module is connected to Neptune LTE2 the RXD and TXD lines must be crossed, while CTS and RTS on Neptune connect directly to CTS and RTS on the BT module. RXD and TXD have been crossed on the BT module already; therefore, BLUE_TX of the BT module is connected to TXD2 and BLUE_RX of the BT module is connected to RXD2 on Neptune LTE2 257 pin package. The Bluetooth UART is a dedicated UART from Neptune LTE2. This bus is not shared with external peripherals. Although most signaling is done over the HCI, wakeup signaling is done with dedicated signals. Neptune LTE2 uses a GPIO to wake up the BT module.

The BT module uses a dedicated signal BLUE_HOST_WAKEB connected to a Neptune LTE2 interrupt to wake-up the host processor. The codec is connected onto a shared 4 wire bus with Neptune LTE2 and Atlas referred to as the BB_SAP (Base Band Serial Audio Codec Port). The Atlas acts as the master and provides the clock and frame sync signals for the bus. The labeling on the Bluetooth module is in reference to the Neptune LTE2. Therefore, the ASAP_TX line is an input and ASAP_RX is the output from Bluetooth. Bluetooth is reset in a number of different ways. When software first initializes Bluetooth, it sends an HCI reset command over the UART interface to place the BCM2035 into a known state.

If software fails to detect a response to the initial HCI reset command, it will power cycle the RF and Core voltages thus forcing a power on reset on the BCM2035. Additionally, Neptune LTE2 can reset Bluetooth using the RESET_OUT signal. A level shifted version RESET_OUT at 2.775 V is connected to RESET_N of the BT module. RESET_N is active low. This option would be used when the software initiates a soft reset, but power

supplies or the main RESETB signals are not asserted. The Broadcom chipset requires two different frequency references, a lower frequency low power reference (32.768 kHz), and a high frequency main reference (15.36 MHz, 26 MHz, etc.).

The low power reference is a standard frequency available on the GSM phone whenever the phone is powered. As such, this reference is directly connected to CLK_32KHZ, the buffered port from the oscillator on PCAP. As this module will be primarily used on GSM platform, PLL components on the module were tuned for 26 MHz with the intent to share the crystal frequency oscillator of the phone, Neptune LTS XTAL OSC. Unlike the low power reference, the Neptune XTAL OSC, is not available all the time and does not provide a dedicated buffered output. When Bluetooth requires this reference when being paged, it must wake up its host processor (Neptune LTE2) if it is in deep sleep.
When the Bluetooth switches to the main reference it should not disturb the Neptune LTS XTAL OSC circuit in regards to frequency, or noise performance, thereby dictating some amount of isolation or buffering. This option uses a 2.5 x 3.2 mm discrete 26 MHz crystal with two shunt capacitors (15 pF).
The XTAL circuit oscillator is contained on the BCM2035 and enables itself without any control from the host processor. The host processor, though, must program a trim value to the Bluetooth module via an HCI command every time the Bluetooth module is POR. This trim value is programmed in the phone's SEEM at the time of factory phasing. CKO is a multiplexed clock output available from LTE2. Software will need to program Neptune LTE2 to configure the CKO pin to use this uncorrected clock on every POR. Enabling signal for this option will be via the BLUE_CLK_ENB signal which is connected to interrupt INT2 of Neptune LTE2. Software will also provide a trim value to the Bluetooth module on every POR as with the case for the discrete Oscillator Buffer described above.

Figure 15. System Block Diagram