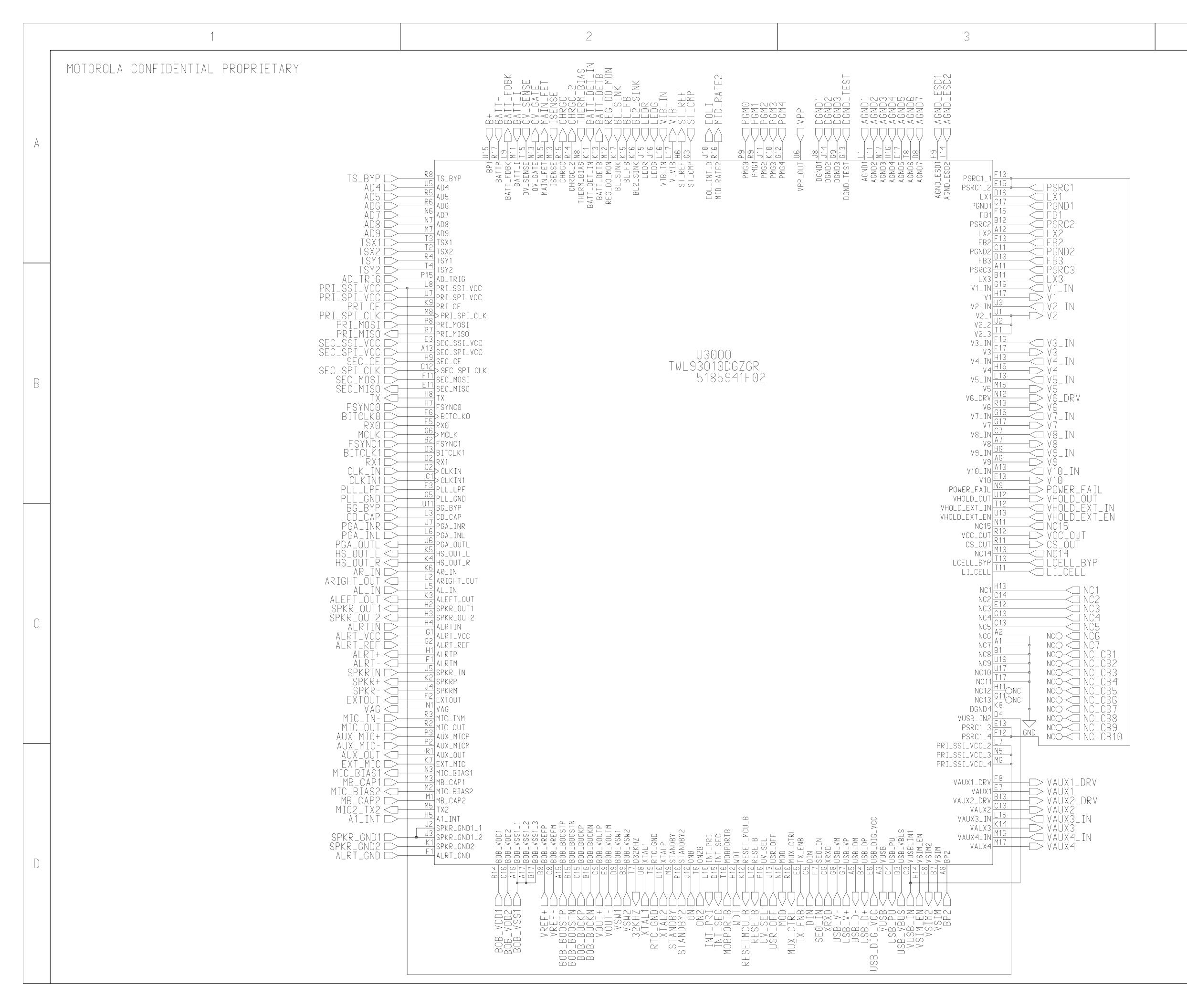
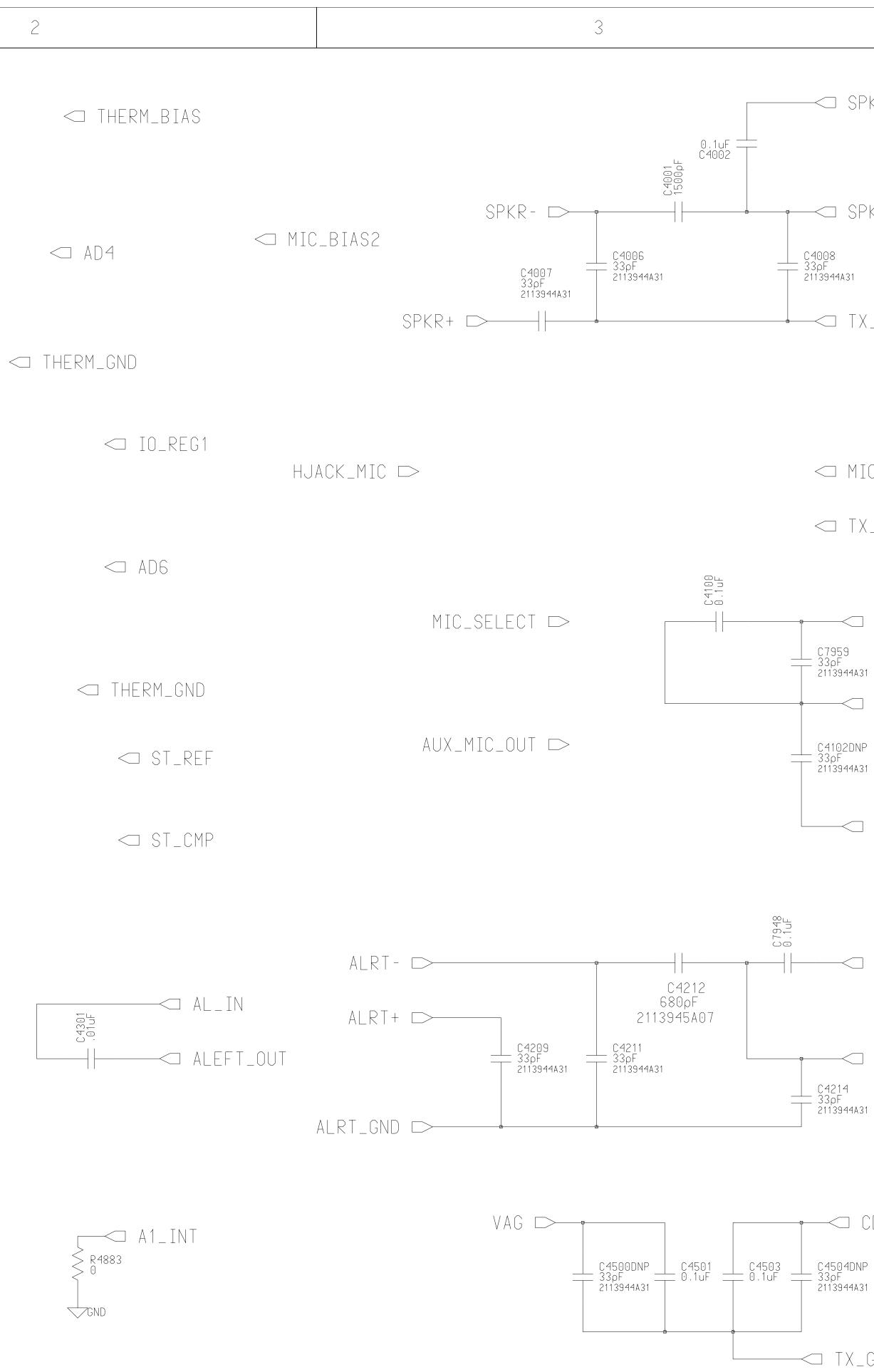


A 1 3 A Engineer: Rajesh Verma Drawn by: Rajesh Verma R&D CHK: DOC OTDU CUK: C C D D C N C	<b>A</b> <i>I</i> <b>NC</b> . Size: 11x17
R&D CHK:   TITLE:	Size;
DOC CTRL CHK: $\Box$	
MFG CTRL CHK: Top Level	ge: Of:
QA CHK: W16748 Changed by: Tuesday, December 21, 2004	Time: 3:27:32 pm

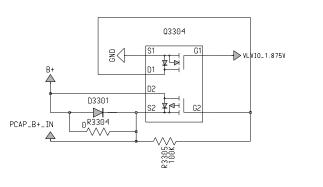


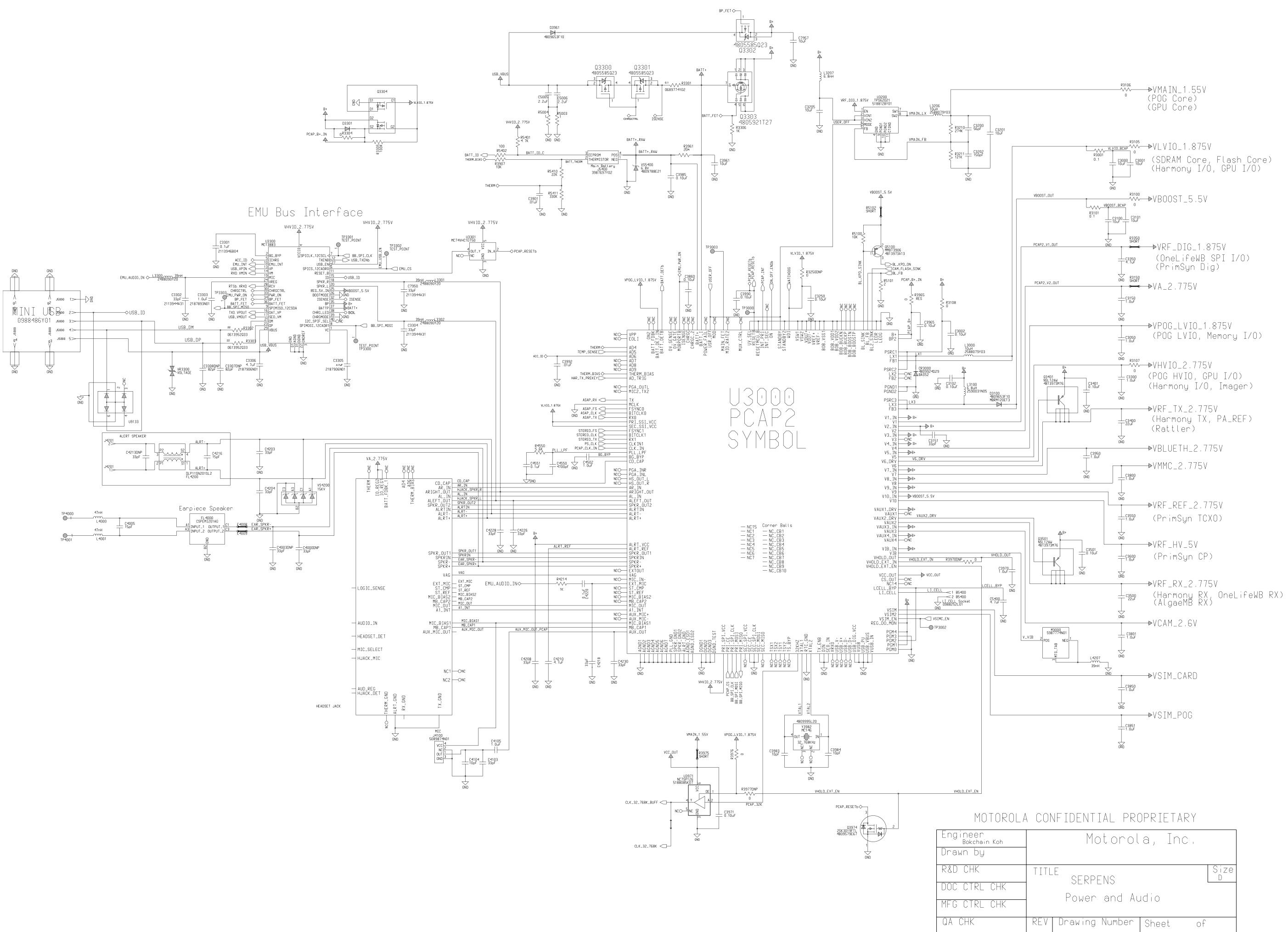
	4	
Engineer: Drawn by:	A MOTOROLA	INC.
R&D CHK:	TITLE: V980 / V975	Size:
DOC CTRL CHK:	PCAP	
MFG CTRL CHK:		
QA CHK:	REV: Drawing Number: Page: P9 8488453Y07	Of:
Changed by:	Date:	Time:

	1		
A	MOTOROLA CONFIDENTIAL PROPRIETARY AUDIO_IN 🕞	THERM	
		<pre>LOGIC_SENSE</pre>	
В		⊂ TX_GND BATT_FDBK_1 ▷	
С		HEADSET_DET	
	In case Audio Module is used:	AR_IN ARIGHT ARIGHT	ſ_OUT
	RX_GND NC1 NC2	AUD_REG 🕞	
D		HJACK_DET 🕞	

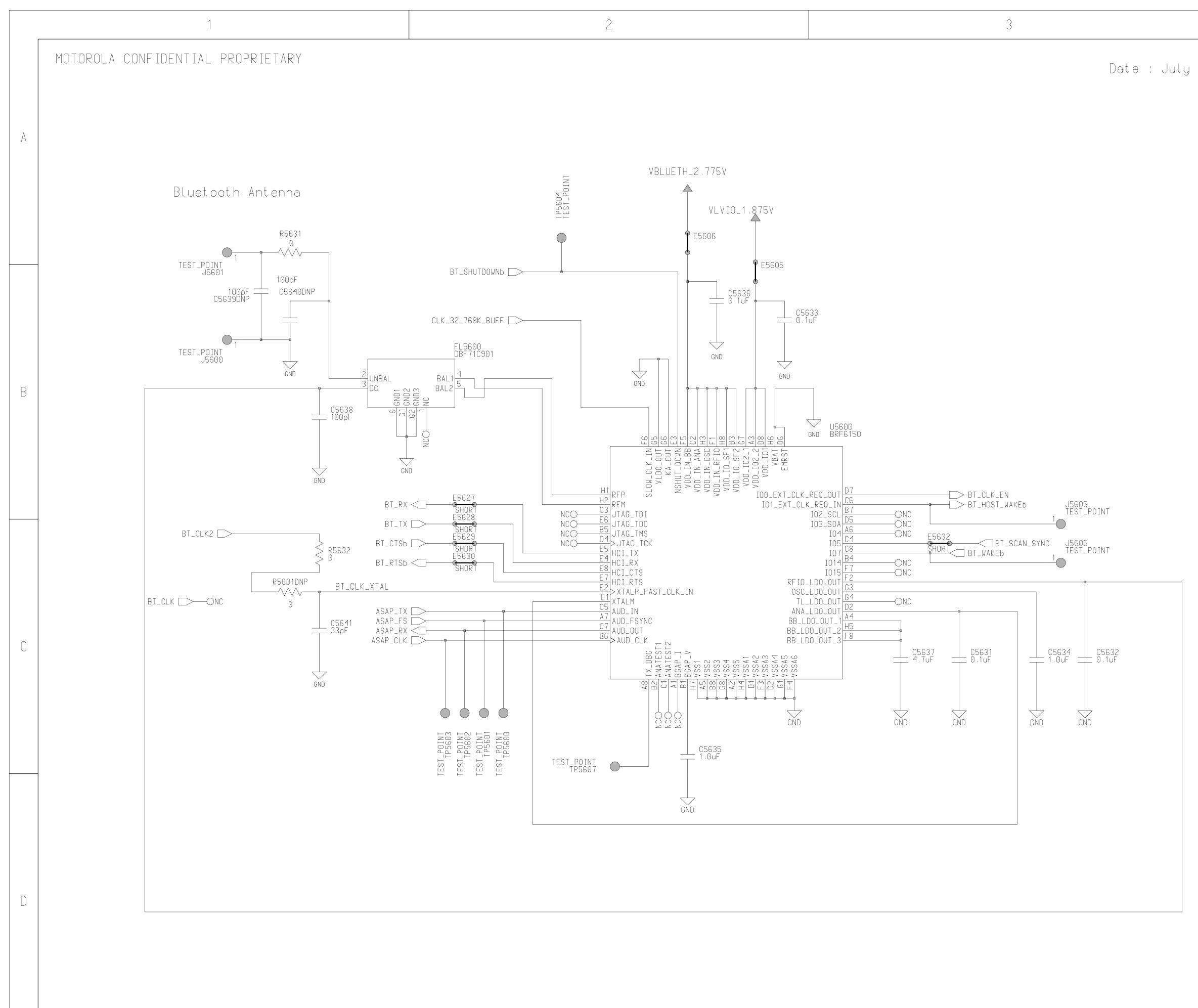


		4	
	Engineer:	A MOTOROLA	
°KR_OUT1	Drawn by: R&D CHK:	))	Size:
	DOC CTRL CHK:	TITLE :	
	MFG CTRL CHK:		
°KRIN	QA CHK:	REV: Drawing Number: Page:	Of:
	Changed by:	Date:	Time:
(_GND			
[C_OUT			
(_GND			
MB_CAP1			
1			
MIC_BIAS1			
D			
1			
TX_GND			
SPKR_OUT2			
ALRTIN			
1			
CD_CAP			
p			
1			
GND			

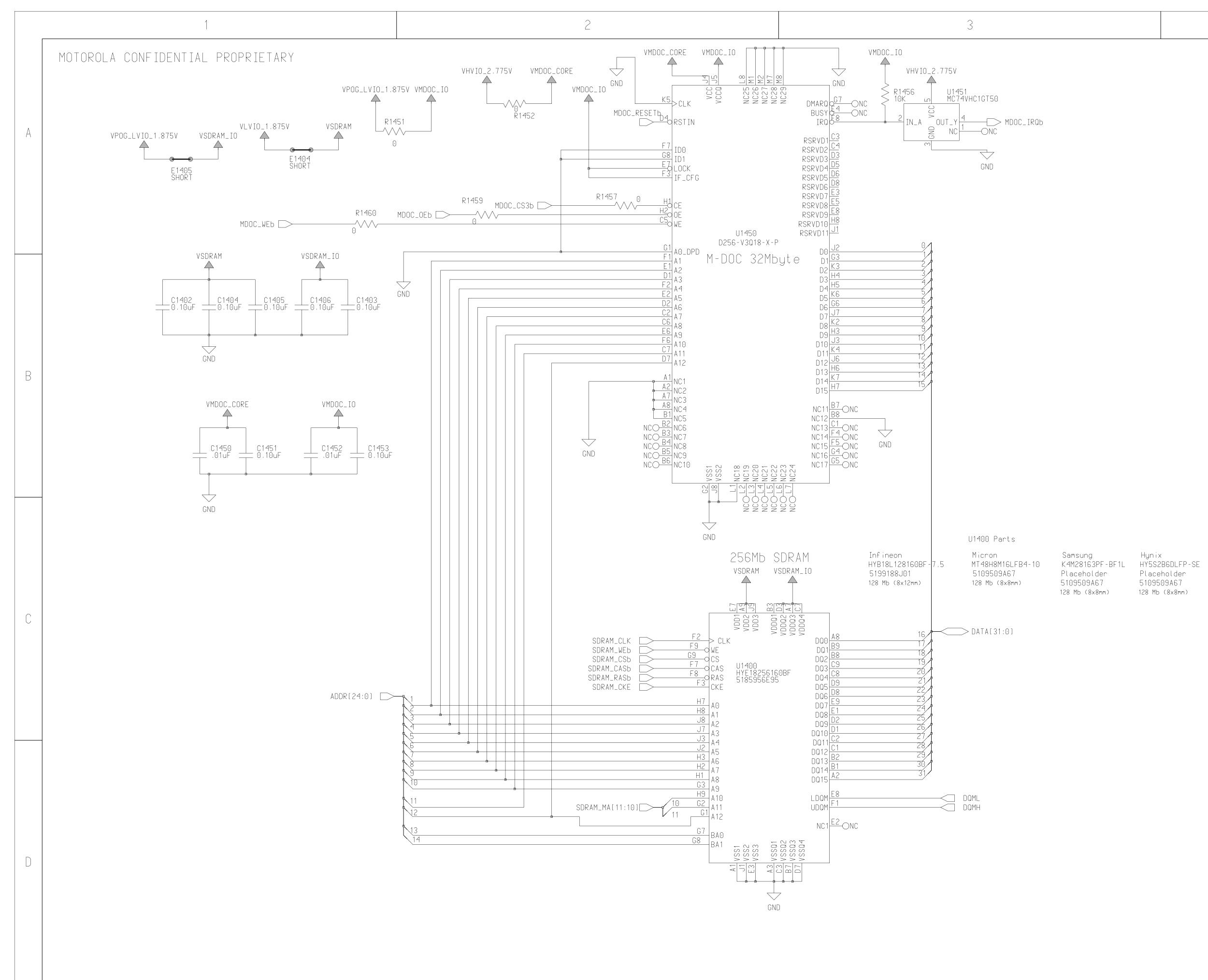




Motorol	a, Inc	× / 1
RPENS		Size
ver and Au	idio	
ing Number	Sheet	of

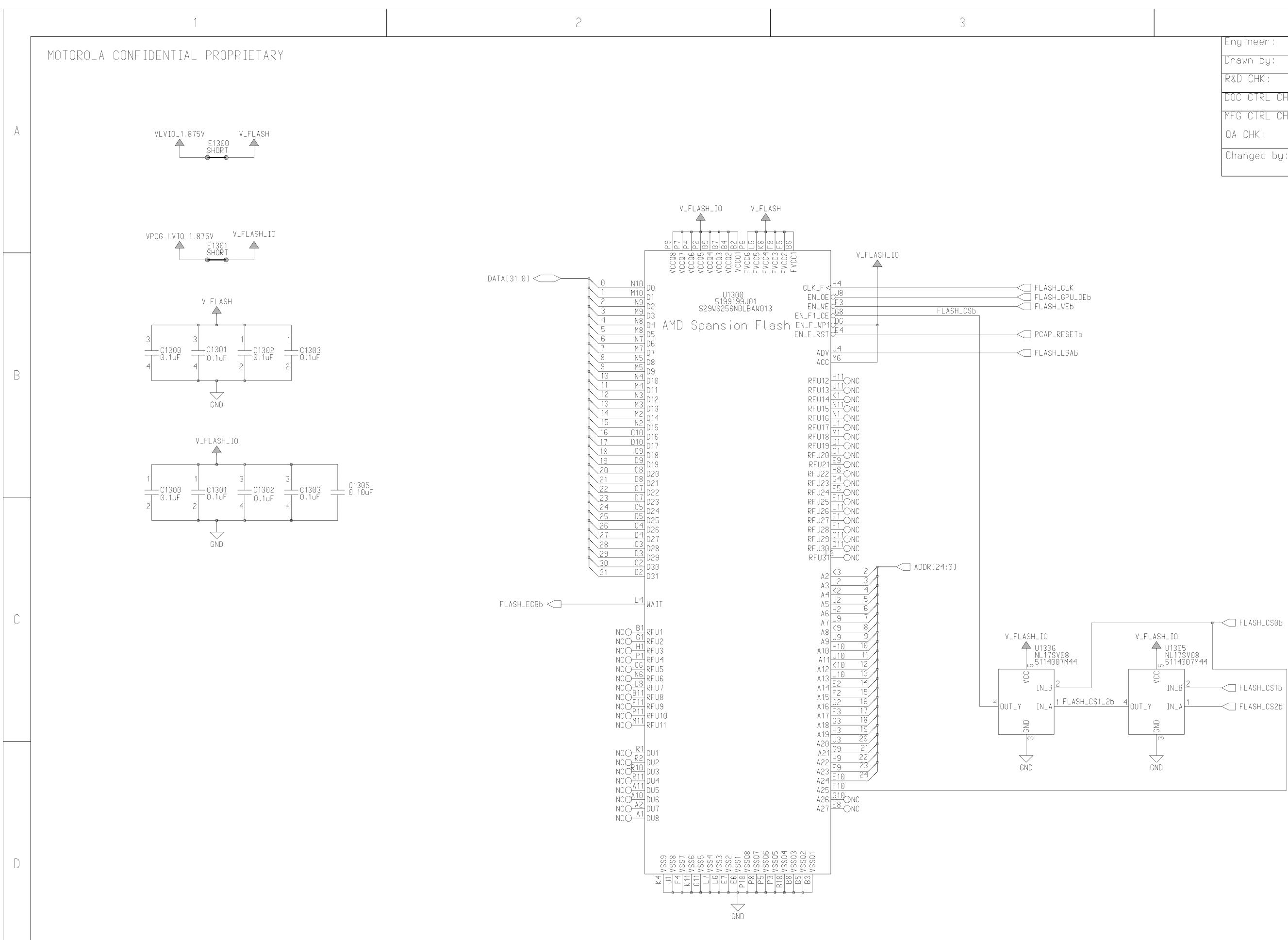


			4			
23, 200	1	Engineer: Bokchain Koh Drawn by:		MOTO	DROLA	INC.
,		R&D CHK: DOC CTRL CHK:	TITLE:	SERF	PENS tooth	Size:
		MFG CTRL CHK: QA CHK:	REV: [		nber: Page:	Of:
		Changed by: Rajesh Verma		te: ecember	22, 2004	Time:
			Updated	d Bluetooth	symbol to v3	12/22/04

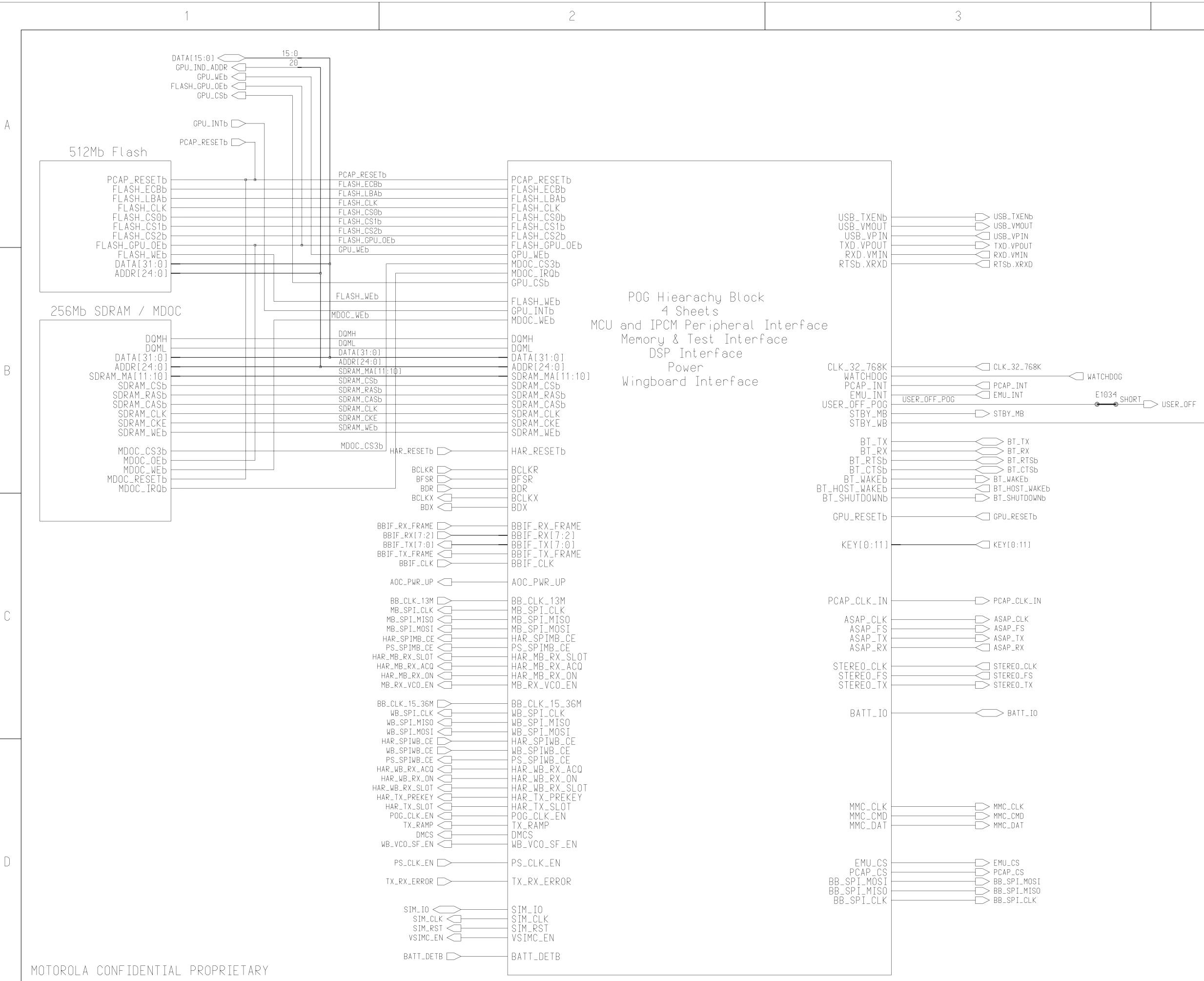


	4
Engineer: Drawn by:	A MOTOROLA INC.
R&D CHK: DOC CTRL CHK: MFG CTRL CHK:	TITLE: SERPENS SIZE:
QA CHK:	REV: Drawing Number: Page: Of: P9 8488453Y07
Changed by:	Date: Time:

Placeholder 5109509A67 128 Mb (8x8mm)



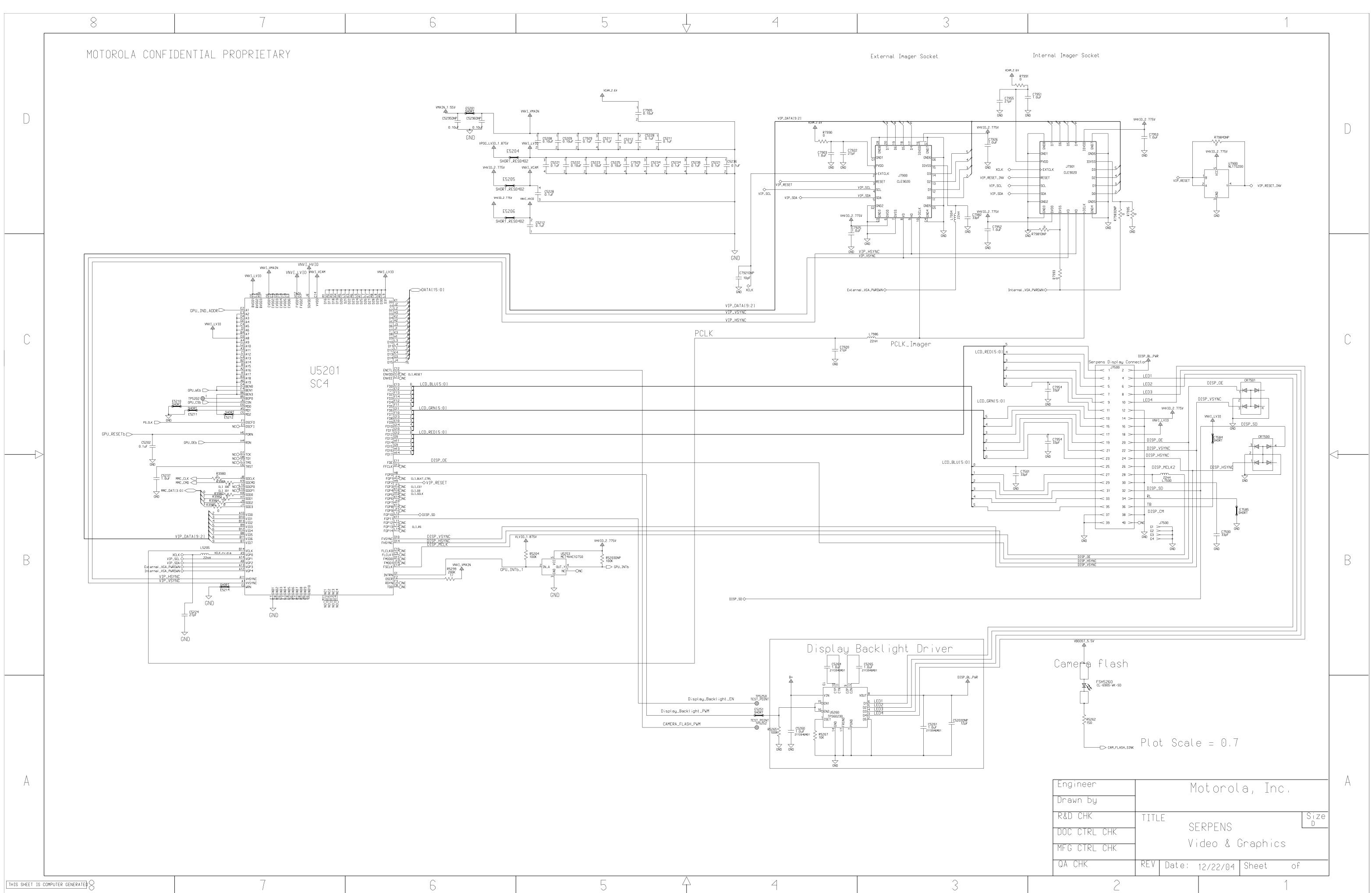
	4	
Engineer: Drawn by:	A MOTOROLA	INC.
R&D CHK:	TITLE: SERPENS	Size:
DOC CTRL CHK:	Flash Memory	
MFG CTRL CHK:		
QA CHK:	REV: Drawing Number: Page: P9 8488453Y07	Of:
Changed by:	Date:	Time:



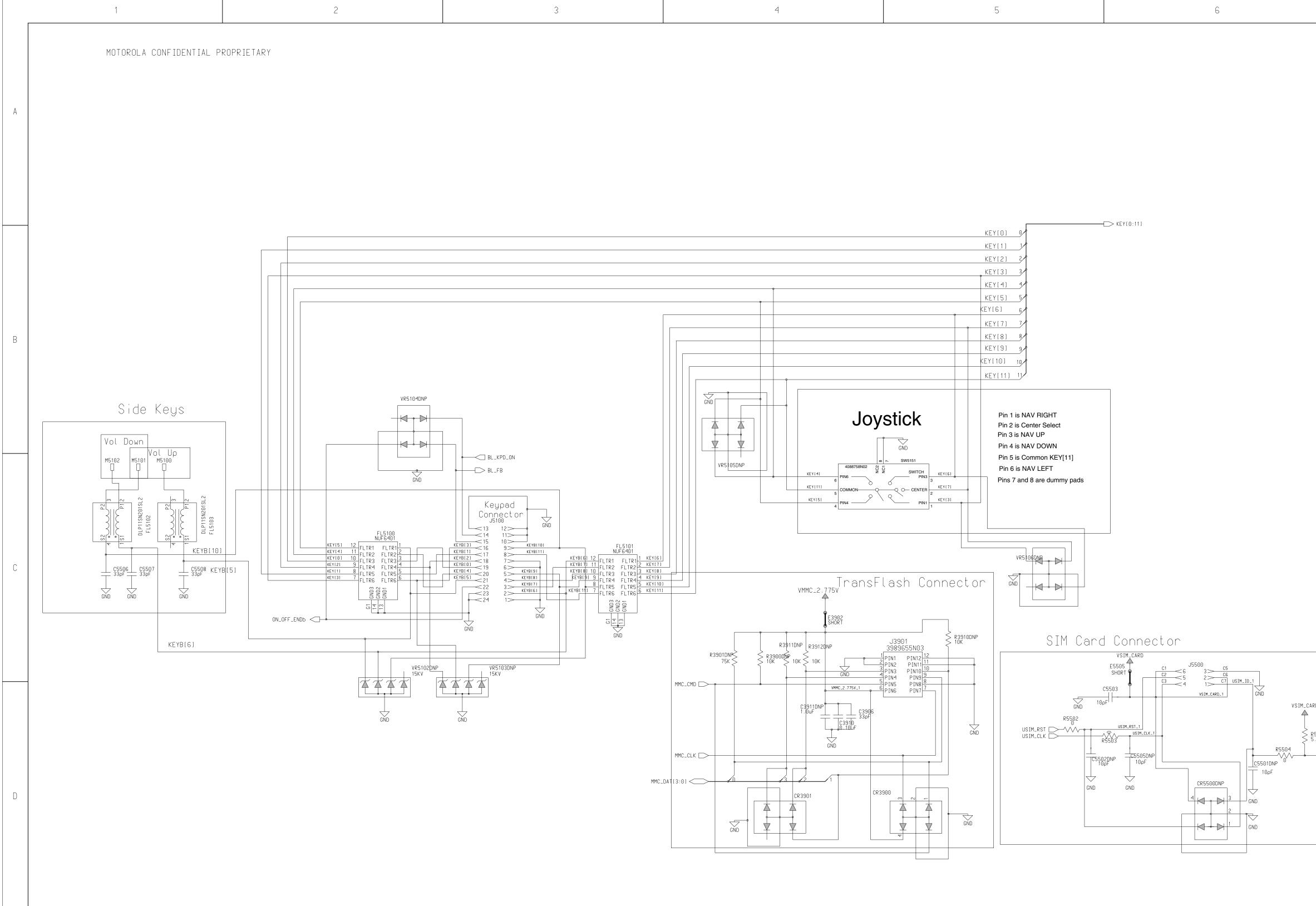
$\langle \rangle$	
$\smile$	

	4	
Engineer: Drawn by:	A MOTOROLA	INC.
R&D CHK: DOC CTRL CHK: MFG CTRL CHK:	TITLE: SERPENS POG & Memories	Size:
QA CHK:	REV: Drawing Number: Page:	Of:
Changed by:	Date:	Time:
Production U1019DNP R1038 R1032DNP U1020DNP	Development U1019 R1038DNP R1032 U1020	

T STBY\_WB Desense Cap  $\checkmark$ GND



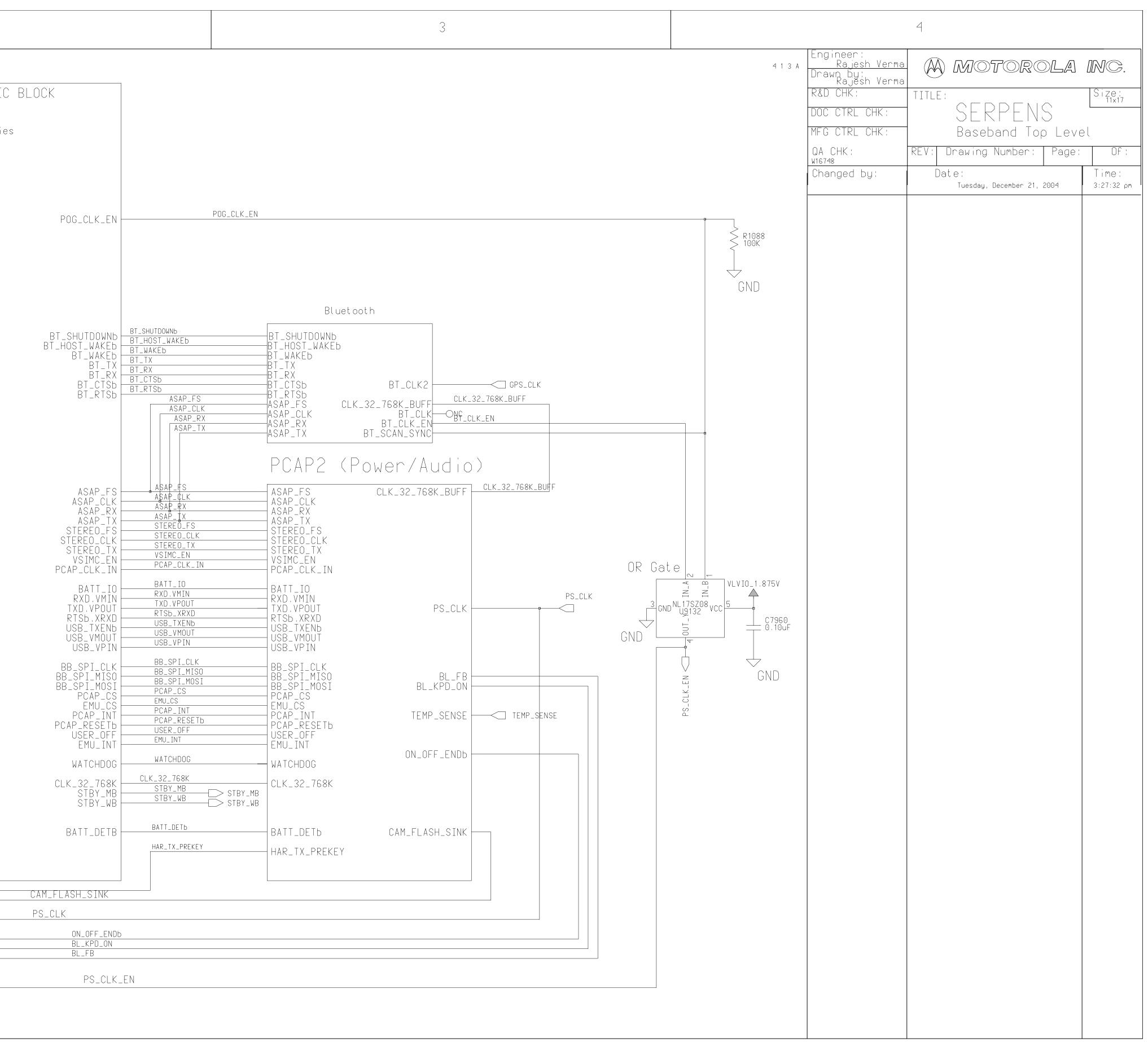
5	$\bigwedge$	4	3

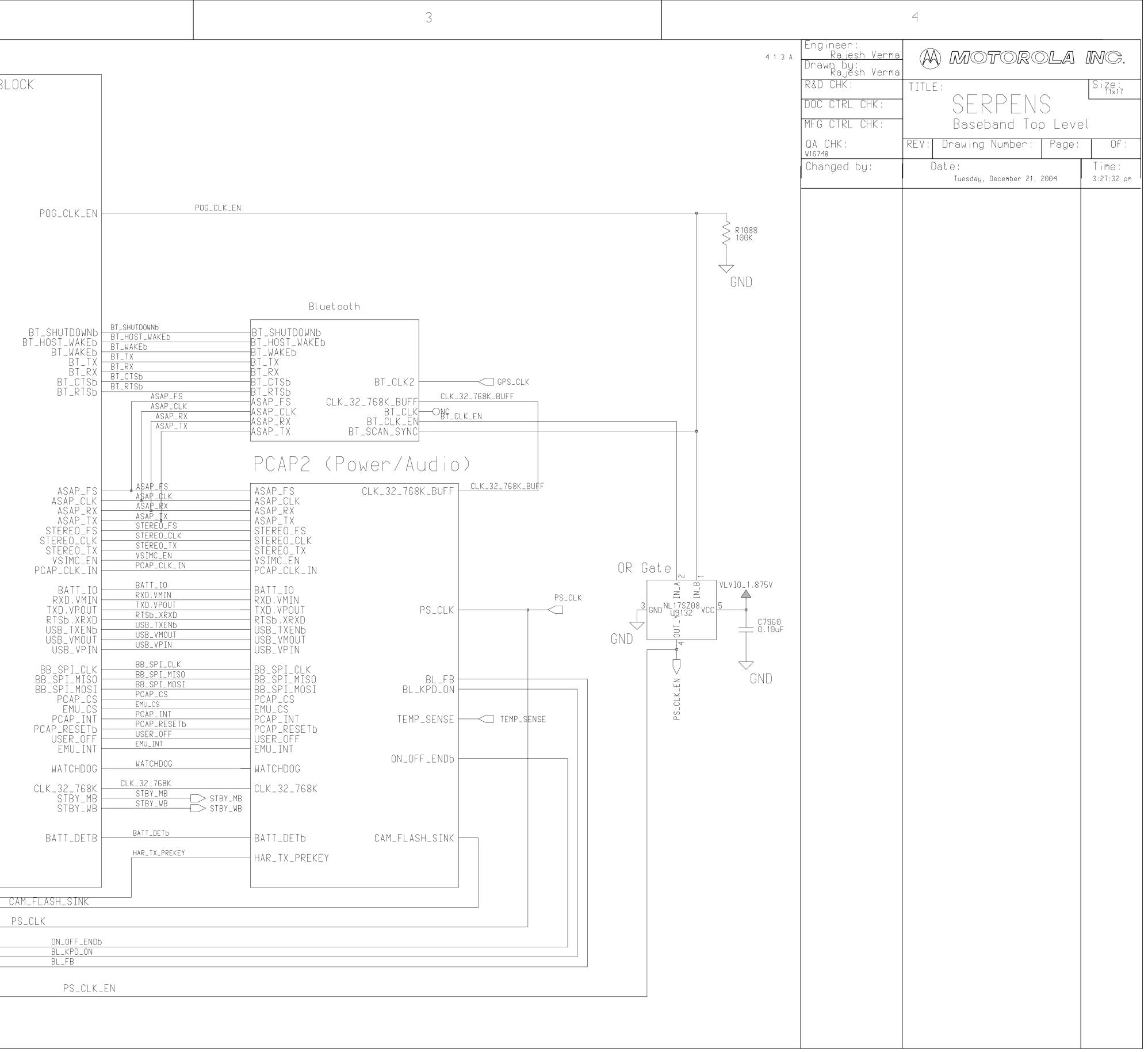


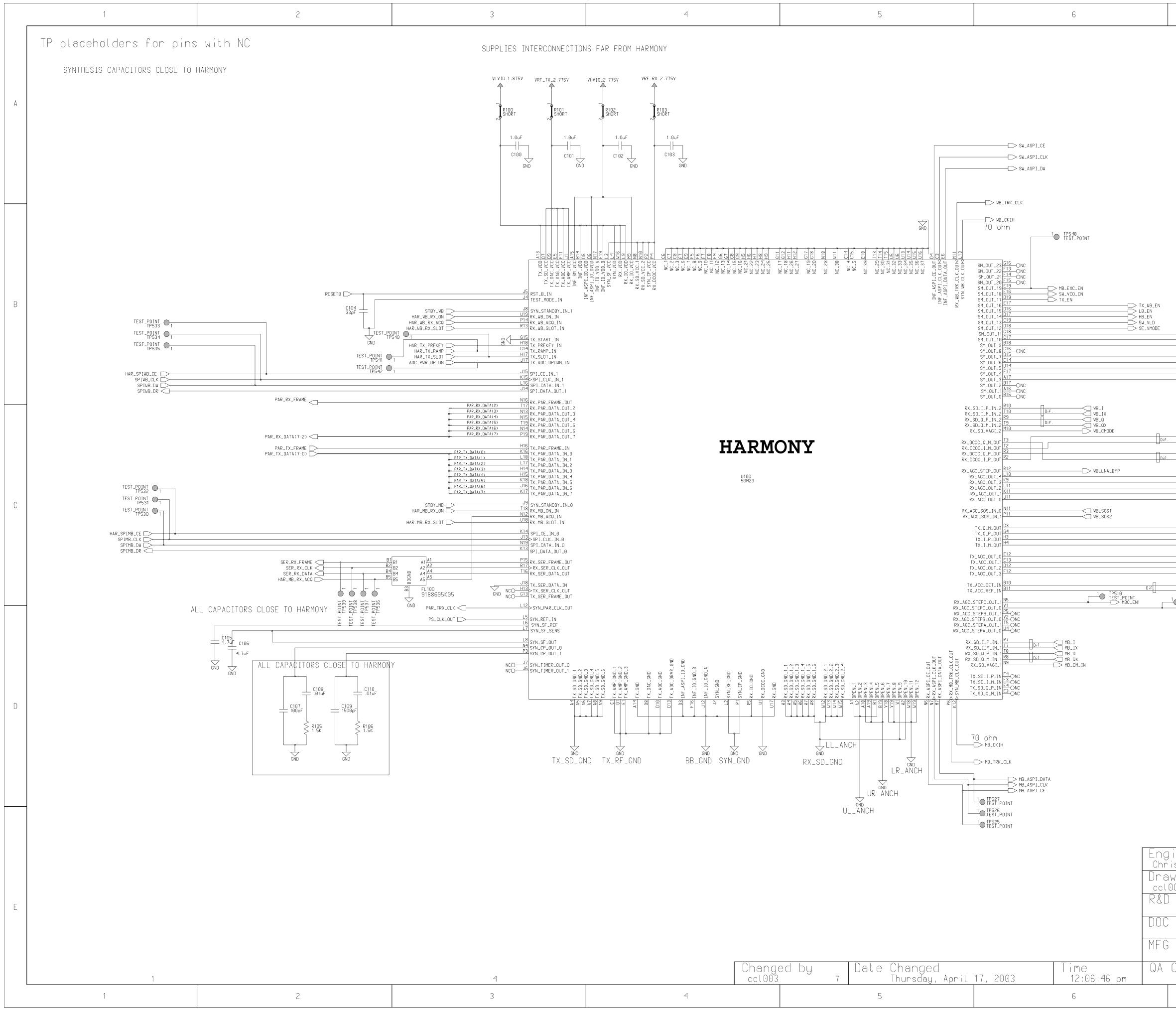
4	5	6

		7		8		
		4 1 3 A	Engineer: Rajesh Verma Drawn by: Rajesh Verma	A MOTOROLA	INC.	
			R&D CHK: DOC CTRL CHK:	TITLE: SERPENS	Size: 11x17	
			MFG CTRL CHK:	Misc. Connectors		
			QA CHK: w16748 Changed by:	REV: Drawing Number: Page: Date:	Time:	٨
				Tuesday, December 21, 2004	3:27:32 pm	A
						В
						С
					-	
RD						
25501 5.6K						
~	USIM_IO					
						D
						U
	]					

	1			2
MOTOROLA CONFIDENTIAL PRO	PRIETARY	MMC_DAT[0] MMC_CMD	Γ	
	Misc Connectors Keypad Connector USIM TransFlash	MMC_CLK	— MMC_DAT	OGIC 20G mories
	- BL_FB USIM_CLK BL_KPD_ON USIM_RST ON_OFF_ENDD USIM_IO - MMC_DAT[3:0] - MMC_CMD KEY[0:11] - MMC_CLK	USIM_CLK USIM_RST USIM_IO KEY[0:11]	SIM_CLK SIM_RST SIM_IO KEY[0:11]	
	Display & Imager Interfaces MMC_CLK DATA[15:0] MMC_CMD GPU_IND_ADDR MMC_DAT[3:0] GPU_CSb GPU_OEb GPU_WEb GPU_WEb GPU_INTb GPU_RESETb PS_CLK	DATA[15:0] GPU_IND_ADDR GPU_CSb GPU_OEb GPU_WEb GPU_WEb GPU_INTb GPU_RESETb	<ul> <li>DATA[15:0]</li> <li>GPU_IND_ADDR</li> <li>GPU_CSЬ</li> <li>FLASH_GPU_OEЬ</li> <li>GPU_WEЬ</li> <li>GPU_INTЬ</li> <li>GPU_RESETB</li> </ul>	
	- CAM_FLASH_SINK	HAR_RESETD BCLKR BFSR BDR BCLKX BDX TX_RX_ERROR BBIF_RX[7:2] BBIF_TX[7:0] BBIF_TX_FRM BBIF_CLK	HAR_RESETЬ BCLKR BFSR BDR BCLKX BDX TX_RX_ERROR BBIF_RX_FRAME BBIF_RX[7:2] BBIF_TX[7:0] BBIF_TX_FRAME BBIF_CLK	
		BB_CLK_13M MB_SPI_CLK MB_SPI_MISO MB_SPI_MOSI HAR_SPIMB_CE PS_SPIMB_CE HAR_MB_RX_ACQ HAR_MB_RX_SLOT HAR_MB_RX_ON MB_RX_VCO_EN AOC_PWR_UP BB_CLK_15_36M	BB_CLK_13M MB_SPI_CLK MB_SPI_MISO MB_SPI_MOSI HAR_SPIMB_CE PS_SPIMB_CE HAR_MB_RX_ACQ HAR_MB_RX_SLOT HAR_MB_RX_ON MB_RX_VCO_EN AOC_PWR_UP BB_CLK_15_36M	
		WB_SPI_CLK WB_SPI_MISO WB_SPI_MOSI HAR_SPIWB_CE WB_SPIWB_CE HAR_WB_RX_SLOT HAR_TX_SLOT HAR_WB_RX_ACQ HAR_WB_RX_ON TX_RAMP DMCS PS_SPIWB_CE WB_VCO_SF_EN HAR_TX_PREKEY	WB_SPI_CLK WB_SPI_MISO WB_SPI_MOSI HAR_SPIWB_CE WB_SPIWB_CE HAR_WB_RX_SLOT HAR_WB_RX_ACQ HAR_WB_RX_ON TX_RAMP DMCS PS_SPIWB_CE WB_VCO_SF_EN HAR_TX_PREKEY	
			PS_CLK_EN	

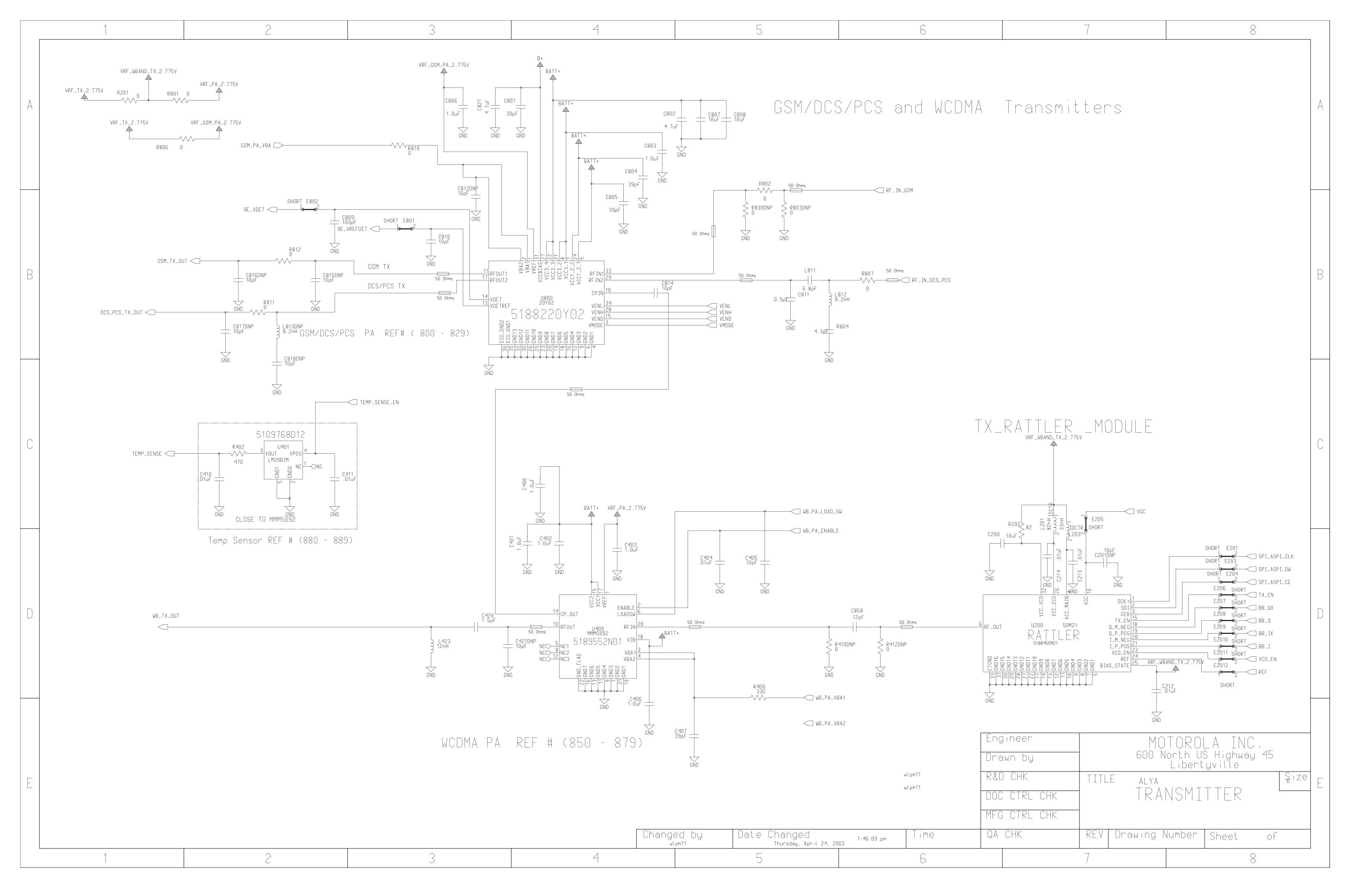






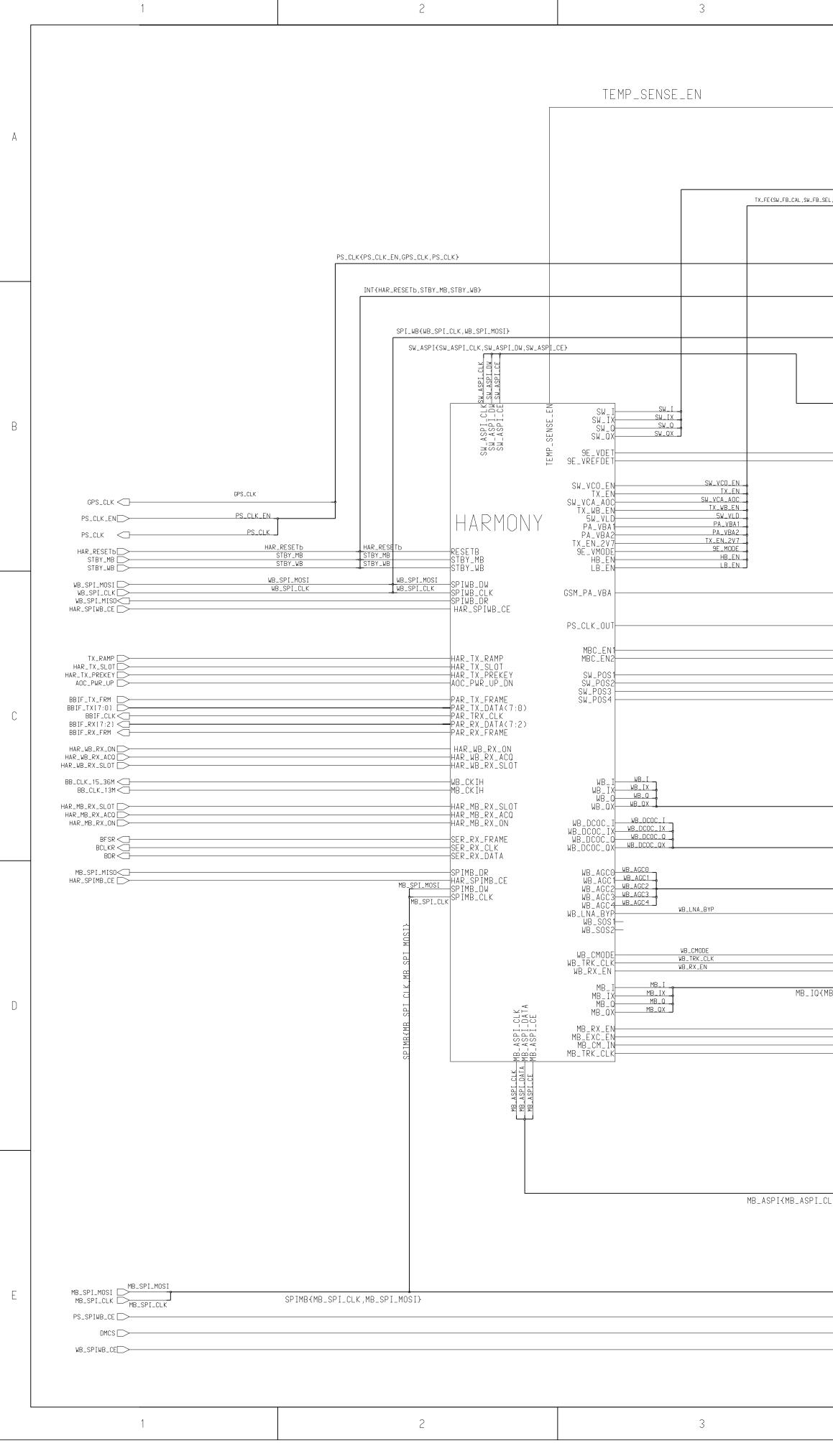
	4	5	6
) (	NS FAR FROM HARMONY		
	VHVI0_2.775V VRF_RX_2.775V		

	7	8	
			A
TX_EN_2V7 SW_POS1 SW_POS2	SW_POS3 TEMP_SENSE_EN SW_POS4 WB_RX_EN WB_RX_EN U9129 TEST_POINT		В
1         TP518 TEST_POINT           1         TP519 TEST_POINT           WB_DCOC_I         WB_DCOC_O           WB_DCOC_O         WB_DCOC_OX		1 TP515 TEST_POINT 1 TP512 TEST_POINT 1 TP511 TEST_POINT WB_AGC3 WB_AGC2 WB_AGC0 WB_AC0	С
TP509 TEST-POINT MBC_EN2			D
ineer is Leyh wn by 303 CHK CTRL CHK CTRL CHK CHK	MO 600 N TITLE HARMONY: ALY, REV Drawing N 1	A	ZeEE

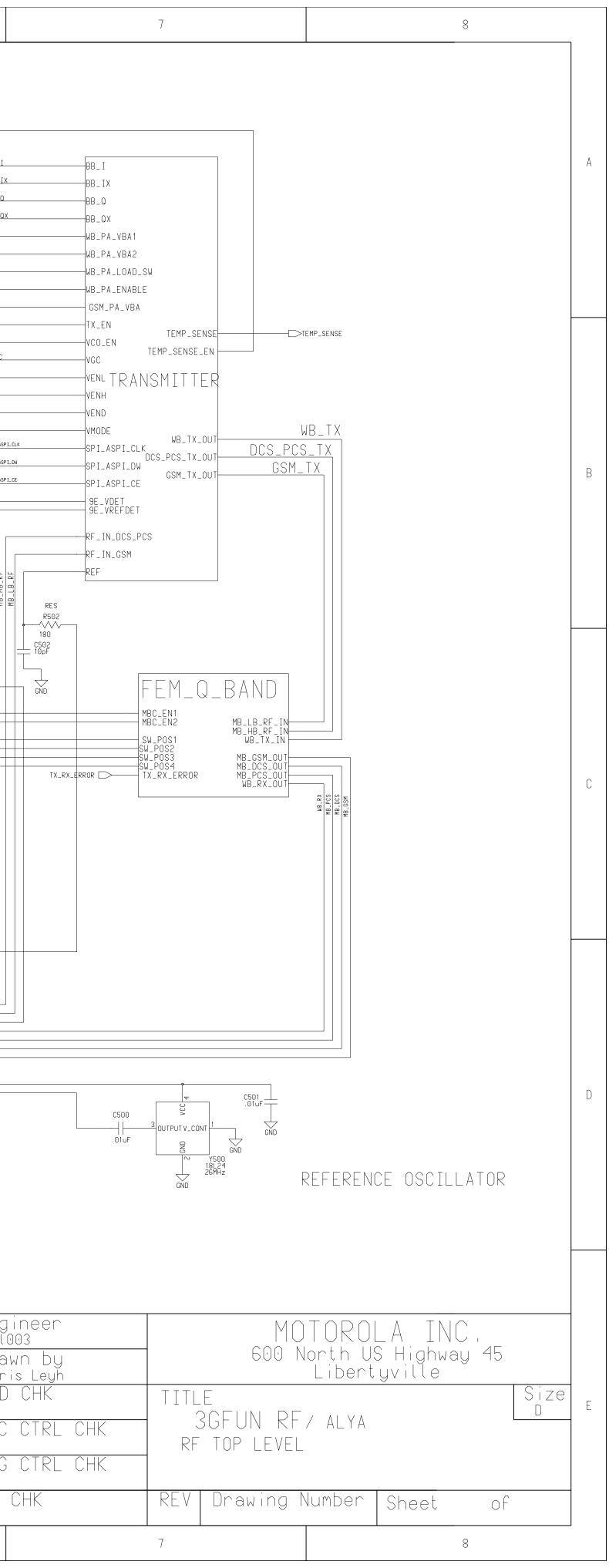


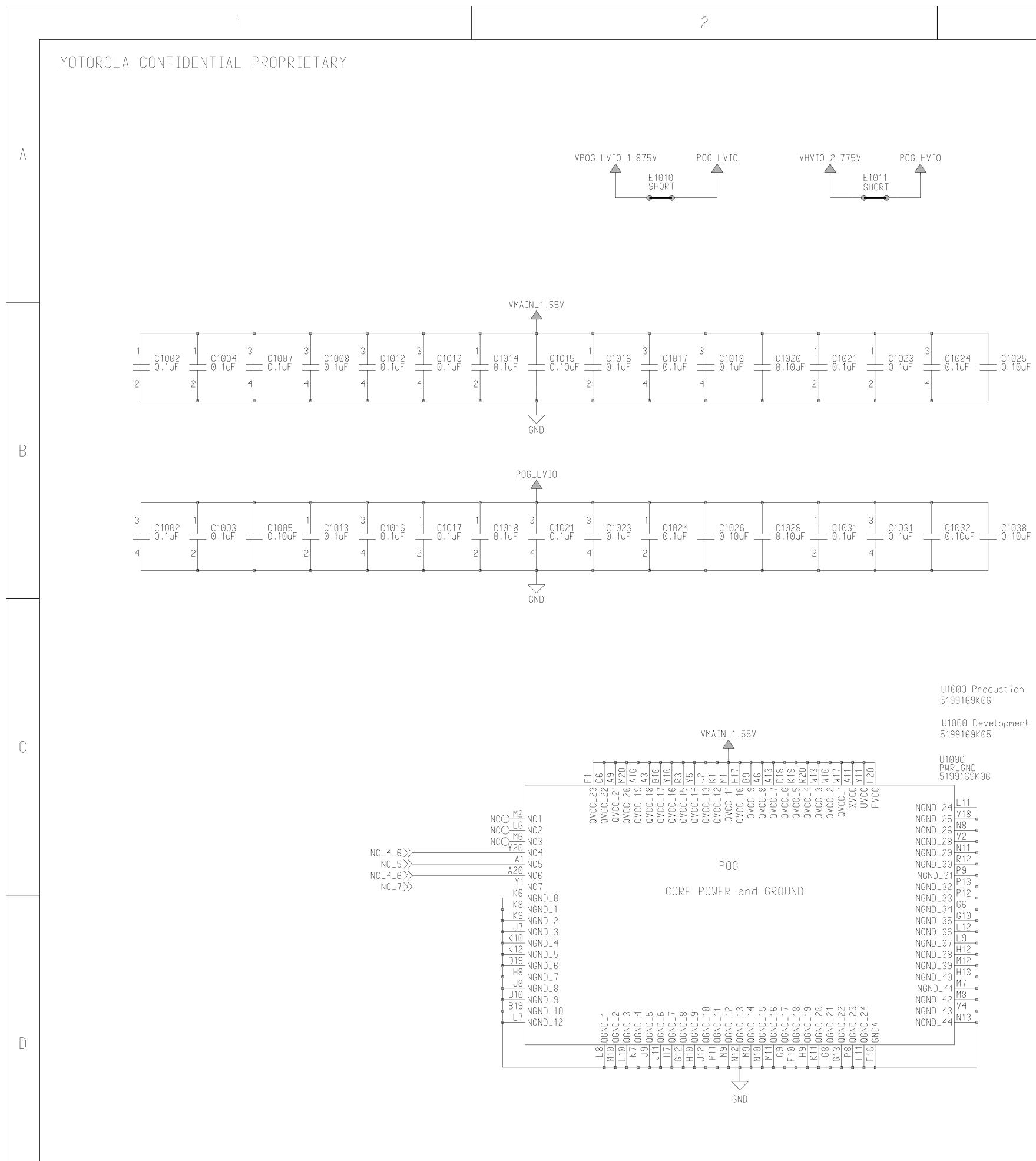
A TPs for test_1 & test_2	2	3 ORG,	a Blue Modu	le VERSIO	5 Do No N 2, 0	OT DELETE WB_DCS_IN XTAL_OUT WB_PCS_IN MB_GSM850_IN SW_VCO_FB_X		7	8	A
		T903 HHM1526	MB_DCS_IN_POS MB_PCS_IN_NEG MB_PCS_IN_NEG MB_PCS_IN_NEG MB_PCS_IN_NEG MB_DCS_IN_NEG MB_DCS_IN_NEG MB_DCS_IN_NEG MB_GSM900_IN_NEG		SER_TX_CLK DMCS MB_RX_VCO_EN TEST_POINT TEST_POINT TEST_POINT MB_ASPI_CE MB_ASPI_CE MB_ASPI_CLK MB_LB_RF_OUT MB_LB_RF_OUT MB_LB_RF_OUT CT933 C908 MB_HB_RF_OUT CT933 C908 MB_HB_RF_OUT CT933 C908 CT933 C908 C1932 C908	B41     MB-b5-12.NEG     WB-V       DT     GND15     WB_DC0C.       C1     MB_BB_0_POS     WB_DC0C.       C4     GND13     WB_DC0C.       E4     GND13     WB_DC0C.       C4     GND13     WB_DC0C.       C4     GND13     WB_DC0C.       C4     GND13     WB_DC0C.       C4     MB_ASPI_CE     WB_DC0C.       C4     MB_ASPI_CLK     WB_BB.       C5     MB_ASPI_CLK     WB_BB.       E1     MB_SF_OUT     WB_BB.       F4     WCC_MB_EXC     WB_BB.       F4     GND21     WB_BB.       WB_C5     WB_C7     WB_BB.       WB_C6     WB_C7     WB_BB.       WB_C7     WB_C7     WB_C7       WB_C7     WB_C7     WB_C7	AGC. 0 <u>C10</u> TEST. 2 <u>C11</u> TEST. 1 <u>D11</u> TEST. 1 <u>D11</u> TEST. 2 <u>C11</u> TEST. 1 <u>D11</u> TEST. 2 <u>C11</u> TEST. 2 <u>C11</u> TEST. 2 <u>C11</u> CND24 <u>F2</u> CND35 <u>L12</u> VCC. BB <u>E9</u> VCC. BB <u>E9</u> VB_0 VCC. CN <u>F8</u> CCC. VCC <u>F9</u> VB_0 VB_0 CCC. VCC <u>F9</u> VB_0 VCC. EN <u>F8</u> CND45 <u>K9</u> CND45 <u>K9</u> CND	22.775V		В С
				Changed by		SPIMBLIE	Engineer Chris Leyh Drawn by Chris Leyh R&D CHK DOC CTRL CHK MFG CTRL CHK	CC TITLE Rx/Syn: ALYA		of
1	2	3	4		5	6		7	8	

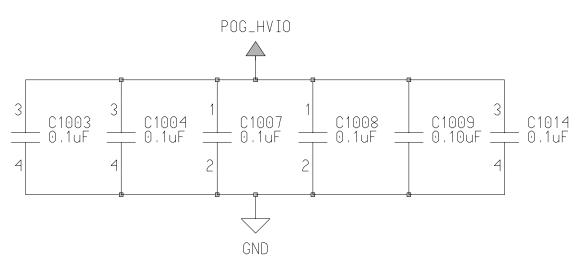
1	2	3	4	5	6	7	8
Α							A
В		Front End Module REF # (000 - 0		SWITCH 0987378K01 SWITCH 0987378K01 C003DNP 330F 2113930F39 GND ANT_SW_RX FL002 S0 Dhms NEAR FL001 IN OUT S0 Dhms NEAR FL001 IN OUT S0 Dhms CF61A2203 IN OUT S0 Dhms CF61A2203 S0 Dhms CF61A2203 CF61A2203 S0 Dhms CF61A2203 CF61A2203 CF61A2203 CF61A2203 CF61A2203 CF61A2203 CF61A2203 CF61A2203 CF61A2203 CF61A20 CF61A203 CF61A203 CF61A203	C013 0.3pF 2189687Y06 L013 1.0nH		В
C		MB_PCS_OUT MB_DCS_OUT		V1 4 V2 3 V4 V2 3 V4 V2 3 V4 V2 3 V4 V4 V4 V4 V4 V4 V4 V4 V4 V4	- WB_TX_IN	VLVID_1.875V U003DNP NC IN_A OUT_Y GND VL TSZ16 TX_RX_ERROR	C
			HO	S0 Dhms 50 Dhms 12 12 12 12 12 12 12 12 12 12	C005 33pF 50 Ohms C014DNP C014DNP C014DNP C014DNP 2189687Y14 C026 L015 L015 L015 L015 C014 C014DNP C026 L015 L014 C014		
Е	2	3	Changed ccloos		Engineer Chris Ley Drawn by ccl003 R&D CHK DOC CTRI MFG CTRI MFG CTRI 8:25:56 am 6	L CHK Quad Band Fro AL L CHK	DTOROLA INC , North US Highway 45 Libertyville Size D ent End Module .YA Number Sheet of 8

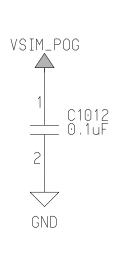


	4 5 6	
1		I
EL . SI	SW_IQ{SW_I,SW_O,SW_QX}	SW_Q
		PAVBA1
		TX_WB_EN
		- LB_EN - HB_EN - TX_EN_2V7
		SW_ASP1_CL
		SW_ASP1_CE
		Γ
		MB_HB_RF MB_LB_RF
		ž ž
	PS_CLK_OUT	
	MBC_EN1         MBC_EN2           SW_POS1	
	SW_POS2     SW_POS3       SW_POS4     SW_POS4	
	WB_IQ{WB_I, WB_0, WB_0X}	
	WB_IQ{WB_I, WB_IX, WB_Q, WB_QX}	
	WB_DCOC_Q WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_QX WB_DCOC_Q WB_DCO	
	WB_AGC1WB_AGC0, WB_AGC1, WB_AGC2, WB_AGC3, WB_AGC4} WB_AGC1 WB_AGC1 WB_AGC2 WB_AGC2 WB_AGC2 WB_AGC2 WB_AGC2 WB_AGC3 WB_AGC3 WB_AGC4 WB_AGC4 WB_AGC4 WB_AGC4 WB_AGC4 WB_AGC4 WB_AGC4 WB_AGC4 WB_AGC4 WB_LNA_BYP MB_LB_RF_OUT PS_CLK_OUT	
	WB_AGC4         WB_AGC4         WB_AGC4         MB_HB_RF_OUT           WB_LNA_BYP         MB_LB_RF_OUT         PS_CLK_OUT           WB_UMTS_IN         MB_PCS_IN           WB_TRK_CLK         MB_CSM900_IN           WB_RX_EN         MB_CSM850_IN	
1B_	I, MB_IX, MB_0, MB_0X}	
	MB_RX_EN XIAL_OUI MB_EXC_EN PS_SPIWB_DW MB_CM_IN SPIMB_DW MB_CM_CLK SPIMB_CLK BDX BDX BDX BDX BDX BDX BDX BDX	
	BCLKX SER_TX_CLK WB_VCO_SF_EN MB_RX_VCO_EN MB_RX_VCO_EN SCO IIII SER_TX_CLK WB_VCO_SF_EN MB_RX_VCO_EN SCO IIIII SER_TX_CLK WB_VCO_SF_EN SER_TX_CLK SCO SER_TX_CLK SCO	
	Understanding of the second se	
LK	,MB_ASPI_DATA,MB_ASPI_CE}	
	WB_VCO_SF_EN	Engi cclor Draw
	SPIMB{MB_SPI_CLK,MB_SPI_MOSI}	Chris R&D
	PS_SPIWB_CE	DOC
	Changed by Data Changed ITime	MFG
	Changed by Date Changed Friday, February 28, 2003 10:20:44 am	QA (

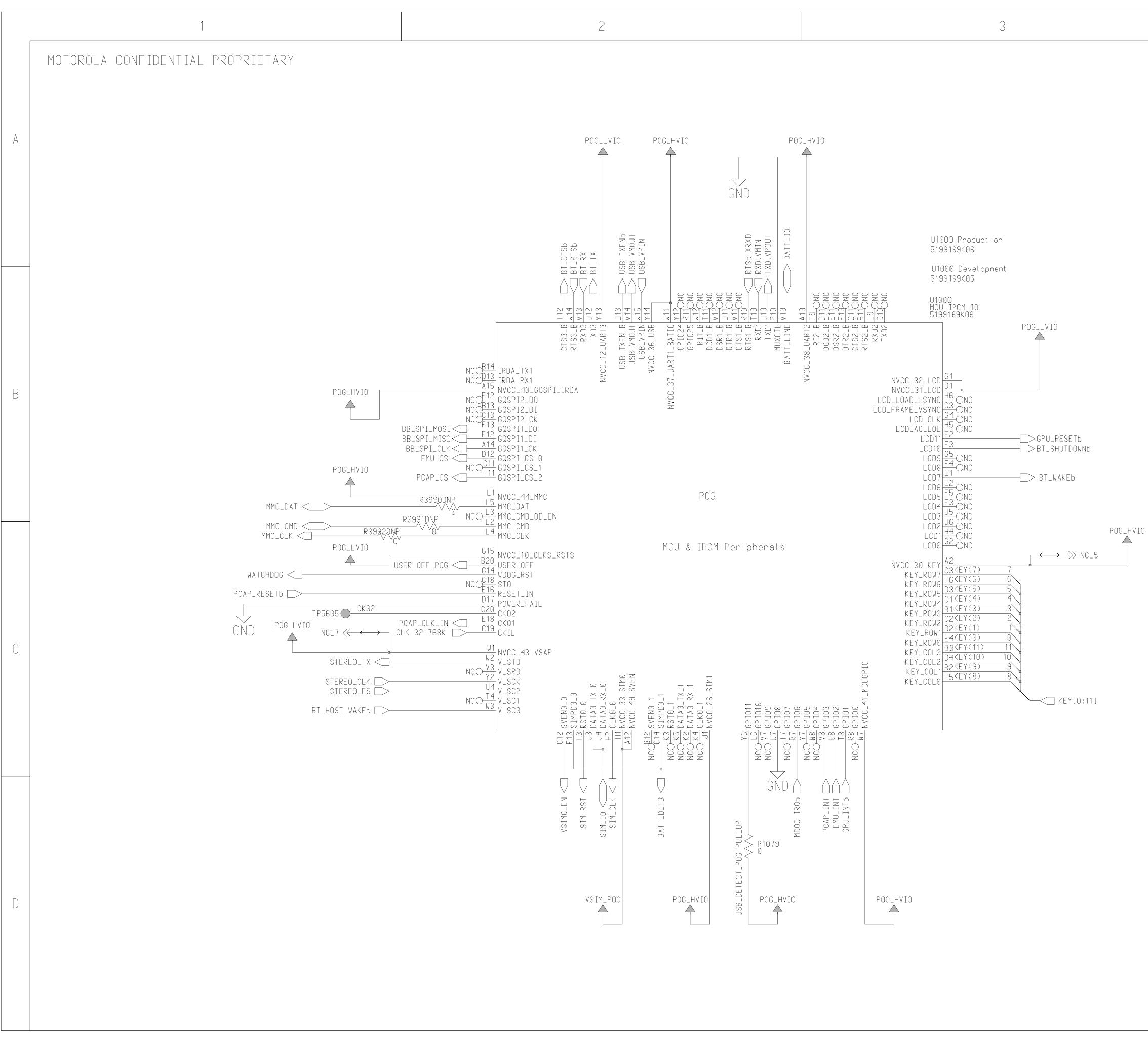




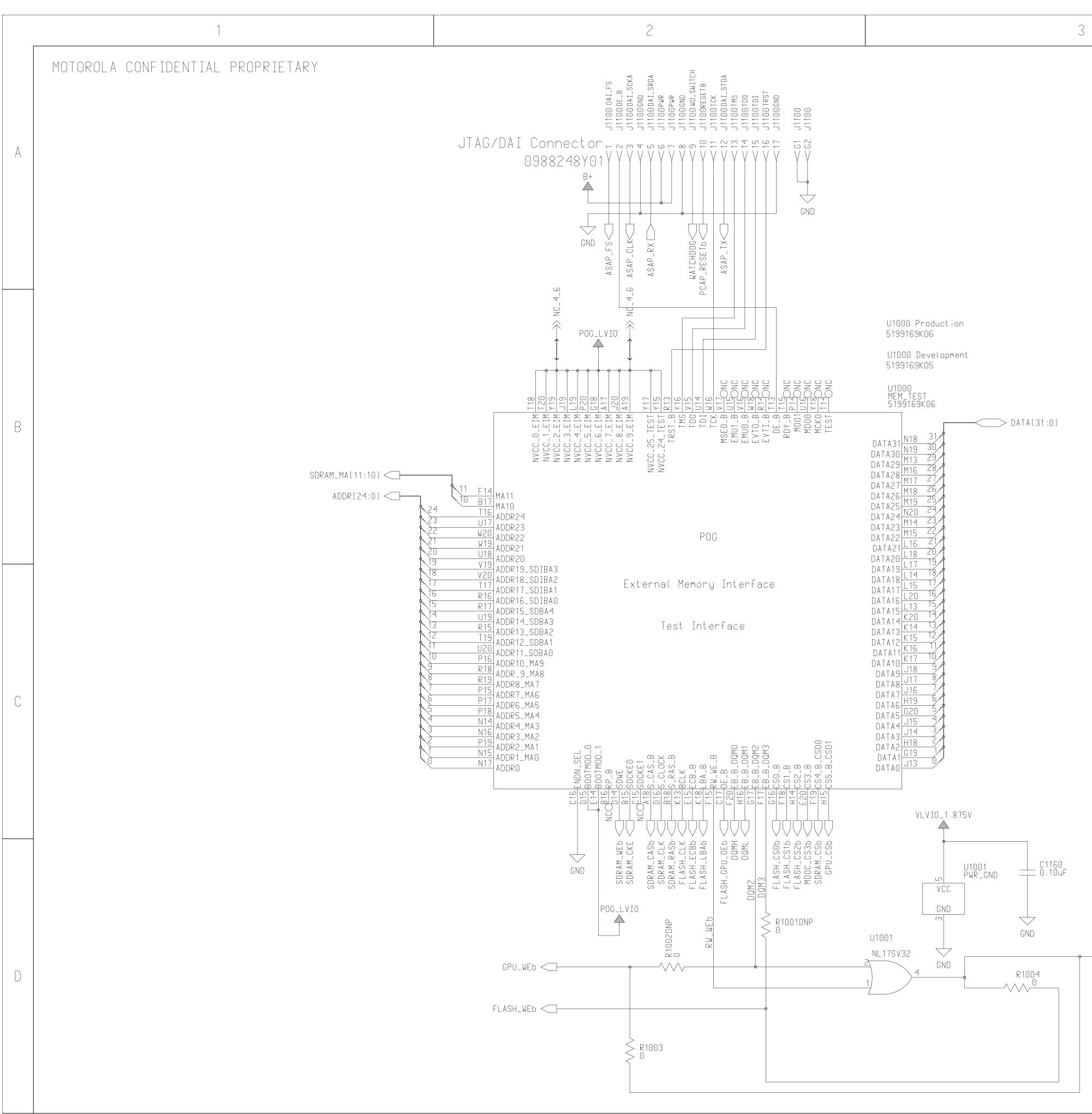




	4	
Engineer: Drawn by:	A MOTOROLA	INC.
R&D CHK: DOC CTRL CHK:	TITLE: SERPENS POG Power Interface	Size:
	REV: Drawing Number: Page: Date:	Of: Time:
Changed by:		



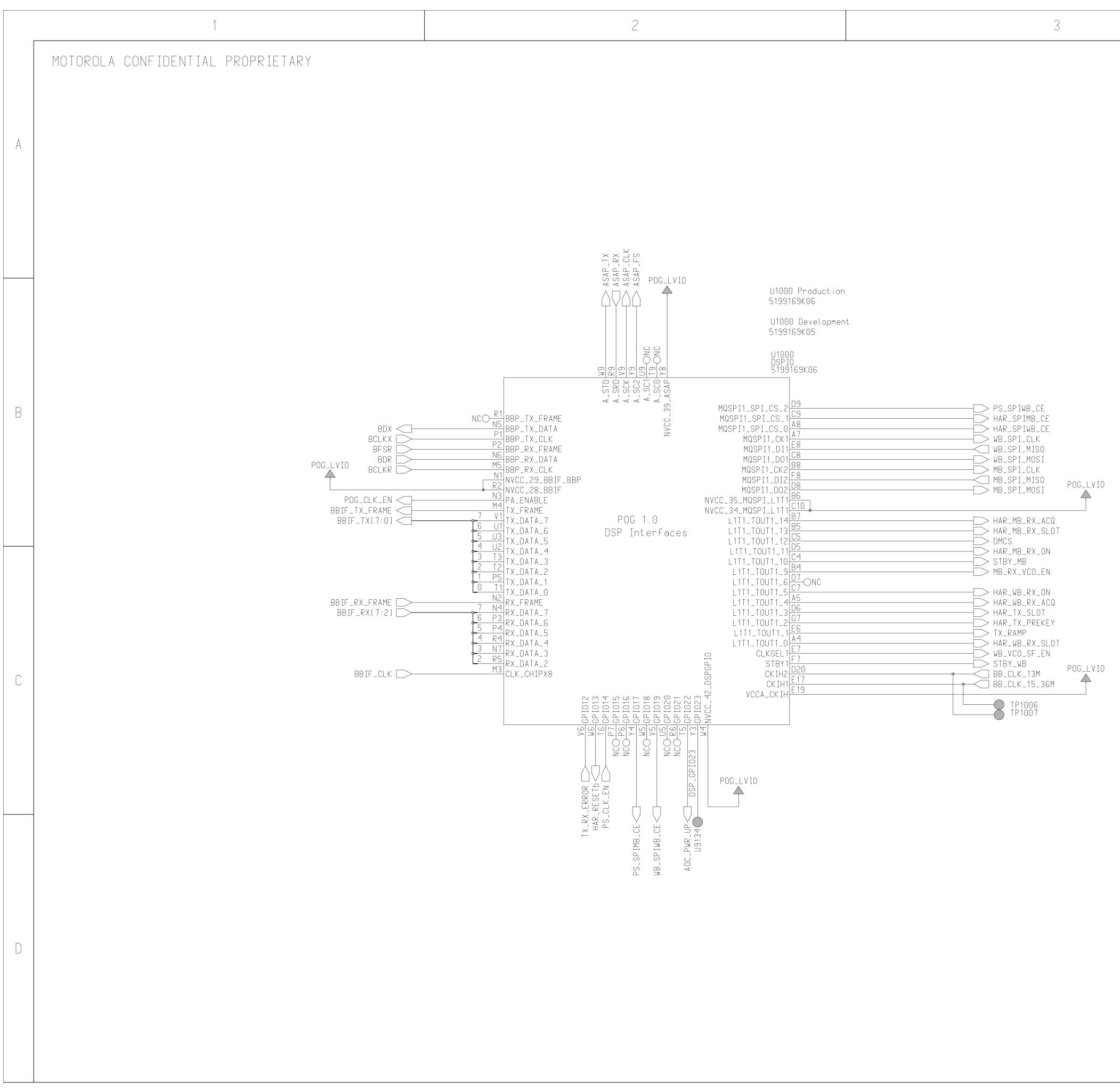
	4	
Engineer:	A MOTOROLA	
Drawn by:		
R&D CHK:	TITLE: SERPENS	Size:
DOC CTRL CHK:	POG	L
MFG CTRL CHK:	Peripheral Interface	
QA CHK:	REV: Drawing Number: Page: P9	Of:
Changed by:	Date:	Time:





———> MDOC\_WEb

	4
Engineer: Drawn by:	A MOTOROLA INC.
R&D CHK:	TITLE: SERPENS Size:
DOC CTRL CHK: MFG CTRL CHK:	POG
	Memory & Test Interface
QA CHK:	REV: Drawing Number: Page: Of:
Changed by:	Date: Time:



Engineer: Drawn by:	A MOTOROLA	INC.
R&D CHK:	TITLE: SERPENS	Size:
DOC CTRL CHK:	POG	
MFG CTRL CHK:	DSP Interface	
QA CHK:	REV: Drawing Number: Page: P9 8488453Y07	Of:
Changed by:	Date:	Time: