# E365 Theory of Operation

*Service Manual*

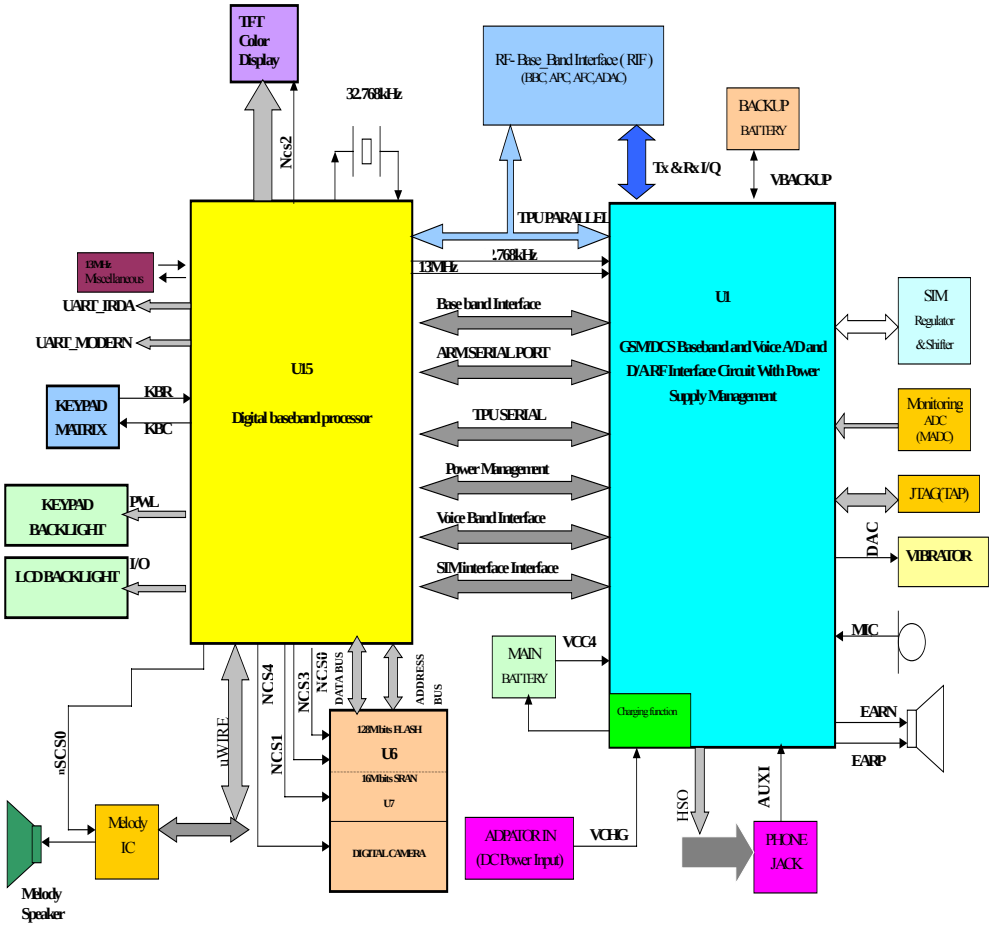
**Compal Communications, Inc.**

# △ Baseband function Descriptions

## 1. Introduction

Baby Garnet use TI's chipset (Calypso c035 and IOTA) as base-band solution. Calypso c035 is a GSM digital base-band logic included microprocessor , DSP , and peripheral. IOTA is GSM analog/codec solution. It contains the base-band codec, voice-band codec, several voltage regulators and SIM level shifter etc. The baby garnet add some features such as digital camera , photo sensor , TFT display , sixteen tone melody etc.

## 2. Base-band block




## 3. Theory

### 3.1 CALYPSO

Calypso is a chip implement the digital base-band processes of a GSM/GPRS mobile phone. The chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a micro-controller core with emulation facilities(ARMTDMIE), internal 8Kb of boot ROM memory , 4M bit SRAM memory , a clock squarer cell, several compiled single-port or 2 ports RAM and CMOS gates.

### 3.1.1 Real Time Clock (RTC)

### 3.1.2 Pulse Width Tones (PWT)

The PWT generates a modulated frequency signal for the external buzzer. Frequency is programmable between 349Hz and 5276Hz with 12 half tone frequencies per octave.

### 3.1.3 Pulse Width Light (PWL)

The PWL allows the control of the backlight of LCD and keypad by employing a 4096bit random sequence. The block used a switchable clock of 32kHz .

### 3.1.4 Modem-Uart

### 3.1.5 I2c master serial interface (I2C)

### 3.1.6 General purposes I/O (GPIO)

Calypso provides 16 GPIOs in read or write mode by internal registers. In Baby garnet we use 9 of them as follows.

| GPIO PIN | Used As.. | Description |
|---|---|---|
| IO0 / TPU_WAIT | IO0 | DTR_MODEM Output ; RS232 DTR output signal |
| IO1 / TPU_IDLE | IO1 | disable |
| IO2 / IRQ4 | IO2 | LEDLCM_EN: LCM backlight=1 active |
| IO3 / SIM_RnW | IO3 | LCDA0 ; LCD Data or Command Control signal |
| IO4 / TSPDI | IO4 | nIRQ_melody:Melody IC interrupt, active=0 |
| IO5 / SIM_PWCTRL | SIM_PWCTRL | For SIM Card Power Control |
| IO6 / BCLKX | IO6 | EAR_DETECT ; input |
| IO7 / NRESET_OUT | nRESET_OUT ? | LCD Peripherals reset |
| IO8 / MCUEN1 | IO8 | nIO_PWR_EN: Accessary power control : active=1 |
| IO9 / MCSI_TXD | MCSI_TXD | DAI interface ,reserved; disable |
| IO10 / MCSI_RXD | IO10 | COMS_LDO_EN ; active=1 |
| IO11 / MCSI_CLK | IO11 | COMS_ASK ; input |
| IO12/ MCSI_FSYNCH | IO12 | IO_PWR_EN: Accessary power control : active=1 |
| IO13 / MCUEN2 | IO13 | LCD_ID; input |
| IO14 / nBHE | nBHE | nBHE |
| IO15 / nBLE | nBLE | nBLE |

### 3.1.7 Serial Port Interface (SPI)

The SPI is a full-duplex serial port configurable from 1 to 32 bits and provides 3 enable signals programmable either as positive or negative edge or level sensitive. We use SPI to control the melody IC.

nSCS0 :Chip select 0

SDO: Data out.

SDI: Data in

SCLK: Serial clock

### 3.1.8 Memory interface and internal static RAM

A 4Mbit SRAM is embedded on the die and memory mapped on the chip-select CS6 of the memory interface.

### 3.1.9 SIM interface

### 3.1.10 JTAG

### 3.1.11 Time Serial Port (TSP)

### 3.1.12 TSP Parallel interface (ACT)

| Herculse Pin no | Pin Name | Used As.. | Description/Net |
|---|---|---|---|
| M12 | TSPACT0 | TP5 | X |
| M14 | TSPACT1 | TSPACT1 | PAENA (Chip enable for Power Amp IC) |
| L12 | TSPACT2 | TSPACT2 | PDNB (RF IC power down control) |
| L13 | TSPACT3 | TSPACT3 | X |
| J10 | TSPACT4 | TSPACT4 | X |
| K11 | TSPACT5 | TSPACT5 | X |
| K13 | TSPACT6/nCS6 | TSPACT6 | TRENA (T/R switch enable) |
| K12 | TSPACT7/CLKX_SPI | NC | X |
| K14 | TSPACT8/Nmreq | TSPACT8 | GSM_TXEN (Used both within the RF switch and the Power Amp to select the GSM Frequency Band) |
| J11 | TSPACT9/MAS1 | TSPACT9 | X |
| J12 | TSPACT10/nWAIT | NC | X |
| J13 | TSPACT11/MCLK | NC | X |

### 3.1.13 Radio Interface (RIF)

## 3.2 IOTA

IOTA is an analog base-band device which a digital base-band device is part of a TI DSP solution intended for digital cellular telephone applications. This includes the GSM 900, DCS 1800, PCS 1900 standards.

IOTA includes a complete set of base-band functions that perform the interface and processing of the following voice signals, the base-band in phase(I) and quadrature (Q) signals. Which support both the single-slot and multislot modes. IOTA also includes associated auxiliary RF control features supply voltage regulation, battery charging controls , and switch on/off system analysis.

IOTA interfaces with the CALYPSO through a digital base-band port and a voicebad serial port. The signal ports communicate with a DSP core. A microcontroller serial port communicates with the microcontoller core and a time serial port communicates with the time processing unit for real-time control.

### 3.2.1 Base-band Codec (BBC)

### 3.2.2 Automatic Frequency Control ( AFC)

### 3.2.3 Automatic Power Control ( APC)

### 3.2.4 Time serial port (TSP)

### 3.2.5 Voice band Codec (VBC)

### 3.2.6 SIM card shifters (SIMS)

### 3.2.7 Voltage Regulation (VREG)

Several low-dropout(LDO) linear voltage regulation supply power to internal analog and digital circuits to the DBB processor and to external memory

**a.** VRDBB is a programmable regulator that generates the supply voltages( 1.8V , 1.5V , and 1.3V) for the core of the CALYPSO. In baby garnet , it is programmed to 1.5V. During all modes, the main battery directly supplies VRDBB.

**b.** VRIO is a programmable regulator that generates the supply voltages(2.8V) for I/Os of the CALYPSO and IOTA. During all modes, the main battery directly supplies VRIO.

**c.** VRMEM is a programmable regulator that generates the supply voltages(2.8V and 1.8V) for external memories (typically flash memories) and CALYPSO memory interface I/Os. In baby garnet , it is programmed to 2.8V. During all modes, the main battery directly supplies VRMEM.

**d.** VRRAM is a programmable regulator that generates the supply voltages(2.8V and 1.8V) for external memories (typically SRAM memories) and CALYPSO memory interface I/Os. In baby garnet , it is programmed to 2.8V. During all modes, the main battery directly supplies VRRAM.

**e.** VRABB is a programmable regulator that generates the supply voltages (2.8V ) for the analog functions of the IOTA. During all modes, the main battery directly supplies VRRAM.

**f.** VRSIM is a programmable regulator that generates the supply voltages (2.9V and 1.8V )for SIM card and SIM card drivers. During all modes, the main battery directly supplies VRRAM.

**g.** VRRTC is programmable regulator that generates the supply voltages

(1.3V, 1.5V ,and 1.8V) for CALYPSO's backup RTC. It is switched on the main or backup battery, depending on the phone state.

**3.2.8 Base-band Serial Port (BSP)**

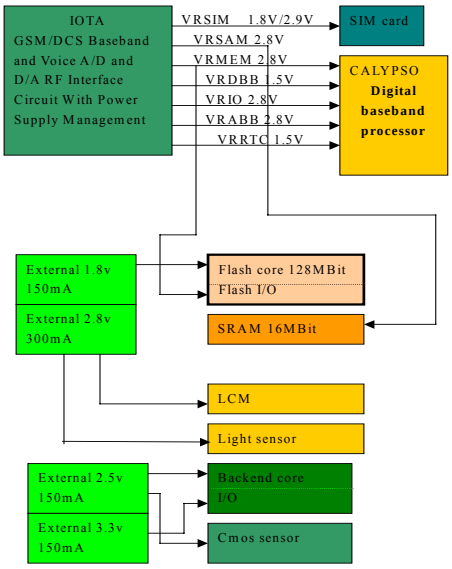
**3.2.9 Battery charger interface (BCI)**

**3.2.10 Monitoring ADC (MADC)**

**3.2.11 Reference Voltage / Power on control (VRPC)**

**3.2.12 Internal bus and interrupt controller( IBIC)**

## 3.3power supply circuit




The phone is mainly supplied from the main battery. The main battery supply the two parts : RF block, base-band block.

The input power to IOTA is divided into 4 blocks.

VCRAM: to provide power for VRRAM

VCMEM: to provide power for VRMEM

VCIO1,VCIO2: to provide power for VRIO and VRSIM

VCABB: to provide power for VRABB

VCDBB: to provide power for VRDBB

The IOTA provides seven low drop-out voltage regulators.

VRRAM:2.8V@50mA, to supply SRAM

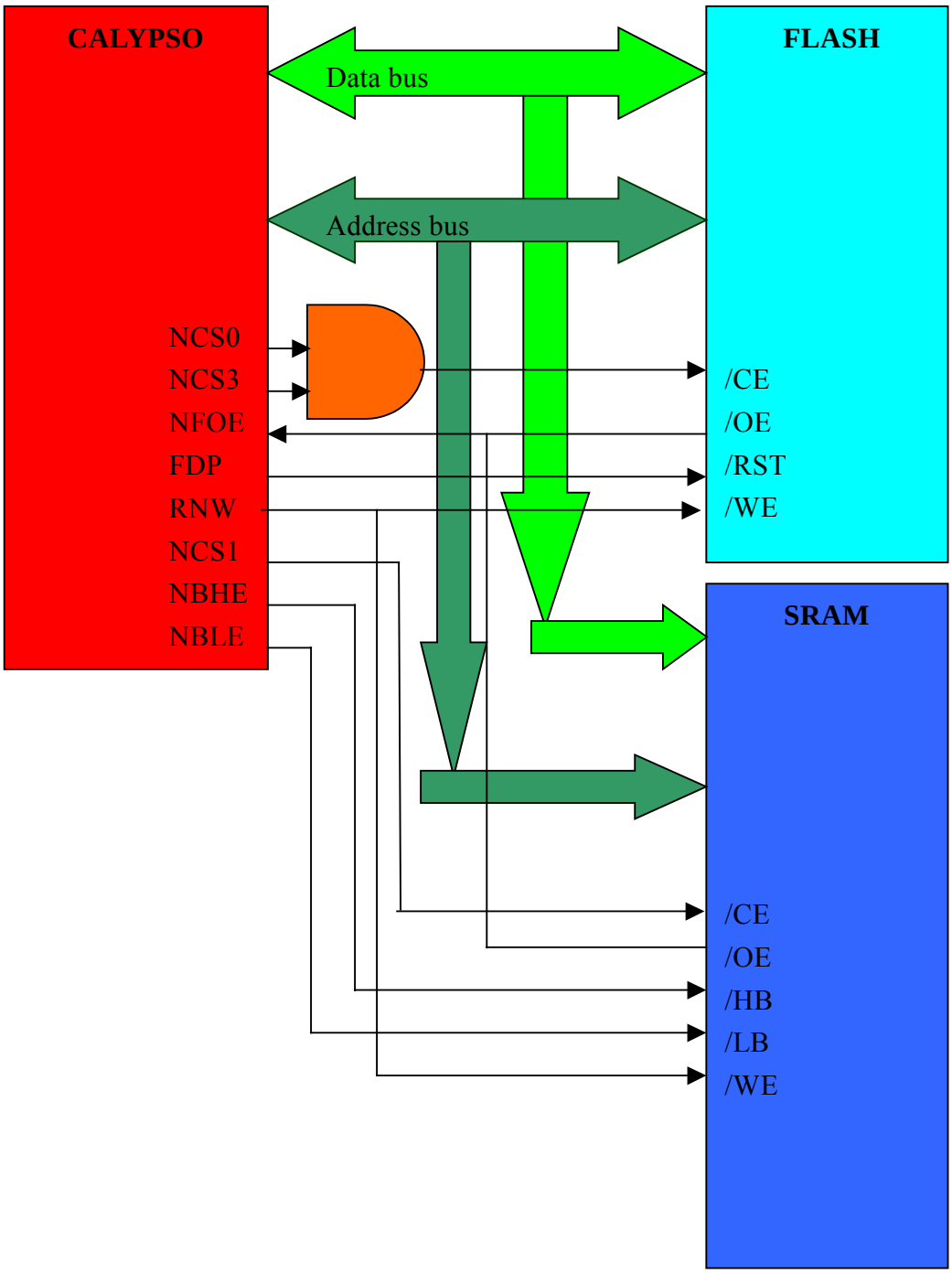
VRMEM:2.8V@60mA, to supply flash I/O and CALYPSO memory interface I/Os.

VRDBB;1.5V@120mA. to supply the core of the CALYPSO

VRIO:2.8V@100mA, to supply I/Os of the CALYPSO and IOTA

VRABB;2.8V@50mA to supply the analog functions of the IOTA
VRRTC:1.5V@10uA, to supply the CALYPSO's backup RTC.
VRSIM:1.8V or 2.9V@10mA , to supply the SIM.

### 3.4 memory circuit

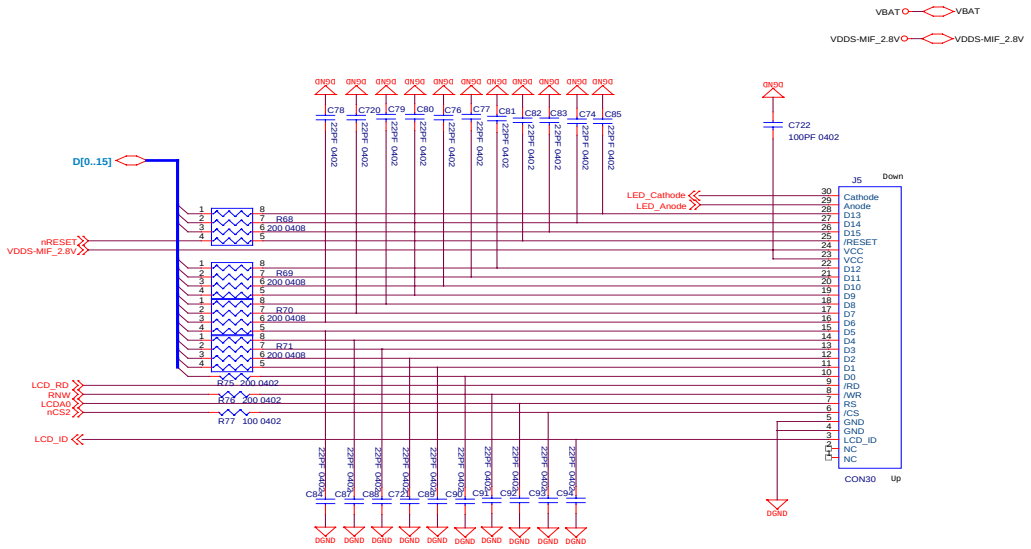


## Description

Flash is a 128Mbit device, supported by external LDO and VRMEM. The access time of flash is 90ns. The total 128Mbit are divided into two sections: 112Mbit is used for software program code and 16Mbit is used for user's data.

SRAM is a 16Mbit device supported by VRRAM. The access time of flash is 70ns.

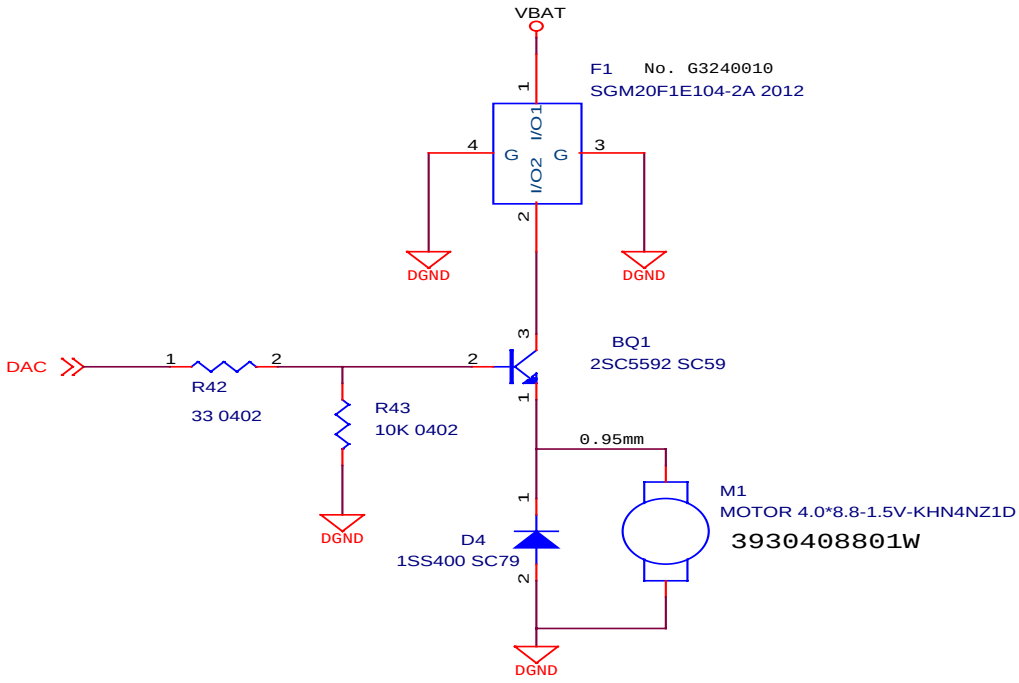
## 3.5 display circuit




## Description

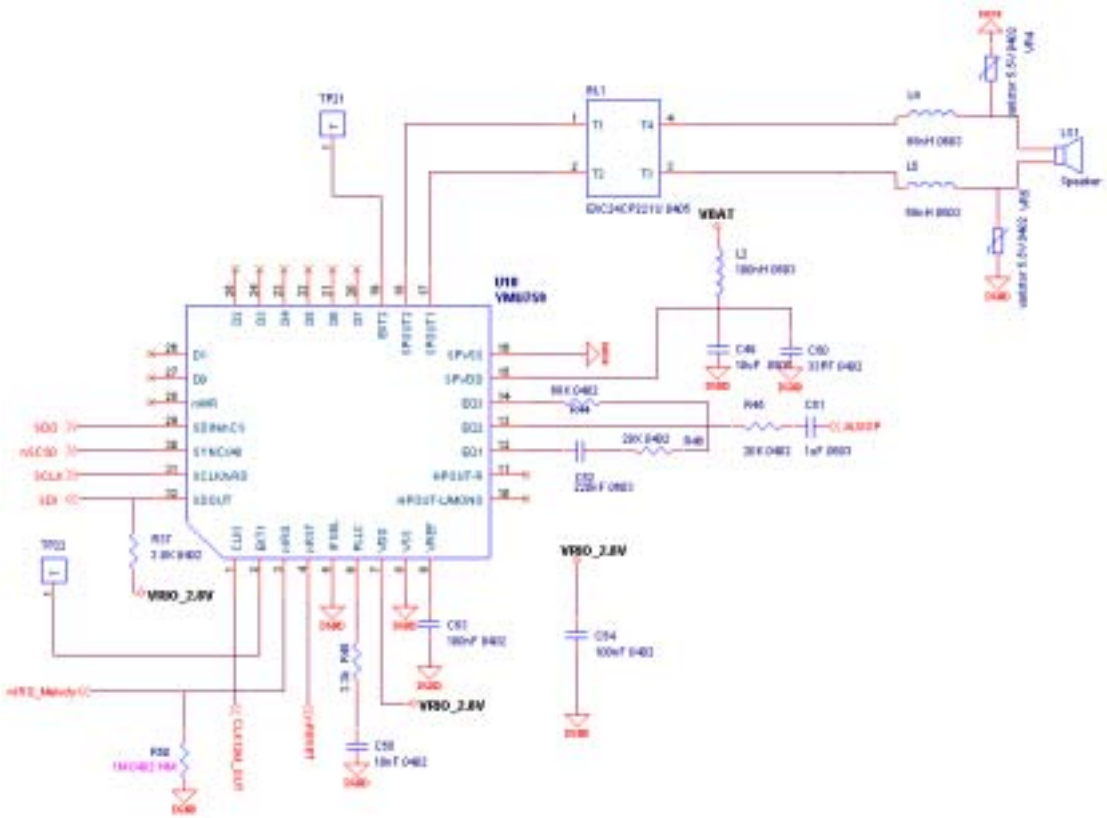
The display area is a 128*160 resolution LCD module. The power of LCDM is supplied from external LDO (2.8V). It is controlled by CALYPSO via parallel interface : data bus and chip select .The Ncs2 is low active to enable the LCDM data bus. Resistance and capacitance is used for radiation suppression.

### 3.6vibrater circuit




DAC of the IOTA is used to control the vibrational level. D4 is used to protection the vibrater. In the 3.8V, the DAC output voltage is 1.9V and drain current is around 90mA .

### 3.7 speaker circuit



**Description**

The Melody IC MA2 works as follows.

First, the CPU (G2) fetch melody data from flash and fed them into MA2 by serial interface. After receiving these data, MA2 will start decode its content and start its sequencer for processing. After completing this process, the MA2 will generate the tones we want according to the melody data. Then, these data will run through MA2's DAC, which inside it. Then, the converted signal is fed into an equalizer, and then followed by an amplifier, which they are inside MA2. Then this signal will be outputted from SPOUT1 and SPOUT2 to drive the speaker.

Here, the R44 and R46 provide optimal gain control for MA2. To ensure the speaker not to be overdrove.

## 3.8 DSC (Digital Still Camera) function block diagram and circuit description

### 3.8.1 Function block diagram

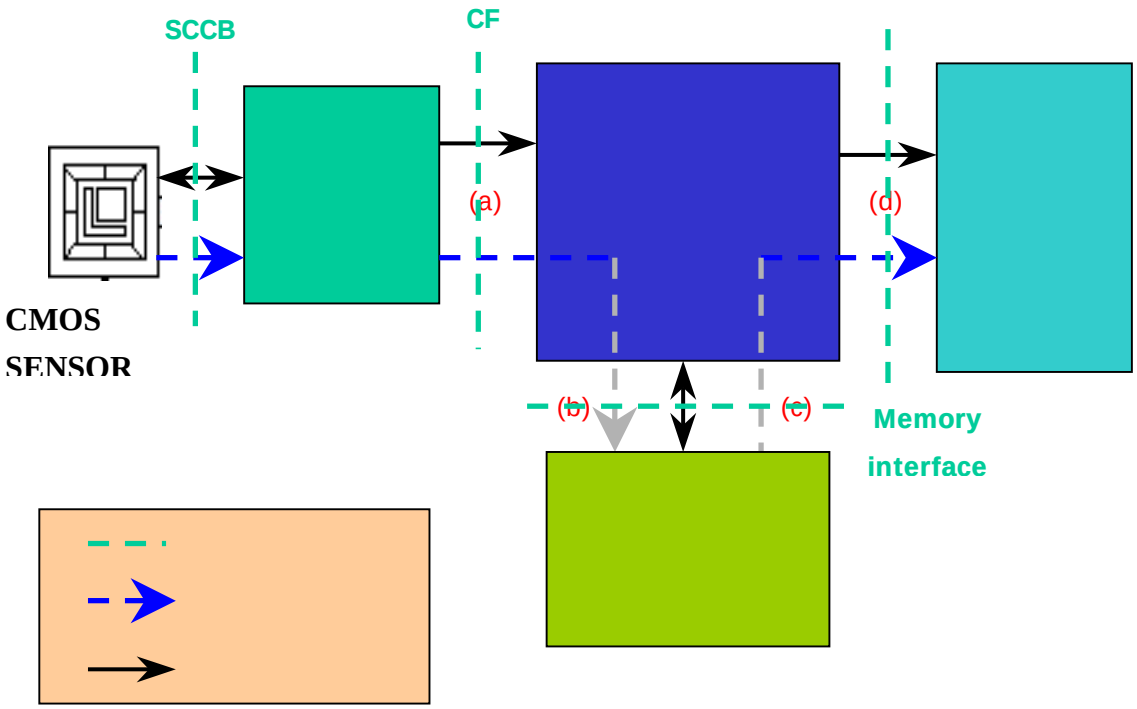
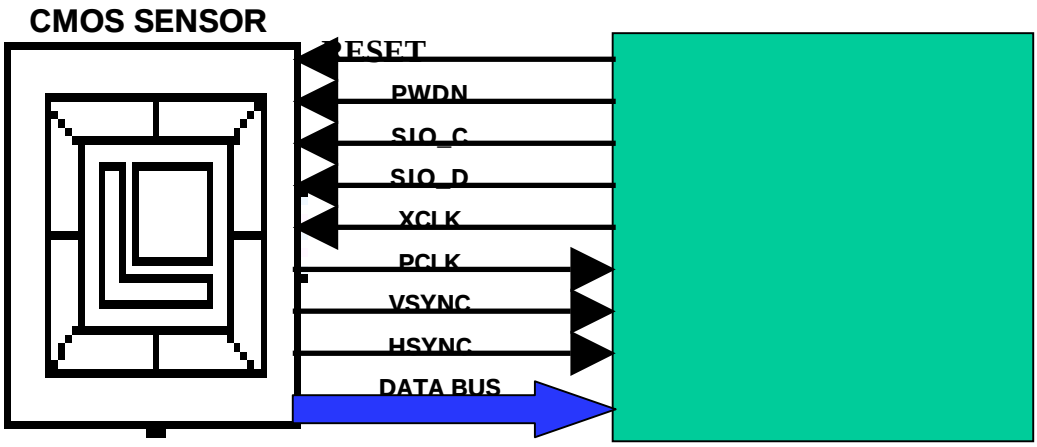



**Fig. 1 Imbedded DSC block diagram**

Imbedded DSC included two portions, one is front-end sensor module and another is backend DSP chip. There are including two interfaces which are SCCB (Serial Camera Control Bus) and CF (Compact Flash). The function block diagram is shown in Fig.1. The SCCB is used in sensor to backend interface, and the backend to host (G2) is used CF interface.

**3.8.1. Sensor to Backend Interface**




**RESET**: (default 0) chip reset with active high

**PWDN**: (default 0) power down mode selection

"0" normal mode, "1" power down mode

**SIO_C**: SCCB (Single Chip Camera Bridge) serial interface clock input

**SIO_D**: SCCB (Single Chip Camera Bridge) serial interface data input and output

**XCLK**: Clock input

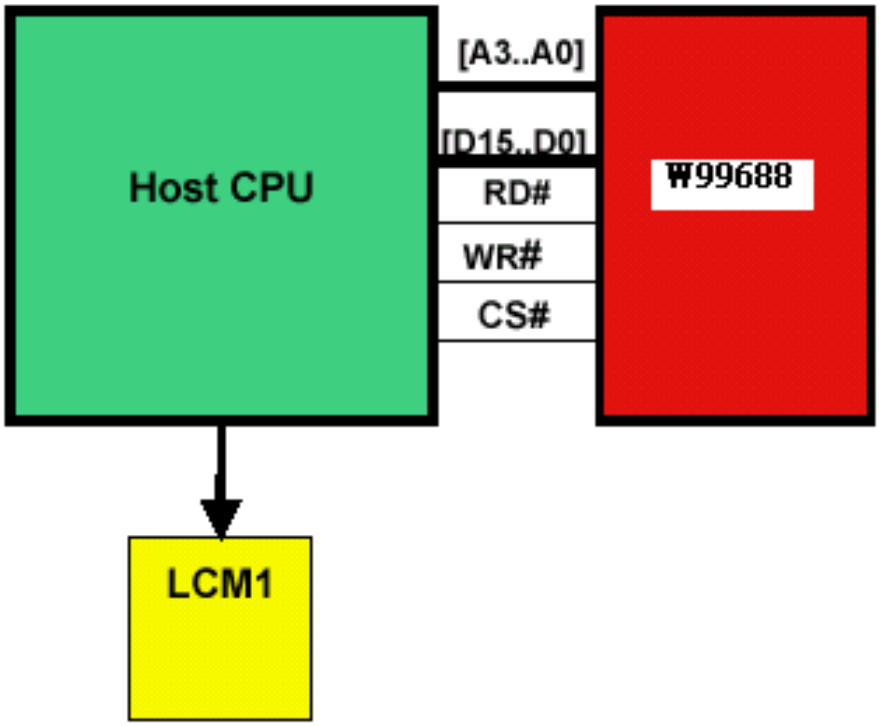
**PCLK**: Pixel clock output

**VSYNC**: Vertical sync output

**HSYNC**: Horizontal sync output

**Data Bus**: 8 bits

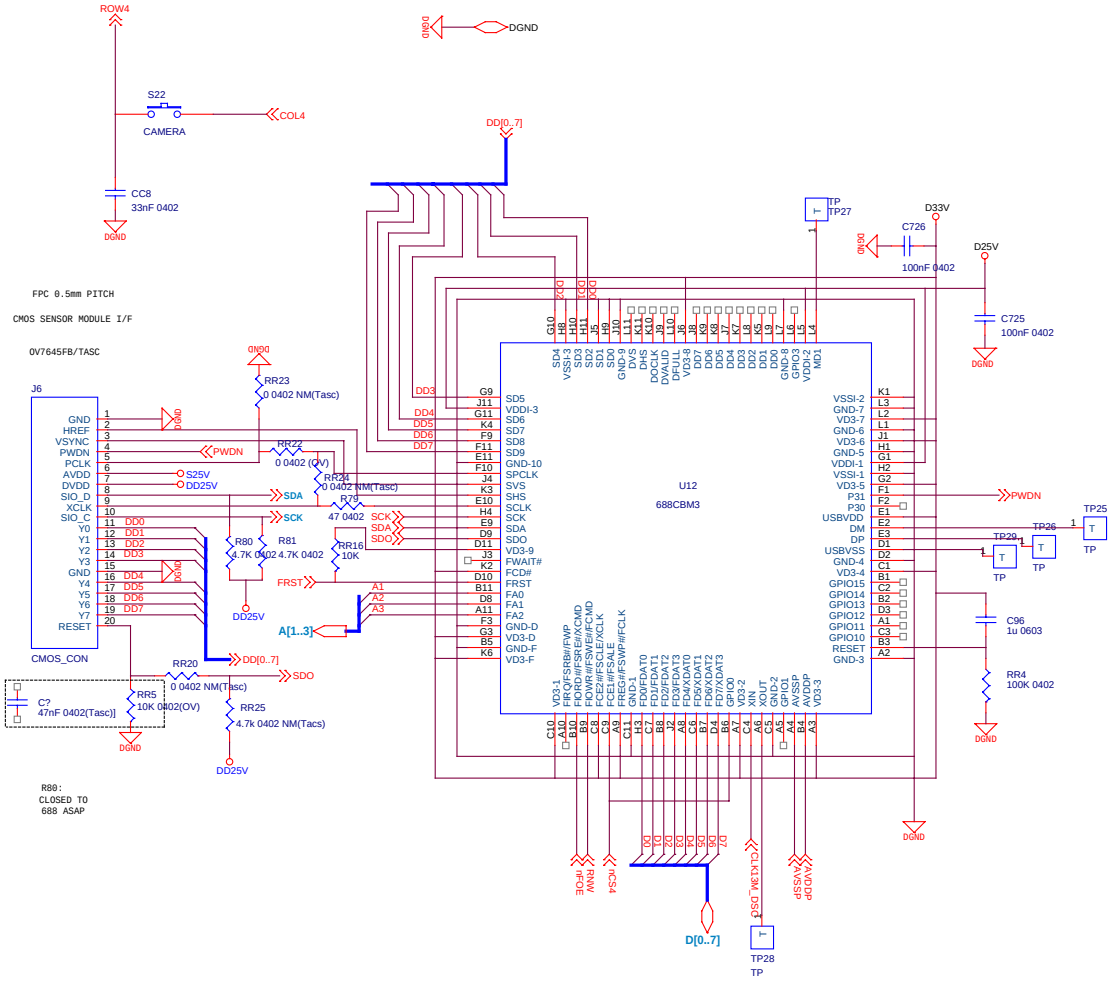
### 3.8.1.2 Backend to Sensor Interface




**A0..A3**: Compact Flash: Address-0~3 for command
**D15..D0**: Data bus connect to Host
**RD#**: Read data or command
**WR#**: Write data or command
**CS#**: Chip select

### 3.8.2 Circuit description

#### 3.8.2.1 Main circuit




D33V: Power supply for I/O pads +3.3 V

DD25V: Power supply for CMOS sensor digital part +2.5 V

S25V: Power supply for CMOS sensor analog part +2.5 V

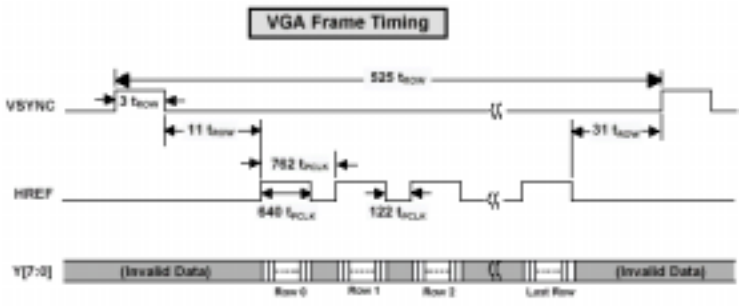
D25V: Internal core logic power supply. +2.5 V.

AVDPP: Power supply for PLL analog 2.5V

AVSSP: Ground for PLL analog

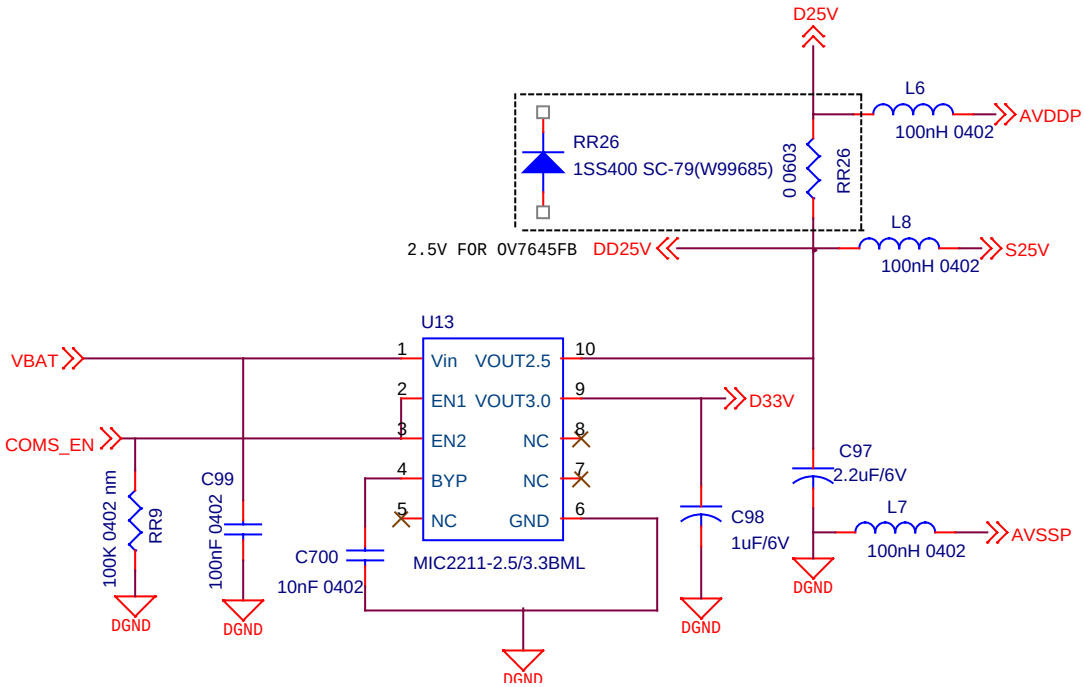
FSRT: Compact flash: RESET/RESET# signal (High enable 2.8V)

Vsync & HREF relation:



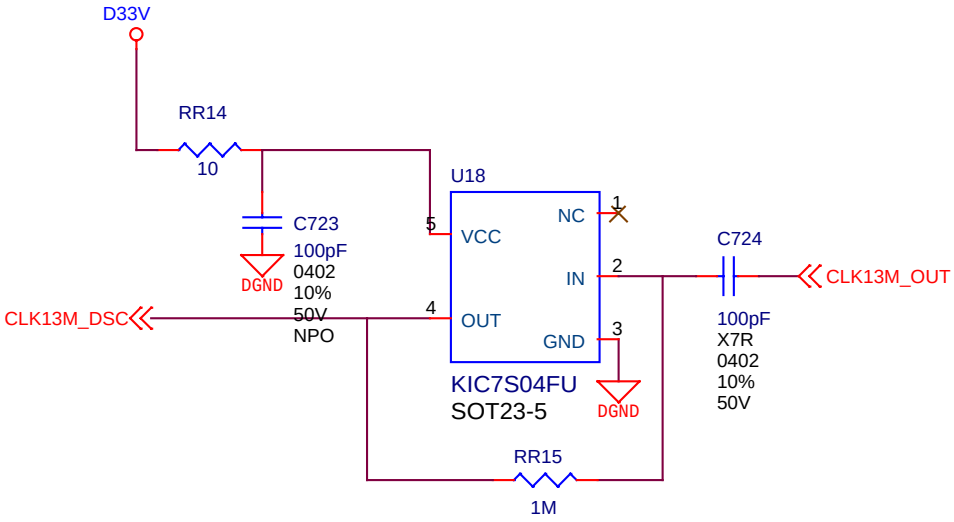
The backend power on reset is 100ms that generated by C96 (1uF) and RR4 (100k ohms). The backend clock CLK13M_DSC is 13MHz (Vp-p 3.0V), and XCLK is 24MHz ( Vp-p 3.35V) that is generated from backend to sensor. Then sensor will base on XCLK to generate PCLK for image data clock that is 12MHz (Vp-p 2.3V).

### 3.8.2.2 DSC DC power




CMOS_EN is used to control DSC power enable. It is high active (2.8V). L6, L7 and L8 are formed low pass filter with C97 in order to suppress low frequency noise.

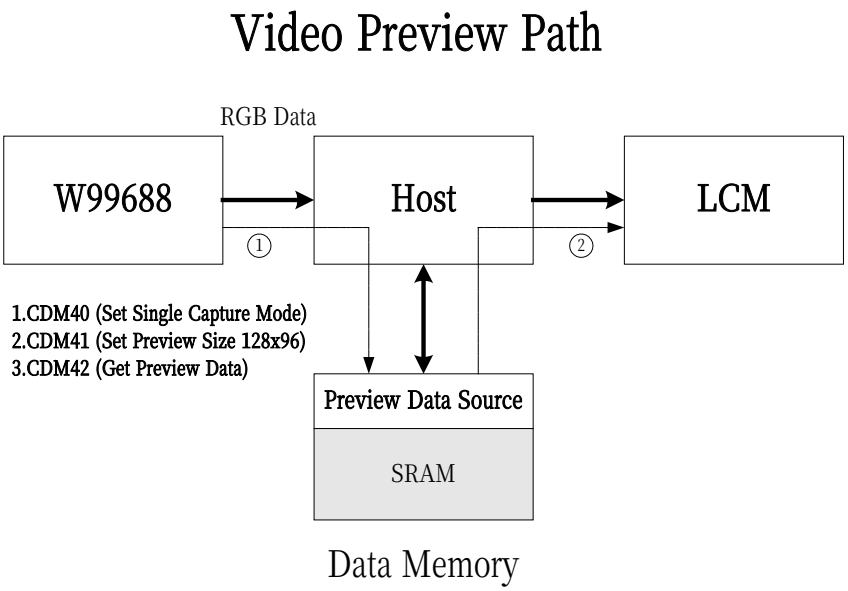
### 3.8.2.3 DSC system clock



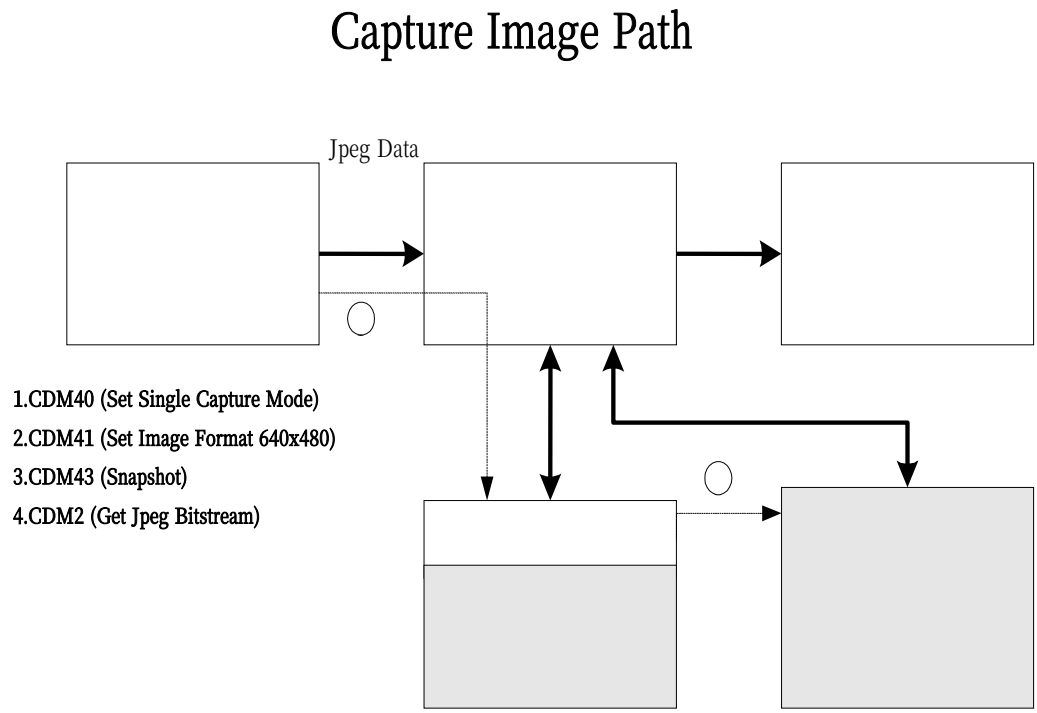

Add buffer to avoid CLK13M_OUT over load causing system hang.

## 3.8.3 Function flow chart

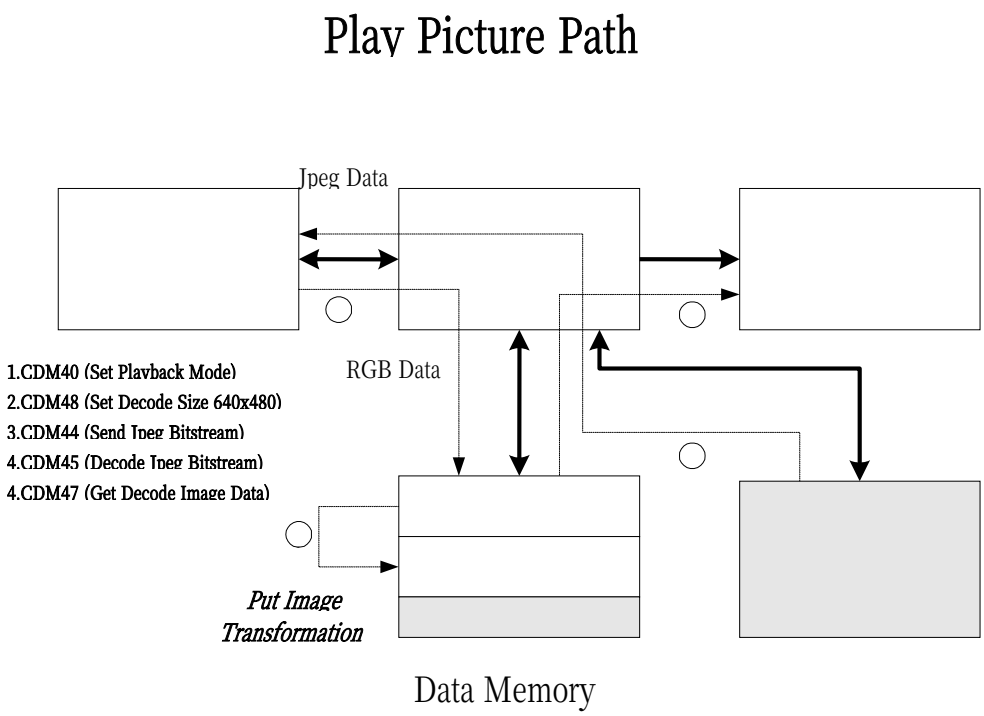
### 3.8.3.1 Preview:



### 3.8.3.2 Capture:

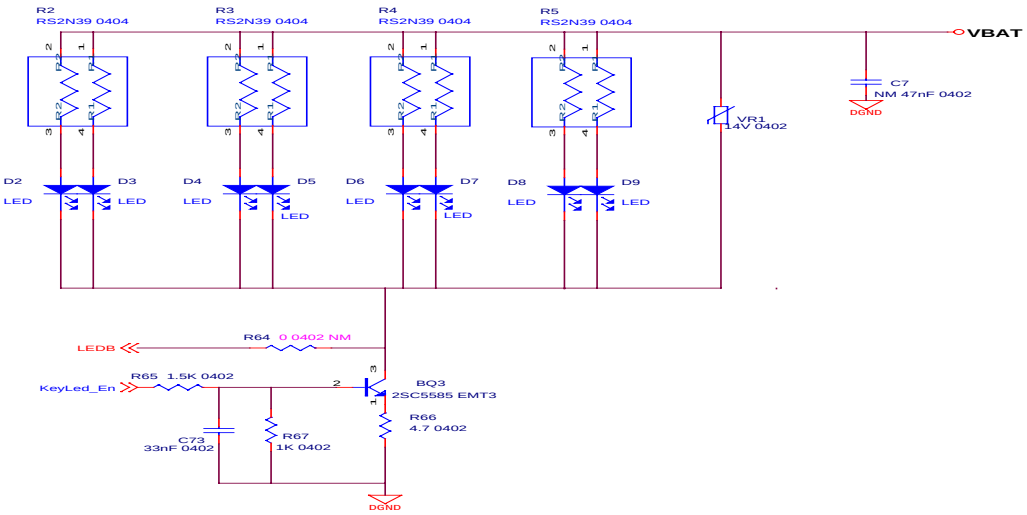



### 3.8.3.3 Playback:

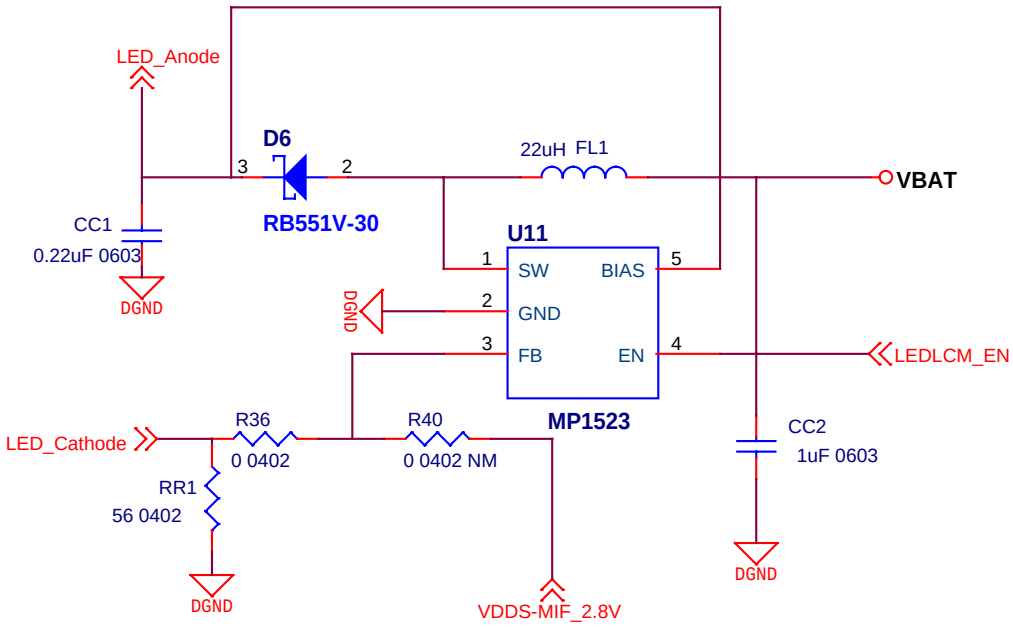


## 3.9 led circuit

### keypad backlight




### LCD module backlight

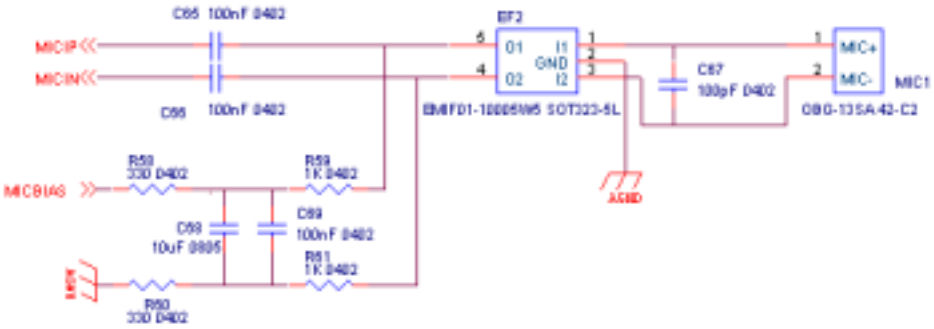



### description

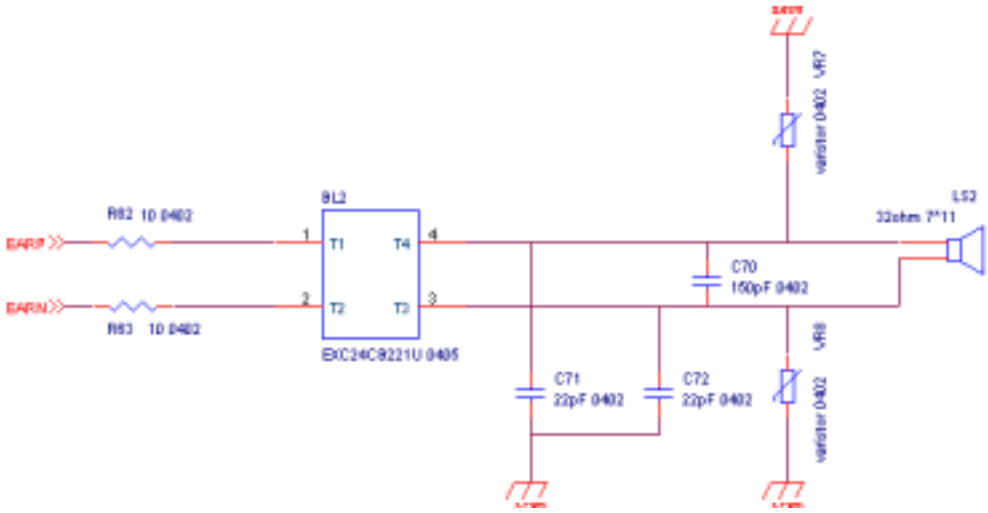
The baby garnet employ three LEDs for LCD module backlight and six LEDs for keypad backlight. The keypad backlight is controlled by PWL (Pulse with light). The LCD module backlight is controlled by GPIO of the CALYPSO. The CALYPSO is used to enable BQ3 and U11. The total current of LCD backlight LED's and keypad backlight LED's is about 70mA during all LED work.

### 3.10 audio circuit

Uplink:




Downlink:




**Description**

The acoustic circuit can be divided into two parts, ***Uplink*** and ***Downlink*** path.

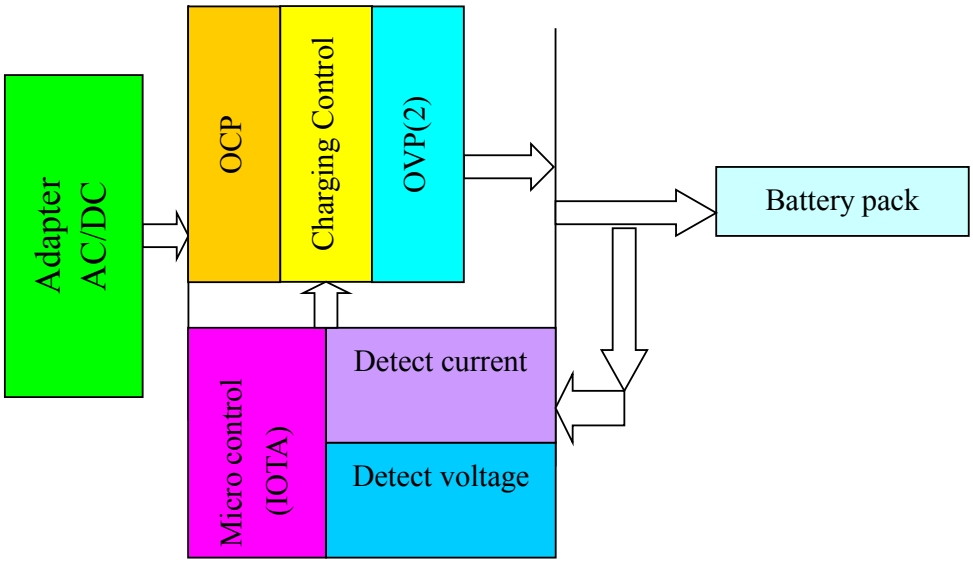
For the ***Uplink*** path, the analog signal, or Voice, is fed into IOTA (MICIP and MICIN) by the microphone's differential input. This signal is then sampled and transmitted into G2 DSP via the VSP (Voice-Band Serial Port) interface. After being modulated, the signal goes through the uplink I/Q path to the RF transceiver and then being transmitted by the antenna.

The microphone is biased by the IOTA MICBIAS pin (2.5V). Where the bias circuit R58, R59, R60, R61 provide optimal operation point for the microphone.

For the ***Downlink*** path, the signal is received from antenna. Then it is down-converted to I/Q signal and then send into G2 DSP. After being demodulated, the signal is then transmitted into IOTA via VSP interface. After re-construct this signal, this signal is then amplified and drove the receiver.

### 3.11 charging circuit

### 3.11.1Function Block




### 3.11.2 function description

When the charging device is plugged in, the charging scheme for the Li-ion battery is constant current first (MAX current is 400mA) then followed by constant voltage charging. When battery voltage has been detected full, the BCI of IOTA will be turned off till a Low voltage threshold has been detected. At charger plug OUT, the charger status bit CHG_STS is driven from “1” to “0” and an interrupt of the INT2 type is generated making the uC aware of the charging device unplug. When over-discharging (battery voltage is less than 3.2V), the BCI of the IOTA will be the pre-charge state (charging current equal to 30mA). Until battery voltage bigger than 3.2V, it returns to normal charge. When ICHG bigger than 1 A, the OCP (over current protection) will be enabled. When the battery voltage is higher then 4.35V, the OVP (over voltage protection) will be enabled.

### 3.12 Earphone block diagram and circuit description

#### 3.12.1 Function block diagram

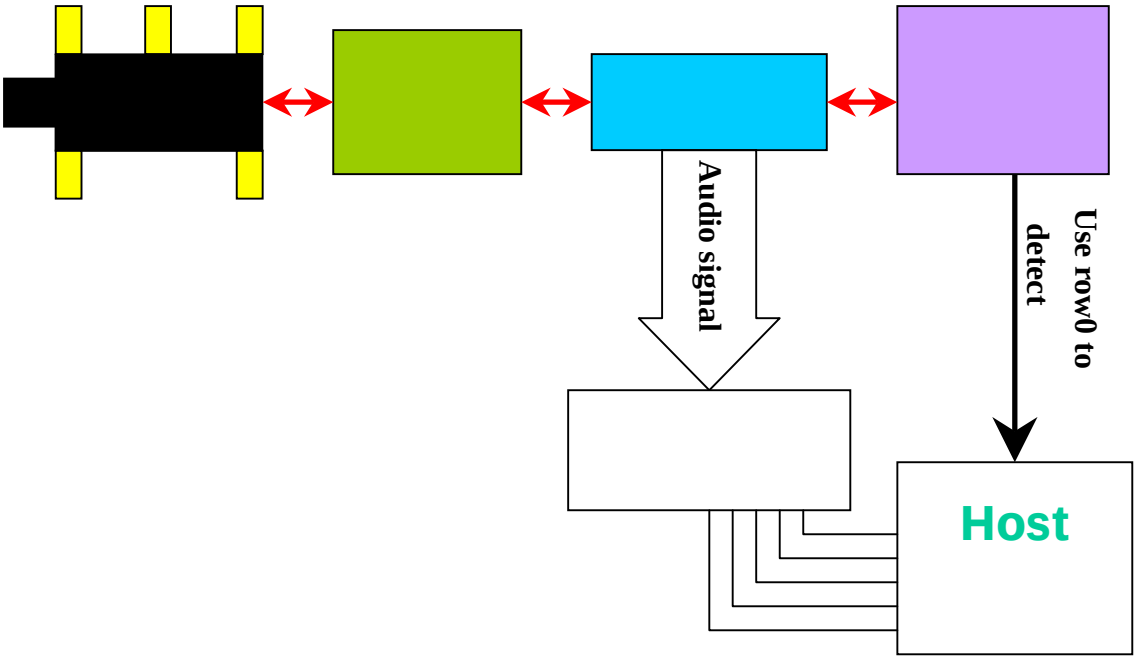
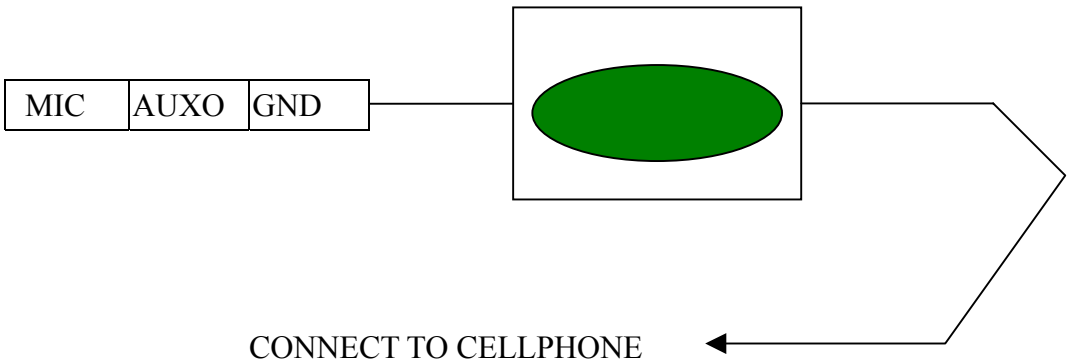



**Fig. 1 Earphone block diagram**

The earphone circuit included audio jack, protect circuit, EMI circuit and Send-End key controller. The all design based on external earphone which characteristic is shown below.

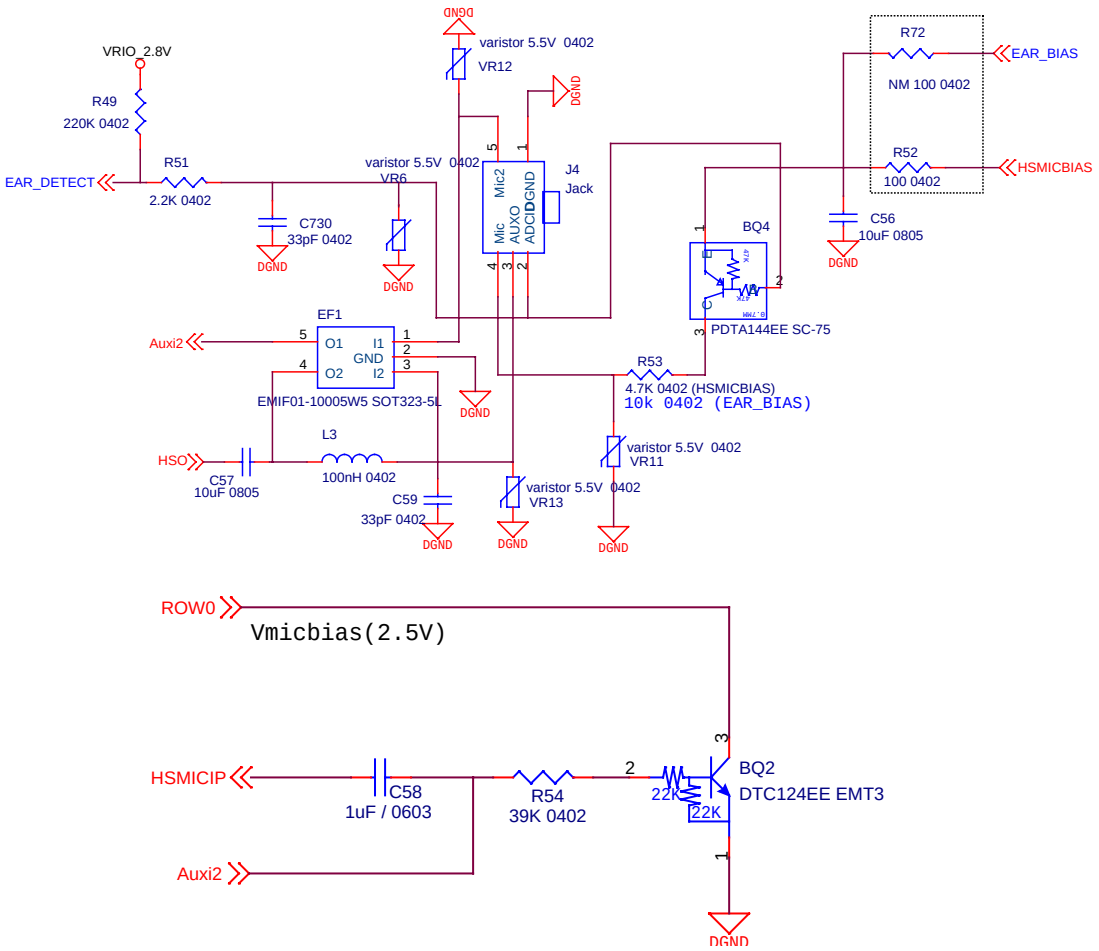
##### 3.12.1.1 Outward appearance:




##### 3.12.1.2 Impedance:

| The status of send-end key | Relaxed | Pressed |
|---|---|---|
| MIC TO GND | 1.7kΩ | OPEN |
| AUXO TO GND | 35Ω | 35Ω |

### 3.12.2 Circuit description



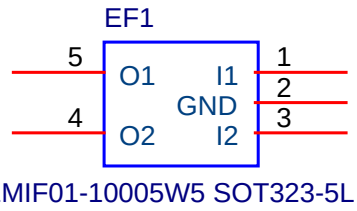

BQ4: It is used to avoid error function on earphone plug in/out.

J4: Audio jack

EF1: Filter audio and circuit noise.

BQ2: Send-end key detected. When BQ2 turned on, the send-end function work.

#### 3.12.2.1. EMI Filter including ESD protection

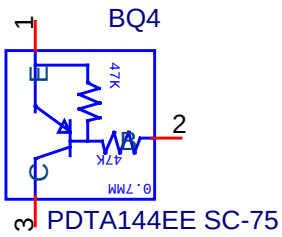



Rd=Rd1=Rd2=100Ω

Rd1 is the dynamic impedance between I1 and O1.

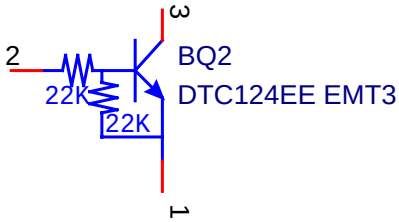
Rd2 is the dynamic impedance between I2 and O2.

### 3.12.2.2. Digital transistors (built-in resistors)




Vi(off) input-off voltage Vi≥1.2V, ($V_O$=0V)
Vi(on) input-on voltage Vi≤1.6V, ($V_{CE}$ = 300 mV)
R1 (input resistor) =47k ..Resistor ratio=1

### 3.12.2.3 Digital transistors (built-in resistors)




Vi (off) input-off voltage＜0.9V, ($V_O$=0V)
Vi (on) input-on voltage＞1.1V, (0.1V＜$V_{CE}$＜0.3V)
R1 (input resistor) =22k ..Resistor ratio=1

We could base on EAR_DETECT, HSMIBIAS and ROW0 to function. EAR_DETECT used to detect “earphone plugging” and it is high active. HSMIBIAS is high active that is used to switch internal path or external earphone path. Send-end function is based on ROW0 which is low active. The three signals high/low level are shown to below.

| | EAR_DETECT | HSMIBIAS | ROW0 |
|---|---|---|---|
| **High level (V)** | 2.8 | 2.5 | 2.8 |
| **Low level (V)** | 0 | 0 | 0 |

The function status is following below:

**3.12.2.4 Status1**:

Insert the headset plug when the phone holds over idle mode without the headset plug in the jack.

| | EAR_DETECT | HSMIBIAS | ROW0 |
|---|---|---|---|
| **Status** | L | L | H |

**3.12.2.5 Status2**:

Receive an incoming call and the phone rings

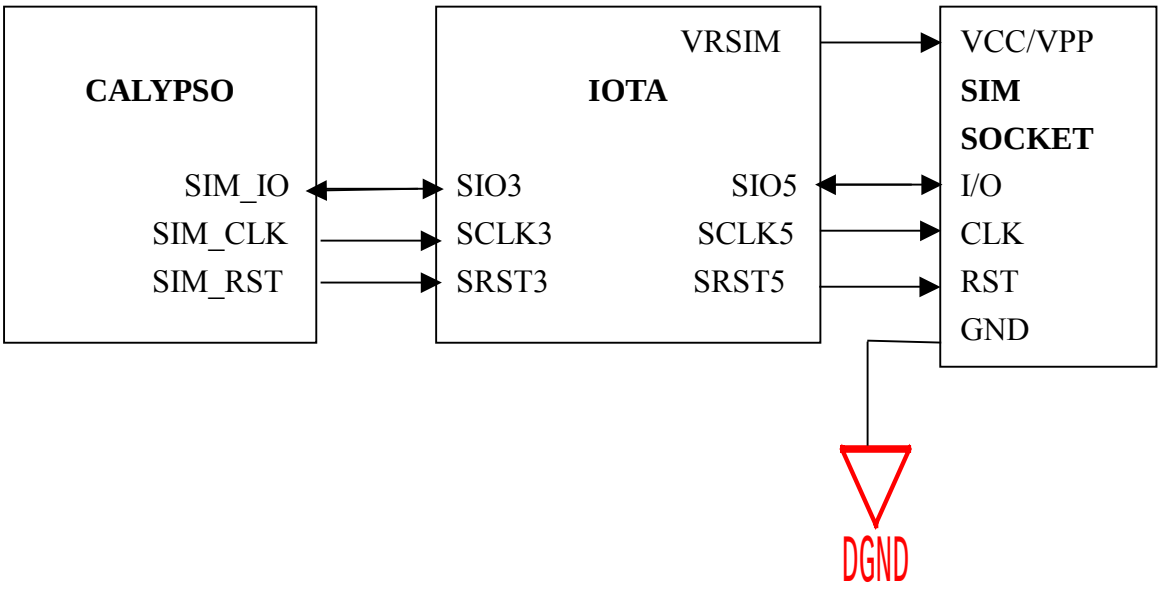
| | EAR_DETECT | HSMIBIAS | ROW0 |
|---|---|---|---|
| **Status** | L | H | H |

**3.12.2.6 Status3**:

Press the send-end key to answer the call.

| | EAR_DETECT | HSMIBIAS | ROW0 |
|---|---|---|---|
| **Status** | L | H | H to L (falling edge) |

**3.13sim circuit**




**Description**

The IOTA SIM interface is composed by a dedicated LDO and I/O level shifters. It is able to support 3V and 1.8V SIM cards.

SIM_IO: DATA

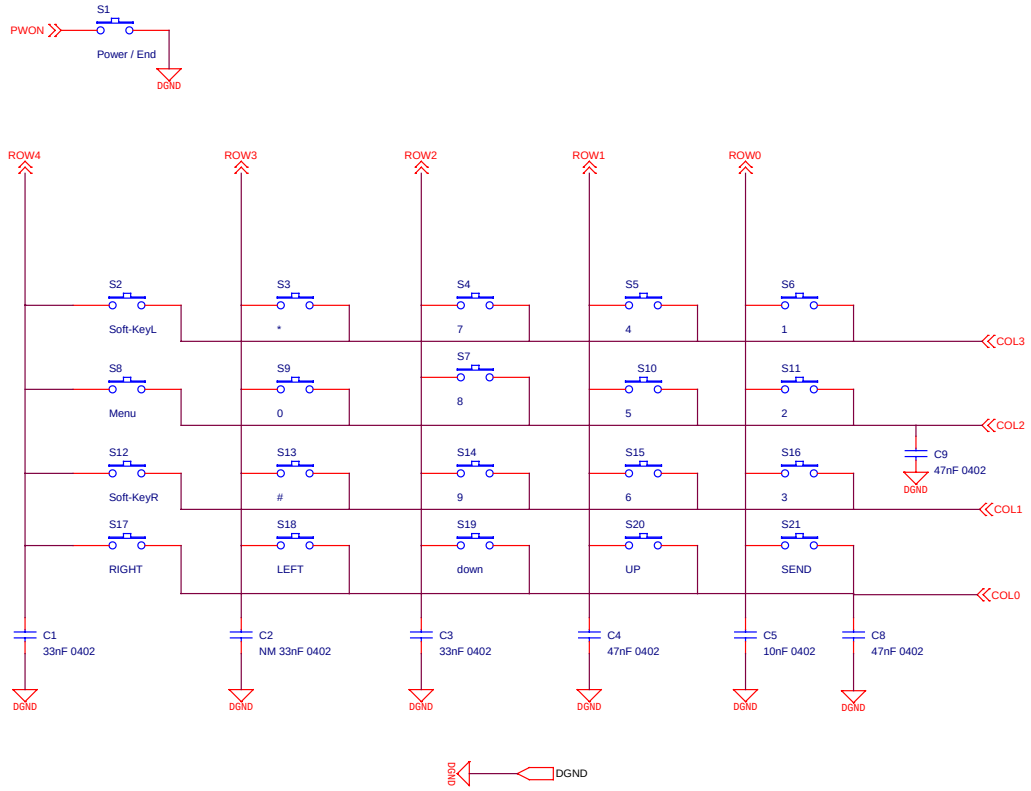
SIM_RST :Reset signal

SIM_CLK: Clock

For that reason correct enabling sequence is the following :

a. Selection of the SIM voltage and enable of the SIM LDO
b. Wait for the SIM LDO output voltage set up.
c. Enable SIM level shifter when SIMRSU=1.

## 3.14keypad circuit




## Description

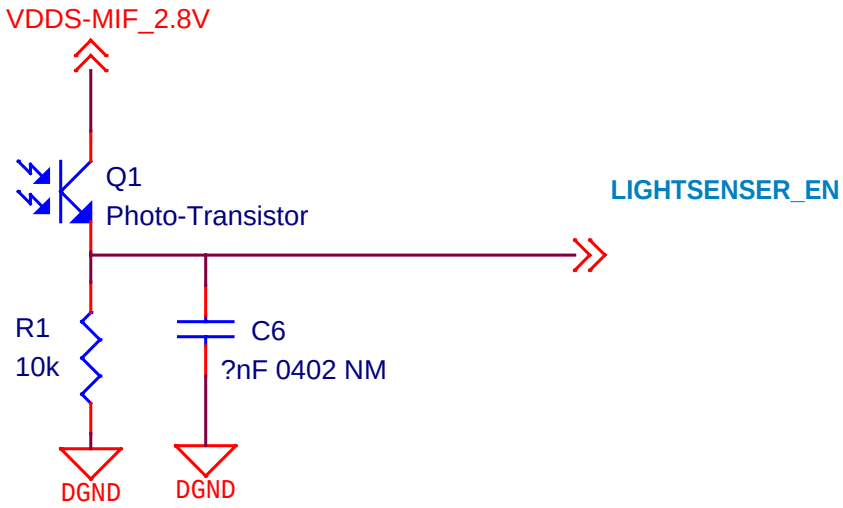
3.14.1 The keypad is made of a 5Column * 5 Row matrixes.

3.14.2 The keypad matrix is as follows:

| Function | key | Col 0 | Col 1 | Col 2 | Col 3 | Row 0 | Row1 | Row 2 | Row 3 | Row 4 |
|---|---|---|---|---|---|---|---|---|---|---|
| No/PWR | S1 | | | | | | | | | 0 |
| MEDIR | S2 | | | | 0 | | | | | 0 |
| * | S3 | | | | 0 | | | | 0 | |
| 7 | S4 | | | | 0 | | | 0 | | |
| 4 | S5 | | | | 0 | | 0 | | | |
| 1 | S6 | | | | 0 | 0 | | | | |
| MENU | S7 | | | 0 | | | | | | 0 |
| 0 | S8 | | | 0 | | | | | 0 | |
| 8 | S9 | | | 0 | | | | 0 | | |
| 5 | S10 | | | 0 | | | 0 | | | |
| 2 | S11 | | | 0 | | 0 | | | | |
| STYLE | S12 | | 0 | | | | | | | 0 |
| # | S13 | | 0 | | | | | | 0 | |
| 9 | S14 | | 0 | | | | | 0 | | |
| 6 | S15 | | 0 | | | | 0 | | | |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 3 | S16 | | 0 | | | 0 | | | | |
| RIGHT | S17 | 0 | | | | | | | | 0 |
| LEFT | S18 | 0 | | | | | | | 0 | |
| DOWN | S19 | 0 | | | | | | 0 | | |
| UP | S20 | 0 | | | | | 0 | | | |
| SEND | S21 | 0 | | | | 0 | | | | |

### 3.15 photo sensor circuit

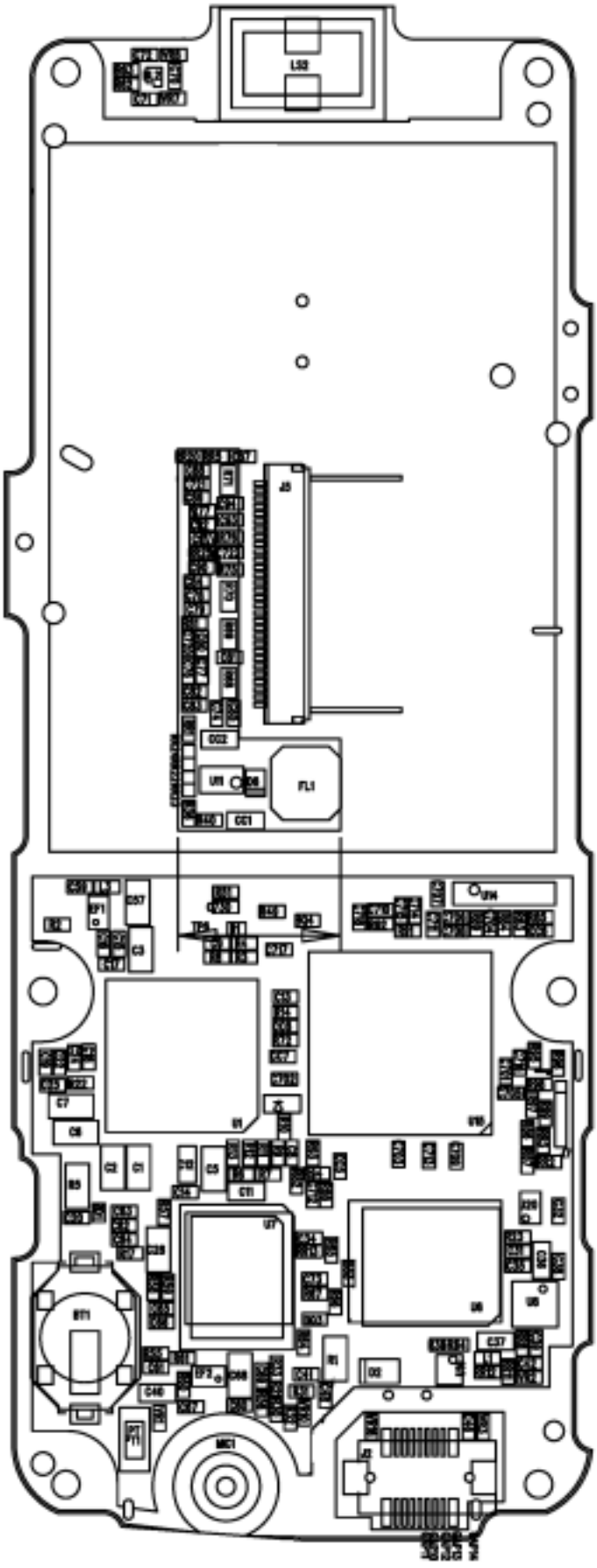



**Description**

The phototransistor is used to switch the backlight of keypad according to the R1 voltage level. This saves energy and add to stand by time .We use analog digital converter (ADC) to detect the voltage variation in the R1. The Q1 is a phototransistor. The light affect the current variation. The lightsenser_en is from the IOTA'S ADC. So we know the voltage variation, and control the backlight of keypad. If the brightness is too strong, we will turn off the LED of keypad.

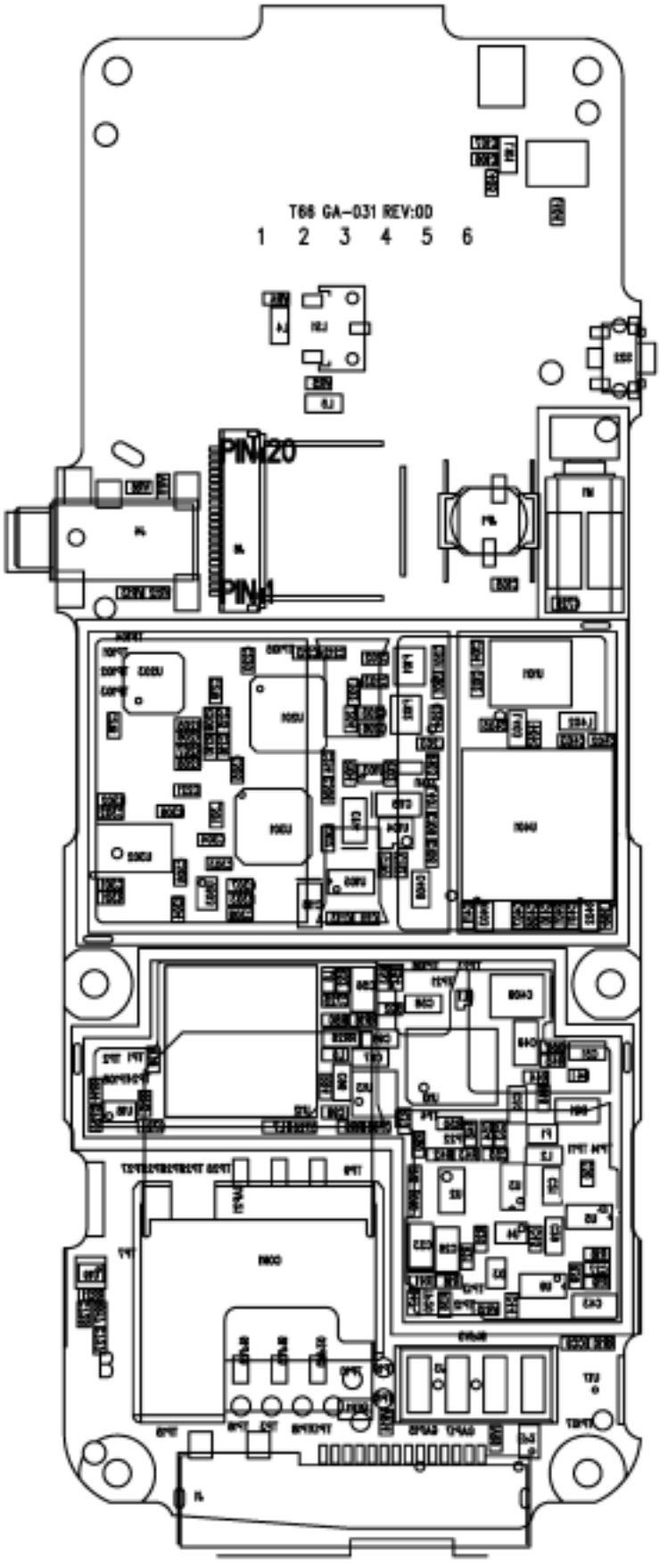
△ **Radio Frequency function Descriptions**

**Top Side**

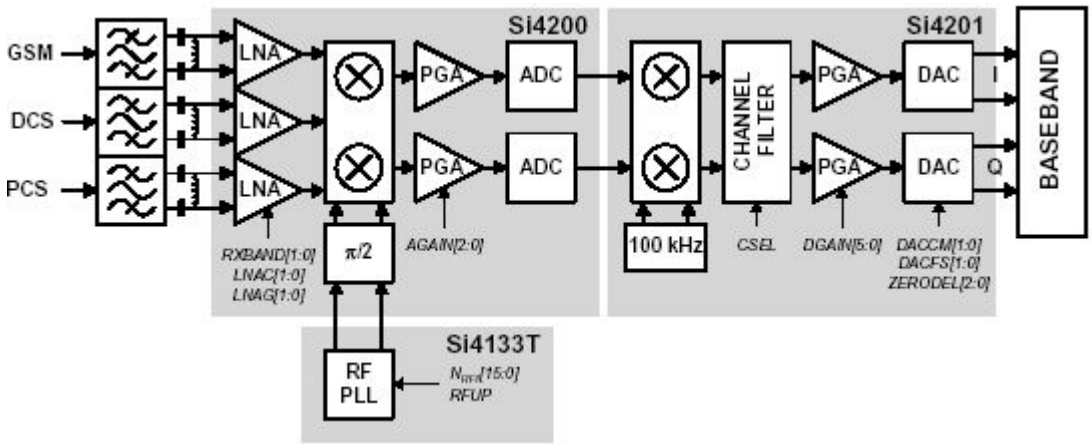


**Bot**

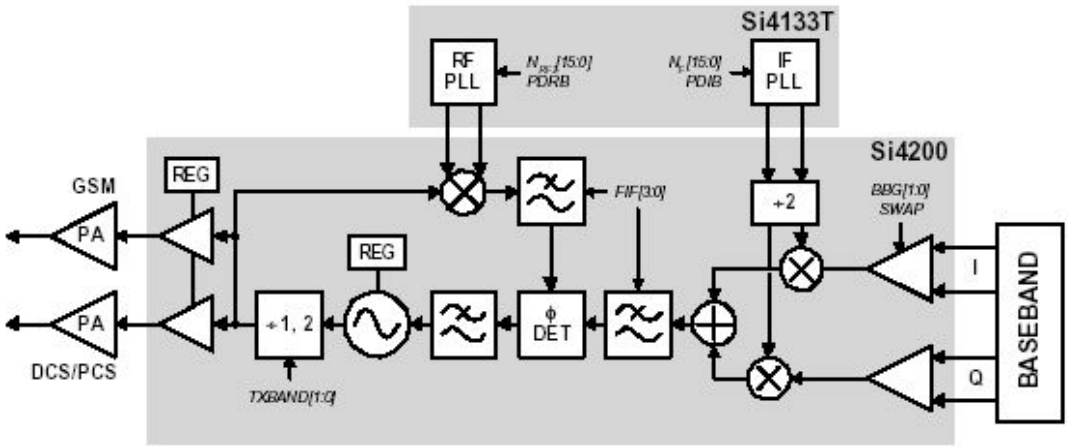
# tom Side



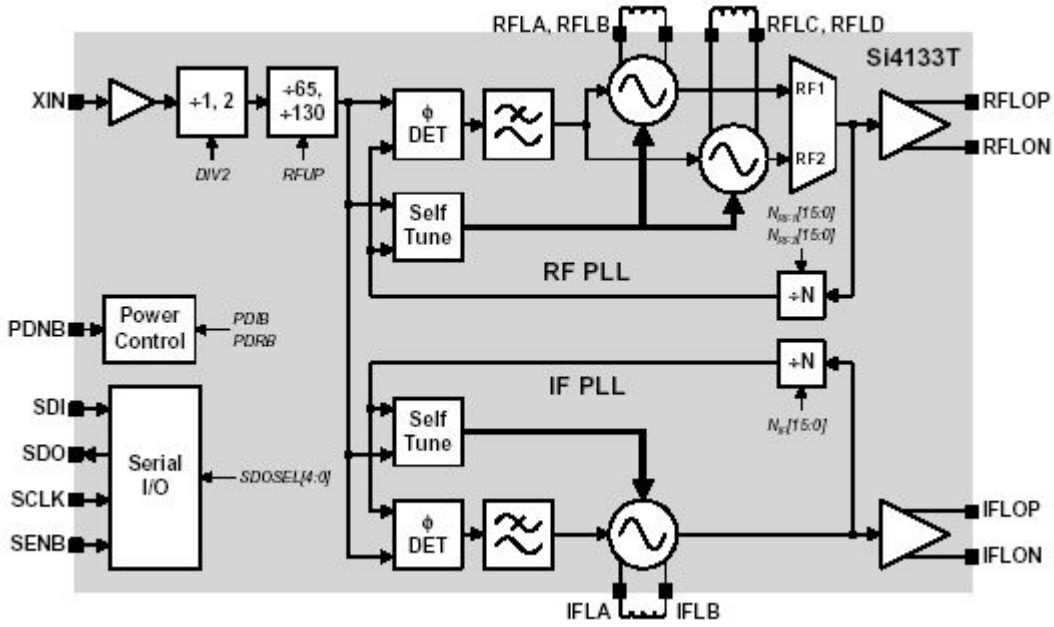
## Receiver Block Diagram




## Transmitter Block Diagram




## Frequency Synthesizer Block Diagram



1.**T/R Switch:**

U101 is a front-end switch device for GSM/DCS. The below table shows the three operating mode.

| **Mode** | Vc1 (pin2) | Vc2 (pin11) |
|---|---|---|
| GSM TX | **L** | **H** |
| DCS TX | H | L |
| **GSM/DCS RX** | L | L |

These four control signals are generated from U103, which controlled by T/R Switch.

**2.Power Amplifier:**

PA (U401) is control by signal PAENA, BS, and APC. The power controlloop is a voltage sensor.

**3.Transceiver:**

U201 is the transceiver.

**A. Receiver Operation**

Received signals from the antenna are passed to the T/R switch U101.This T/R switch contains a diplexer which filters the signal to the required receiver path (E-GSM900 or GSM1800).Pin diode switches within U101 route the signal path from the transmitter or to the receiver as required. Output signals from U101 are then applied via the SAW filter F101 or F102 to the balanced Low Noise Amplifiers (LNA) onboard U201.Output from LNAs are applied to a pair of Gilbert Cell mixers within U201.An image-reject mixer downconverts the RF signal to a 100kHz intermediate frequency (IF) with the RFLO from the U301 frequency synthesizer. The RFLO frequency is between 1737.8 to 1089.9MHz, and is divided by to in the Si4200 (U201) for GSM 850 and E-GSM 900 modes. The mixer output is amplified with an analog programmable gain amplifier (PGA), which is controlled with the internal register. The quadrature IF signal is digitized with high resolution A/D converters. The signal is then down converted by a demodulator to I and Q. The Si4201 (U203) downconverts the ADC output to baseband with a digital 100kHz quadrature LO signal.

**B. Transmitter Operation**

The transmitter chain converts differential IQ baseband signals to a suitable format for transmission by a power amplifier. A quadrature mixer upconverts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate a SSB IF signal which is filtered and used as the reference input to the OPLL. The Si4133 (U301) generates the IFLO & RFLO frequency.

## 4.Synthesizer:

U301 is a dual frequency synthesizer that performs IF and RF synthesis. Two complete PLLs are integrated including VCOs, varactors, loop filters, reference and VCO dividers, and phase detectors. Differential outputs for the IF and RF PLLs are provided for direct connection to the Si4200 (U201) transceiver. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode and uses a single VCO.