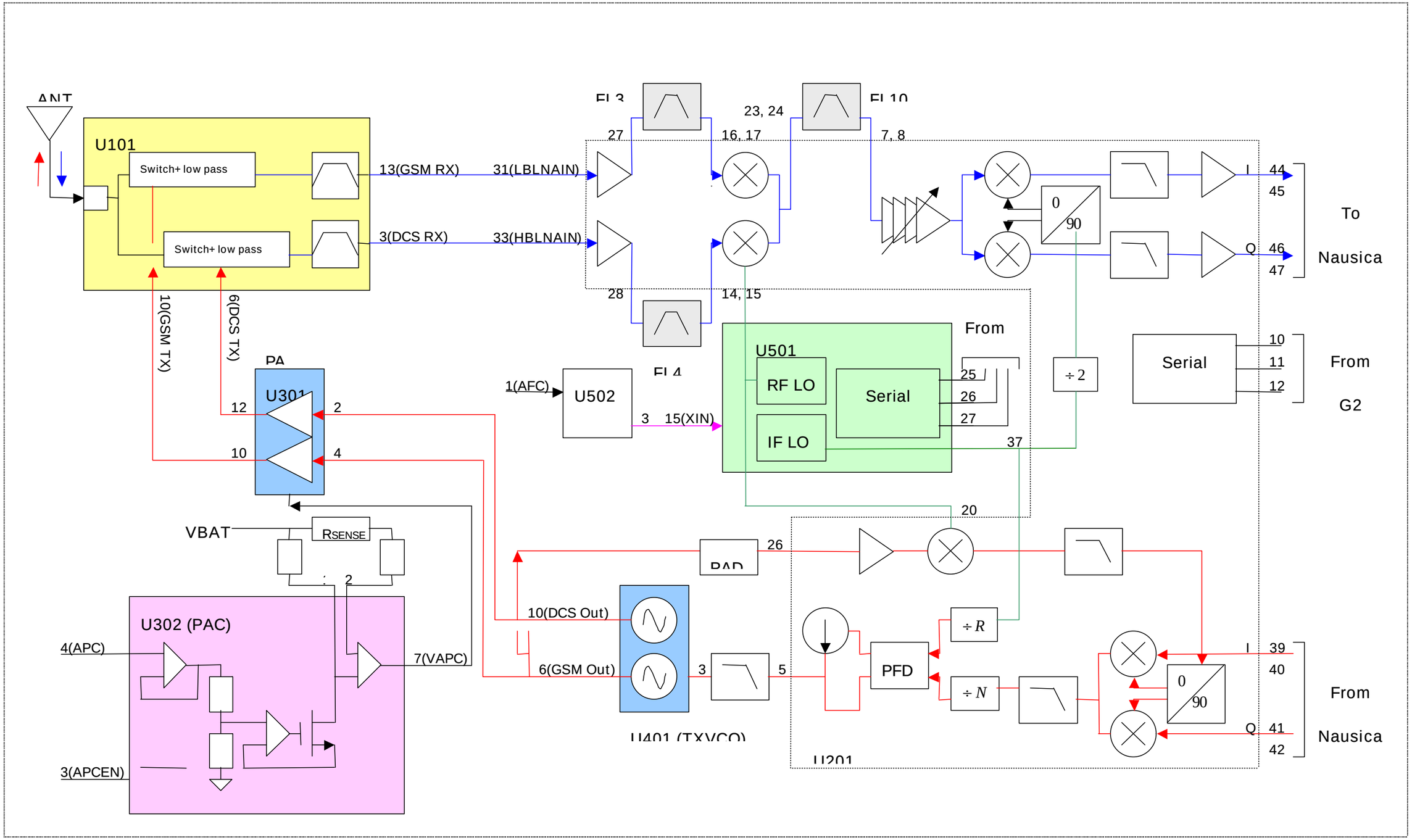
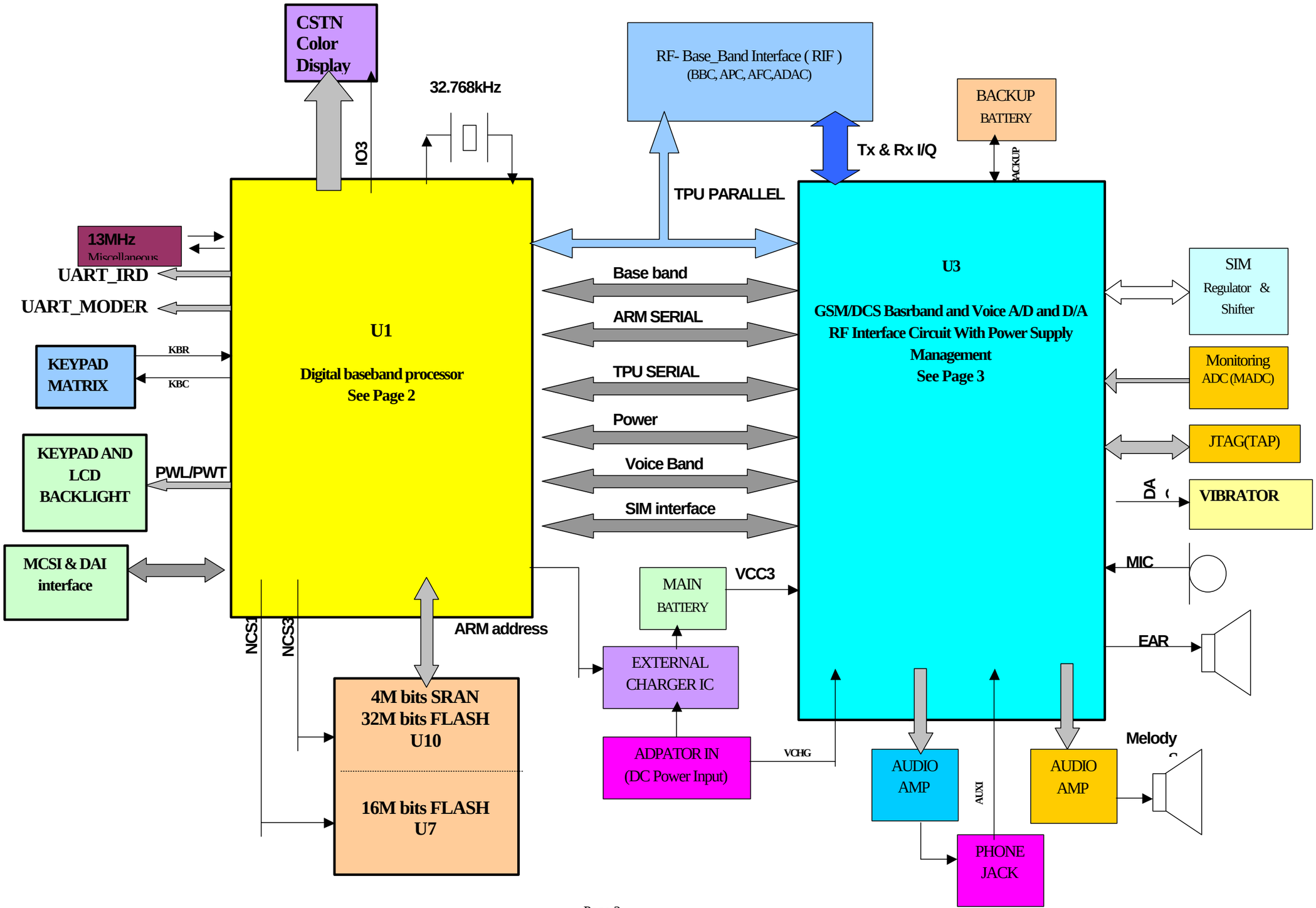
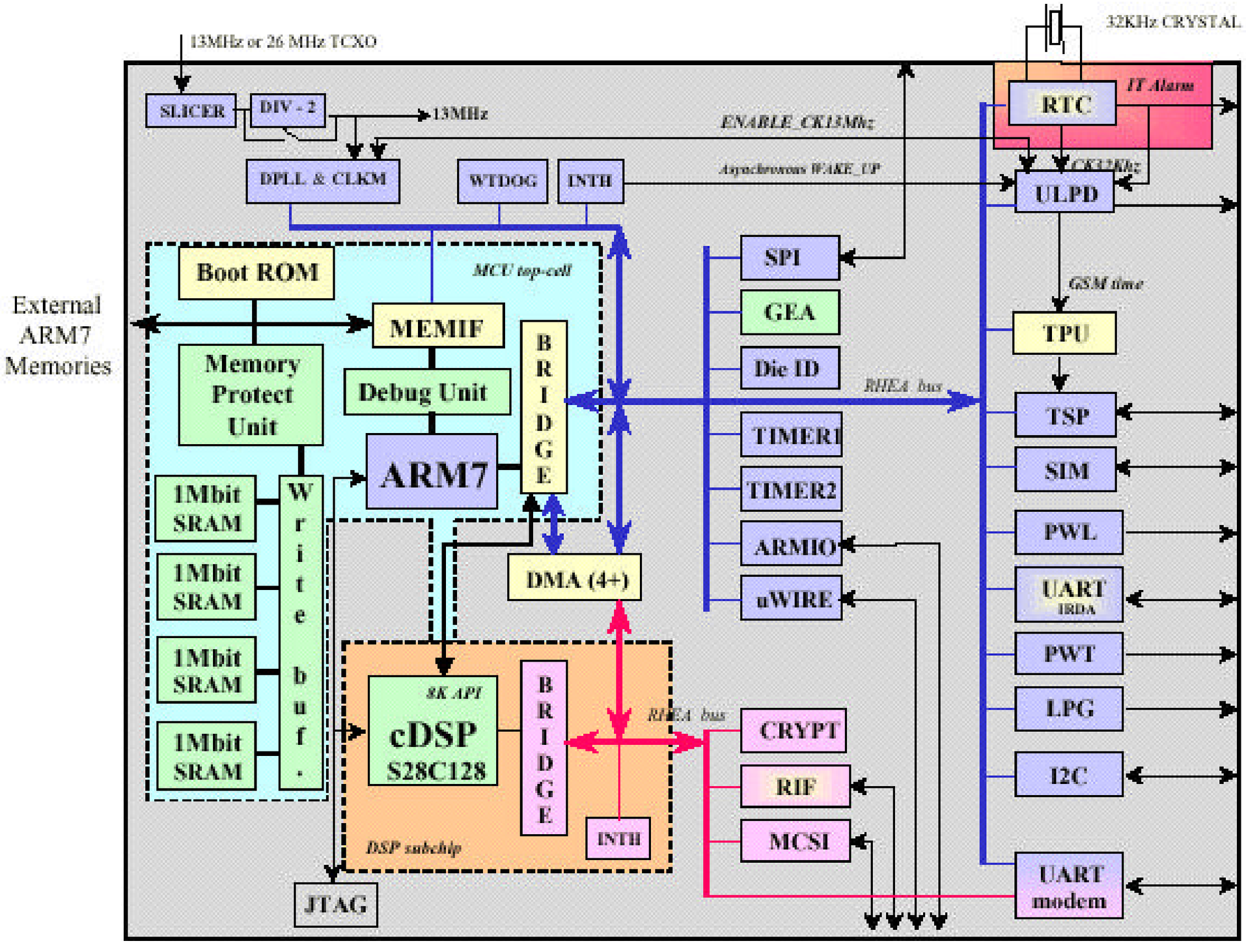
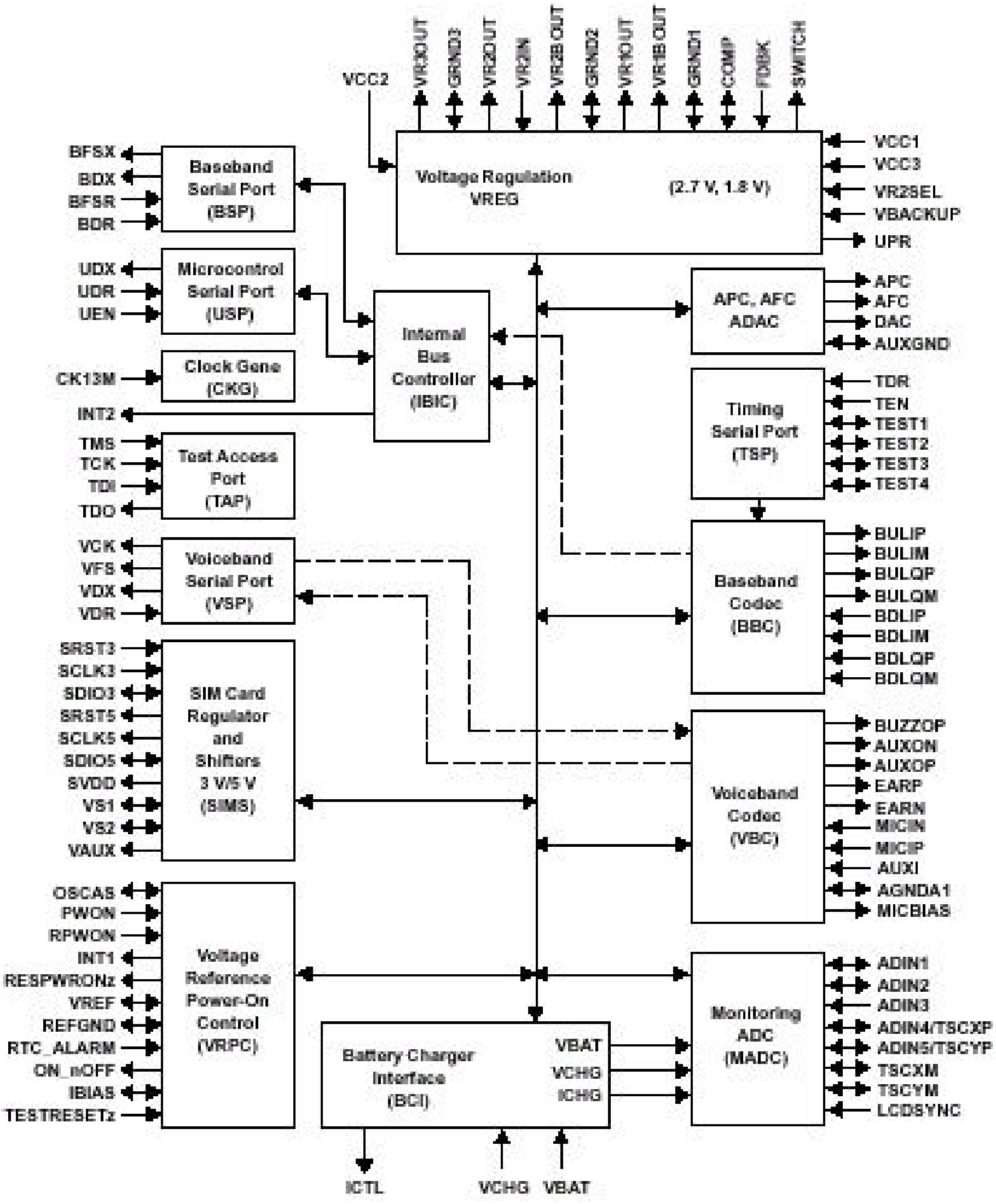
# DUAL BAND GARNET RF BLOCK DIAGRAM



# DUAL BAND GARNET Baseband BLOCK DIAGRAM



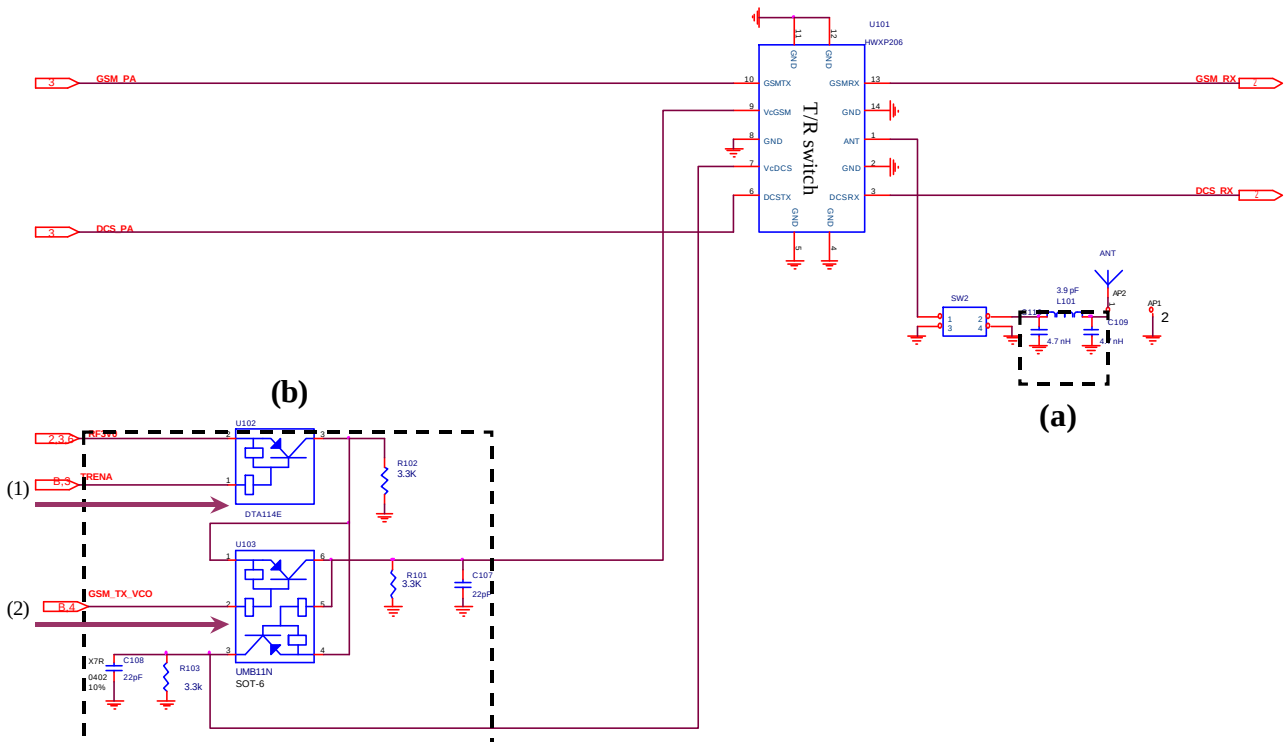

32KHz CRYSTAL
13MHz or 26 MHz TCXO
SLICER
DIV - 2
13MHz
ENABLE_CK13MHz
RTC
IT Alarm
DPLL & CLKM
WTDOG
INTH
Asynchronous WAKE_UP
CK32Khz
ULPD
External ARM7 Memories
Boot ROM
MCU top-cell
SPI
GEA
Die ID
GSM time
TPU
MEMIF
Memory Protect Unit
Debug Unit
RHEA bus
TSP
TIMER1
TIMER2
SIM
ARM7
BRIDGE
ARMIO
PWL
1Mbit SRAM
1Mbit SRAM
1Mbit SRAM
1Mbit SRAM
Write buf.
DMA (4+)
uWIRE
UART IRDA
PWT
LPG
8K API
cDSP S28C128
BRIDGE
RHEA bus
CRYPT
I2C
RIF
INTH
MCSI
DSP subchip
JTAG
UART modem


VCC2
VR3OUT
GRND3
VR2OUT
VR2IN
VR2B OUT
GRND2
VR1OUT
VR1B OUT
GRND1
COMP
FDBK
SWITCH
Voltage Regulation
VREG
(2.7 V, 1.8 V)
VCC1
VCC3
VR2SEL
VBACKUP
UPR
BFSX
BDX
BFSR
BDR
Baseband
Serial Port
(BSP)
UDX
UDR
UEN
Microcontrol
Serial Port
(USP)
CK13M
Clock Gene
(CKG)
INT2
Internal
Bus
Controller
(IBIC)
APC, AFC
ADAC
APC
AFC
DAC
AUXGND
Timing
Serial Port
(TSP)
TDR
TEN
TEST1
TEST2
TEST3
TEST4
TMS
TCK
TDI
TDO
Test Access
Port
(TAP)
VCK
VFS
VDX
VDR
Voiceband
Serial Port
(VSP)
Baseband
Codec
(BBC)
BULIP
BULIM
BULQP
BULQM
BDLIP
BDLIM
BDLQP
BDLQM
SRST3
SCLK3
SDIO3
SRST5
SCLK5
SDIO5
SVDD
VS1
VS2
VAUX
SIM Card
Regulator
and
Shifters
3 V/5 V
(SIMS)
Voiceband
Codec
(VBC)
BUZZOP
AUXON
AUXOP
EARP
EARN
MICIN
MICIP
AUXI
AGNDA1
MICBIAS
OSCAS
PWON
RPWON
INT1
RESPWRONz
VREF
REFGND
RTC_ALARM
ON_nOFF
IBIAS
TESTRESETz
Voltage
Reference
Power-On
Control
(VRPC)
Battery Charger
Interface
(BCI)
VBAT
VCHG
ICHG
Monitoring
ADC
(MADC)
ADIN1
ADIN2
ADIN3
ADIN4/TSCXP
ADIN5/TSCYP
TSCXM
TSCYM
LCDSYNC
ICTL
VCHG
VBAT

# RF section Circuit description

**RF part:**

## I. T/R switch




| RF Board Signals | | | |
|---|---|---|---|
| GSM Tx band | TRENA (1) | GSM_TX_VCO (2) | Vp-p=2.8V<br>TRENA: low<br>GSM_TX_VCO: low |
| DCS Tx band | | | Vp-p=2.8V<br>TRENA:<br>GSM_TX_VCO:<br>high(2.8V) |

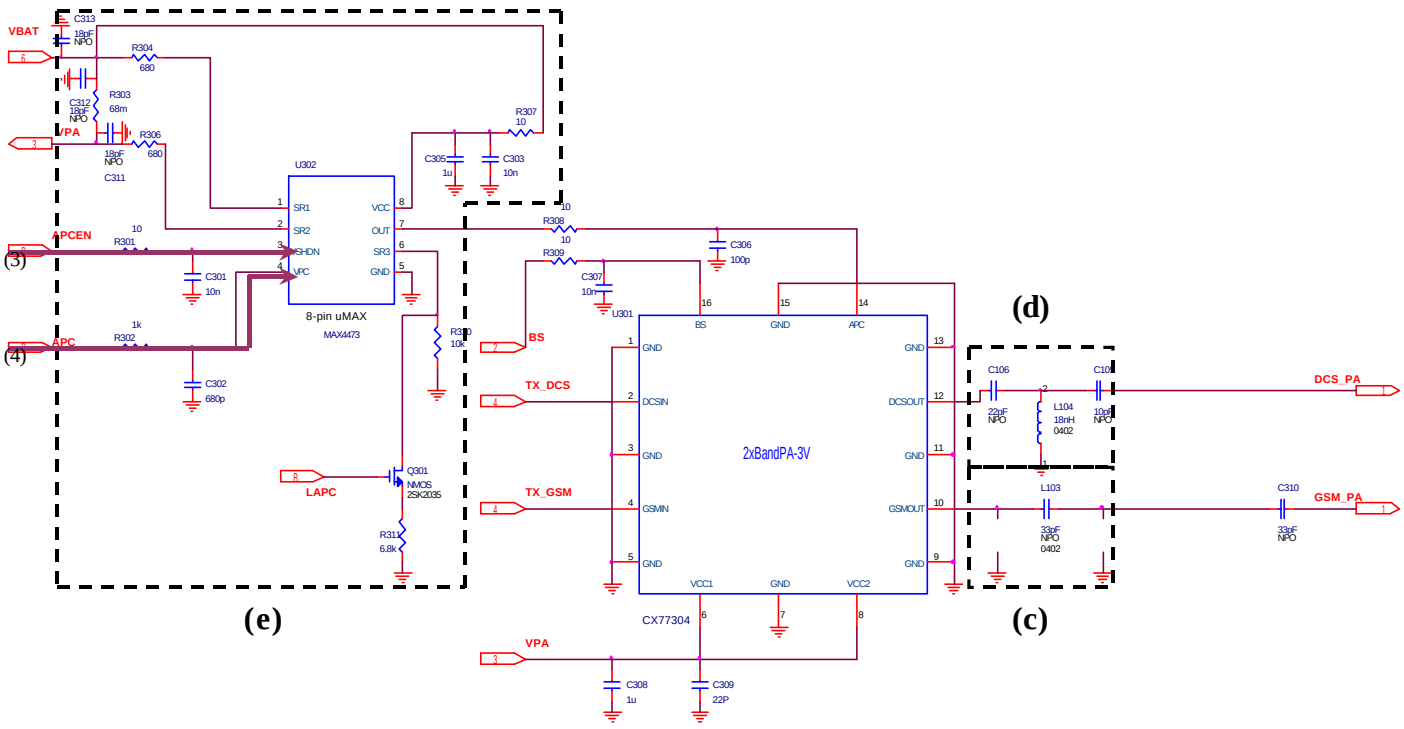
Note:

(a) Matching circuit of antenna to T/R switch.

(b) Controlled Tx and Rx in GSM and DCS band.

| GSM band | TRENA | GSM_TX_VCO |
|---|---|---|
| Tx band | L | L |
| Rx band | H | H |
| DCS band | TRENA | GSM_TX_VCO |
| Tx band | L | H |
| Rx band | H | H |

## II. PA module




| RF Board Signals | | |
|---|---|---|
| Apcena (3) | | Vp-p=2.8V<br>APC ENA<br>Vp-p=2.8V |
| APC (4) | | High level<br>GSM_APC=2.0V<br>DCS_APC=1.5V |

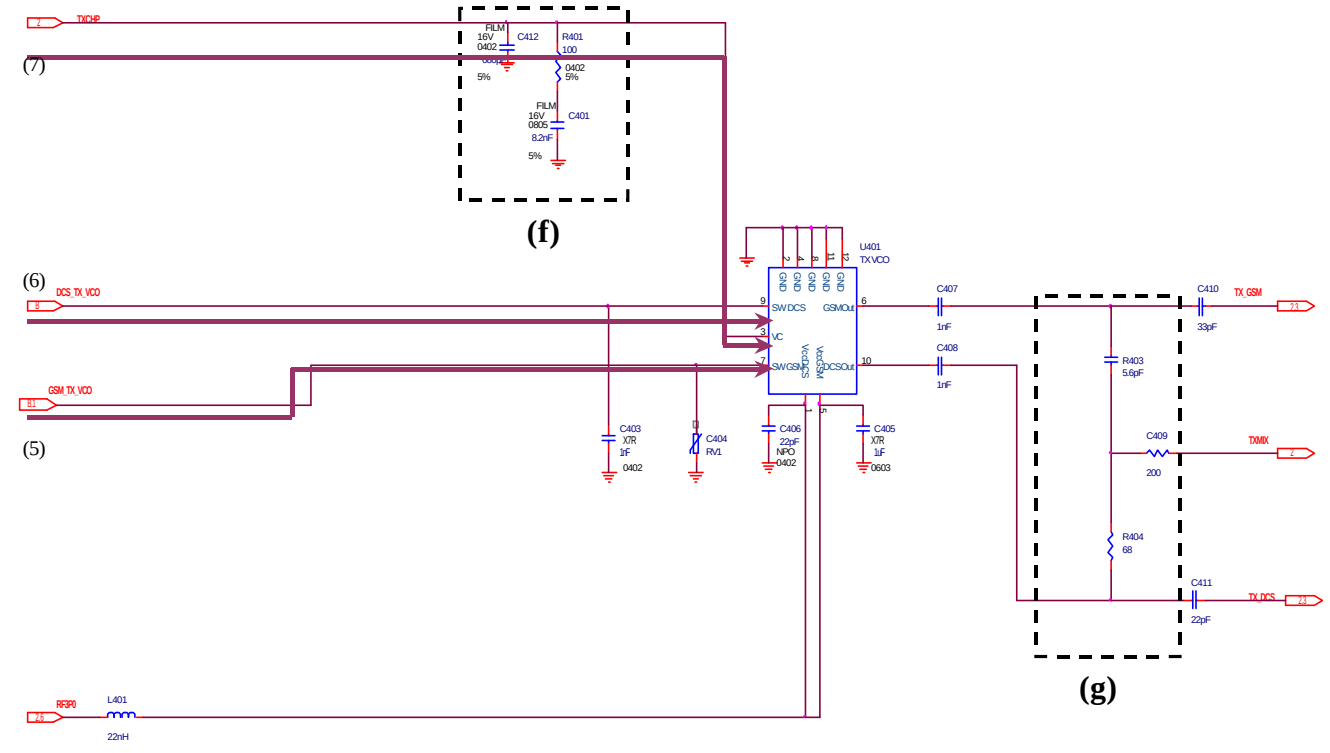
Note:

(c) PA output matching circuit in GSM band

(d) PA output matching circuit in DCS band.

(e) PA controllor

## III. Txvco



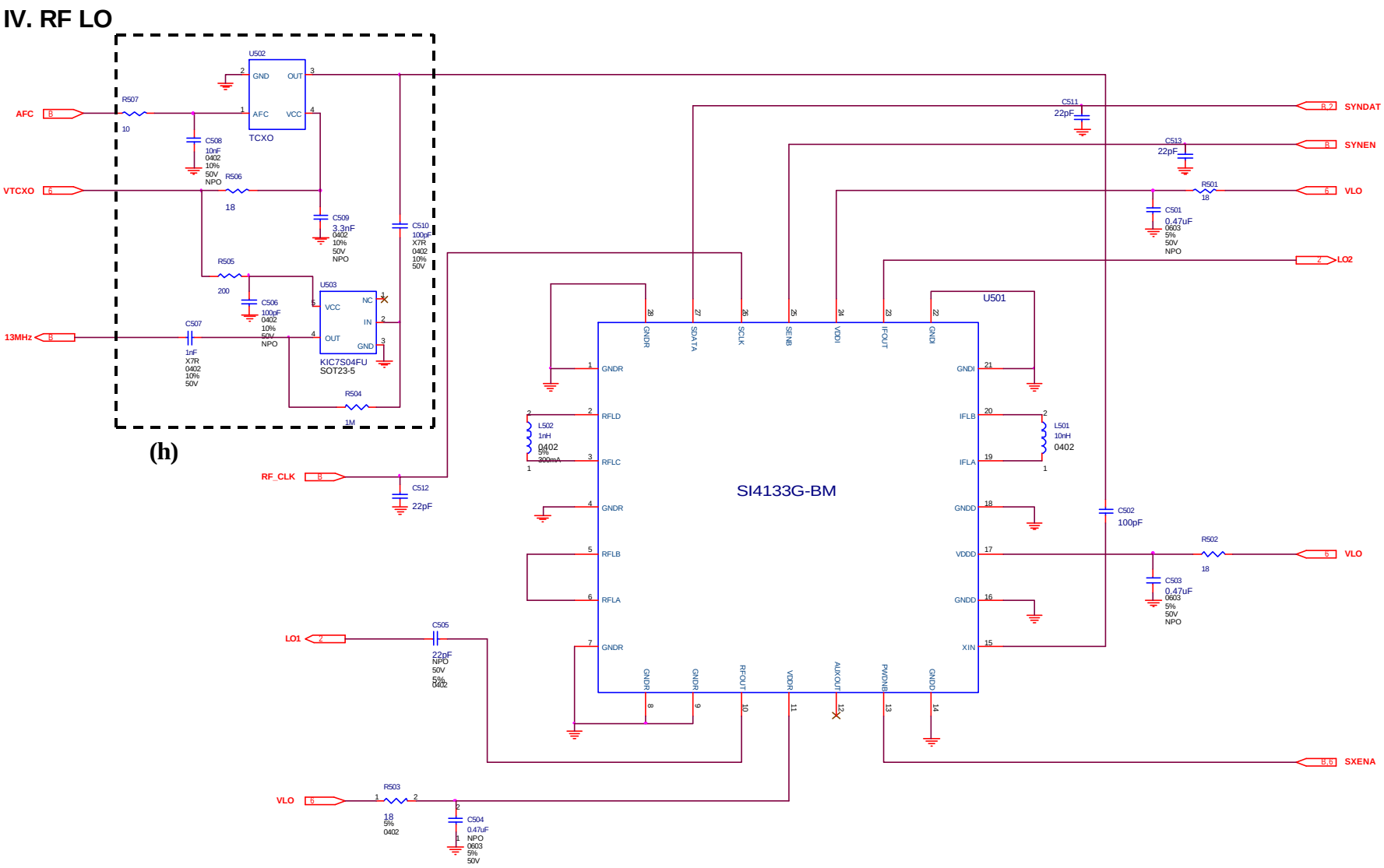

Note:

(f) 2nd order loop filter

(g) Power divider of Txvco to PA and offset mixer

| RF Board Signals | | | |
|---|---|---|---|
| GSM Tx band | GSM_TX_VCO (5) | DCS_TX_VCO (6) | Vp-p=2.8V<br>GSM_TX_VCO: low<br>DCS_TX_VCO: high |
| DCS Tx band | | | GSM_TX_VCO: high<br>DCS_TX_VCO: low |
| Charge pump (7) | GSM | DCS | Vp-p=3V |

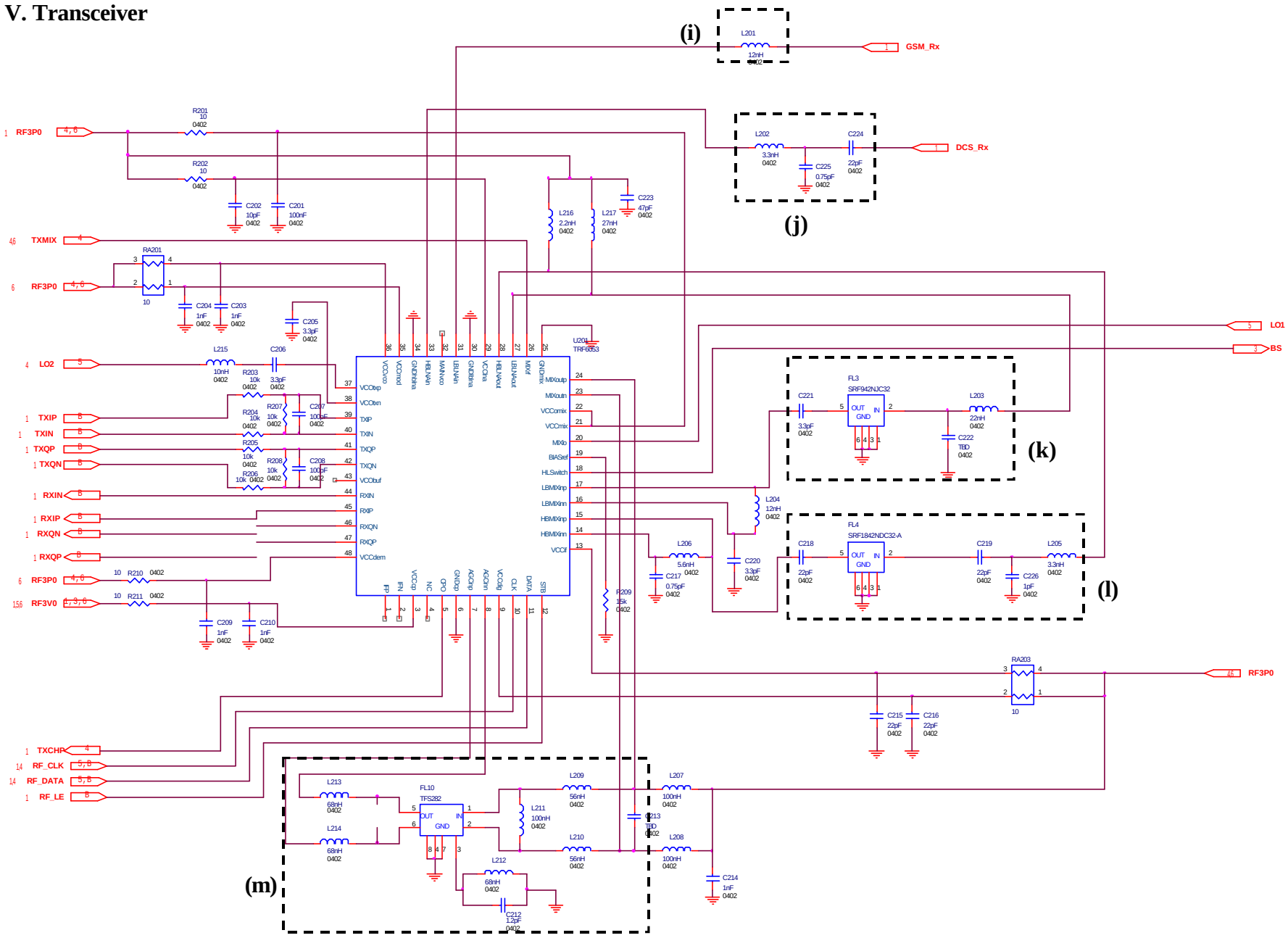
## IV. RF LO




Note:

(h) Tcxo 13MHz reference frequency to supply frequency synthesizer.

## V. Transceiver




Note:

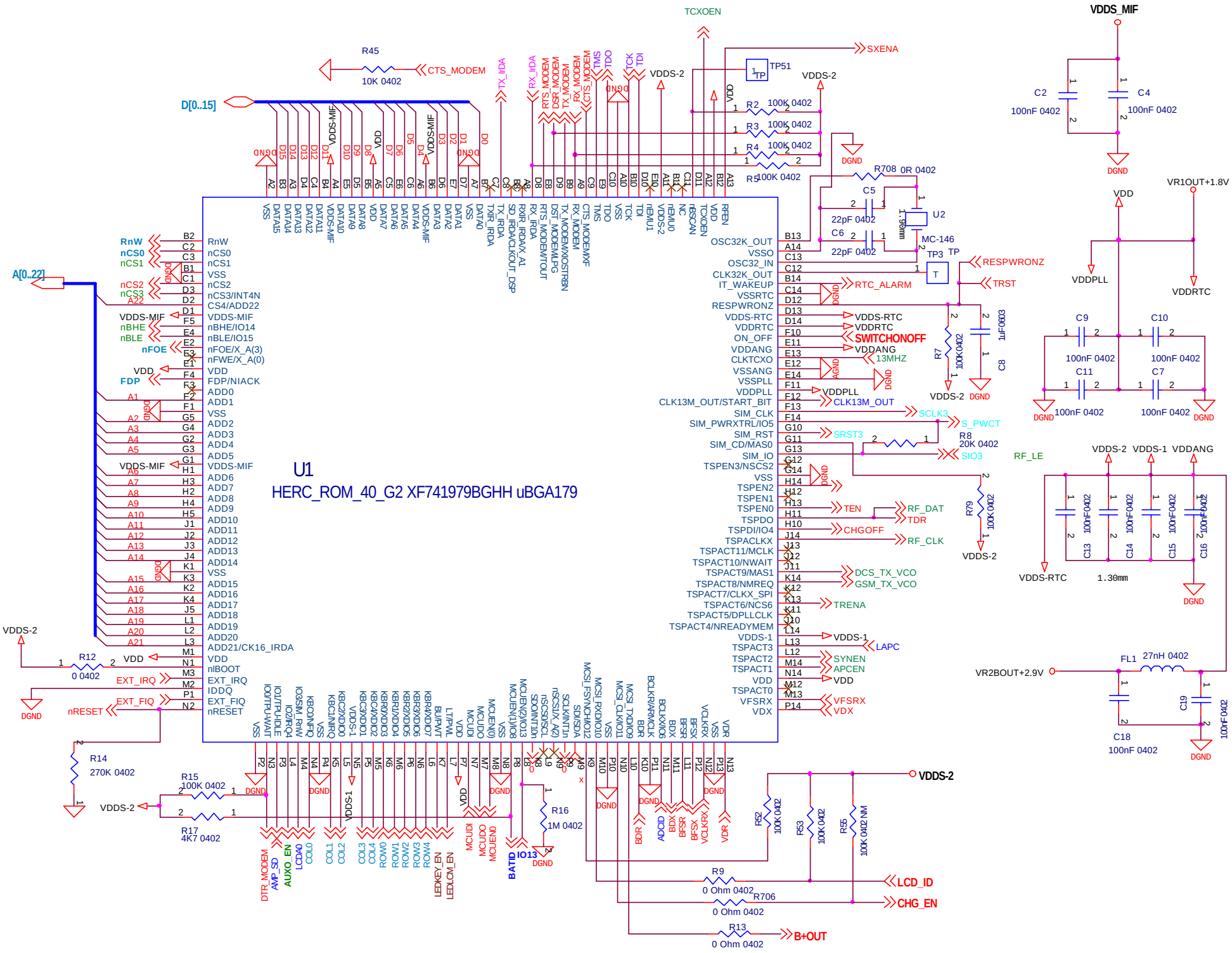
(i) T/R switch to LNA matching circuit in GSM band.
(j) T/R switch to LNA matching circuit in DCS band.
(k) GSM RF saw
(l) DCS RF saw
(m) IF saw

## VI. Regulator

# Base band Section Circuit description

## BASE BAND PART

### 1. Base Band micro controller and DSP




**POWER & GROUND :** 33 pins. Nb of use

| | | | |
|---|---|---|---|
| VDD | VCC | voltage for ASIC core & CPUs | 6 |
| VDDPLL | VCC | voltage for DPLL | 1 |
| VDDRTC | VCC | voltage for RTC split powered | 1 |
| VDDS-MIF | VCC | voltage dedicated to memory interface | 4 |
| VDDS-RTC | VCC | voltage dedicated to RTC split powered I/Os | 1 |
| VDDS-1 | VCC | voltage for ASIC I/Os | 2 |
| VDDS-2 | VCC | voltage for ASIC I/Os | 1 |
| VSS | | common ground for ASIC core, I/Os and CPUs | 12 |
| VSSPLL | | ground dedicated to DPLL | 1 |
| VSSRTC | | ground dedicated to RTC split powered | 1 |
| VDDANG | | Analog VCC for clock squarer. | 1 |
| VSSANG | | Analog ground for clock squarer | 1 |
| VSSO | | Reference ground for 32KHz oscillator. | 1 |

**TPU SERIAL PORT :** 7 pins. Reset

| | | | |
|---|---|---|---|
| TSPDO | OUT | Output serial data. | 0 |
| TSPDI | IN | Input serial data (VEGA3 compatibility only) | input |
| TSPEN(3) | OUT | Configurable triggers (edge/level) | 1 |
| TSPEN(2) | OUT | Configurable triggers (edge/level) | 0 |
| TSPEN(1:0) | OUT | Configurable triggers (edge/level) | 11 |
| TSPCLKX | OUT | Transfer serial clock (VEGA3 compatible) | 0 |

| **SIM INTERFACE :** 6 pins. | | | Reset |
|---|---|---|---|
| SIM_RST | OUT | Sim reset. | 0 |
| SIM_PWCTRL | OUT | Power Control. | 0 |
| SIM_IO | IN/OUT | Input output signal. | 0 |
| SIM_CLK | OUT | Output clock. | 0 |
| SIM_CD | IN | Card detect (Pull High) | Input |
| SIM_RnW | OUT | Used for IO3 | 0 |

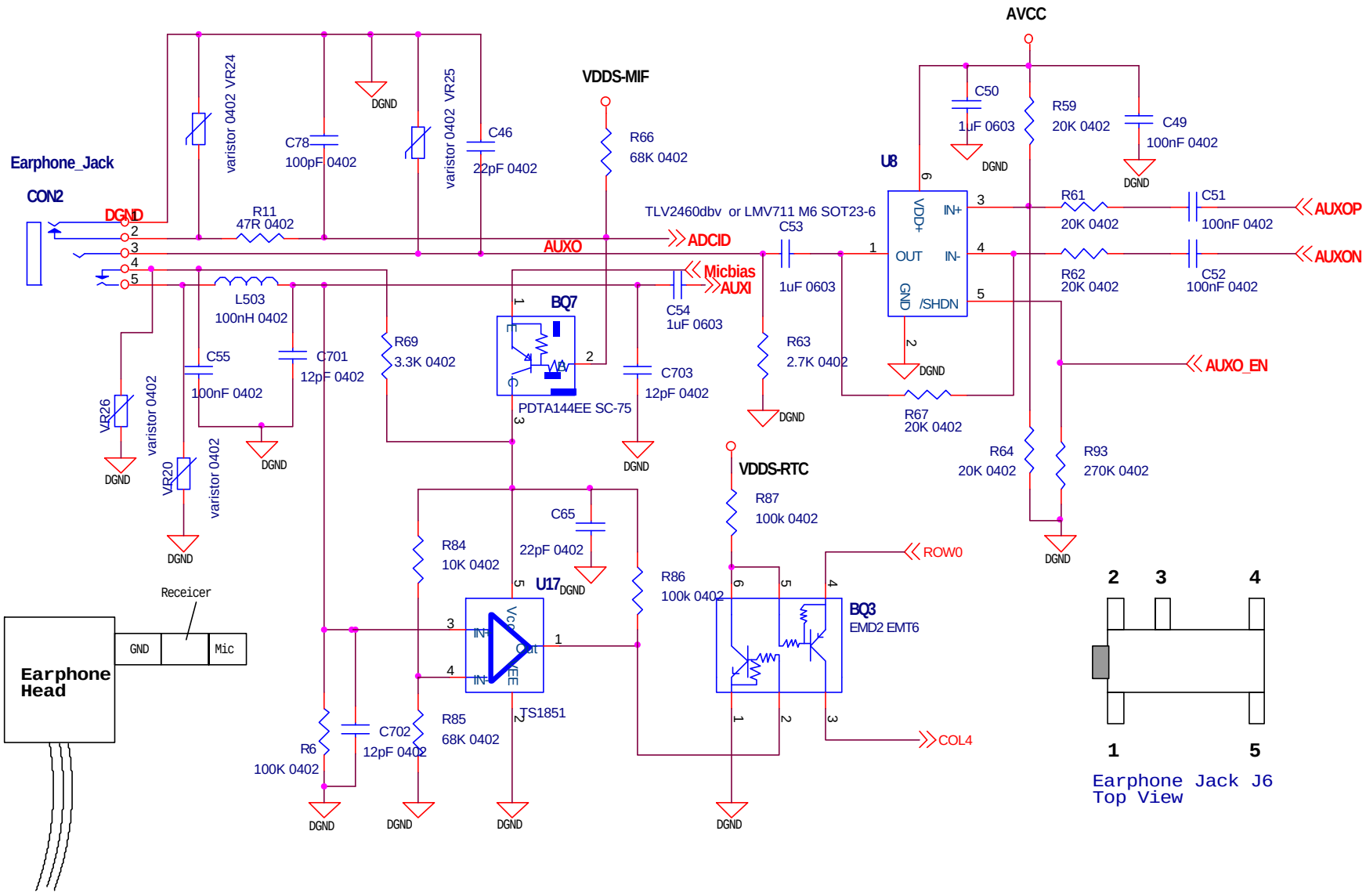
| **VOICE BAND INTERFACE :** 4 pins. | Pull | | Reset |
|---|---|---|---|
| VCLKRX | IN | Transmit / Receive clock. | Input |
| VDX | OUT | Transmit Data. | 0 |
| VDR | IN | Receive data. | Input |
| VFSRX | IN | Transmit / Receive Synchro. | Input |

| **MCSI INTERFACE :** 4 pins. | | Pull | Reset |
|---|---|---|---|
| MCSI_TXD | OUT | Used for IO9 | 0 |
| MCSI_RXD | IN | Receive serial data | Input |
| MCSI_CLK | IN/OUT | Bit synchronization clock | Input |
| MCSI_FSYNCH | IN/OUT | Frame synchronization clock or SS reset | Input |

| **ARM SERIAL PORT :** 5 pins. | | Pull | Reset |
|---|---|---|---|
| MCUDI | IN | Input serial data. | Input |
| MCUDO | OUT | Output serial data. | 0 |
| MCUEN(2:0) | OUT | Configurable enable triggers (edge/level) | 111 |

| | | | |
|---|---|---|---|
| CLKTCXO | IN | VCTXO input clock (13MHz or 26MHz). | Input |
| CLK13M_OUT | OUT | CLKM output clock (13MHz). | 0 |
| OSC32K_ IN | IN | Input component signal of 32KHz quartz. | Input |
| OSC32K_OUT | IN | Output component signal of 32KHz quartz. | Input |
| CLK32K_OUT | OUT | 32.768KHz Square Waveform Output with test point TP3 | |

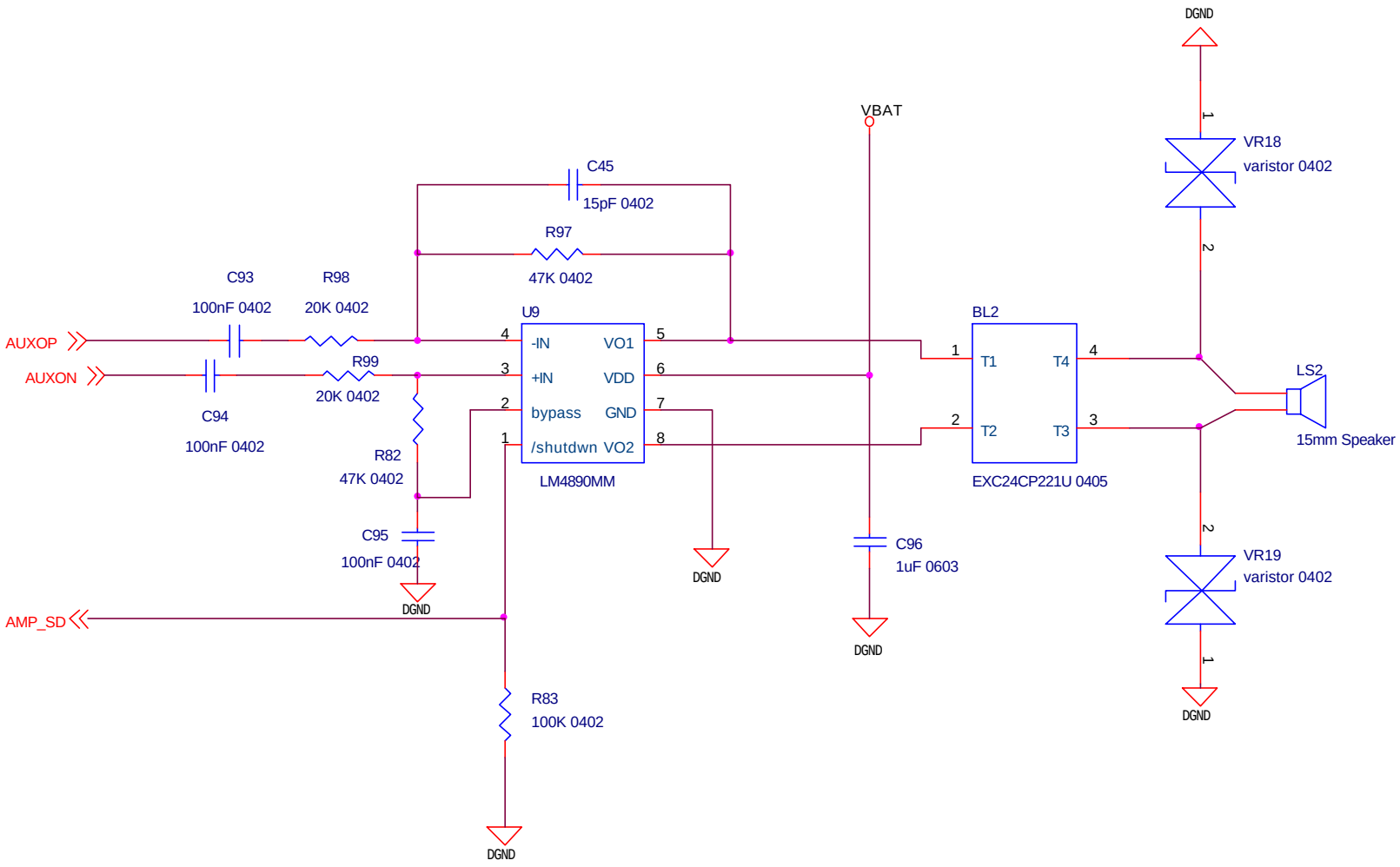
## 2. Earphone I/O control circuit, Send/End key acceptable




In order to pass a signal without distortion due to insufficient SR, the amplifier must have at least the maximum SR of the signal.
Situation. U8 is OP-AMP to support sufficient SR from AUXOP & AUXON.
U8 enable by AUXO_EN pull high.
Terminal 1 & 2 , Terminal 4 & 5 are short and ADCID change to low level when earphone head insert to the phone jack.
BQ7 can pass Microphone DC Bias 2V through CON2 pin 4 to earphone' s microphone when earphone has been inserted to CON2.
Microphone bias exist 2VDC when incoming call alerting and remain 2VDC during speech state till end call.
U17 is an OP-AMP used to compare the partial voltage of Microphone bias to difference the SEND/END key has been pressed or not.
Earphone microphone is a normal close circuit and should be opened when SEND/END key has been pressed.

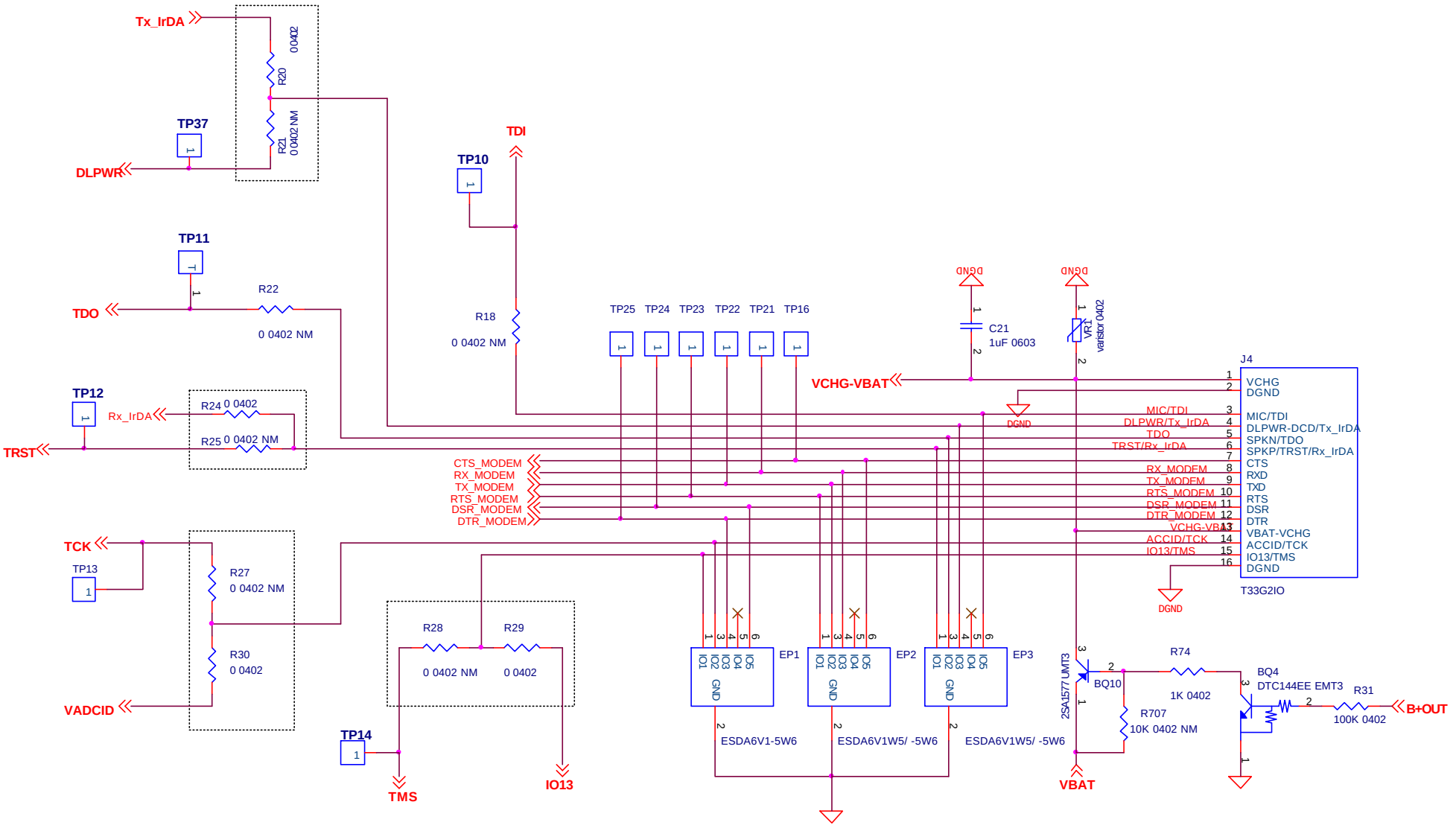
| Condition of SEND/END key | Voltage of U17 pin 3 ( OP-AMP + ) | Voltage of U17 pin 4 ( OP-AMP - ) | Voltage U17 pin 1 (OP-AMP output) | BQ3 Row 0 & Col 4 state |
|---|---|---|---|---|
| Pressed | 2VDC | 1.74VDC | 2V | Short |
| No Press | 1VDC | 1.74VDC | 0V | Open |

## 3. Melody & ring tone circuit




AUXOP and AUXON have same frequency response but with 180 degree difference.
These two signal s have 1.2VDC carrier and 620mVp-p max AC signal
U9 audio amplifier should work with AMP_SD 2.85VDC HIGH
Output of U9 have same frequency response but with 180 degree difference
These two output signal have 2VDC carrier and 1.75 Vp-p max AC signal

## 4. Earphone I/O control circuit, Send/End key acceptable




B+OUT High support external DC power drain

Modem port default work with Data Cable

VADCID detect accessory insert ( Data cable has 82k ohm for identification)

VCHG-VBAT support charger adaptor in with ( Linear Adaptor 3.6V 600mA )

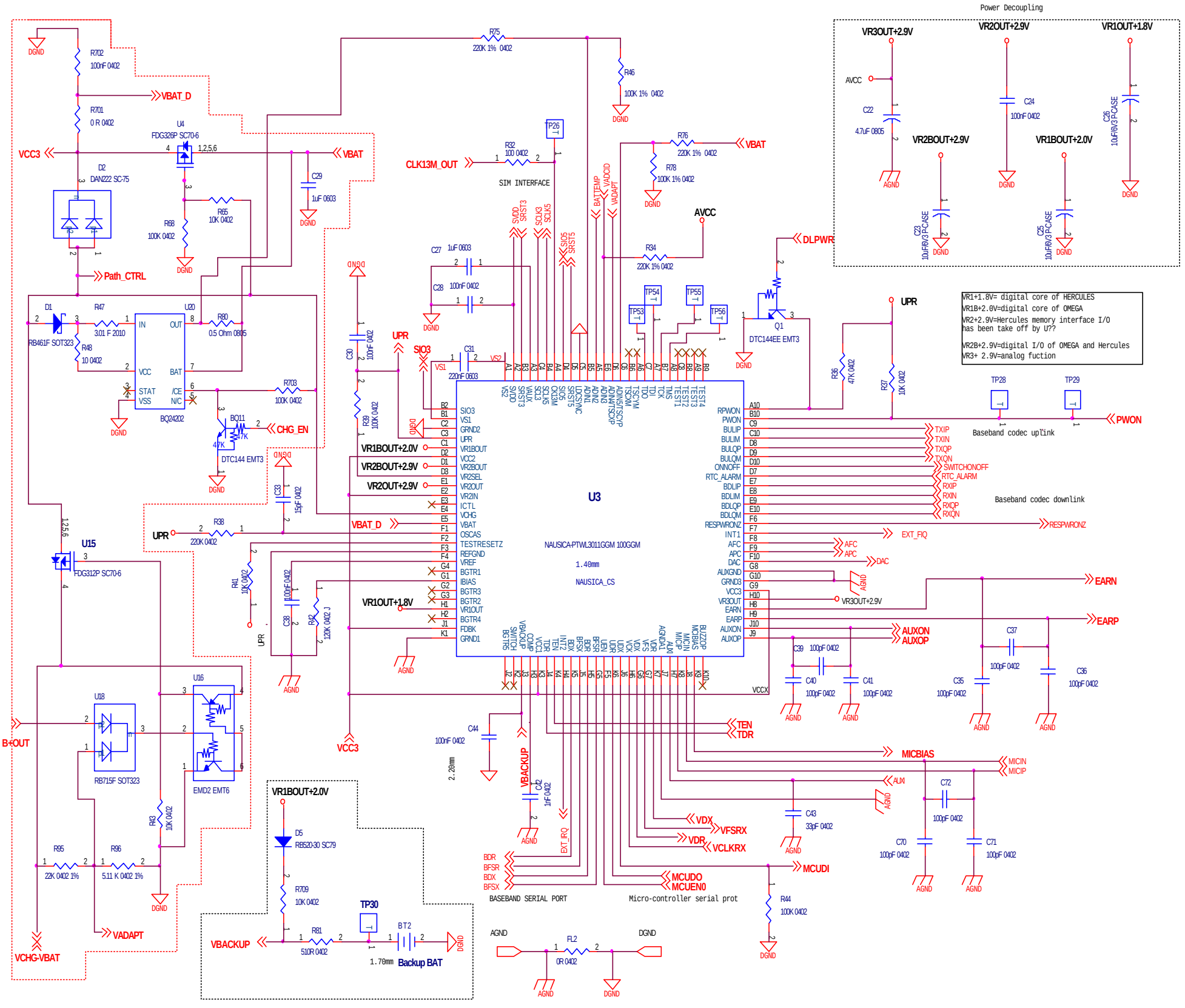
Component EP1, EP2, EP3 and VR1 used for ESD protect

TPx are test points on board

### Data I/O connector J4 Pin define and functional description

| Connector IO number | Function | Description |
|---|---|---|
| S1 | VCHG | Charging power input |
| S2 | DGND | Charging Ground |
| S3 | TDI | From PC-JTAG ( need jumper resistor) |
| S4 | Tx_IrDA | Trace Tx |
| S5 | TDO | To PC-JTAG (need jumper resistor) |
| S6 | Rx_IrDA | To PC-JTAG TRST (no used) / Trace Rx |
| S7 | CTS_Modem | From PC- DTR |
| S8 | RXD_Modem | From PC-TXD |
| S9 | TXD_Modem | To PC-RXD |
| S10 | RTS_Modem | From PC- DSR |
| S11 | DSR_Modem | To PC-RTS |
| S12 | DTR_Modem | To PC-CTS |
| S13 | B+OUT | To Accessory power input |
| S14 | VADCID | From PC-JTAG TCK(need jumper resistor)/HF-ID |
| S15 | IO13 | To PC-JTAG TMS(need jumper resistor) / No Use. |
| S16 | DGND | Ground |

## 5. D/A , A/D & Codec base band chip and External Charger IC



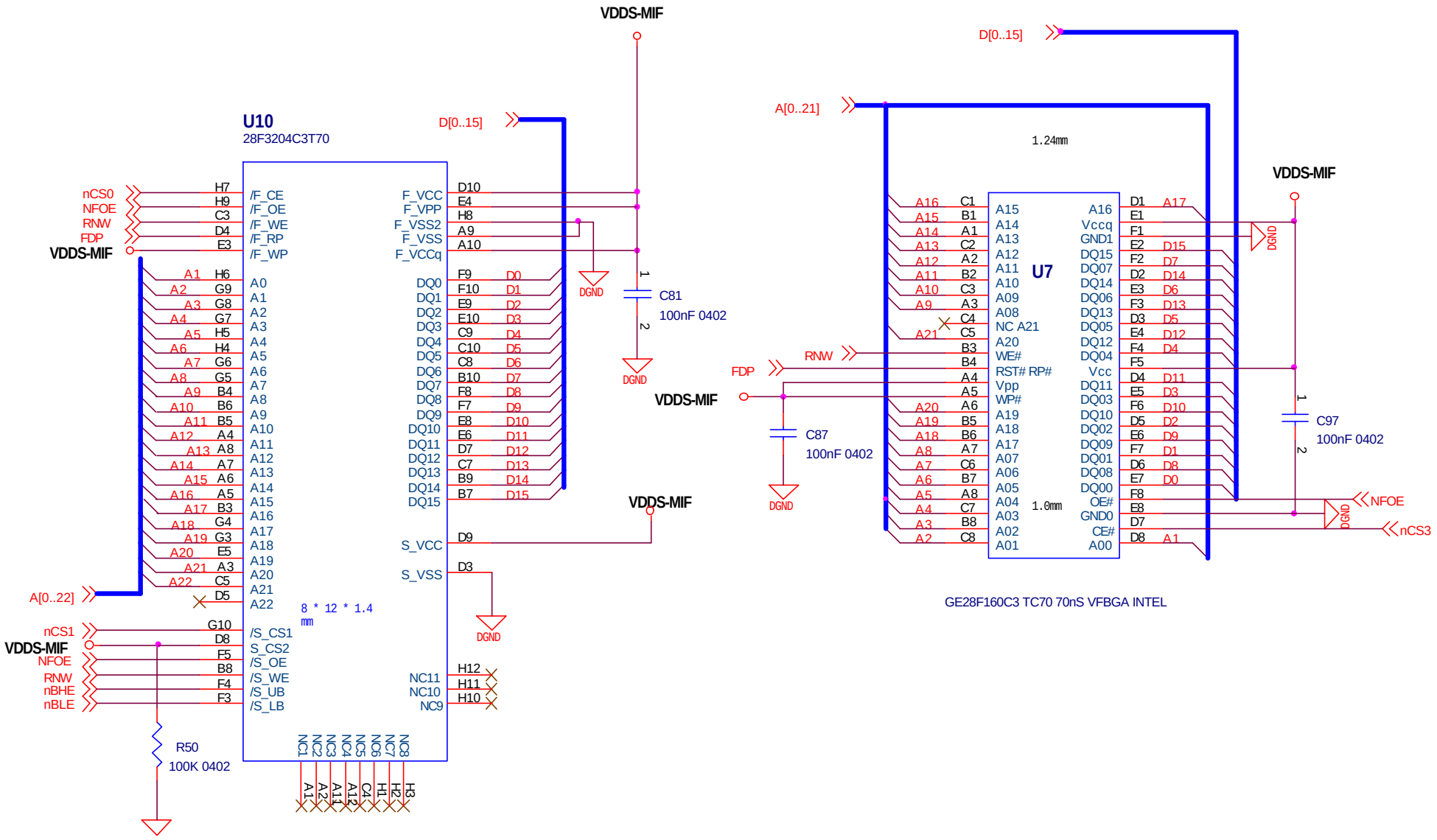

| | |
|---|---|
| PWON | Power On button input and should be used in Pullup state |
| SWITCHONOFF | Output for Mobile ON or OFF |
| RESPWRONz | Output for Mobile power-on reset |
| RPWON | Input for Remote power-on and should be used in Pullup state |
| UPR | Output for Uninterrupted power rail output and need External capacitor |
| TESTRESETz | Reset input for test mode only should be Pullup |
| OSCAS | I/O Internal low-power oscillator adjustment with External RC |
| VBAT_D | Battery voltage sense input External capacitor |
| VCC1 | Input of dc-dc with External capacitor |
| VCC2 | Input of regulator VR1B, VR2, VR2B, and charge pump with External capacitor |
| VCC3 | Input of regulator VR3 and VDD pin for VRPC analog External capacitor |
| VR2IN | Regulator VR2 input Optional FDBK |
| VR2SEL | Select voltage of VR2BOUT |
| FDBK | DC-DC converter, feedback input, VR1 input |
| Path_CTRL (VCHG) | Charger voltage input External capacitor |

| | |
|---|---|
| VREF | I/O Reference voltage (1.2 V) External capacitor |
| VR1OUT | Regulator VR1 output with External capacitor |
| VR2OUT | No used for Regulator VR2 output with External capacitor 100nF |
| VR3OUT | Regulator VR3 output with External capacitor |
| VR1BOUT | Regulator VR1B output with External capacitor |
| VR2BOUT | Regulator VR2B output with External capacitor |
| RTC_ALARM | Real-time clock wake-up input |

Back up battery: Reset RTC backup battery if open circuit voltage of RTC battery below 2.36VDC
Charging currnet –680uA MAX
Charging threshold = 2.95VDC
Discharge current under normal turn off condition = 65 uA MAX
Discharging current under emergency condition = 120 uA MAX
External charger IC circuit: U20 with 4.2VDC regulation voltage and 500 mA limit internal power MOSFET
U15, U16, U18 together support over charge protect for 6.5V S/W control and 7V H/W control
Charging & Discharging: Over discharge condition if main battery VBAT < 3.2V
Charging complete if VBAT > 4.17 and charging current < 100 mA

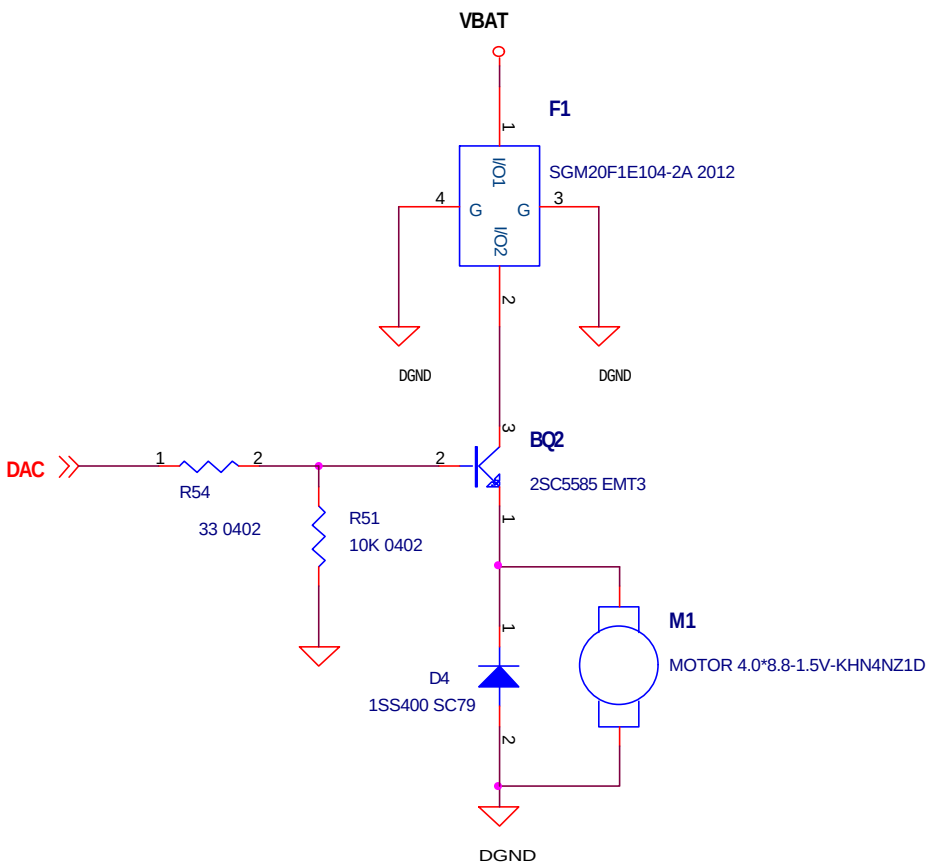
| | | |
|---|---|---|
| BDLIM | I | In-phase input (I–) baseband codec downlink |
| BDLIP | I | In-phase input (I+) baseband codec downlink |
| BDLQM | I | Quadrature input (Q–) baseband codec downlink |
| BDLQP | I | Quadrature input (Q+) baseband codec downlink |
| BDR | I | Baseband serial port receive data |
| BDX | O | Baseband serial port transmit data |
| BFSR | I | Baseband serial port receive frame synchronization |
| BFSX | O | Baseband serial port transmit frame synchronization |
| BULIM | O | In-phase output (I–) baseband codec uplink |
| BULIP | O | In-phase output (I+) baseband codec uplink |
| BULQM | O | Quadrature output (Q–) baseband codec uplink |
| BULQP | O | Quadrature output (Q+) baseband codec uplink |
| SIO3 | I/O | SIM card shifters data (3 V) External pullup |
| SIO5 | I/O | SIM card shifters data (3 V/5 V) External pullup |
| SRST3 | I | SIM card shifters reset input (3 V) |
| SRST5 | O | SIM card shifters reset output (3 V/5 V) |
| SVDD | O | SIM card supply (3 V/5 V) should with External capacitor |
| SCLK3 | I | SIM card shifters clock input (3 V) |
| SCLK5 | O | SIM card shifters clock output (3 V/5 V) |
| EARN | O | Earphone amplifier output (–) |
| EARP | O | Earphone amplifier output (+) |
| MICBIAS | O | Microphone bias supply |
| MICIN | I | Microphone amplifier input (–) |
| MICIP | I | Microphone amplifier input (+) |
| AUXI | I | Auxiliary speech signal input |
| AUXON | O | Auxiliary speech signal output (–) |
| AUXOP | O | Auxiliary speech signal output (+) |

## 6. 32Mbits FLASH + 4 Mbits SRAM and 16Mbits FLASH



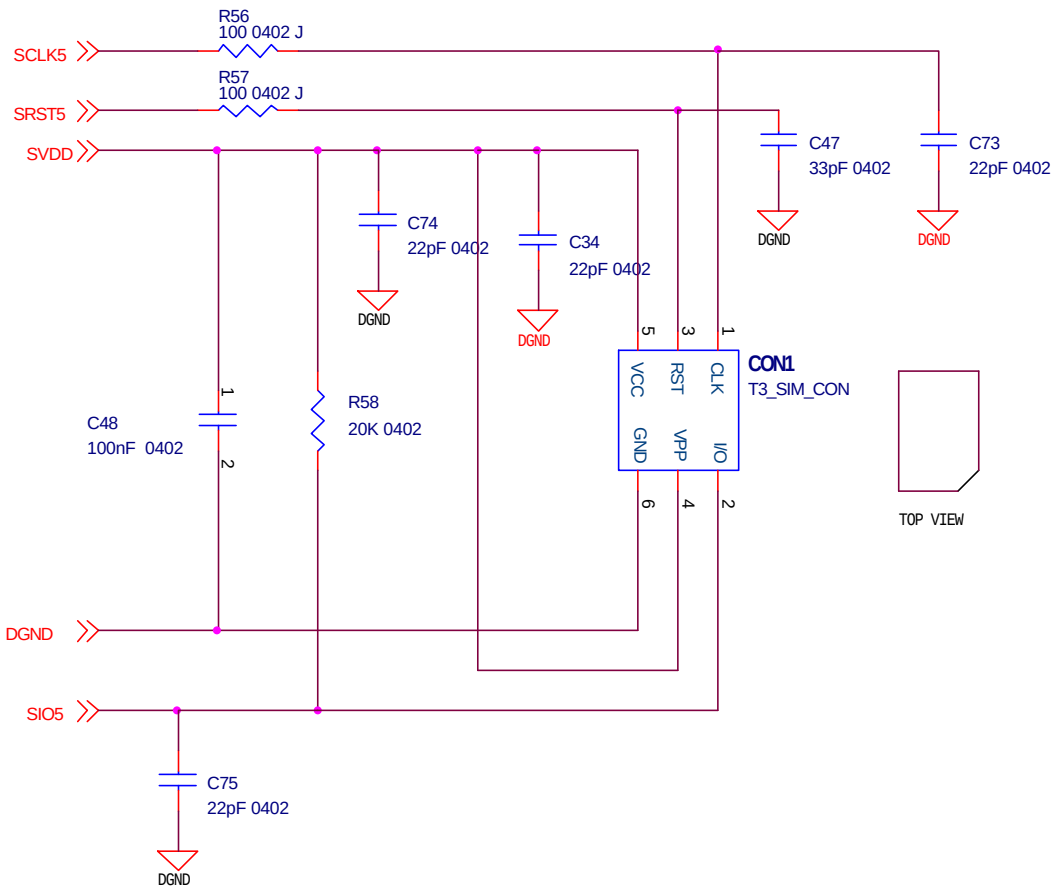

U10 is 32Mbits FLASH add 4Mbits SRAM stacked memory with nCS0 and nCS1 chip select
U7 is a single 16Mbits Flash memory with nCS3 chip select

## 7. Main function: Vibrator driver circuit



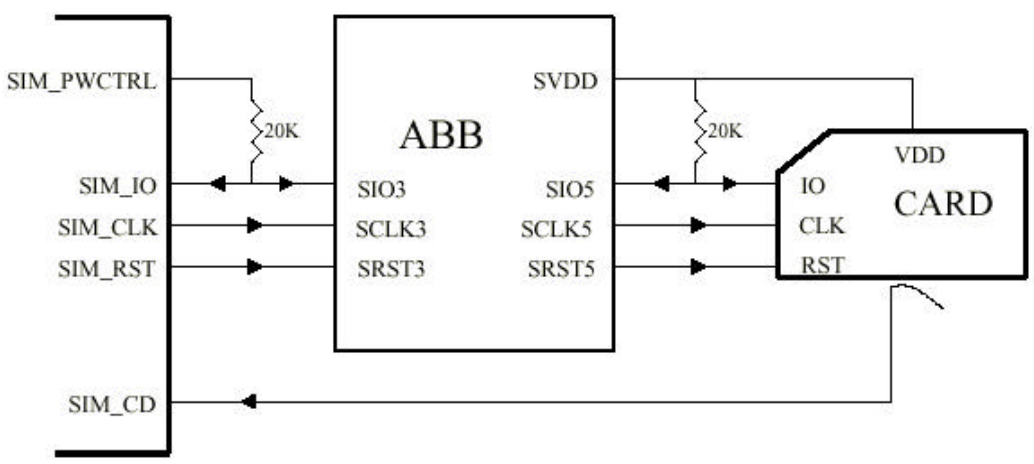

7.1 1.9Vp-p with 0.5Hz cycle input during vibration active
7.2 250mVp-p with 4.6ms cycle input during vibration idle
7.3 Motor starting voltage 1.4 Max
7.4 DAC is 2VDC

## 7. SIM card interface circuit

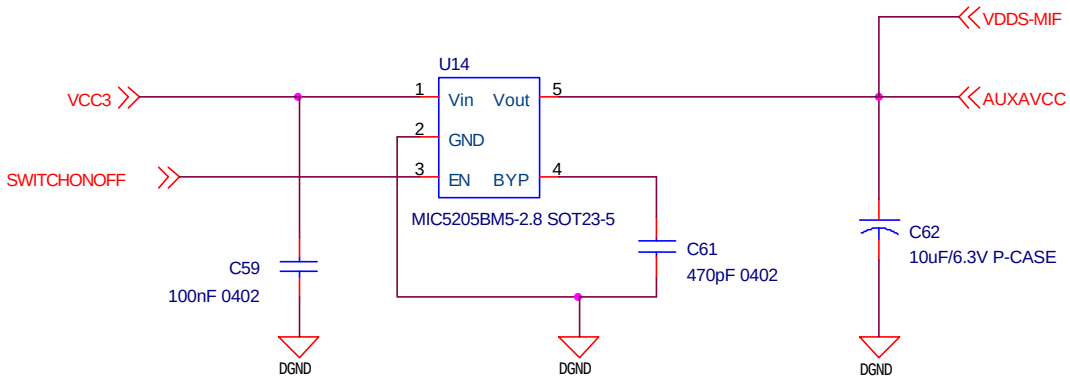



SIMS block includes a charge pump followed by a switchable 3-V or 5-V voltage series regulator that delivers supply voltage SVDD to the SIM module. To accommodate the 3-V or 5-V SIM cards

- SIM_CLK SIM card reference clock
- SIM_RST SIM card async/sync reset
- SIM_IO SIM card bidirectional data line
- SIM_PWCTRL SIM card power activation
- SIM_RnW SIM card data line direction
- SIM_CD SIM card presence detection

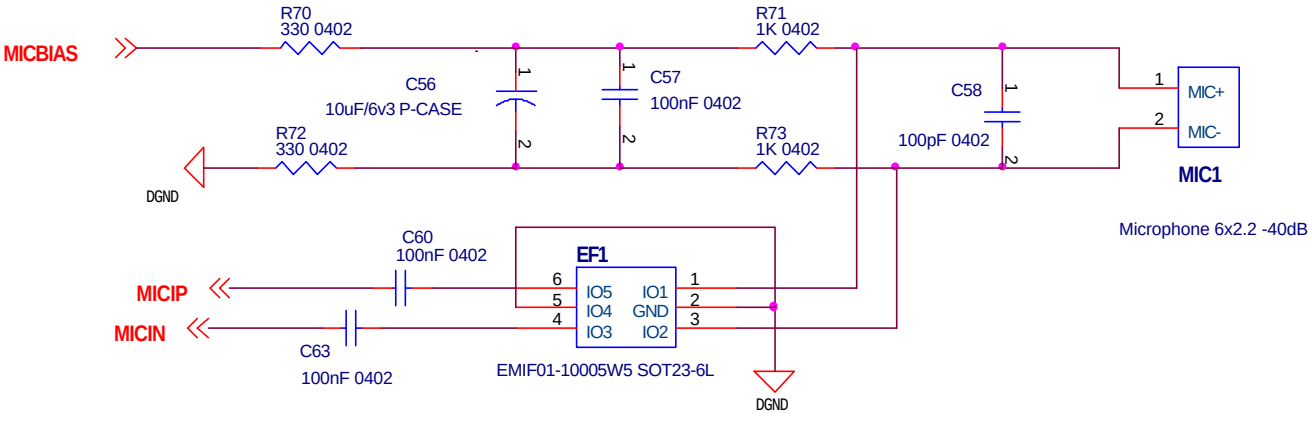



## 9. LDO for memory, LCD power and Earphone control




This LDO can be switched off and switched on by control the switchonoff low and high.
U14 is a 2.8VDC low drop out regulator which support Memory, LCM and Earphone control power.

## 10. Microphone biasing and filter circuit

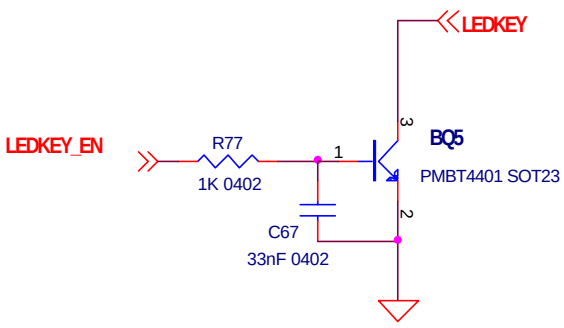



MICBIAS has been set to 2 volts

Nausica DBB chip support MICBIAS during call alert and access the speech communication.

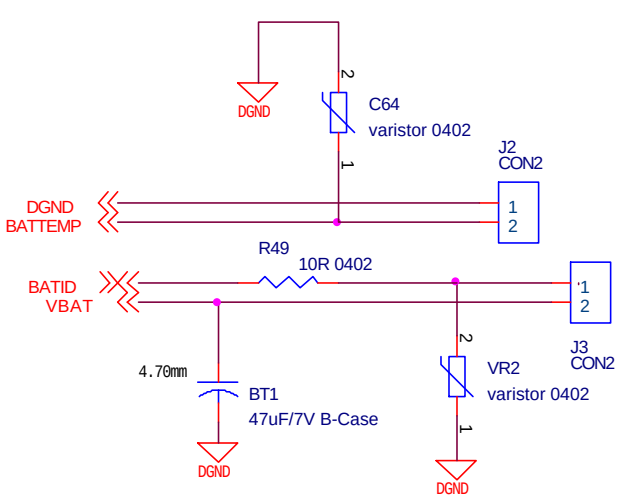
EF1 is an EMI filter to reject noise from microphone

## 11. KEY PAD Backlight driver circuit




LEDKEY become LOW when LEDKEY_EN HIGH

## 12. Battery Connector circuit




VR2 and C60 are used for ESD protect

R49 is used for current limit

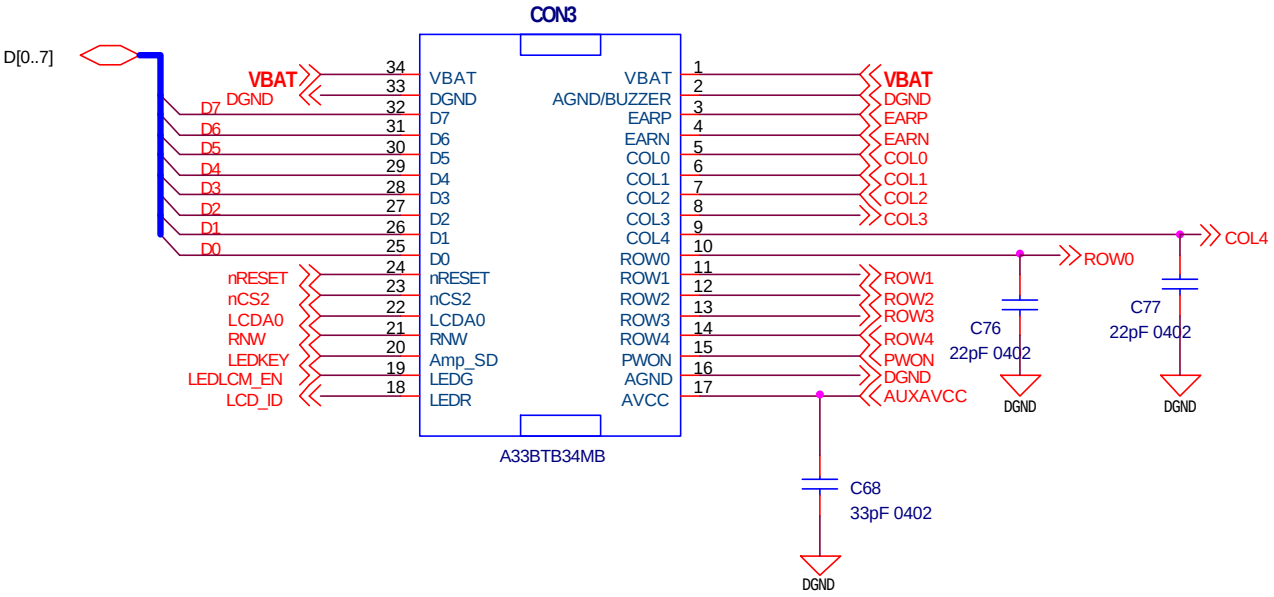
VBAT = main battery voltage ( Li-ion single cell 3.6V typical 600mAhr Min)

BATID is battery identification

BATTEMP is battery temperature detect ion

DGND is system digital ground

## 13. Board to Board connector circuit ( MB side )



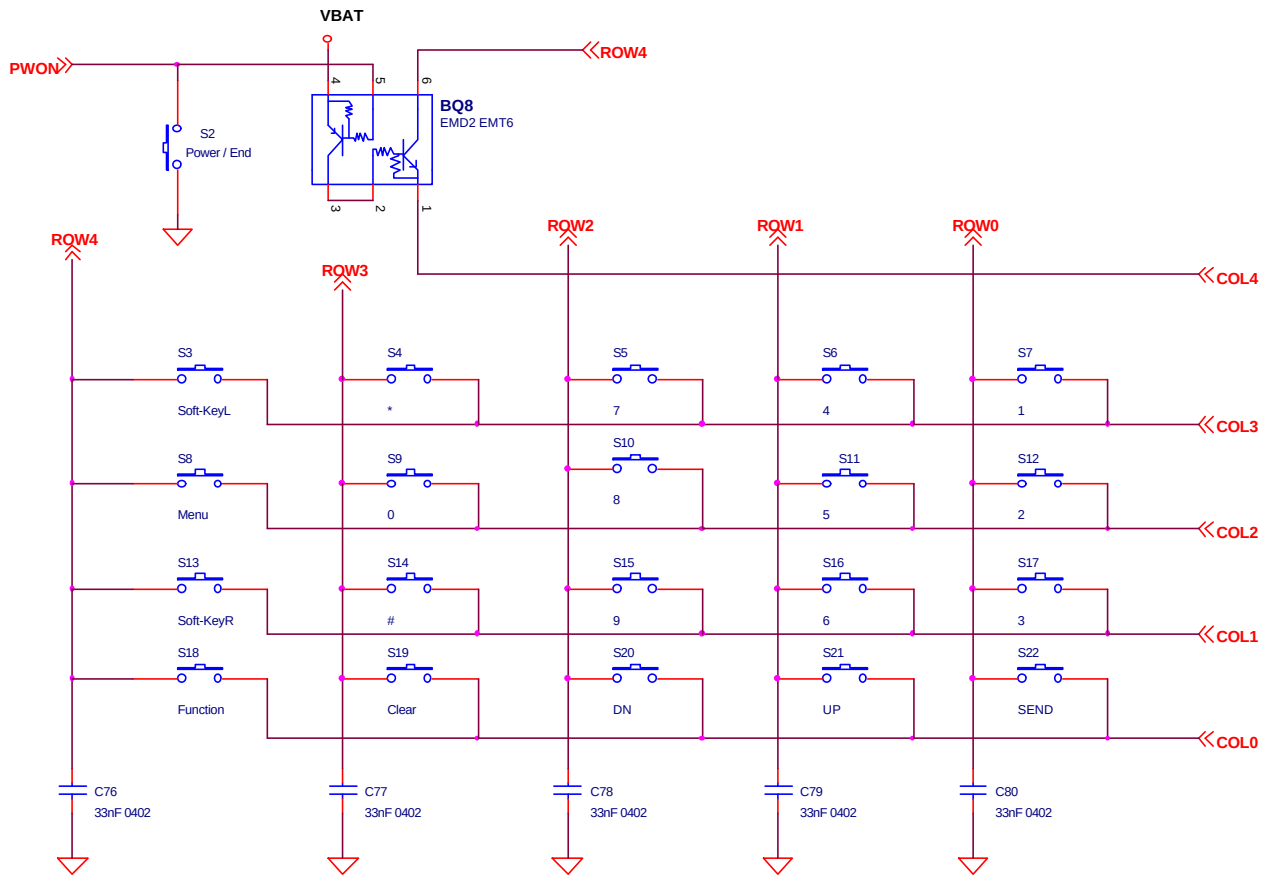

CON3 is mounted on Main Board to link CON4 in MMI Board

C68 used for noise suppression.

C76 and C77 can make earphone send/end key function more stable

## MMI Board

## 14. Key Pad circuit



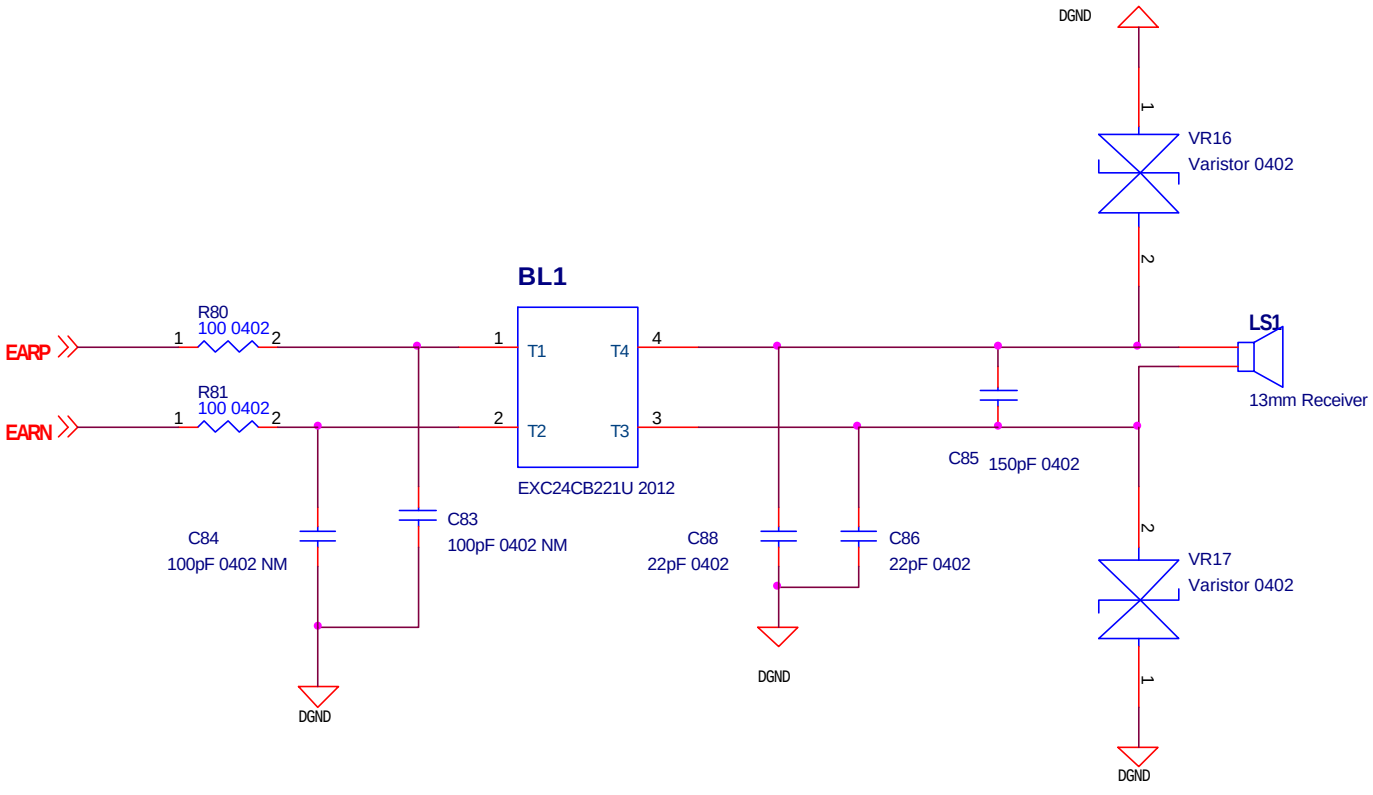


ROW 0 ~ ROW3 = 2.855 VDC

ROW 4 = 2.875 VDC

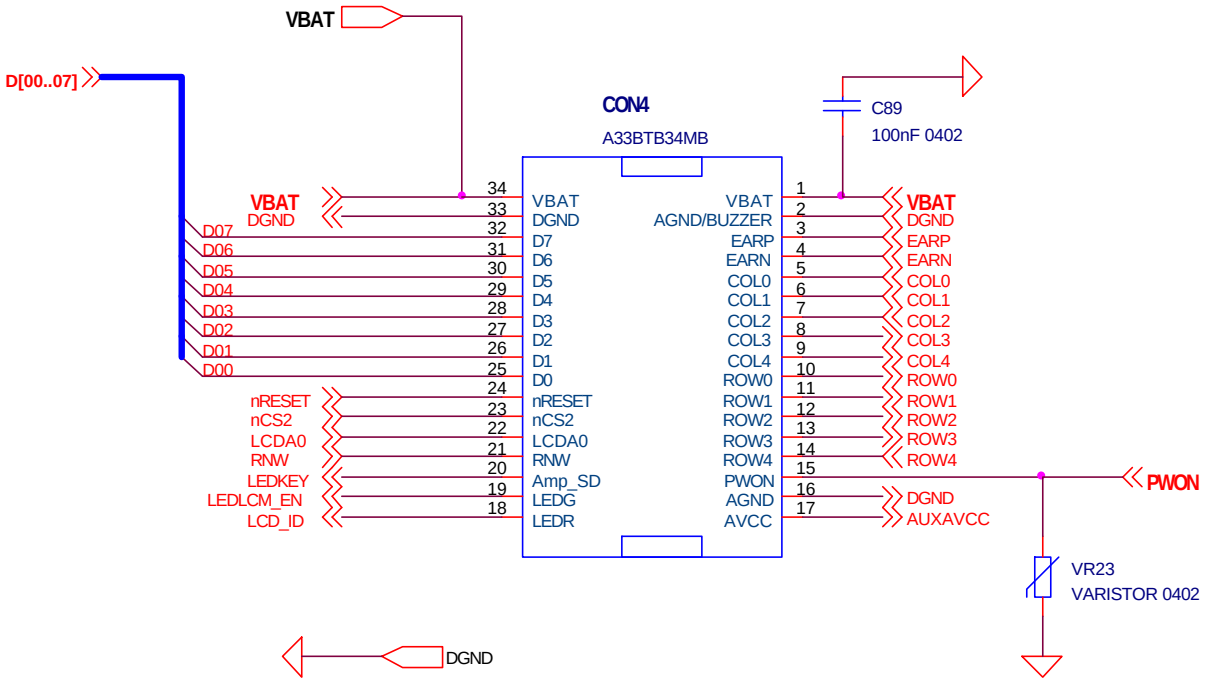
COL 0 ~ COL 4 = 0 VDC

## 15. Receiver filter circuit



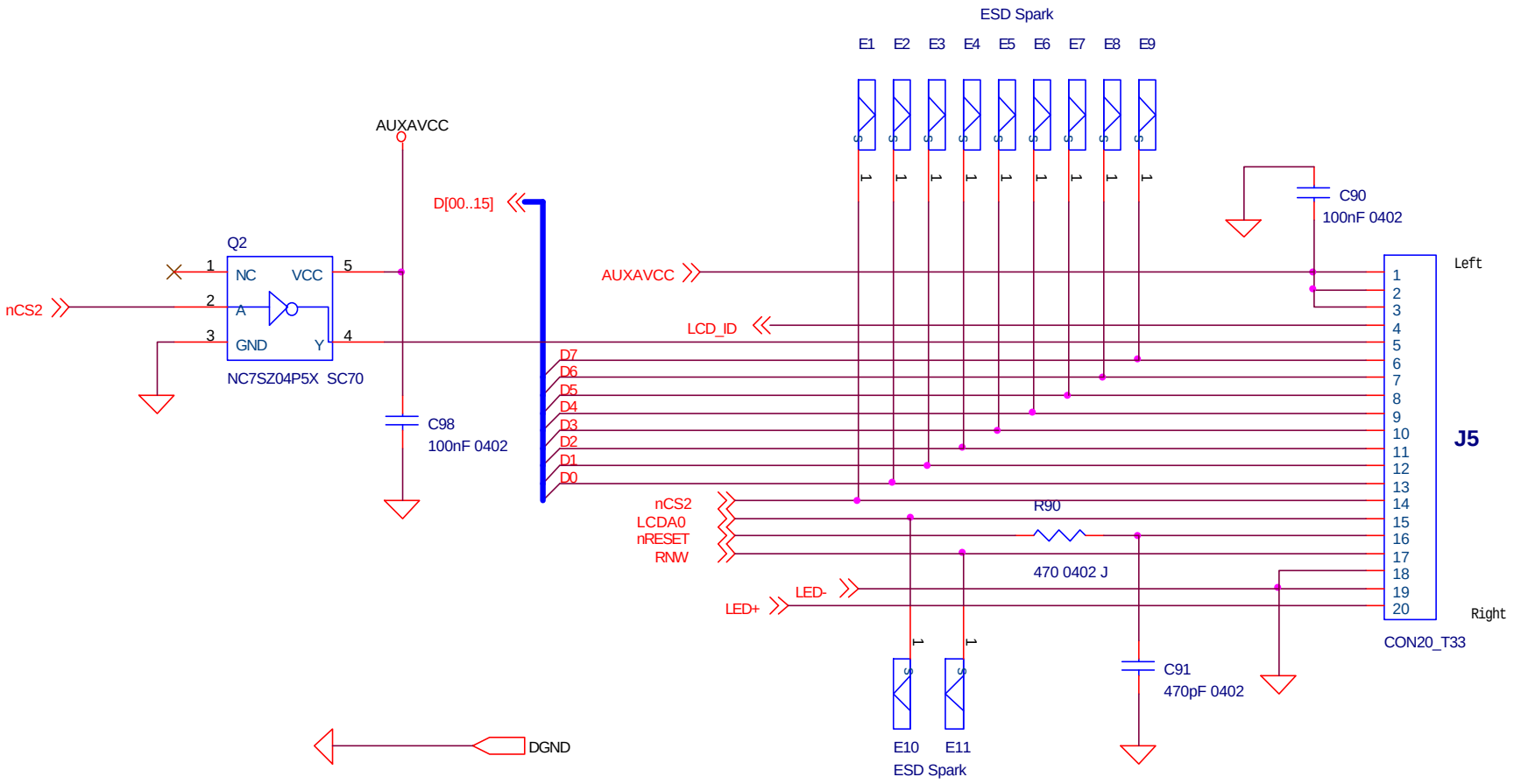

EARP and EARN have 1.2VDC carrier and 2Vp-p AC signal with maximum key tone.
Normal speech have 600mVp-p AC signal maximum.

## 16. Board to Board connector circuit ( MMI side )




VR23 is ESD protect component

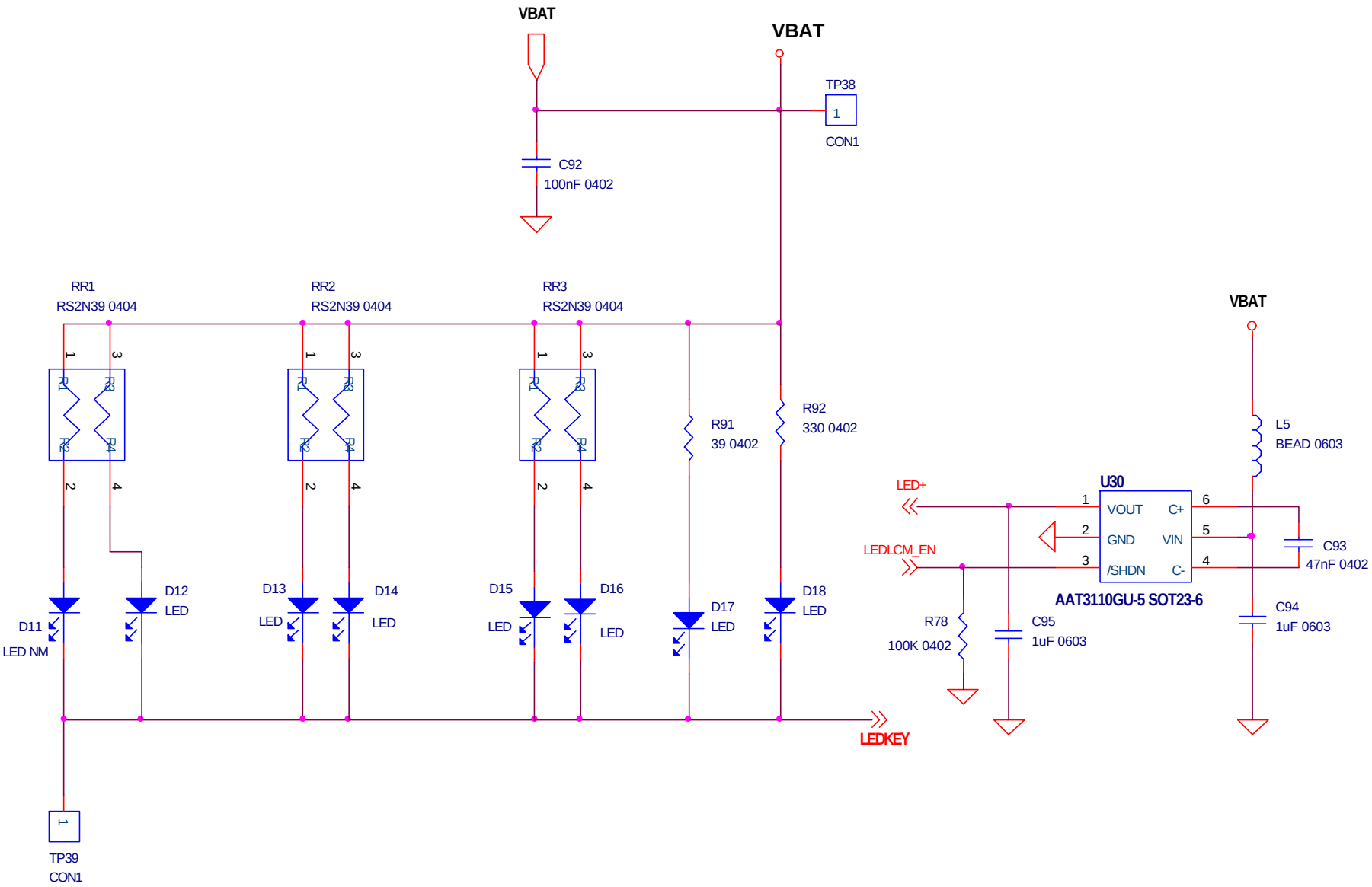
## 17. COLOR LCM connection circuit




**Pin description of Color LCM connector**

| Pin No | Symbol | Description | I/O | Remark |
|---|---|---|---|---|
| 1 | VEE | VEE level pin | - | For LCD driving |
| 2 | VDD | VDD level pin | - | For Logic driving |
| 3 | SEL68 | CPU interface selection port | I | H=68 series,L=80 series |
| 4 | D_ID | ID select pin | O | L: current(HM17C4096N) |
| 5 | RD(E) | Read control input pin | I | "L" active |
| 6 | D7 | Data Bus | I/O | - |
| 7 | D6 | Data Bus | I/O | - |
| 8 | D5 | Data Bus | I/O | - |
| 9 | D4 | Data Bus | I/O | - |
| 10 | D3 | Data Bus | I/O | - |
| 11 | D2 | Data Bus | I/O | - |
| 12 | D1 | Data Bus | I/O | - |
| 13 | D0 | Data Bus | I/O | - |
| 14 | CS | Chip select input pin for main LCD | I | "L" active |
| 15 | RS | Register select pin | I | - |
| 16 | RESB | Reset signal input pin | I | "L" active |
| 17 | WR | Write control input pin | I | "L" active |
| 18 | VSS | Ground level pin | - | - |
| 19 | CA_LED | LED back light (Cathode) | - | 5(typ)V-input |
| 20 | AN_LED | LED back light (Anode) | - | - |

## 18. Key Pad backlight and LCD backlight DC/DC converter circuit




D12 to D18 blue LED are working when LEDKEY LOW
LED+ has 5V regulation voltage output when LEDLCM HIGH
U30 is a DC/DC upper converter with output 5VDC and enable by LEDLCM_EN control high