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ZAP ANALYSIS OVERVIEW

Contents

Section 1

Product Strategy

The demand for a Dual Band phone in a fresh, new design is critical in competing with new product offerings by the competition. The Zap product is a SMoC- based, band aware, and targeted toward mid to high tier business users. It will replace the 8000 series product line, which includes a SmoC - based 8700, SmoC-based 8700 with Voice Annotator, and a band aware version (8900).

Zap will incorporate the latest in feature offerings including HDML, multi-rate speech coder, one-touch voice memo recording, and offer market leading talk and stand-by times. A full line of accessories will be developed to support Zap including DHFA with Voice Recognition, headset with mic, desktop charger, and data cable which eliminates the need for a PCMCIA card. Several different batteries will be available, allowing the user to either minimize weight, or maximize performance.

To fully capitalize on Motorola's leadership in band aware technology, Zap must be introduced no later than Q4 1997. Dancall and Ericsson, among others, have announced their intentions of new product offerings in this category. Aggressive ramp schedules must be met to achieve a Europe-wide launch in December 1997.

Target Markets

The target market for Zap will be mid to high tier business, with emphasis on the focused and balanced business user segments.

Focused Business: These are the heaviest users, and are prone to use the phone for business only. Viewing the phone as an absolute necessity, the focused business user is able to carry out professional responsibilities efficiently and tirelessly. Mainly travelling to dense urban environments, call success rate is extremely important to this segment.

Balanced Business: The balanced business user primarily uses the phone for business related activities, but has also integrated its use into personal life. Characterized by working the longest hours and travelling the most, these users primarily depend on performance.

Section 2

History so far

The Zap radio is a band aware product that was developed for use in areas where both GSM and DCS systems are in existence.

The Zap dates back to December of 1996 when development initially took the GSM 8800 circuitry and modified it to what we currently know as Zap. The Zap is smaller and lighter than GSM 8800 and from a mechanical viewpoint, it is a derivation of the GSM/DCS Modulus product line.

The radio is very easy to assemble and not as sensitive to operator issues as the Clam Rae product.

The first proto run was performed in July 1997 in the Advanced Realization Centre. In August 1997, the first proto run in the European Subscriber Division was realised. At that time, they were using blank Flash IC's which had to go through boot-code before going to tuning. Later builds had the EPROM pre-programmed when placed on the board, so it was not necessary for the boards to go through boot-code.

In Libertyville Tech-ops are currently working on a testbay setup where the unit under test will go through boot-code just prior to being tuned. This is a setup that is currently being employed at Easter Inch with great success.

Flensburg have planned to start production of Zap for early 1998 and are currently doing proto runs of approximately 50 - 100 units. There is poor availability of Sram's and PA's which is limiting the amount of radios built during these proto stages.

Easter Inch are planning to do a proto run sometime between weeks 48 & 52, hopefully week 48 but more realistically week 49, with a plan to start full scale production Feb. 1998.

Section 3

Brief Description

Zap is the latest look in the evolving MOTOROLA MicroTAC Flip phones. It is being developed for GSM/ DCS systems worldwide.

The RF portion of Zap is capable of being modified for operation on EGSM frequencies.

A single phone will work on GSM 900 and DCS 1800 Bands. It provides the service provider the ability to better manage congestion by transferring traffic over to the other less congested system. The user has the advantage of being able to roam into either one of the systems that is available.

The transceiver board and keypad/display board are mated by a 32 pin connector. The transceiver board being made up of 6 layers.

The phone utilises a real time clock, internal fast charger, a 32 x 96 graphics display, Personality software, smart button, voice annotator and also accommodates a small SIM card.

The Zap will also support the RAE universal transformer and CLA. The RAE desktop charger will be modified to fit the ZAP form factor.

Marketing has requested new accessories which include a boom headset, data cable, smart card reader, and three new car kits.

The ZAP will utilise the butt plug and one battery as power source options. Support for alkaline AA batteries is also being investigated.

The Zap also incorporates the SMoC IC which is a composition of Speech Coder, Modem and Codec. This component is found on various other products for example 8700 and Modulus.

The Zap also uses 3 BGA's (Ball Grid Array):-

- 68338 uP (BGA)
- Flash EPROM (uBGA)
- SRAM (uBGA)

The transceiver board is almost entirely covered with cans similar to Modulus but are solid with a few holes placed to aid can removal.

The receiver and transmitter are very similar to bandaware but the switching network is simpler and more integrated.

The Zap will be the first MOTOROLA digital phone to utilize a voice annotator.

Section 4

Preliminary Design/Dimensions

Physical Characteristics:

Transceiver weight = 98g
Volume (with slim battery door) = 135cc
Lightest/smallest config. (LP4 battery) = 120g
Length = 130mm
Width = 55.25mm
Depth = 26.95mm

Electrical Design:

Zap utilizes a 2.7V platform, Rae style connector, 3.6V battery support, and the latest components to minimize both Tx and Rx current drain. A BIC 4.2 is required to support recognition of a small SIM and smart card. NiMH, LiIon and alkaline technologies will be supported.

Front Housing:

The front housing design includes an earpiece, and allows the use of a lens and 18-key keypad. Three side buttons are utilized on the left side, functioning as up and down scroll, and smart key (similar to StarTAC). One right side button will serve as the dedicated voice memo record button. A microphone port is located bottom centre left, with two other styling ports for symmetry. A protective ridge is used around the power key to avoid inadvertent operation.

Rear Housing:

The rear housing is cut away at the bottom to utilize a battery door concept. An escutcheon at the top of the rear housing makes visible the Motorola brand name while the phone is in use and covers two assembly screws. A call alert port is positioned below the escutcheon and to the right.

Battery door:

Zap uses a battery door concept. Three doors will exist; a slim door which will house the LP4, AAA Longs and LSQ8 batteries, a slightly larger door will cover the AA batteries and a door large enough to cover two LP13 batteries. The doors will be completely removable, and will mount to the rear housing by placing the heel of the door into a guide and rotating down until it snaps to the back housing. The doors will be the same colour and texture of the front and rear housing.

Display/Indicators:

The display consists of a 96 x 32 pixel LCD module, with full graphics support and icons. Utilizing the same pixel density of StarTAC and 8700, the display size is slightly smaller, measuring 34mm by 23mm. The display icons are arranged in two rows, located at the top of the display.

Top row: signal strength indicator, real time clock, battery charge indicator

Bottom row: off-hook, roam, home, voicemail message, SMS, ringer-on

The top row will be continuously on, while the illumination of the bottom row icons will depend on the specific operating conditions. New with Zap, the ringer on icon will be illuminated when the ring alert has been selected. The icon will not be visible when either vibracall or silent alert has been activated.

Lens:

The lens is curved to follow the contour of the front housing. Motorola branding is positioned at the top of the lens. The lens has a glossy finish, and has the same colour as the housing.

Flip:

For the flip version of Zap, the flip is designed to fully cover the keypad. The top edge of the flip will coincide with the lens. A cam mechanism is utilized. Clicking must not be audible when operating the flip, and the design must give a sturdy, unbreakable perception. The flip has an escutcheon pocket positioned at the top.

Keypad:

The keypad consists of 18 keys. A domed plastic key is used to enhance tactile feel. The keypad layout is as follows:-

Quick Access	MENU	C	OK
1	2 ABC		3 DEF
4 GHI	5 JKL		6 MNO
7 PQRS	8 TUV		9 WXYZ
*	0 +		#
Power Icon			M+

The key colours are as follows; Background (except power key)- black. Digits, Alpha, MENU, M+ - white. C - red. OK - green. Power - white background with black icon

External Keys:

Three side keys are used on the left side of the phone. The top and bottom keys scroll through menus and phone book entries, while the middle key functions as a smart key (similar to StarTAC). The middle key is oval and domed with moulded diamond icon. The scroll keys are domed, half oval with moulded up and down indicators.
One key is present on the right side, just under the antenna, for dedicated voice memo recording. The key is "flush to below" the housing to prevent inadvertent operation.
All external keys are made of soft silicon rubber and are process black.

Earpiece:

The earpiece is a recessed oval with the middle detail slightly raised with a slot pattern to accommodate the dynamic speaker. The actual slot design allows sufficient air movement to maximize audio clarity. This slotting was determined by engineering to achieve best results.

SIM Card:

Zap uses a small SIM design. It is positioned in the back housing, under the battery. A sliding, flip up door configuration is used to allow for easy insertion/removal.

Batteries:

Shrink wrapped, 3.6V batteries are used for Zap. In addition to cost effectiveness, this design allows minimal product thickness. Lithium Ion, Nickel Metal Hydride and Alkaline batteries are supported. Because of the huge variation in performance when using alkaline batteries, these batteries are promoted as "emergency use only". Average talk and stand-by times should not be associated with alkaline batteries. Five battery configurations will be available:

1. LP4 (Li Ion, 500 mah) $56
2. AAA Long (NiMH, 700 mah) $9
3. LSQ8 (Li Ion, 900 mah) $21
4. AA (NiMH, 1500 mah) $13
5. Double LP13 (Li Ion, 2600 mah) $100
6. AA Alkaline (emergency use only)

LED Indicator:

A status LED indicator is positioned at the top left of the phone, towards the front. This indicator has similar functions as the one used on StarTAC: green will flash when phone is on and in service, red when the phone is on and out of service, and orange when the user is in roam.

Antenna:

The antenna must support both 900 and 1800Mhz frequencies. Both the stub and pull out style antennas were evaluated with regards to signal performance and the tendency is leaning towards using the stub antenna.

Voice Annotator:

Zap supports the voice annotator feature, allowing at least 3 minutes of multiple messages with store and erase capability. To maintain consistency with the 8700 memo product, hands free operation must be available when using the voice annotator with a car kit.

Key/Unique Features

Automatic Band Switching:

As the majority of the market will be moving towards dual band capability, Zap will be positioned as a high performance, band aware offering in a new, ergonomic design.

HDML support:

To carry internet access into the cell phone arena, **Unwired Planet** has agreed to support our efforts in integrating this feature into Zap.

Performance:

Targeted toward the mid to high tier business user, performance is critical. Zap will take a leadership position with the Extra Performance package, offering stand-by time of over 2 weeks.

Smart Card support:

eCash and paperless ticketing are two examples of smart card applications. Through a smart card accessory, Zap will offer smart card support, allowing the user access to the variety of other potential applications.

Multi Rate speech coder:

Now becoming a competitive necessity, Zap will offer excellent audio quality through this feature.

SIM Tool Kit:

A competitive necessity, this will allow operators to customize their software load according to their needs.

Form Factor:

In several user surveys focusing on design, the Zap form factor has repeatedly ranked among the highest. Test subjects indicated the phone was very comfortable to hold, looked expensive, and appeared like it was easy to use.

Data Compatibility:

With the data cable accessory, Zap will support:

1. Data: 9600 baud, transparent and non-transparent, AT and V.25 bis command operation. V.42 bis compression/decompression is supported.
2. Fax: 9600 baud, transparent and non-transparent, EIA/TIA class 1, 2, and 2.0 AT command operation.

Software and MMI description:

Zap uses the personality II interface, however scrolling through menus is accomplished by using the up and down side buttons. As with current products, User Configurable Quick Access is supported. The Smart button functions identical to StarTAC 110. The dedicated voice annotator key functions the same as it did on 8700 memo product (multiple messages totalling 3 minutes), including instant recording by pressing the dedicated button.

Section 5

CONTENTS

Rx Path Brief Description

* As the Zap product is bandaware there are two RF paths to follow GSM and DCS the following deals primarily with GSM and has the equivalent DCS parts in **Bold** type.

* The RF Signal enters the Radio via the antenna, then passes through the RF switch, depending on the switching signals present at the switch network of U401and U403.

* From the RF switch the signal then passes through FL400/**FL401** which are bandpass filters where it is cleaned up before being passed onto C413/**C433** (de-coupling capacitors).

* The signal is then passed onto the base of Q410/**Q430** (low noise amplifiers), where it gains small amplification.

* The output of the LNA now passes through FL461/**FL462** which are combination bandpass filters with approximate losses of 3dbm across the filters.

* The MAIN VCO signal also enters the filters(FL461/**FL462**) at this point and both signals are passed onto the Mixer Stage (Q460). The output of the mixer consists of 3 main components F1 x F2, F1 + F2, F1 - F2. You will also find various harmonics at this point.

  F1 = Rx signal
  F2 = Main VCO signal

* To remove the unwanted signals at the output of the mixer these signals are fed through a SAW filter (Surface Acoustic Wave) FL480 which only passes the difference of these two signals 215Mhz.

* The signal then passes onto the Isolation Amplifier (Q480), which provides a little gain and also prevents feedback/noise from the GIF_SYN I.C. U220.

* The now “cleaned” I.F. signal now enters U220 via pin 31 (pre_in) where it is mixed internal to U220 with a pure 215Mhz signal. The internal 215Mhz signal is derived from the 430Mhz L.O. which is divided by two internally, this again gives us the difference.

* From the mixing of the two 215Mhz signals, of which one has modulated data (derived from the external RF Signal), we derive two signals the RxI and the RxQ which contain the Digital information.

* This is further demodulated in the SMoC I.C. (U500) and provides serial data, which is then D/A converted, amplified by the G-Cap and presented to the speaker.

RF SWITCH

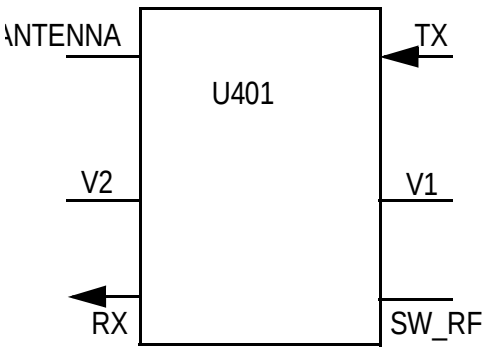
Circuit Description:

The RF switch has two basic functions. Firstly it prevents RF entering the Rx path when the unit is transmit mode. Secondly it switches the path for the RF signal from the antenna(A1) to the SW_RF connector (J600 pin2).

U403 is the logic switch that controls the state of U401 (RF switch).

When the radio is in a transmit state Tx_EN is high and Rx_EN is low therefore V1 is going to be high (+3V), V2 will therefore be low (-7V). The state of these two control signals will determine the path taken, in this case, RF will only pass through the antenna and not enter the receive path.
In receive mode the reverse will be true, and RF will be directed to the Rx path.

In the second case the circuit must be able to establish whether the antenna or the SW_RF connector is connected. This is done by sensing the impedance to ground(>10K) of the auxiliary RF connector. Switch U403 also detects the 50ohm resistance of the RF cable used when the SW_RF is connected, thus allowing antenna or AUX RF connection.



SW_RF	TX_EN	RX_EN	V2	V1	ANT	AUX
YES	LOW	HIGH	+3V	-7V		RX
YES	HIGH	LOW	-7V	+3V		TX
NO	LOW	HIGH	-7V	+3V	RX	
NO	HIGH	LOW	+3V	-7V	TX	

ZAP T/R SWITCH COMBINATIONS

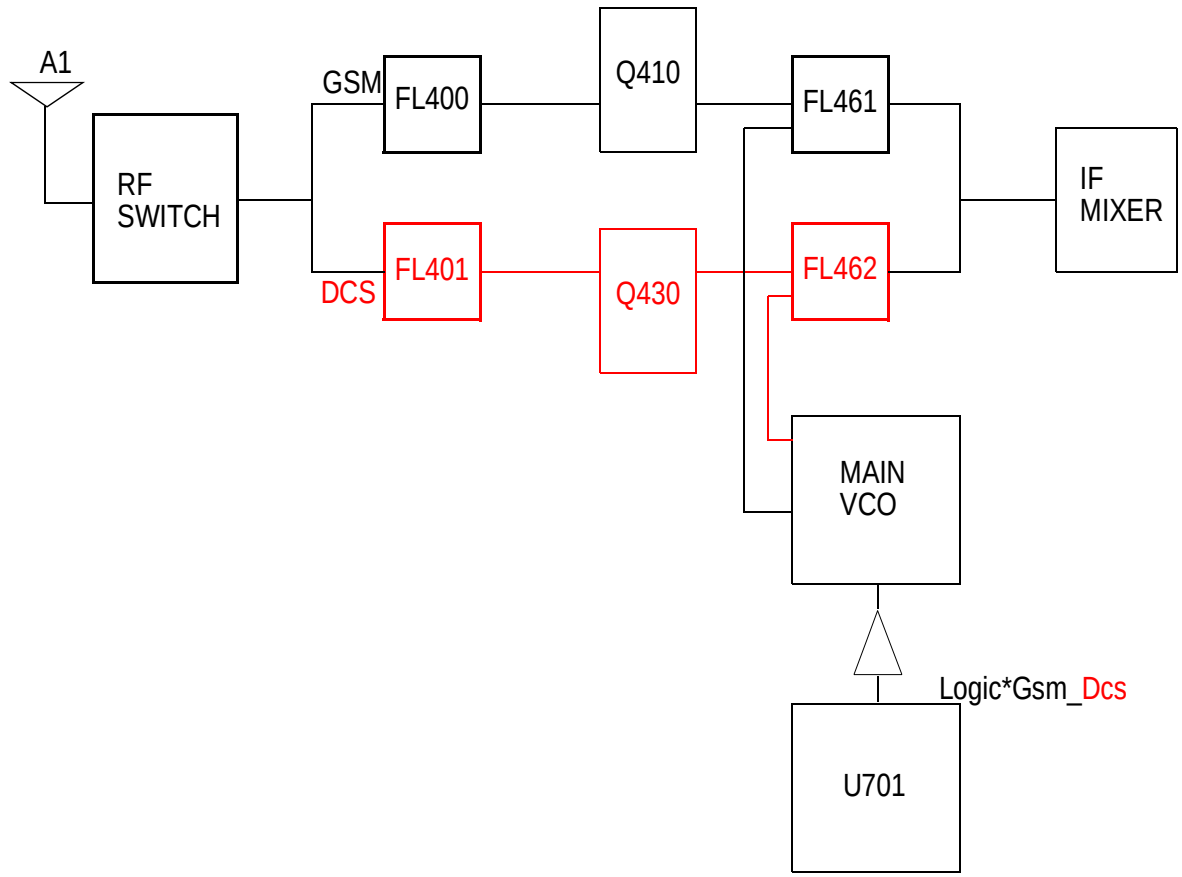
FROM RF SWITCH TO RECEIVER FRONT END

Circuit Description:

The RF signal enters the antenna(A1) and when the Rx_EN is high the signal passes through the RF switch to FL400/**FL401**, these are bandpass filters with pass bands of 935-960Mhz (BW=25Mhz) for GSM and **1805-1880Mhz for DCS (BW=75Mhz)** respectively both having approximately 3db loss.

The signal passes onto Q410/**Q430** which are low noise amplifiers with a typical gain of 13/**9.5**dBm. L410/**L430** are RF chokes to prevent AC getting to the DC bias voltage Rx275. Capacitors C413/**C433** and C412/**C432** are coupling capacitors and there purpose is to prevent DC bias voltage from Q410/ **Q430** from reaching the other stages. Q410/**Q430** are enabled from Rx_EN via U701 pin A9 and LOGIC_GSM_*DCS from U701 pin B5 via Q412, which controls Q411/**Q431** hence de-activating either Q410 or **Q430**.

The signal then goes to a second filter FL461/**FL462** and then onto the mixer stage. In addition to the receive signal entering FL461/**FL462** the MAIN VCO signals for the particular band (GSM or **DCS**) enters at these Combination Filters.



RF SWITCH TO RECEIVER FRONT END BLOCK DIAGRAM

MAIN VCO/RX VCO

Circuit Description:

The main VCO is a 3V Dual Band design based on Knifeswitch which consists of a colpitts oscillator(Q202), which operates from 720 to 745Mhz/**795 to 832.5Mhz** and is controlled by the GIF_SYN I.C. (U220, pin23). The output of the ocsillator is supplied via a common base buffer(Q201) followed by separate 2nd stage common emitter buffers for GSM and DCS (Q206/**Q200**), and resistive splitters to drive the receiver front end, GIF_SYN prescaler and the TIC I.C. **The second buffer stage in DCS mode is used as a doubler (output frequency = 1590 - 1665Mhz)**. From there the signal goes through FL461/**FL462** to achieve the correct levels at the input to the mixer.

The tuning voltage representing the channel is output on MAIN_CP (U220 pin23) to the varactor diode CR202; **note that CR203 and associated components R215,R236 and C214 are in circuit for DCS mode when the correct condition is met via the *GSM_DCS line from Q100 & Q105.** The change in capacitance will control the frequency of oscillation. The higher the voltage the lower the capacitance and the higher the oscillating frequency.

The main VCO is adjusted by the RF_SPI and RF_SCK lines from the Call Processor to the SMoC I.C. and from the SMoC I.C. to the GIF_SYN and thereafter the MAIN CP is changed accordingly.

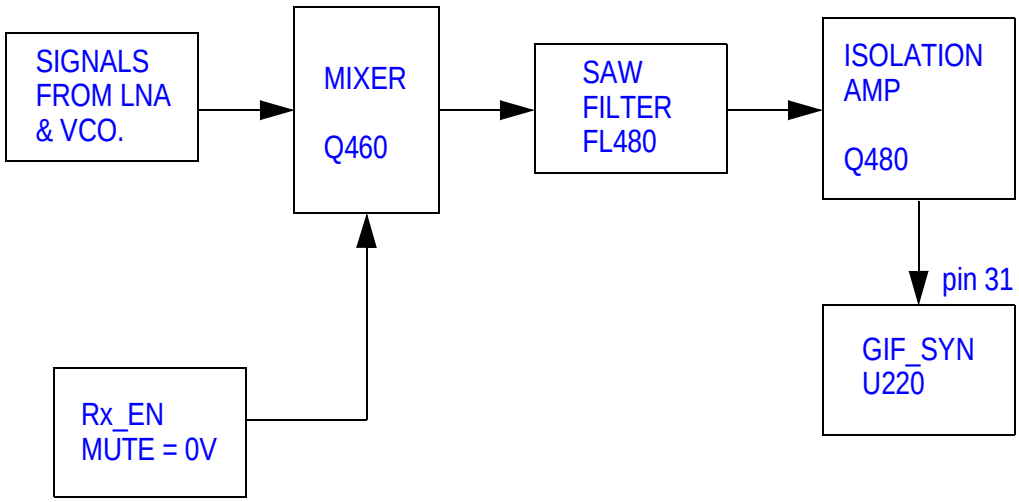
The supply for the main VCO is derived from pin 21 of U220 which is the SF_OUT. This supply is the super filtered supply to eliminate any noise generated. It is a 2.55V dc level.

OUTPUT OF LNA TO GIF_SYN (U220)

Circuit Description:

The RF signal and the main VCO signal pass through the combination bandpass filters FL461/**FL462** (2.5dB loss) and are mixed in transistor Q460 (10dB gain). The output of the mixer will contain the original signals, their sum, difference, product and harmonics. The strongest signal will be the difference (215Mhz). The signal is then passed through FL480, which is a **S**urface **A**coustic **W**ave (**SAW**) filter that passes only the 215Mhz signal with a bandwidth of 180Khz.

The signal then goes to the Isolation Amplifier (Q480), the bias of which is provided by SW_VCC and that is supplied by U220 pin 33. The IF signal from the Isolation Amplifier(10dB gain) then goes to pin 31 (PRE_IN) of U220. The purpose of the Isolation Amplifier is to isolate U220 from the receive path. It is used to decrease the reverse feedback of the 215Mhz local oscillator and step up the impedance to the IC. The use of this amplifier improves the noise figure performance, while providing an opportunity to compensate for gain variations in the rest of the receive path over temperature (AGC).



BLOCK DIAGRAM OF LNA TO GIF SYN.

Muting the receiver:

The Rx_EN is used to mute the receiver when Rx_EN is low. When it is high, the base of the mixer Q460 goes high and the amplifier is turned on. When it is low the base of the transistor goes low, and the amplifier is turned off, thus muting the receiver front end.

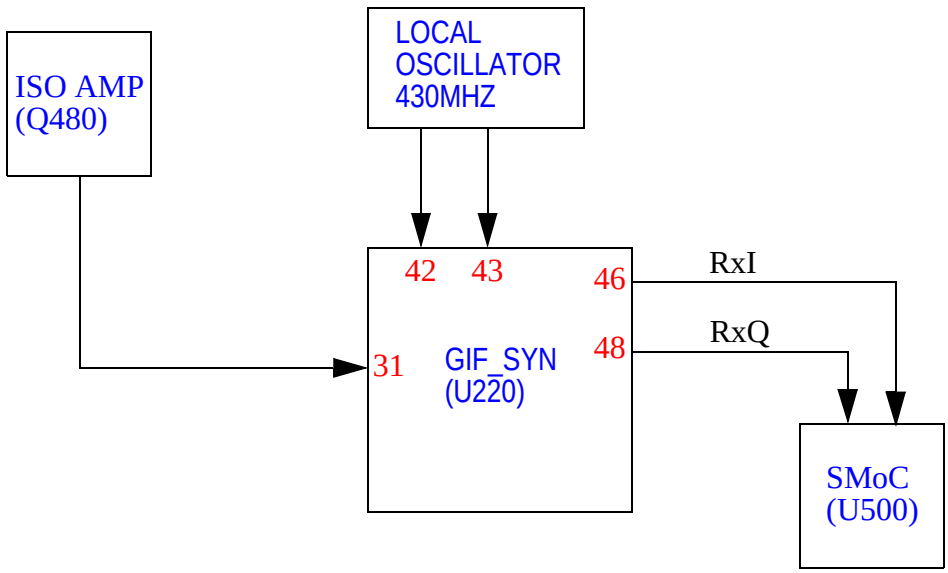
FROM MIXER TO GIF SYN(U220)

Circuit Description:

The 215Mhz IF goes into pin 31 of U220. In the GIF_SYN(U220) the signal passes a 25dB step attenuator (internal to U220) on its way to the Quadrature Demodulator. The step attenuator is designed to improve the range of the receiver, by keeping the RF signal in the range of the amplifier.
i.e. When the signal is too strong the step attenuator will kick in and drop the signal by 25dB.

Inside the GIF_SYN the IF is mixed with the 430Mhz from the external tank circuit, (which is divided by two internal to U220), and demodulated to give two signals RxI and RxQ on pins 46 and 48 of U220. RxI and RxQ are Quadrature baseband analogue signals at 1vp-p on a 1.65v DC level. These two signals then go to the SMoC I.C. where they are further demodulated.

The signals RxI and RxQ then go to pins 23 and 22 respectively of the SMoC I.C.(U500). In the SMoC I.C. the I & Q signals are A/D converted and the digital data is transmitted serially to the Call Processor (U701) pin E1 (MISO). The SMoC I.C. also decodes and decompresses the signal before D/A conversion.



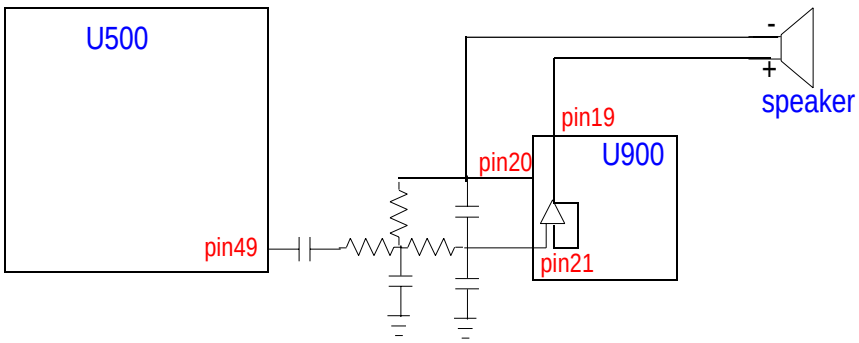
BLOCK DIAGRAM OF ISOLATION AMP TO SMoC.

AUDIO PATH FROM SMoC TO SPEAKER

Circuit Description:

After being decoded from digital to analogue, the audio signal exits the SMoC (U500) at pin 49 (SPKR). Now named Rx_AUDIO, the signal travels via C825 and R810,R801 to the GCAP (U900) pin 21(SPKR IN). The signal is amplified internally by U900 and then output on U900 pins 19 and 20 (SPKR+ and SPKR -). The speaker is driven differentially and is connected via R852 (+) and R853 (-).

The audio tones which are heard when a key is pressed, are generated as digital signals within the U500 before being converted to analogue. The signal then follows the path described above.



BLOCK DIAGRAM OF AUDIO PATH FROM SMoC TO SPEAKER.

The internal amplifier of U900 is controlled by the Call Processor via the control ports at pins 57 & 60 of U500(AUD_EN2 & AUD_EN1) which go to U900 pins 44 & 45 respectively. To activate the internal mic and speaker amplifiers U701 drives AUD_EN1 low and AUD_EN2 high.

Section 6

CONTENTS

Tx Path Brief Description

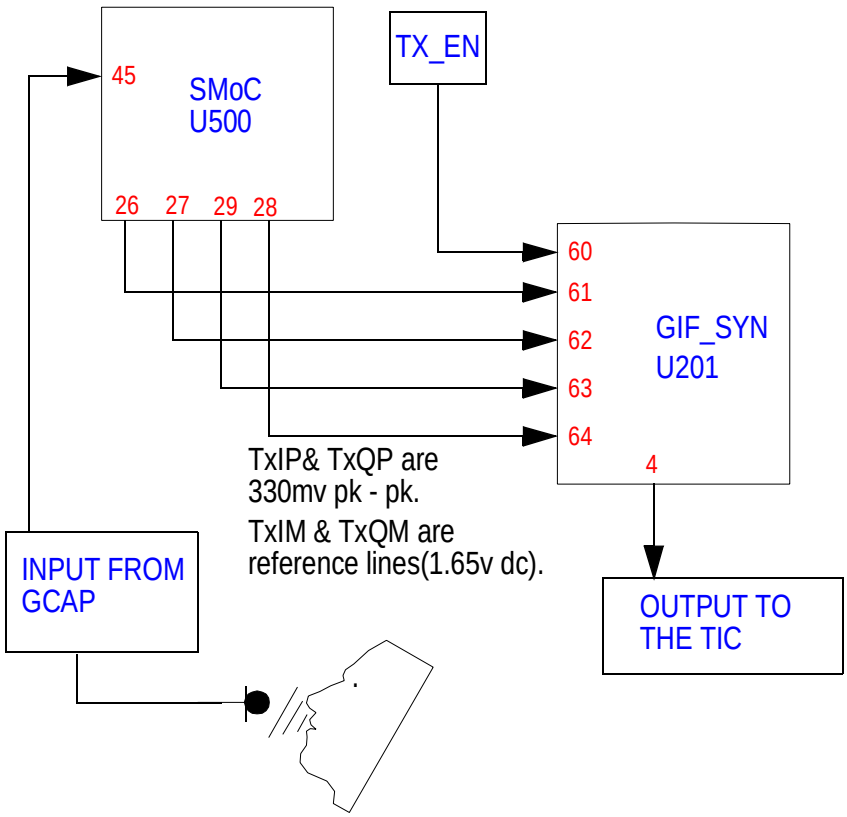
* Audio from the microphone (analogue signal) is amplified by U900.
* The signal is then A/D converted by the SMoC I.C.
* The SMoC also adds error correction bits and encodes the signal, the data is then GMSK digitally modulated and then D/A converted.
* See notes for GMSK modulation:
* The modulated analogue signal is then sent to the GIF_SYN I.C. as inphase (I) and Quadrature (Q) components. These ride on a DC level.
* The Q signal lags the I signal by 90 degrees.
* These are then modulated onto a 170/**120**Mhz signal.
* The 170/**120**Mhz signal then enters the TIC I.C.(U370) along with the main VCO. The TIC I.C.utilizes a phase lock loop configuration to modulate the TX_VCO (GSM/**DCS** = Q351/ **Q350**).
* The now modulated TX_VCO is then preamplified by the exciter.
* The gain of the exciter is controlled by the PAC I.C. (U340).
* This is then fed to a fixed gain Dual Pack PA amplifier and then output via an RF switch to the antenna.

FROM MIC TO SMoC I.C.

Circuit Description:

Audio from the microphone enters the GCAP (U900) at pins 8 & 9(mic in +-) where it is amplified and then output on pin 10 (micout). This signal then goes to the SMoC I.C. U500 (pin 45).

Inside the SMoC this signal is then A/D converted, error detection bits added and compressed.The resulting data stream is then GMSK digitally modulated, D/A converted and then filtered.This modulated analogue signal is then sent to the GIF_SYN U201 as inphase (I) and quadradine (Q), which are commonly called TxIP and TxQP on pins 63 & 61 respectively.These signals are roughly 330mV pk-pk riding on a 1.65v DC level (I-Qref).



BLOCK DIAGRAM OF MIC TO GIF_SYN.

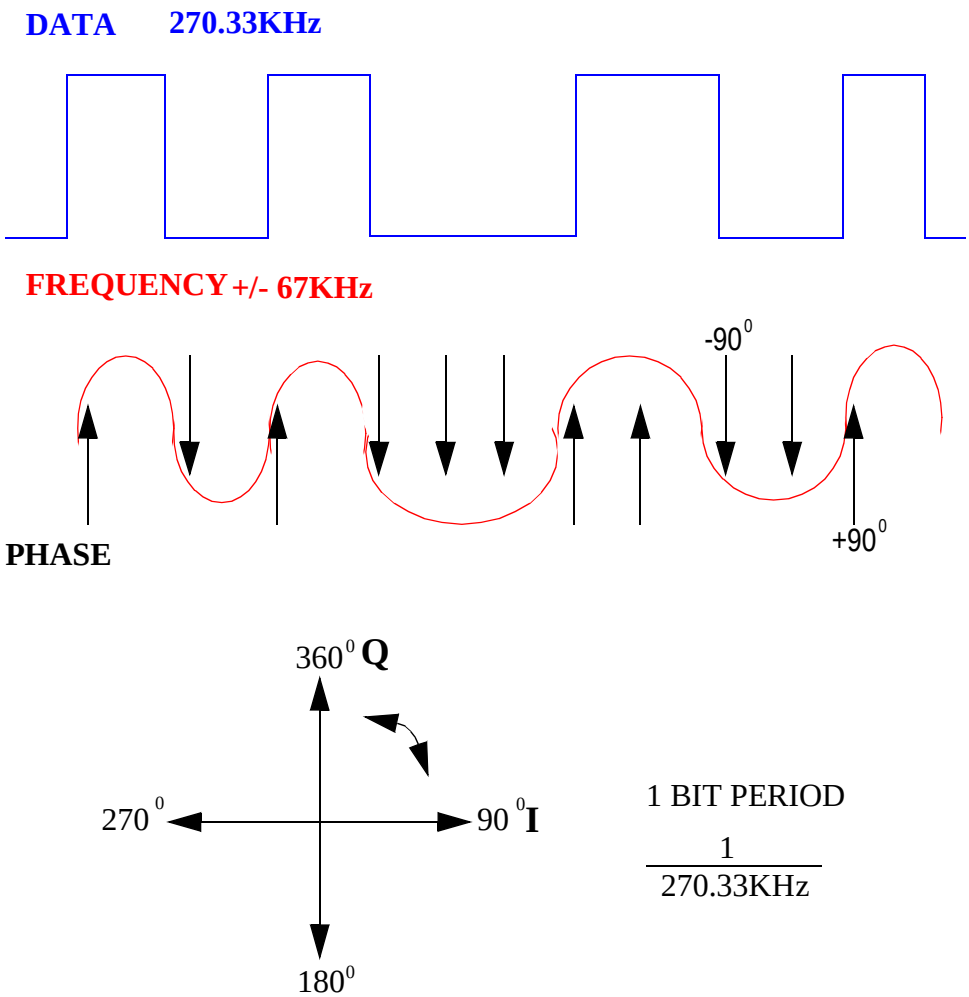
GMSK- Gaussian Minimum Shift Keying

GMSK is a digital modulation technique where 1's and 0's are represented by shifting the RF carrier by plus or minus 67.708Khz. The data rate of GSM is 270.833 Kbits/second which is exactly four times the RF frequency shift.

GMSK is not phase modulation. Information is not conveyed in absolute phase states, but by the change in phase states.

1's are seen as a phase increase of 90 degrees
0's are seen as a phase decrease of 90 degrees

If a constant stream of 1's are being transmitted, MSK will stay 67.708Khz above the carrier centre frequency. If the carrier centre frequency is taken as a stationary phase reference, the 67.708Khz signal will cause a steady increase of phase. In one bit period, the phase will go a quarter of the way round the IQ diagram, or 90 degrees. Two 1's cause a phase increase of 180 degrees, three 1's - 270 degrees, and so on. 0's cause the same phase shift but in the opposite direction. See diagram below;



GIF SYN TO TRANSLATIONAL IC (TIC)

Circuit Description:

Inside the GIF_SYN, the baseband TxIQ inputs from the SMoC pass through an IQ low pass Filter.The inputs labelled TxI_P, TxI_M, TxQ_P, TxQ_M in the GIF are differential in-phase and quadrature inputs. Q is defined as lagging I by 90^0. These inputs may be driven either single-ended or double-ended. In the single ended configuration TxI and TxQ are inputs while TxIX and TxQX are tied to VREF(A/D). The baseband single-ended inputs to the IQ Modulator are 0.12 x Vcc ± 10% peak centred on VREF.

The IQ inputs must be filtered to avoid alias components and must keep all noise components below -79dBc on the exciter output.

After filtering the IQ signals are sent to the IQ modulator where they are mixed along with the TX Offset LO (see below). A pair of active mixers are used at this point where the outputs are recombined in a passive load and then buffered and amplified and then passed to the limiter stage and is output at -16dBm ±2dB into 200ohms at pin 4 of U220.

The output of the modulator is controlled by the MOD_EN pin 60 (U220). This is a digital input which controls the output of the limiter. A logic high on this pin enables the limiter output and a logic low reduces the output to -35dBm or less, this logic low also reduces current by disabling the TX Quad Generator, Mixers, IQ Buffers and limiters. The offset LO will remain locked.

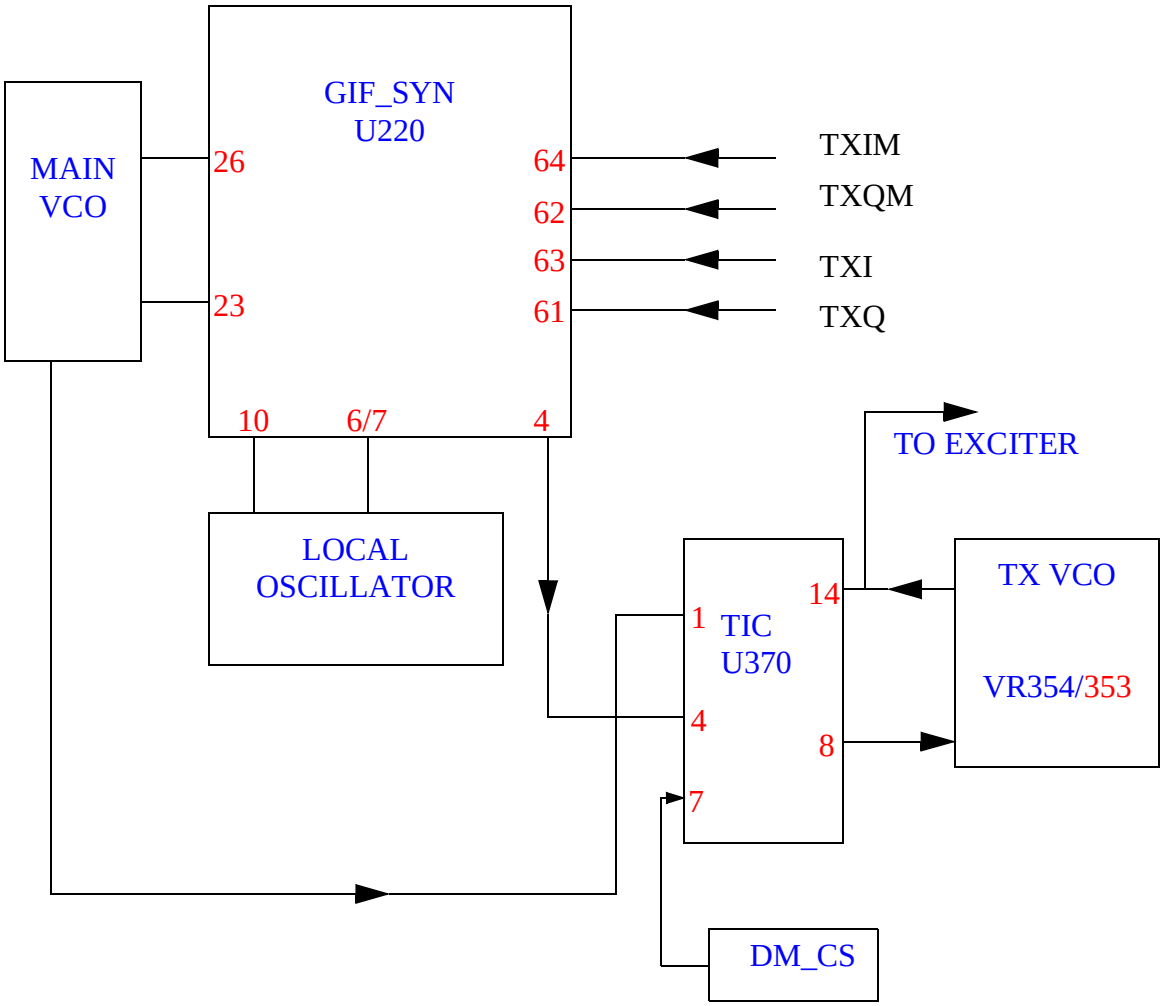
The Tx Offset LO does not frequency hop but is still fast to assure turn on times of less than 600useconds. This allows the offset VCO to be shut down between Tx bursts. The Tx Offset LO uses a 1Mhz reference derived from the 13Mhz reference.The tank circuit used operates at 340Mhz for GSM **and 240Mhz for DCS** and is divided by two internal to the GIF_SYN.

The resultant output of the limiter 170/**120**Mhz ± 67Khz frequency shift, depending on the relationship of Q & I, is then sent to pin 4 of the TIC I.C.

The TIC I.C. (U370) converts the low frequency GMSK modulated IF signal from GIF_SYN pin 4 to the final transmit frequency without introducing noise. The TIC uses a phase lock loop (PLL) to lock the low frequency modulated 170/**120**Mhz signal to the difference between the main VCO (RX VCO) and the Tx VCO, so the loop would be locked if the difference between the Rx VCO and the Tx VCO is 170/**120**Mhz.

The Tx VCO signal is sent to pin 14 of the TIC. The Rx VCO enters the TIC at pin 1. These two signals are mixed and the difference is input to the phase detector, internal to the TIC, along with the IF input and the resultant output of the phase detector is the correction voltage that goes to the VR354/**VR353** of the GSM/**DCS** Tx VCO to change the VCO frequency. The output of the TIC is enabled by the DM_CS signal(pin 7) that is controlled by U701 pins D2 & F1.

See Diagram Overleaf;



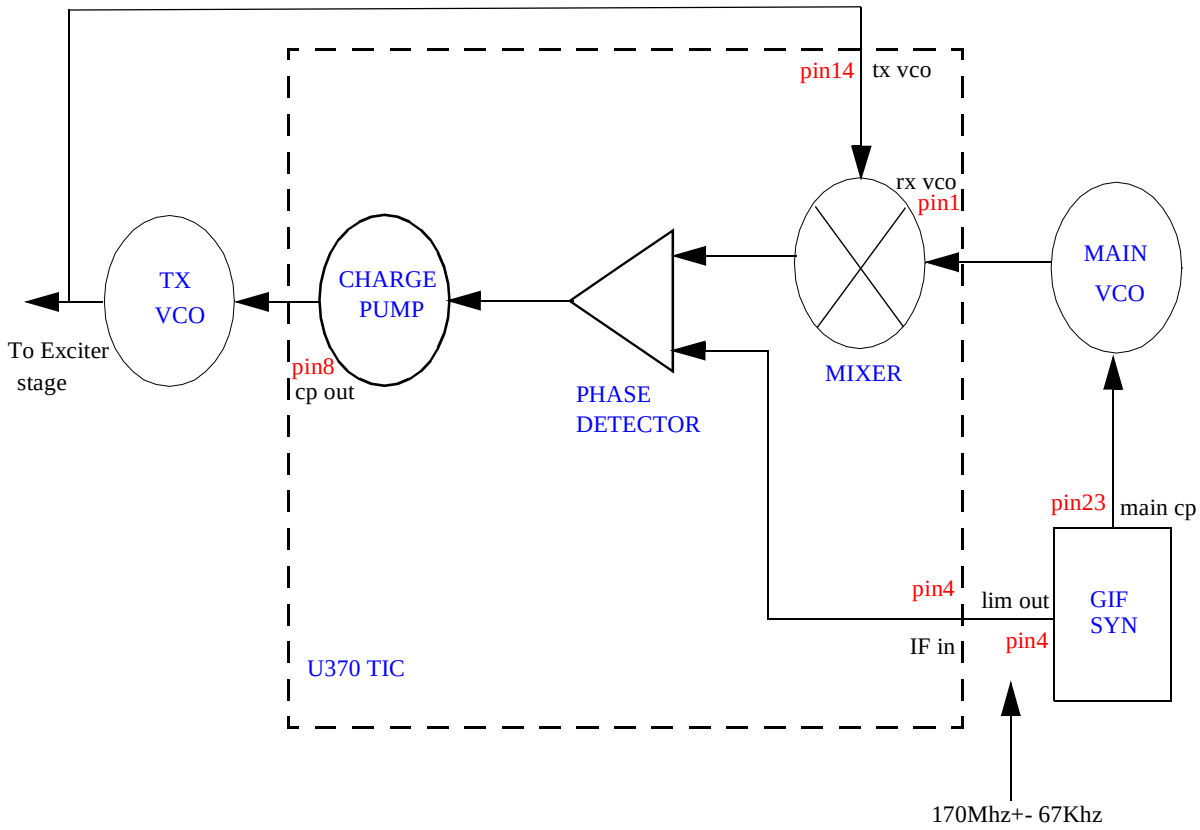
BLOCK DIAGRAM OF GYF SYN TO TIC.

TIC OPERATION.

For the following example, we will use the mid channel on GSM.

The GIFSYN (U220) will tune the main VCO to 794.2 MHz by outputting the proper DC voltage on pin 23 (MAIN_CP). This main VCO signal will then be input to pin 1 of the TIC (U370). The GIFSYN (U220) will also output a 170 MHz +- 67 KHz signal on pin 4 (LIM_OUT). This signal will be input to pin 4 of the TIC (U370).

Initially, the output of the mixer will not be 170 MHz because the TX VCO feedback (pin 14) is not 902.4 MHz. So, the PLL will not be locked. The phase detector will then steer the charge pump to change CP OUT (pin 8) until the TX VCO is oscillating 170 MHz above the main VCO and the PLL will be locked. When the radio changes channels the GIFSYN will tune the main VCO to the desired channel. This in-turn will change the output of the mixer causing the phase detector to steer the charge pump to change CP OUT until the TX VCO signal is 170 MHz above the main VCO and the PLL is locked.



BLOCK DIAGRAM OF TIC OPERATION.

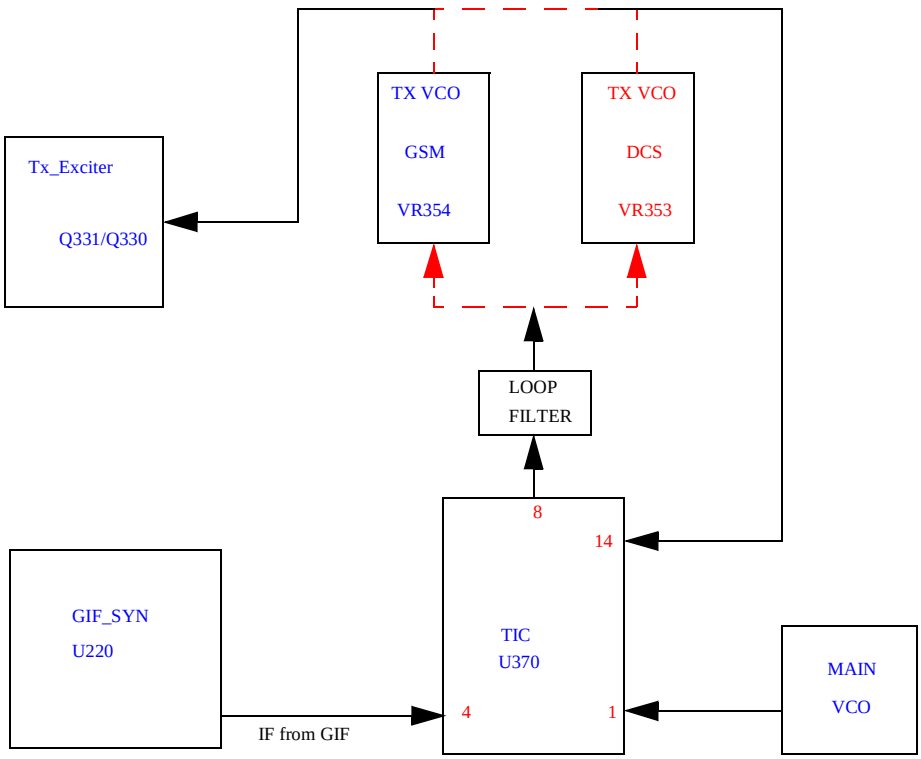
Tx VCO TO EXCITER.

Circuit Description:

Zap utilizes two Tx VCO circuits one for GSM the other for DCS. These Tx VCO's are of Colpitts oscillator configuration (capacitive feed back) where VR354 & C364 form a tank circuit for Q351,the oscillating device for GSM, and **VR353 & C356 form the tank circuit for Q350, the oscillating device for DCS.** The control voltage, CP_OUT, from the TIC (pin 8) passes through the loop filter (C378,C379 & R377) in order to clean up this signal before it reaches the required varactor for the mode of operation. Q309 determines what Tx VCO is on via control signals C1 & C2. C2 forward biases Q351 for GSM and C1 forward biases Q350 for DCS. This control voltage from the TIC changes the capacitance of the varactor; the higher the voltage, the lower the capacitance and therefore, the higher the frequency of oscillations.

Capacitors C360 & C361 are feedback capacitors for GSM and **C354 & C355 are feedback capacitors for DCS.** TL350 and TL360 are used as RF chokes to prevent RF from going to the control lines Logic_GSM_*DCS, DM_CS and B+. L350 is used as an RF choke to prevent RF from going onto the R275 supply voltage. Transmission lines TL351 & TL361 are used as part of the frequency determining network for their respective circuits.

The output of the VCO's are then sent to two points: pin 14 of the TIC and to the base of the Tx Exciter buffer amplifier Q331 and then onto the exciter Q330.



BLOCK DIAGRAM OF Tx VCO TO EXCITER

FROM EXCITER TO POWER AMP.

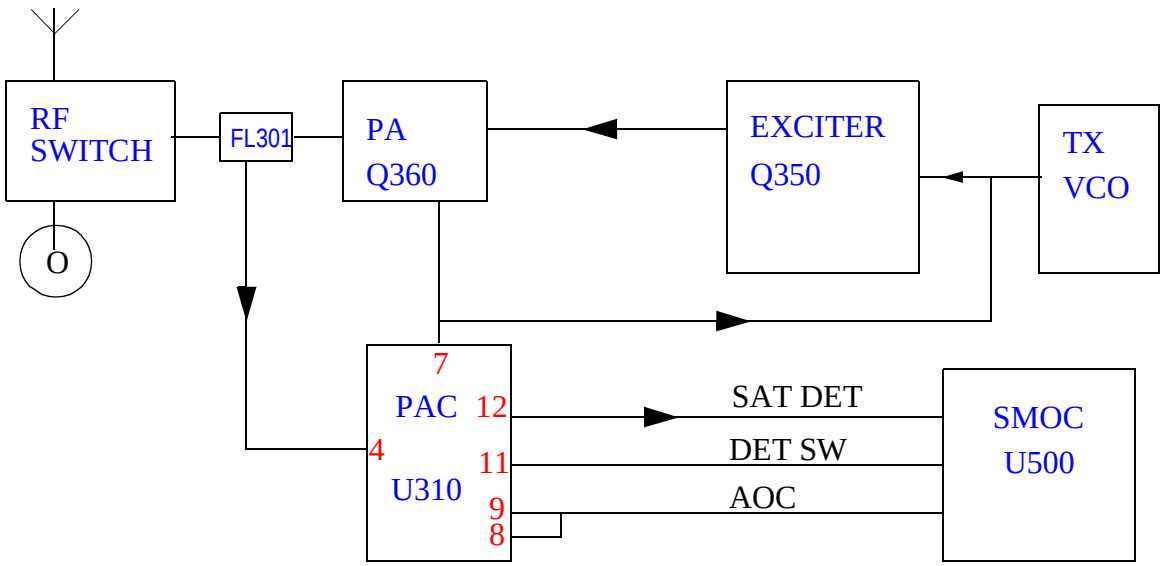
Circuit Description:

The input from the Tx VCO is passed through the driver Q330 to produce a gain of 8dBm/12dBm, then the signal is passed through a impedance matching circuit using C316, C334, C329, C324, C396, TL310, TL309. The signal is then input to the PA via pin 8. The exciters output is controlled by the PAC I.C. (U340). This IC allows the amplifier to have a linear control voltage for ramp up/down of the PA output level. Once the transmitter is on, the peak RF power of the PA will be coupled back to pin 2 (RF_IN) of the PAC via the filter FL301. The RF detector internal to the PAC, will output a DC voltage proportional to the peak RF power. The RF detector output will be an input to a comparator (internal to the PAC), which is used to indicate the presence of the RF power. The gain is determined by pin 11 (DET_SW). This is a control signal from the SMoC to the PAC.

The AOC is an input from the SMoC to the PAC, its output level is determined by the PA DAC values 0-15. The voltage on the AOC will determine the output power of the transmitter. The output on pin 7(EXC of the PAC) will drive the exciter and PA stages so that the RF power level presented to the RF detector results in equality of the voltage present at pin 6(INT) and pin 8(AOC).

When this condition is met, the PA is being driven at the proper level.The PAC I.C. also contains a saturation detector. If the buffer amplifier lags too far behind the AOC signal, its output pin 12(SAT_DET) will go low, indicating that the loop is near saturation. SAT_DET is output from the PAC I.C. to the SMoC I.C., when this signal is low the SMoC will reduce AOC until pin 12(SAT_DET) goes high.

The Tx output of the PA (pins 2,3,4) will be input to the bandpass filter FL301(17dBm/**13dBm** Loss) before being passed onto the RF Switch (U401 pin 2). The RF Switch will then route the Tx signal to the antenna or the external connector whichever is required.



PAC IC OPERATION.

Circuit Description:

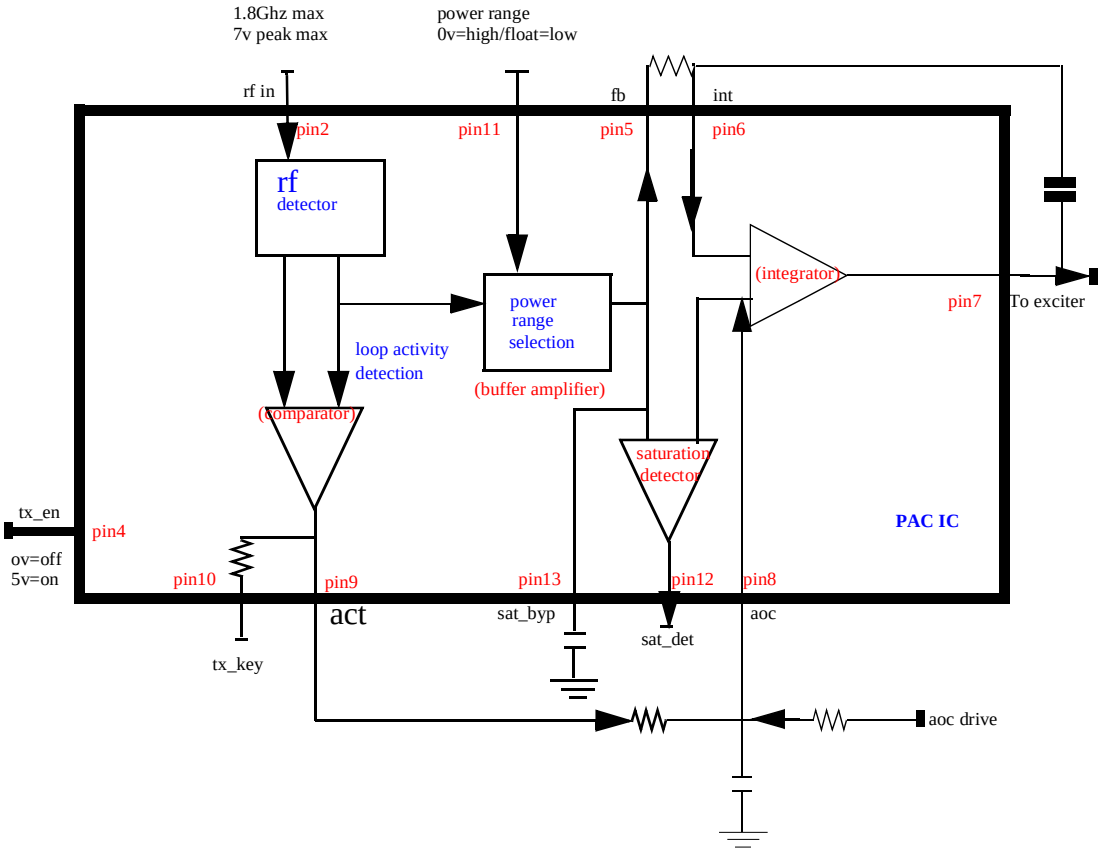
The PAC IC (U340) is used to provide precise control for the ramp up/down, of the transmit power of the radio transmitter.

Once the transmitter is on, the peak RF power out of the PA (U301) will be fed back to the PAC IC pin2(RF_IN) via FL301 and C341. The RF detector internal to the PAC, will output a DC voltage proportional to that of the peak power. The RF detector output will then be an input to a comparator (internal to the PAC), which is used to indicate the presence of RF power, a sufficient RF level must be present in order to be measured by the detector, the RF detector output will also go through a buffer amplifier which has a two gain setting. This gain setting is determined by pin11 (DET_SW). This is an input to the PAC IC from the MODEM. Its output level (high or low) is determined by the DAC values (DET_HIGH and DET_LOW). When pin11 (DET_SW) is low the gain will be **1** and when it is high the gain will be **3**.

The comparator output which is pin9 (ACT) will be low when the RF detector detects an RF signal at pin2 (RF_IN). The output from the buffer amplifier will be an input to the integrator from pin5 (F.B.) via external resistor R340 and back to pin6 (INT). The other input to the integrator will be pin8 (AOC). The AOC is an input to the PAC IC from the MODEM IC, its output level is determined by the PA DAC values 0-through-15. The voltage on the AOC line will determine the output power of the transmitter. The integrator output pin7 (EXC) will drive the exciter and PA stage, so that the RF Power level presented to the RF detector results in equality of the voltage present at pin6 (INT) and pin8 (AOC).

When this condition is met, the PA is being driven at the proper level. The PAC IC (U340) also contains a saturation detector. The output of the buffer amplifier and the input on pin8 (AOC) will be the inputs to this detector.

See Diagram overleaf:



BLOCK DIAGRAM PAC IC.

RELEVANT CONTROL SIGNALS FOR THE RF PATH.

Rx_EN

Rx_EN is generated by the microprocessor (pinA9) and is used to control the mixer and LNA bias. When Rx_EN is low the front end is muted.

Rx_275

This supply to the front end is taken from the V2 regulator(Q221) on the GIF_SYN. It is used to bias the receive front end LNA. The voltage is regulated at 2.75Vdc +/- 50m Vdc.

SW_VCC

This signal comes from the GIF_SYN regulator via pin 33 and is used to supply the Isolation amp. It also supplies the diode switching network Q100 & Q105 for the GSM_*DCS/*GSM_DCS signals.

VREF

This switched supply is generated in the GCAP (pin 11) and is on when ever the radio is on. The supply is used for the reference inputs of the GIF_SYN IC regulators on the RF section. typically 2.75Vdc +/- 75mVdc.

RF_START

This signal is generated in the microprocessor (pin C2) and drives the GIF_SYN IC. The signal must be high in order the allow changing data into the shift registers without affecting the current programming. The pulse also initiates the adapt sequence in the receive IF section.

R475

This regulated supply is generated by the FCAP (pin 41) and is on when ever the radio is powered up. It is used to drive the charge pump section of the GIF_SYN IC and TIC IC.
Typically 4.75 +/- 75mVdc.

R275

This signal is generated by the GCAP (pin 28) and is used to supply voltage for the TIC and the TX_VCO.
Typically 2.75Vdc +/- 75mV
(Note all these sections will be enabled by TX_EN.

Tx_EN

This is an inverted version of TX_ON_OFF from the microprocessor(pin B1) and is used by the GIF_SYN,TIC, TX_VCO, and the T/R-RF switch.

-1OV

This is a low current supply used by the Tx/Rx switch and is generated externally by regulator U101 using L500 as its supply.

DM_CS

This signal is generated by inverting the *DM_CS generated by the microprocessor at pinD2 (TP51).The inverted signal is a 3V CMOS level signal which is also routed to the 3V SMoC IC.

TX_KEY

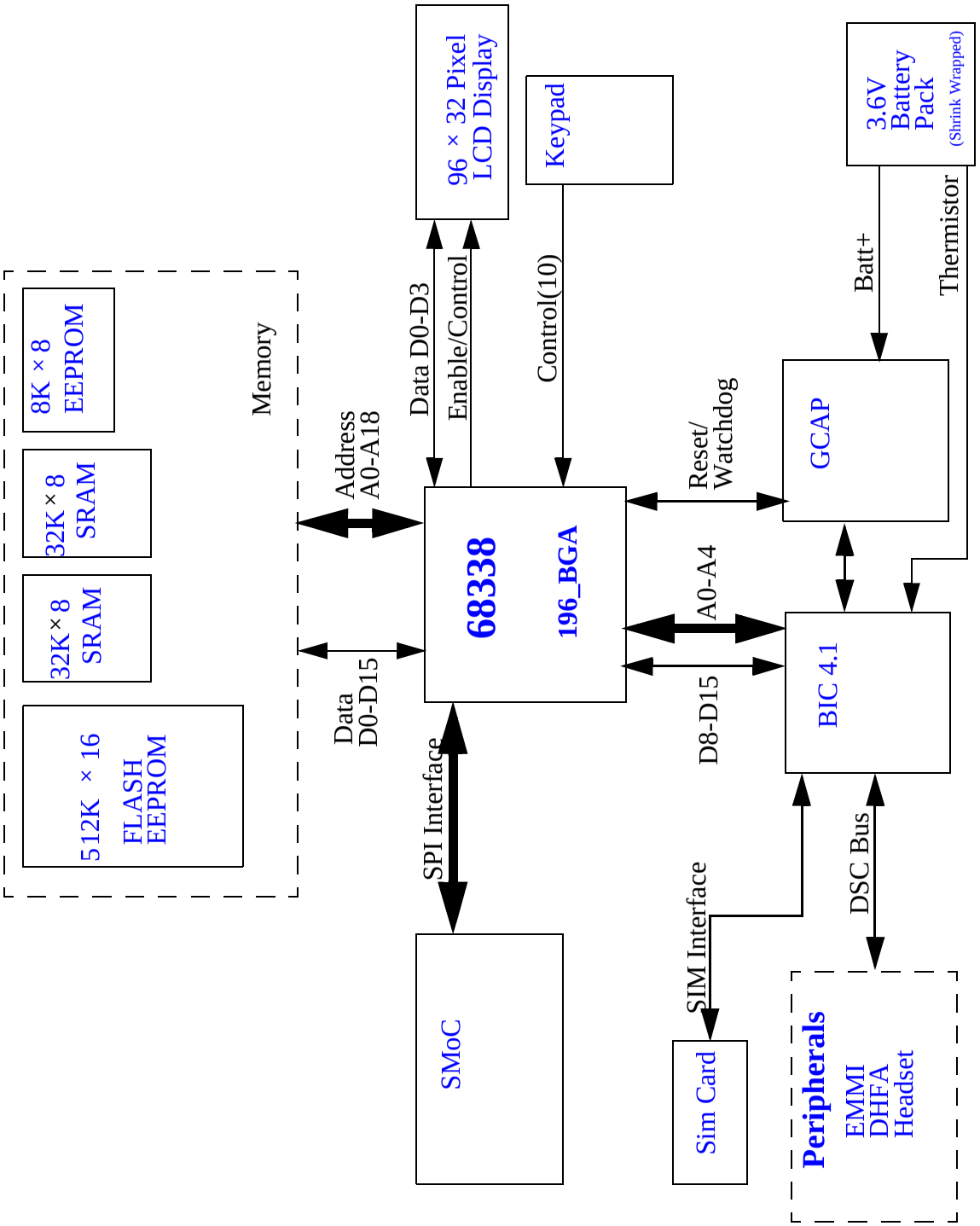
This is an Active high digital input to the SMoC IC(pin16) generated by the microprocessor(pinC1) indicating the location of the transmission bursts. It interrupts the SMoC IC and indicates the transmitter ramp up and down operation.

*GSM_DCS

This is an active low digital signal inverted from the Logic GSM_*DCS signal generated by the microprocessor(pinB5). It is used to control GSM or DCS operation and switches the Main Vco/Tx External oscillator/Tx Vco/PA/Tx filtering and LNA stages accordingly.

Section 7

CONTENTS


Memory
8K × 8 EEPROM
32K × 8 SRAM
32K × 8 SRAM
512K × 16 FLASH EEPROM
Address A0-A18
Data D0-D15
68338
196_BGA
Data D0-D3
Enable/Control
96 × 32 Pixel LCD Display
Keypad
Control(10)
SPI Interface
SMoC
Reset/ Watchdog
GCAP
Batt+
3.6V Battery Pack (Shrink Wrapped)
Thermistor
A0-A4
D8-D15
BIC 4.1
SIM Interface
Sim Card
DSC Bus
Peripherals
EMMI
DHFA
Headset

I.C.DESCRIPTION

U220 Gif Syn 5.2.

This chip has the following functions:
Generation of RXI & RXQ signals, Supplies Main VCO and external tanks, cleans up the 13Mhz, RX de-modulation, Tx modulation and data links with the SMoC.

U340 PAC IC.

This IC controls the transmit power levels of the phone.

U370 TIC IC.

This IC operates as a phase lock loop, it controls the TX VCO by the use of the Modulated IF from the Gif, the Main VCO and feedback from the TX VCO.

U500 SMoC.

This IC carries out the following functions:
Modulation, Demodulation, Rx Baseband Analogue Signals (RXI&Q + IQref), Tx Inphase & Quadrature signals, RF_SPI & RF_SCK, SPI Bus from Microprocessor to RF Board, DM_CS for TX path enable, AOC/SAT_DET/DET_SW for PAC Control, Routes speech data between SMoC and BIC, AFC Control, AGC Control and A/D Conversion via the MDM_ANA_VCC.

U701 Microprocessor.

The Call processor controls the keypad, Tx, Rx, etc. and routes data to the various IC's in the phone.

U702 SRAM.

This IC contains the phones Random Access Memory.

U703 BIC 4.1.

The Bus Interface chip is responsible for all the external communication interfacing, it contains the A/D and D/A convertors and also routes the clock to the logic IC's.

U704 Flash Eprom.

This chip contains the phones software.

U705 EEprom.

This chip contains the phones phasing data after it has passed through test.

U900 GCAP IC.

The GCAP (Global Control Audio Power) provides regulated power supplies for both the Logic and RF sections of the phone. These supplies are R475, R275, L500, L275, VREF and VSWITCH.

R475: supplies the charge pumps in the GIF and the TIC, which drive the VCO's.

R275: Is the supply/VCC for the TX VCO and the TIC IC.

L500: Is the 5V supply for the DSC bus, SIM interface and the -10V regulator used for the T/R Switch control.

L275: Is the 2.75V supply for all logic IC's, SMoC and the display

VREF: Is the reference voltage for the GIF.

VSWITCH: The supply voltage is too low for the R475 & L500, so the DC/DC convertor mode of the GCAP is used to convert the supply up to 5.6V(Vswitch).

BOOTCODES

Bootcode programming is necessary when we are using unprogrammed or virgin Eproms.

The main reason for using Virgin Eproms are:
1. Supply.....There are no problems associated with the supply of virgin eproms.
2. Cost.....The cost of using virgin Eproms is significantly reduced.
3. Adaptabilty.....Changes in software can be incorporated into the virgin Eproms much easier.
4. Security.....Our software stays in-house reducing the risk of security breaches.

The following is a list of the BDM (Background develop mode) fail codes.

BDM L275

This is a check to see if the 2.75V is present at the output of the Gcap. The L275 voltage level is checked by the bootcode bay probing onto one of the boot code test points on the board. Note that the L275 is a supply for the logic side of the PCB.

BDM SIMS

This is when the bootcode bay software sets up the SIM Register in the processor, so that background mode can take control.

BDM ERAS

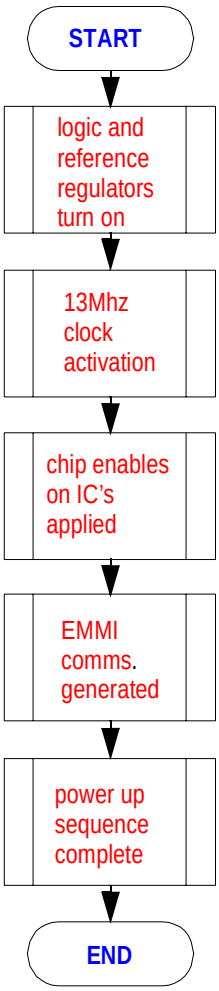
This is when the bootcode bay tries to erase all the data in the bootcode area of the Eprom whether it has already been done or not.

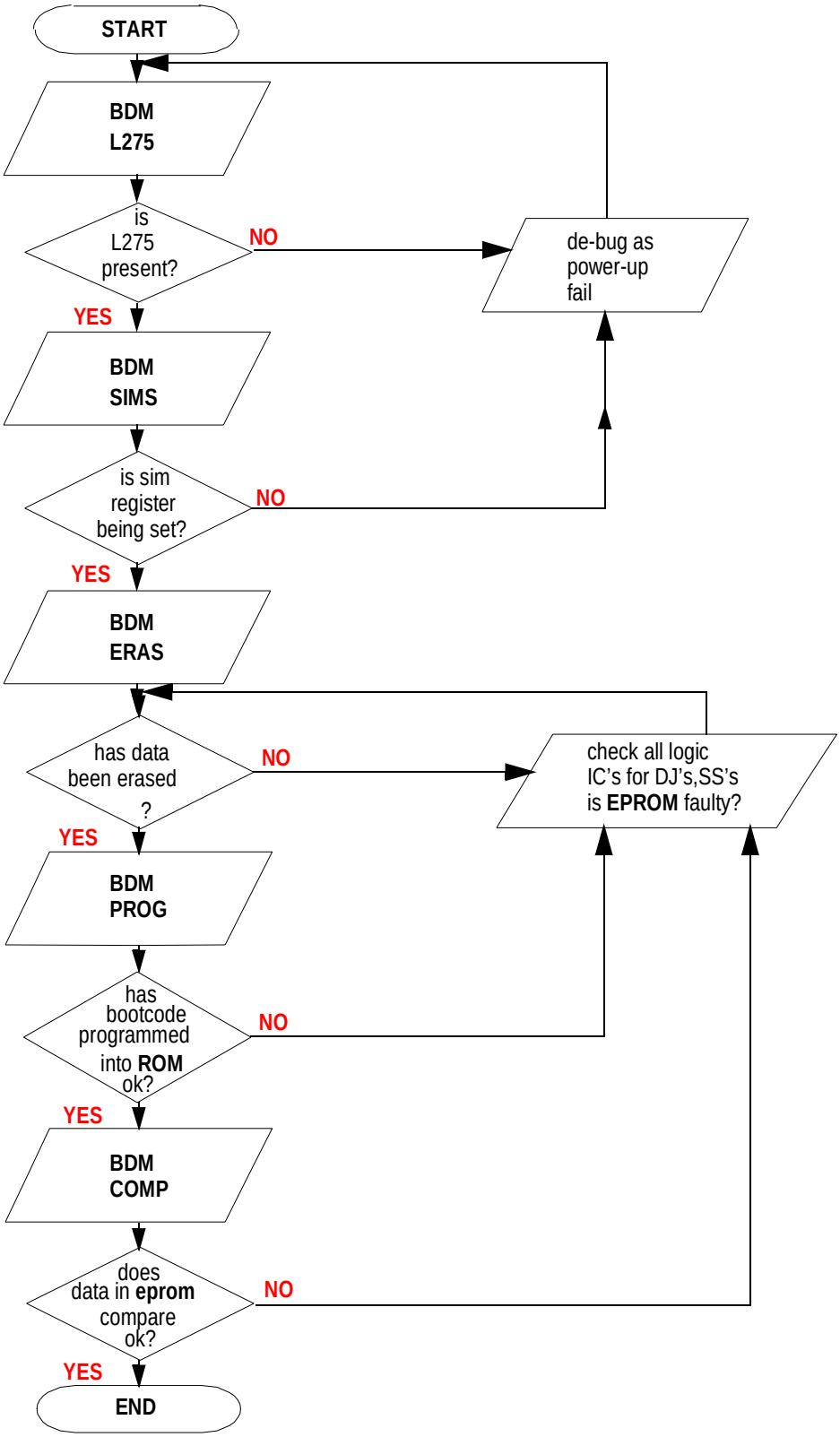
BDM PROG

The bootcode is programmed into the Eprom at this point which contains factory information relating to that particular model of phone.

BDM COMP

At this point the contents of the bootcode area of the Eprom is read back by the testbay and compared to the original data sent out.


START
logic and reference regulators turn on
13Mhz clock activation
chip enables on IC's applied
EMMI comms. generated
power up sequence complete
END



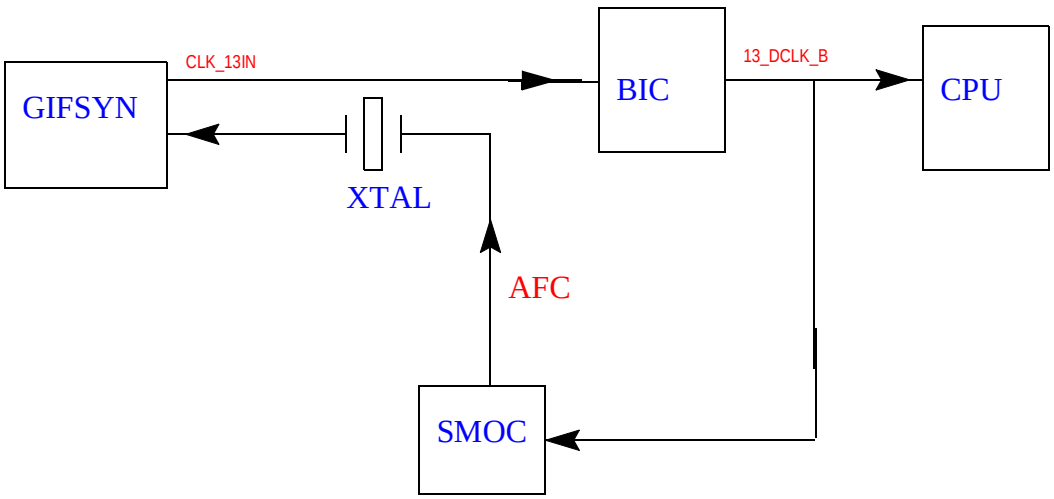
BDM FLOW CHART

POWER UP SEQUENCE

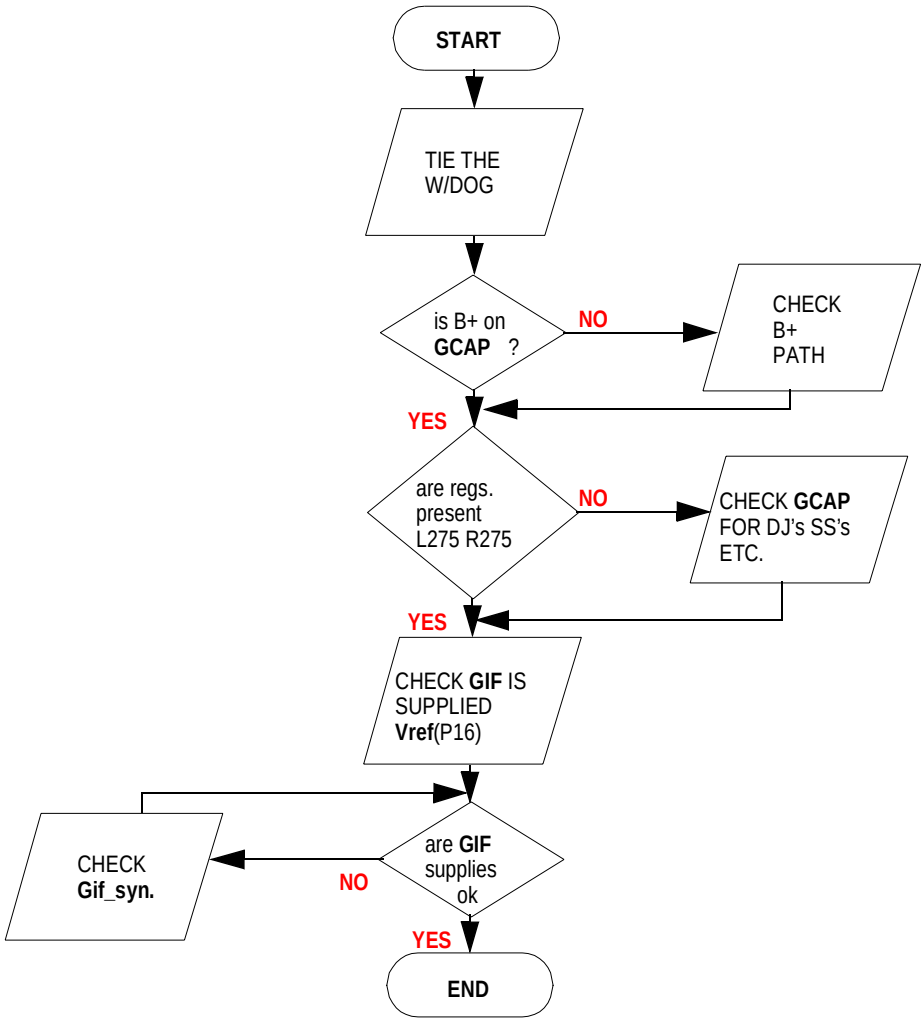
When the ON button is pressed pin 24 on the Gcap is taken low, when this happens if B+ is present at pin 40 of the Gcap, then the Gcap turns on the logic and reference regulators L275/R275 (pins 22/28). Once this has happened VREF pin11 is fed to the Gif_syn on pin 16.

When all these supplies are present the Gif_syn will turn on the 13Mhz clock. This 13Mhz clock is generated by the crystal Y702 and output by the Gif_syn at pin 59 and fed to the BIC, SMoC and Microprocessor.

At the same time the ON button is pressed the Gcap sets the reset line (pin 30) low, which allows the 13Mhz to stabilise and then allows reset to go high, allowing for bootcode programming and systems execution, i.e. chip enables, data/address bus and EMMI communications.

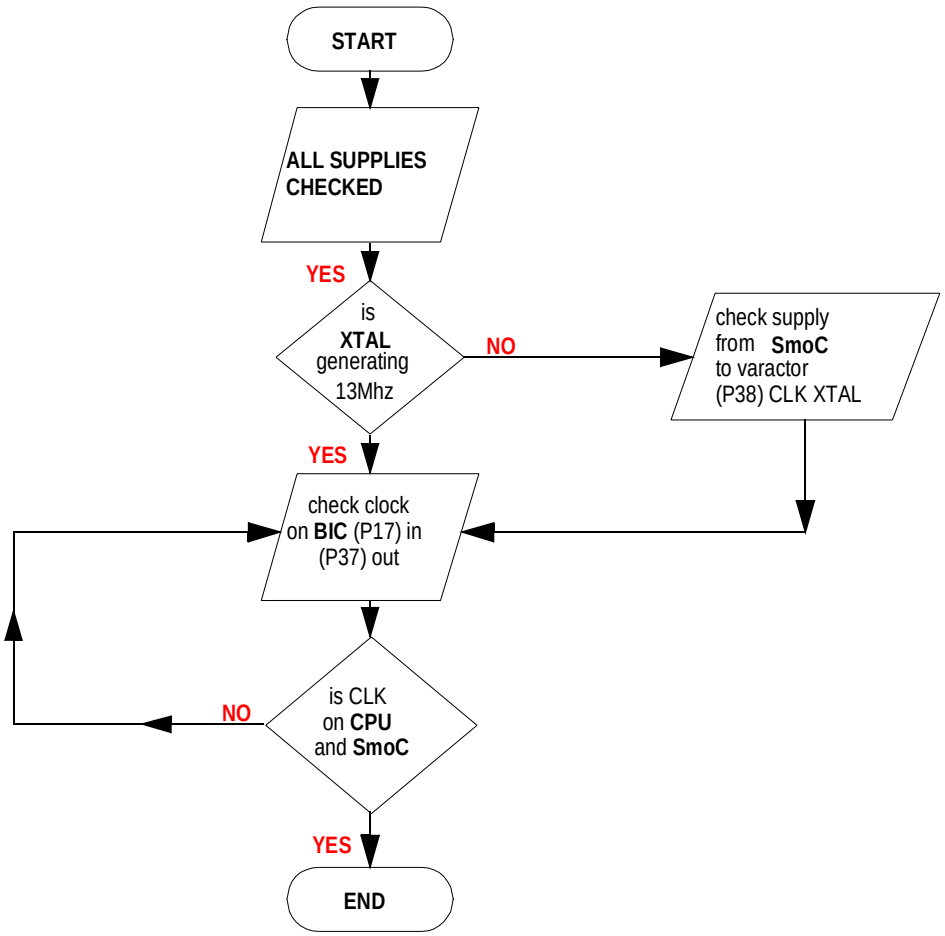


POWER SUPPLY FLOW CHART


START
TIE THE W/DOG
is B+ on GCAP ?
NO
CHECK B+ PATH
YES
are regs. present L275 R275
NO
CHECK GCAP FOR DJ's SS's ETC.
YES
CHECK GIF IS SUPPLIED Vref(P16)
are GIF supplies ok
NO
CHECK Gif_syn.
YES
END

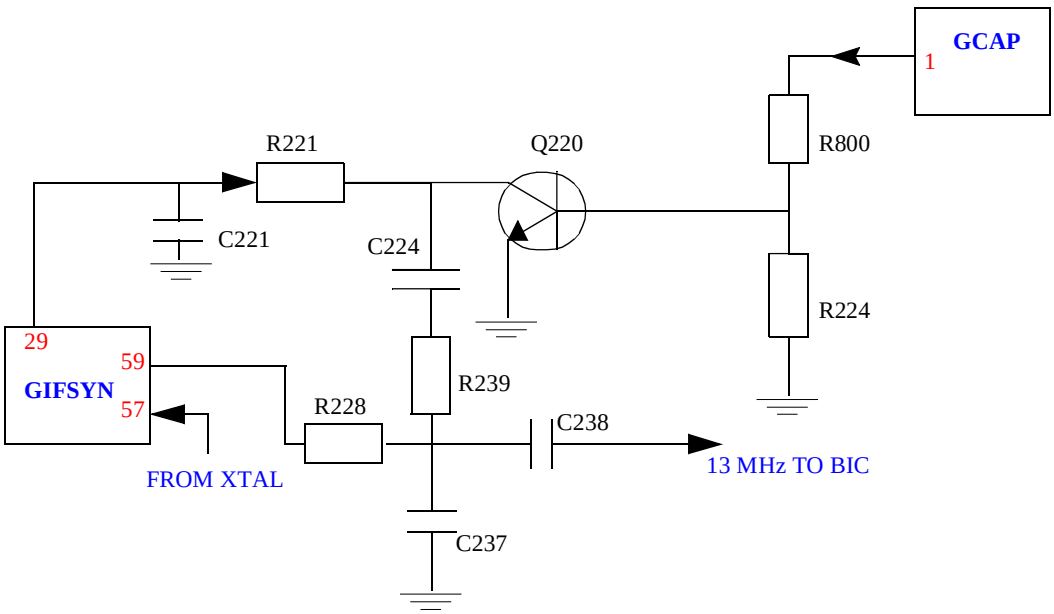
13Mhz CLOCK

The 13Mhz clock is generated by the crystal oscillator circuit (Y702). It is input to the Gif_syn (U220) at pin 57. This signal is used internally by the Gif_syn for the 2nd LO and offset VCO by dividing down to 1Mhz and for the main VCO by dividing down to 2.6Mhz to supply a reference to those circuits. The 13Mhz clock will be output from the Gif_syn on pin 59 and input to the BIC (U703)on pin 17. The BIC will amplify and square up the 13Mhz and output it on pin 37, where it changes to 13_DCLK_B. This signal will then go to the microprocessor (U701) pin M7 and also the SMoC at pin 40.



CLOCK MODULATION CIRCUIT

Due to the 62nd and 63rd harmonics of the 13Mhz crystal clock interfering with the transmit frequencies on channels 5 and 70, a clock modulation circuit is used on the clock output. Internally programmed in the Gif_syn is the software to enable this, only when on these two channels. When this happens the Gif_syn outputs a 2.75V 500Khz pulse to the collector of Q220. The Gcap constantly gives a pump output to the base of Q220, which is also a 500Khz signal. These two signals will switch on Q220 and amplitude modulation takes place in the 13Mhz output from the Gif_syn. This will introduce some phase modulation which will knock the 13Mhz plus or minus off frequency very slightly and will therefore knock the 62nd and 63rd harmonics off frequency a lot further away from the transmit channel frequencies of channels 5 and 70. See below:



AUDIO CONTROL CIRCUITRY

When referring to audio circuitry we are talking about the circuitry used to transfer the audio signals from the input source to the U500 (SMoC), or from the U500 to the audio output. The audio input source can either be from the radio's microphone or an external microphone. The audio output source can either be the radio's speaker, the radio's alert speaker or an external speaker. We can therefore see that there are a number of different paths that can be used by the phone to transfer these audio signals.

The routing of these signals is controlled by the microprocessor (U701) via the SMoC IC using the control ports AUD_EN1(U500 pin 57) and AUD_EN2(U500 pin 60). These Audio Enable lines go to U900 pins 44 and 45 respectively. By switching these ports either high or low the processor can control which of the internal amplifiers of U900 are activated thus controlling which audio path is being used. The table below shows the Audio enable signal combinations.

AUDIO SOURCE	AUD_EN 1	AUD_EN 2	Ear Piece	Alert	Mic	Ext. Aud
No Audio Signals	0V	0V	OFF	OFF	OFF	OFF
Radio mic/speaker	0V	2.7V	ON	OFF	ON	OFF
Alert	2.7V	0V	OFF	ON	OFF	OFF
Car Kit Connection	2.7V	2.7V	OFF	OFF	OFF	ON

Audio Enable Signal Combinations.

A-D CONVERSION OF AUDIO SIGNAL

When the audio is in a call, the analogue signal is digitally coded inside the U500. The digital coding process is as follows:

* Analogue signal enters U500.

* The signal is A-D converted by the codec section of the U500 (SMoC) resulting in a 64 kBits/sec data stream.

*The 64kBits/sec digital data is then input to the speech coder section of the U500 where it is compressed to 13kBits/sec by internal software algorithms.

* A further 9kBits/sec of error correction bits are added to the signal in conjunction with the microprocessor (U701) giving a total of 22kBits/sec of digitally speech coded signal for transmission.

* This digital stream is then sent to the modem section of the U500 where the signal is converted into TXI & Q signals which are then transmitted via the transmit path.

D - A CONVERSION OF AUDIO SIGNAL

D - A conversion is the reverse of the above process as far as the codec. Then, after the codec converts the signal to analogue, it is amplified within the U500 before being sent to U900. The attenuation is variable from 0 - 35dB in eight 5dB steps and controls the audio volume. The signal then exits U500 and follows the configured audio path to U900.

Note:- When the radio is in audio loopback mode the following happens.

* Audio signal is passed through the input path.
* Signal is digitally coded.
* Digital information is looped back and decoded to analogue.
* Signal is passed through output path.

When in audio loopback mode the analogue signal is coded, looped back and decoded - it is not sent to the modem to be converted to I & Q signals.