GSM
Service Support
Level 3 Authorized

C37x/C450/ C550 Family

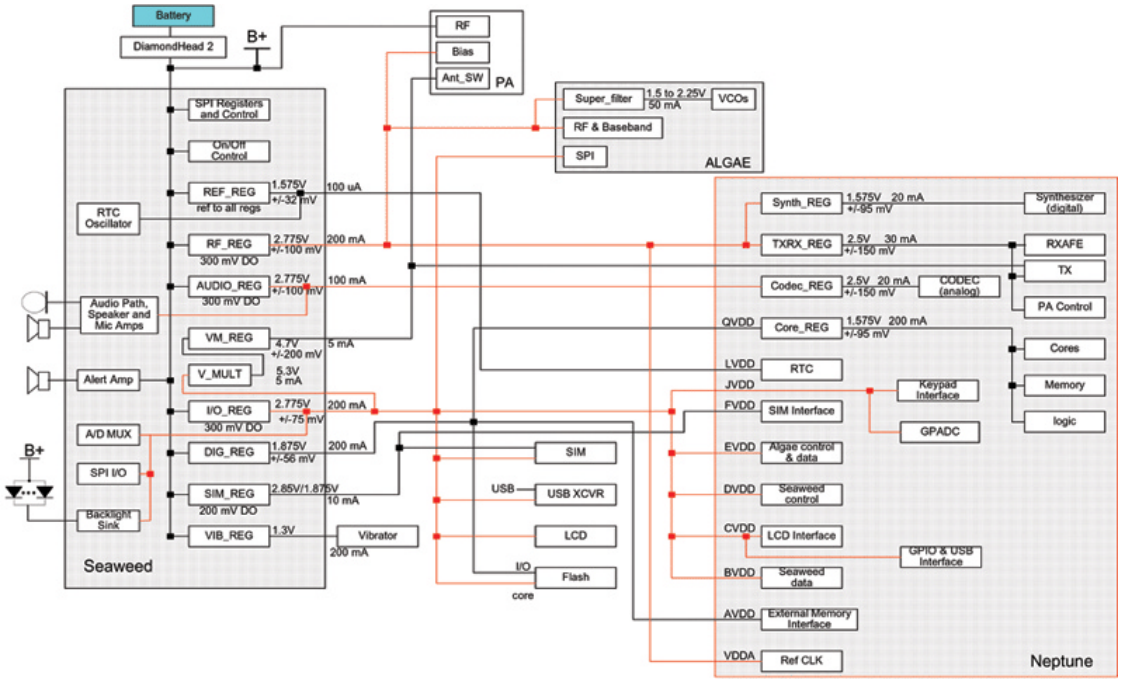
Level III
Circuit Description V1.0

General

The LCA Platform contains the new Triton Chipset consist of:
ALGAE, NEPTUNE,ATHENA, SEAWEED and DIAMONDHEAD with extrenal protection circuit. The phone is designed with an internal Antenna and as Quard Band Tranceiver but will only be sold as Dual Band 850/1900 MHz or 900/ 1800 Mhz. This is done by flexing the phone to the need of the different regions.

Power Distribution Overview

Power is distributed throughout the Triton Chipset from a variety of linear regulators, a capacitive voltage multiplier, as well as direct connections to B+. The primary power manager is the Seaweed IC, which receives its voltage input from the battery via the Diamond Head2 B+ output. A detailed description of DiamondHeads charge/safety functionality is presented from Page 7-9. Seaweed alone contains 8 of the 12 linear regulators present in the chipset. These regulators provide power to module blocks both internal and external to Seaweed. In addition, Seaweed contains a capacitive voltage multiplier that provides a 5.3V nominal output, which is linearly regulated down to 4.7V to supply the higher voltage modules. Seaweed's 1.575V trimmed voltage reference is used as the reference to all Seaweed regulators as well as all Neptune regulators. Neptune contains 4 linear regulators that are powered from the Seaweed regulated supplies. Both the Core and Synthesizer Regulators are used to provide a more solid supply to their respective blocks. The TXRX and Codec Regulators are used to improve power supply rejection on their blocks, which are sensitive to noise and supply ripple. The rest of the Neptune blocks are powered directly from the Seaweed regulated supplies.
Algae contains 1 linear regulator which is powered from a Seaweed regulated supply. This Super Filter Regulator provides power to the noise sensitive VCO's. The rest of the Algae blocks are powered directly from the Seaweed regulated supplies.
The Athena PA module receives its RF power directly from radio B+, due to its voltage and current requirements. The rest of the Athena blocks are powered directly from the Seaweed regulated supplies.
The Figure next page shows the intended power distribution of the Triton Chipset, based on voltage and current requirements, as well as considerations for noise and isolation. All regulator outputs are shown with their nominal voltage, output tolerance, and current sourcing capability. See drawing 1.0 below



Drawing 1.0

Power Up/ Down Sequence

Radio Power On Methodes:

The phone is enabled by one of the following conditions:

1. A high to low transition on the Seaweed **PWR_SW** input Pin F2 when the **B+** voltage is above the Under Voltage Threshold of 2.65V DC (nominal). **PWR_SW** is asserted low by the ON/OFF key depression.
2. A low to high transition on the Seaweed **EXT_PWR_ON** input.
   EXT_PWR_ON is asserted by the DiamondHead 2 IC when external power from a charger is applied and when the battery voltage is above the Turn On Threshold of 3.0V (nominal).
3. A low to high transition on the Seaweed **STANDBY_TODAI** input when the **B+** voltage is above the Under Voltage Threshold of 2.65Vdc (nominal) and **RESETB** is set low.
   STANDBY_TODAI is asserted by the Neptune IC when the phone recovers from a power cut or when a Time of Day alarm from the Real Time Clock is due.
4. The **B+** voltage rises above the Under Voltage Threshold of 2.65V nominal.

Radio Power Down Methods:
The phone is disabled by one of the following conditions:

5. Software-initiated power down.
   When the user requests to turn the phone off by pressing the ON/OFF key, or when a low battery voltage is detected by software through the general purpose ADC measurement, or when the RTC timer expires, Neptune drives the WDI line low. When WDI goes low the Seaweed IC and therefore the phone turns off.

6. Hardware-initiated power down.
   When the B+ voltage drops below the UV Comparator Threshold, **RESETB** goes low which in turn causes Neptune to put the **WDOGB** output into a high impedance state. An internal pull down resistor on Seaweed brings the W**DOGB** line low and thus the phone shuts off.

Power Up/ Down Sequence

Power On from ON/OFF Key:

1. ON/OFF key is pressed when the **B+** volt. is above the U. Volt. threshold (B+>2.55V)
2. **PWR_SW** goes low internal \ON goes high
3. ReferenceRegulator **RTC_GRP** is always on if battery is in a good range
4. In U900 the internal signal REGBIAS_EN goes high
5. 2 msec later the two Regulators **DIG_1,875** and **IO_2,65** goes high
6. 4msec later the two Regulators **RF_REG** and **VM_REG** goes high
7. 8msec later the internal Seaweed WATCHDOG and RESET Timer start counting
8. 4msec later the two Regulators**VM_REG** and **AUDIO_REG** goes high
9. 46msec later RESET Timer output goes low, **RESETB** goes high
10. within 50msec Neptune asserts **WDOGB** before Watchdog timer output goes low
11. ON/OFF key is released

Power OFF from ON/OFF Key:

1. ON/OFF key is pressed
2. **PWR_SW** goes low
3. In U900 the internal signal **REGBIAS_EN** goes high
4. 2 msec later the two Regulators **DIG_1,875** and **IO_2,65** goes low
5. 4msec later the two Regulators **RF_REG** and **VM_REG** goes low

8msec later **REGBIAS_EN** goes low; all regulators except for **REF_REG** are disabled

Power OFF from Under Voltage:

1. **B+** voltage drops below UV Threshold (B+<2.55V)
2. Internal Seaweed UnderVoltage Comparator and UV Timer output goes low,
3. **RESETB** goes low
4. within 5msec Neptune puts the **WDOGB** output into a high impedance state and 100K pulldown on Seaweed pulls WDI low
5. Int. U920 signal REGBIAS_EN goes low; all Reg. except for **REF_REG** are disabled

Power Sources:

Power for the unit can be obtained from 2 sources, battery pack or external power.

Battery Pack:

The battery connector P800 will have 3 contacts, these being:
Pin 1 – **GROUND**
Pin 3 – **ATH_B+** as source on the Diamond IC U920.
Pin 2 – **TP_BATT_DETB** as battery temperature control signal to U920 **Pin 19.**

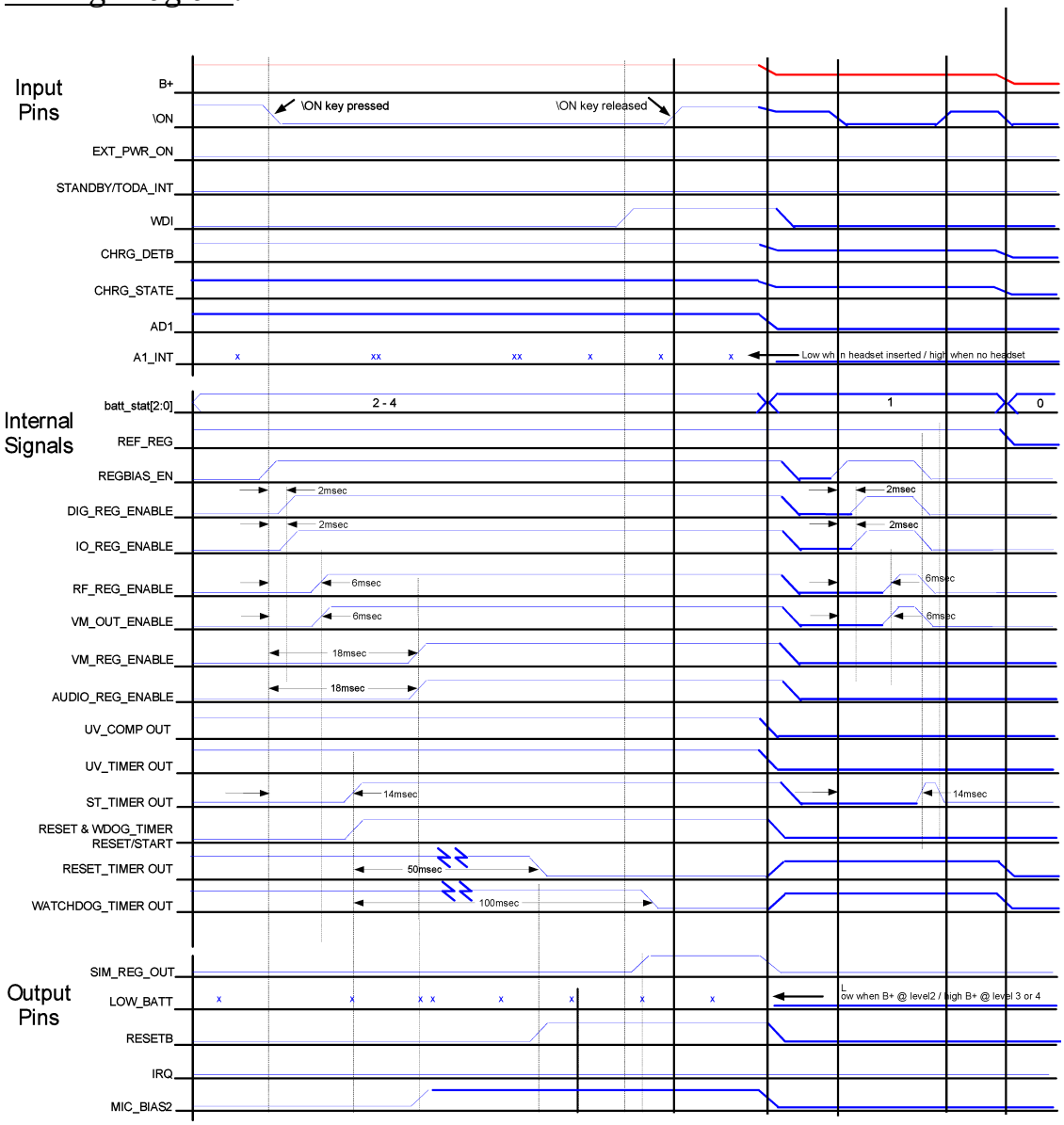
External Charger:

The external Chager source is **EXT_B+** connected via Charger Jack J900.
There are two signals to read and control the external Source.
The Signal **CHRG_ SW** is used to control the output current of EXT source, If high **CHRG_TYP** line will be read (External Charger pull down resistor biases the voltage on Charger Jack Pin2) and current is set to 400mA limit. If low current is set to 900mA limit.
External Charger could be:

1. an unregulated, current-limited wall adapter
2. a 6.2VDC nominal Vehicle Power Adapter with 1A nominal current limit

Power Up/ Down Sequence

Timing Diagram:



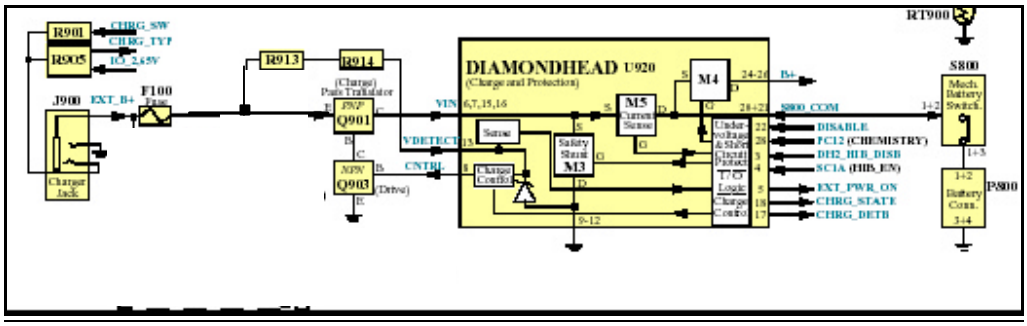
Drawing 1.1

Charger System – Diamondhead IC

General Overview:

1. The Diamondhead 2 IC U920 contains the battery charging and protection circuitry required by the Triton.
2. The battery charger is designed to function with a lithium-ion battery that is either fixed (non-removable) or removable (battery pack). The part has been designed to operate with a very inexpensive AC wall charger which provides an unregulated output voltage or a Cigarette Lighter Adapter (CLA) which provides a regulated output voltage and greater current sourcing capabilities.
3. All charging of the battery is controlled by Diamondhead 2. Protection against failure modes is handled by the design and configuration of Diamondhead 2 and the supporting external components. Over voltage, under voltage, over current and over dissipation conditions are all handled by the control circuits with Diamondhead 2 and the external protection circuit U960.
4. When the battery voltage drops below 2.375V the IC disconnects the battery cell from radio B+ in order to conserve as much energy in the cell as possible.

Drawing 1.2 Block Diagram of Diamond 2 IC



Dead Battery operation:

The IC will charge the battery up to 2.575 volts at a trickle rate 200 mA max. or less if power dissipated exceeds 0.8 watts. Once it has reached 2.5 volts, the charger will go into full rate and continue charging this way. Up until the battery voltage reaches 3.0 volts, the phone will be off. When the battery voltage goes above 3.0 volts, the EXT_PWR_ON line goes high and the phone turns on and then indicates to the end user that the phone is charging. Usually this will only take a couple seconds but may take up to several minutes in unusual situations.

Q901 Power dissipation:

Charge current control is achieved using an external bipolar PNP power transistor Q901. The Q901 device may be saturated (full rate charge) or controlled in a linear mode for trickle/topoff charging. A current-limited external power supply is required. During trickle/topoff mode, significant U-CE drop across Q901 can lead to high power dissipation even at moderate or low current levels. The DH2 IC monitors power dissipation in Q901 by measuring the voltage across Q901 Emitter to Cell+ [Q901 Vce+Voltage across M5] and I-CE (same as current through M5, used as a sense-FET) for Q901 and limiting power to a safe value.

Diamondhead Control signals:

The phone can disable charging using a logic signal to control the **DISABLE** pin. The charge limit threshold can be selected using the signal **PC12** (CHEMISTRY) pin. Charge status information is provided to the phone's logic using the **CHRG_STATE** and **CHRG_DETB** logic outputs.

CHRG_DETB – An open drain output which is low when a powered transformer connected.

CHRG_STATE – An open drain output which is low when the charging system is in the constant current charging phase.

DISABLE – An input which can be used to disable charging. Bringing this high and then low will reset the charging system.

EXT_PWR_ON – A logic output (with B+ as its rail) which goes high when a charger and a battery are present and the battery voltage is > 3 volts. This provides drive to a **MOBPORTB** type function in the Seaweed IC.

BATT_DETB – This input when pulled low is used to detect the presence of a battery. The charging system is only enabled in the presence of a battery. This is used in removable battery applications.

SC1A (HIB_EN) – Input which when brought high enables Hibernate Mode

DH2_HIB_DISB – An Input which when brought to ground disables Hibernate Mode

PC12 (CHEMISTRY) – An input which when high sets the charge termination voltage to 4.15 volts and when low to 4.10 volts.

TMDATA – Used in IC test only

TMCLK – Used in IC test only

Charging:

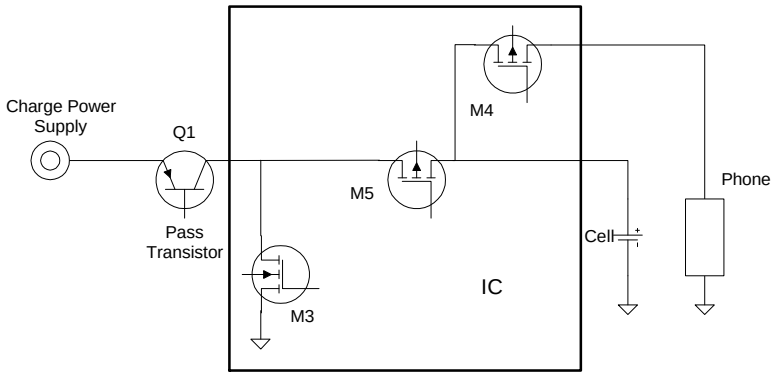
Depending on the state of charge of the cell **S800_COM / ATH_B+** (cell voltage), charging and discharging can occur simultaneously.

There are two scenarios:

discharge while charge power supply is connected and discharge while charge power supply is disconnected.

This will impact the operations of the internal PMOS/NMOS devices and the Pass Transistor Q901.

Drawing 1.3 below illustrates the relevant components of the system



Drawing 1.3 **Circuit Block Diagram**

The charge current will flow through pass Transitor Q901 (Q1) followed by M5. A part of the current will flow into the cell and a part of the current will flow through M4 to the phone. When the charge power supply is not connected the Pass Transistor Q901(Q1) will be turned off and M5 will be off. The current will be discharged from the cell through M4. A discharge state will transfer to a charge state when the IC detects the charge power supply present signal is detected. The Disable input signal will have no effect on the operation of M4 or the Discharge Operation

Fuse:
The Fuse F100 is a 2A fuse with a resistance of 0,036 Ohm at normal temperature.
It opens at 2A current after 4hours, at 4A current after 5 sec., at 6A current after 0,2sec.

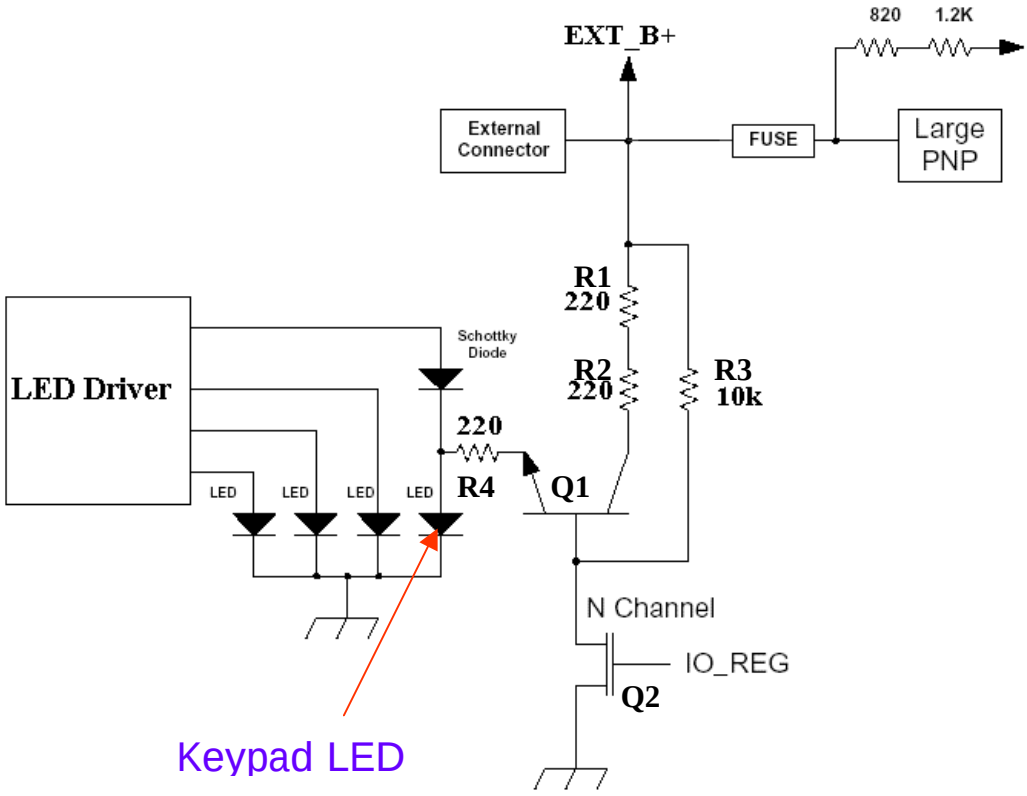
Protection System – Diamondhead IC

Internal IC protection operation: (see Drawing 1.2)
The Diomondhead has three internal protections:

1. The zener diode in the internal VETECT line to protect the Charge control for overvoltage.
2. The Savety Shunt M3- operates as a shunt theoretical zener diode with inputs from both Vin and Cell +. If Vin reaches 5.0 volts, the fast shunt operates to regulate this voltage to 5.0 volts. If Cell + reaches 4.35 volts, the slow shunt operates to regulate the Cell voltage to 4.35 volts. If the charger gets connected in reverse (Plus to Minus), M3 will turn on to protect the IC at about - 0.5 volts. The source Switch M5 is enabled in a Cell voltage range from 3 Volt to 4,35 Volt.

Sign of Life

The “sign of life circuit” turns on one keypad LED when the charger is inserted. This will give an indication of “life” to the user, that the charger has been inserted correctly and charging is in progress.
No software change is required.
Total of 7 discrete components added.



When the phone is off, than **IO_REG** is low and Q2 is open. If **EXT_B+** is connected, the Ube above Q1 closes the Collector-Emitter way and is now available to support the single Keypad LED.
If the battery in a good charge condition and the phone will be powered on, the Seaweed will generate the **IO_REG.** With presence of **IO_REG** at the Gate of Q2, the Source Drain way of Q2 will be closed and the Base from Q1 is pulled down to ground. The collector Emitter way of Q1 is now open and the LED is disconnected from **EXT_B+.**

Receive:

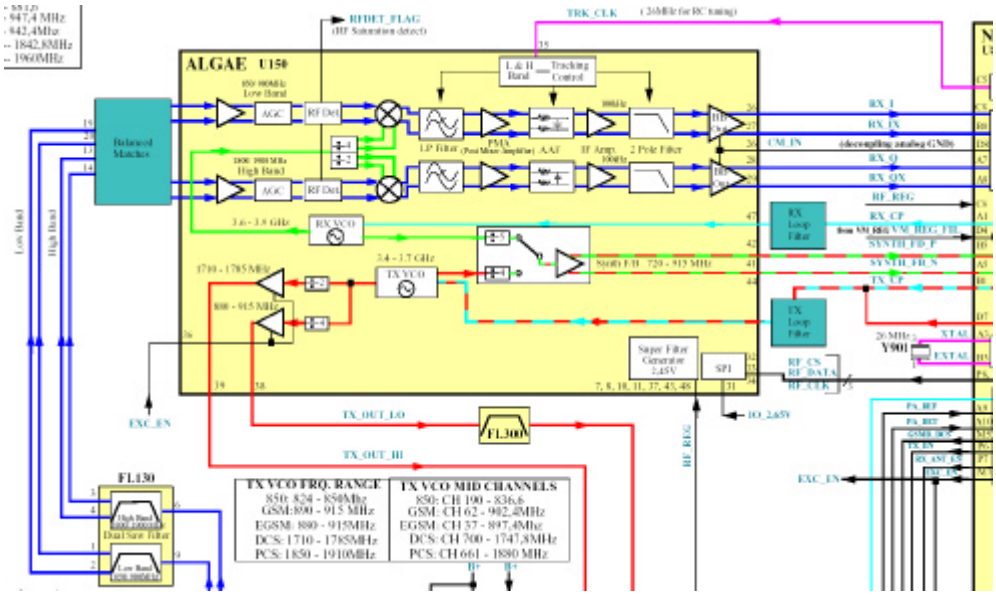
Band selection

The received signal is received through the Antenna A10.

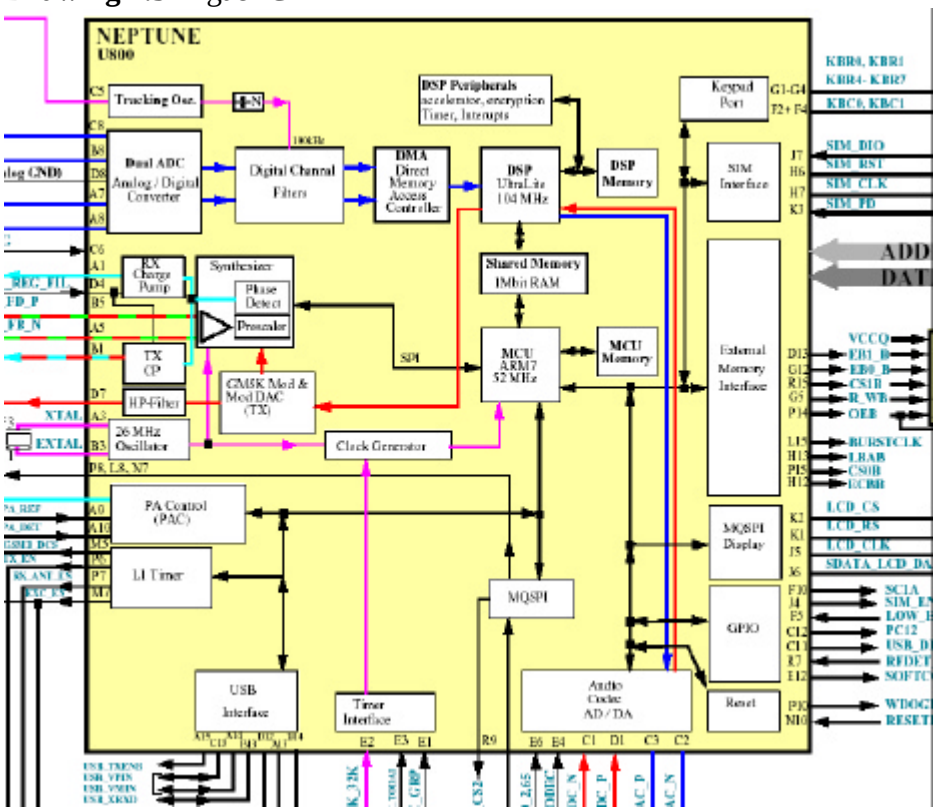
1. The received frequency is then passed through Antenna matching LC circuitry, and into the mechanical AUX RF switch J100. This is used as the Auxiliary RF Phasing / test port. The input from / to the Main antenna is **Pin 2**. The input/ Output from the Athena IC U300 is entering on **Pin 1** (The Antenna is physically disconnected once an external RF Cable is connected)
2. The received frequency is then fed into the Athena IC U300, **Pin 18**.
3. Part of the Athena is the internal Antenna Switch for RX/ TX and LOW/ HIGH band selection. The Antenna Switch is controlled by the Switch Control Circuit supported by **VM_REG.** The following three signals are driving the Switch Control Circuit: **RX_ANT_EN** as RX indication, **EXC_EN** as an TX indication and **GSMB_DCS** as an Band select indication . RX output of the Athena are the **Pins 23 /25** for LOW and HIGH Band . This signals are routed via the Dual Saw filter FL130 and the Discrete Balaced Matching circuit to the Algae Frontend.

Frontend

The receiver block diagram in the Algae IC U150 is shown in **Drawing 1.5**. Two LNAs are provided to eliminate the need for external RF switches when using the available receiver frequency bands. The LNAs drive an AGC current steering stage which will feed an RF Detect stage. If the receiver runs in saturation the RF Det. stage indicates as **RF_DET_FLAG** signal that information to the Neptune IC. At the output of the AGC follows the quadrature mixers that convert the RF signal in use of the RX VCO to **100 khz baseband**, quadrature I and Q. Large integrated capacitors are used to provide a low frequency low pass corner at the output of the mixer. The signal then passes through the baseband amplification, anti-aliasing filtering, IF amplification and 2 pole filter before going to an ? ?analog to digital converter on Neptune.



Drawing 1.5 Algae IC



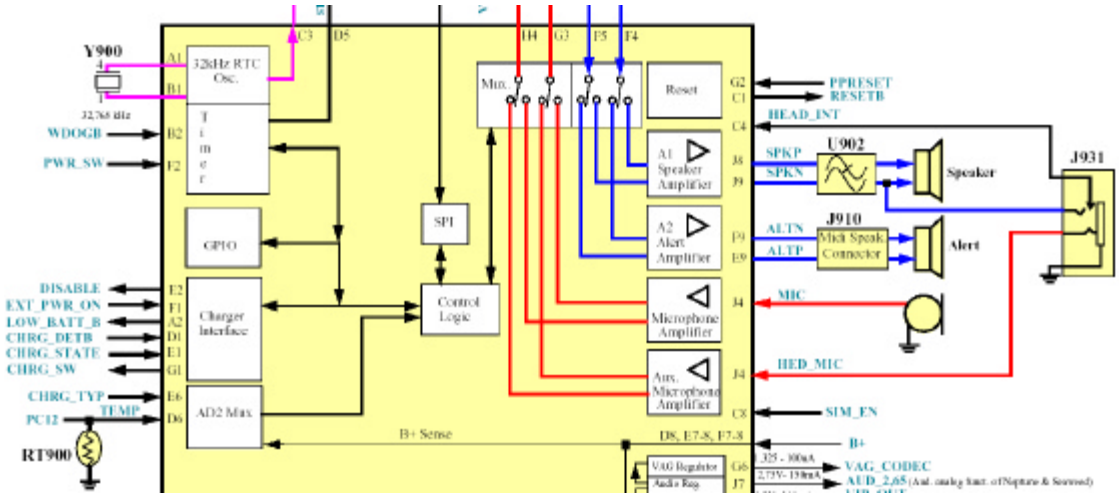
Drawing 1.6 Neptune IC

Demodulation (Neptune U800)

The RXI and RXQ signals are feeded in the ??Dual ADC stage on **Pin C8, B8, A7 and A8**. From here the digital converted signal needs to be removed from the 100Khz IF Carrier. This will be done in the Digital Channel Filter section with help of the down converted Tracking Osc. Signal to 100Khz. (zero mixing).
The demodulated signal then will pass in the DMA stage: This stage will work as an Memory Buffer for the received data packages. The DSP (digital Speech Processor) will request the data packages in time from the Memory (RX_ACQ funktion on Whitecap Platfrom).
The DSP will split the package in Audio and Control . The Control datas will be used from the Neptune Core MCU to control the phone.

Audio (Neptune U800)

The Audio datas will be feed down to the Audio Codec Stage to convert them to analog.
The Audio Ringer signal will also be generated in the DSP to be routed down to the codec.
Output to the Seaweed IC U900 are **Pin C2 and C3**.



Drawing 1.7 Seaweed IC

Receive Audio (Seeweed U900)

Input at the Seaweed are **Pin F4 and F5 DAC_N** and **DAC_P** (**D**igital/**A**nalog **C**onverted **N**egative /**P**ositive)**.** The audio will be multiplexed to the Speaker or to the Alert aplifier, depending of the signal. This will be controlled in use of the SPI Bus from Neptune to Seaweed.
The Alert is connected via J910 elastomer pads to the PCB and Pin **F9/E9 ALTN /ALTP** to the Seaweed IC.
The Speaker amplifier signal output, **Pin J8/J9 SPKP/SPKN** from Seaweed is passing the U902 Audio Filter to avoid noise signals in the Speaker.

Polophonic IC U980 (OKI)
The polophonic IC is responsible to enhance audio quality in the ring tones.
The IC contains a CPU a clock circuit, GPIO and a sound generator. The IC is supported by IO_2,65. Communication is provided via the Seaweed SPI Bus lines **MOSIA, MISOA** and **SPI_CLK** as clock. The clock output **CLO** from Neptune is triggering the system clock of the internal U980 CPU. The active low **SPI_CS2** from Neptune enable communication on the Seaweed SPI Bus. **RESETB** is used as the system reset signal. **TOUT5** is the Interrupt request signal. It is high when the IC is requesting the next datas.

Headset Audio
If a headset is connected to the phone, the **HEAD_INT** line will be pulled to **GND**.
This indicates to the Seaweed that the **SPKP** line will shold be disabled. This causes that the Speaker will be inactive. The Headset speaker will be supported from **SPKN** to **GND**.

RX VCO
The green LO signal is provided by a fully integrated RX VCO that drives either a divide by 2 or divide by 4 quadrature generator. In addition, a divide by five circuit is used to feedback the LO signal to the synthesizer. The divide by five circuit drives an output stage that will provide the appropriate signal level to the synthesizer prescaler. The synth. feedback balanced output stage is shared with the TX path and provides the synth. feedback signal in both transmit and receive..

Synthesizer
The synth. is controlled by the core processor via internal SPI bus and clocked by the down converted 26MHz System clock as internal 200kHz. The pescaler is programmable based on the synth. Channel information from the cpre processor. Depending of the Phase offset between the synth. feedback and the 200Khz reference,the RX or TX Charge pump is providing the CP tuning voltage to control the VCO´s signal.

26MHz System Clock
The Neptune IC contains the 26 Mhz system Clock with external Cristal Y901.
The sytem clock synchronize all time depending devices including the tracking Osc.
It will be converted down with variable divider to a usable smaler internal reference clock.

Tracking Oscillator
The tracking Osc. isolates the Neptune system clock to syncronize the digital filters in the frontend section of the Algae IC. The responsible signal is the 26Mhz **TRK_CLK** clock.

Transmit:

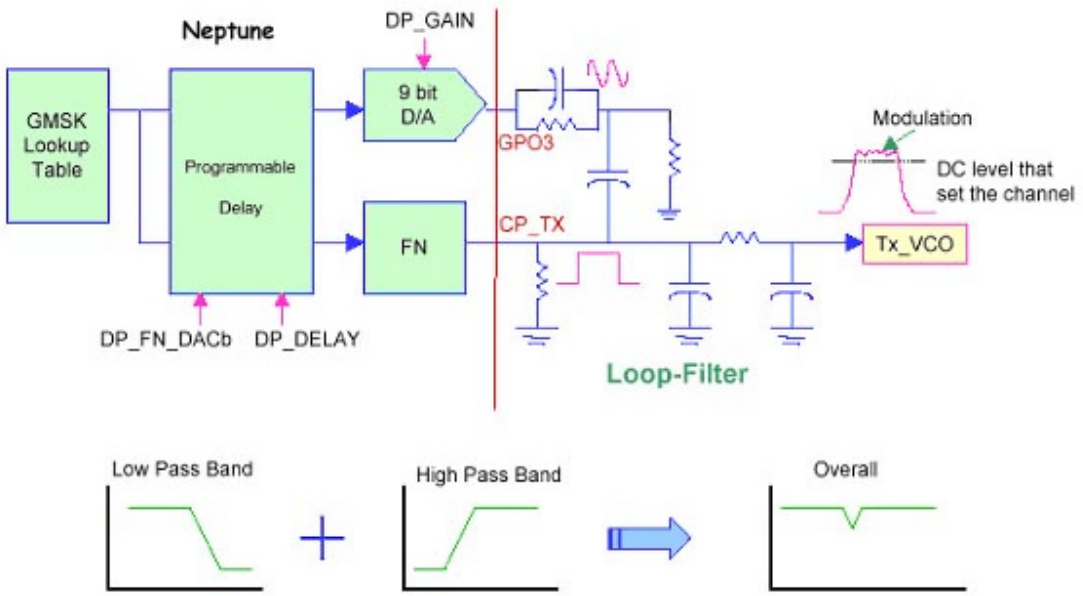
Microphone/ Headset Audio
as there were two output for Receice, there are also two methods of audio input.
First is the microphone audio at **Pin J3** at U900.
Second method is as in Receice described the Headset Microphone audio from J931 to U900 **Pin H5**.
If a headset is connected to the phone, the **HEAD_INT** line will be pulled to **GND.**
Microphone input **Pin J3** at U900 will be disabled and **Pin H5** for Headset audio will be enabled.

Transmit Audio (Seeweed U900) (Neptune U800)

Also as described in the Receive section the audio selction in the Multiplexer section of U900 is controlled by the **HEAD_INT** signal. Output Pin´s are H4 and G3 **ADC_N** and **ADC_P** (**A**nalog **D**igital **C**onverter **N**egative and **P**ositive) to Neptune input **Pin´s C1/ D1.**
Neptune converts the audio to digital signals and feeds them into the internal DSP stage.

Dual Port Modulation (Neptune U800**)**

As mentioned in earlier descriptions products we use also in the LCA series Dual Port Modulation. The high level explanation of why we have gone to this method is to reduce the phase errors that have affected past products. Basically we need to get a loop filter bandwidth of approximately 200Khz, however, the nearer we get to 200Khz, the ORFS (Output RF Spectrum) is improved but modulation quality is reduced. The closer we get to 300KHz, ORFS is affected but Modulation quality is improved.
The way it works is as follows:
As before get a GSMK waveform from the Look up Rom and the Serial Data
This waveform will then be input to a 9-bit D/A, which will output an analogue format that follows the waveform
In effect this output is added to the signal from the **TX_CP** output within the loop filter and restores the high frequency components that have been attenuated in the PLL process of **TX_CP**. (See Diagram Below)
This of course improves the purity of the output burst.
The charge pump drive signal **TX_CP** from U800 **Pin B1** is now forwarded to the Loop filter consisting of C154-C156 / R154 / R155.
The loop filter is designed as an active device that reacts to changes in output frequency of the Neptune modulated charge pump and in addition to performing the 'smoothing' function to stop any discrepancies in CP voltage being fed to the TX VCO, it also adds the high frequency modulation components from the dual port modulation output.



Drawing 1.8 Dual Port Modulation

TX VCO (in Algae U150)
The TX VCO has two outputs. The first is used as feedback signal passing the divide by 4 circuit in the Synthesyer Feedback module. As balaced output signals **SYNTH_FB_P** and **SYNTH_FB_N** of this module the signalsare then feeded to the synthesyzer close the loop-circuit. The 2nd output is the low power transmitter signal and will be multiplied by 2or 4 depending of the selected frequency band.
The selected output then will be amplified and leaves as **TX_OUT_LO** and **TX_OUT_HI** the Algae IC U150 at **Pin 38 and 39**.

TX PA (in Athena U300)
The Pins 37 and 39 are input for the signal **TX_OUT_LO** and **TX_OUT_HI** at U300.
The signal **TX_OUT_LO** is passing the TX Clean-up Filter Fl300 before.
Each signal will be amplified by an independent 3 stage PA circuit. The Circuit will be contr. by by the PA Control circuit from Neptune. Output of the PA Circuit will be the full ampilfied and modulated transmitter signal. The signals then are passing as **RF_OUT_DCS** and **RF_OUT GSM** the internal power detection filter followed by Low Pass filter into the Antenna Switch for Band selection. Now the signals are ready to be transmitted on the selected Antenna.

TX PA Power Control (in Athena U300)
Starting at the output of the PA amplifier the power will be detectet by the Rf detectors. The signal is the feeded into the Matching and Combiner Network. The output of this circuit will feed into the PAC II IC. The PAC is supported by the 2.775 V RF_REG output of U900.
The PAC outputs, **PA_REF** and **PA_DET**, are input to a comparator in Neptune. **PA_REF** is typically at 60 mV and **PA_DET** (if no RF is applied) is typically at 50 mV. As the RF signal is increased, the **PA_DET** voltage increases. Once the **PA_DET** voltage becomes greater than 60mV (>10mV rise), the analog activity detector in the PA control of the Neptune is tripped. If the analog activity detector is selected, the analogue comparator output signal **AOC_DRIVE** **Pin B9** of the PA Control is used to close the loop. This signal drives the PA Bias Circuit that controls the 3 stage PA.

General Interfaces:

Display
The display is driven from the Neptune SPI Display Interface. The display driver is part of the display module that is connected in use of an elastomer to the main PCB.
Comunication signal are:
LCD_CS - **C**hip **S**elect for LCD driver
LCD_RS - **R**egister **S**elect indicates if display data or controldatas are written
LCD_CLK - Serial **CL**oc**K** output to LCD driver
SDATA_LCD_DATA - **S**erial **DATA** output from Neptune Display SPI interface
RESETB - active low RESET
The display is supported by **IO_2,65V**.

Kepad and Display Backlight
Four LED´s are the backlight for the Kepad and Display. The Led driver IC is U400 that is supported by **B+** at **Pin 3**. The **LED _CNTRL** signal from U800 is controling the enable/disable function of the IC.

SIM

The Neptune Sim Interface takes direct control of the SIM card.
The SIM Connector is supported by **SIM_VCC** and **IO2,65V** at **Pin 4 and 1.**
The Presence detect switch works as follows:
The SIM PD switch is part of the Sim connector J800. If the SIM door is open the **SIM_PD** line will be pulled to high by **IO2,65V**. If the Sim door is closed and locked the SIM_PD line is open on Low level.

SIM control signals are as follows:
SIM_DIO - **D**ata **I**n and **O**utput from and to SIM Card / Interface
SIM_RST - active low **R**e**S**e**T** signal from SIM interface
SIM_CLK - output **CL**oc**K** from Sim Card Interface to SIM Card

Combined Memory (Flash & SRAM)

The C37x / C450 Series are using internal Neptune Memory for the DSP and MCU.
U701 is used as external combined 16Mbyte flash and 4MByte SRAM memory.
The flash part contains space for Phone Software and for the EEProm function like IMEI Number, Customer Phone numbers, Phasing datas a.s.o.
It is split up in 2 hardware partitions
U701 is supported by **DIG_1,875V**.
Control / Comunication signals are:
BURSTCLK- **BURST CL**oc**K** is to syncronize the loading of addresses and delivery of burst read data
R_WB – active low **R**ead **W**rite indication signal to Flash and SRAM
LBAB - **L**oad **B**urst **A**ddress **A**ctive low- causing that the Flash is loading a new starting burst Address
CS0B - **C**hip **S**elect **0** - active low (**B**) output is used as external Flash memory partition 1 select
CS2B - **C**hip **S**elect **2** - active low (**B**) output is used as external Flash memory partition 2 select
OEB - **O**utput **E**nable-active low (**B**)- is indicating that the bus access is a read and enables slave devicesto drive the bus with read data.
RESETB - Active low (**B**) **R**esest
ECBB - **E**nd Off **C**urret **B**urst-active low (**B**)- to indicate to FLASH the end of current burst sequence.
ADDRESS 0-21 – Address lines
Data 0-15 – Data lines

The SRAM part is supported by **VCCQ** that is sourced **by DIG_1,875**.
Control / Comunication signals are:
EB1_B - Used as write **E**nable to partition of SRAM
EB0_B - Used as write **E**nable to partition of SRAM
CS1B - **C**hip **S**elect **1** - active low (**B**) output is used as external SRAM memory chip select
R_WB – active low **R**ead **W**rite indication signal to Flash and SRAM
OEB - **O**utput **E**nable-active low (**B**)- is indicating that the bus access is a read and enables slave devicesto drive the bus with read data.
ADDRESS 0-21 – Address lines
Data 0-15 – Data lines

32KHz RTC

The Realtime Clock Interface is part of the Seaweed IC U900. It is supported internal by the "always on" **RTC_GRP** (1,55V).
The clock signal **CLK_32K** is running on 32Khz as reference for the Clock module and as DeepSleep Clock.

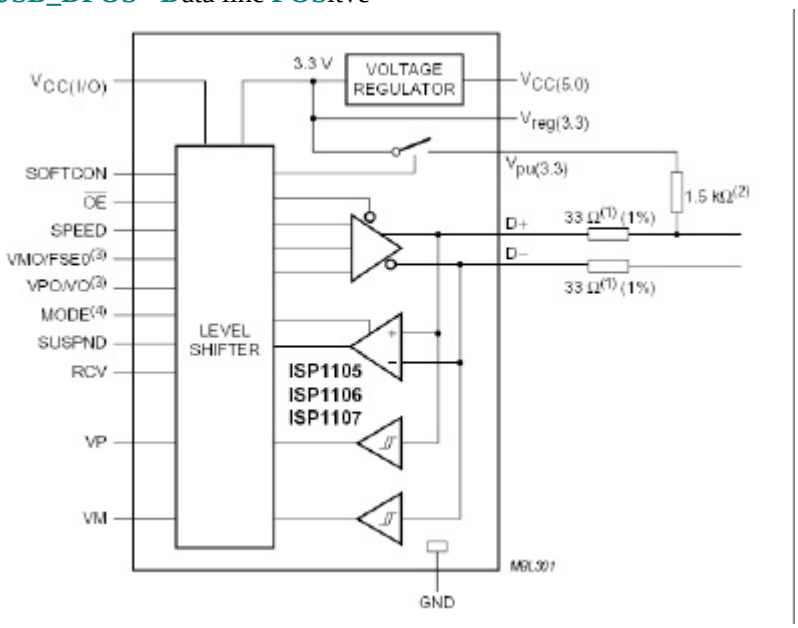
Keypad

SYNERGY FUNCTION	Row / Column ?		R0	R1	R4	R5	R6	R7	C0	C1
	SWITCH	Patriot pin # ?	J2	H4	J3	G8	J1	G9	G4	H8
1	S503		X							X
2	S502		X						X	
3	S520			X						X
4	S501					X			X	
5	S505				X					X
6	S504				X				X	
7	S506		X	X						
8	S517			X				X		
9	S511			X			X			
*	S510				X		X			
0	S509			X	X					
#	S515		X					X		
SEND	S514		X				X			
END / Pwr	S513	Signals only								
ARROW RIGHT	S522						X		X	
ARROW LEFT	S523							X		X
ARROW UP	S518						X			X
MENU	S519				X			X		
ARROW DOWN	S516							X	X	
SOFT LEFT (below display)	S508					X		X		
SOFT RIGHT (below display)	S512		X		X					
PPRESET (not in phones with ext. battery)		Signal only								

USB

The main control function is in the USB interface of Neptune IC U800.
This interface uses the external USB IC U600 to communicate via the Mini USBconnector J600 with external perepheries. The external comunication lines at the Mini USB connector J600 are:
USB_ VCC - supply for external USB devices

USB_DNEG - **D**ata line **NEG**ative
USB_DPOS - **D**ata line **POS**itve



Drawing 1.9 USB IC

USB IC Signal Description

Drawing 1.9 shows the USB Interface IC U600.
The IC works as Level Shifter/Buffer circuit.
D+ (**USB_DPOS**) on **PIN 10** described above
D- (**USB_DNEG**) on **PIN 9** described above
VCC (I/O) (**USB_VCC**) on **PIN 14** - described above
VCC (**IO_2,65V**) on Pin 7 - 2,65 Volt supply to U600
Vreg - connection to external Capacitor C602 for internal voltage regulator
Vpu – connection to external pull up resistor for USB Data speed indication
SOFTCON on **PIN 16** - connect / disconnect indication input
OE (**USB_TXENB**) on **PIN 1** - active low input- signals to USB device when to transmit data on USB bus.
SPEED (**USB_DET**) on **Pin 8** Speed Detect input to U600. Adjusts the slew rate of D+ and D-
VMO/FSE0 (**USB_VMOUT**) on **Pin 12** **USB**- (**M**inus) data from U800 to U600
VPO/VO (**USB_VPOUT**) on **Pin 11** **USB**+ (**P**ositive) data from U800 to U600
MODE (**GND**) on **Pin 6** - ground connected
RCV (**USB_XRXD**) on **Pin 2** CMOS logic value of value received from USB wires
VP (**USB_VPIN**) on **Pin 3** **USB**+ (**P**ositive) data from U600 to U800
VM (**USB_VMIN**) on **Pin 4** **USB**- (**MIN**us) data from U600 to U800
SUSPND (**USB _SUSPEND**) on **Pin 5** active high - indicates to U800 that the USB device is **SUSPEND**ed, enters low power state in Neptune USB module

Temperature

To compensate the temperture problems the RT900 is sensing the PCB temperature.
The signal **PC12** is biasing the **TEMP** line into the A/D converter of U900.
Also the **PC12** signal sets the with its high level the battery type at **Pin 28** at U920.

Camera Module (for C550 only)

The Camera module is connected over a spring connector with the PCB.
The sensor support a resolution of 640x480 dots.
The Camera module contains a CPU, a clock circuit and GPIO. The module is supported by **B+**. Communication is provided via the Neptune SPI Bus lines **MOSIA, MISOA** and **SPI_CLK** as clock. The clock output **CKO** from Neptune is triggering the system clock of the internal camera CPU. The active low **SPI_CS0** from Neptune enable communication on the Neptune SPI Bus. **TOUT8** is the Interrupt request signal. It is high when the IC is requesting the next datas. **INTO** is a interrupt signal from the camera to the Neptune.