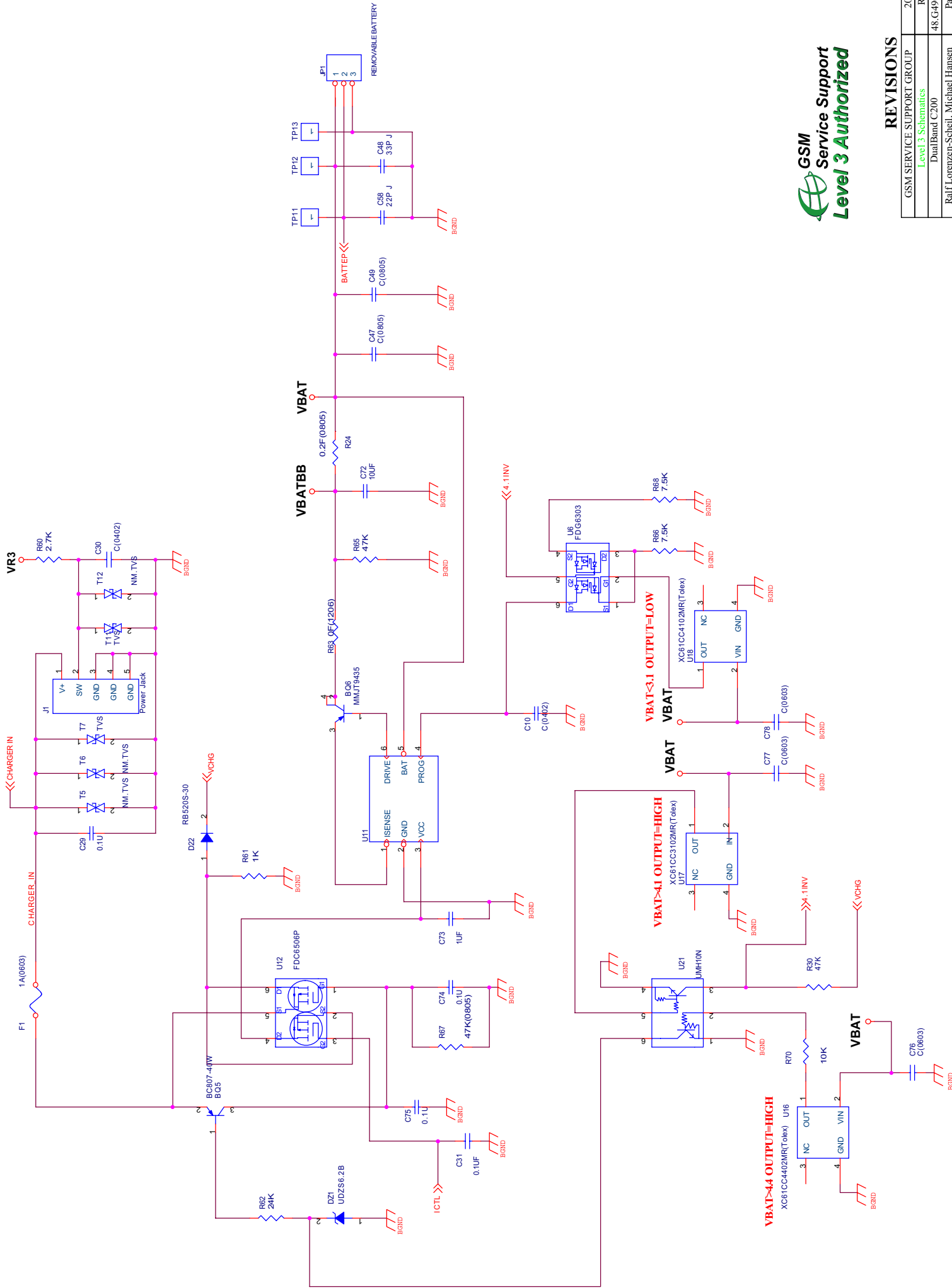


VR1 (1.8V) ==> VDD, VDDARM, VDDLMM
 VR2 (2.9V) ==> VDD51
 VR2B (2.9V) ==> VDD52
 VR3 (2.9V) ==> VDDA1



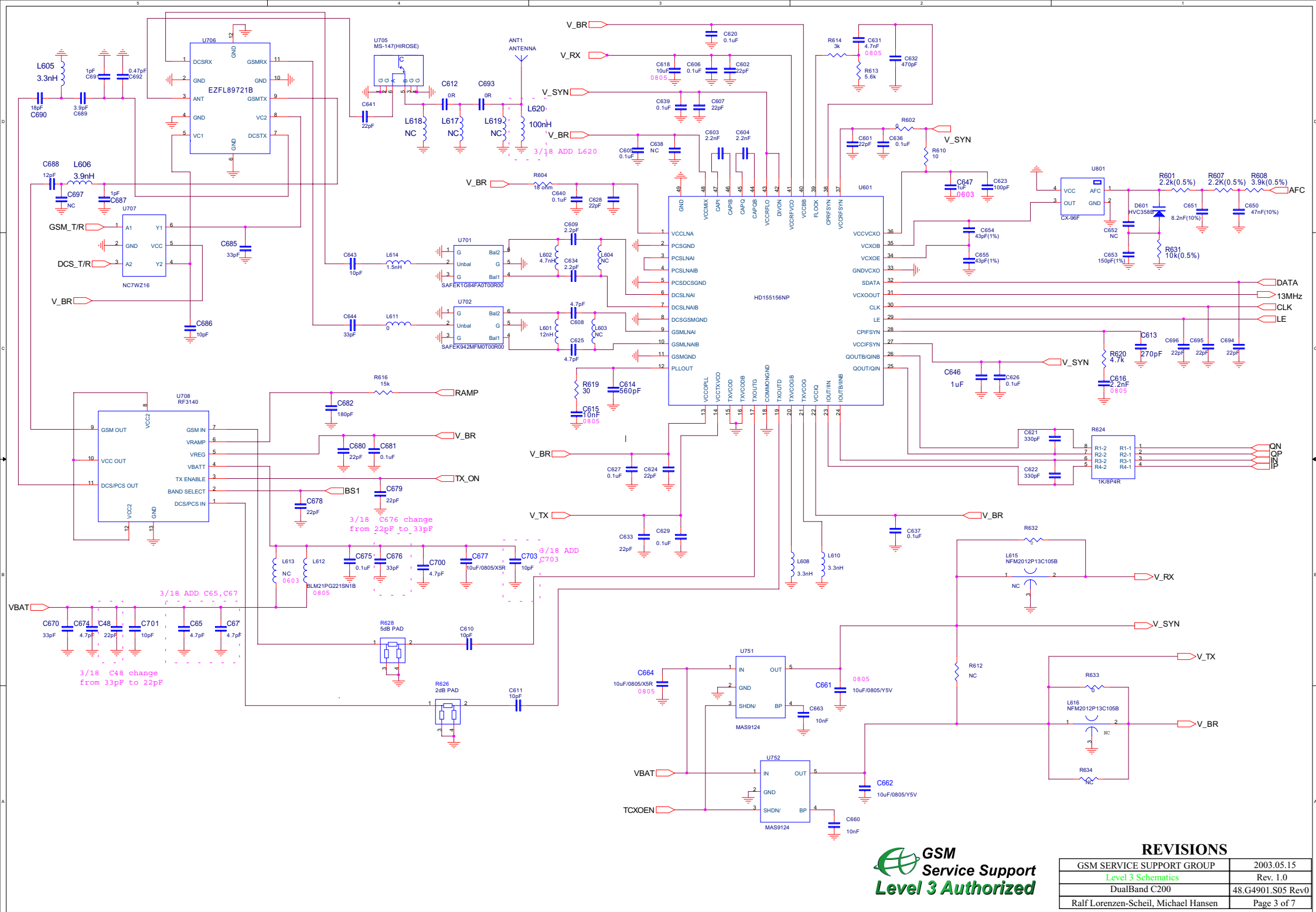
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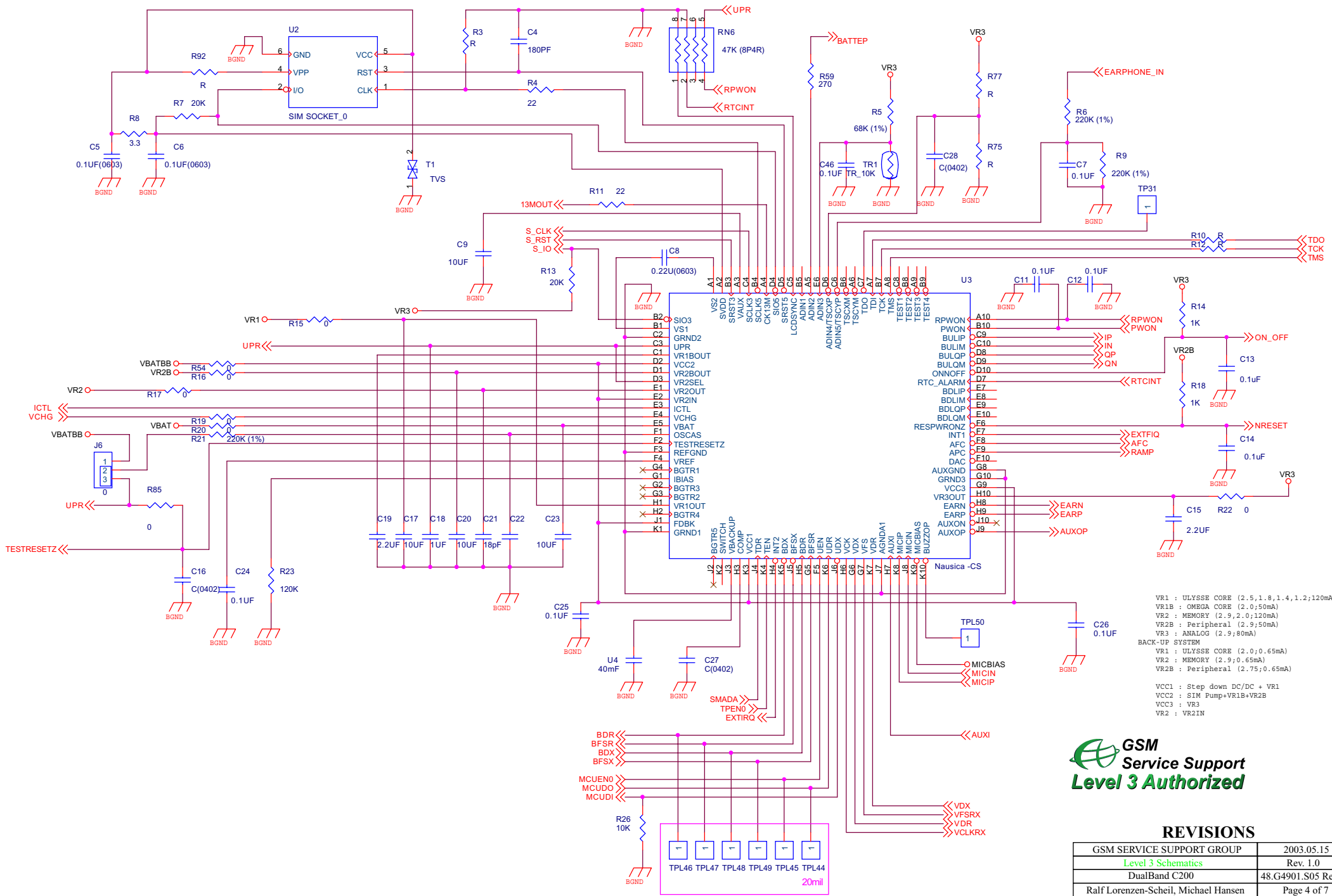
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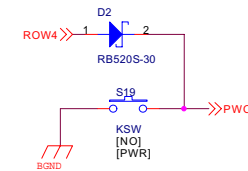
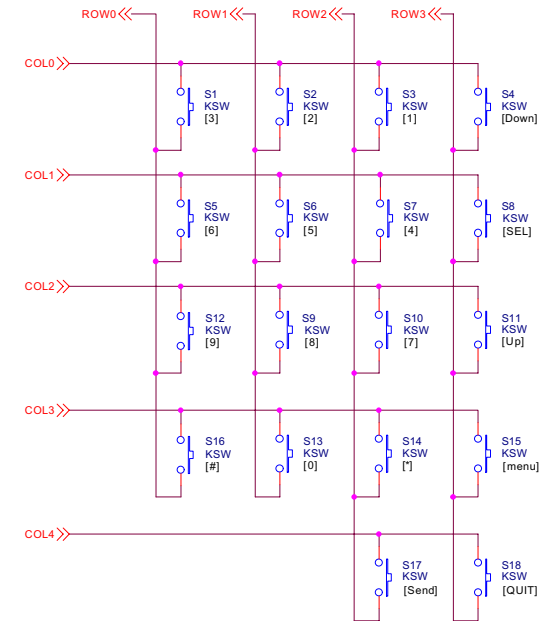
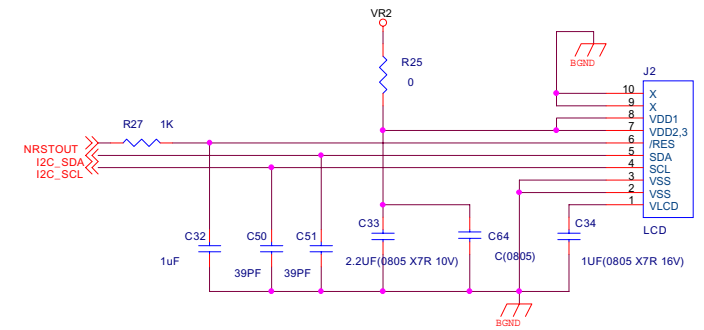
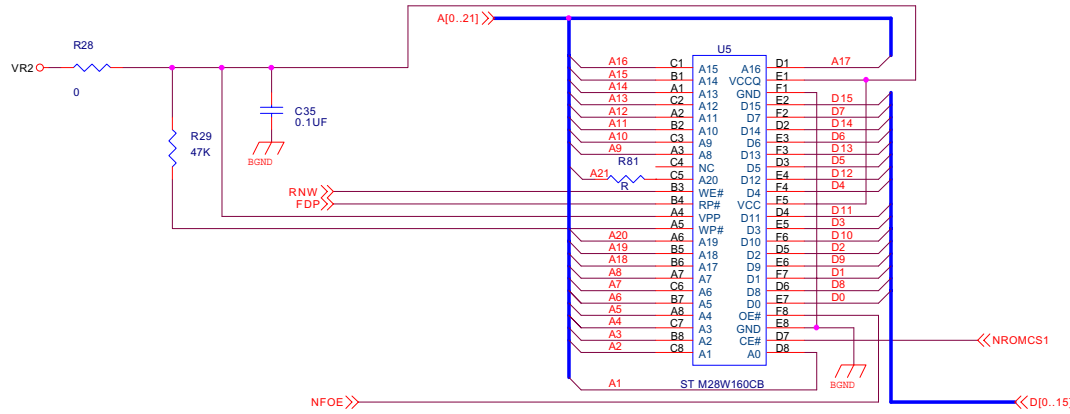


- VR1 : ULYSSE CORE (2.5,1.8,1.4,1.2;120mA)
 - VR1B : OMEGA CORE (2.0;50mA)
 - VR2 : MEMORY (2.9,2.0;120mA)
 - VR2B : Peripheral (2.9;50mA)
 - VR3 : ANALOG (2.9;80mA)
- BACK-UP SYSTEM
- VR1 : ULYSSE CORE (2.0;0.65mA)
 - VR2 : MEMORY (2.9;0.65mA)
 - VR2B : Peripheral (2.75;0.65mA)
- VCC1 : Step down DC/DC + VR1
 - VCC2 : SIM Pump+VR1B+VR2B
 - VCC3 : VR3
 - VR2 : VR2IN



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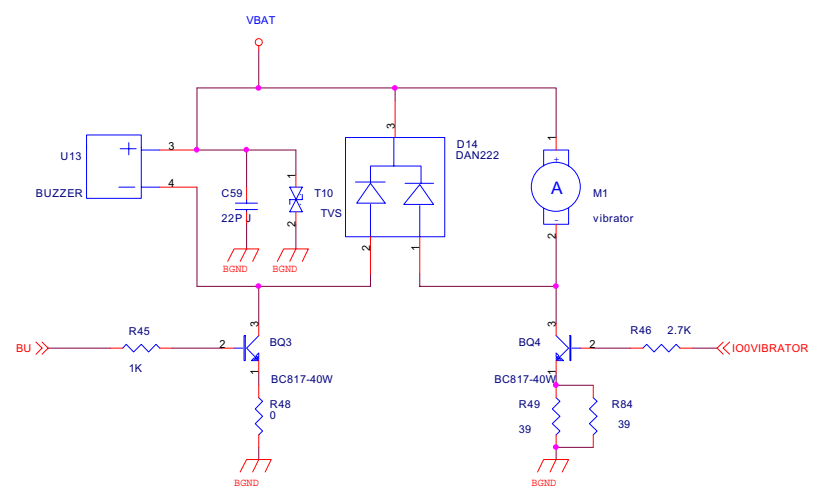
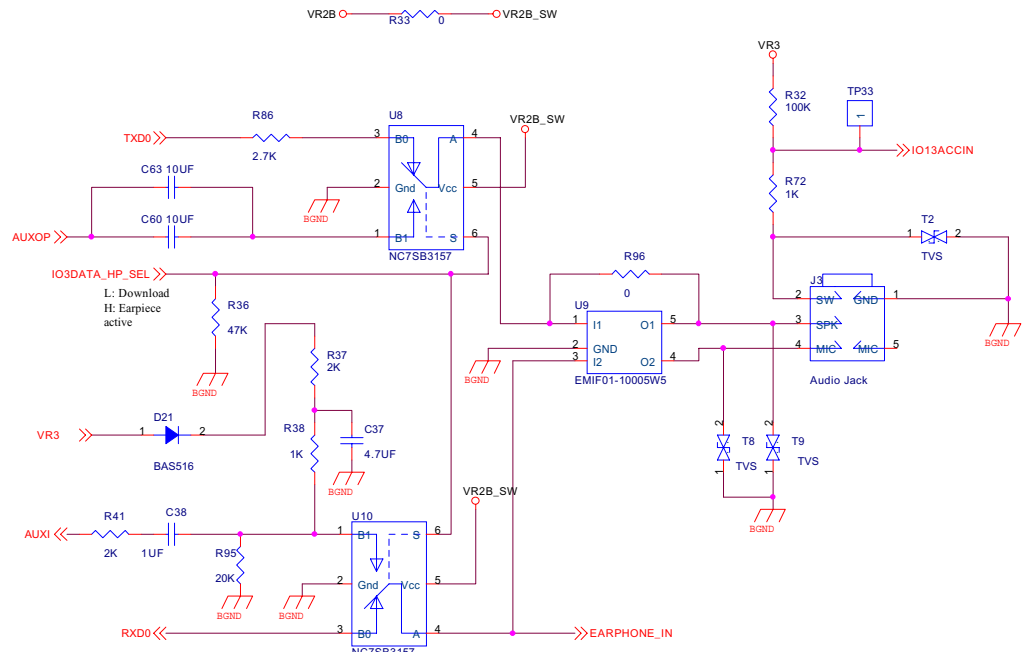
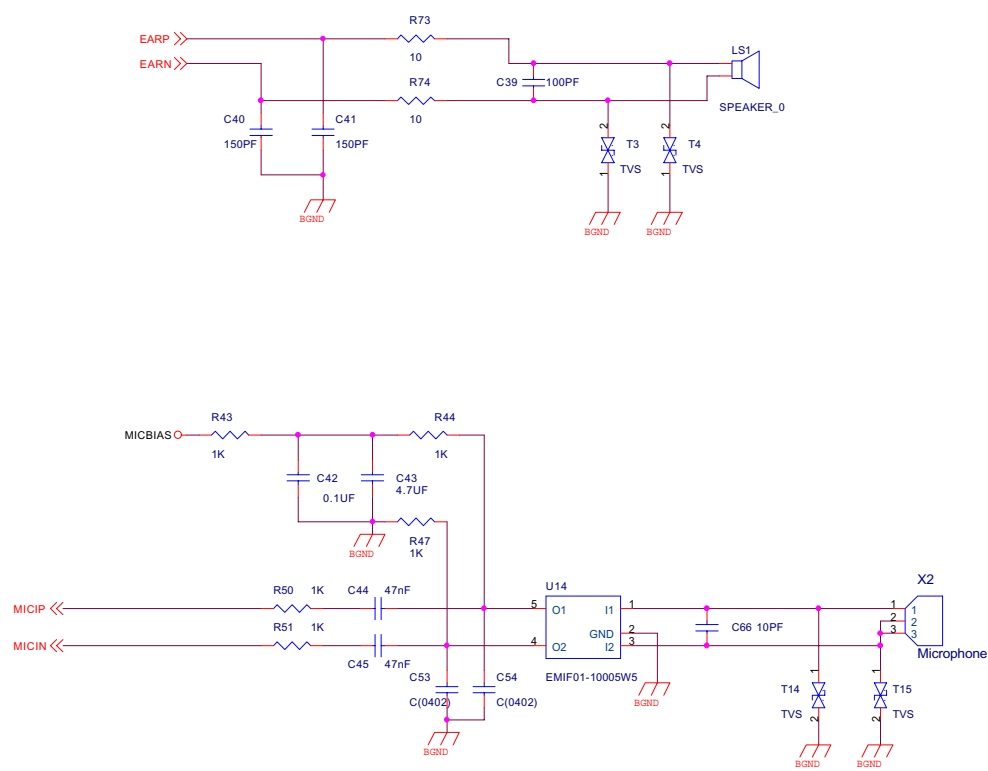
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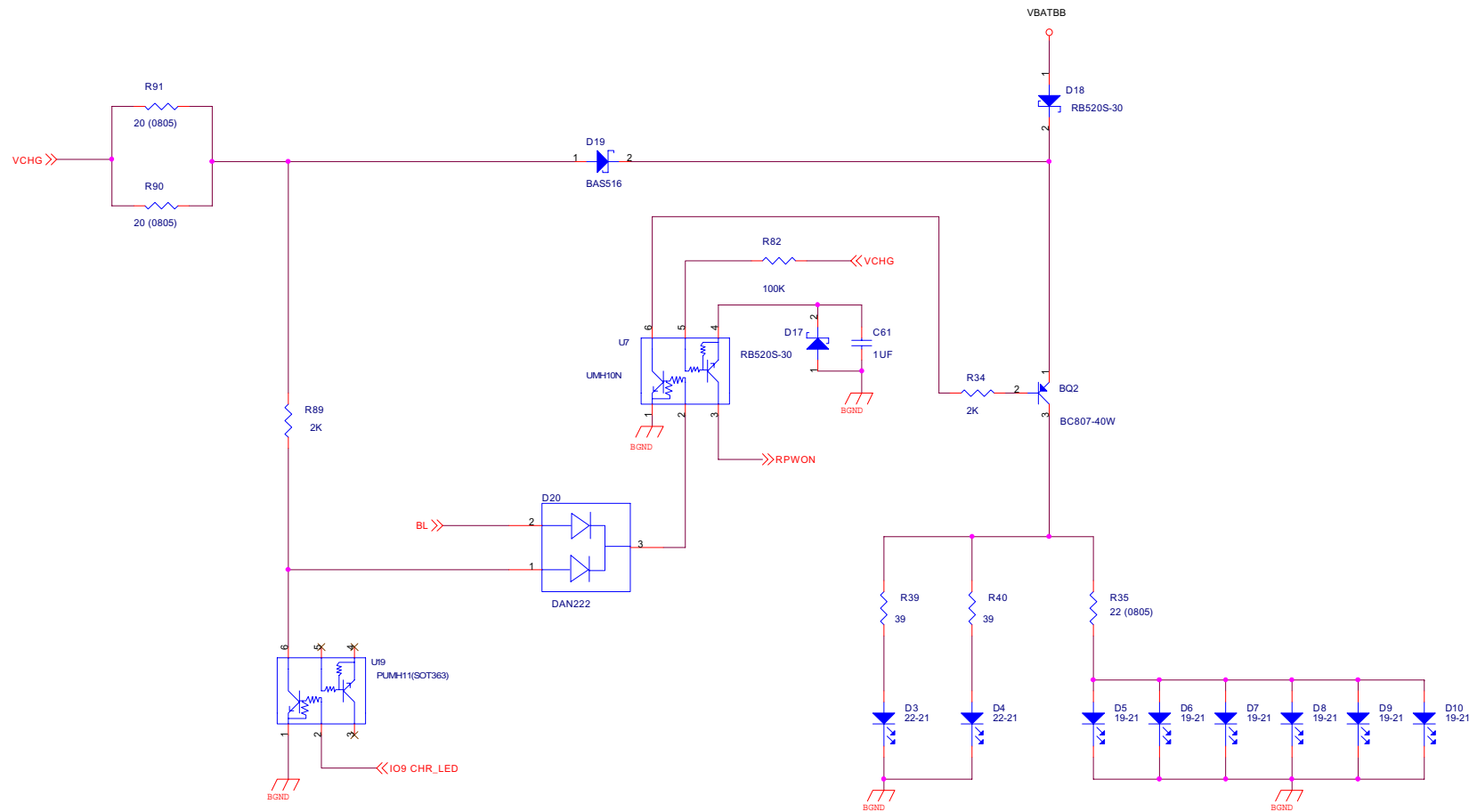
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