Motorola ™ Milestone

Theory of Operation

Rev. 1.0

Repair Optimization Service Training
Level 3 Authorized

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1 Introduction

The Motorola Milestone mobile device is an Android device with full qwerty keypad in a convenient slider design. The MILESTONE boasts a full suite of mobile technologies that includes Quand band GSM and EDGE, WCDMA, Bluetooth, WiFi & GPS. It also has a 5.0 mega pixel camera, and a vivid 3.7", 854x480 touch sensitive display. The phone also contains a Secure Data (SD) removable memory expansion slot.

The Motorola MILESTONE mobile phone is designed to the horizontal slider form factor. The design consists of a main housing assembly that contains the battery, battery cover, accessory connector, main circuit board, chassis, qwerty keypad, primary microphone, and internal antenna. The slider section slides sideways to reveal the qwerty keypad. The slider assembly houses the main display, touch screen IC, ear piece, Home key, Back key, Menu Key & Search key. The MILESTONE also changes screen orientation when the slider is opened or closed to enhance viewing of some applications & also has the Accelerometer to determine the orientation of the device. The 5.0 mega pixel camera is located on the back of the phone.

The Motorola MILESTONE phone consists of a main housing assembly that contains the battery, battery cover, accessory connector, main circuit board, chassis, keypad, and internal antenna. The camera, battery compartment, and rf connectors are located at the rear of the device. The main circuit board contains the Receiver, Transmitter, Synthesizer and Control Logic Circuitry which together comprise the phone electronics.

1.1 Key Features

- Qwerty keypad
- Application specific lighting effects
- 854 x 480, 3.7" WVGA Touch Display
- 5.0 Mega Pixel Fixed Focus Camera
- MOD, VOD, LBS Capable
- Integrated Speakerphone
- TI OMAP3430
- Infineon transceiver
  - Smarti UED
- Removable memory
  - MicroSD up to 32 GB
- Messaging – 2–Way (MO/MT) SMS, EMS, MMS
- Browser
- GPS
- Bluetooth V2.1 + EDR Class 1 including A2DP for MOD
- WLAN b/g
- Accelerometer for Landscape / Portrait orientation
- Magnetometer for e-compass
- Proximity Sensor

1.2 Operating Frequencies

1.2.1 Europe, Middle East, and Asia Variant

	TX				RX		
Frequency (MHz)	**Low**	**Mid**	**High**	**Frequency (MHz)**	**Low**	**Mid**	**High**
CEL850	824.2	836.6	848.8	**CEL850**	869.2	881.6	893.8
GSM900	880.2	897.6	914.8	**GSM900**	925.2	942.6	959.8
DCS1800	1710.2	1747.6	1784.8	**DCS1800**	1805.2	1842.6	1879.8
PCS1900	1850.2	1880	1909.8	**PCS1900**	1930.2	1960	1989.8
Band1 (W2100)	1922.4	1950.0	1977.6	**Band1 (W2100)**	2112.4	2140.0	2167.6
Band8 (W900)	882.4	897.6	912.6	**Band8 (W900)**	927.4	942.6	957.6
Channel (TX)	**Low**	**Mid**	**High**	**Channel (RX)**	**Low**	**Mid**	**High**
CEL850	128	190	251	**CEL850**	128	190	251
GSM900	975	38	124	**GSM900**	975	38	124
DCS1800	512	699	885	**DCS1800**	512	699	885
PCS1900	512	661	810	**PCS1900**	512	661	810
Band1 (W2100)	9612	9750	9888	**Band1 (W2100)**	10562	10700	10838
Band8 (W900)	2712	2788	2863	**Band8 (W900)**	2937	3013	3088

- GSM (2G) / EDGE (2.5G) modes
- WCDMA (3G) modes

Table 1. EMEA Variant Supported Frequencies and Modes

1.2.2 Latin America Variant

	TX				RX		
Frequency (MHz)	**Low**	**Mid**	**High**	**Frequency (MHz)**	**Low**	**Mid**	**High**
CEL850	824.2	836.6	848.8	**CEL850**	869.2	881.6	893.8
GSM900	880.2	897.6	914.8	**GSM900**	925.2	942.6	959.8
DCS1800	1710.2	1747.6	1784.8	**DCS1800**	1805.2	1842.6	1879.8
PCS1900	1850.2	1880	1909.8	**PCS1900**	1930.2	1960	1989.8
Band1 (W2100)	1922.4	1950.0	1977.6	**Band1 (W2100)**	2112.4	2140.0	2167.6
Band2 (W1900)	1852.4	1880.0	1907.6	**Band2 (W1900)**	1932.4	1960.0	1987.6
Band5 (W850)	826.4	836.6	846.6	**Band5 (W850)**	871.4	881.6	891.6
Channel (TX)	**Low**	**Mid**	**High**	**Channel (RX)**	**Low**	**Mid**	**High**
CEL850	128	190	251	**CEL850**	128	190	251
GSM900	975	38	124	**GSM900**	975	38	124
DCS1800	512	699	885	**DCS1800**	512	699	885
PCS1900	512	661	810	**PCS1900**	512	661	810
Band1 (W2100)	9612	9750	9888	**Band1 (W2100)**	10562	10700	10838
Band2 (W1900)	9262	9400	9538	**Band2 (W1900)**	9662	9800	9938
Band5 (W850)	4132	4183	4233	**Band5 (W850)**	4357	4408	4458

- GSM (2G) / EDGE (2.5G) modes
- WCDMA (3G) modes

Table 2. Lat Am Variant Supported Frequencies and Modes

1.3 Product Pictures

Figure 1. MILESTONE Form Factor

2 RF Overview

The Milestone UMTS RF architecture is based upon the Cedarpoint 1.0 two-sided virtual module. The major components are:

- Infineon Smarti UEMD Transceiver
- Pollux GSM/EDGE amplifier and SP8T antenna switch
- Castor WCDMA amplifier(s) and duplexer combination
- Tri-band low noise amplifier
- Penta-band filter module
- Tri-band diversity filter module

Because the CP1.0 platform was designed to be very flexible in banding configurations, there are several components that are jumpered in/out of circuit in the two Milestone banding variants. Although the reference design includes these options, all components in dark grey are not populated and all dashed lines are not used in Milestone' design.

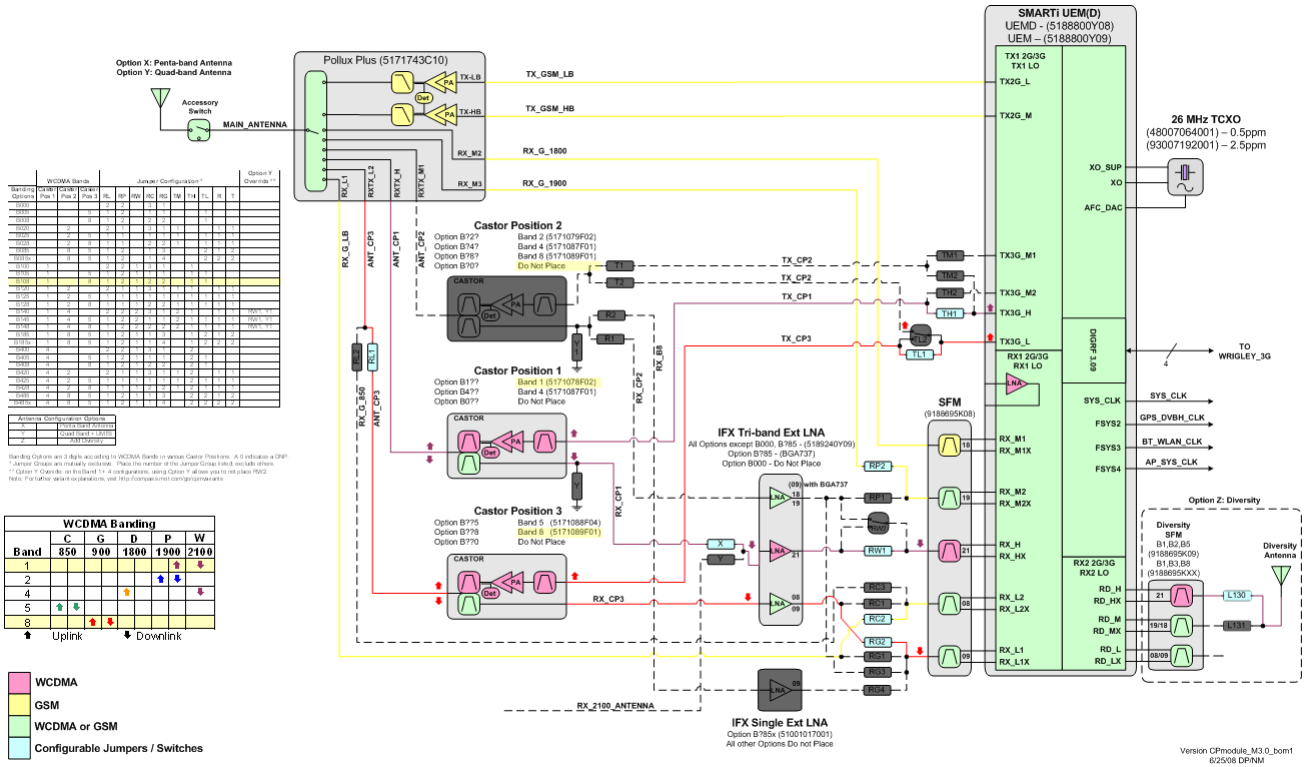

Figure 2. EMEA Variant High level RF function block diagram

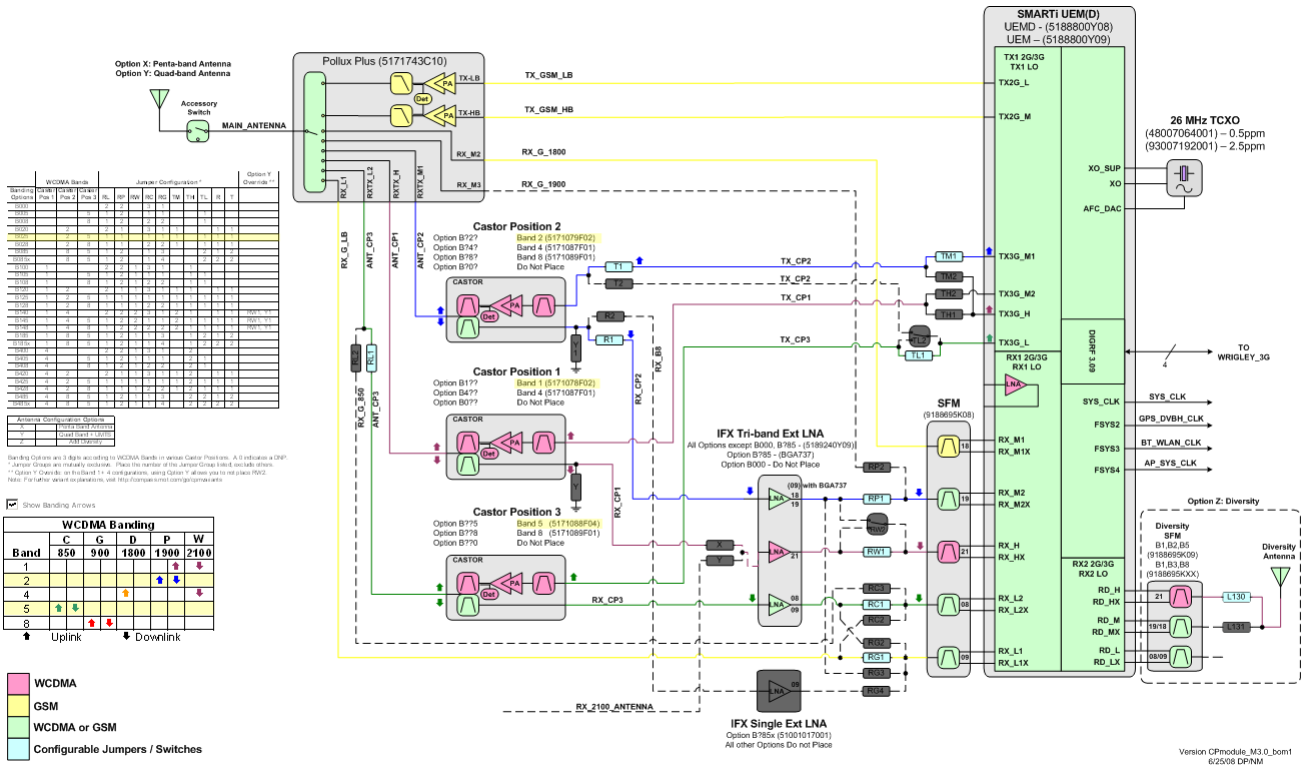

Figure 3. LatAm Variant High level RF function block diagram

2.1 Transceiver (Smarti UEMD)

The RF engine is the Infineon Smarti UEMD transceiver. The chip is a zero-IF design that downconverts received signals directly from RF to baseband and upconverts transmitted signals directly from baseband to RF. Smarti supports GSM, EDGE, and WCDMA signaling.

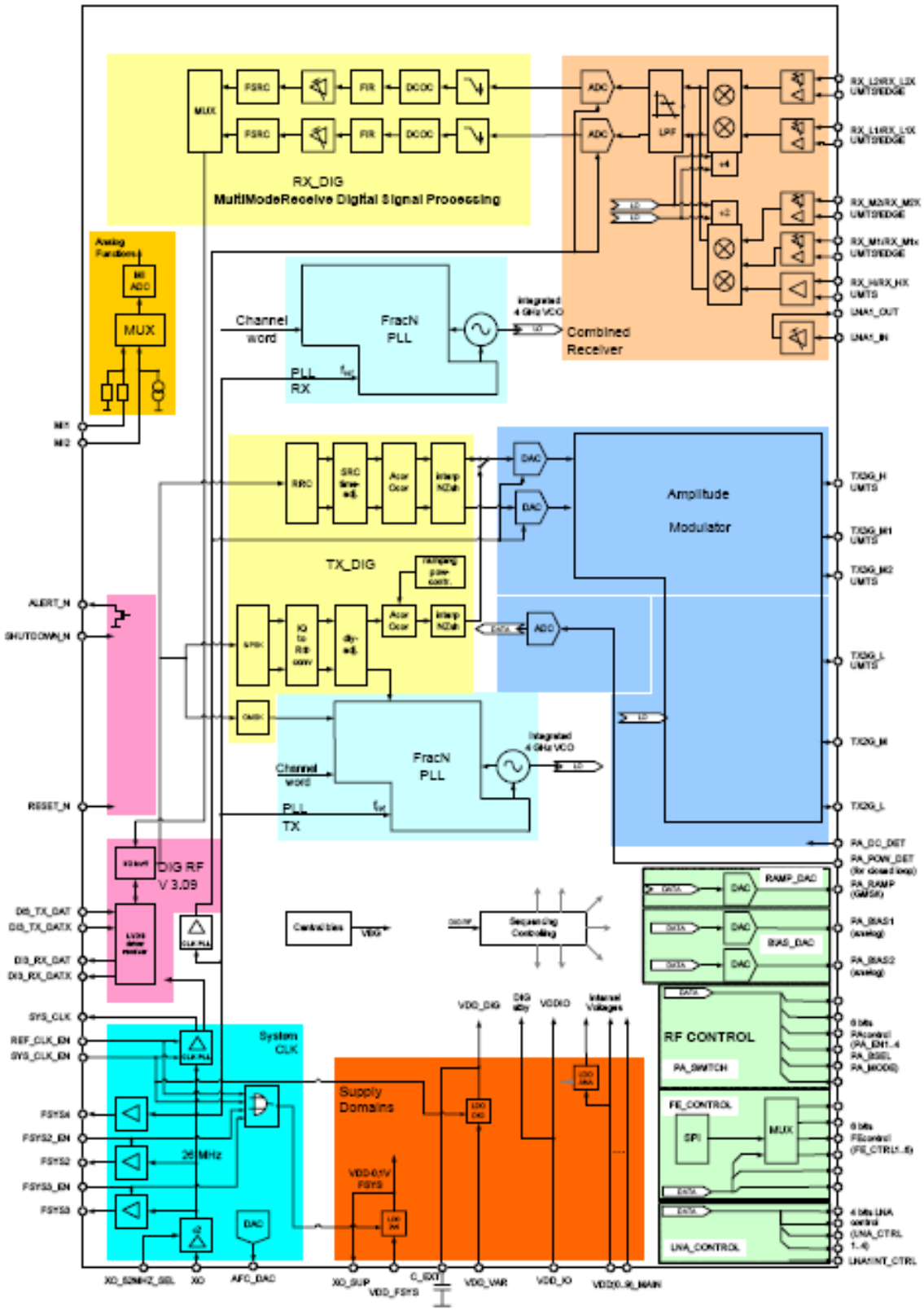

Figure 4. Smarti Transceiver Block Diagram

2.2 Pollux

Pollux is a SPI controlled single-pole 8-throw RF switch packaged together with dual PAs (low band to cover CELL850 & EGSM900, the other to cover DCS1800 & PCS1900).

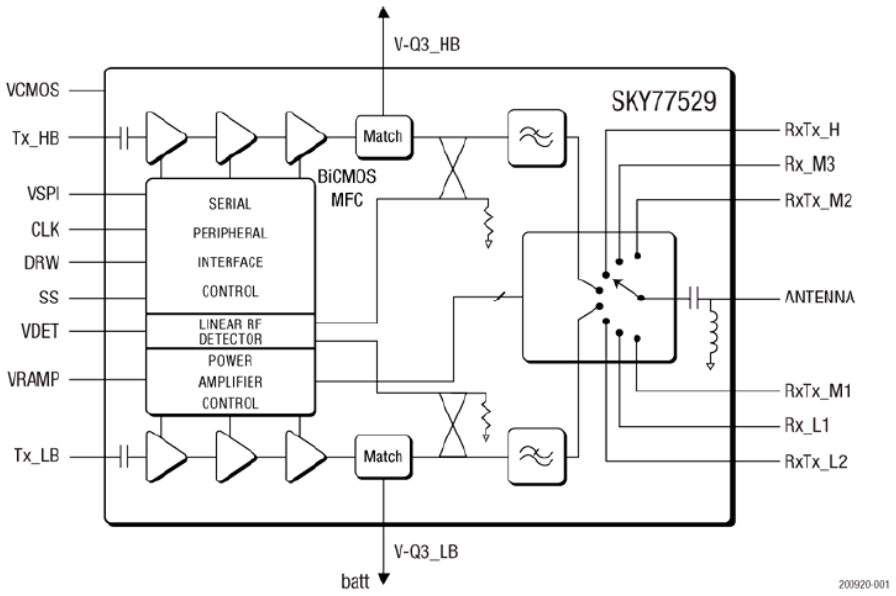

Figure 5. Pollux RF Switch and GSM PA Block Diagram

2.3 Castor

Castor is a DC controlled, 50ohm, single band, single mode, WCDMA power amplifier module that is packaged together with an interstage filter, coupler, power detector, and TX/RX duplexer filter.

A unique Castor module is used to cover each WCDMA band.
U440: W2100 (band 1); U421: W900 (band 8) for Milestone EMEA
U440: W2100 (band 1); U421: W850 (band 5); U401: W1900 (band 2) for Milestone LATAM

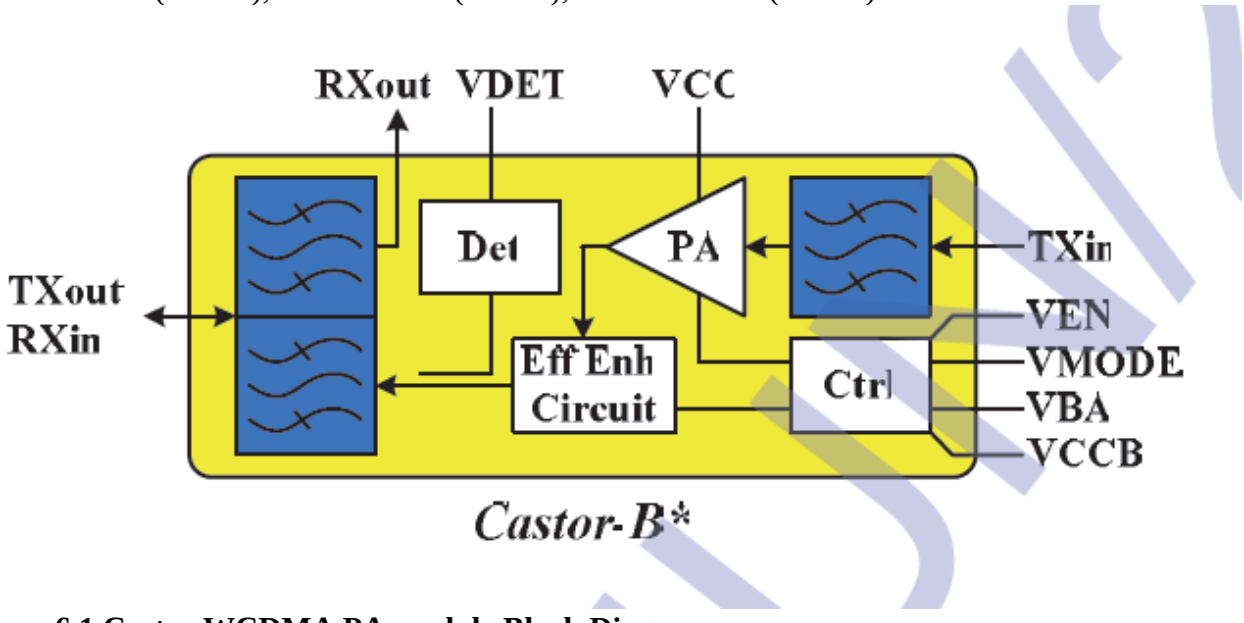

Figure 6.1 Castor WCDMA PA module Block Diagram

DC CONTROL				CONDITIONS
Module State	Ven	Vmode	Vba	
Off	Low	Low	Don't Care	PA is put in low current standby mode
High Power Mode	High	Low	Don't Care	PA will transmit between 10 and 25.2 dBm output power
Low Power Mode	High	High	0.5-1.9V	PA will transmit between -57 and +16 dBm output power. Supplier can choose min and max Vba, but 0.5-1.9V is available.
PA Identification Mode	High	High	0.0-0.3V	PA will output specified identifier voltage on the Vdet output

*Each supplier will be assigned a PA ID voltage that they will use on all bands.

Figure 6.2 Castor WCDMA PA module DC control function table

2.4 Tri-band low noise amplifier

This integrated chip (reference designator U301) is a high linearity tri-band (2140, 1900/2140, 800/900 MHz) low noise amplifier (LNA). External input and output matching networks are needed in order to optimize each LNA for best noise figure and gain while maintaining high linearity. Ven1 and Ven2 are logic signals that allow the selection of a specific LNA. Each of the 3 LNAs has a high gain state and a low gain state and logic signal Vgs controls the selection of the gain states. Figure 6 below shows a block diagram of the tri-band LNA.

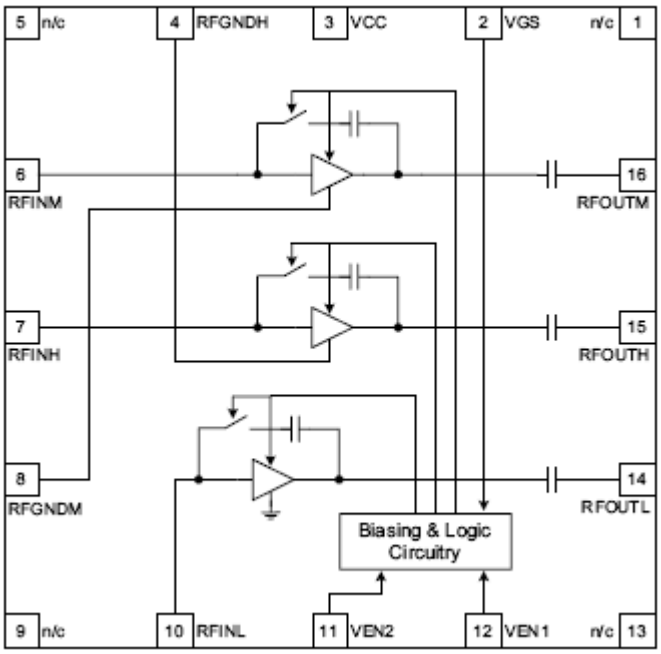

Figure 7. Tri-band low noise amplifier block diagram

2.5 Penta-band filter module

As the name suggests, the penta-band filter module (reference designator FL101) consists of 5 different filters integrated into a single device. The frequencies supported are 850 MHz /900 MHz /1800 MHz /1900 MHz /2140 MHz. Since the input of SMARTI UEMD transceiver is differential, each filter has a single-ended input and differential outputs. Each filter also has an integrated differential output matching network. Figure 7 shows a block diagram of the penta-band filter module.

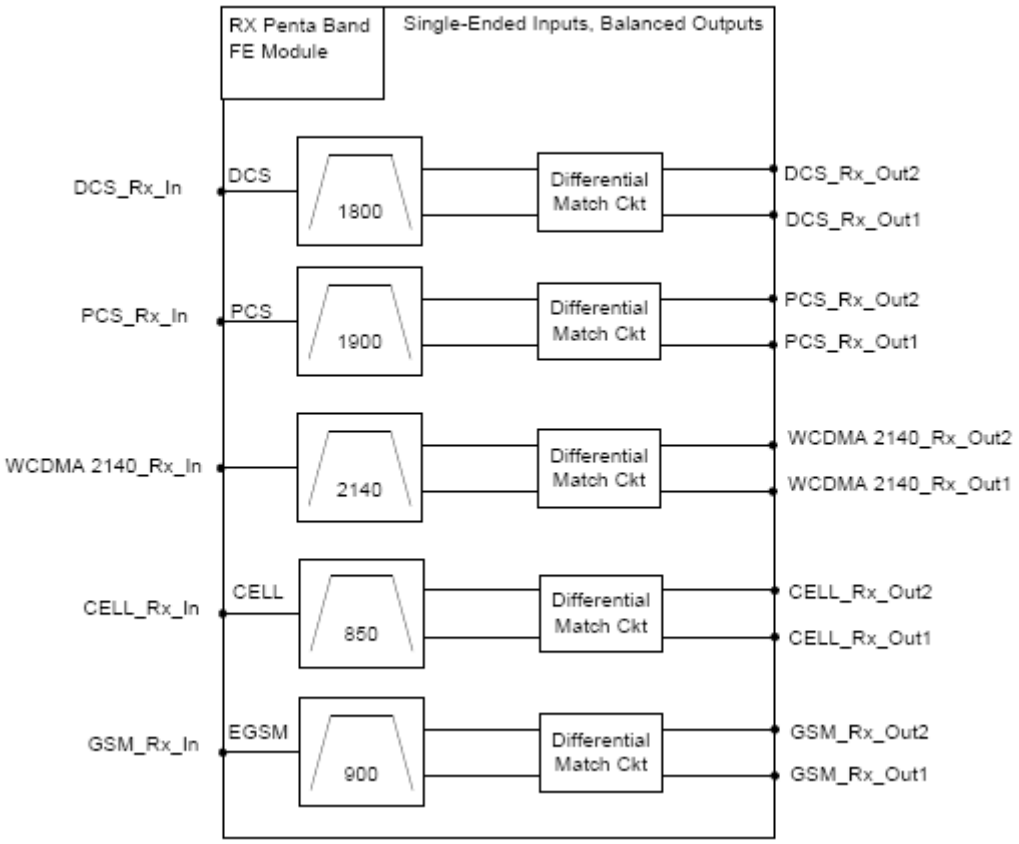

Figure 8. Penta-band filter module block diagram

2.6 Tri-band diversity filter module

The tri-band diversity filter module (reference designator FL130) consists of 3 different filters integrated into a single device. The frequencies supported are 850 MHz /1900 MHz /2140 MHz. Since the input of SMARTI UEMD transceiver is differential, each filter has a single-ended input and differential outputs. Each filter also has an integrated differential output matching network. Currently Milestone UMTS only supports WCDMA band I diversity and hence only the 2140 MHz filter is used whereas the other two filters are left disconnected. Figure 8 shows a block diagram of tri-band diversity filter module.

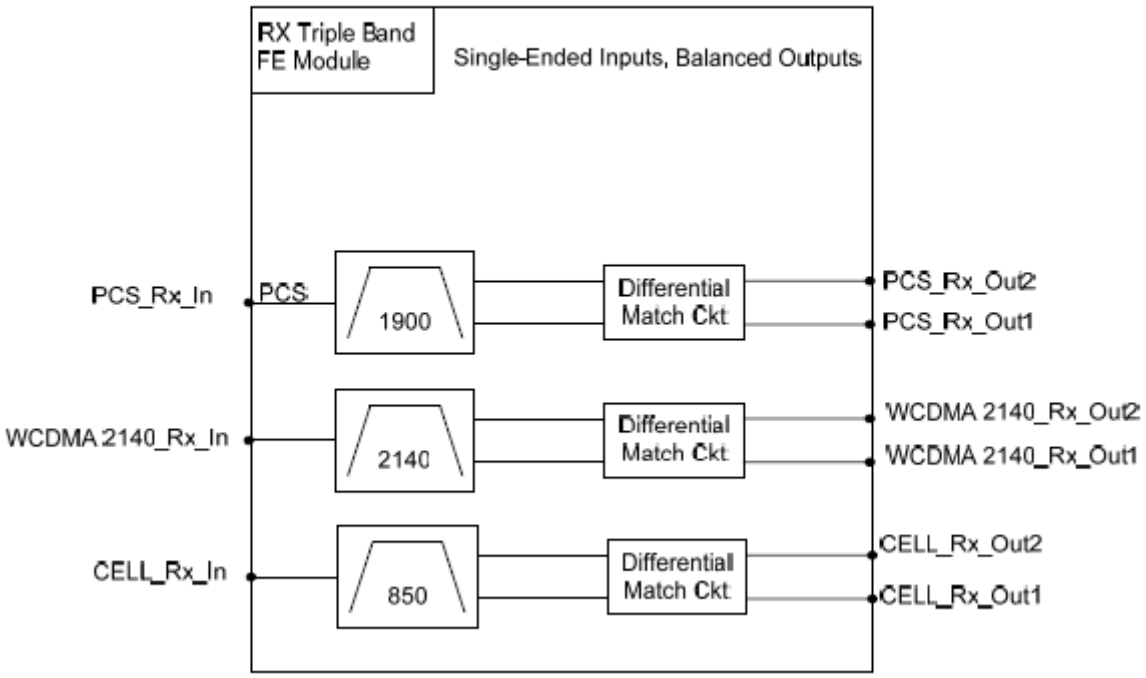

Figure 9. Tri-band diversity filter module block diagram

3.0 Chipset Overview

3.1 TI OMAP 3430

The OMAP 3430 is packed in Hancock3G (U1000) with Wrigley3G modem die.

The OMAP3430 is an applications processor with integrated ARM® Cortex™-A8 superscalar microprocessor core. The ARM Cortex-A8 enables faster user interfaces, faster data access and boosts productivity and entertainment applications on the mobile phone, while maintaining power efficiencies expected in a handset.

With the advanced multimedia capabilities of the OMAP3430 a multi-standard DVD-quality camcorder can be added to a phone. In addition, the ARM's vector floating-point acceleration, coupled with the OMAP3430's dedicated 2D/3D graphics hardware accelerator, provides outstanding gaming capabilities. The OMAP3430 processor embeds Imagination Technologies' POWERVR SGX™ graphics core, and supports OpenGL ES® 2.0 and OpenVG™, providing superior graphics performance and advanced user interface capabilities.

An integrated image signal processor (ISP) allows for image quality enhancement while reducing external components, lowering system costs and lowering system power. The OMAP3430 can connect to images sensors up to 12 mega pixels in size with minimal shot-to-shot delay, enabling camera phones that are equivalent to or better than most digital still cameras on the market today.

The OMAP3430 is designed to support all high-level operating system (HLOS) platforms, including the leading Linux®, Microsoft® Windows Mobile™, and Symbian™ OSes.

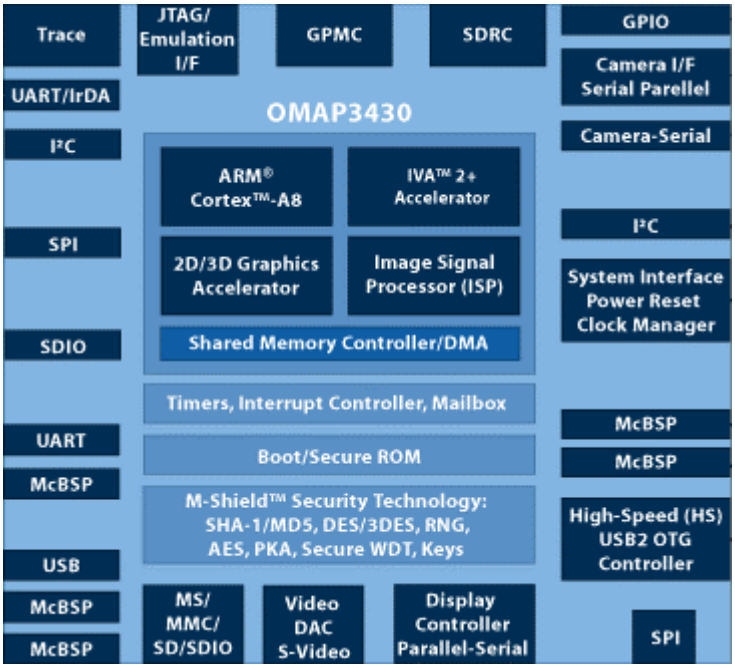

Figure 5. OMAP functional block diagram

The OMAP is connected to the various accessories as shown in the diagram below.

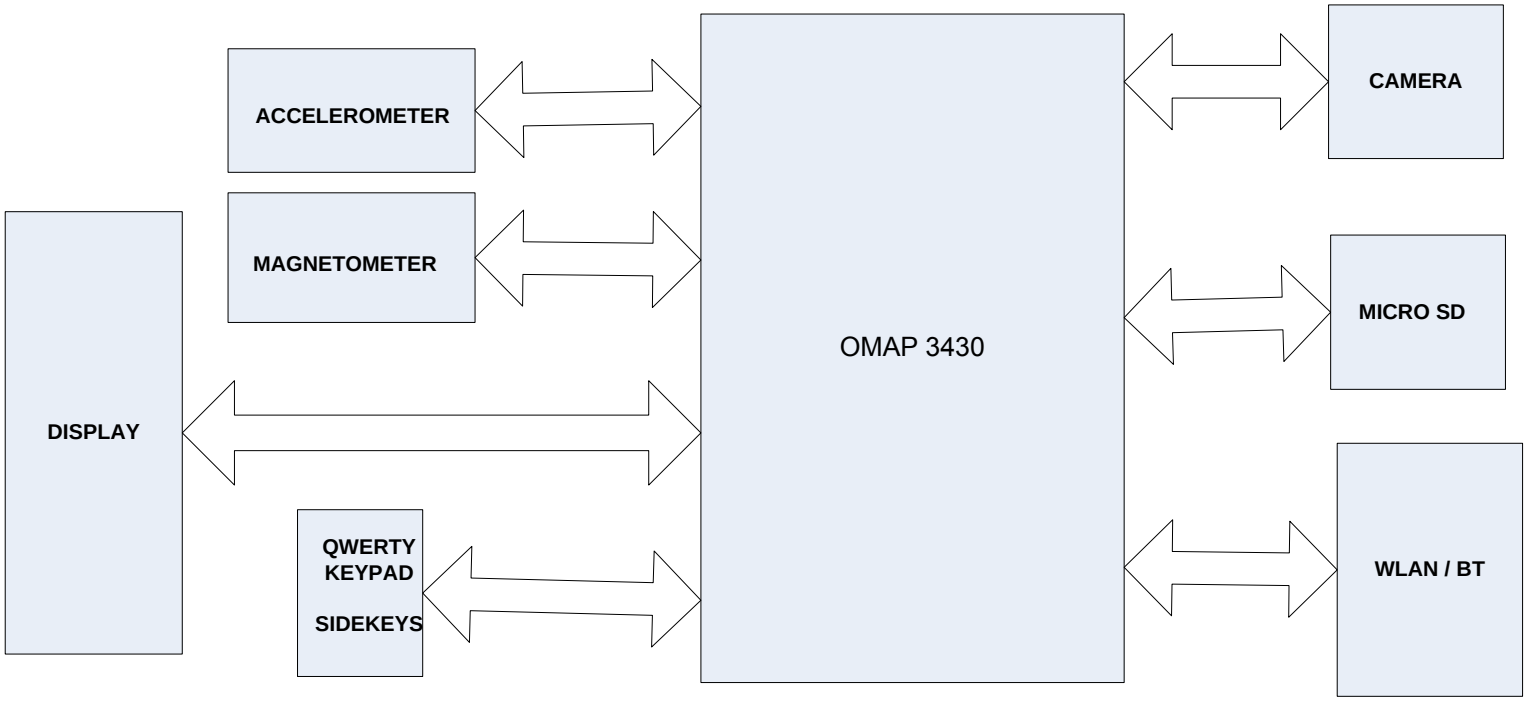

Figure 6. OMAP & Accessories block diagram

3.1.1 High Level OMAP Features

- New OMAP™ 3 architecture combines mobile entertainment with high performance productivity applications
- Industry's first processor with advanced Superscalar ARM® Cortex™-A8 RISC core enabling 3x gain in performance versus ARM11
- Industry's first processor designed in 65-nm CMOS process technology adds processing performance
- IVA™ 2+ (Image Video Audio) accelerator enables multi-standard (MPEG4, WMV9, RealVideo, H263, H264) encode/decode at D1 (720x480 pixels) 30 fps
- Integrated image signal processor (ISP) for faster, higher-quality image capture and lower system cost
- Flexible system support
- Composite and S-video TV output
- XGA (1024x768 pixels), 16M-color (24-bit definition) display support
- Flatlink™ 3G-compliant serial display and parallel display support
- High Speed USB2.0 On-The-Go support
- Seamless connectivity to Hard Disk Drive (HDD) devices for mass storage
- Leverages SmartReflex™ technologies for advanced power reduction
- M-shield™ mobile security enhanced with ARM TrustZone™ support
- Software-compatible with OMAP™ 2 processors
- HLOS support for customizable interface
- Support for OpenGL ES 1.1

3.2 CPCAP

3.2.1 Input Power Management

CPCAP is the main power management IC and it powers both the AP and BP side of the phone. It also handles audio, USB communication and other housekeeping items such as the 32Khz clock. The input power management portion of its block accepts power from common sources – the main battery or an external charger – and generates all the regulated voltages needed to power the appropriate handset electronics. It monitors and controls the power sources, detecting which sources are applied, verifying that they are within acceptable operational limits, and coordinating battery and coin cell recharging while maintaining the handset electronics supply voltages.

3.2.2 Output Voltage Regulators

CPCAP contains four buck-mode switching regulators (SW1, SW2, SW3, and SW4) and two boost switchers (SW5, SW6). The switching regulators will operate from the 32 KHz

internal clock multiplied by an internal 96x PLL (~ 3MHz switching frequency). A number of linear regulators and low-current reference outputs are also incorporated to provide power to specific circuits in the handset. These regulators may take their input from the switch mode supply outputs or directly from BP, depending on the application. Two of the linear regulators (VRF1 and VWLAN2) have an option to use an external pass transistor to support high-current loads without excess heat generation inside the CPCAP device. Most CPCAP regulators have adjustable outputs, and can be enabled or disabled by SPI commands.

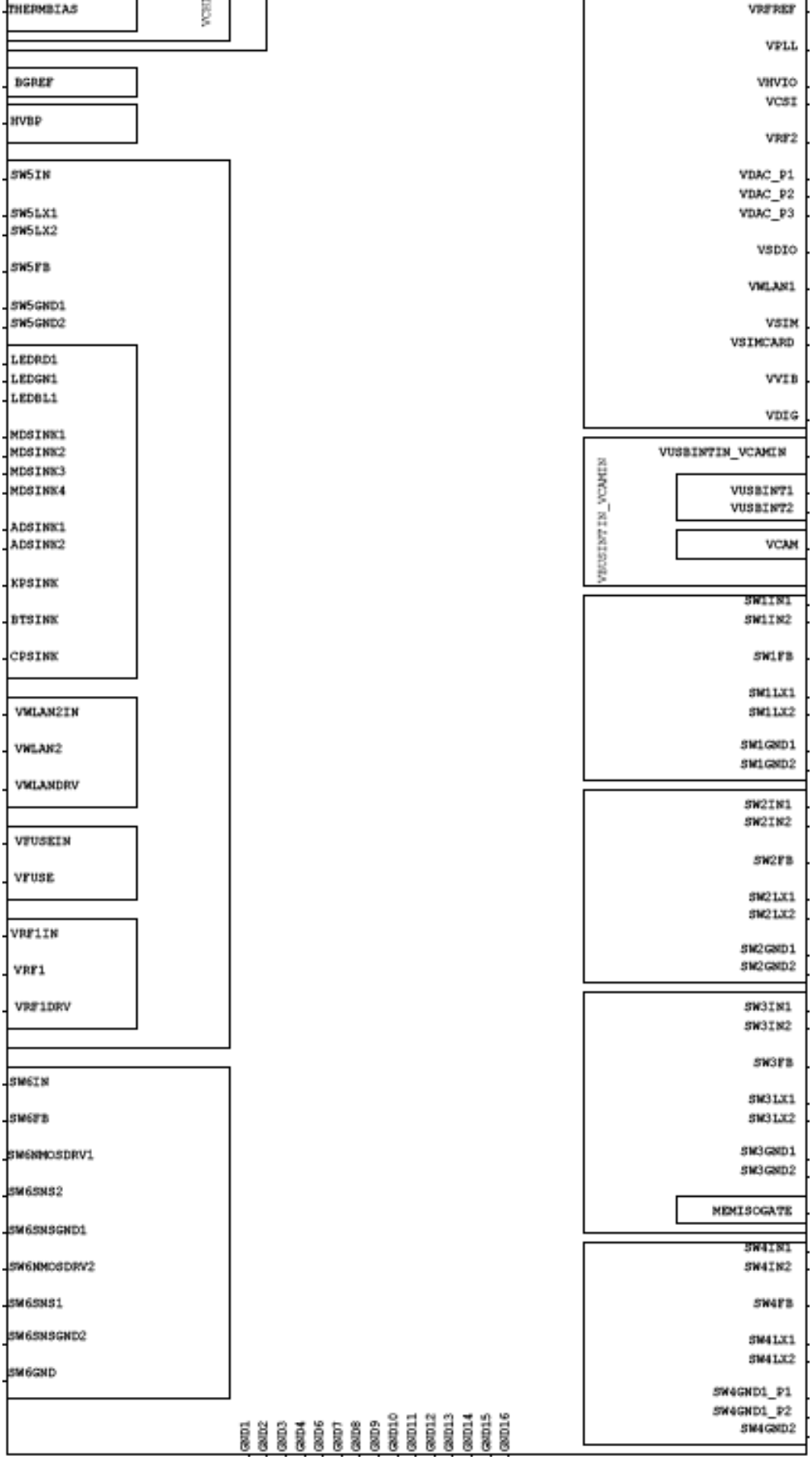

Figure 7. CPCAP functional block diagram

3.2.4 High Level CPCAP Features

- 2 SPI control interfaces with arbitration logic
- 2 SSI buses used to carry audio data. (1 SSI shall have MIPI SLIMbus muxed onto it.)
- 10 bit ADC with 16 input channels including a touch screen interface
- Voice CODEC 16 bit linear dual A/Ds and single channel D/A
- 16 bit linear Stereo DAC
- Various audio amps to interface microphones, headset, handset and 2 Class-D loud speaker amplifiers.
- LiIon Battery charger with 20V tolerant inputs
- 16 low drop out linear regulators for external loads, 2 with capability for external PNP pass devices
- uC with vendor specific sized fast turn ROM to provide for programmable regulator defaults and start-up timing
- 4k bytes of RAM (< 1uA leakage) for uC application code.
- 32.768Khz real time clock system with TOD alarm and stop watch counter
- USB 2.0 HS transceiver including OTG and with 12 pin SDR ULPI
- Support for proprietary EMU and proprietary GCAI bus
- Lighting controller support for keypad, display, auxiliary display, charging sign of life, Bluetooth, RGB, and camera flash
- 4 Buck Switching regulators, 3 with DVS control and integrated FETs
- 1 Boost Switching Regulator for USB and backlights
- 1 Boost Regulator for camera flash with external NMOS
- Coulomb Counter for battery metering
- Very low quiescent current
- 7 General Purpose Inputs/Outputs
- Power Cut support
- Advanced SPI Echo debug interface

3.3 Memory Interface

The OMAP 3430 and Wrigley modem engine share an external NAND/SDRAM memory part (U1051). The memory part is placed on the top of Hancock (U1000, OMAP and Modem) as POP. The size of the Memory is 512MB NAND Flash & 256 SDRAM.

4.0 Charging

4.1 Voltage regulation (VDD or VBAT)

The Charging Regulator in BP mode regulates the voltage at the CHRGISNSN pin on CPCAP to 4.3 +/- 0.1 volts. It is not software selectable. The Charging Regulator in BATTP mode regulates the voltage at the BATTP pin on CPCAP to a programmed setting which defaults to 4.1 volts. The phone's software can change it to a higher voltage, like 4.2 volts. This value is either hard coded or read from the battery EPROM.

Unsafe failure mode is when the Charge Regulator passes current from the Charging Input to BATTP when it is not supposed to or when the regulator does not properly regulate its output current or voltage. Thus failures occur when the CHRGCTRL1 signal is accidentally held low, or a short circuit develops across the M1 FET or the 0.1 ohm resistor, broken pin connections, etc.

The table below describes the voltage programmability in CPCAP IC of the Charge Regulator while in BATTP mode.

Parameter	Value	Battery Regulator Output Voltage (V)
VCHRG[3:0]	0000	3.80
	0001	4.10
	0010	4.15
	0011	4.20
	0100	4.22
	0101	4.24
	0110	4.26
	0111	4.28
	1000	4.30
	1001	4.32
	1010	4.34
	1011	4.36
	1100	4.38
	1101	4.40
	1110	4.42
	1111	4.44

Table 2. Voltage Programmability Table

The voltage that it regulates to (at the CHRGISNSN pin) is selectable. It defaults to 4.1 volts. The software normally will select the 4.20 volt setting based on the value in the battery EPROM. In this case, however, the 4.20 volt setting is hard coded in the phone's software. The 3.80 volt setting is for extended temperature operation
A plurality of settings between 4.20 and 4.44 are provided to allow flexibility in supporting higher voltage Lithium Ion battery packs.

4.2 Current Regulation, Monitoring, and Over-Current Protection

The table below describes the current level programmability in CPCAP IC of the Charge Regulator while in BATTP mode. The current that it regulates to (as sensed by the voltage developed across the 0.1 volt resistor and measured between the CHRGISNSP and CHRGISISN pins is described in this table. With USB, the highest value is 0101. With other chargers, the highest value planned for use is 1101.

ICHRG[3:0]	Minimum	Typical	Maximum
0000	0.0 mA	0.0 mA	0.0 mA
0001	55.0 mA	70.0 mA	85.0 mA
0010	158.4 mA	176.0 mA	193.6 mA
0011	237.6 mA	264.0 mA	290.4 mA
0100	316.8 mA	352.0 mA	387.2 mA
0101	396.0 mA	440.0 mA	484.0 mA
0110	475.2 mA	528.0 mA	580.8 mA
0111	554.4 mA	616.0 mA	677.6 mA
1000	633.6 mA	704.0 mA	774.4 mA
1001	712.8 mA	792.0 mA	871.2 mA
1010	792.0 mA	880.0 mA	968.0 mA
1011	871.2 mA	968.0 mA	1064.8 mA
1100	950.4 mA	1056.0 mA	1161.6 mA
1101	1029.6 mA	1144.0 mA	1258.4 mA
1110	1425.6 mA	1584.0 mA	1742.4 mA
1111	Fully on, meaning no current limiting BATT_FET made to be OFF in Hardware (software controls have no effect)		

Table 3. Current Programmability Table

4.3 Pass-Transistor Power Limiting

The software will regulate the power dissipated across the Charge Regulator during charging. It will:

- Measure the Battery Voltage and Measure the Charger Input Voltage
- Based on the difference voltage and based on the power rating of the devices, as determined by the setting in a factory programmed register (default is 0.7 watts), the software will adjust the maximum current that the regulator can pass.

- Approximately every 2 seconds this is updated while the battery is being charged.
- When charging is started and whenever the ICHRG and VCHRG values are changed, we allow the charging system to stabilize for a couple seconds before implementing the power dissipation management.

4.4 Main Battery Charging

This Diagram below shows how the power paths lead to the battery within a phone using CPCAP. The Main FET is a switch used to selectively connect the BP to Battery.

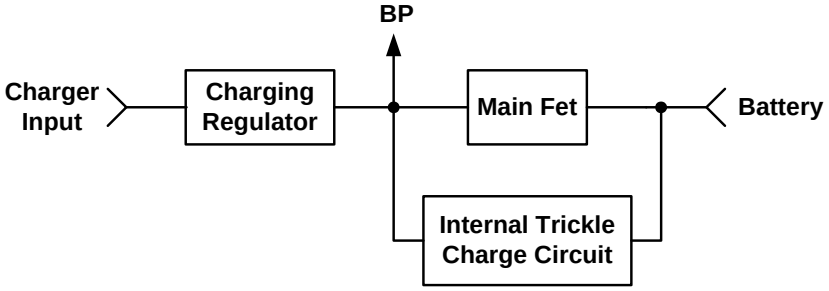

Figure 9. Charging Circuits

The Charging Regulator is a hardware regulator circuit with 2 modes, BP mode and BATTP mode. In both modes, it limits the voltage going to BP and in BATTP mode is also limits the maximum current from the Charger Input going to BP.

The Internal Trickle Charge Circuit is entirely enclosed in the CPCAP IC. Its purpose is to charge dead batteries up by passing current from BP to Battery.

4.5 Trickle-Charging

The internal trickle charger provides means to recover a dead battery. It defaults off and is turned on when the software programs the ICHRG_TR bits.
It does not regulate its output voltage but is fed from BP. The Charge Regulator in BP mode regulates the BP voltage to 4.3 +/- 0.2 volts. Software is needed to enable the Internal Trickle Charge path AND Software is needed to disable the Internal Trickle Charge path.

Parameter	Value	Trickle Charge Current (in mA)		
		min	nom	max
ICHRG_TR[1:0]	00	0	0	0
	01	16.8	24	31.2
	10	33.6	48	62.4
	11	50.4	72	93.6

Table 4. Trickle Charge Current Table

An unsafe failure is when the Internal Trickle Charger passes current from BP to BATTP when it is not supposed to. These failures occur when there are software defects or when there is an IC failure.

4.6 Battery-Voltage Detector

The software runs and it checks the battery voltage. if it is high enough to Rapid Charge (3.0 volts), it configures the Charge Regulator into BATTP mode and turns on the Main Fet. In sets the Charge Regulator current limit and voltage set points. Charging begins. If it is not high enough, the Charge Regulator remains in BP Mode, Main Fet stays off, and the Internal Trickle circuit is enabled at a typical value of 72 mA. This continues until the Battery reaches 3.0 volts, whereupon Rapid Charging is started.

5.0 Audio Interface

The audio voice call Tx path supports three analog inputs: a handset microphone, a headset microphone, and a speaker phone mode microphone, (no USB audio is supported). All three of these inputs are analog inputs to the CPCAP. The CPCAP has an internal ADC that converts the analog audio to PCM format for sending digital audio to to Hancock (OMAP and MODEM).

For tx audio other than voice call, (such as camcorder, voice notes, and voice recognition), the primary microphone or headset microphone are used. These inputs are analog into the CPCAP and then sent to the OMAP3430 using the same PCM bus.

The voice call audio Rx path supports a mono/stereo headset, differential ear speaker and differential class D speaker phone. For voice call audio the received audio in digital is sent to the CPCAP from Hancock via the same PCM bus. The CPCAP receive output section consists of the voice code, the stereo DAC and an external PGA.

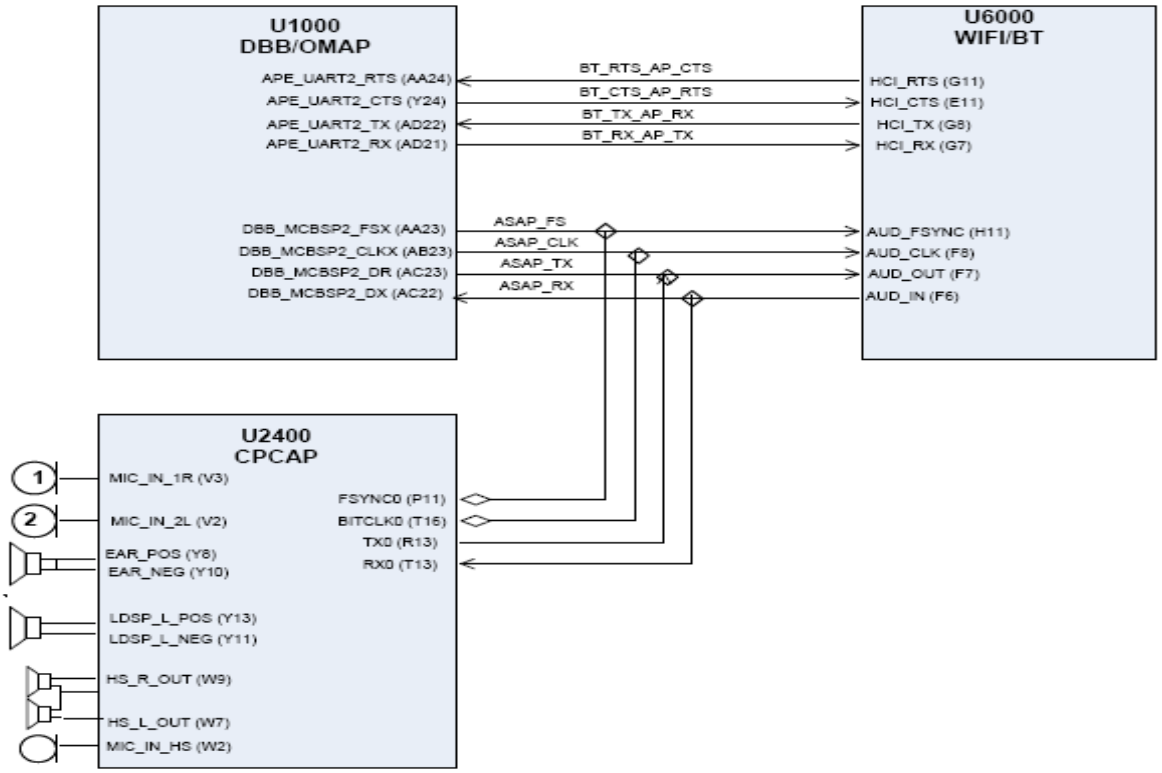

Figure 10. Audio Block Diagram

5.1 Headsets

MILESTONE supports a 3.5mm conventional headset. Both headsets with/without a microphone can be used. If no microphone is detected then the tx audio will use the primary microphone for in a call.

5.1.1 3.5 mm Headset

Stereo headsets using a 4-pole 3.5mm connector will be treated as a stereo headset.

The headset jacks can support multiple devices.

5.1.2 Headset Detection

Headset detection can be broken down into two, headset presence and mic detection.

The presence of the headset is detected when a headset is connected and HS_DET_B voltage drops from 2.8V to below 1.8V, (typically ~0.8V). This will also turn on the audio jack microphone bias from CPCAP. The high to low transition of HS_DET_N will cause an interrupt for “accessory attach” detection. When the headset is unplugged, the Low to high transition will generate the same interrupt for detach detection and will also turn off the headset microphone bias.

After the headset presence detection the current of the headset mic bias will be monitored to see if a headset with a microphone is connected.

5.1.3 Headset Button Press (SEND/END) Detection

For headset operation, the MIC_BIAS2 circuitry provides the ability to detect a Send/End event and to determine whether or not a short circuit condition exists at the MIC_BIAS2 pin. Send/End detection is available when the microphone bias supply voltage is enabled as well as when it is not. A 2.2kΩ bias resistor is placed between the MIC_BIAS2 pin and the microphone pin of the headset jack. The PTT_DET pin is connected to the headset jack side of the bias resistor. The PTT_DET comparator monitors the voltage at the PTT_DET pin and provides an indication of a Send/End event or short circuit condition.

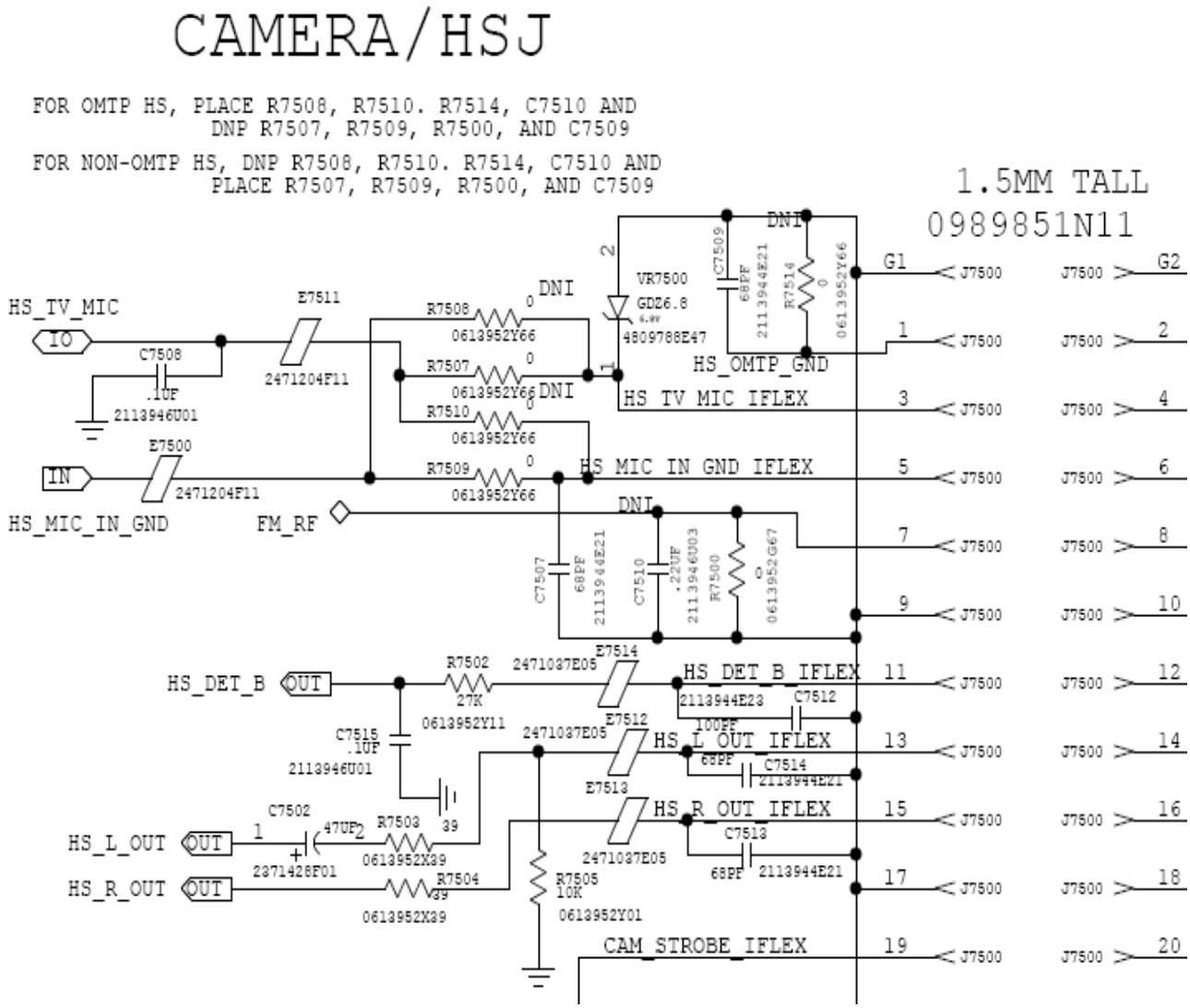

Figure 11. 3.5 mm Headset Circuit

6.0 Display Interface

The main display is 3.7", 854 x 480 WVGA module. It is located in the slider and connected to the slider pcb. The display driver IC is part of the display module and is connected via a display flex connector.

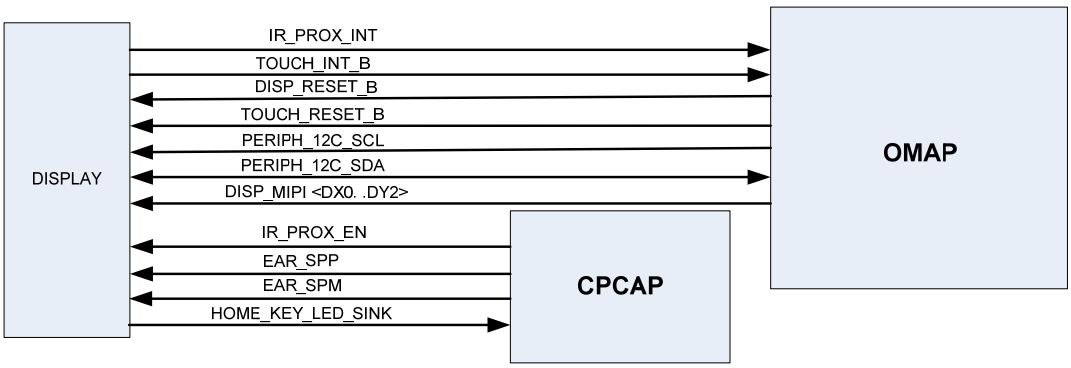

Figure 12. Display Block Diagram

6.1 Display/Touch Button Lighting

An LM3530 current mode boost converter is used to drive backlight LEDs for the display. The device uses the I2C interface to communicate with the boost circuit. ALS, I2C and PWM interface are used to enforce seamless readability. CABC is used to control the power consumption under different display settings.

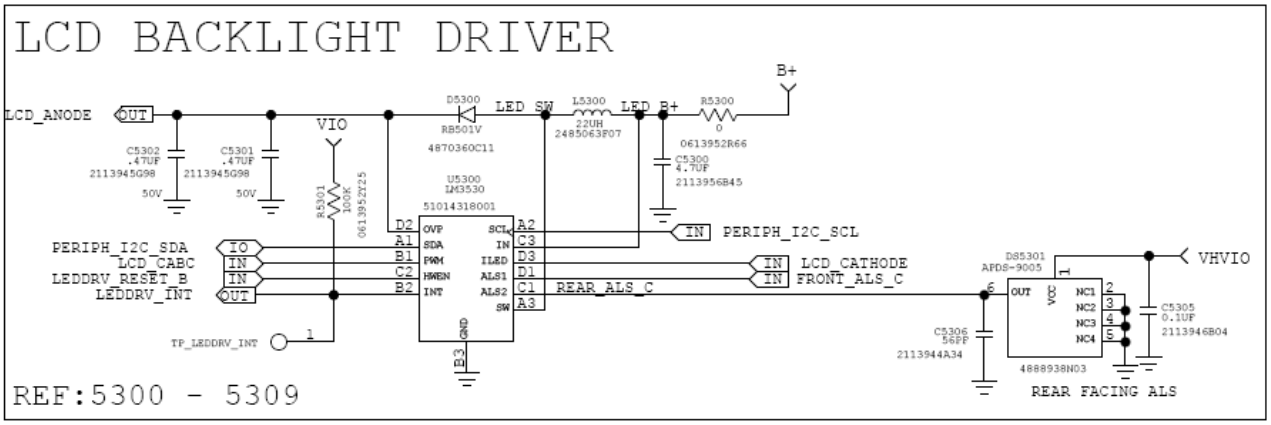

Figure 13. Display Backlighting Diagram

6.2 Home Key Lighting

Home keys are controlled by a CPCAP current sink called KPSINK. Signal name is HOME_KEY_LED_SINK. 6mA/led is the limit set for the home key leds. VBOOST_SLIDE

is the anode and measures 2.8V. 100ohm resistor is used to control the current sink and provide uniformity across 4leds.

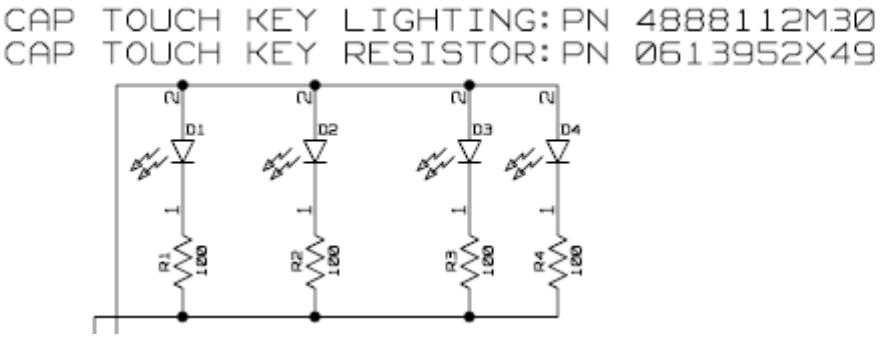

Figure 14. Home key Backlighting Diagram

6.3 Message LED

Message LED is a tri colored RGB led controlled by CPACP current sinks. REDSINK_1 controls the color red, GREENSINK controls green and BLUESINK controls blue. Red and green are mixed to produce emerald color and all three rgb are mixed in specific proportion to generate white color.

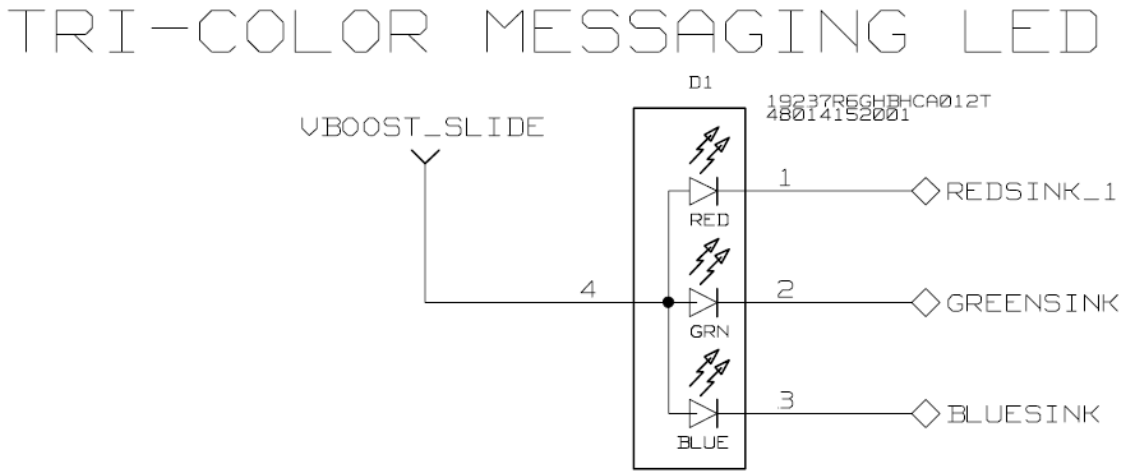

Figure 15. Message LED Backlighting Diagram

7.0 Qwerty Keypad lighting

The Milestone QWERTY keypad uses EL backlighting. The EL backlighting driver supports two EL zones, however, only EL1 is used. EL_EN turns the EL panel on and off and is connected to PM_GPIO6 on the CPCAP IC. The EL is on when EL_EN is high (1.8v) and off when EL_EN is low (0v). The 2 test points (TP_EL2_xxx) are not used.

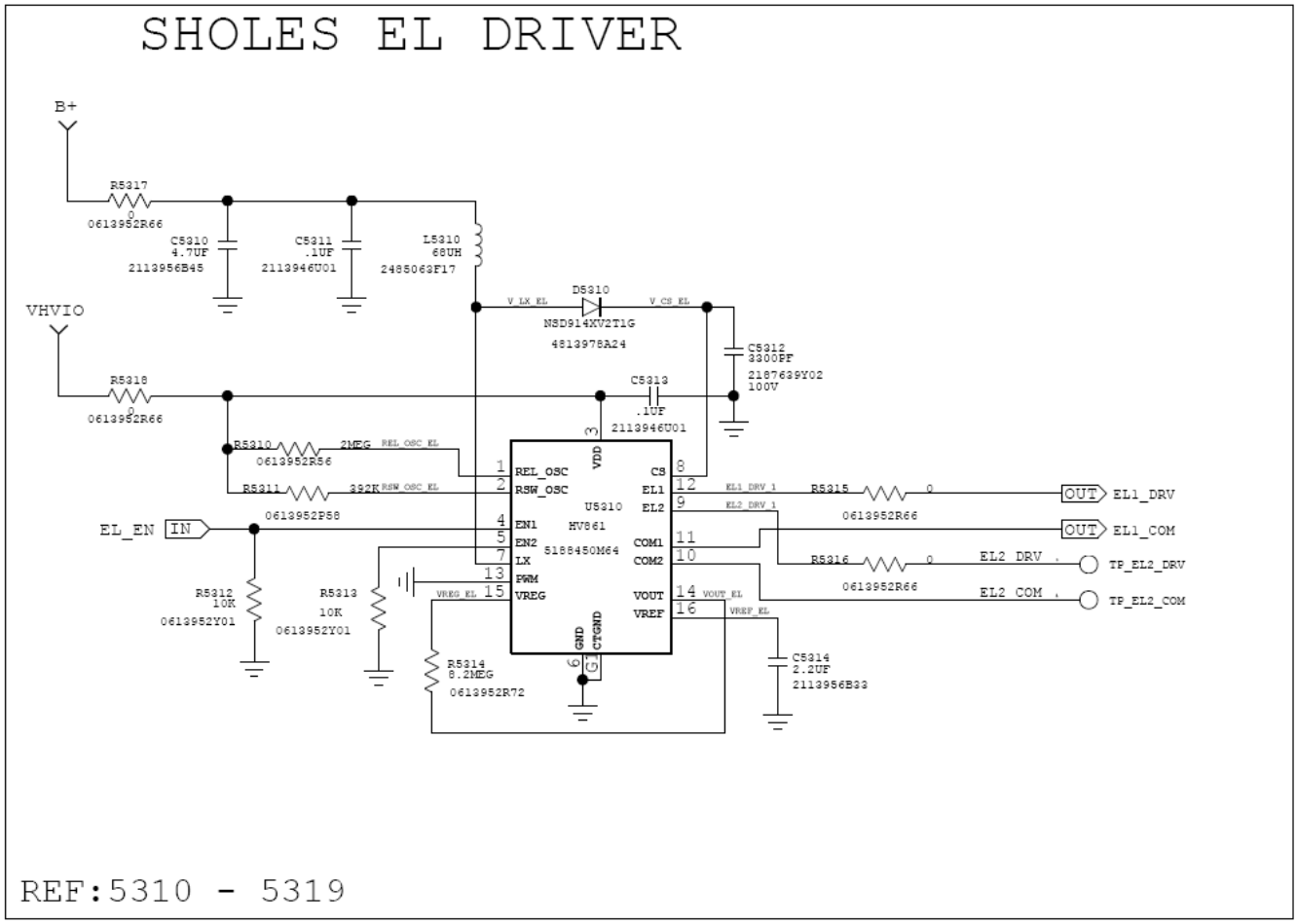

Figure 16. QWERTY Backlight Diagram

8.0 Slider Detect & Dock Detect

8.1 Slider Hall Effect

Milestone uses 2 Hall effect sensors. One for slider detect, the other for docking station detect. Both Hall effect sensors are powered by a 1.8v rail (therefore outputs are 1.8v).

The Milestone slider Hall effect sensor detects the presence of a magnet in the slider. The magnet is positioned above the sensor (detect) when the slider is closed. The output of the sensor (pin5 of U8000) is connected to APE_MCSPI1_CS3/GPIO_177 on OMAP and is driven high by the sensor device when no magnetic field is present. When either a north or south magnetic field is detected, the device is said to be 'in detect' and the output is driven low (0v).

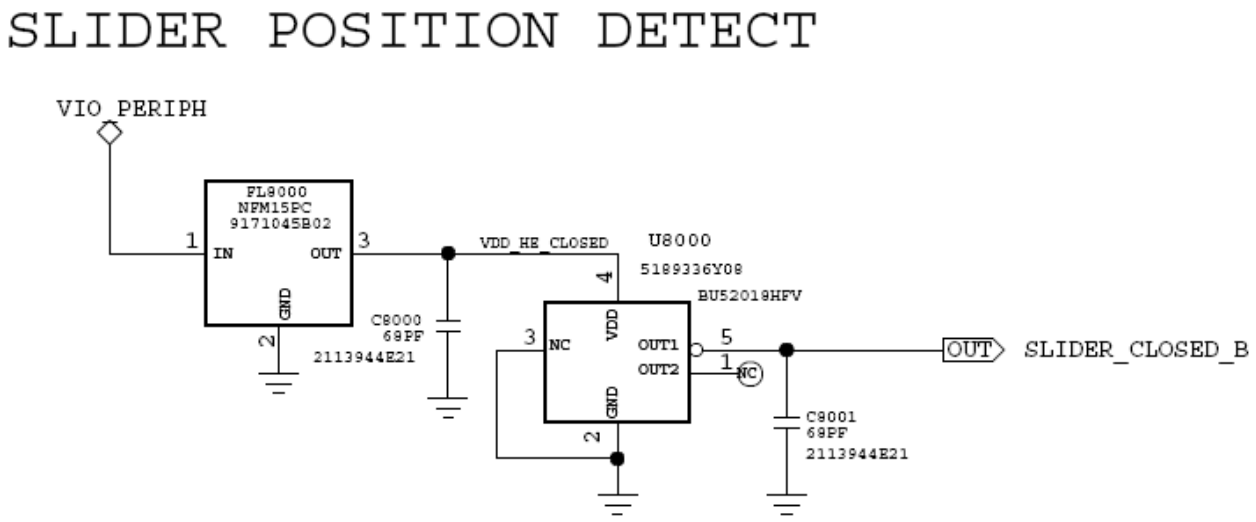

Figure 17. Slider Detect Schematic

8.2 Dock Hall Effect

Milestone uses 2 Hall effect sensors. One for slider detect, the other for docking station detect. Both Hall effect sensors are powered by a 1.8v rail (therefore outputs are 1.8v).

The Milestone dock Hall effect sensor detects the polarity (North or south) of a magnet in a docking station external to the phone. The magnet in the dock is specifically polarized north or south to tell the phone what type of dock it is in. There are two outputs on the dock sensor that are connected to GPIO10 (north) and GPIO111 (south) on OMAP. These outputs correspond to the polarity of the magnetic field detected. Both outputs are driven high by the sensor device when no magnetic field is present. When either a north or south magnetic field is detected, it's corresponding output will be driven low (0v). Please see Table 5 below for specific information.

DOCKING STATION DETECTION

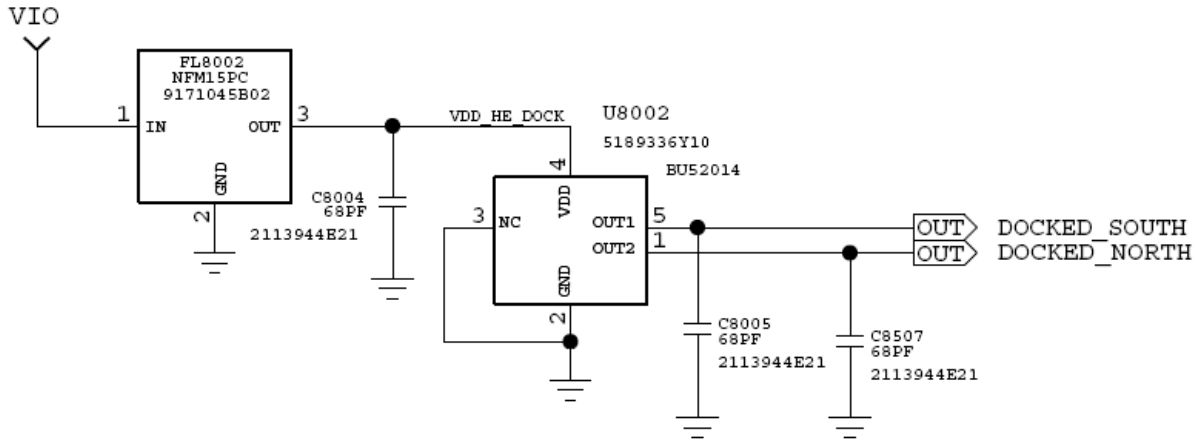

Figure 18. Dock Detect Schematic

Schematic Netname	GPIO <Package Pin Name> (BGA)	5189336Y10 Device pin number	Description
DOCKED_SOUTH	GPIO111 <APE_CAM_XCLKB/GPIO_111> (E25)	5	This pin goes low in the presence of a South pole
DOCKED_NORTH	GPIO10 <ape_sys_clkout1> (AE14)	1	This pin goes low in the presence of a North pole

Table 5. North & South GPIO Description

9.0 Capacitive Touch Sensor

Capacitive Touch Screen Sensor IC – This device is a digital burst mode charge-transfer sensor designed specifically for matrix layout touch controls; it includes all signal processing functions necessary to provide stable sensing under a wide variety of changing conditions.

The circuit operates by scanning each X line sequentially, with the associated channels along each X line sampled in parallel. X axis keys are known as rows while Y axis keys are referred to as columns, although this has no reflection on actual wiring. Key scanning begins with X0. Keys are scanned sequentially by X line.

Capacitors absorb charge from the key electrodes on the rising edge of each X pulse. On each falling edge of X, the Y matrix line is clamped to ground to allow the electrode and wiring charges to neutralize in preparation for the next pulse. With each X pulse charge accumulates on Cs causing a staircase increase in its differential voltage.

Touch is detected because a human finger absorbs charge and this change in charge transfer is how a capacitive touch screen using charge transfer technology can track touch.

- ATMEGA324P running custom 51001211009A-S firmware
- 1024X1024 resolution touch screen for user input.
- 84 lines (12 x 7 matrix) serving as the sensor signals.
- The interrupt signal will activate whenever the screen is pressed and released.
- I2C used to get key status and issue other commands.

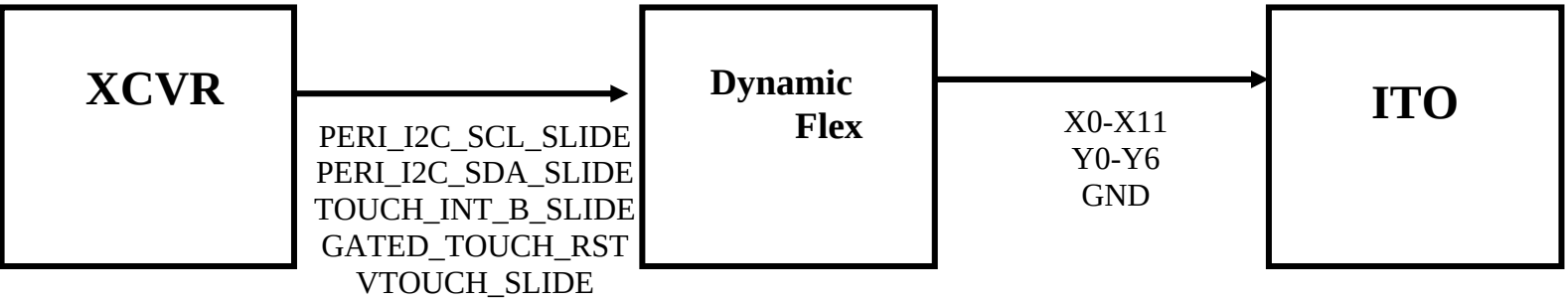

Figure 19: Touch screen Block Diagram

The MILESTONE uses an ATMEGA324P for the main touch screen panel. The touch panel supports a touch screen resolution of 1024 x 1024 which extends beneath the display for the 4 touch sensitive buttons. The touch panel has 84 channels (12 x 7) serving as the sensor signals. The touch screen sensor IC uses the TOUCH_INT_B_SLIDE (main touch screen) to notify the OMAP when the screen is pressed and released. An I2C interface is used to get touch status and issue other commands to the touch screen IC.
The touch IC is running at 400kHz.

Additional information as follows:

- Main power supplies include VTOUCH_SLIDE (2.8V) which is generated via a dedicated LDO on xcvr from B_PLUS.
- TOUCH_INT_B_SLIDE is an active low signal.
- The 4 buttons at the bottom are not real touch sensitive buttons. Instead, the touch screen extends below the display active area. When a user touch any of the 4 buttons, the touch screen driver reports back a X,Y value. The driver interprets if this value falls in the pre defined target area for each of these buttons. If it does, the touch driver reports a key event to the HAL layer as opposed to a touch event.

10.0 Vibration Motor

The rotary vibrator is used for global alert as well haptics. The current scheme is explained in the schematic shown below.

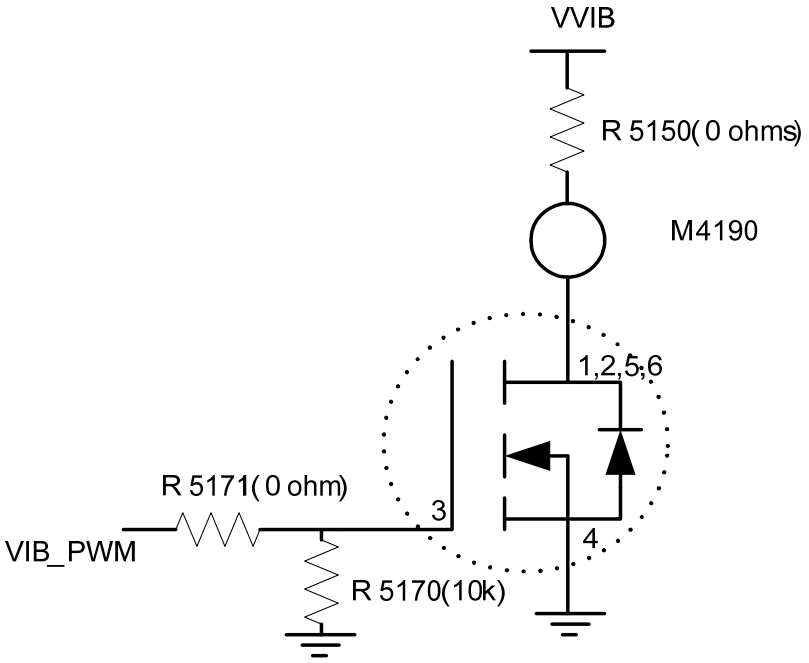

Figure 20: Schematic for rotary vibe drive circuit

VVIB is a CPCAP dedicated power supply for rotary vibe and is rated for 200mA current. It has 4 configurable modes for voltage out: OFF, 1.8V, 2.0V, 3.0V. VIB_PWM is a GPIO connected to OMAP. For vibe operation, OMAP enables the FET by enabling VIB_PWM which turns on the FET and the rotary vibe.

Current implementation in K29 software has set the global alert at 3V for VVIB.

Haptics are used for the 4 touch sensitive buttons. The Touch driver reports the button presses to OMAP. OMAP then enables haptics for these keys by enabling VIB_PWM. Global alert is also implemented by OMAP by controlling VIB_PWM signal.

11.0 Camera

A455 has 5.0 Mega pixel CMOS camera with autofocus and LED flash. The camera interface connects directly to the Applications Processor (OMAP). The OMAP accepts raw Bayer pattern data which is process by a Hewlett Packard software image pipe (running on the OMAP) where it is converted (RGB interpolation, color space conversion, auto white balance, auto exposure, gamma correction, etc.) for display, still image or video capture.

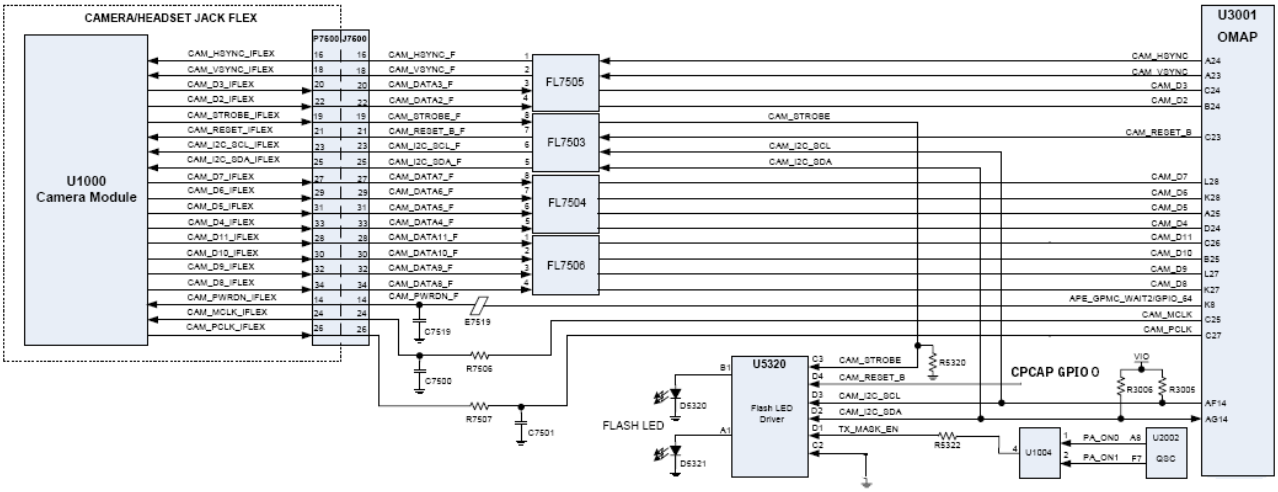

Figure 21. Camera Connectivity Diagram

The camera is mounted on a flexible PCB and connects to the main PCB via a 34 pin board to board connector. The camera shares the flexible PCB with the external headset jack and associated passives.

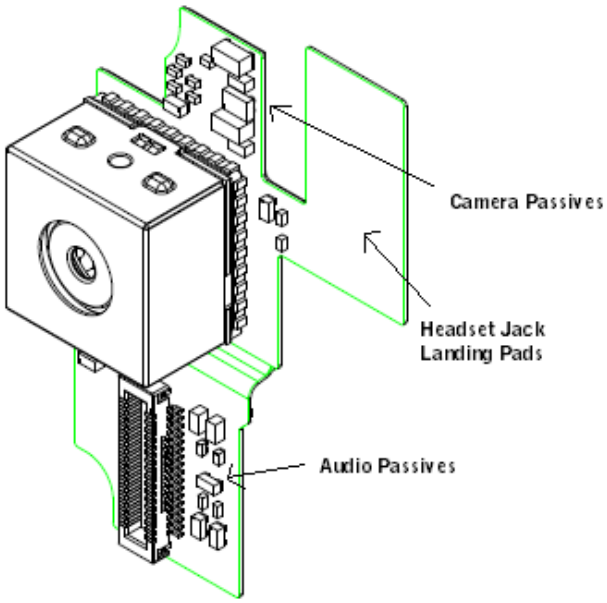

Figure 22. Camera Module & Flex

The camera requires 3 separate power supplies, 1.8V, 2.8V and 2.9V. The 1.8 volt supply is the core digital supply and is supplied by the CPCAP. The 2.8V supply is the analog/pixel supply and is generated from an on board (camera flex) 2.8V LDO, driven by the battery voltage. The 2.9V supply is the Auto Focus supply and is generated by the CPCAP. The LDO is enabled by the 2.8V pixel supply.

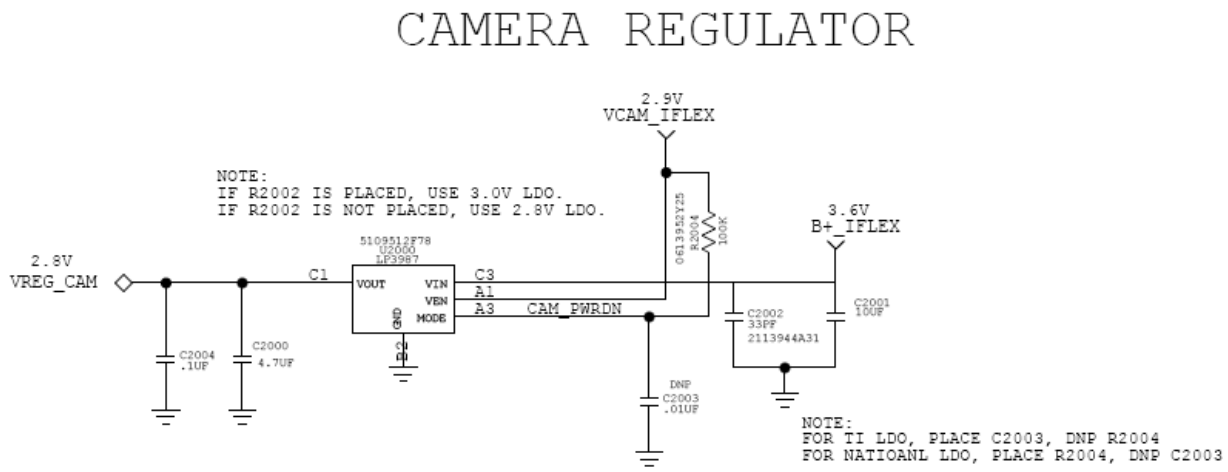

Figure 23. Camera Supply

The camera interface consists of 10 data bits (d0-d9), a horizontal sync (hsync), vertical sync (vsync), a pixel clock (pclk) and an input clock (mclk). The camera input clock mclk is 48Mhz, and is active any time the camera is turned on. The output clock is either 53.6Mhz (live view mode 1296X972) or 55.8Mhz (capture mode 2592X1944). The core of the camera module is a Aptina 5131 raw bayer CMOS sensor.

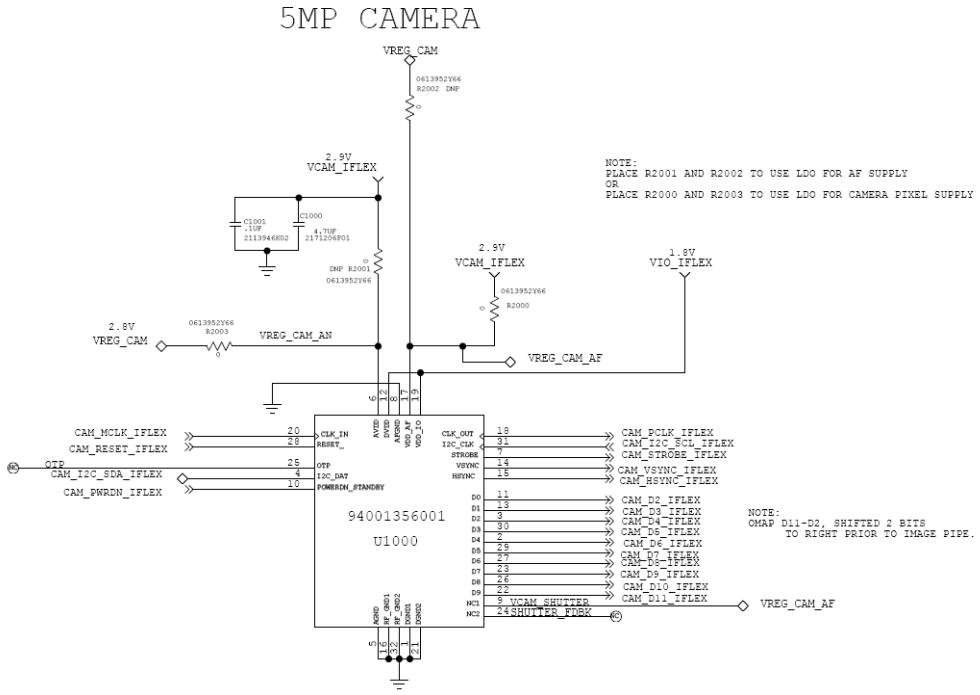

Figure 24. Camera Module

The camera is configured via I2C bus. There are 4 devices on the camera I2C bus, the camera sensor (0x6C), camera autofocus (0x0A), camera calibration memory (0xA0), and camera flash driver (0xA6). The Autofocus driver and the calibration memory are located within the camera module housing.

The camera flash driver is on the main PC board, adjacent to the camera flex assembly.

The camera flash is implemented using a LM3554 Dual LED driver. The LM3554 supports dual Flash outputs, indicator LED and a 4.5/5V regulated output rail. Only the dual LED outputs are utilized in the A455 design. The LM3554 utilizes 3 GPIOs that can be configured to support still image flash, video torch, and flash to torch setback modes of operation. The driver is configured and controlled via a set of I2C accessible registers.

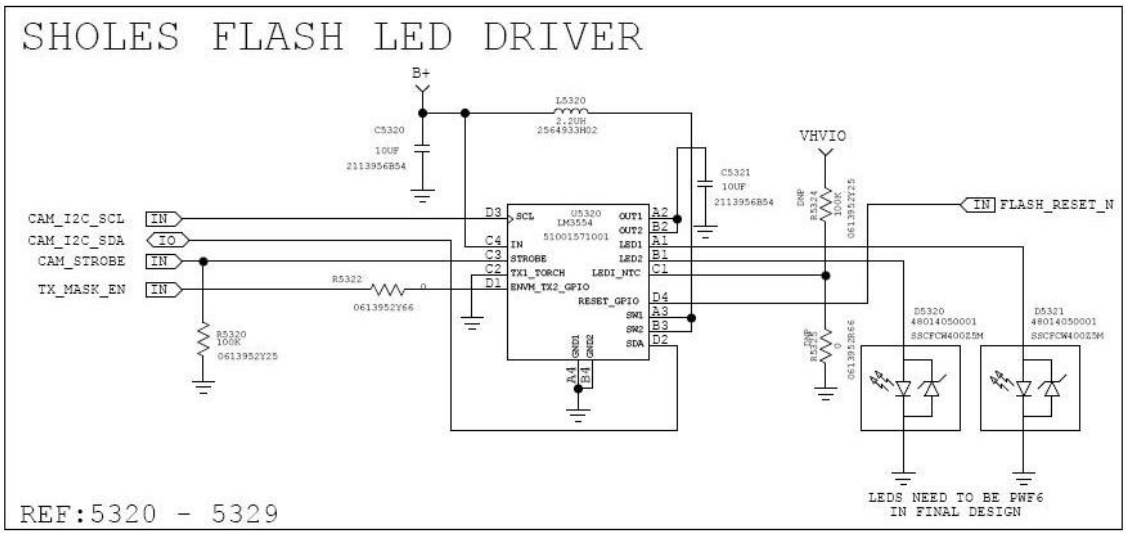

Figure 25. Camera Flash

The still image flash can be controlled via the camera strobe line (LM3554 STROBE pin, driven directly by the camera module) or directly via I2C command. The flash duration is determined by the strobe pulse duration and the preset timeout value written to the LM3554 Flash Duration Register. The flash brightness is determined by a configurable LM3554 I2C register.

Video torch mode must be controlled via an LM3554 I2C register. The torch brightness is determined by a configurable LM3554 I2C register.

The flash can be forced to low current torch mode via the LM3554 LM ENVM_TX2_GPIO pin after configuring the LM3554 for flash inhibit mode via an I2C configuration register.

11.0 Magnetometer

Milestone contains Asahi Kasei Microsystems (AKM) magnetometer AK8973N. The AK8973 IC contains three integrated magnetic sensors for detecting geomagnetism, and circuits for processing signals from each sensor. It also contains a temperature sensor. Sensor data is accessible via I2C. A high-level block diagram of the AK8973 IC is shown below.

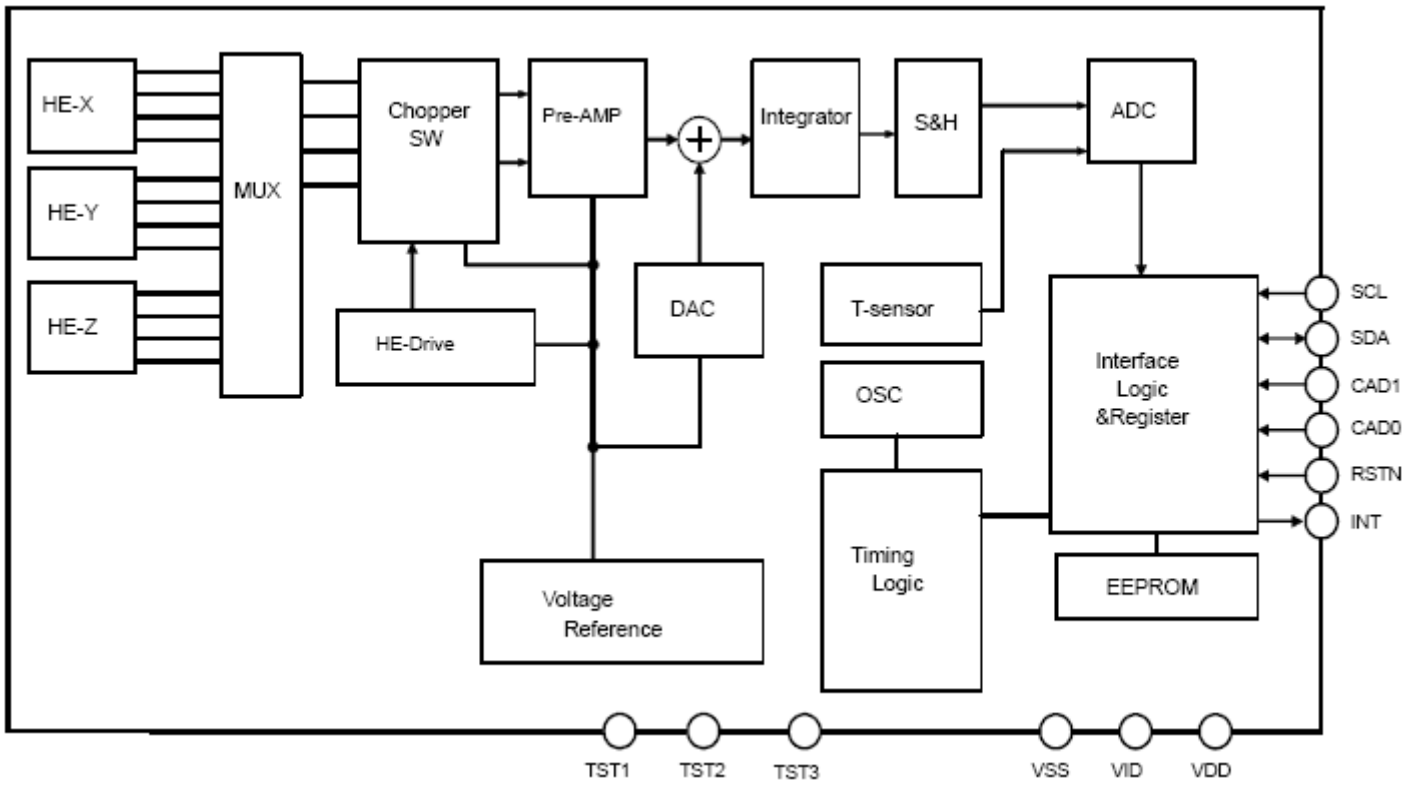

Figure 26. AK8973 Block Diagram

Combining sensor outputs from AK8973 and an accelerometer IC, along with appropriate application software algorithms, make it possible to determine heading. Application software that provides a user with heading determination is often called an “electronic compass” or “eCompass”. Referring to the magnetometer itself as an “eCompass” is misleading and technically incorrect since in most situations information available from the magnetometer alone is insufficient to determine heading.

The schematic of the magnetometer section from Milestone is provided below. Two power supply inputs are required: VHVIO (~2.75VDC) to power the IC core and VIO (~1.8VDC) to supply the digital interface between AK8973 and application processor.

Signal MAG_RESET_B is an input to AK8973 from the application processor – note the schematic incorrectly indicates this signal is an AK8973 output. When asserted, MAG_RESET resets IC internal registers to their power-on reset states.

Data in to/out of AK8973 flows over an I2C interface to the application processor.

Interrupt output DIG_COMP_INT alerts the application processor that a requested magnetic field vector measurement is complete, and measurement data is valid and ready to be retrieved over I2C.

Input pins CAD0 & CAD1 are used for hardware-defining the I2C address of the AK8973 IC. In Milestone, both CAD pins must connect to ground to ensure AK8973 conforms to I2C address mapping assigned by development.

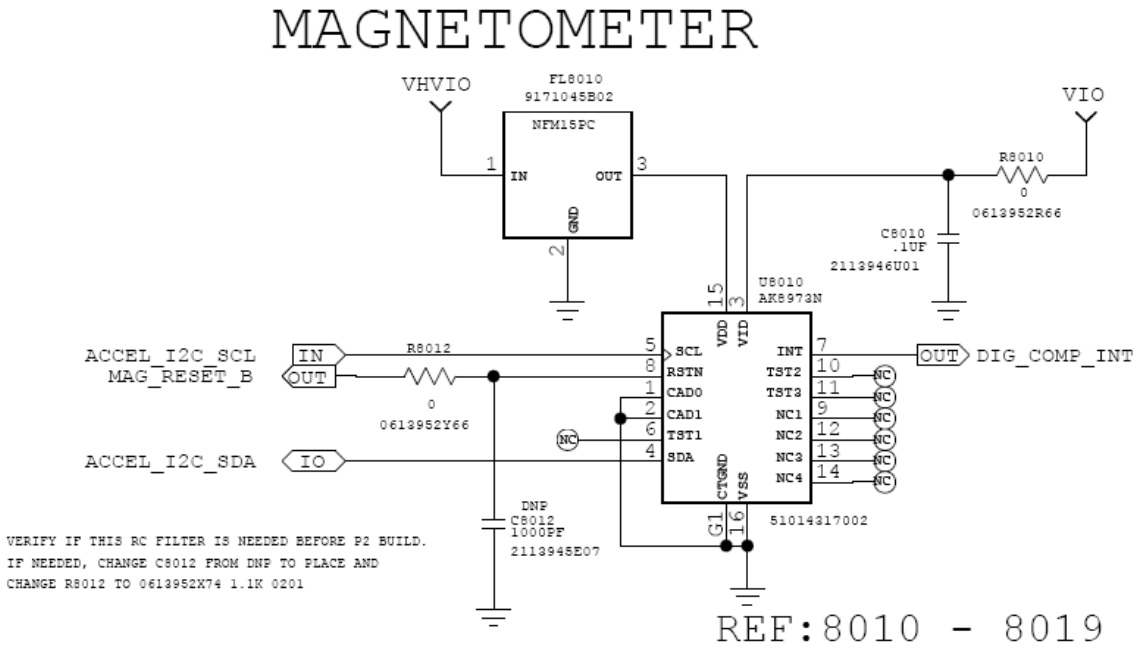

Figure 27. Magnetometer schematics

12.0 Accelerometer

The lis331dlh is a three access linear accelerometer. The accelerometer has dynamically user selectable full scales of ±2*g*/±4*g*/±8*g* and it is capable of measuring accelerations with output data rates from 0.5 Hz to 1 kHz. The self-test capability allows the user to check the functioning of the sensor in the factory to ensure that all three axis are functional. The device has 2 interrupts but are not used in the Android SW.

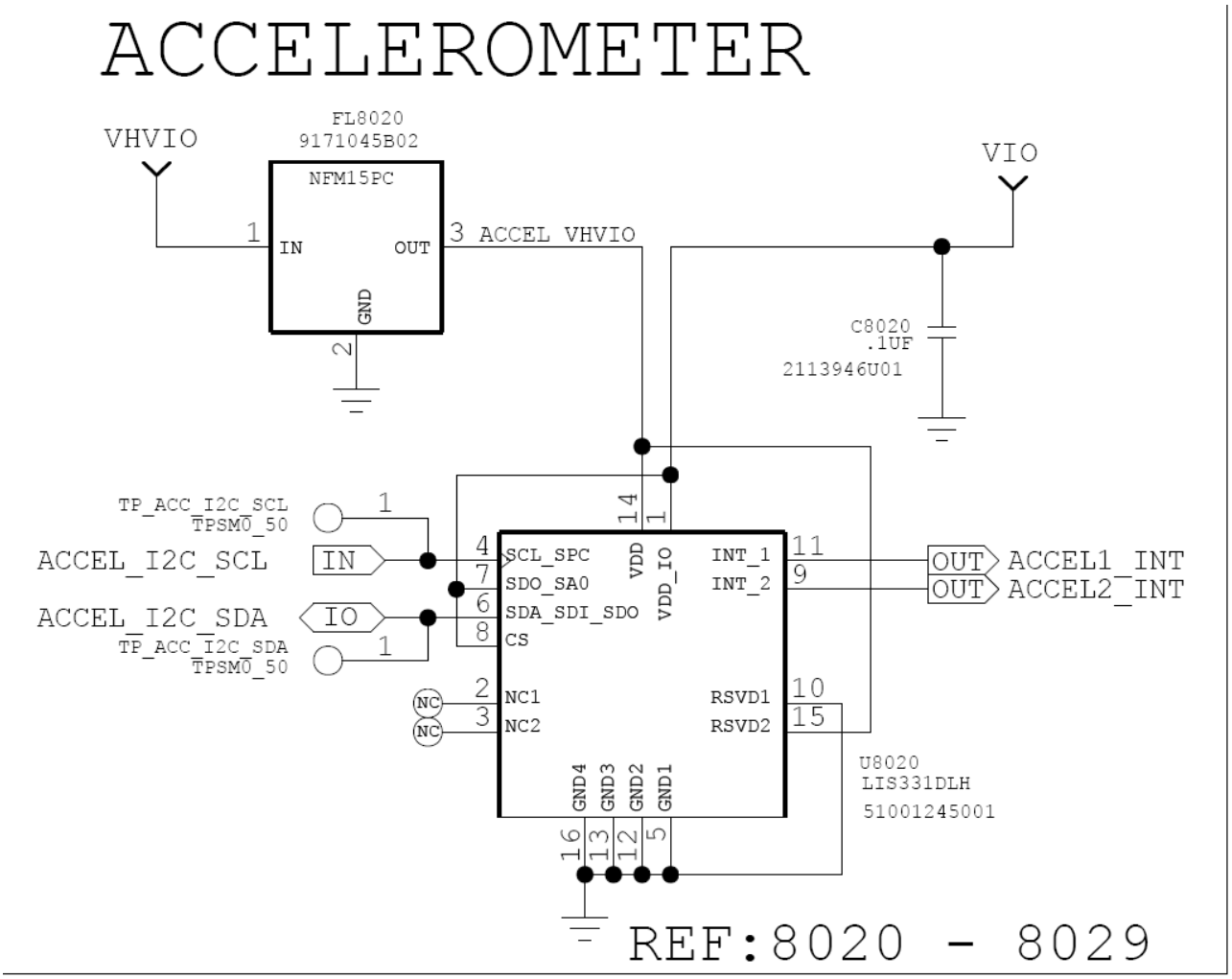

Figure 28. Accelerometer diagram

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13.0 Proximity Sensor

SFH7743, Digital proximity detector with integrated emitter driver is used to enable the proximity feature on Milestone. It works with the external emitter SFH4058 to provide a detect distance of about 60mm on white surface. It is an extremely low power consumption device with very small smd package. It has high ambient light suppression. It is used as a short range proximity detector to detect any obstruction(typically user's face) when in call to turn off the display backlight. The circuit is shown below:

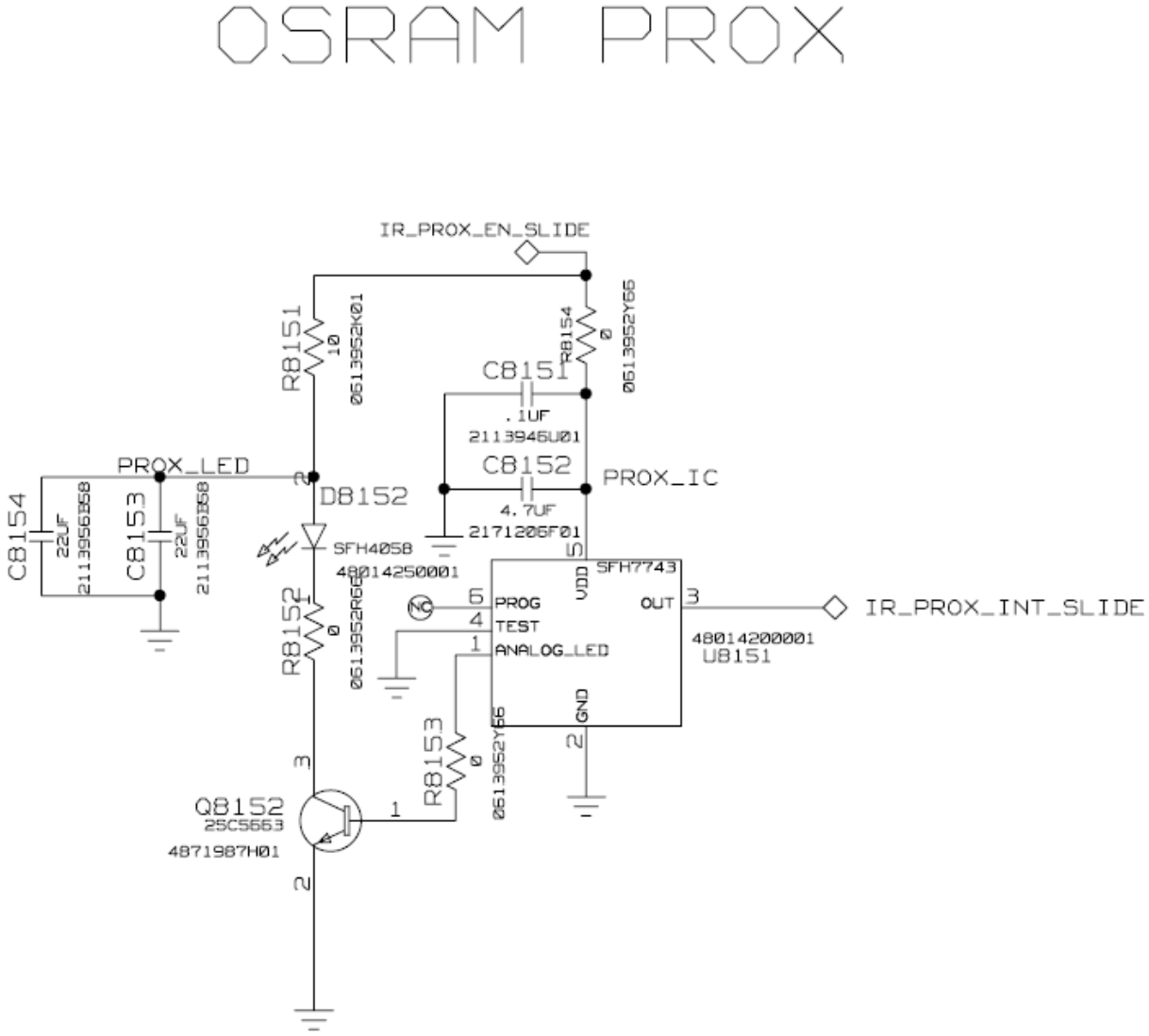

Figure 29. Accelerometer diagram

IR_PROX_INT_SLIDE triggers when the sensor sees an obstruction.

14.0 WLAN & Bluetooth

14.1 WLAN

A wireless LAN is a data transmission system designed to provide location-independent network access between computing devices by using RF rather than a cable infrastructure. The 802.11 standards focus on the bottom two levels the ISO model, the physical layer and link layer.

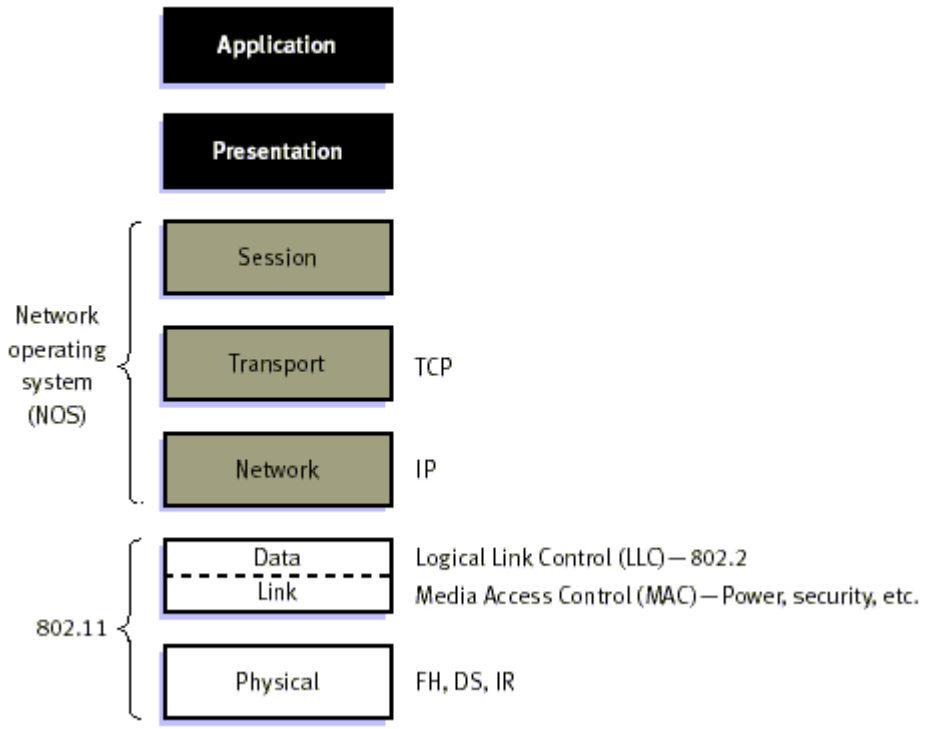

Figure 30. The OSI Model

The original 802.11 wireless standard defines data rates of 1 Mbps and 2 Mbps via radio waves using frequency hopping spread spectrum (FHSS) or direct sequence spread spectrum (DSSS).

FHSS techniques allow for a relatively simple radio design, but are limited to speeds of no higher than 2 Mbps. For greater speeds DSSS is used.

The data link layer within 802.11 consists of two sublayers: Logical Link Control (LLC) and Media Access Control (MAC).

MILESTONE supports 802.11 b/g standards.

- **802.11b** was the first 802.11 standard to be released. It is also called Wireless Fidelity, or Wi-Fi, it has a range suitable for use in big office spaces. Wi-Fi is currently the most popular and least expensive wireless LAN specification. It operates in the unlicensed 2.4 GHz radio spectrum and can transmit data at speeds up to 11 Mbps within a 30m range. It can be affected by interference from mobile phones and Bluetooth devices which can reduce transmission speeds.
- **802.11g** is the latest standard and promises to be the most popular format. It operates in the unlicensed 2.4 GHz radio spectrum and can transmit data at speeds up to 54 Mbps.

14.2 Bluetooth

Bluetooth provides short-distance two-way wireless connection from to cordless earpieces, stereo headset, handsfree car kits, and others. The Bluetooth radio transceiver complies with Bluetooth Core Specification 2.1+EDR. The transceiver contains on-chip modulator/demodulator, signal processing, and ARM-core processor. Bluetooth modulation is frequency-hopping spread spectrum, operating on 79 channels 1-MHz-wide 2.402 GHz to 2.480 GHz. Transmit power level is Class 1.5, for 20-meter operating range.

Baseline data rate is 1 Mbit/second. Two higher speeds are possible in Enhanced Data Rate modes—2 Mbit/s and 3 Mbit/s. The EDR modes save battery life between two EDR-capable Bluetooth devices by shortening transmit/receive time.

Bluetooth supports two basic link types: Asynchronous Connecton less Link (ACL) and Synchronous Connection-Oriented (SCO). Two devices establish an ACL link for initial device pairing and certain data-centric applications. Stereo audio to a Bluetooth headset also uses an ACL. A SCO link handles full-duplex digital voice during a pone call between two paired devices. Different ACL & SCO link types trade error correction capability for power saving or permitting multiple linked devices

The Bluetooth transceiver requires a unique ID, the Bluetooth Device Address (BD_ADDR), which is loaded during flashing.

14.3 TI WL1271

The WL1271 from Texas Instruments is a highly integrated single-chip CMOS (65-nm process) WLAN / Bluetooth / FM RX/TX device that forms a complete standalone WLAN 11b/g/n, Bluetooth wireless communication system and FM Radio transceiver.

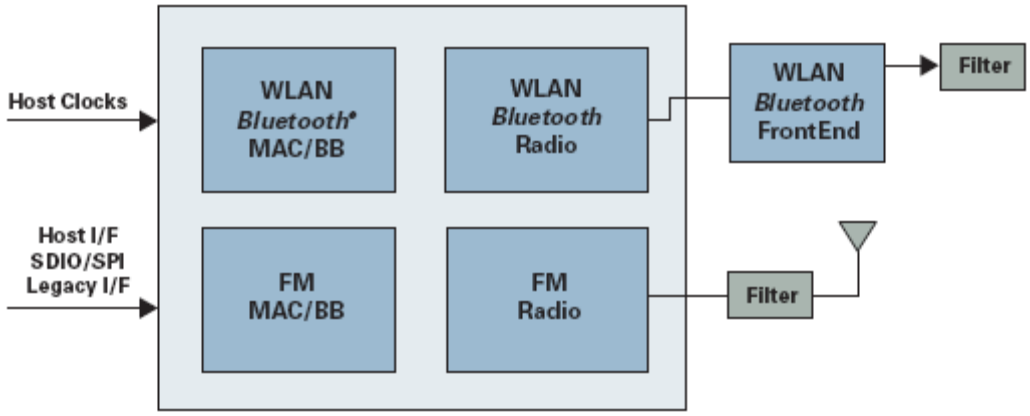

Figure 31. WL1271 Block Diagram

14.3.1 WLAN Features

- WLAN MAC Baseband Processor and RF transceiver which is IEEE802.11b/g and IEEE802.11n PICS compliant
- Optimized for ultra low current consumption in all operating modes including extremely low power modes
- Accepts 19.2, 26, 38.4, 52-MHz reference clock Inputs for easy integration into cellular handsets
- IEEE Std 802.11d,e,h,i,k,r,s PICS compliant
- Supports Cisco Client eXtensions (CCX) standard
- Supports serial debug interface
- Supports Secure Digital Input/Output (SDIO) Serial Peripheral Interface (SPI) Host Interfaces
- Medium-Access Controller (MAC)
    - Embedded ARM™ Central Processing Unit (CPU)
    - Hardware-Based Encryption/Decryption Using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys,
    - Supports requirements for Wireless Fidelity (Wi-Fi) Protected Access (WPA and WPA2.0) and IEEE
- Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
    - Designed to Work With IEEE Std 802.1x for Virtual Private Network (VPN) Solutions

- Baseband Processor
    - IEEE Std 802.11n single-stream data rates (MCS0-7) and SGI support
- 2.4 GHz Radio
    - Digital Radio Processor (DRP) implementation
    - Internal LNA
    - Supports: IEEE Std 802.11b, 802.11g, 802.11b/g and 802.11n

14.3.2 Bluetooth Features

Bluetooth 1.1, 1.2, 2.0+EDR and 2.1+EDR specification compliant (Lisbon release) - up to HCI level.

- BT Enhanced Data Rate (2 and 3 Mbps)
- Enhanced host interfaces (UART, btSPI)
- Very low power consumption
- On-chip Embedded radio
    - Integrated 2.4 GHz RF transceiver
    - All digital PLL transmitter with digitally controlled oscillator
    - Near zero IF architecture
    - On-chip TX/RX switch
    - Support for Class-1.5 applications
- Embedded ARM Microprocessor System
    - High rate four wire UART HCI (H4) and Three Wire UART HCI (H5)
    - Automatic clock-detection mechanism
- Flexible PCM and I2S interfaces: full flexibility for data order, sampling and positioning
- Temperature detection and compensation mechanism ensures minimal variation in the RF performance over the entire temperature range
- TI-proprietary low-power scan achieves paging and inquiry scans at 1/3 normal power.
- Digital Radio Processor (DRP) single-ended 50 W I/O for easy RF interfacing
- Patch trap mechanism and reserved RAM enables easy bug fixes
- Advance Audio Interfaces and capabilities
    - A2DP support
    - A2DP internal loopback
    - Wide-Band Speech support
    - On board SBC encoder/decoder - offloads host for A2DP and WideBand speech processing

15.0 USIM interface

Milestone SIM card interface supports both 2G and 3G, and both 1.8 and 3V SIM cards. In Fig 32, SIM_IO, SIM_CLK and SIM_RST are from OMAP3430. VSIMCARD is supplied by CPCAP and can be set at either 1.8V or 2.9V by software depending on the supply voltage a SIM card specified.

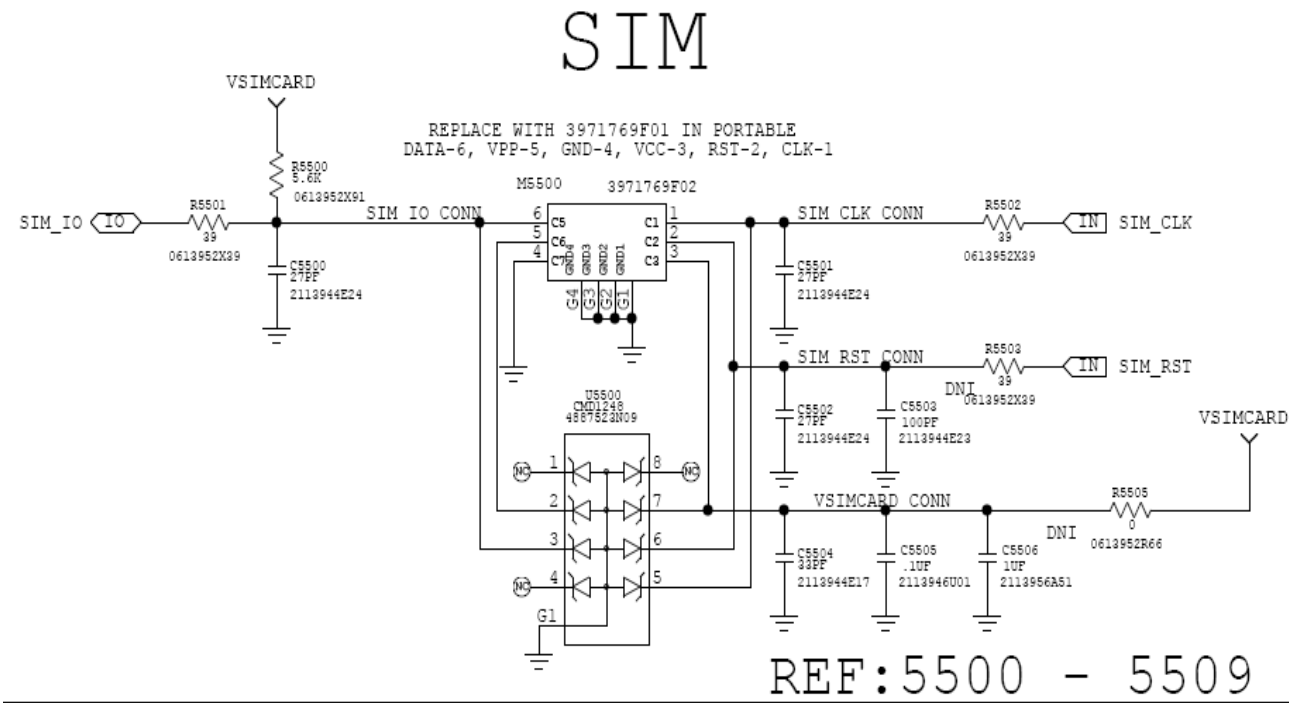

Figure 32. USIM Interface