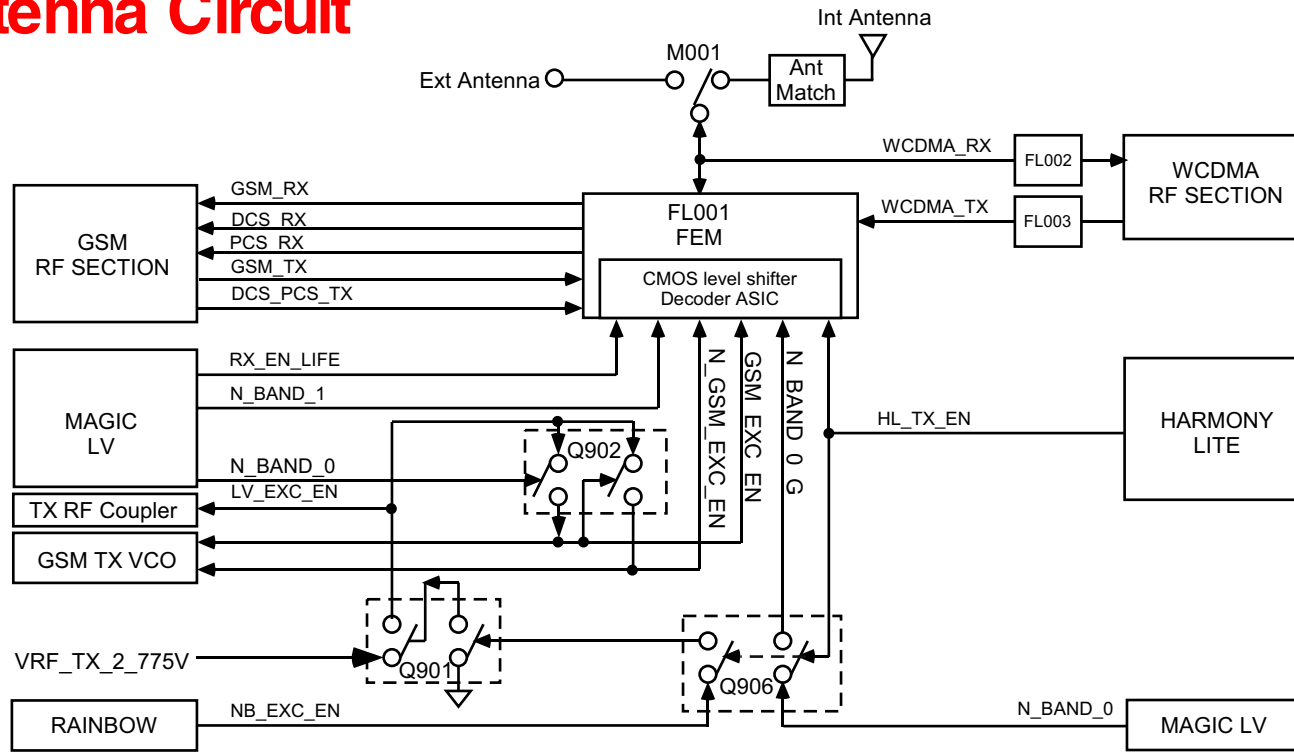


## 4-2 A835: Antenna Circuit



### Description

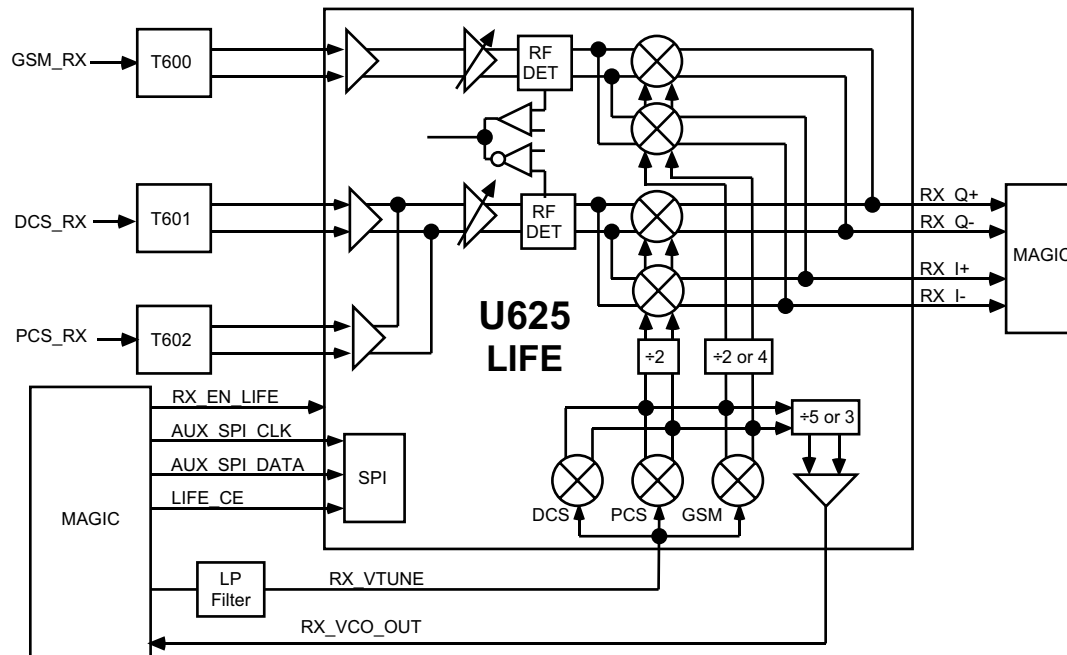
All cellular receive bands are fed into either the internal antenna or external antenna. M001 is a mechanical switch which has the internal antenna path connected when a no insertion condition exists. The RF path will switch to external antenna upon insertion of a male SMA connector to M001. The internal antenna path is fed to the FEM(Front End Module) through antenna matching components. The FEM provides band selection and filtering between the EGSM, DCS, PCS and WCDMA receive and transmit bands to a single antenna port. GSM band selection is done by control lines N\_BAND\_1 and N\_BAND\_0\_G. Mode selection is done by control lines HL\_TX\_EN, RX\_EN\_LIFE, N\_GSM\_EXC\_EN, and GSM\_EXC\_EN. The diplexing arrangement permits reception of WCDMA signals in any FEM switch position. This allows the phone, while in a GSM call in any band, to detect signals from a WCDMA base station. The decision may then be made to hand over to the WCDMA system. Similarly, EGSM base station signals can be detected while the phone is in a WCDMA call to permit a handover decision from WCDMA to EGSM (This is not possible for base station signals in the DCS and PCS bands.).

Signals received at the antenna between 2110 - 2170MHz will see the RF switch as an open circuit at any position. Consequently WCDMA Rx signals will go through FL002 to the WCDMA receiver. FL002 should have a maximum insertion loss of ~0.5dB. Outside of the WCDMA Rx band, FL002 behaves as an open circuit, preventing out-of-band signals from reaching the WCDMA receiver.

GSM, DCS, and PCS receive signals from the antenna port through the FEM should have a maximum insertion loss of -4.4dB. The FEM EGSM transmit path should have a maximum insertion loss of -2.5dB. The FEM DCS transmit path should have a maximum insertion loss of -3.1dB. The FEM PCS transmit path should have a maximum insertion loss of -3.7dB.

Q902 is a dual FET package that's being used to multiplex function of the N\_BAND\_0 control signal coming from the Magic LV. With the use of Q902, N\_GSM\_EXC\_EN will follow N\_BAND\_0. GSM\_EXC\_EN will be the inverted level of N\_BAND\_0. Q906 is another dual FET package that's used to prevent simultaneous GSM and WCDMA transmission conditions. During WCDMA transmission conditions, HL\_TX\_EN will be in a high state. This will open both FETs in Q906, thus, disabling any signal functions from control lines NB\_EXC\_EN and N\_BAND\_0. Q901 is used to invert the control signal coming from Q906.

## 4-4 A835: GSM RX Front End



### Description

The EGSM, PCS and DCS signals must first pass through baluns before reaching the LIFE IC. Since the LIFE expects differential inputs, the baluns will provide this. Baluns provide the change from an unbalanced to a balanced line condition. By directly connecting to lines together, a possibility might arise where one line might ground a signal and impair the operation of a circuit. This situation is solved through the use of an un-balanced to balanced transformer, a balun. Expected nominal losses is  $\sim .5 - 1.0\text{dBm}$ .

The first IC in the EGSM, DCS, and PCS RX line up is U625 (LIFE), which is an LNA, VCO, and down converter mixer. The RX frequency is mixed down to a Very Low Intermediate Frequency (VLIF) of  $\sim 100\text{KHz}$ . This design is utilized to improve LO leakage causing RF self-mixing, DC offsets, and noise performance. The LIFE IC operates from the MAGIC\_LV (tracking regulator), MAGIC\_RF\_V2\_475, and MAGIC\_SF (isolated supply for the VCO).

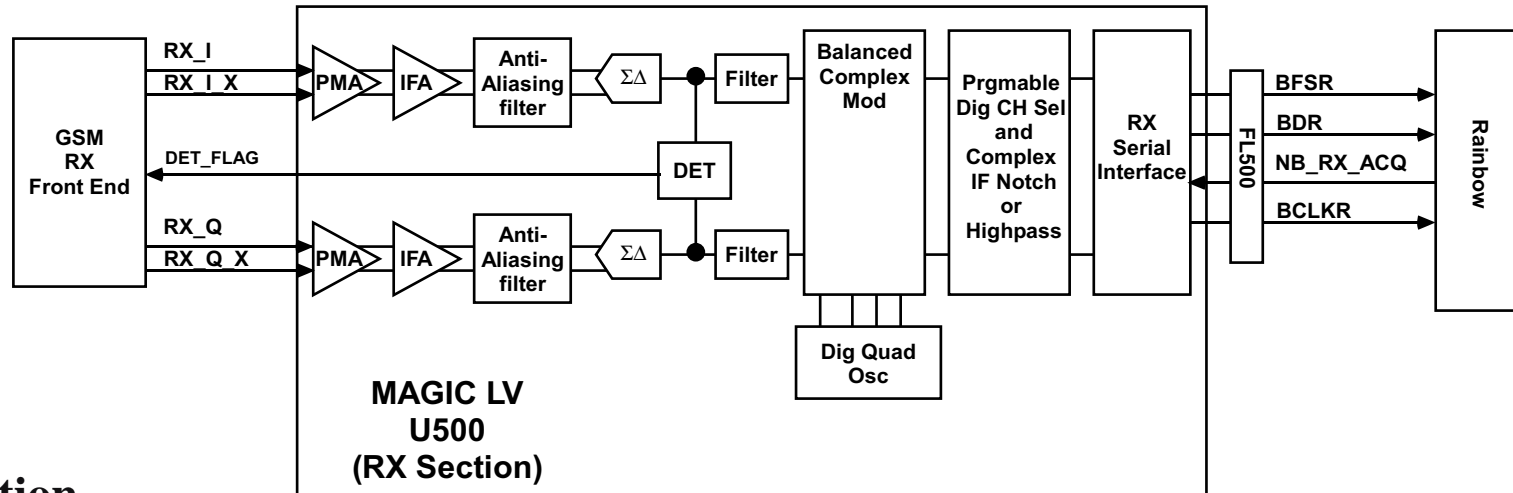
LIFE is comprised of four low noise amplifiers (three of which are used) with two quadrature mixer paths for use in receive GSM 900 (925- 960MHz), DCS (1805- 1880MHz), and PCS (1930-1990MHz) frequency bands, all SPI programmable. The RX\_VCO signal is fed back to the MAGIC\_LV prescaler input. Although the frequency will be dependent of the channel selected, the amplitude signal is  $\sim 30\text{dBm}$ .

LIFE contains three fully contained VCOs which operate at  $\sim 4\text{GHz}$ . These VCOs are internally divided to provide precise quadrature down conversion for the three frequency bands. The input signal RX\_VTUNE from the RX backend processor (MAGIC\_LV) selects the VCO frequency to operate at. The tune range is  $.5 - 4.5\text{V}$ . The VCO frequencies for the three technologies are: DCS 3610 - 35759MHz, EGSM 3700 - 3838MHz, and PCS 3859 - 3980MHz.

The AGC is provided by a common amplifier section, which is shared by all four LNAs. The AGC amplifier gain control is controlled by the voltage on the AGC pin, utilizing the internal 6-bit D/A to set the AGC via the SPI lines (SPIDATA, SPI\_CLK, and SPI\_CE). LIFE has an internal RF detector at the input of the AGC amplifier. The detected DC output level will be compared against a reference, which corresponds to the maximum safe input level to the mixer. This reference is SPI selectable so that the threshold can be set to 0dB, 3dB, 6dB, or 9dB below the level, which results in the mixer malfunction. If the detected level is above the reference then AGC\_FLAG will go high. The MAGIC\_LV will receive this signal as an interrupt and will reprogram the AGC until the level drops below the safe mixer input level as signified by AGC\_FLAG returning low.

The output signals I / IX and Q / QX are @  $\sim 100\text{KHz}$  IF value for the Very Low IF. The input pin, RX\_EN\_LIFE controls the on / off state of the receiver and the PLL circuits. For input amplitude at the antenna of  $-50$  to  $-40\text{dBm}$  the expected nominal output should be an AC rms peak-to-peak voltage of  $\sim 4.5 - 14\text{mV}$ .

## 4-6 A835: GSM RX Back End (Magic LV)



### Description

The MAGIC\_LV (U500) handles the backend processing for the EGSM, DCS and PCS (VLIF: RX\_I, RX\_I\_X, RX\_Q, and RX\_Q\_X) signal lines from LIFE. Simply, the MAGIC\_LV performs an analog to digital conversion of I/Q and sends it to the data to the board processor (RAINBOW) via the SSI (serial synchronous interface). The MAGIC\_LV also has a programmable and phase-able digital IF to improve image rejection.

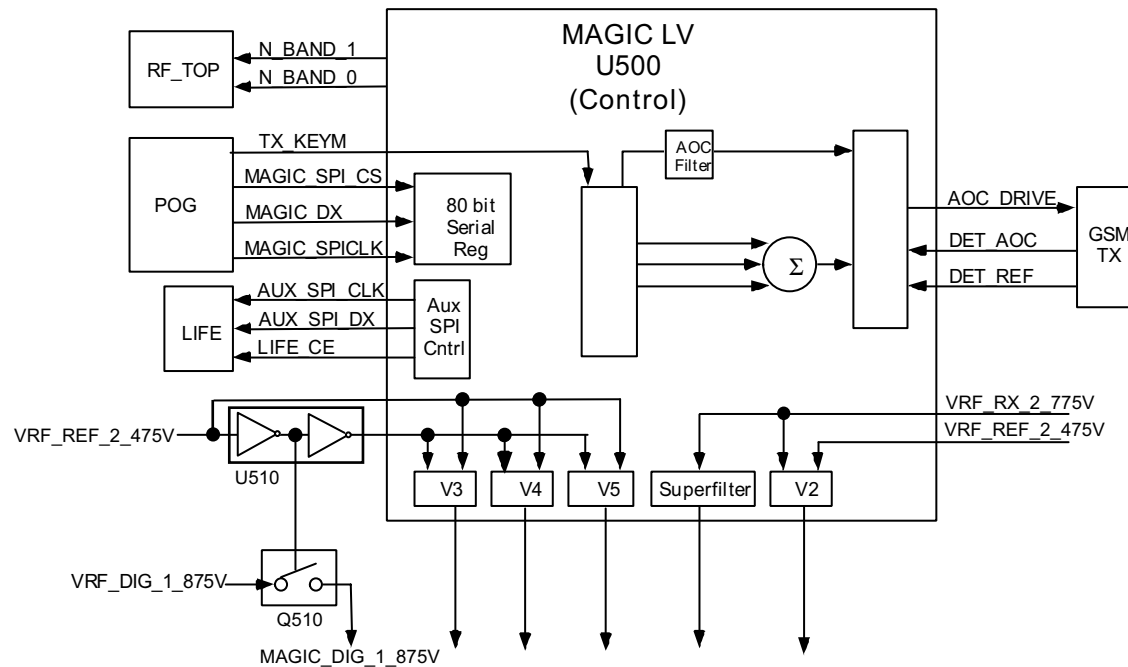
In MAGICLV, each channel is comprised of a Post Mixer Amplifier (PMA), an integrated passive two pole filter, a gain stage (AMP1) followed by an active programmable 2 pole anti-aliasing filter (mainly required to meet the blocking specs). This is followed by a lowpass sigma-delta ADC with a programmable oversampling clock OVSCCLK (derived from the reference oscillator) equal to 13MHz for 200kHz channel spacing (13bits).

Digital detector circuits are placed on each channel at the output of the sigma delta converters. The outputs of these detectors are compared against a level defined by DET\_LVL. If either of the detected levels exceeds the programmed threshold then the pin DET\_FLAG is set high. This indicates that the signal level is excessively high for the sigma delta modulator. DET\_FLAG is read by the processor, which will respond by re-programming one of the AGC settings to a lower gain until DET\_FLAG returns low.

The outputs of the sigma-delta modulators are digitally processed through a noise cancellation circuit, comb and decimation filters. A second programmable digital LO based on a look up ROM generates digital quadrature oscillators with programmable gain/phase correction (called balanced complex multiplier) to digitally downconvert the I/Q signals to baseband (digital zero IF) through four quadrature mixers that provide image rejection of adjacent/alternate channels. Gain/ Phase correction at a single baseband frequency is performed on the Digital Quadrature Oscillator to compensate the analog gain/phase mismatch of the quadrature I and Q paths. After baseband downconversion and image reduction, the quadrature I and Q signals are further processed by digital filters that perform channel selectivity and out of band noise rejection.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data in 2's complement format. BDR and BFSR are outputs from MAGIC LV. BFSR is a framing signal which marks the beginning of an I,Q transfer. BDR is the serial data. The clock used for the serial transfer is BCLKR. When NB\_RX\_ACQ goes high MAGIC LV will activate the SSI interface in the digital receiver section. The data transmission over the serial bus will begin at the next normal occurrence of valid I and Q data, as defined internally to the digital receiver.

## 4-8 A835: MAGIC LV Control Functions



### Description

The MAGIC LV contains 4 tracking regulators and one superfilter, which will generate the supplies for most of the IC as well as the front end and the main VCO. The tracking regulators derive their internal power from the REG\_REF pins. The reference voltages are filtered and buffered for use on the IC. The buffered voltages should track the references within +/-1.5%. A raw supply voltage is provided to the tracking regulators which is higher than REG\_REF as specified below for each regulator. A superfilter is needed for the external VCO power supply. This superfilter, cascaded with an external regulator and any filtering in front of the IC, will need to provide 80dB of rejection to a 0.1V step occurring at a 217Hz rate with a risetime of 20us on the raw supply (battery) and a duty cycle of 0.125. The superfilter will use an internal pass transistor that is capable of driving a 30 mA load with a voltage drop of less than 0.4V relative to SF\_SPLY from the SF\_OUT pin. An external 1uF cap is required on SF\_OUT. As the superfilter will track SF\_SPLY it will need to sense the power on reset and turn off even though its supply may remain active. All supplies within the IC must be within 5% of their final values after 5msec from the start of POR\_LB. The power on reset circuit contained within the crystal reference oscillator is used to aid this functionality.

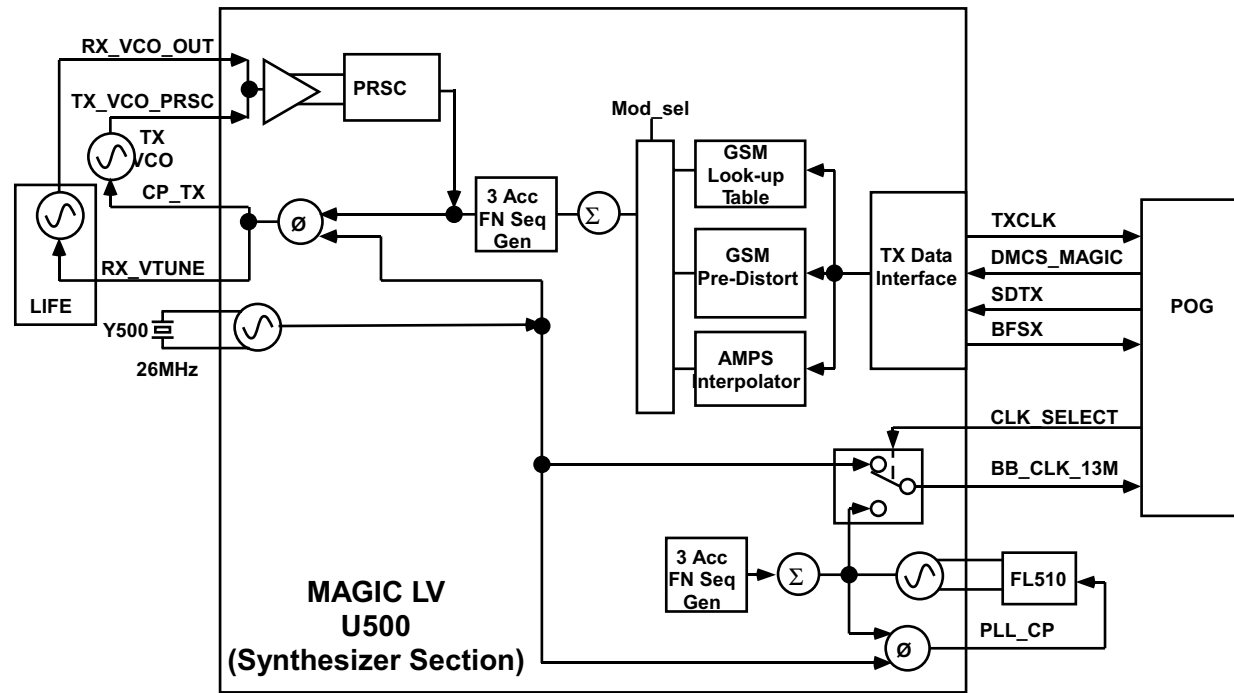
The MAGIC\_LV has two sets of SPI interfaces; one set is for handling the control interface for the LIFE IC (AUXSPI lines) and ones for interfacing with RAINBOW (SPI lines). AUX\_SPI\_DX is the serial data input line. AUX\_SPI\_CLK is the clock input line, where data shifting occurs at the rising edge of this signal. LIFE\_CE is the clock enable line, active high, for the LIFE IC.

MAGIC\_LV will integrate a system of D/As and control logic to generate the power amplifier control ramps. In addition, MAGIC\_LV will integrate the op-amps and comparators which receive the detected output of the power amplifier and create the necessary control voltage to drive the power amplifier control port based on the control ramps. When TX\_KEYM goes high, the ramp controller receives a positive input. This will cause the AOC\_DRIVE pin to linearly rise which in turn will cause the PA output power to rise. The rising PA output power will cause DET\_AOC to begin to rise until the DC level on DET\_AOC exceeds the DC level on DET\_REF by the intentional offset of the RF detector versus its reference. At this point the "Active Detect" comparator will go low and break the input voltage to the integrator with the ramp controller. This will cause the PA power to stop rising and hold the present power level as determined by the 8 bit offset value fed to the ramp controller. The PA control loop is now at a minimal power needed to keep the control system in a closed loop for a controlled ramp up of the power.

The MAGIC uses two SPI driven GPO lines which are used to control the operating bands of the GSM RF circuits. They are N\_BAND\_0 and N\_BAND\_1.

When the MAGIC LV is set to battery save mode it will shutdown the receiver analog sections (via RX\_EN\_LIFE), the AOC, the main synthesizer and the superfilter.

# 4-10 A835: MAGIC LV (Synthesizers/Transmitter)



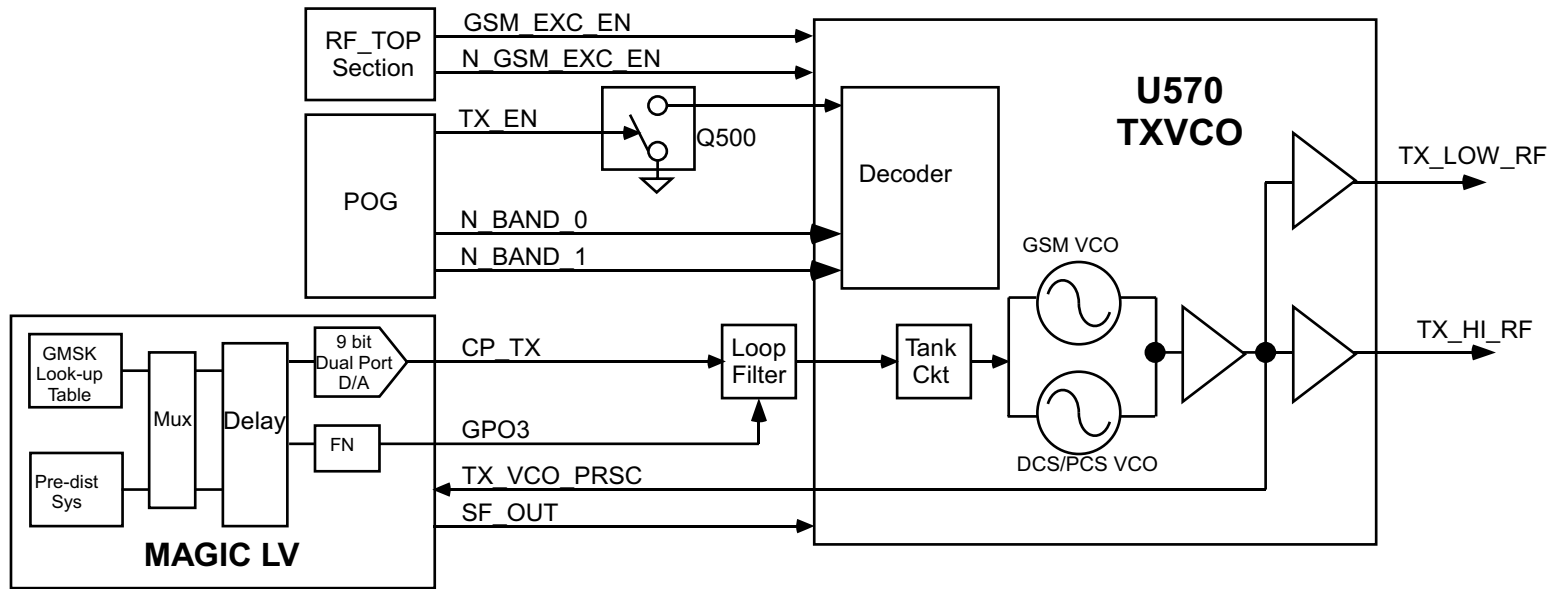
## Description

The MAGIC\_LV receives SSI Tx data at DMCS (digital input to start Tx modulation), TXCLK (clock for serial transfer) and SDTX (serial Tx data) from POG. The present serial data bit and the three previous data bits are used to set up one of 16 possible waveforms based on the sum of Gaussian pulses stored in a look up ROM. The resulting signal will then be clocked out at a 16x over-sampling rate. This data pattern input to three-accumulator fractional N synthesizer with a 24-bit resolution. The VCO control lines must have compliance over an output voltage range of 0.3VDC to  $V_{cc}-0.3V$ . The charge pumps will have their own supply pin. The voltage on this pin is expected to be 2.775V typically to obtain sufficient compliance. This will drive external loop filters, which will in turn drive external VCOs. A dual port modulation mode is obtained with a 9 bit D/A which follows the modulation look up table output waveform is output on the GPO3 pin. This signal is then coupled into the loop filter to add in the higher frequency components of the modulation which may have been attenuated in the main PLL path. This will allow the use of a lower bandwidth main PLL to improve the spectral purity of the transmit signal. For EGSM the synthesizer output is 880 - 915MHz, DCS is 1710 - 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

The prescaler for the main LO is able to accept input frequencies as high as 2.0GHz. The level of this signal shall be between -20dbm and -10dbm. There are two prescaler inputs to this point each has a 100W resistor in series between the pin and the actual prescaler input.

The reference oscillator is a free running 26MHz crystal. AFC is provided through the SPI bus as a programming offset to the fractional N division system. Since the 26MHz crystal is not locked to the AFC, a second fractional divider system is necessary to derive an accurate 200KHz system reference. This reference is then multiplied in a PLL to 13MHz for use as an accurate clock to the logic sections of the transceiver.

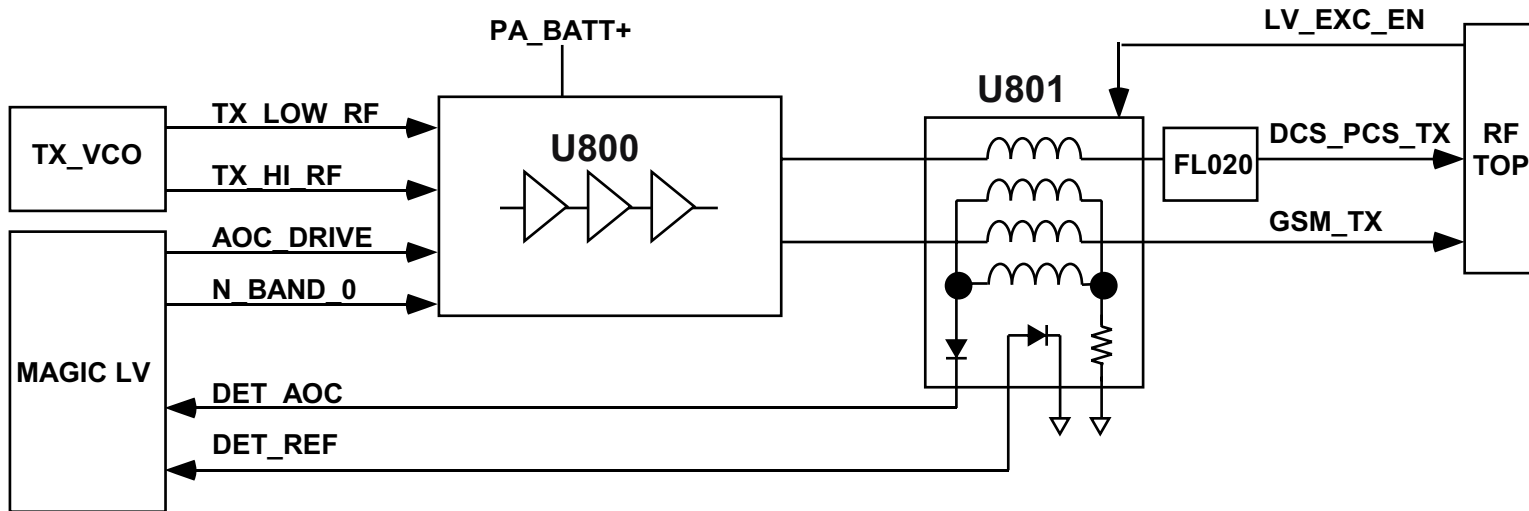
# 4-12 A835: GSM TX VCO



## Description

The VCO frequencies are 897 - 1880MHz, handling the three technology bands. The technology bands are controlled by MAGIC\_LV via the data lines: N\_BAND\_0 and N\_BAND\_1. CP\_TX and GPO3 provides a dual port modulation mode for the TXVCO. N\_BAND\_0 and N\_BAND\_1 will select which VCO band will be activated. GSM\_EXC\_EN and N\_GSM\_EXC\_EN will enable the buffer stage of U570. TX\_EN is activated prior to enabling the buffer and PA. TX\_VCO\_PRSC is fed back to the MAGICLV for proper PLL operation. The output frequency for GSM is TX\_LOW\_RF and PCS / DCS is TX\_HIGH\_RF. The charge pump output (CPTX) from MAGIC\_LV is the input (VT) for the VCO.

# 4-14 A835: GSM PA

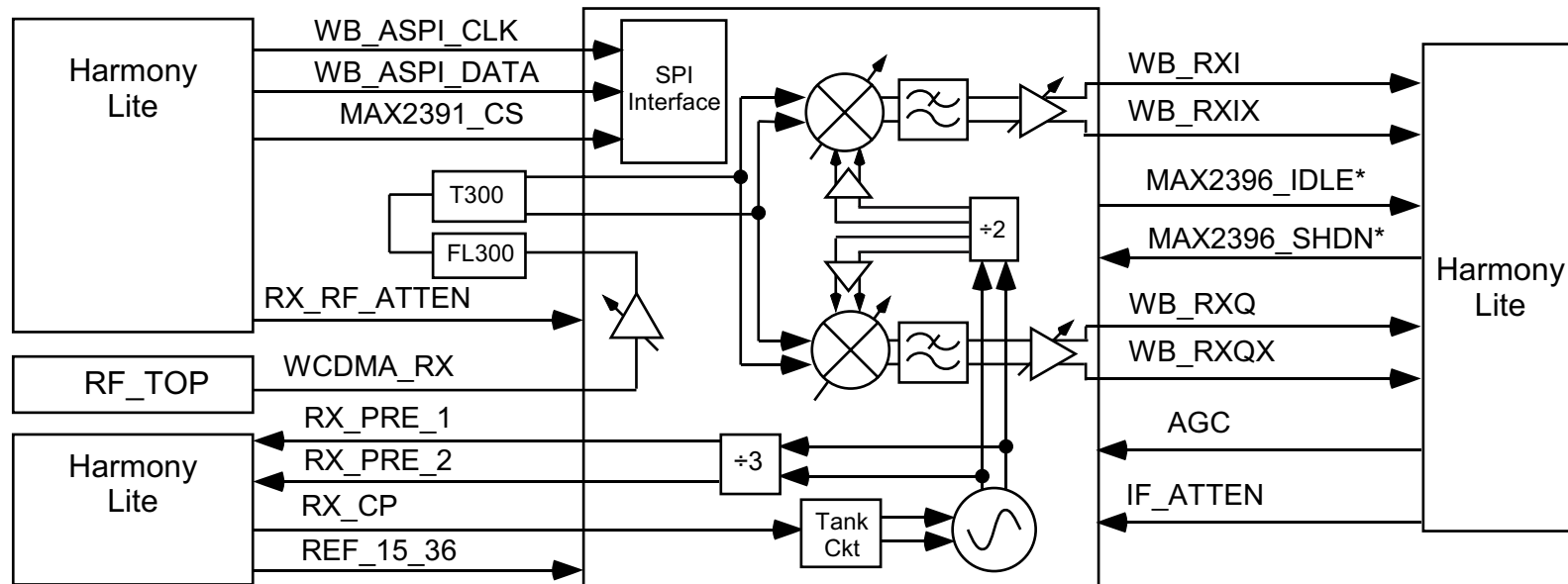


## Description

U800 is a tri-band PA module that operates in EGSM, DCS and PCS bands. The nominal expected maximum gain is ~30dB. . The AOC\_DRIVE input from MAGIC\_LV controls the PA output. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases. N\_BAND\_0 is used to select the operating band. LV\_EXC\_EN will enable PA operation.

The power detector receives the amplified GSM signal at #1 (EGSM\_IN), PCS and DCS at pin #12 (DCS\_PCS\_IN) from the U800. U801 is a dual combination directional coupler and temperature compensated power detector output. The power detector couples the Tx power input and feedbacks an output DET\_AOC to MAGIC\_LV. A comparator within the MAGIC LV will sample DET\_AOC and based on the power amplifier ramps will provide any necessary control voltage adjustments to AOC\_DRIVE. The DET\_REF is a reference voltage to MAGIC\_LV. Expected nominal loss is < 3dB.

## 4-18 A835: WCDMA Zero-IF Receiver (MAX2396)



### Description

The Max2396 (U300) is a fully integrated direct-conversion receiver IC family for WCDMA applications, targeting the emerging 3GPP market.

The Max2396 provides a complete solution for the 3GPP WCDMA FDD receiver (2110-2170MHz, 3.84Mcps) from antenna to baseband I/Q outputs, eliminating the use of an off-chip IF SAW filter and of RFVCO.

The MAX2396 receiver IC has over 90 dB of dynamic gain control, partitioned between RF and baseband sections. It consists of an ultra-low current LNA with on-chip output matching and two-step gain modes. The zero-IF demodulator has a differential circuit topology for best input IP2 and for minimum LO leakage to receiver's input. The channel selectivity is done completely in the baseband section of the receiver with an on-chip low-pass filter. The AGC section has over 50dB of gain control range. LO quadrature generation is done on-chip through a divide-by-2 prescaler. The DC-offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop connected over the AGC section. For large DC-offsets transients, very fast settling time is obtained by automatic optimization of the time-constant of the DC-offset cancellation circuit.

The AGC ensures that the I/Q inputs to HARMONY LITE are at constant signal level. The IF\_AGC line is controlled by HARMONY\_LITE with a DC control range of 1.2V to 2.1V.

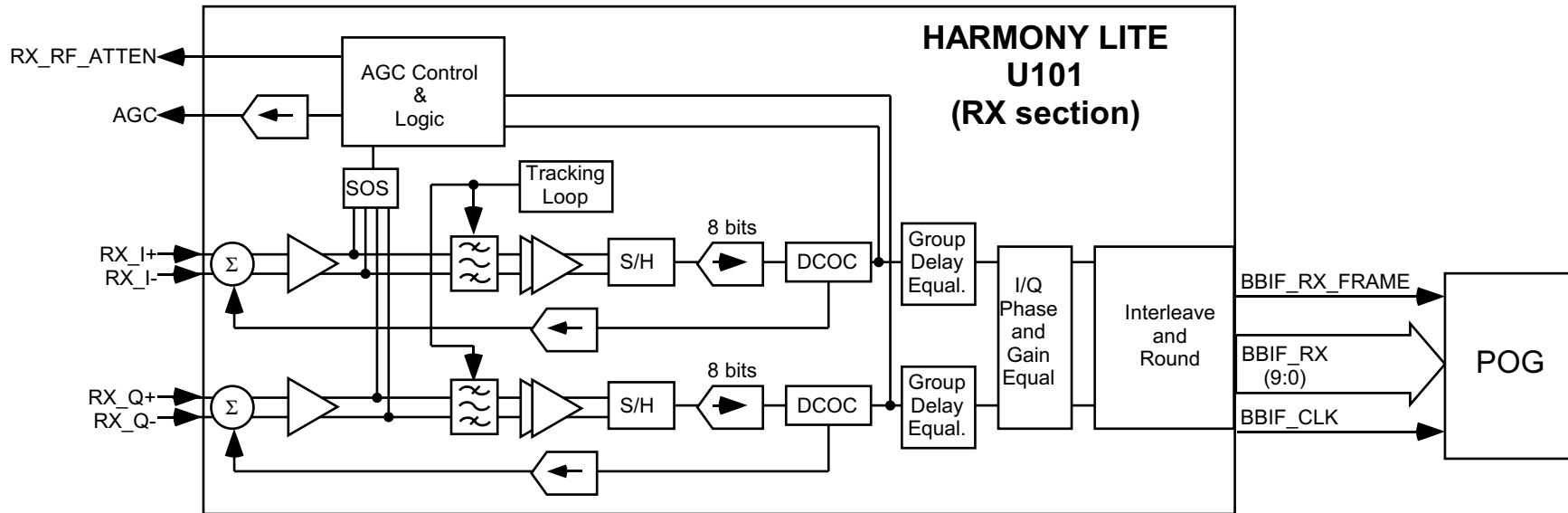
The MAX2396 includes a 3-wire serial bus for PLL programming and for configuring the different receiver modes. The MAX2396\_SHDN\* line is used for full device shutdown and the MAX2396\_ILDE\* line is used for device idle mode.

RX\_RF\_ATTEN controls the LNA gain control pin of the MAX2396(U300), allowing high gain mode operation for low RF signal conditions and low-gain mode for high RF signal conditions. IF\_ATTEN controls the mixer gain control pin of the MAX2396, allowing high gain mode operation for low IF signals and low gain mode for high IF signals.

The MAX2396 VCO frequency is controlled by an external phase lock loop (PLL) synthesizer found in the Harmony Lite. The VCO output frequency at RX\_PRE\_1 and RX\_PRE\_2 is through a divide-by-3 prescaler. The VCO output signal is then fed into the PLL synthesizer found in the Harmony Lite. The internal phase detector within Harmony Lite drives the charge pump, RX\_CP. The RX\_CP line drives the tunable resonant network, altering the VCO frequency and closing the loop.



## 4-20 A835: Harmony Lite (Receive Section)



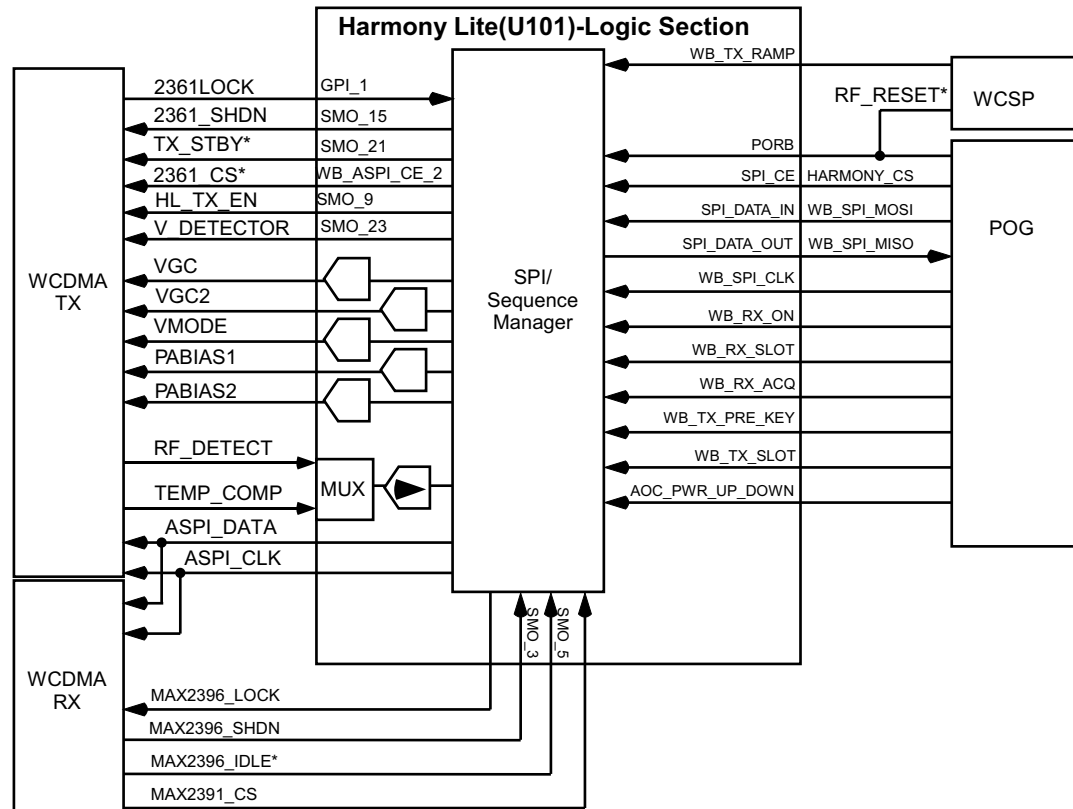
### Description

The HARMONY LITE (U101) handles the backend processing of the WCDMA in phase (RX\_I+, RX\_I-) and quadrature (RX\_Q+, RX\_Q-) signals from the demodulator. The HARMONY LITE performs an analog to digital conversion of gain, phase and DC offset correction of the RX data and sends it to the POG (U1000) via data lines BBIF\_RX(9:0).

The analog I and Q signals are applied to the Harmony Lite IC, which processes the analog baseband portion of the radio. The SOS detector is used as an off-channel detector to detect the level of undesired interfering signals. It monitors the voltage swing at the input to the baseband filters, and provides a logic level output to the AGC/RSSI controller to indicate if the level is greater than a threshold specified by SPI bits, which then sets the appropriate gain setting in the front-end and IF stages. The AGC system provides overload protection for both the strong on-channel signal and the off-channel portion of the signal (interferers) that is present in the RF receive band. Signal levels are detected at the baseband filter inputs of the Harmony Lite (off-channel detector) as well as after the channel filtering and analog-to-digital conversion (on-channel detector). The digital AGC/RSSI block controls the bypass mode of the LNA and the IF variable gain amplifier. A digital representation of the desired received signal strength is sent to the POG via the SPI.

Low pass filtering is performed on the complex I and Q signals, and then applied to the associated 8-bit ADCs and sampled at a rate of 4 times per symbol. A DC offset correction loop corrects for any DC offsets at the I and Q ADC inputs. A group delay equalizer is employed in the receive signal path following the baseband SRRC filter to minimize performance loss from the analog active order SRRC channel filter. Gain and phase mismatches between the I and Q channels can affect the detectability of a WCDMA signal in static and multipath fading conditions due to distortion caused in the QPSK signal constellation map. Thus, I/Q magnitude and phase imbalance correction circuits are used. At the output of the Magnitude Equalizer, the I and Q values are rounded from 8 bits to 6 bits and then multiplexed and routed to the digital signal processing circuitry located on the POG IC.

# 4-22 A835: Harmony Lite (Control Section)



## Description

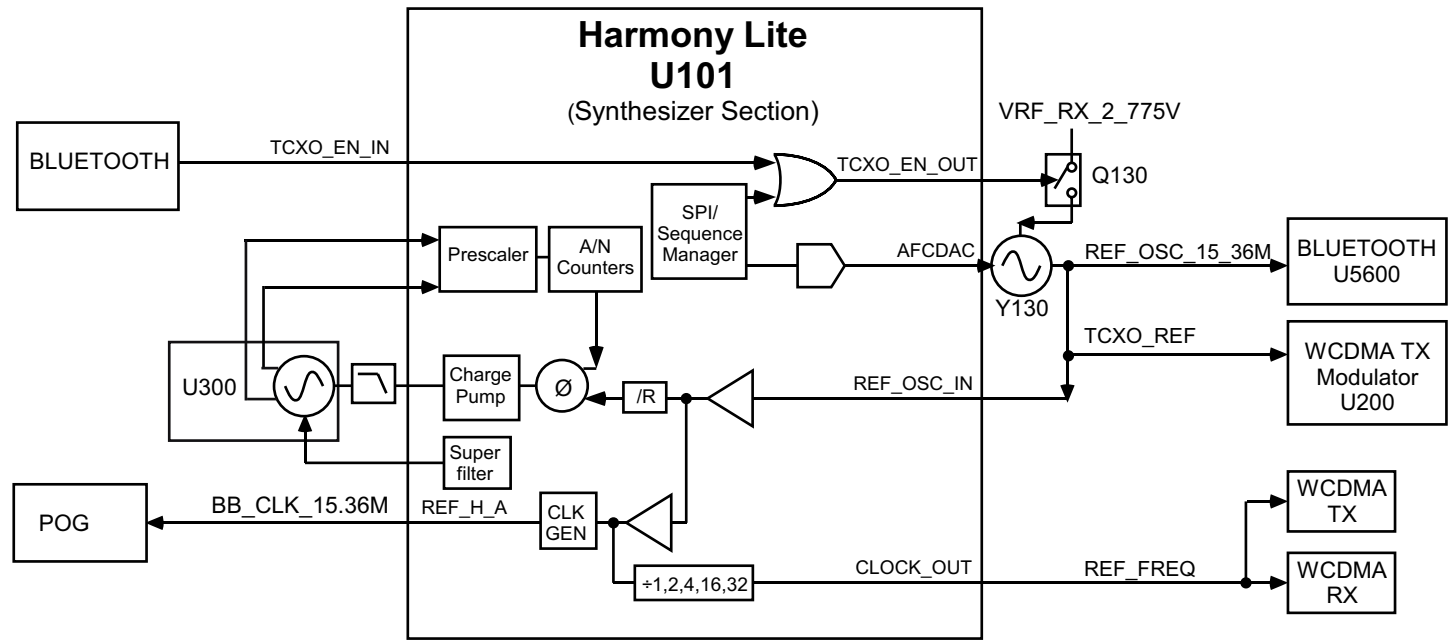
There are several functions that the sequence manager is controlling.

1. Sequence manager outputs to external devices
2. On/Off control of clocks, battery save signals etc...
3. Clock frequency selection for correction paths
4. DCOC register selection coarse, medium and fine modes

The HARMONY LITE has two sets of SPI interfaces; one set is for handling the control interface for the transceiver (AUXSPI lines) and ones for interfacing with POG (SPI lines). Further, all SPI interface is generated from POG and written to HARMONY\_LITE or parsed through to the MAXIM (U200 & U300) parts.

Layer one timing signals control the functionality of the RF section of the transceiver relative to the air interface. There are three signals defined on each transmit and receive section of the transceiver. TX\_PRE\_KEY and RX\_ON are asserted before the need to receive or transmit in order to launch the necessary sequence of events to warm up the required functional blocks. TX\_RAMP and RX\_AQUIRE are asserted when actual transmission and reception are to begin. RX\_SLOT and TX\_SLOT are used during continuous transmission and reception to trigger events that must be aligned with slot boundaries. It's important to reiterate, the TX\_RAMP directly corresponds to the PA turning on and RX\_AQUIRE corresponds to data being sent to the WCSP.

## 4-24 A835: Harmony Lite (Synthesizer Section)



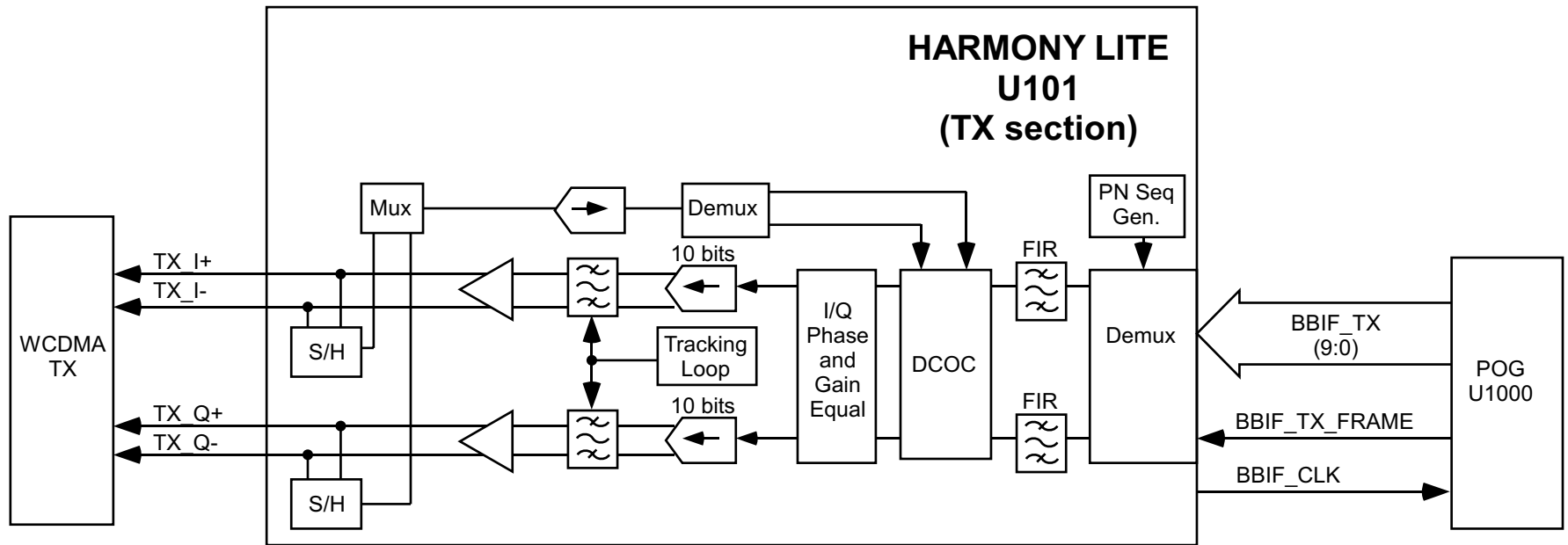
### Description

The clock source for the Harmony Lite (HLite) is a 15.36Mhz oscillator (TCXO). Y130 is used to generated the 15.36MHz clock source. AFC for Y130 is controlled by the Harmony Lite sequence manager via the AFCDAC line. The 15.36MHz clock source is enabled by an internal SPI bit and external control signal coming from 15.36M\_CLK\_EN\*). The 15.36MHz clock source provides clocks to all A/Ds, DACs, external references and internal digital circuits of the Harmony Lite. In addition, clock references are generated for the RAINBOW, WCSP, RX and TX RF circuits.

The WCDMA VCO, integrated in U300, has a frequency range of 2.3G thru 2.36GHz, supplying the receiver with an LO. The LO signal is generated for the receiver by using a phase locked loop (PLL) architecture integrated in the Harmony Lite. The phase locked loop uses a fractional loop divider to permit fast lock times and low phase noise on the output signal. The control range is controlled by HARMONY\_LITE with a control range between 0.5 - 2.5V, with an output power @ ~-3 - 3dBm. The VCO output frequency is fed into a prescaler and divided down into a desired comparison frequency. The 15.36MHz reference frequency is also divided down into a comparison frequency. The two divided frequencies are then compared with a phase detector. The phase detector will then drive the charge pump. The charge pump output is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency and closing the loop.

The superfilter block is used to provide a filtered supply voltage to the WCDMA VCO.

## 4-26 A835: Harmony Lite (TX Section)



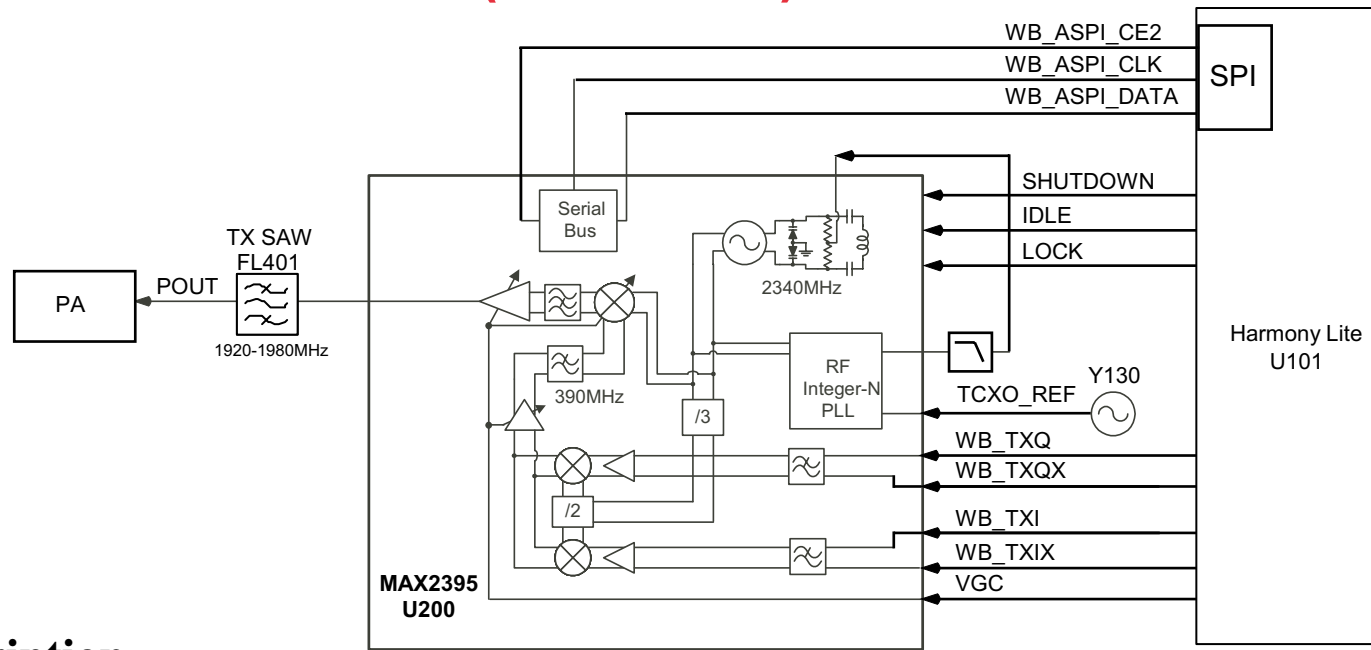
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### Description

The BBIF(BBIF\_TX) is the transmit data path for transferring digitally sampled I / Q data from the POG. The demultiplexing unit performs the I/Q deinterleaving function to supply separate I and Q channel data into the transmit FIR filters. The FIR filter design is used to meet 3GPP spec requirements of simultaneous transmission of a pilot channel and of multiple data channels each requiring a different spreading code and each requiring separate power control. The PN sequence generator provides I/Q interleaved 8-bit PN data into the demultiplexing section. The DC correction(DCOC) block is able to correct for DC offsets due to the D/A's, anti-aliasing filters, and transmit FIR filters in a feedback control loop. A mixed mode control loop located at the output of the transmit FIR filter is employed to correct DC offsets and I/Q gain imbalances, i.e. DCOC and I/Q Phase and Gain equalizer. The outputs of the I/Q gain equalization unit is fed into 10-bit I and Q DAC's. The programmable gain anti-aliasing filters, or TX smoothing filters, accepts differential I/Q signals of DC to 1.92MHz frequency components from the D/A Converters to attenuate the unwanted clock signals of 15.36MHz and to smooth the signals for the TX modulator(MAX2363). The output of the TX smoothing filters are then fed into a multiplexed 6-bit A/D with sample/hold scheme. This gives the information of the amplitude and the DC common mode voltage from the I / Q Tx filter outputs by a single Analog-to-Digital Converter (ADC) as the part of digital correction loop.

The differential TX I and TX Q signal are finally fed into the TX modulator(MAX2363).

## 4-28 A835: TX Modulator (MAX2395)



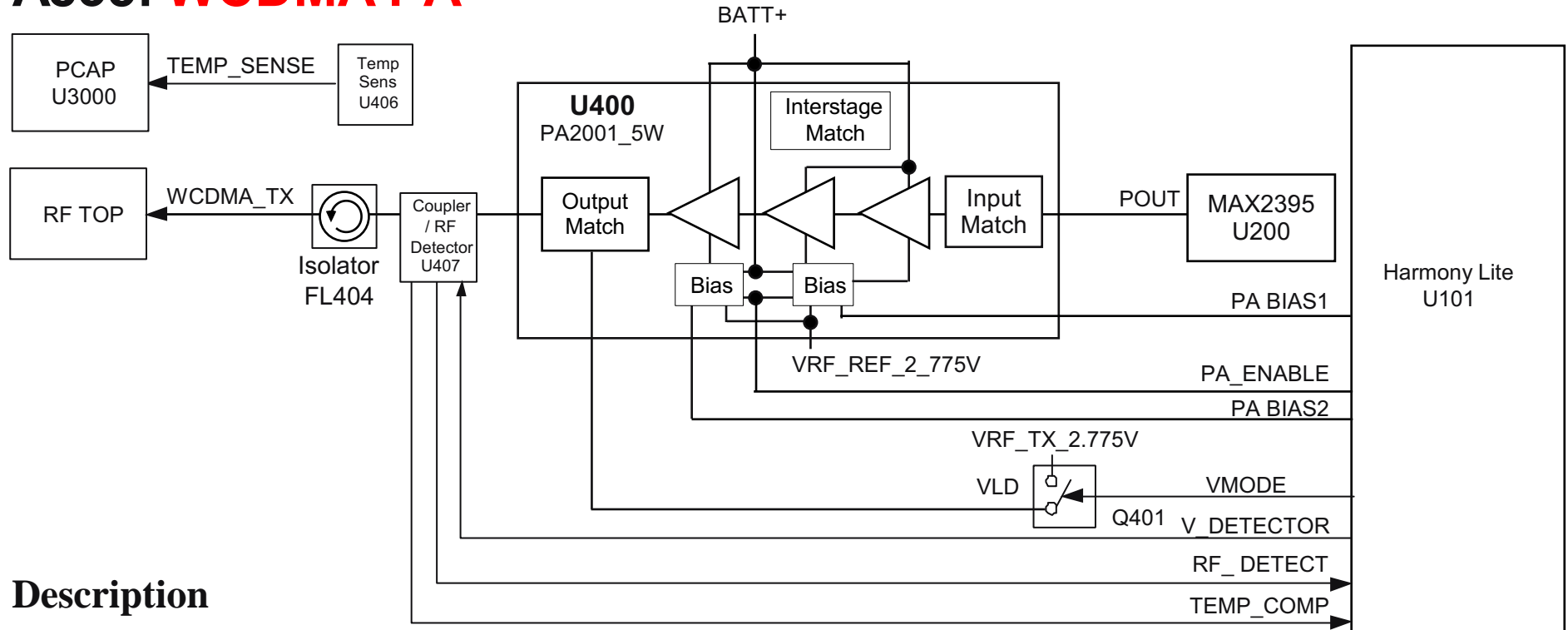
### Description

The MAX2395 is a fully monolithic quasi-direct modulator IC for use in WCDMA/UMTS transmitters. The quasi-direct modulation architecture reduces system cost, component count, and board space compared to transmitters using IF SAW filter with IF VCO and IF synthesizer blocks.

The MAX2395 includes I/Q baseband filters, an IF I/Q modulator with VGA, a fully monolithic VCO with PLL, a up-converter mixer with VGA, and a power amplifier driver. The differential baseband I/Q signals are modulated onto a variable-IF carrier in the 384 396MHz band; The IF signal is then up-converted to the 1920 - 1980MHz band. On-chip Image rejection in the 2688 - 2772 MHz frequency band is done with an integrated notch filter. The RF VGA and IF VGA provide a nominal 90dB of output power control. The use of the quasi-direct modulator scheme ensures excellent carrier suppression over the total power control range. In addition, only one on-chip VCO and one integer-N PLL are needed to generate both LO signals for the IF and RF sections. The on-chip component matching by monolithic integration at IF frequencies results in excellent phase accuracy and amplitude balance.

The PLL operation is programmed by loading data on the SPI/Microwire compatible 3-wire serial bus. In addition, the WCDMA required compressed mode can be selected via an external IDLE pin. The IC operates from a single 2.7V - 3.3V supply.

# 4-30 A835: WCDMA PA



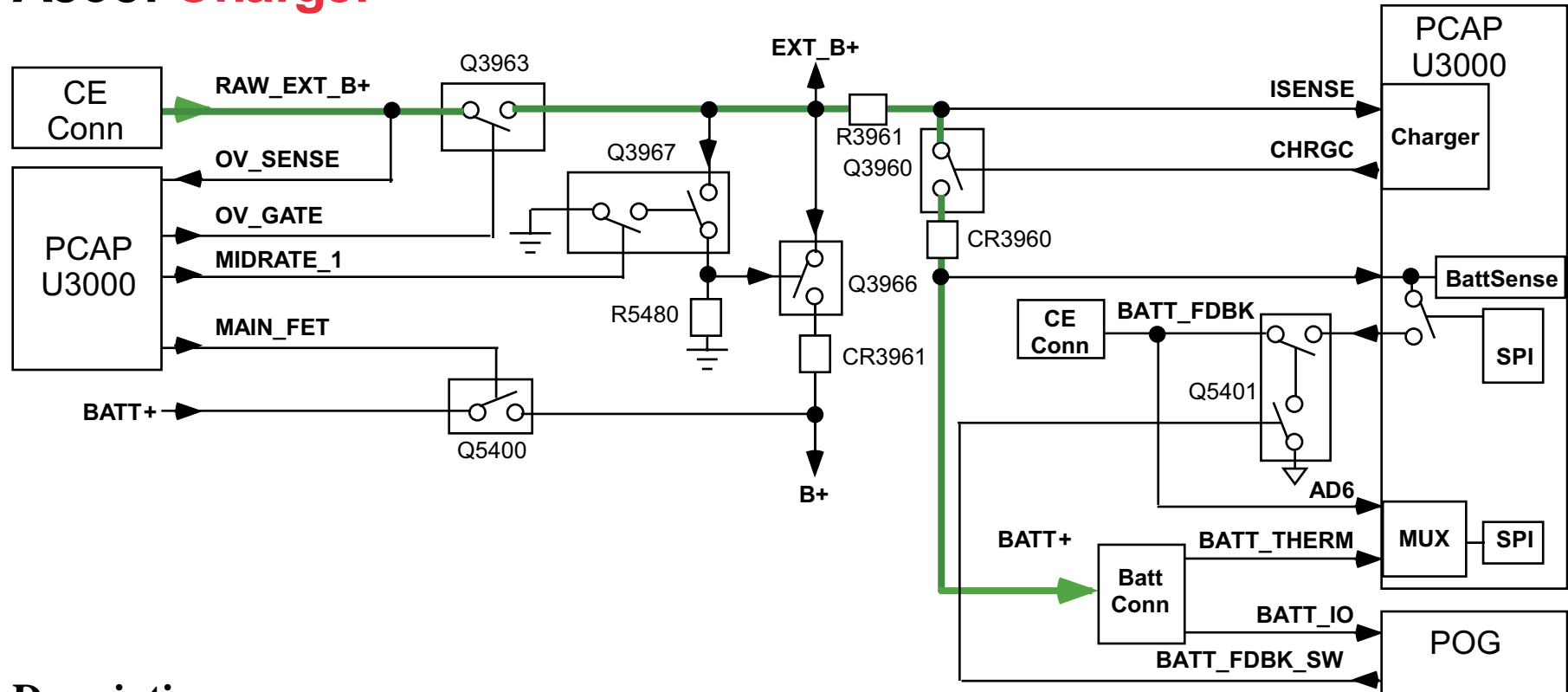
## Description

U400 is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 - 1980MHz. The nominal expected maximum gain is ~30dB. HARMONY\_LITE controls the RF biasing of the amplifier at PA\_BIAS1 and PA\_BIAS2 with a control range of 0 - 2.5v. HARMONY\_LITE also controls VLD for PA load switching. PA load switching in WCDMA is vitally important to conserve battery life and to avoid unnecessary radio interference with base stations. When VLD is at a low state (0v), the transmitter is in high power mode, consuming higher current but with overall better PA performance. When VLD is at a high state, the transmitter is in low power mode, consuming less current with overall poor PA performance. In theory, as the Tx power level increases or decreases beyond a certain power threshold, VLD is enabled or disabled. As Tx power decreases (as requested from a base station) down to ~14.5dBm, VLD will switch high. If Tx power is requested to increase beyond ~19dBm, VLD is switched low.

The power detector receives the amplified WCDMA RF signal at RF\_IN from the PA. U407 is a combination directional coupler and temperature compensated power detector with a differential output. The power detector couples the TX power input and feedbacks an output RF\_DETECT to HARMONY LITE. The TEMP\_COMP also obtains the coupled power but removes the RF signal content, leaving a DC level. The DC level is feedback to HARMONY LITE. Expected nominal loss is < . 3dB.

The isolator (FL404) provides isolation between Front-End Module (FEM) and transmitter path. Nominal insertion loss is ~ 0. 55dB.

# 4-32 A835: Charger



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## Description

The majority of the charging circuit is integrated in PCAP. This includes a digital to analog converter, analog to digital converter, battery feedback switch, thermistor switch/pullup, and current control sense. External FETs (Q3966 and Q5400) are provided to enable/disable EXT\_B+ and BATTERY supply paths to radio circuitry (B+). An external sense resistor (R3961) and a charging FET (Q3960) are provided to control charging current between EXT\_B+ and BATTERY.

Due to pin count constraints on the CE bus, the Charger Identification input signal and Battery Feedback output signal share the same accessory connector pin. Software will first detect the Charger ID Voltage (AD6) before enabling the Battery Feedback Voltage via the Battery Feedback Switch in PCAP. The Battery Feedback switch must not be enabled at any time for an accessory that is not a valid Fast Charger.

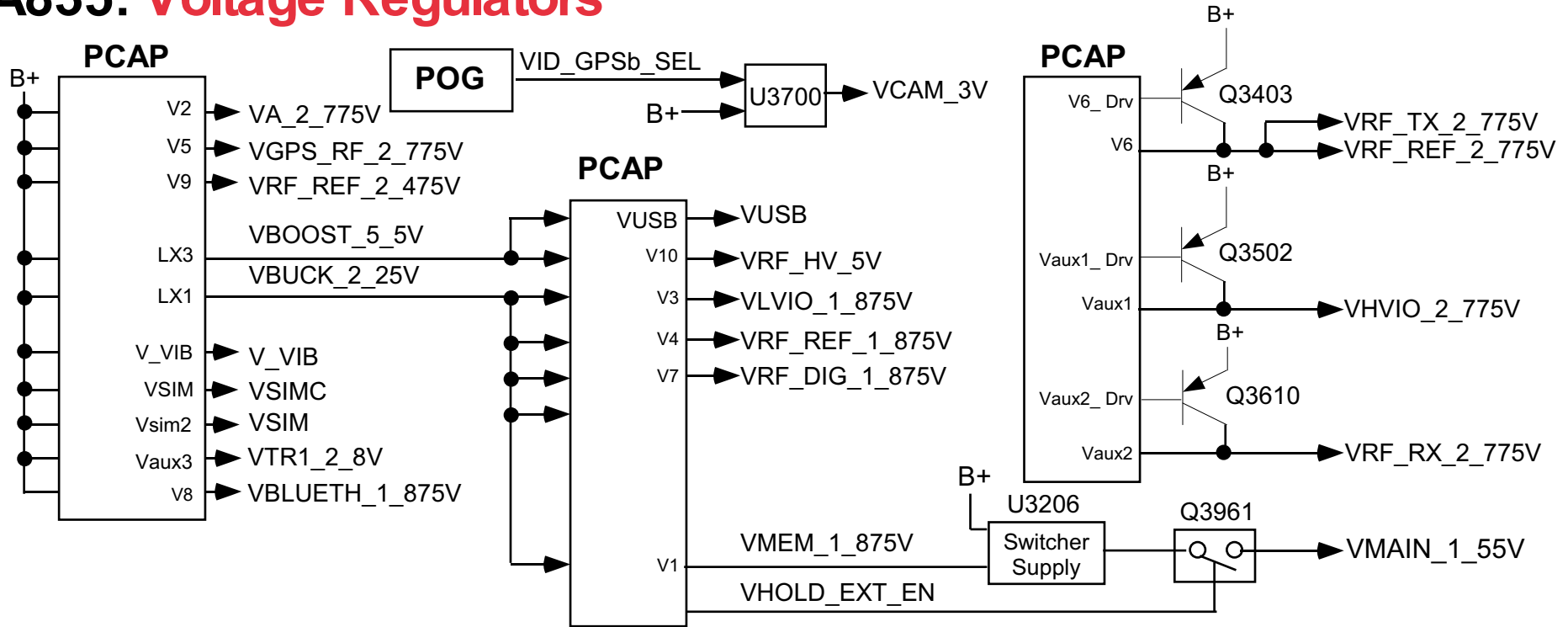
Battery Feedback Voltage provides a reference voltage to the external power supply during charging. The battery feedback switch is needed to remove the battery feedback voltage from the feedback loop of the AC/DC Adapter or VPA when charging is complete or after a fault has occurred. This switch will be enabled before the charger DAC is programmed when charging is to begin. Battery feedback will turn on before the charger is enabled. The charger will be turned off before battery feedback is disabled.

A thermistor in the battery package is used to determine cell temperature of the battery pack before charging begins. The battery EPROM (BATT\_IO) will contain limit parameters that determine the minimum and maximum temperatures at which charging can occur.

PCAP has an integrated over-voltage detection circuit that provides protection against damage caused by external charger voltages exceeding 7.0Vdc. If an over-voltage condition occurs, the EXT\_B+ FET (Q3963) will be disabled. This will prevent high voltage (>7Vdc) from being applied to radio circuitry (B+).

Mid-rate charging is supported if a valid mid-rate charger and valid battery are detected. A mid-rate charger will source up to 400mA of current to the radio circuitry and charging circuitry during idle mode. The mid-rate charger will supply 5.9Vdc (up to 400mA) to the phone, regardless of the BATT\_FDBK voltage. If the phone is in transmit mode, mid-rate current will be supplied to the battery and radio circuitry via the charging path only (EXT\_B+ FET (Q3966) will be disabled via the MIDRATE\_1 line). Dead battery TX operation or 'No Battery' operation is not supported with a mid-rate charger.

# 4-34 A835: Voltage Regulators



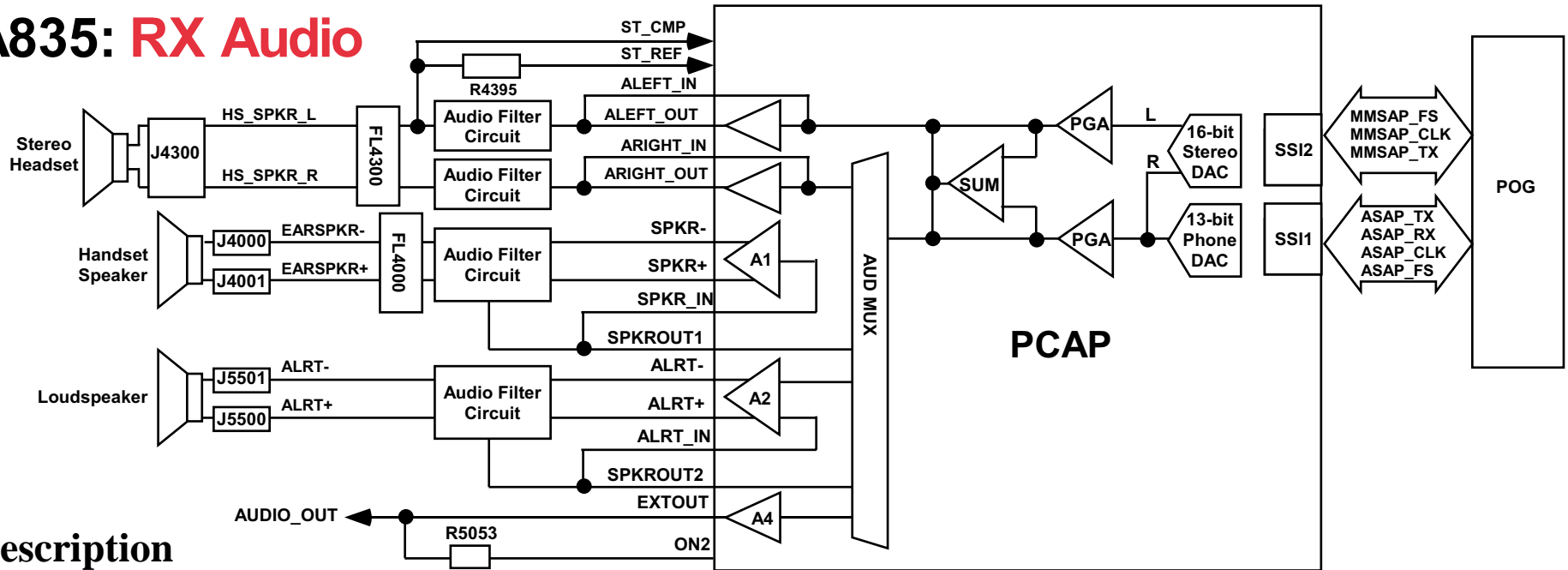
## Description

Voltage regulation is provided by the PCAP IC (U3000). Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are described below:

- VBOOST\_LX(VBOOST\_5\_5V) - VUSB and V10 input voltage regulator
- VBUCK\_LX(VBUCK\_2\_25V) - V1, V3, V4, and V7 input voltage regulator
- V\_VIB - Vibrator
- Vsim2(VSIM) - SIM card interface
- Vaux1(VRF\_TX\_2\_775V) - HV I/O, Display(20), Imager(12), GPS Baseband(8), GPS Flash,
- Vaux2(VRF\_RX\_2\_775V) - RF RX circuits
- Vaux3(VMMC\_2\_8V) - SD Flash
- VUSB - PCAP USB xcvr
- V1(VMEM\_1\_875V) - Baseband Processor Flash Core
- V2(VA\_2\_775V) - Audio
- V3(VLVIO\_1\_95V) - Magic LV I/O,
- V4(VRF\_REF\_1\_875V) - RF reference
- V5(VGPS\_RF\_2\_775V) - GPS RF
- V6(VHVIO\_2\_775V) - RF TX circuits
- V7(VRF\_DIG\_1\_875V) - RF digital
- V8(VBLUETH\_1\_875V) - Bluetooth
- V9(VRF\_REF\_2\_475V) - RF Reference
- V10(VRF\_HV\_5V) - RF HV



# A835: RX Audio



## Description

Receive audio data is transferred from the POG to the PCAP through the ASAP interface for mono audio and the VSAP interface for stereo audio data. The data is then converted into an analog form through a 16-bit Stereo DAC or 13-bit phone DAC. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins SPKR- and SPKR+, they are routed through R4004 and R4005 respectively, and then connected to the transducer. Off the SPKR- path, SPKR\_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR\_OUT1 from PCAP is routed through C4000 and C4002 to SPKR- which is the DAC output of the CODEC. SPKR\_IN and SPKR\_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

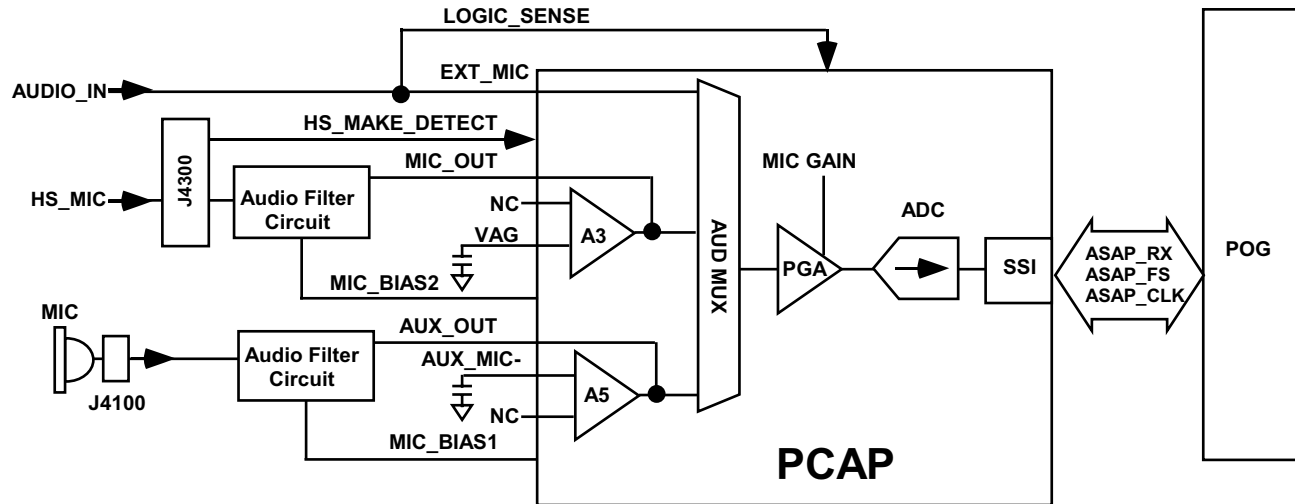
The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS\_SPKR\_L of the headset jack, which is pulled high by R4395 and connected to the ST\_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight\_Out and ALeft\_Out, they are routed through C4356, R4352 and C4306, R4302 respectively, and then connected to the headset jack. Off the ARight\_Out path, AR\_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ALeft\_Out path, AL\_IN is tapped off through C4304 for the inverting input of the audio amp ALEFT.

The External Speaker is connected to pin 15 of J5000 (AUDIO\_OUT), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio\_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio\_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio\_Out line, the phone will toggle it's ON/ OFF state.

The Loudspeaker is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT\_IN is routed through R4201 for the inverting input of the alert amp A2. SPKR\_OUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

## 4-38 A835: TX Audio



### Description

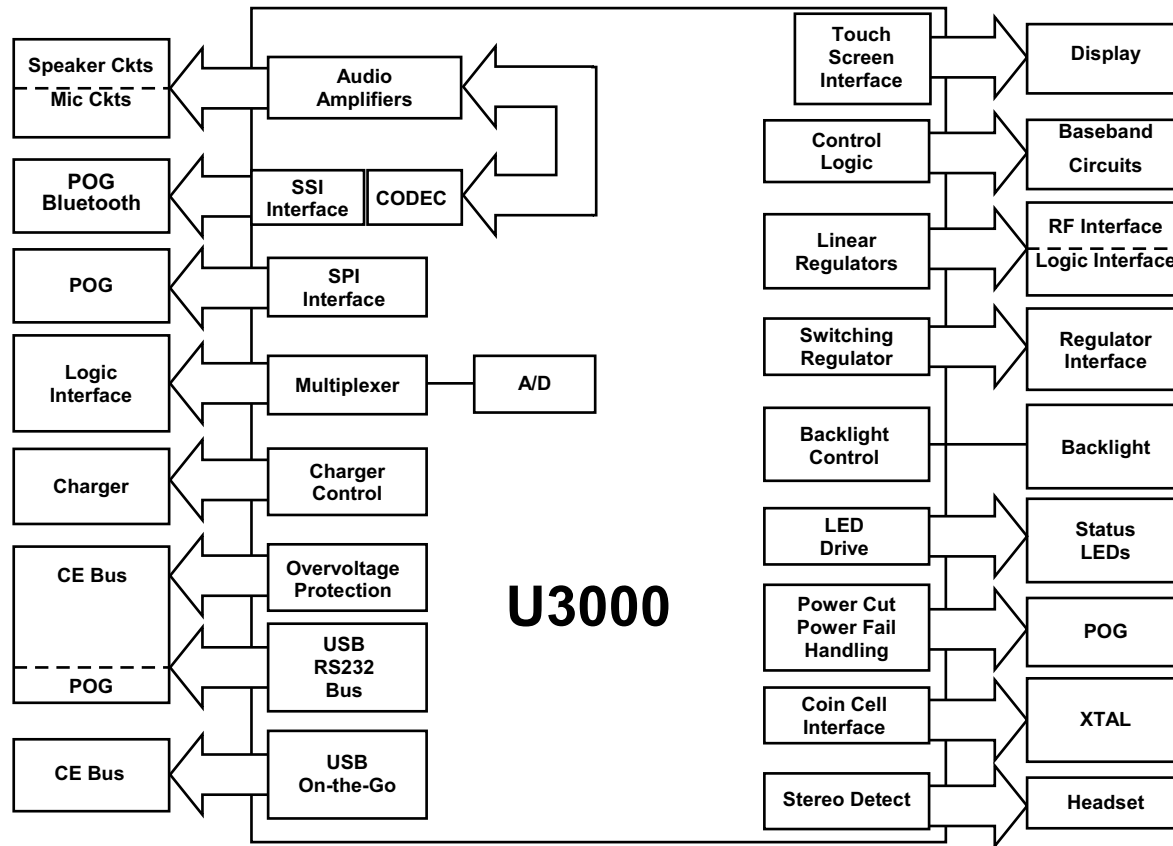
The Internal Microphone is a single ended part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC\_BIAS of 2.0V from pin MIC\_BIAS1 of PCAP. C4198 is connected to MIC\_BIAS1 and MB\_CAP1 pin on PCAP to bypass the gain from the VAG to MIC\_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 to AUX\_OUT pin on PCAP, bypassing the input to the A5 amplifier.

The headset microphone path (HS\_MIC) is biased through R4396 and R4392, which is connected to pin MIC\_BIAS2 on PCAP and bypassed with C4199 connected to pin MB\_CAP2. From here the signal is routed through C4395 and R4388 to MIC\_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC\_IN- input to R4389 connected to the MIC\_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS\_MAKE\_DET line monitors the presence of a headset by detecting the voltage at A1\_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS\_MAKE\_DET path to ground, depending on whether the headset is attached or not.

The External Microphone input (AUDIO\_IN) is connected to the accessory connector for the mobile phone. The path is routed through L4400, C4401 and R4401 to the EXT\_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage. In addition to audio signals, AUDIO\_IN supports detection of accessory devices. The accessory attached to the CE bus shall have an output impedance that will load LOGIC\_SENSE to a predetermined level. The POG will read the input level of LOGIC\_SENSE and configure the audio accordingly.

The proper Microphone path is selected by the AUD MUX controller and path gain is programmable at the PGA. The A/D converter will convert incoming analog signals into 13-bit, 2's complement, linear PCM words. The digital audio signals are then transferred to the POG DSP through a four wire serial interface (ASAP).

# 4-40 A835: PCAP



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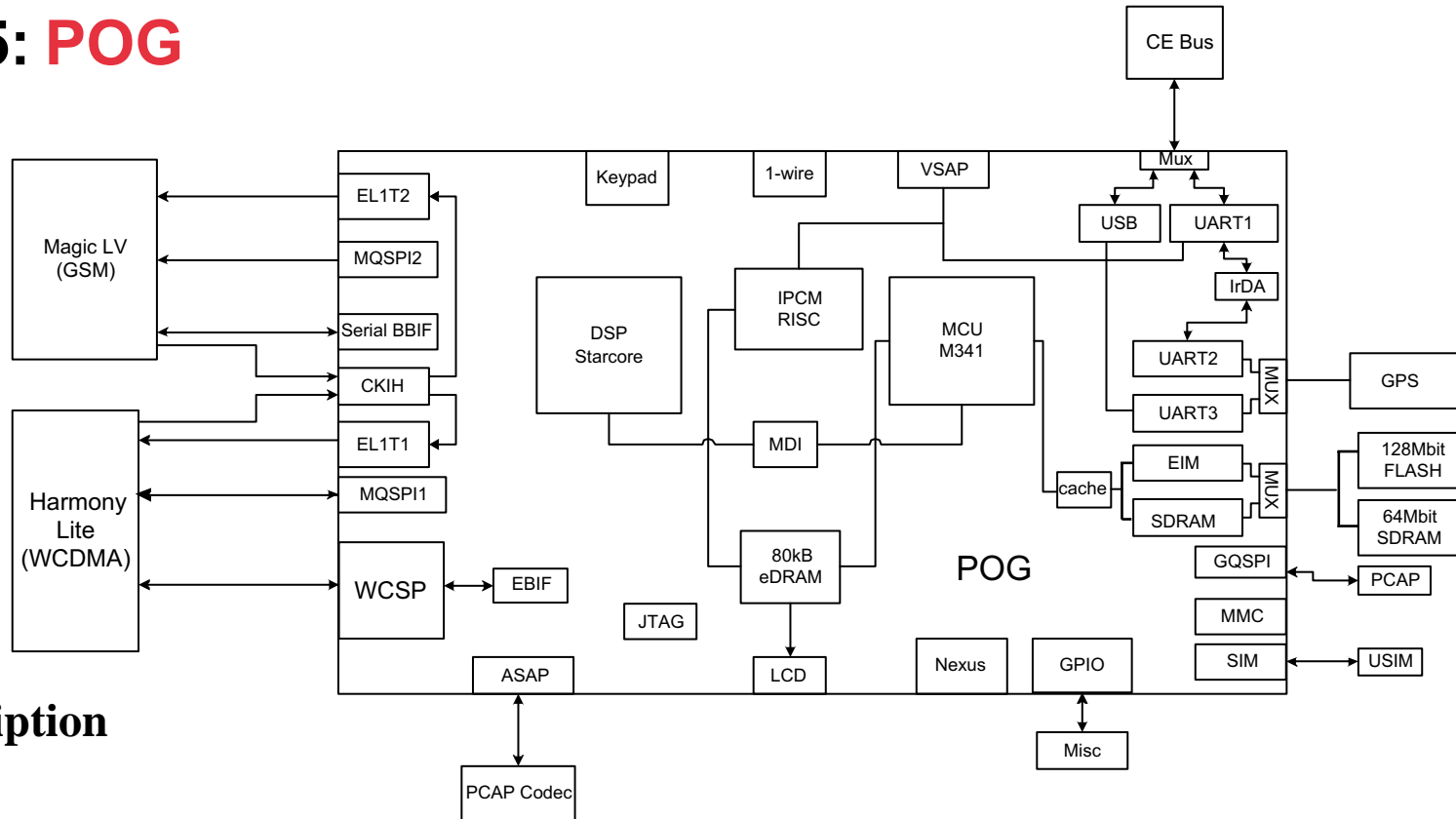
## Description

The Platform Control Audio Power IC (PCAP), U3000, is a mixed signal IC that contains the following features:

- Audio input/output amplification and filtering
- Audio path selection
- Voltage regulation
- Battery charging control
- Real time clock
- Ringer/vibrator control
- RS-232/USB drivers
- Back-light control
- Status LED control
- Multiplexed DAC inputs for temperature and voltage monitoring
- Dual SPI control interface to allow access from two independent baseband processors
- Stereo DAC
- Overvoltage protection
- Touch Screen

The PCAP IC is controlled and configured by the Baseband Processor IC through a four-wire SPI interface. The Baseband Processor has read/write access to the PCAP IC. Audio data is transmitted/received via the Baseband Processor through a four-wire SSI interface.

# 4-42 A835: POG



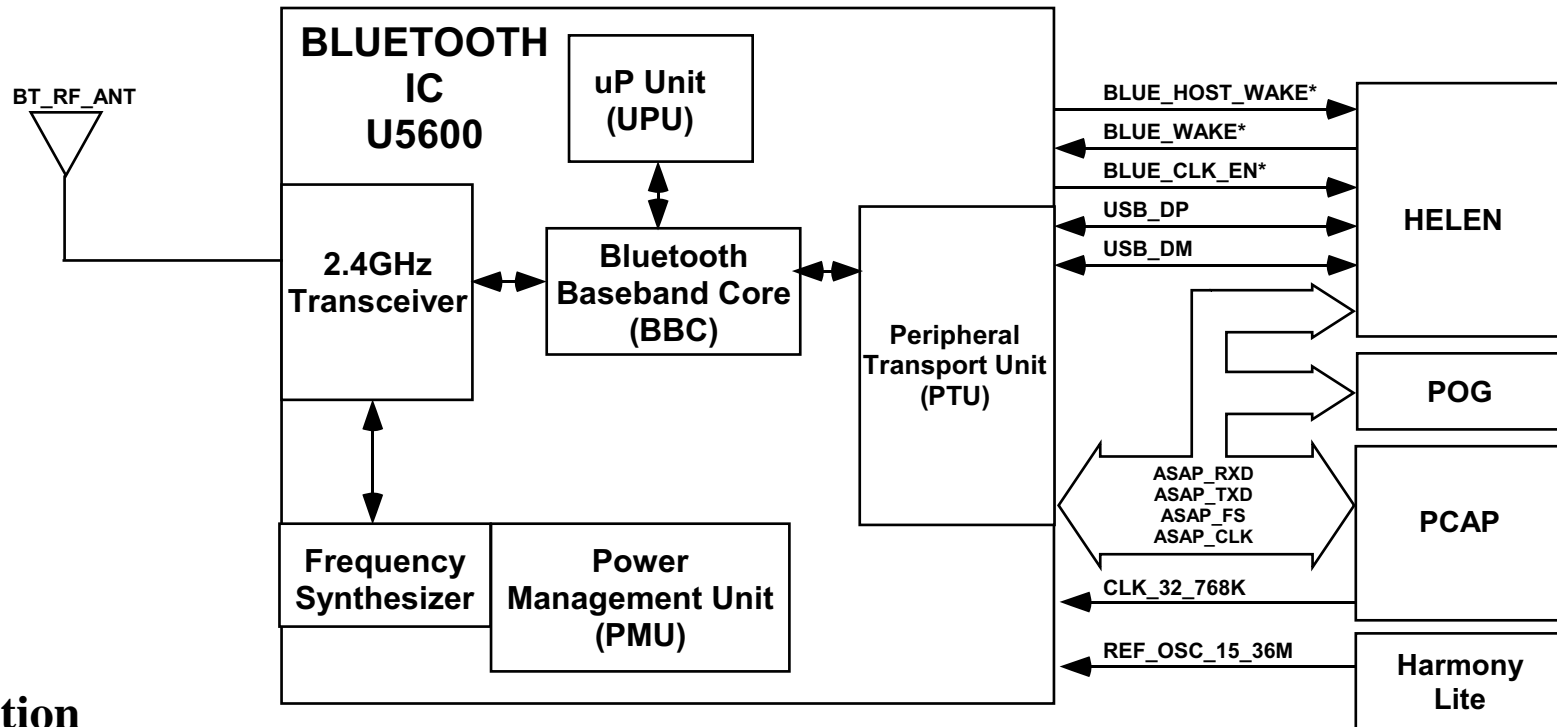
## Description

The POG(baseband processor) integrates a 32-bit RISC Communications Engine (MCU), a 32-bit DSP Core and an Interprocessor Communications Module (IPCM) along with associated peripherals and co-processors. The following provides a brief description of the cores and associated peripherals being used in this design.

- MCU – Micro Controller
- DSP for GSM Signal processing
- EIM(external interface module) interfaces to FLASH and DRAM
- USB/Serial Communications
- GPIO - For A/Ds
- IPCM which provides a multichannel DMA between the Mcore, DSP and peripherals.
- WCSP Interface
- GQSPI - PCAP Interface
- EBIF(External Bus Interface) DMA – WCDMA Data Transportation
- MQSPI1(Qued Serial Peripheral Interface) – WCDMA Control Signals
- EL1T1(Enhance Layer Timer) – WCDMA Event timer
- CKIH - WCDMA 15.36MHz clock
- GPS Interface
- USIM interface
- ASAP interface for PCAP and Bluetooth audio interface
- Serial BBIF(Baseband Interface) – GSM Data Transportation
- MQSPI2(Qued Serial Peripheral Interface) – GSM Control Signals
- EL1T2(Enhance Layer Timer) – GSM Event timer
- CKIH - GSM 13MHz clock

In addition to POG's internal memory system, the architecture provides 128Mbits (16M byte) of external flash memory via two Intel Danali 64M bit parts. The memory bus is 23 address bits and 32 data bits. The flash memory runs at 42-45MHz.

## 4-46 A835: Bluetooth IC



### Description

The BCM2035 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth RF Specification v1.1 and meets or exceeds the requirements to provide the highest communication link quality of service.

The receiver has a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The BCM2035 also features a fully integrated transmitter. Baseband data is GFSK modulated and upconverted to the 2.4 GHz ISM band via an internal mixer. The output Power Amplifier (PA) provides a nominal power output of 0 dBm and has a power control to provide 24 dB of gain control in 8 dB step sizes. Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels.

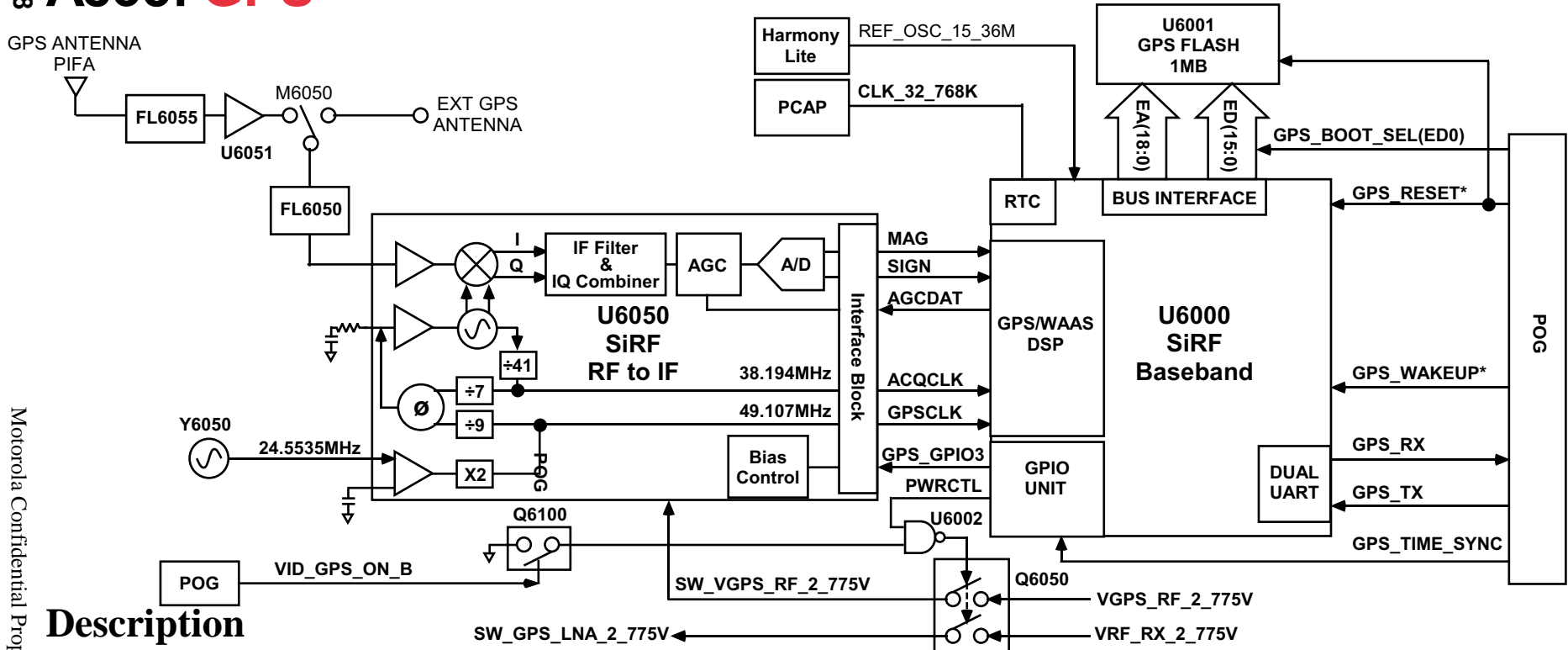
The uPU runs software from the Link Control (LC) layer, up to the Host Controller Interface (HCI). The microprocessor is an enhanced performance 8051 micro-controller.

The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets.

The Peripheral Transport Unit (PTU) handles the Device Interface. The PTU supports three types of devices: USB, UART, and PCM.

The PMU provides power management features that can be invoked by either software through power management registers, or “packet handling” in the baseband core.

# 4-48 A835: GPS



## Description

The 1575.42 MHz satellite signal can be received through the GPS antenna PIFA (Planar Inverted F Antenna) or external GPS antenna. GPS signal received through the PIFA will pass through FL6055 and LNA U6051. The signal is then passed to the LNA input of U6050 through FL6050.

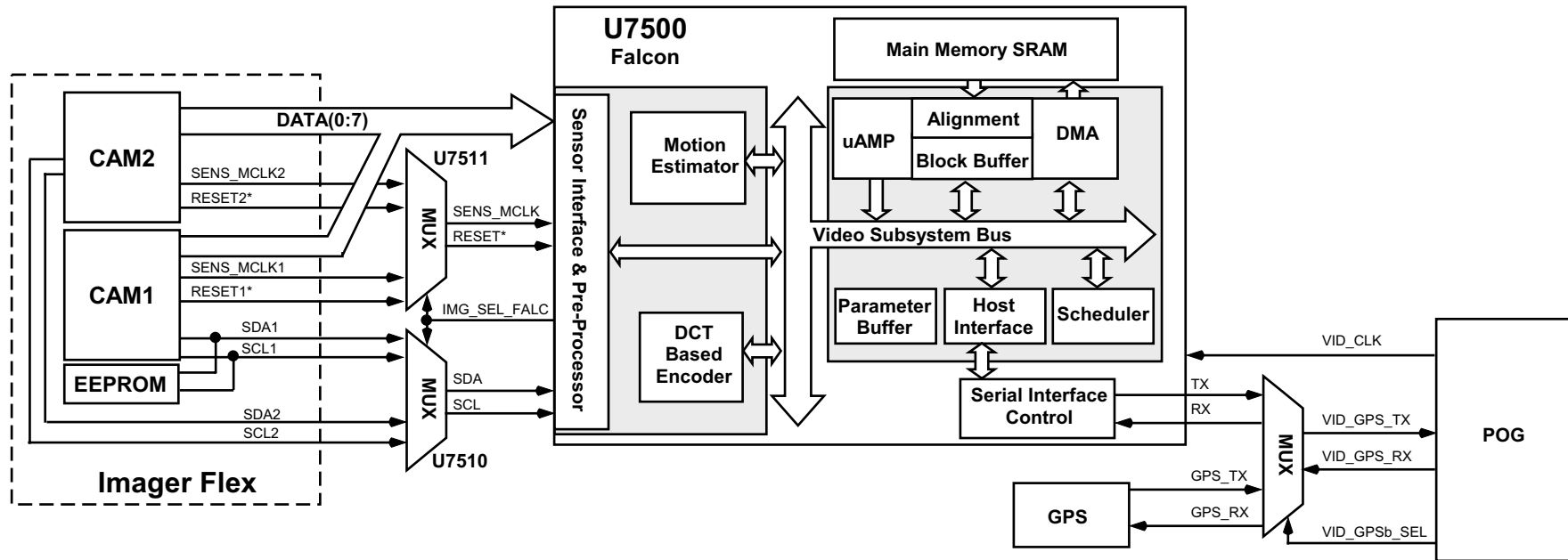
The input signal at the LNA of U6050 is a Direct Sequence Spread Spectrum (DSSS) signal at 1575.42MHz with a 1.023 Mbps Bi-Phase Shift Keying (BPSK) modulated spreading code. The DSSS signal is then injected into an image reject mixer. The Mixer and on-chip 1565.97 MHz VCO will produce an IF center frequency of 9.45MHz. An IF filter is required between the Mixer and AGC Amplifier to provide an anti-aliasing function before A/D conversion. The IF filter block also contains an I-Q phase shift combiner. This circuit properly phase shifts and sums the I and Q outputs from the image reject mixer to a single channel. The AGC amplifier provides the additional gain needed to optimally load the signal range of the 2-bit A/D Converter. The 2-bit A/D converter will then provide signal and magnitude output bits to the Interface Block. The outputs of the Interface Block provide clocks and the 2-bit sample data to the CGSP2e/LP(U6000). These signals use single-ended PECL(Positive Emitter-Coupled Logic) signaling to simplify the complexity of this interface. The interface block inputs are the single-wire AGC interface, (AGCDAT) and the Power Control pin (PWRCTL).

The GPS DSP within U6000 correlates the incoming MAG and SIGN data. Wide parallel search architecture enables simultaneous search of 1,920 time/frequency bins which enables a powerful combination of very fast reacquisition along with the capability to find and track very weak signals. The UART residing in U6000 is used to interface data information between the GSP2e/LP(U6000) and POG. An integrated GPIO unit provides support for a variety of peripherals.

RTC is an ultra-low power implementation of a high precision 32-kHz driven clock derived from the PCAP. It is separately powered by the VDDRTC to allow maximum battery life by maintaining time for the next power on. REF\_FREQ is used as an external clock source for U6000.

GPS\_WAKEUP\* is an active low signal from POG to wake up SiRFLoc client from the deep sleep mode. GPS\_RESET\* is an active low hard reset signal for the SiRF BB IC and Flash. GPS\_BOOT\_SEL is used by POG to set boot configuration upon reset. GPS\_TIME\_SYNC is an active high signal to provide time stamping of the precise time aiding that is sent over from POG over the UART.

## 4-50 A835: Camera



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### Description

The Imager Module includes two image sensor ICs with the lenses which comprise the optical element and the mechanical mount for the lenses, a flexible interconnection cable, and any required passive components for the image sensors, serial EEPROM and connector. The image sensor is of the color CMOS type, with an imager format of VGA: 640 x 480 pixels. The image sensor produces color image data in the Bayer RGB (Red, Green, Blue) format. The lens system will be a two-element, fixed focal length design. The finished module will have bad pixel data for the both imagers stored in the EEPROM. Imager selection is processed through a multiplexer and **IMG\_SEL\_FALC** line.

The Falcon IC (U7500) is a video encoder chip designed to directly interface to a CMOS image sensor and output encoded video to a host processor (POG). The Falcon has on-board memory for QCIF (176x144) sized video. A frame rate of 30 per second is sustainable providing the host removes the compressed images at that same rate. The Falcon is also capable of capturing VGA still images in JPEG format.

The video encoder sensor interface allows the encoder to receive the Bayer formatted data from the image sensor. The Bayer formatted data is then processed through a color interpolation in which Red (R), Green (G), and Blue (B) components will be contained in each pixel. The bitmapped RGB image will contain 8 bits/color and 24 bits/pixel. The RGB image is then sent through a color space conversion where the luminance and chrominance data is compressed and sent to the POG through a RS232 interface. The POG IO for the camera is multiplexed with the GPS circuit. POG selects whether it's going to interface with GPS or camera via **VID\_GPSb\_SEL**.