Service Manual

Level 3

Draft 1.0

MOTOROLA™

DIGITAL WIRELESS TELEPHONE

Model A835

UMTS 2100MHz/ PCS 1900MHz/ DCS 1800MHz/ GSM 800MHz

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3G Flash Procedures

Introduction

This document is intented to decribe the flashing(software updates) and procedures for 3G terminals. The 3G terminal described in this document will be limited to the A835.

Software updates need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the correct software is programmed.

Software updates allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific conditions, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the A835.

Power options

1. Fully Charged battery (SNN5638A)

2. Full-rate Charger (PSM5049A)

Interface Options

1. USB Data Kit (S8951)
   USB Cable (SKN6311A)
   Data Software CD

2. RS232 Data Kit (S8952)
   RS232 Cable (SKN6315A)
   RS232 to CE converter (SYN0279B)
   Data Software CD

Software Requirements

The Product Support Tool (PST) is used to allow functions such as flashing, flexing, and memory transfers. Contact your local Motorola service representative to receive download information for the PST and related support files.

For download information on Flash software, contact your local Motorola service representative.

A830 Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a non-functional (Bricked) 3G terminal.

The A830 contains a Flash EPROM with a total memory of 16MB. The memory resides within two 8MB Intel EPROMs connected in parallel.

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery Solution
2. Full-Rate Charger Solution (recommended)

If the user decides on using the battery solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the fhash process. This action may cause unrecoverable failures to the 3G terminal.

Hardware connection solutions

There are two types of hardware solutions to perform a flashing procedure.

1. USB configuration (recommended)
2. RS232 configuration

RS232 configurations should be used only if the PC is running an operating system (OS) that doesn't support the USB interface. USB configurations will provide a faster data transfer rate than RS232. As a result, flash durations will be reduced when using a USB connection.

PST Flash Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal.

1. Download the desired flash software into the computer.

2. Connect the desired hardware configuration as illustrated in figure 1.

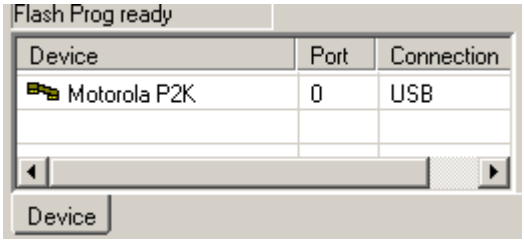
3. Power up the 3G terminal

4. If the 3G terminal doesn't power up, refer to the Force Flash section.

5. Launch the PST application by choosing Start/ Programs/Motorola PST/Flash & Test Commands.

6. Click on the Browse button and select the desired flash software

7. Select the device that will be flashed



8. Once the 3G terminal is placed in flash mode, the Flash button will be enabled.

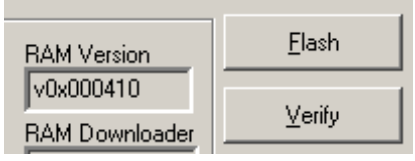


Figure 1. PST Hardware Configuration

9. Click on the Flash button to begin flashing. DO NOT interrupt any hardware connections during the flash process. Connection interuptions may cause the flashing process to fail and render the 3G terminal non-operational.

10. When flashing is complete, a message will pop up stating," Flash another phone?". At this time you may safely disconnect the 3G terminal and select the appropriate response.

11. Power up the 3G terminal to insure that the flash procedure was successful.

Force Flash Procedures

The procedures described in this section apply only to situations where the 3G terminal will not initiate it's normal power up sequence, but may recover functionality by a repeat flash procedure.

There are three possible alternatives to place the 3G terminal in force flash mode.

Key Hold Solution

Hardware: Refer to Figure 1 (USB solution)

Step 1. Remove the battery from the 3G terminal

Step 2. Prior to connecting the USB cable, press and hold the "*" and "#" key from the 3G terminal

Step 3. Attach the USB cable

Step 4. Verify that the PST application detects the 3G terminal, if it's not detected, press and hold "*" and "#" once again.

Force Flash USB Cable Solution

Hardware: Refer to Figure 1 (USB solution), except, replace USB cable (SKN6311A) with force flash cable (SKN6168A)

Step 1. Connect the force flash cable in the same manner described in Figure 1.

Step 2. The 3G terminal will automatically be placed in force flash mode. There's no need to press the power key. The PST application will now detect the 3G terminal

Junior Board Solution

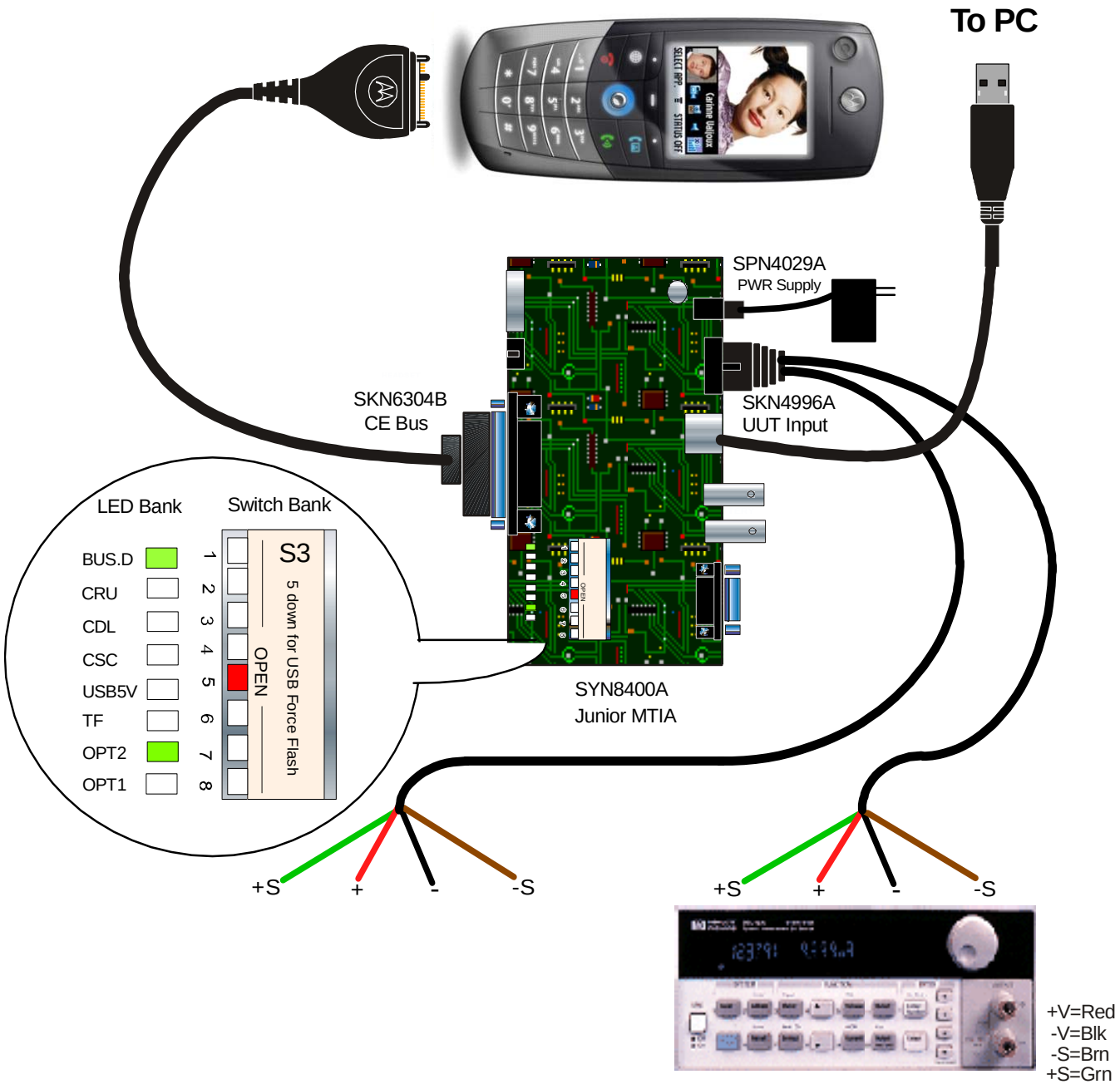
Hardware: Refer to Figure 2.

Step 1. Insure that dip switch #5 is in the down position and all other switches are in the up position.

Step 2. Connect the 3G terminal to the CE bus cable. Insure that the power supply is set to 4.4Vdc

Step 3. The PST application should now detect the 3G terminal

Figure 2. Junior Board Configuration



Handset Test Commands

Introduction

The Handset Test Command mode of the phone is provided primarily for service personnel without access to equipment capable of exercising Test Commands over a computer connection. This mode collects input from the user and packages it in the format required by the Test Command component within the phone.

User Interface

Three screens are used, as described below, for command data entry and command response display: the opcode entry screen, the field entry screen, and the command results screen. The following screen flow diagrams do not depict an actual test command, but instead demonstrate the general behavior of the mode.

As the phone does not provide an easy method of hexidecimal entry, all input and output will be in decimal format, with the exception of output fields considered to be data streams. This requires careful consideration as a significant portion of this document is described using hexadecimal format. As an aid in the decimal entry of opcodes, Table 1 is provided which indicates the decimal equivalent number for supported opcodes.

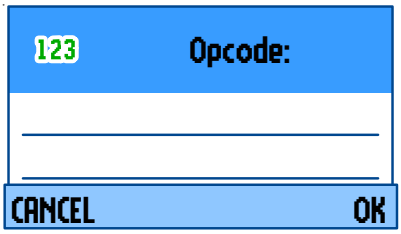
The END key exits handset test command mode or restarts the phone (if suspended). However, pressing the END key in the waiting for results screen (a "frozen" version of the final entry screen) has no effect, though the power key still allows the phone to be powered down.

Handset Test Command Mode Entry

The mode is entered using a key shortcut, "<MENU> 0 HTCMD *".

The user will be taken to the initial screen (the opcode entry screen).

Figure 3. Opcode Screen



The mode may only be entered from the idle screen. Entry is not allowed while an active computer test command session exists (ie RS232 or USB); an error will be displayed if a computer session is active.

When the handset test commands feature is invoked, the handset is not suspended by default. The handset can only be suspended by executing the SUSPEND test command. The user can exit the feature and return to idle if the handset has not yet been suspended. Otherwise, exiting the feature will cause a restart.

Command entry

Once the mode is entered, two screens are used to collect command request information from the user. The opcode entry screen (Figure 5) allows the entry of either an entire command as described in this section, or entry of a partial command. If a partial command is entered, the user will be prompted to enter the remaining required information via an appropriate number of field entry screens (Figure 7). Pressing OK with no data entered in the opcode or field entry screen will cause a parse error (unless the field is optional).

The asterisk is used to delimit fields on the opcode entry screen and is not allowed on the field entry screen. On the opcode entry screen, it is not legal to have an asterisk immediately follow another asterisk.

Opcode entry

The opcode entry screen allows the user to enter the opcode for the test command, or the opcode plus additional parameters delimited by the * character.

Figure 4. Opcode Entry Screen

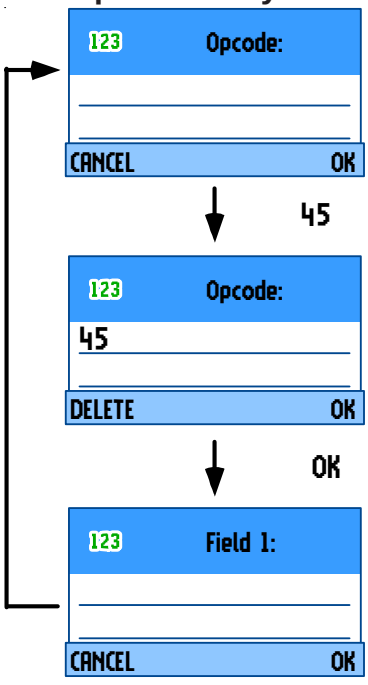
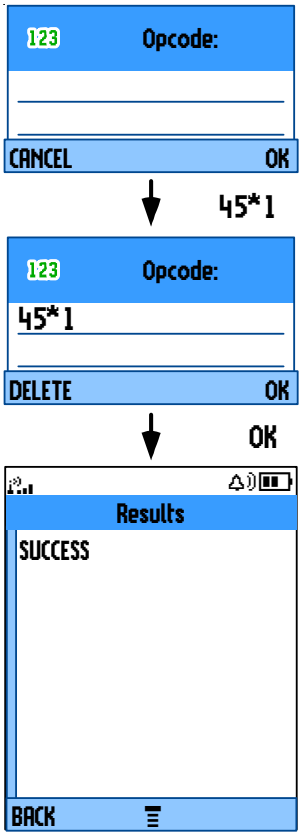


Figure 5. Multiple Parameter Entry



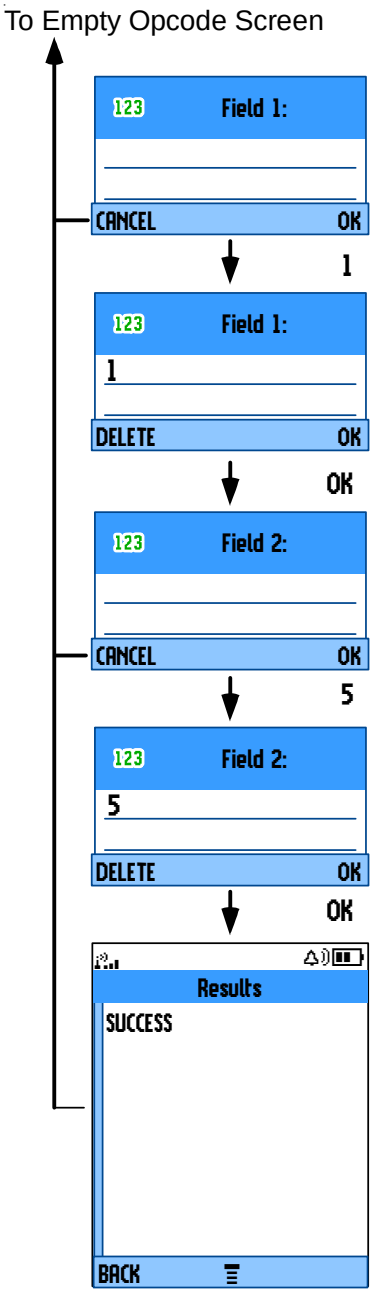
Opcode Entry Screen Keymap:

0-9: command data
*: field delimiter
OK: process value, move to next screen
DELETE (short): delete single char
DELETE (long): delete all chars
CANCEL: return to idle or restart if suspended
End: return to idle or restart if suspended

Field entry

The field entry screen allows the user to enter fields for the test command separately from the opcode. Each field entry screen allows only one field to be entered. The user will be led through the remaining parametersone by one until the command is completed.

Figure 6. Field Entry Screen



Field Entry Screen Keymap:

0-9: command data
OK: process value, move to next screen
DELETE (short): delete single char
DELETE (long): delete all chars
CANCEL: return to opcode entry screen
End: return to idle or restart if suspended

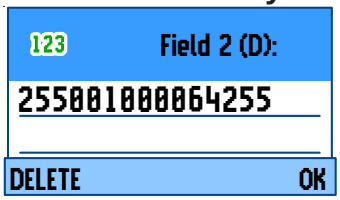
Numeric Field Entry:

Fields are numeric by default. The digits entered for the field will be evaluated as a single decimal number.

Data Field Entry:

The user must enter 3 digits for each byte of a data field (variable or non-variable length). Zero padding is required if all 3 digits are not required to represent the value. Any data field which is not a multiple of 3 digits will generate a parse error. The field title of any data field will be tagged with a (D). Figure 8 is an example of a 5 byte data field.

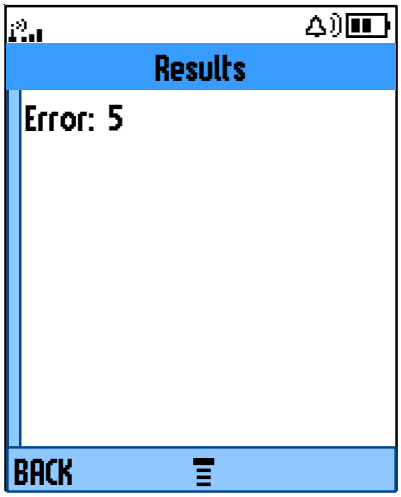
Figure 7. Data Field Entry Screen



Command Results

If a command completes successfully with returned data, the data is displayed in a results screen as depicted in Figure 9. If a command is successfully completed but does not produce any output data, the user will be returned to the opcode entry screen. In the case of a command error, the standard response code (Table 2) is displayed on the results screen.

Figure 8. Command Results Screen



There is no way to abort or power down from the waiting for results screen. The waiting for results screen is simply a “frozen” version of the final entry screen as opposed to having a dedicated screen.

Table 1. Handset Test Command Summary

Opcode Hexadecimal	Opcode Decimal	Opcode Mnemonic	Key Entry Format	Op Code Description
0	0	AUD_TN_LST	0 *<Action> * <Tone Identifier>OK	Generate/disable predefined tone
3	3	AUD_CTRL	3 *<Device/Process> * <Action>OK	Control various audio functions; enable/disable vibrator
4	4	AUD_LPB	4 *<Loopback Type> * <Action>OK	Enable audio loopback
5	5	AUD_LVL	5 *<Get/Set>*<Volume>OK	Set audio level
6	6	AUD_PATH	6 *<Input Path>*<Output Path>*<RX Mute>*<TX Mute>OK	Change audio path
7	7	CARRIER	7 * <Option> * <Action> OK	Enable GSM TX carrier
0A	10	CP_MODE	10 * <Set/Get> * <Sub-mode> OK	Set Call Processing Mode
12	18	INVM	18 * <level> OK	Master clear or reset
14	20	LOAD_SYN	20 * <Channel> * 0 OK	Set GSM channel
22	34	RESTART	34 * OK	Generate a software restart
2D	45	SET_RF_PWR	45 * <Power level> OK	Set GSM Power level
36	54	SUSPEND	54 OK	Terminate normal mode and enter test mode
37	55	TST_DISP	55 * <Parameter> * <Parameter Data> OK	Display predefined patterns
39	57	VERSION	57 *<version Type>OK	Retrieve SW version information
3E	62	LEDS	62 * <LED> * <Action> * <Data> OK	Control status LEDs
C0B	3083	WLOAD_SYN	3083 * <RX_FREQ_ID> * <TX_FREQ_ID> OK	Set WCDMA channels
C0E	3086	W_CARRIER	3086 * <Channel ID> * <Action> * <Tx Pwr> * <Max Pwr> * <Min Pwr> * <Data Pattern> * <Channelization> * <Scrambling> * <DPCCH Spread Factor> * <DPDCH Spread Factor> * <Channelization Code> * <Scrambling Code> OK	Enable WCDMA TX carrier

Table 2. Standard Response Codes

Opcode (Hexadecimal)	Opcode (Decimal)	Response Field Definition
0000b (0x00)	0	parse error (no data follows): invalid data length for command
0001b (0x01)	1	parse error (no data follows): inadequate security level for command/parameter
0010b (0x02)	2	parser error (no data follows): command/parameter not supported for current protocol (CDMA, GSM, TDMA)
0011b (0x03)	3	parse error (no data follows): command/parameter not supported for current mode (normal, test mode, handset test mode)
0100b (0x04)	4	parse error (no data follows): unsupported/invalid opcode
0101b (0x05)	5	parse error (no data follows): unsupported/invalid parameter for opcode
0110b (0x06)	6	command response: generic success (no data follows)
0111b (0x07)	7	command response: generic failure (no data follows)
1000b (0x08)	8	command response: data follows
1001b (0x09)	9	unsolicited/multiple response: data follows (sequence tag is 0)
1010b (0x0A)	10	error: couldn't allocate memory
1011b (0x0B)	11	error: internal task error
1100b (0x0C)	12	error: Test Command task timed out waiting for response from another SW component
1101b (0x0D)	13	CDMA: parse error (no data follows): command/parameter not supported for current sub-mode TDMA: command not supported in current Call Stack Test Mode
1110b (0x0E)	14	error: length specified in command header greater than length received by transport layer
1111b (0x0F)	15	error: irrecoverable error; phone state has been lost. Phone is being powered down

Table 3. Field and Parameter descriptions

Opcode (Decimal)	Opcode Mnemonic	Field	Description
0	AUD_TN_LST	Field 1	0 = start atone 1 = stop a tone
		Field 2	0-9 = DTMF tones
3	AUD_CTRL	Field 1	0 = Vibrator 2 = Echo canceling 3 = Noise suppressor
		Field 2	0 = Disable 1 = Enable
4	AUD_LPB	Field 1	0 = PCAP loopback 6 = CODEC loopback 7 = VOCODER (speech) loopback
		Field 2	0 = Disable Audio loopback 1 = Enable Audio loopback
		Field 3	This field is valid only for VOCODER loopback 0 = AMR 4.75 1 = AMR 5.15 2 = AMR 5.90 3 = AMR 6.70 4 = AMR 7.40 5 = AMR 7.95 6 = AMR 10.20 7 = AMR 12.20 8 = Full Rate 16 = Enhanced Full Rate 32 = Half Rate
5	AUD_LVL	Field 1	0 = Set the volume specified
		Field 2	0 = lowest, 7 = loudest

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
6	AUD_PATH	Field 1	0 = As is. 1 = Mute input path 2 = Internal (handset) mic 3 = Ext audio input (CE Bus) 4 = Boom (headset) mic 5 = Ext digital audio (USB) 7 = Bluetooth time slot 1 audio input 8 = Bluetooth time slot 2 audio input 9 = Bluetooth time slot 3 audio input
		Field 2	0 = As is 1 = Mute output path 2 = Internal (handset) Speaker 3 = Alert 4 = Ext audio output (CE Bus) 5 = Speakerphone 6 = Boom (headset) speaker
7	CARRIER	Field 1	0 = All zeroes 1 = All ones 2 = pseudo random sequence w/midamble 0 3 = pseudo random sequence w/midamble 1 4 = pseudo random sequence w/midamble 2 5 = pseudo random sequence w/midamble 3 6 = pseudo random sequence w/midamble 4 7 = pseudo random sequence w/midamble 5 8 = pseudo random sequence w/midamble 6 9 = pseudo random sequence w/midamble 7 10 = RACH BURST 12 = pseudo random sequence w/midamble 0 two time slot 13 = pseudo random sequence w/midamble 0 three time slot
		Field 2	0 = disable 1 = enable

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
10	CP_MODE	Field 1	0=set submode 1=get submode
		Field 2	5 = GSM 1900 6 = GSM dual band GSM900/GSM1800 8 = WCDMA Region 1 10 = Automatic - Dual mode: WCDMA region 1 and GSM dual band GSM900/GSM1800.a
18	INVM	Field 1	0 = Master Reset 1 = Master Clear
20	LOAD_SYN	Field 1	Channel number in decimal. Valid channel numbers are: • 1-124 (PGSM 900 MHz) • 0, 975-1023 (EGSM 900 MHz) • 512-885 (DCS 1800 MHz) • 512-810 (PCS 1900 MHz)
		Field 2	Reserved for future use and TDMA; set to 0.
34	RESTART	Field 1	As is
45	SET_RF_PWR	Field 1	PA power level (0-19)
54	SUSPEND	Field 1	As is
55	TST_DISP	Field 1	2 = Display Predefined Pattern 9 = Turn On/Off the Front Light
		Field 2 (Data)	Data for 2, 000 = All pixels off (all black) 001 = All pixels on (all white) 005 = Grey scale block: 16 level, Black to white 006 = Horizontal Zebra Line 014 = Eight Color Box Pattern Data for 9, 000 = Front Light Off 001 = Front Light On, Full Intensity

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
57	VERSION	Field 1	016000 = DSP Version
			017000 = User (login) pf process that created this file
			017001 = Build time (universal) in ISO-8601 format
			017002 = Clearcase view tag name
			017003 = Product base label from Clearcase config spec
			017004 = Product ID
			017005 = Version Number
			017006 = Build commentary
			018000 = Flash Booter version number (P2K Booter Only)
62	LEDS	Field 1	0 = Keypad Backlight LED 3 = Red LED 4 = Green LED
		Field 2	0 = Disable LED (Keypad backlights Only) 1 = Enable LED (Keypad backlights Only) 3 = Set duty cycle (Red/Green LEDS Only)
		Field 3	Duty Cycle setup, (leave blank if field 1 is set to 0) 000 = Off 012 = On
3083	WLOAD_SYN	Field 1	UARFCN for Receive Frequency ID. Valid values are between 0 and 16383. If TX_FREQ_ID is set to 0xFFFF, then RX_FREQ_ID must take values between 190*5 and 16383. **Note:** If a valid TX_FREQ_ID will be entered, RX_FREQ_ID must be set to FFFF.
		Field 2	UARFCN for Transmit Frequency ID. Valid values are between 0 and 16383. If it is set to 0xFFFF the TEST_TASK will derive the TX_FREQ_ID from the RX_FREQ_ID. **Note:** If a valid RX_FREQ_ID is entered, TX_FREQ_ID must be set to FFFF.

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
3086	W_CARRIER	Field 1	Channel identifier (0-16383).
		Field 2	0 = Enable carrier. 1 = Disable carrier.
		Field 3	Initial transmit power (dBm). -128 dBm to 127 dBm
		Field 4	Maximum transmit power (dBm). -128 dBm to 127 dBm
		Field 5	Minimum transmit power (dBm). -128 dBm to 127 dBm
		Field 6	0 = All 0s. 1 = All 1s. 2 = PN9. 3 = PN15.
		Field 7	0 = Disable spreading. 1 = Enable spreading.
		Field 8	0 = Disable scrambling. 1 = Enable long scrambling. 2 = Enable short scrambling.
		Field 9	0 = SF256, slot format 0. 1 = SF256, slot format 1. ... 5 = SF256, slot format 5.
		Field 10	0 = SF256, slot format 0. 1 = SF128, slot format 1. ... 6 = SF4, slot format 6.
		Field 11	Channelization Code Number.
		Field 12	Scrambling Code Number.

Manual Test Procedures

Introduction

The phone allows keypad and computer controlled testing of various digital test parameters.

This chapter includes the keypad/computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

Non-Signalling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signalling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The digital phasing parameters are stored in a EPROM on the Transceiver Board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5639B[1] or equivalent)
- Full-Rate Power Supply (PSM5049A[1])
- Battery Eliminator (5-00-3F-10000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

Control Interface Options (PCS Only)

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

Note: If handset test commands are being used, a control interface is not needed.

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

RF Interface (Everything listed is required)

- SMA/N-type Adapter (0-00-00-40042[2])
- SMA Cable 0.5m (0-00-00-40047[2])
- Repair Fixture (5-00-4T-10000[2])
- USIM (0-00-00-40810[2])

Software Requirements (PCS only)

If PCS call processing procedures are necessary, the user will need to send a test command to the phone prior to beginning the test. The command can be initiated through handset test commands or computer test commands. Software requirements for each method is listed below.

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

Call Origination

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

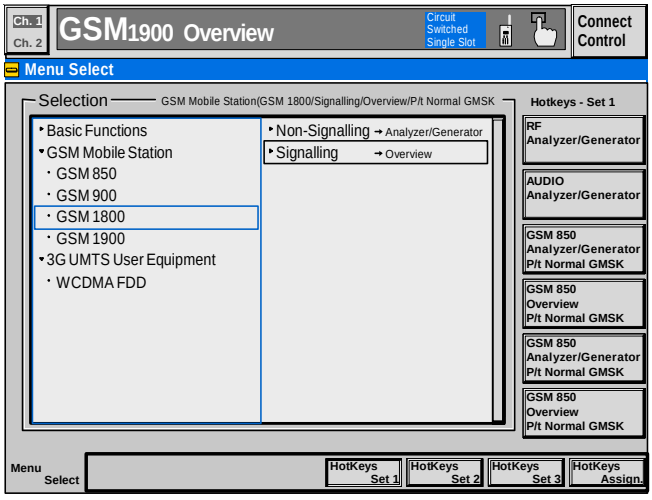
1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 13.

   Note: Control interface doesn't need to be connected at this time.

3. Setup up the test box for GSM, DCS, or PCS Signalling

Figure 9. GSM Signalling Setup



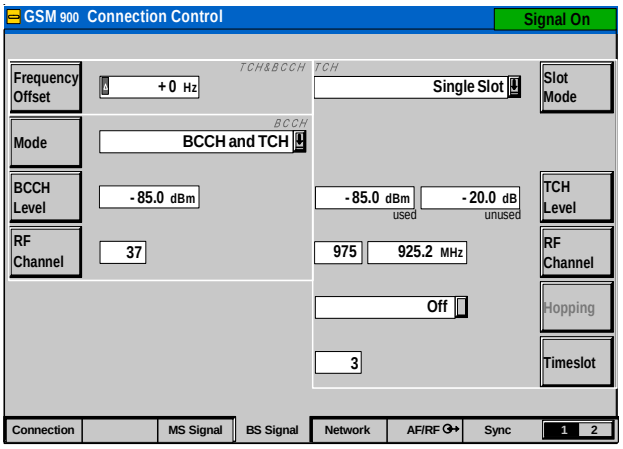
4. Set Broadcast Channel (BCH) to 120 (GSM), 700 (DCS), or 661 (PCS)

5. Set Broadcast channel level to -85dBm

6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS/PCS)

7. Set Traffic channel level to -85dBm

Figure 10. GSM Connection Control



8. Wait until the phone indicates a receive signal

9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 11. GSM Call Connected

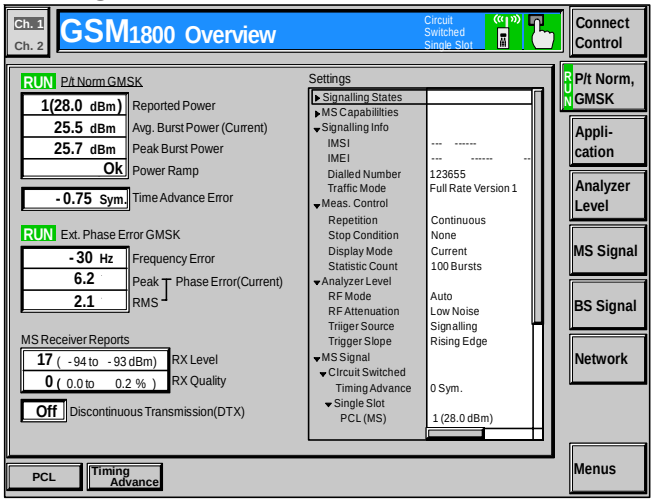
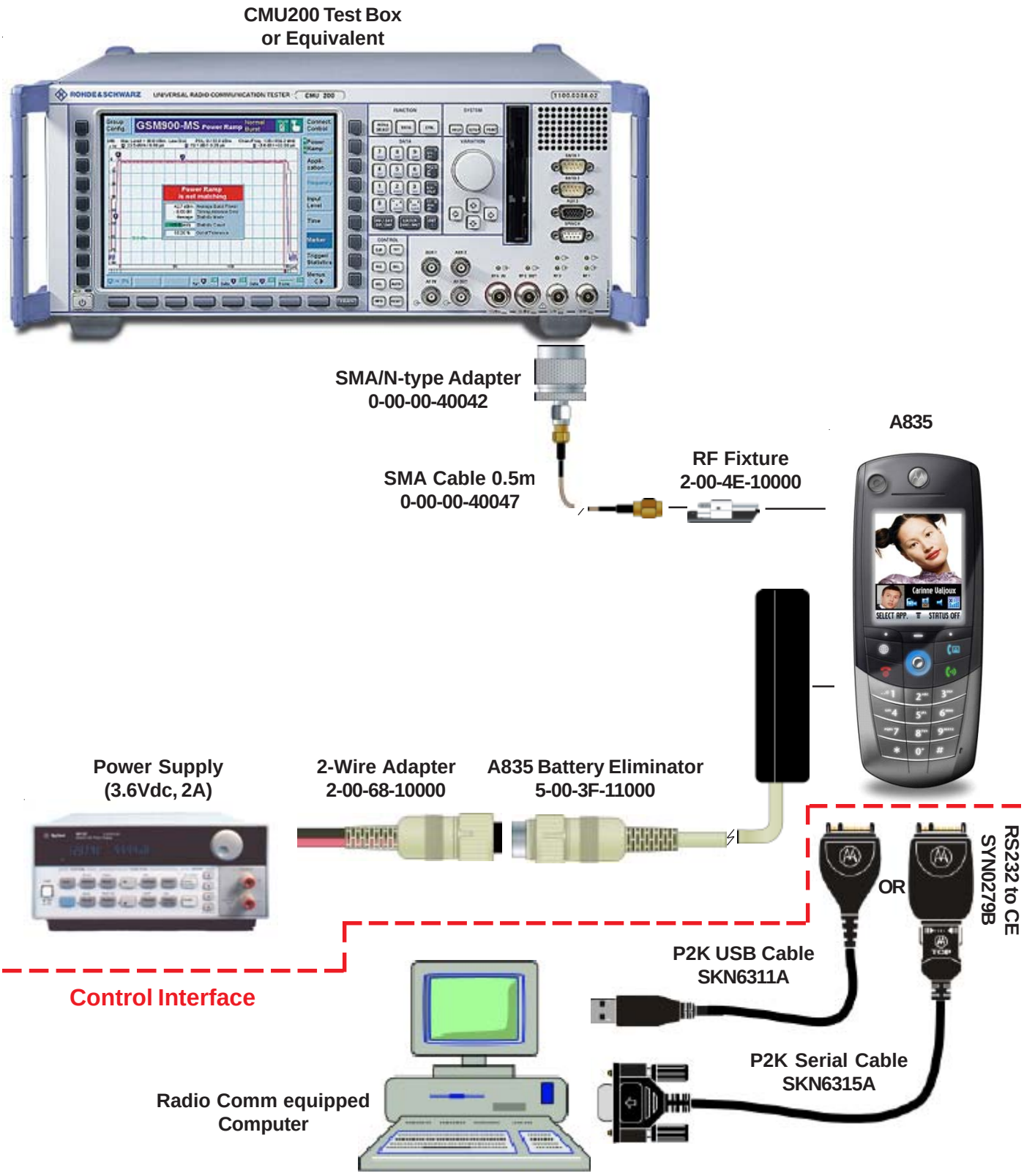


Figure 12. A835 Manual Test Hardware Configuration



Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 4. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	31	33	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 5. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	28	32	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

[1]Power Level = 0
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

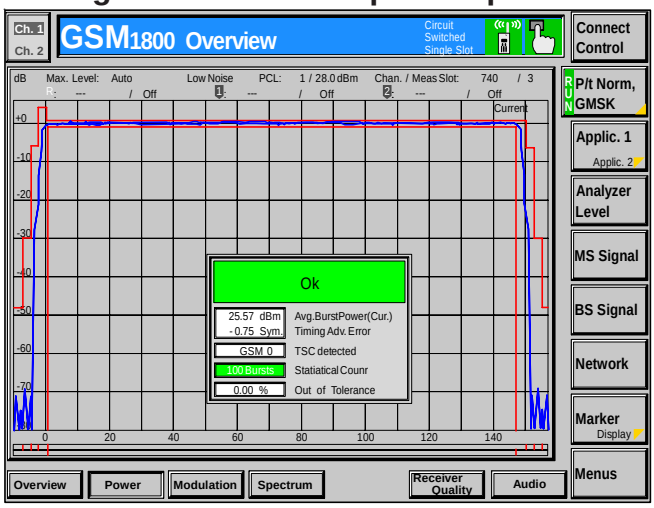
Table 6. PCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	28	32	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 0
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Burst Output Shape should fall within the standard limits of the Power Ramp.

Figure 13. Burst Output Shape



BER measurements is only required if RX Quality reads a value of 4 or greater.

It is recommended that handover procedures be performed as shown in the following table.

Table 7. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 13.

Software Requirements

None.

Call Origination (WCDMA)

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signalling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

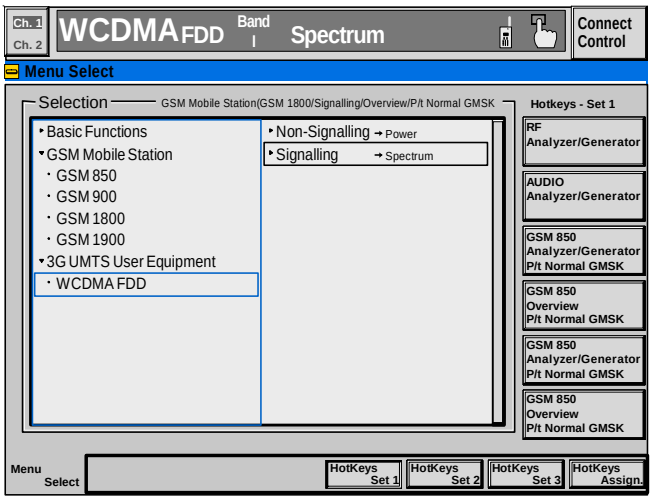
1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

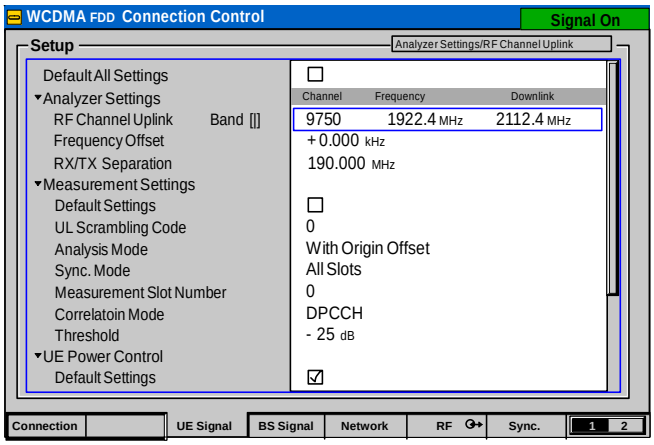
3. Setup up the test box for WCDMA FDD Signalling

Figure 14. WCDMA Signalling Setup



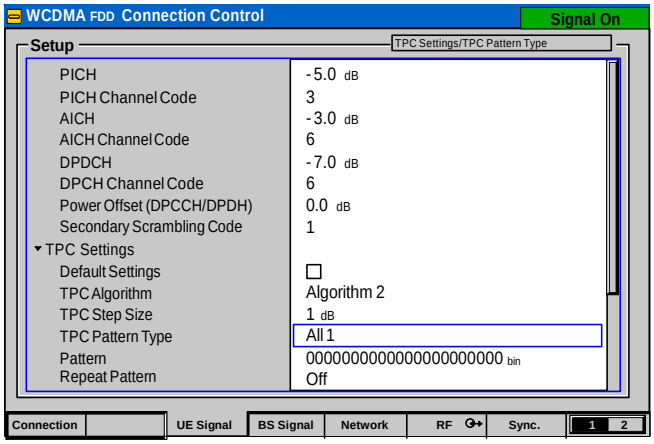
4. Set UE Signal, RF Channel Uplink to 9750

Figure 15. Channel Uplink(UE Signal)



5. Set TPC Pattern Type to All 1

Figure 16. TPC Pattern Type(UE Signal)

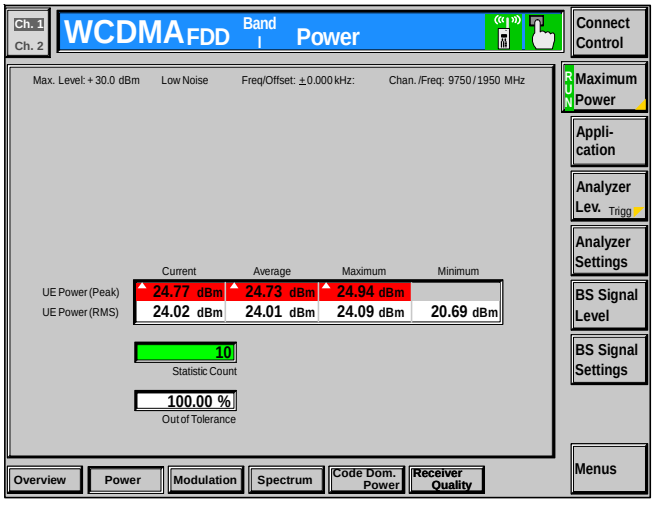


6. Wait until the phone indicates a signal

9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 17. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 8. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 18. WCDMA Modulation

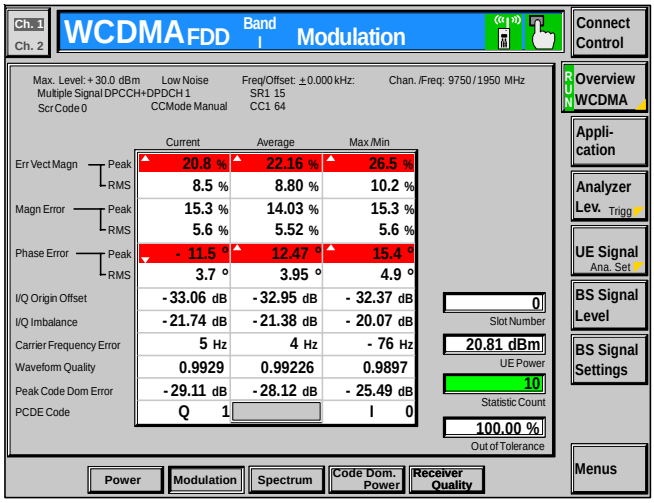
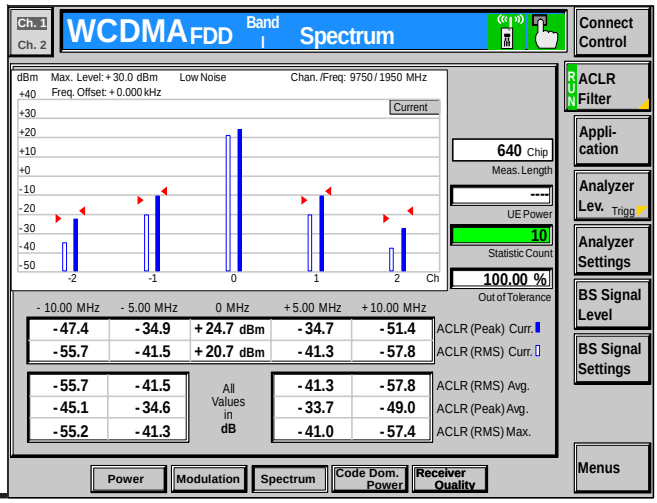


Figure 19. ACLR Screen



Non-Signalling Test Procedures (GSM/DCS/PCS)

To perform non-signalling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands can be sent using the Handset test command interface or through a computer. Please refer to section, "Handset Test commands," for details on how to send test commands through phone keypad entry.

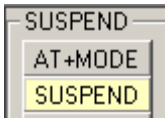
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

Refer to page 3-2 for a list of Hardware. Refer to Figure 13 for a configuration illustration.

Software Requirements

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

Verify TX Power Output (GSM/DCS/PCS)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 9. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28	29.5	dBm
PCS TX Power Out	28	29.5	dBm

Handset Test Commands

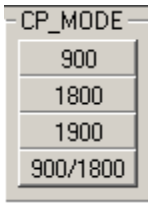
54	Suspend
10*0*10[1]	WCDMA/GSM/DCS mode
20*38*0[2]	Set Channel 38
45*5[3]	Set GSM Power Level 5

[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

7*6*1 Enable Carrier

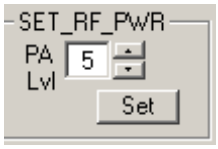
Radio Comm Test Commands

Click on 900/1800 (GSM/DCS) or 1900 (PCS)

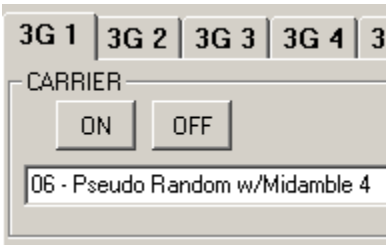


Enter 38 (GSM), 700 (DCS), or 661 (PCS) and then click Set

Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

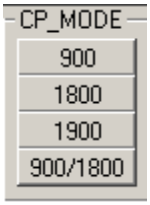
Broadcast Channel (BCH): 20
Broadcast Channel (BCH) Level: -105 dBm

Handset Test Commands

No supported test commands

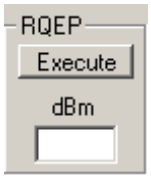
Radio Comm Test Commands

Click on 900/1800 (GSM/DCS) or 1900 (PCS)



Enter Channel 20
Click INIT

Click Execute
Verify return data is approximately -105 dBm



Non-signalling Test Procedures (WCDMA)

To perform non-signalling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands can be sent using the Handset test command interface or through a computer. Please refer to section,"Handset Test commands," for details on how to send test commands through phone keypad entry. Also, refer to, "Computer Test Commands," for details on how to send test commands through the computer.

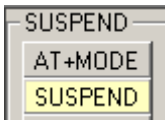
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

Refer to page 2 for a list of Hardware. Refer to Figure 4 for a configuration illustration.

Software Requirements

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 10. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	20.5	21.5	dBm

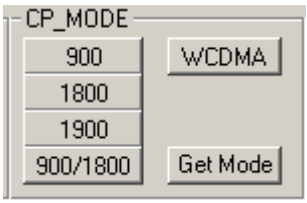
Handset Test Commands

54		Suspend
3086		W_CARRIER
Field 1	9750	Set Channel
Field 2	0	Enable Carrier
Field 3	023	Max Power Out
Field 4	027	Max TX Power
Field 5	206	Min TX power
Field 6	002	PN9 Data pattern
Field 7	1	Enable spreading
Field 8	01	Long scrambling
Field 9	000	SF256, Slot format 0
Field 10	000	SF256, Slot format 0
Field 11	000	Channelization Code
Field 12	000000000	Scrambling Code

Note: Enter 1 in field 2 to disable carrier

Radio Comm Test Commands

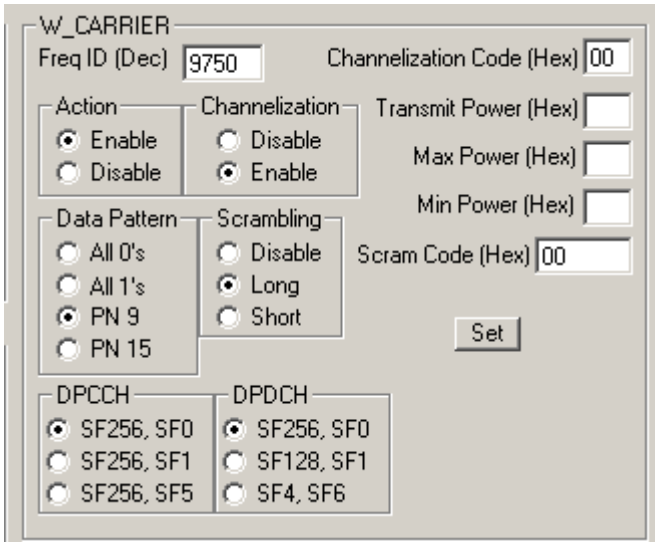
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)



Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

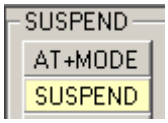
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



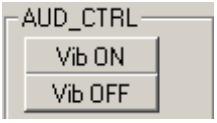
Vibrator Test

Handset Test Commands

3*0*1 Enable Vibrator
3*0*0 Disable Vibrator

Radio Comm Test Commands

Enable or Disable Vibrator



Verification

Verfiy vibration function when enabled.

Handset Mic/Speaker test

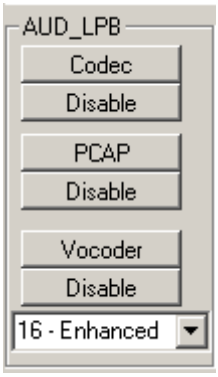
Handset Test Commands

6*2*2	Enable internal mic and handset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

Radio Comm Test Commands

Enable internal mic and headset speaker

Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

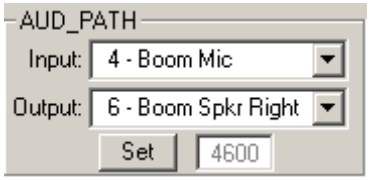
Mono Headset Mic/Speaker test

Handset Test Commands

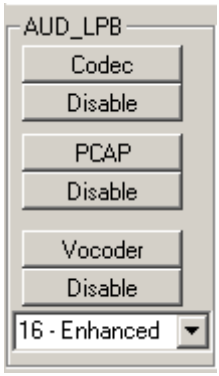
6*4*6	Enable headset mic and headset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

RadioComm Test Commands

Enable headset mic and headset speaker



Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

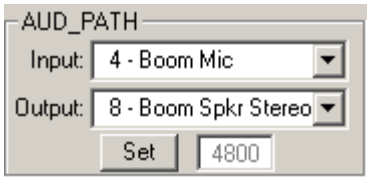
Stereo Headset Mic/Speaker test

Handset Test Commands

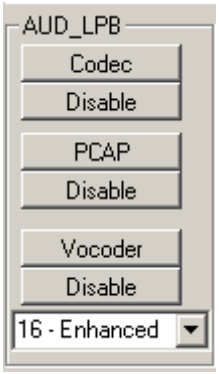
6*4*8	Enable headset mic and headset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

RadioComm Test Commands

Enable headset mic and headset speaker



Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

Handset Test Commands

0*1*245	Play BACH_INVENTION_1
0*0*245	Stop BACH_INVENTION_1

NOTE: DO NOT issue a Suspend command (54 ok) for this test.

RadioComm Test Commands

Currently not supported

Verification

Listen for undistorted audio.

Software Version Check

Use the following procedures to retrieve software information. Software information can also be retrieved from the phone's customer User Interface. Refer to the phone's user manual for details.

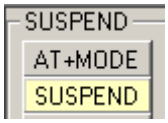
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE (Serial Only)
Click PST Initialize (USB Only)



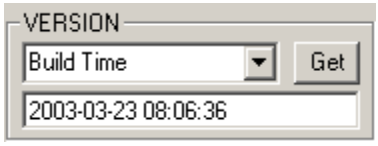
Test Commands

57*017003 Read Software Version
57*017001 Read Build Date

RadioComm Test Commands

Select Product Base Label and click "Get" to retrieve software version

Select Build Time and click "Get" to retrieve Build Date



Display Test Procedures

This section will describe the proper test procedures to determine the functionality of the color display. Any tests that involve displaying a predefined pattern can be returned to the Opcode screen by pressing the right softkey of the phone.

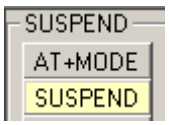
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Display Backlight Test

Handset Test Commands

55*9*000 Backlight Off
55*9*001 Backlight On, full intensity

RadioComm Test Commands

Click "FL Off" to disable backlight
Click "FL On-Full" to enable backlight

Verification

Verify that the backlights respond for each issued command.

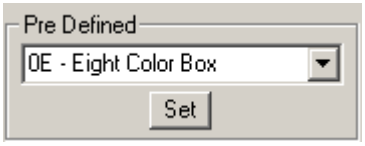
Display Color Test

Handset Test Commands

55*2*014 Eight Color Box Pattern

RadioComm Test Commands

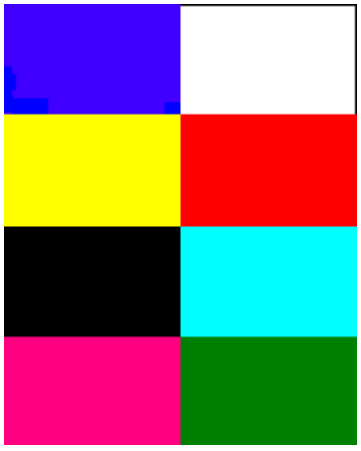
Select Eight Color Box and click “Set”



Verification

Verify that the color pattern on the phone’s display matches the color box in figure 23. Also verify edges (uniform/smooth).

Figure 20. Eight Color Box Pattern



Display Linearity Test

Handset Test Commands

55*2*005 Grey Scale Block

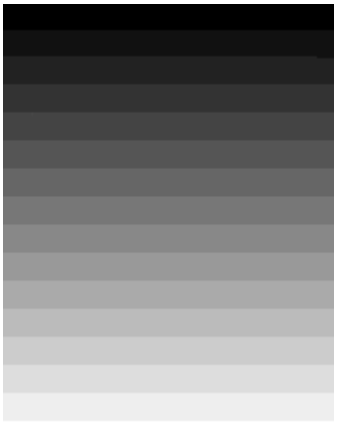
RadioComm Test Commands

Select Grey Scale and click “Set”

Verification

Verify that the Grey scale block on the phone’s display matches the Grey scale block in figure 14. This test can also be used to confirm that the color intensity is linear.

Figure 21. Grey Scale Block



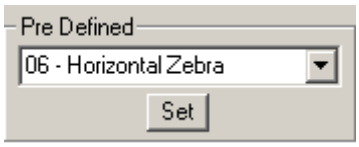
Display Flicker Test

Handset Test Command

55*2*006 Horizontal Zebra Line

RadioComm Test Commands

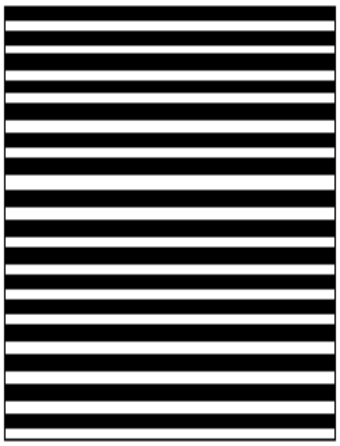
Select Horizontal Zebra and click “Set”



Verification

Verify that no noticable flicker exists.

Figure 22. Zebra Pattern



Display Pixel Defect (Bright)

Handset Test Commands

55*2*001 All pixels on (all white)

RadioComm Test Commands

Select All Pixels Off and click “Set”

Verification

Verify that no greater than two pixels are off.

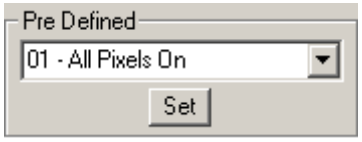
Display Pixel Defect (Dark)

Handset Test Commands

55*2*000 All pixels off (all black)

RadioComm Test Commands

Select All Pixels On and click “Set”



Verification

Verify that no greater than two pixels are on.

LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

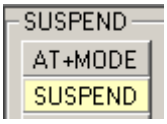
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Status LEDS

Handset Test Commands

62*3*3*012[1] Enable Red LED
62*4*3*012[1] Enable Green LED
[1]000 to disable

RadioComm Test Commands

Select Red LED or Green LED to enable. Deselect Red LED or Green LED to disable.

Verification

Verify that the Red and Green status LEDS activate.

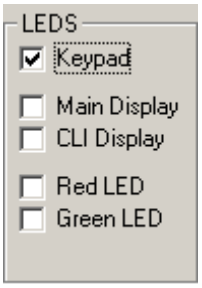
Keypad Backlight

Handset Test Commands

62*0*1[1] Enable Keypad Backlight
62*0*0[1] Disable Keypad Backlight
[1]Leave field 3 blank and press OK

RadioComm Test Commands

Select Keypad to enable. Deselect Keypad to disable.



Verification

Verify that all keypad backlight LEDs activate.

Bluetooth Tests

Use the following procedures to verify functionality of the Bluetooth device integrated in the phone.

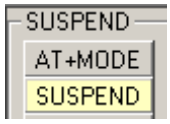
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



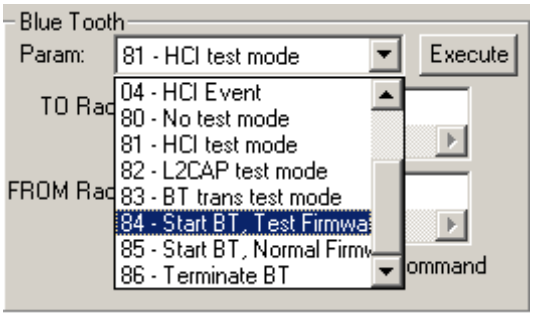
Unmodulated CW TX test

Handset Test Commands

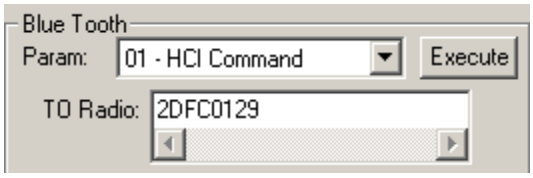
Not Supported

RadioComm Test Commands

Under Bluetooth, select parameter 84 and click execute, then select 81 and click execute.



Under Bluetooth, select parameter 01 and enter 2DFC0129 in the "TO Radio" field. Click Execute.



NOTE: The Bluetooth TX signal will activate momentarily once the HCI command is issued. You must have the RF probe positioned for measurement once you click execute.

Verification

Verify that a 2441MHz signal is present. If the phone is closed, use a RF probe to sniff the strongest signal around the "7" key of the keypad. If the phone is open (shields off), verify that -2dBm to +4dBm is read from R320. An high impedance RF probe is required to read this range. Use of lower quality RF probes will result in signal level differences.

Camera Testing

This section is intended to describe the procedures that will determine whether the camera function of a Motorola terminal is under normal operating conditions.

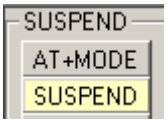
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

Not supported

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click USB Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

The following hardware will be required to properly test the camera function of the phone.

1. Desktop Charger (SPN5032A or equivalent)
2. USB or RS232 control interface (refer to figure 4)
3. Fast Rate Charger (SPN5078A or equivalent)
4. Hardcopy of Macbeth Color Chart
5. Hardcopy of Focus Chart
6. Hardcopy of Grey Chart

Camera Test Configuration

Use any color printer to print a hardcopy of the Macbeth color chart. The Focus chart and Grey chart can be printed using any B/W printer.

For best results follow this recommended setup,

1. Attach chart to a flat vertical surface (wall)
2. Attach the phone to the desktop charger
3. Attach the control interface to desktop charger
4. If necessary, attach power supply to control interface.
5. Turn on phone.
6. Select Camera option in phone
7. Position Desktop charger so that the camera test chart completely fills the viewfinder.

Assign a permanent space in the test lab for these test procedures. Always use the same lighting conditions. Also, it's recommended that a "golden picture" is saved and used for comparison.

There is a variety of ways the camera test charts can be attached to a vertical flat surface. They can be taped, tacked, attached to flip charts, etc. Use your best judgement.

The desktop charger is being used as a fixture to position the phone for test, therefore, it's recommended that the desktop charger is attached to a countertop to prevent any movement.

Figure 23. Camera Test Configuration

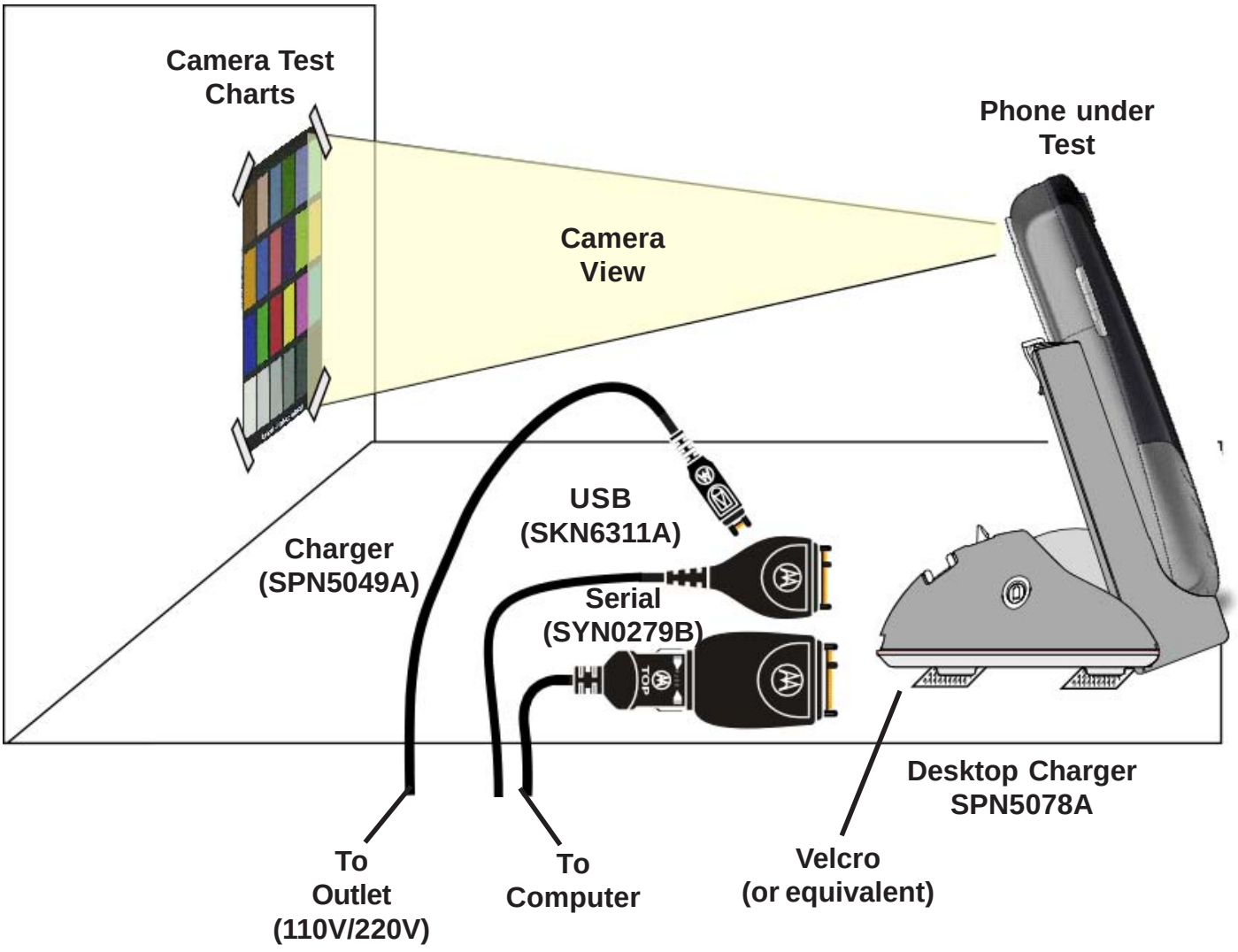


Image Capture

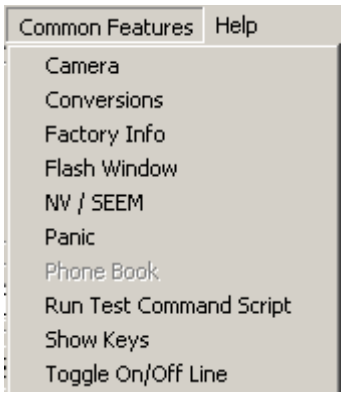
The listed steps should be followed to capture three images (1) the Macbeth color chart, (2) the focus chart, and (3) the grey scale chart. The user will be required to print all images found in Appendix A.

Handset Test Commands

Not supported

Radio Comm Test Commands

Under "Common Features" select Camera



Click "Take Picture"

Once the picture is captured, it'll be displayed on the screen. Click "Save To File"

Macbeth Color Chart

1. From the computer, open the captured color chart image.

2. Compare, the color blocks of the printed Macbeth color chart to the captured image.

Follow the listed verifications to determine the quality of the image.

1. Minimal noise level for Blue, Green and Red on blocks 19 through 24.

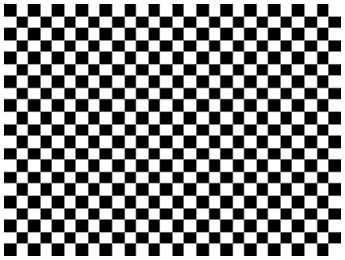
2. Uniformity for grey scale blocks 19 through 24.

3. Good white balance on blocks 19 through 24.

4. Good color reproduction on blocks 13 through 18.

Focus Chart

1. From the computer, open the captured focus chart image.



Verify the focus quality at the center, top-left corner, bottom-left corner, top-right corner, and bottom-right corner.

Grey Scale Chart (Shading Test)

1. From the computer, open the captured grey scale chart image.

Verify that there is minimal shading deviations on all four corners when compared to the center of the image.

GPS Testing

This section is intended to describe the procedures that will determine whether the AGPS function of a Motorola terminal is under normal operating conditions.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

RadioComm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click USB Initialize and click SUSPEND when initialization is complete
(USB Only)

GPS Software Check

Handset Test Commands

Not recommended

RadioComm Test Commands

Under VERSION select GPS Chipset version

Verification

Verify that GPS software version is displayed.

GPS RF Connector Check

Handset Test Commands

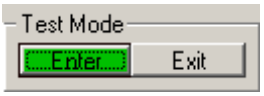
Not supported

RadioComm Test Commands

Under SUSPEND_COMP, select 01-GPS Chipset and UnSuspend.

Click Execute

Under Test Mode, click Enter



Verification

Measure the DC voltage on the center of the GPS RF connector. Verify that the GPS DC voltage reads within 2.69Vdc to 2.86Vdc.

Theory of Operation

Introduction

The A835 is a 3G device. It will deliver on the "promise" of 3G by providing high speed network access and rich multimedia content all in a superior voice-centric unit. A video camera and Assisted GPS provide additional value by offering unique business and entertainment solutions.

The mechanical architecture features a 176 x 220 pixel, 0.198mm pitch TFT activecolor display, a built-in speaker phone, and a removable Li-Polymer battery. The architecture enables full postponement of the front housing and battery door cover by allowing the transceiver brick assembly, keypad, display, microphone, and earpiece speaker to be fully assembled and retained within the rear housing chassis.

Front covers may then be snapped in at distribution based on specific orders. Front housing branding is accomplished through thermal transfer decals.

As a 3G product, the A835 complies with all key specifications as defined by the 3GPP. Key product features are:

- UMTS: WCDMA 2100, GSM 900/1800 and 1900-MHz Tri-band technology,
- GPRS High speed packet data (64kbps UL, 384 kbps DL)
- 176 x 220 TFT Active Color, 64k colors
- 64MB Integrated Flash Memory
- Integrated Bluetooth
- MP3 Player
- Enhanced Multimedia Capability (Audio/Video, Games, MMS)
- Unique 5-way Navigation Key
- New graphical user interface
- Enhanced internet browser (XHTML)
- Full Personal Information Manager (PIM) with SyncML Synchronization (OTA, Desktop)

Figure 24. A835 Transceiver

- Integrated Video/Still Camera and GPS
- Voice Recognition Driven Dialing and Menu Shortcuts
- Voice Note Voice Recorder
- Polyphonic Speakerphone
- Programmable (J2ME)
- iTAP™ Predictive Text Entry
- Integrated Stereo Headset Jack

Video Camera Features:

- JPEG Image Capture @ VGA Resolution
- MPEG4 Video Capture @ QCIF Resolution
- Two imagers (take pictures and video of others or yourself)
- Streaming Video
- Tightly Coupled, Ergonomic Design
- Initial User Applications:
- Sending captured Video Clips and Pictures through MMS, Email, or
- Internet channels
- Simultaneous Voice/Data – Take a picture or video clip and send while you're on the phone
- Future Capabilities:
- Video Conferencing (2-Way Video Telephony)

Location (AGPS) Applications:

- Get to specific location, with appropriate choices of destinations and routes and guidance to destination
- Identify local places of interest for hotels, taxi companies, restaurants, theatres, sightseeing, and shopping
- Receive information through alerts or display on map ahead of traffic congestion.
- • Receive roadside assistance, with rescue service network and location information from the cellular network used to complement any information the pedestrian/driver is able to separately give.
- E911 Services: When roaming on a 2-2.5G GSM E-OTD-enabled network the mobile phone will respond to a request for location when making an emergency call (Please refer to future AGPS MRS for further details).
- Push, Tracking & B2B Applications such as corporate tracking, routing, fleet management, and Buddy tracking (alert)

Baseband Electrical (Digital)

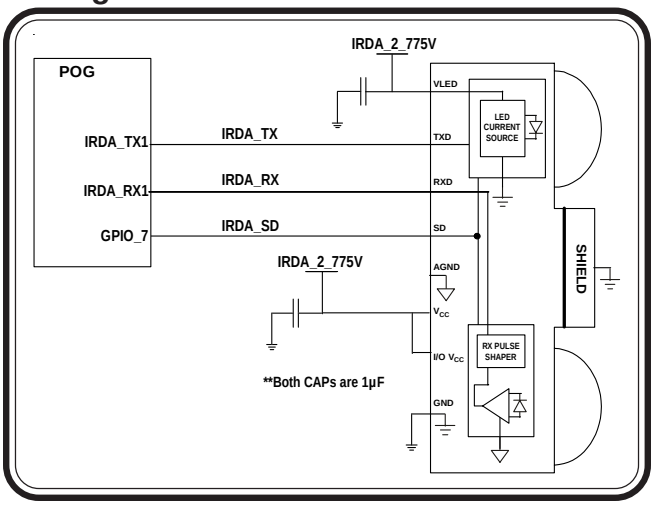
Display Interface

The display uses two programming interfaces, RBG(Red Green Blue) and SPI(Serial Peripheral Interface). The RGB interface is the primary communication bus for the display. It controls how the pixels are displayed. The SPI interface is used for state configurations of the display module. Some states include sleepmode, active, and video modes.

IrDA Interface

The IrDA interface is used to allow infrared data communications between the cellular transceiver and an IrDA device. The IrDA interface will conform to a 30 degree cone angle. The POG IC has integrated the data communications bus for the IrDA device. The IrDA device has a standard baudrate of 9600bps.

Figure 25. POG - IrDA Interface

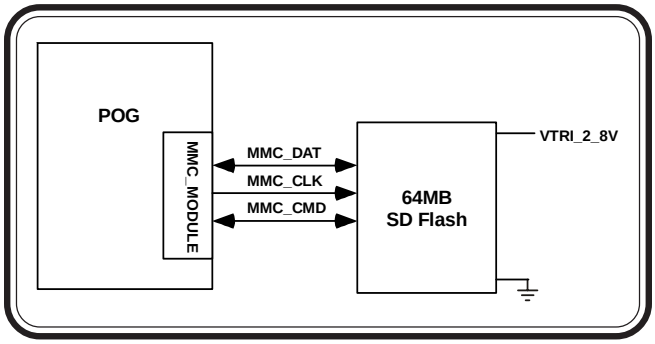


SD Flash Interface

The A835 will interface with an embedded 64 MB NAND flash device. The embedded flash device is a high-density flash memory IC that gives the user the ability to store personal files and use them in low-bandwidth applications.

The MMC/SD interface will operate at 2.8V. The MMC mode will be used; the MMC module in POG does not support SPI mode. The MMC module in POG supports only single bit data transfers at a maximum of 20MHz. Since the MCU will be operating at 90MHz (not 100MHz), the maximum MMC frequency will be 18MHz.

Figure 26. MMC/SD - Block Diagram



Keypad Interface

The keypad processor on the POG can support up to an 8 x 8 row-by-column keypad matrix. However, this keypad matrix will use a line configuration and not a row-by-column configuration. In the line configuration, when a key is pressed, two different signals will be shorted through the key's switch to ground. Keypad backlighting is controlled by the PCAP. The available backlight settings will be "On" and "Off."

Digital Logic

The baseband architecture will consist of a POG / PCAP based architecture. The POG IC integrates a 32-bit RISC Communications Engine (M-Core), a 32-bit SC140 Quartz DSP core, and an Interprocessor Communications Module (IPCM) along with associated peripherals to provide the main phone processing. The PCAP will handle all of the power supply requirements, analog audio circuitry, and control for numerous other functions.

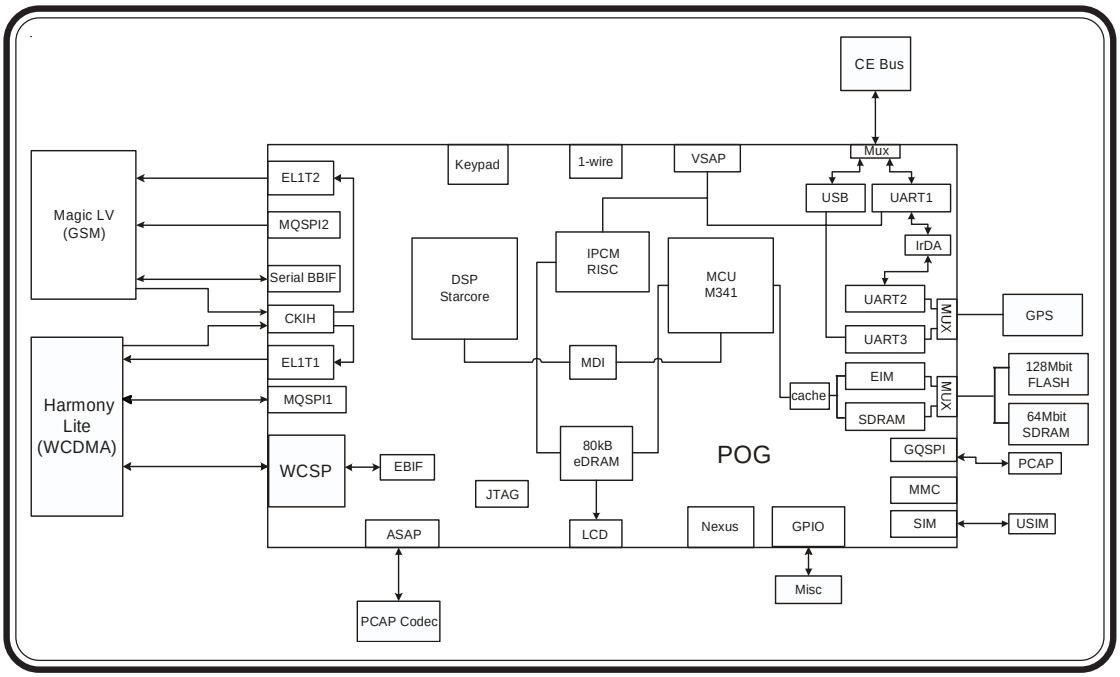
POG is the baseband processor IC of the 3G chipset solution. POG is crafted to provide a high performance embedded solution at low power for 3G mobile devices. POG is a TriCore processor IC integrating a powerful DSP core, a 32bit MCU RISC core with unified cache and a custom 32bit RISC engine for data movement across the processing domains.

The DSP core is a high performance StarCore with four parallel ALUs, the SC140, with a novel Variable Length Execution Set (VLES) architecture which maximizes the execution of multiple instructions in a single clock cycle. The SC140 enables the emergence computational intensive communication applications. The SC140 is assisted by 3G specific hardware accelerators and timers to optimize performance and power. As part of the 3G support, the Wideband CDMA Signal Processor (WCSP) module implements modem functions required by the CDMA subscriber unit in accordance with the 3GPP specifications.

The 32bit MCU RISC core is the M*Core M341 designed for high performance and low power embedded systems. The M341 embodies an 16K unified cache, integer multiplier and MMU in support of virtual memory management OSes.

Data communication across the cores is handled by a flexible 32bit RISC machine, the Inter Processor Communication Module (IPCM). The IPCM supports flex-

Figure 27. POG Block Diagram



ible data flow between the MCU, DSP and the multimedia peripherals.

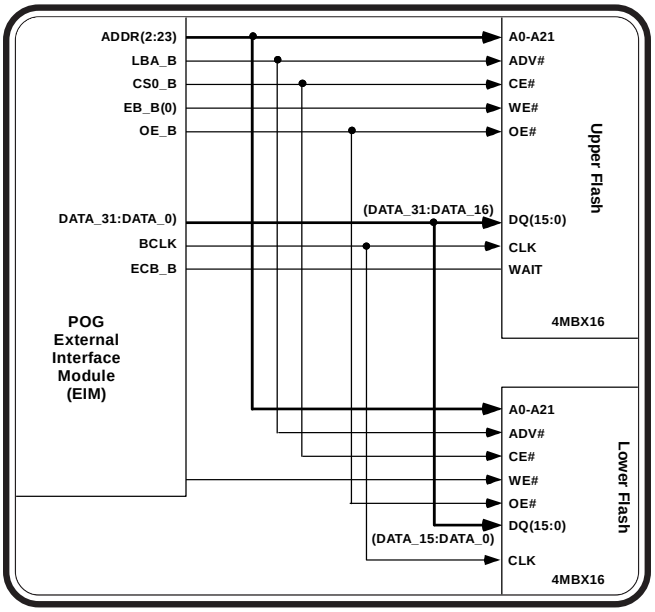
A video buffer is embedded as SRAM memory to optimize display rendering while lowering power. POG offers an advanced SDRAM controller to maximize external memories throughput.

Flash Memory

The software requirement is for 128Mb of flash memory. Memory is divided into 16 partitions of 8Mb each. There is one parameter partition and 15 main partitions.

Two 16-bit W18 ICs will be required to meet the 128Mb requirement. The Intel flash is packaged in a 56 active ball BGA packages with .75 mm ball pitch and 7.7 x 9.0 mm footprint.

Figure 28. Flash Memory Block



Power Supply Architecture

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isloation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are illustrated below.

Figure 29. PCAP Power supplies - 1

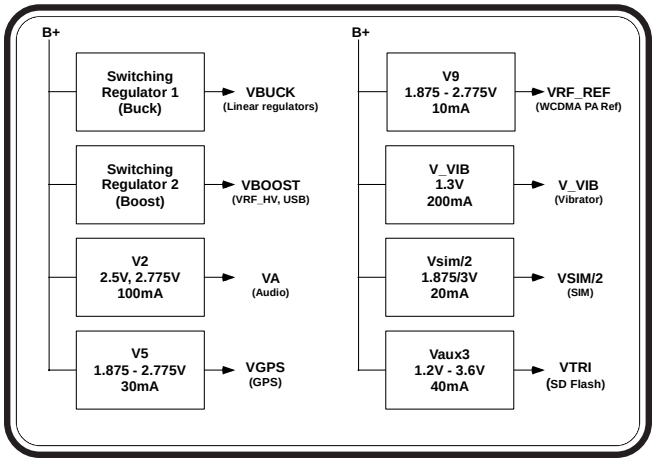


Figure 30. PCAP Power supplies - 2

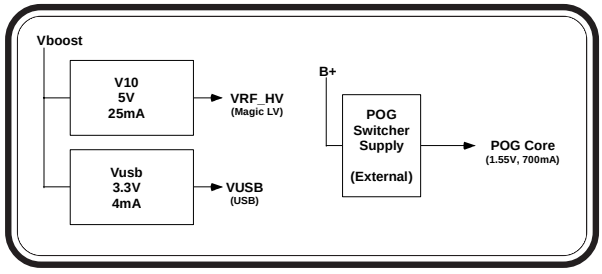
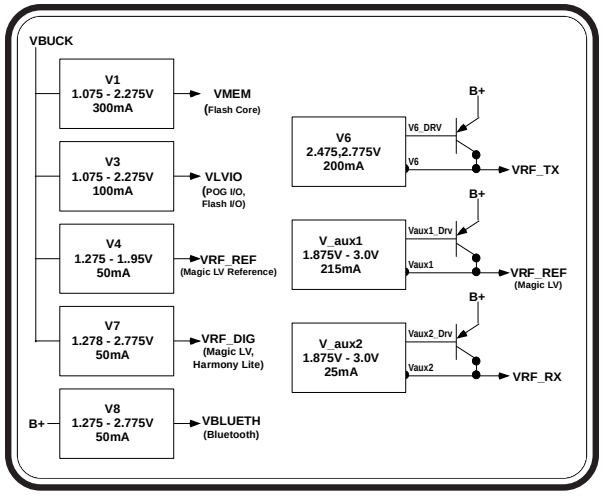


Figure 31. PCAP Power supplies - 3

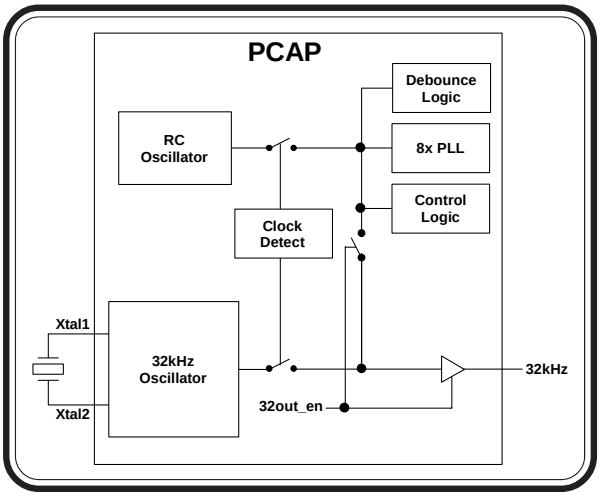


Clock Generation

PCAP can genrate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stabilty that the Rainbow requires for optimal performance, therefore, an external 32.768kHz crystal is used.

The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Figure 32. PCAP 32kHz Clock



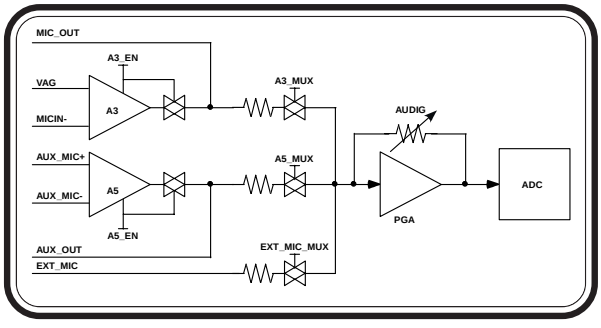
PCAP Audio

TX Audio

The A830 supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single endedwith respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 and R4101 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R4102 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

Figure 33. TX Audio Block



The headset microphone path is biased through R4396, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by using R4399 as a pullup resistor and detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

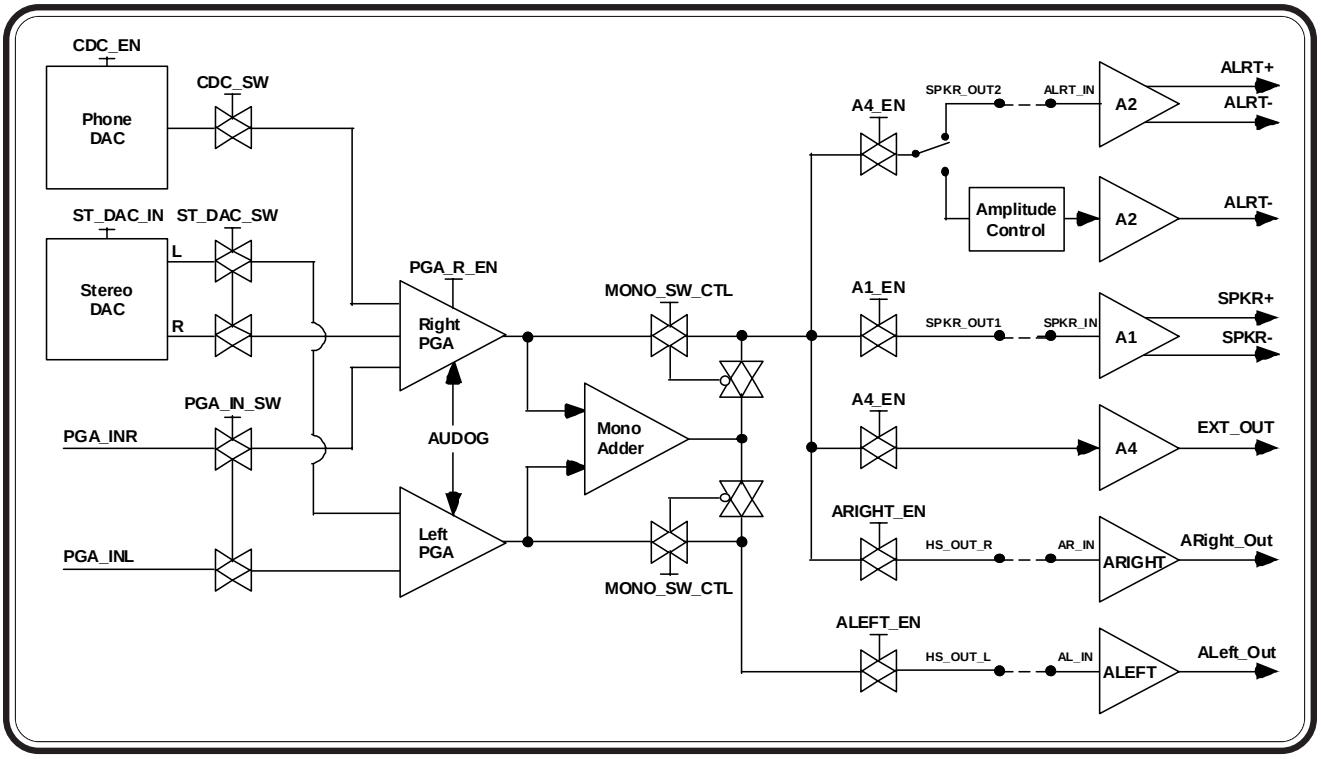
The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loadspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight/ALeft Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R34003 and R34002 respectively, and then connected to the transducer. Off the Speaker-path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to

Figure 34. RX Audio Block



Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R34304 and C4306, R34303 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ARight_Out path, AL_IN is tapped off through C4354 for the inverting input of the audio amp ALEFT.

The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to

PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

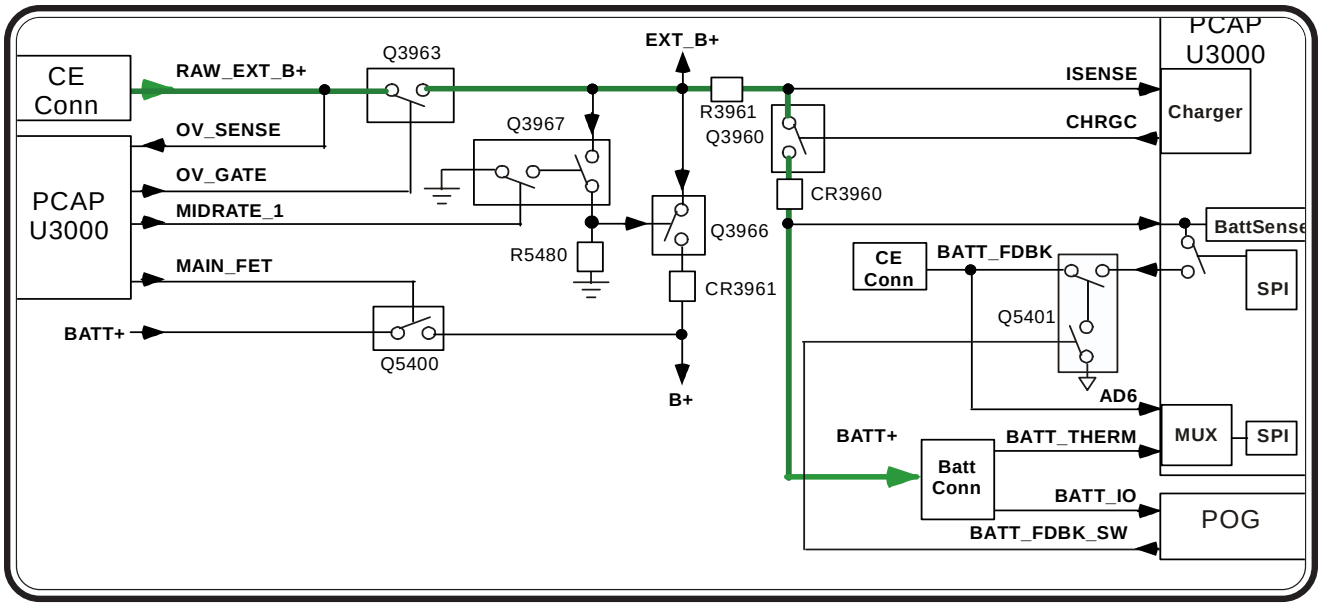
Battery Interface

Batteries interface to the main transceiver board via a 4-pin connector (J5400). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q5400 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U3000) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J5000). During full rate charging, Q3966 is turned ON so that current can be supplied from the external source to B+. Q5400 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q3960. A sense resistor (R3961) provides current sense feedback to the

Figure 35. Battery Interface Block



charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J5000). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Bluetooth

The Broadcomm 2033 Single Chip Bluettoth soultion is being used with this mobile phone. The BMC2033 is a Bluuetooth 1.1 compliant stand alone baseband processor with an integrated 2.4GHz transceiver. The baseband section controls all bluetooth functionalityfrom the physical layers to the HCI layer. The radio section includes PLL, VCO, LNA, PA, upconverter, downconverter, modulator, demodulator, and channel select filtering.

The fractional- N synthesizer can support multiple reference freqwuencies, including 13MHz and 15.36MHz.The UART interface between Rainbow and BCM2033. The SSI interface between Rainbow, PCAP and BCM2033.

RF GSM Receiver

The RF architecture is a dual mode and quad band architecture supporting GSM at 900MHz, DCS at 1800 MHz, PCS at 1900 MHz and WCDMA at 2100 MHz. It is a dual receiver architecture allowing simultaneous decode of GSM and WCDMA channels to minimize the need for compressed mode operation. Although the architecture supports dual receivers, the design uses only a single antenna by employing a sophisticated diplexing scheme.

The GSM architecture is a direct launch/direct conversion architecture built around the Magic LV and LIFE IC's. The LIFE IC is a direct conversion receiver which converts GSM/DCS/PCS RF signals to analog I & Q.

Figure 36. Bluetooth Block

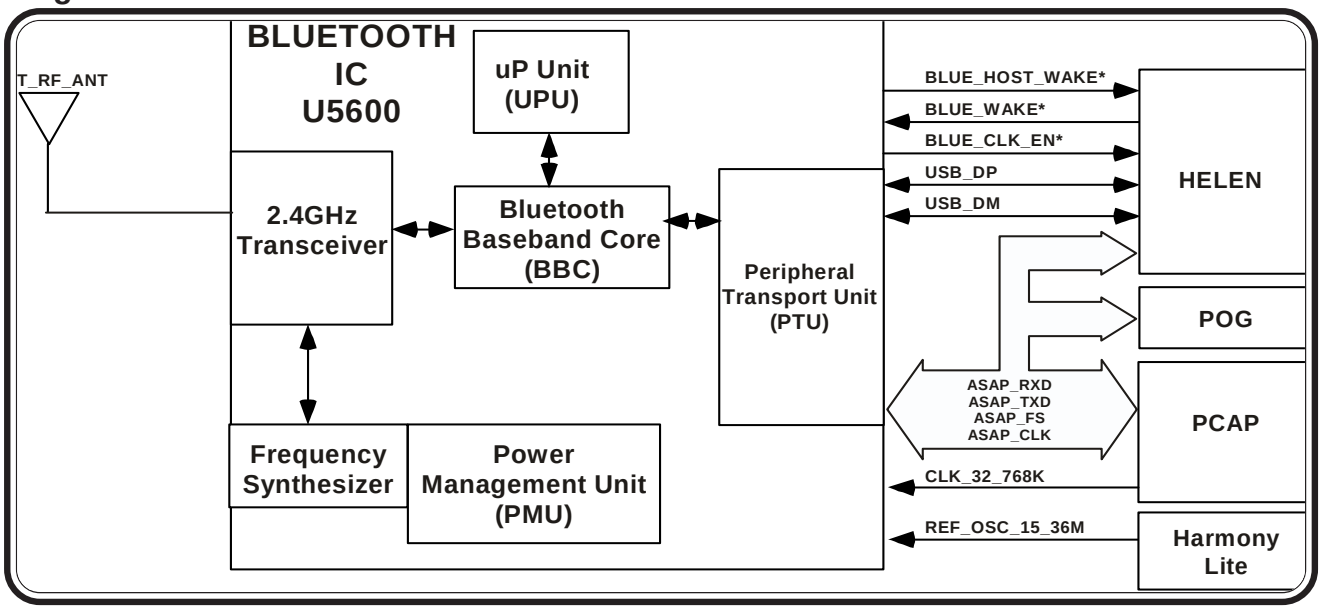
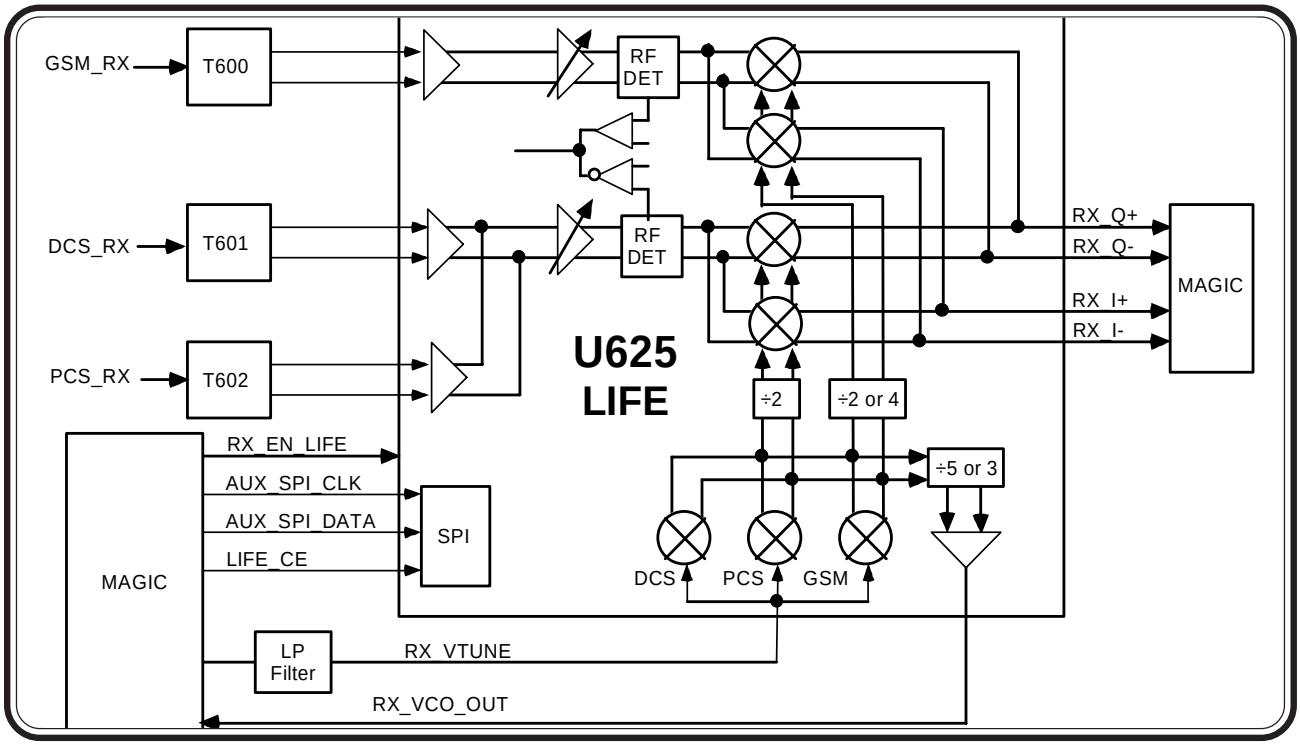


Figure 37. LIFE Block



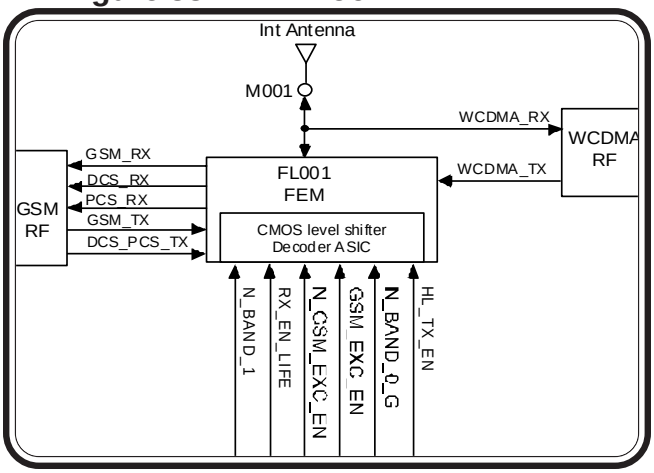
Receive analog I & Q is converted to digital signals and fed to the DSP within Rainbow by the Magic LV.

The received signal from the antenna is fed to the FEM(Front End Module) through antenna matching components. The FEM is used to route a particular band (GSM, DCS or PCS) to it's proper RX and TX path. Band selection is done by control lines N_BAND_1 and N_BAND_0_G. Mode selection is done by control lines HL_TX_EN and RX_EN_LIFE.

Once the received signal passes through the FEM, it is fed into one of three transformers, depending on the band, for differential conversion which is then fed into the LIFE IC (U625). The LIGE is a Low IF Front End complete reciever for GSM/DCS/PCS. The following lists the key components within the LIFE IC.

- Four LNAs with balanced inputs
- Two quadrature mixer paths
- Three integrated RX VCOs at 4 GHz
- Bufferred VCO output
- SPI bus for AGC, transformer match, VCO control, and band switching
- All signals within the IC are differential

Figure 38. FEM Block



The differential receive signal is fed into a LNA, AGC amplifier, RF detector, and mixer. The mixer output will be the differential IQ signals which are sent to the Magic IC.

The integrated VCOs within the Life IC provides the channel selectivity function for the receive signals passing through the LIFE IC. The VCO frequency is controlled by the RX_VTUNE line. For proper frequency stabalization, the generated VCO signal is fed to a PLL via RX_VCO_OUT.

The MagicLV IC will provide digital conversion of the received IQ signals which are then sent over the SPI bus to the baseband section. The following provides a functional overview of MAGICLV.

- AGC control for the PMA and AMP
- Level detector for the Sigma Delta Modulator overload - not used
- High dynamic range band pass Sigma Delta Modulator converter
- Complex mixer for the active image rejection
- Programmable and phaseable digital IF to improve image rejection
- Dual Port modulation
- All TX power control functionalities except for RF detection
- Faster PLL lock time and DC adapt time
- Superfilter and four tracking regulators to power the main VCO and IC
- Auxiliary SPI bus which allows the processorto communicate with only one device to control other RF ICs such as the LIFE
- Greater AGC free dynamic range
- 10 bit AOC DAC for greater resolution

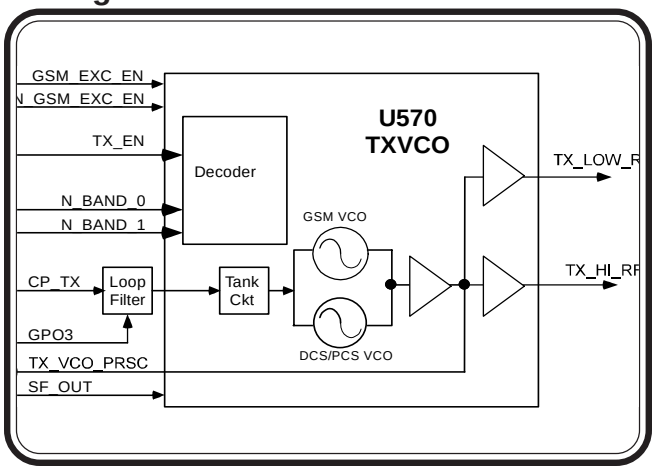
RF GSM Transmitter

Any TX data that needs to be sent will be transmitted from the POG IC to the MagicLV via the SSI bus. The data received through the SSI bus is sampled by selecting 1 of 16 GMSK waveforms found in the Look-up Table ROM. This waveform will then be the input to a 9-bit D/A, which will output an analog format that follows the waveform. This signal is then coupled into a loop filter to add in the higher frequency components of the modulation which may have been attenuated in the main PLL path. This will allow the use of a lower bandwidth main PLL to improve the spectral purity of the transmit signal.

The loop filter is designed as an active device that reacts to changes in output frequency of the MAGIC modulated charge pump and in addition to performing the 'smoothing' function to stop any discrepancies in CP voltage being fed to the TX VCO, it also adds the high frequency modulation components from the dual port modulation output.

The Charge Pump voltage is now fed to the TX VCO U570. The TX VCO is controlled by a number of signals. The operating band is selected using the N_BAND_0 and N_BAND_1 control lines. A sample of the generated TX VCO is fed back out on PROUT

Figure 39. GSM TX VCO

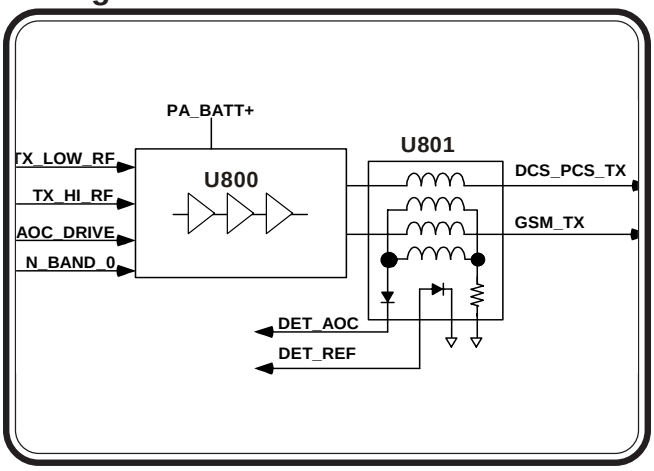


to be used within the MAGICLV as part of the TX PLL.

TheTX VCO signal is then split into the 2 buffers, which are independently switched on or off by the signals N_GSM_EXC_EN & GSM_EXC_EN, which will allow output of the TX output frequency into the correct path. The TX signal is then injected into a Dual PA. Band selection for the PA is done with N_BAND_0. The gain of the PA is adjusted with AOC_DRIVE.

The automatic output design consists of a power detector, detector ADC, and TX IF AOC. The power detector U801 couples the radiated power from the output of the PA and then rectifies it into a DC level (DET_AOC). DET_AOC is then sent to a comparator integrated in the MagicLV IC. The comparator will compare the DET_AOC voltage, controlling the gain of the PA, to the sampled voltage at DET_AOC. Any difference in voltage will be applied to the AOC_DRIVE, thus, correctly tuning the PA power level.

Figure 40. GSM TX VCO



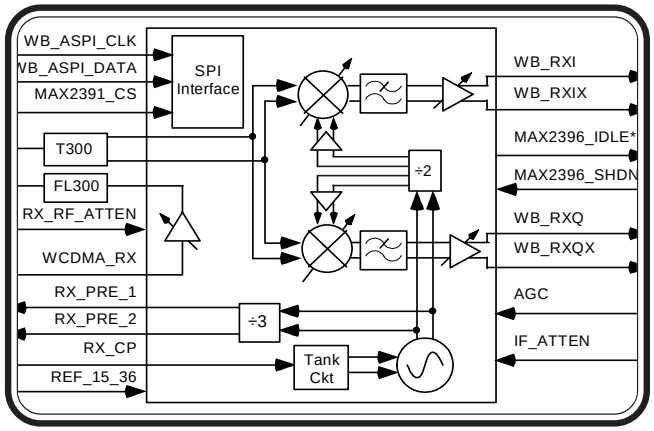
RF WCDMA Receiver

The WCDMA receiver architechture consists of dual conversion, zero-IF receiver which is built around MAX2396, and the Harmony Lite ICs. The MAX 2396 provides the first conversion to provide the receive IF and converts the receive IF signal into analog I&Q signals which are fed into Harmony Lite.

The Max2396 (U300) is a fully integrated direct-conversion receiver IC family for WCDMA applications, targeting the emerging 3GPP market.

The Max2396 provides a complete solution for the 3GPP WCDMA FDD receiver (2110-2170MHz, 3.84Mcps) from antenna to baseband I/Q outputs, eliminating the use of an off-chip IF SAW filter and of RFVCO.

Figure 41. MAX2396 Block



The MAX2396 receiver IC has over 90 dB of dynamic gain control, partitioned between RF and baseband sections. It consists of an ultra-low current LNA with on-chip output matching and two-step gain modes. The zero-IF demodulator has a differential circuit topology for best input IP2 and for minimum LO leakage to receiver‘s input. The channel selectivity is done completely in the baseband section of the receiver with an

on-chip low-pass filter. The AGC section has over 50dB of gain control range. LO quadrature generation is done on-chip trough a divide-by-2 prescaler. The DC-offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop connected over the AGC section. For large DC-offsets transients, very fast settling time is obtain by automatic optimization of the time-constant of the DC-offset cancellation circuit.

The AGC ensures that the I/Q inputs to HARMONY LITE are at constant signal level. The IF_AGC line is controlled by HARMONY_LITE with a DC control range of 1.2V to 2.1V.

The MAX2396 includes a 3-wire serial bus for PLL programming and for configuring the different receiver modes. The MAX2396_SHDN* line is used for full device shutdown and the MAX2396_ILDE* line is used for device idle mode.

RX_RF_ATTEN controls the LNA gain control pin of the MAX2396(U300), allowing high gain mode operation for low RF signal conditions and low-gain mode for high RF signal conditions. IF_ATTEN controls the mixer gain control pin of the MAX2396, allowing high gain mode operation for low IF signals and low gain mode for high IF signals.

The MAX2396 VCO frequency is controlled by an external phase lock loop (PLL) synthesizer found in the Harmony Lite. The VCO output frequency at RX_PRE_1 and RX_PRE_2 is through a divide-by-3 prescalar. The VCO output signal is then fed into the PLL synthesizer found in the Harmony Lite. . The internal phase detector within Harmony Lite drives the charge pump, RX_CP. The RX_CP line drives the tunable resonant network, altering the VCO frequency and closing the loop.

The I&Q signals go through a differential convertion prior to being fed into the Harmony Lite. The Harmony Lite will then convert the analog I&Q signals into digital. The following lists some WCDMA receive functions of the Harmony Lite.

- Autonomous mixed-mode AGC loop
- Digital DC offset correction
- Gain/Phase equalization
- Interleaved 6-bit parallel IQ samples to WCSP latched at 30.72MHz

The digital I&Q signals will then be fed into the WCSP module of the POG where RX bit rate data is converted to chip rate data.

RF WCDMA Transmitter

The Wideband architecture is a dual conversion architecture built around the Harmony Lite, a MAXIM IC and the WCSP (Wideband CDMA Signal Processor), which is integrated in the POG IC. The MAXIM IC up mix the RF signals and modulate analog I&Q. The Harmony Lite IC converts between analog I&Q signals and chip rate data. The WCSP provides the interface between the RF sections and the DSP within the POG. The WCSP converts between chip rate data and TX bit rate data.

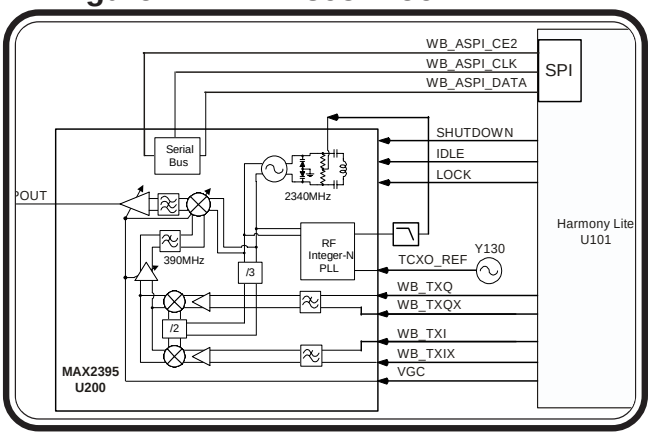
TX data that needs to be sent will be transmitted from the POG through the WCSP and then Harmony Lite. The Harmony Lite will transmit a 300mVpp differencial TXI and Q signal to the MAX2395 IC with a DC bias of 1.4V.

The MAX2395 is a fully monolithic quasi-direct modulator IC for use in WCDMA/UMTS transmitters. The quasi-direct modulation architecture reduces system cost, component count, and board space compared to transmitters using IF SAW filter with IF VCO and IF synthesizer blocks.

The MAX2395 includes I/Q baseband filters, an IF I/Q modulator with VGA, a fully monolithic VCO with

PLL, a up-converter mixer with VGA, and a power amplifier driver. The differential baseband I/Q signals are modulated onto a variable-IF carrier in the 384 396MHz band; The IF signal is then up-converted to the 1920 - 1980MHz band. On-chip Image rejection in the 2688 - 2772 MHz frequency band is done with

Figure 42. MAX2395 Block



an integrated notch filter. The RF VGA and IF VGA provide a nominal 90dB of output power control. The use of the quasi-direct modulator scheme ensures excellent carrier suppression over the total power control range. In addition, only one on-chip VCO and one integer-N PLL are needed to generate both LO signals for the IF and RF sections. The on-chip component matching by monolithic integration at IF frequencies results in excellent phase accuracy and amplitude balance.

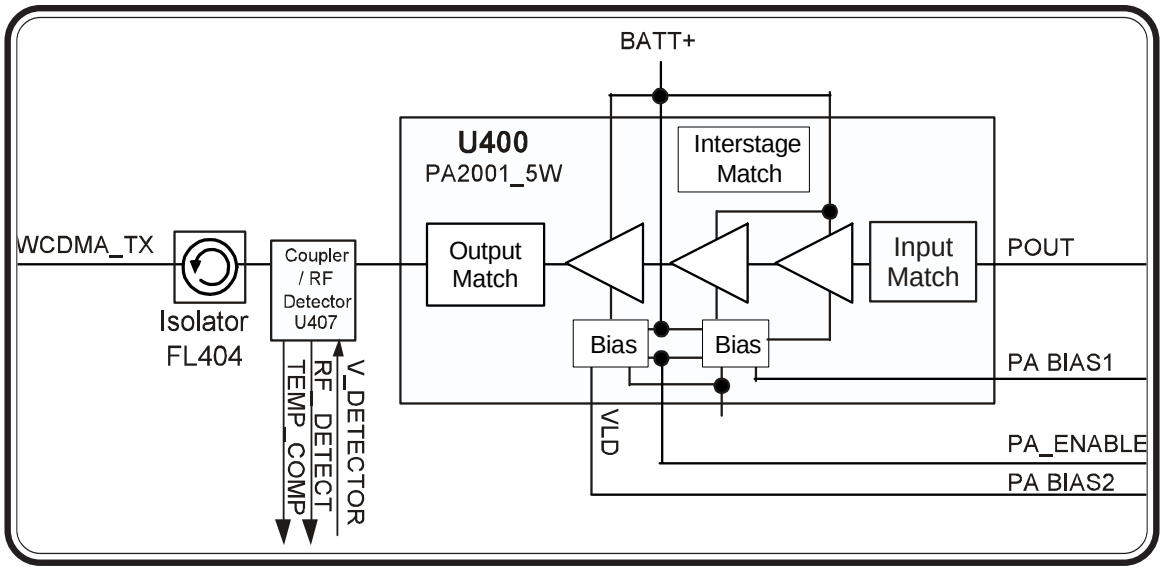
The PLL operation is programmed by loading data on the SPI/Microwire compatible 3-wire serial bus. In addition, the WCDMA required compressed mode can be selected via an external IDLE pin.

The Power amplifier has a gain from 28 to 32 dB for maximum power. During low power mode, the gain of the PA is controlled with TXDAC3 and TXDAC4. TXDAC2 is used to control the load switch for switching to high and low power modes.

The amplified WCDMA carrier is fed into a RF coupler device which has an integrated RF detector. An RF detect and Temp Comp signal will be reported to Rainbow for computing of RF out; used only at high end of the transmitter range.

The isolator provides a stable PA load. It also protects the PA from interfering with other frequency bands. Finally, it gaurds against IM products being produced by the transmitter and affecting receiver circuits.

Figure 43. WCDMA PA Block



Service Diagrams

Introduction

The service diagrams were carefully prepared to allow a Motorola certified technician to easily troubleshoot cellular phone failures. Our professional staff provided directional labels, color coded traces, measurement values and other guidelines to help a technician troubleshoot a cellular phone with speed and accuracy.

We worked hard in trying to provide the best service diagrams, therefore, to avoid cluttered diagrams, we may exclude some components from the service diagrams. Our professional staff carefully selected to excluded components that are unlikely to fail.

Test Point Measurements

The measurements labeled on the service diagrams are approximate values and may vary slightly. These measurements are dependent on the accuracy of the test equipment.

It is strongly recommended that the test equipment calibration schedule be followed as stated by the manufacturer. RF probes should be calibrated for each frequency in which tests are going to be performed.

The types of probes used will also affect measurement values. Test probes and cables should be tested for RF losses and loose connections.

Because of the sensitivity of RF, measured readings will be greatly affected if they're taken in certain locations. To get the most accurate readings, take measurements nearest to the labeled measurement on the service diagram.

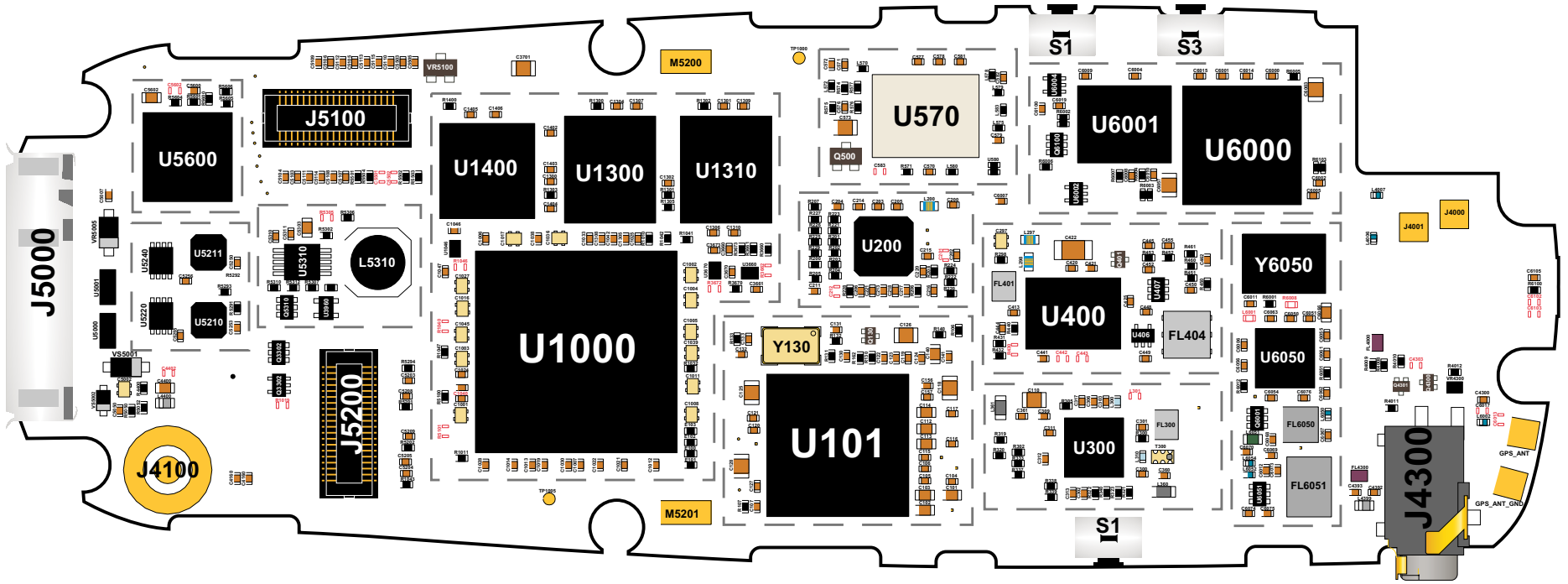
Diagrams

All illustrated diagrams relate to the latest available hardware during development of this document. Some diagrams may deviate slightly in design when compared to actual field returns. Please contact your local Motorola service support center for document updates that may relate to current designs.

The following diagrams are illustration in this section,

- Board Layout Side 1
- Board Layout Side 2
- Signal Flow Diagram
- Schematic Diagrams

Figure 44. Layout Side 1



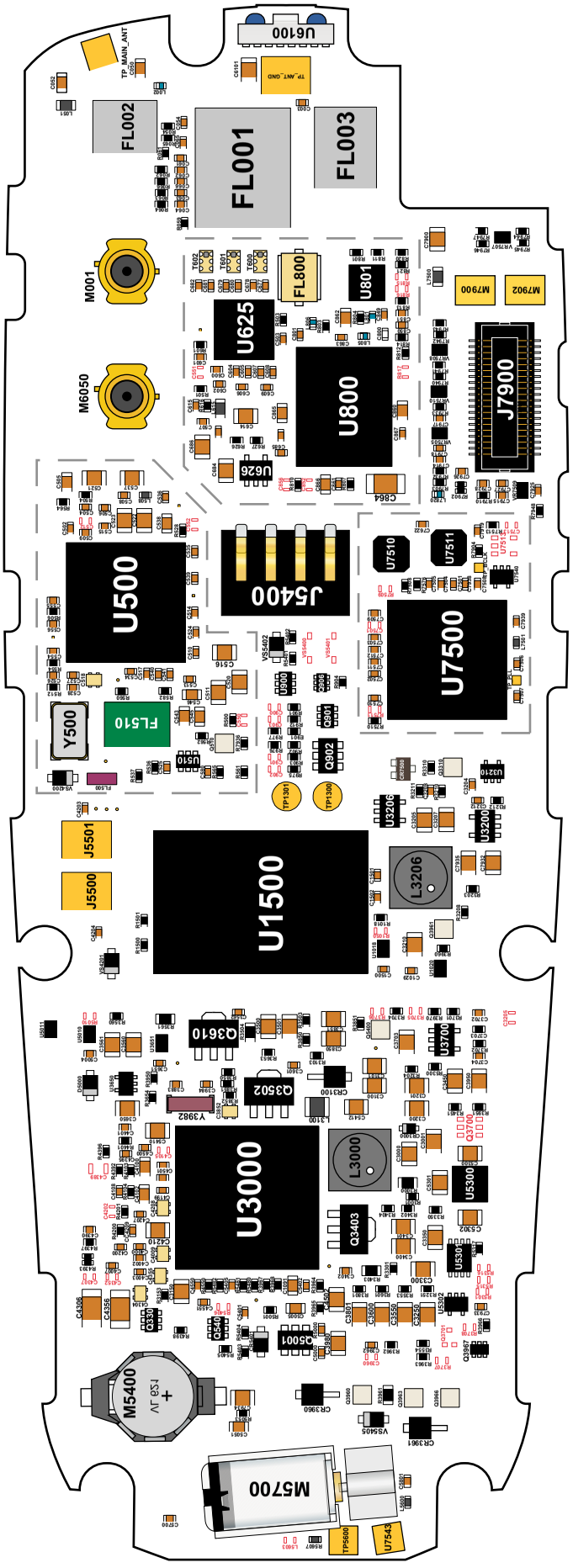


Figure 45. Layout Side 2

Figure 46. Signal Flow - Side 1

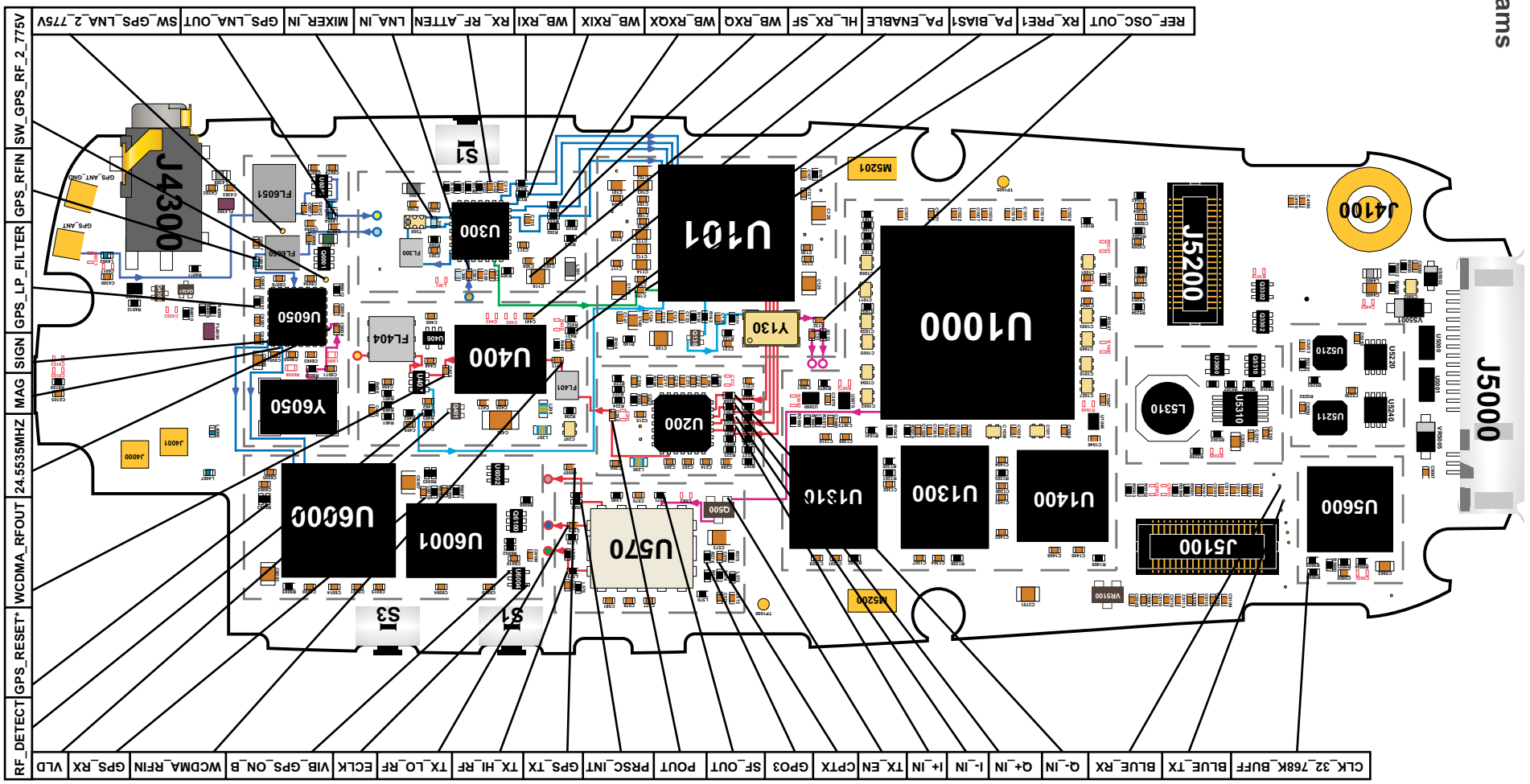
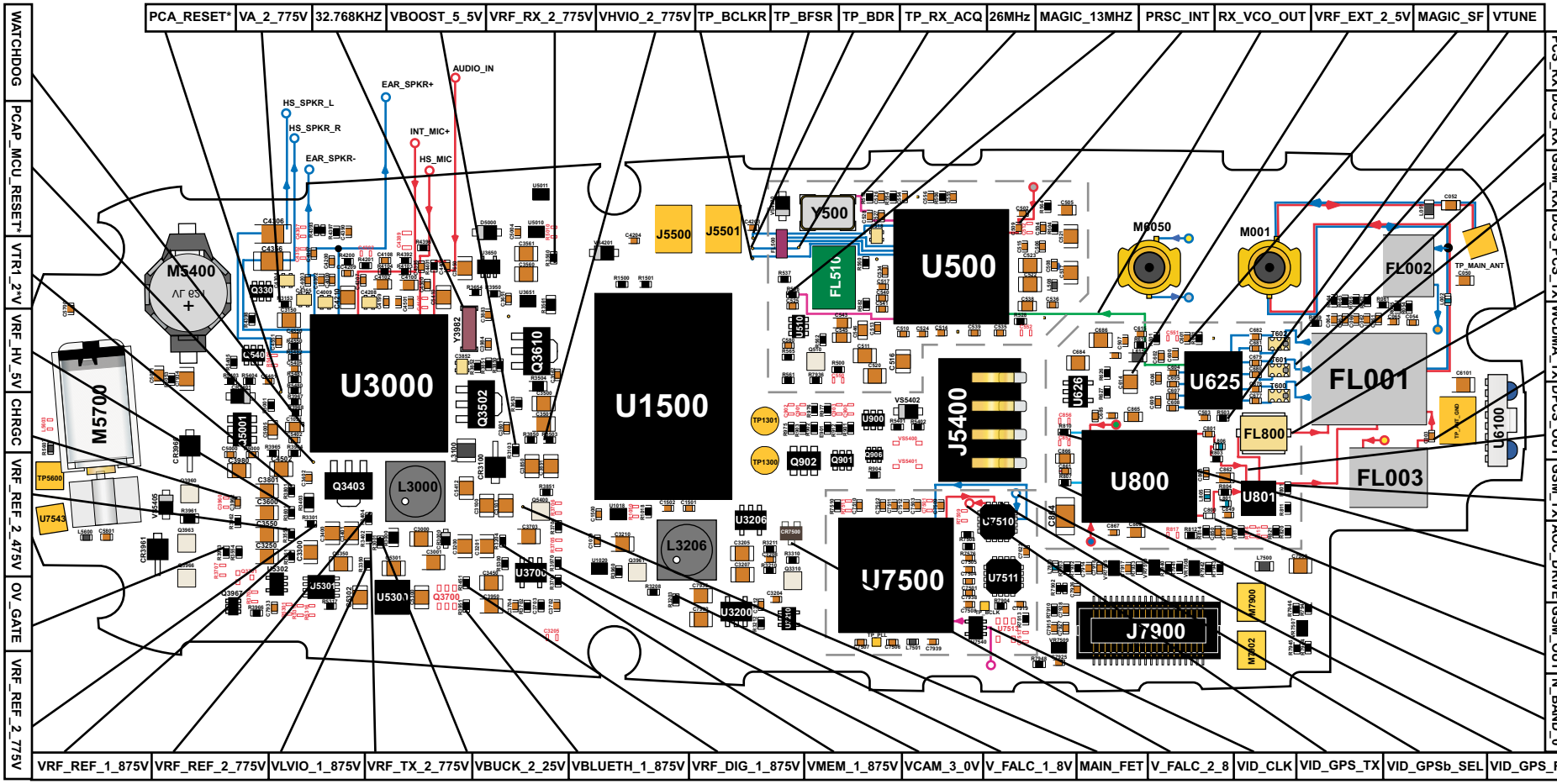


Figure 47. Signal Flow - Side 2



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Drawn by: Ed Naddeo			
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MFG CTRL CHK:	Top Level		
QA CHK:	REV: P6C	Drawing Number: 8487729N06	Page: / Of:
Changed by: Ed Naddeo	Date: January 7, 2003		Time: 10:43:18 am

Baseband

BB_CLK_15_36M
TEMP_SENSE
BBIF_RX_FRM
BBIF_TX_FRM
BBIF_CLK
BBIF_TX[7:0]
BBIF_RX[7:2]
TX_RX_ERROR
HARMONY_CS
WB_SPI_MISO
WB_SPI_CLK
WB_SPI_MOSI
RF_RESET*
BLUE_CLK_EN*
WB_RX_ON
WB_TX_RAMP
WB_RX_ACQ
WB_TX_SLOT
WB_RX_SLOT
AOC_PWR_UP
WB_TX_PREKEY
NB_RX_ACQ
NB_TX_KEYM
NB_TX_EN*
NB_EXC_EN*
DET_FLAG
CLK_SEL
MAGIC_CS
NB_SPI_MOSI
NB_SPI_CLK
REF_15_36
DMCS_MAGIC
BDX
BFSR
BCLKX
BCLKR
BDR
BFSX
BB_CLK_13M
BLUETOOTHCLK
HL_TX_EN

RF

BB_CLK_15_36M
TEMP_SENSE
BBIF_RX_FRAME
BBIF_TX_FRAME
BBIF_CLK
BBIF_TX(7:0)
BBIF_RX(5:0)
BBIF_RX(7:2)
TX_RX_ERROR
HARMONY_CS
WB_SPI_MISO
WB_SPI_CLK
WB_SPI_MOSI
RF_RESET*
BLUE_CLK_EN*
WB_RX_ON
WB_TX_RAMP
WB_RX_ACQ
WB_TX_SLOT
WB_RX_SLOT
AOC_PWR_UP_DOWN
WB_TX_PREKEY
NB_RX_ACQ
NB_TX_KEYM
NB_TX_EN*
NB_EXC_EN*
DET_FLAG
CLK_SEL
MAGIC_CS
NB_SPI_MOSI
NB_SPI_CLK
REF_15_36 (For GPS)
DMCS_MAGIC
BDX
BFSR
BCLKX
BCLKR
BDR
BFSX
BB_CLK_13M
BLUETOOTHCLK
HL_TX_EN

SH01 SHIELD 2688097N01 — GND_RF
SH02 SHIELD 2688098N03 — GND_RF
SH03 SHIELD 2688099N01 — GND_RF
SH04 SHIELD 2688100N01 — GND_RF
SH05 SHIELD 2688101N01 — GND_RF
SH06 SHIELD 2688102N01 — GND_RF
SH07 SHIELD 2688103N01 — GND_RF
SH08 SHIELD 2688104N02 — GND_RF
SH09 SHIELD 2688105N01 — GND_RF
SH10 SHIELD 2688106N01 — GND_RF
SH11 SHIELD 2688107N03 — GND_RF
SH12 SHIELD 2688108N03 — GND_RF
SH13 SHIELD 2688109N03 — GND_RF
SH14 SHIELD 2688110N03 — GND_RF
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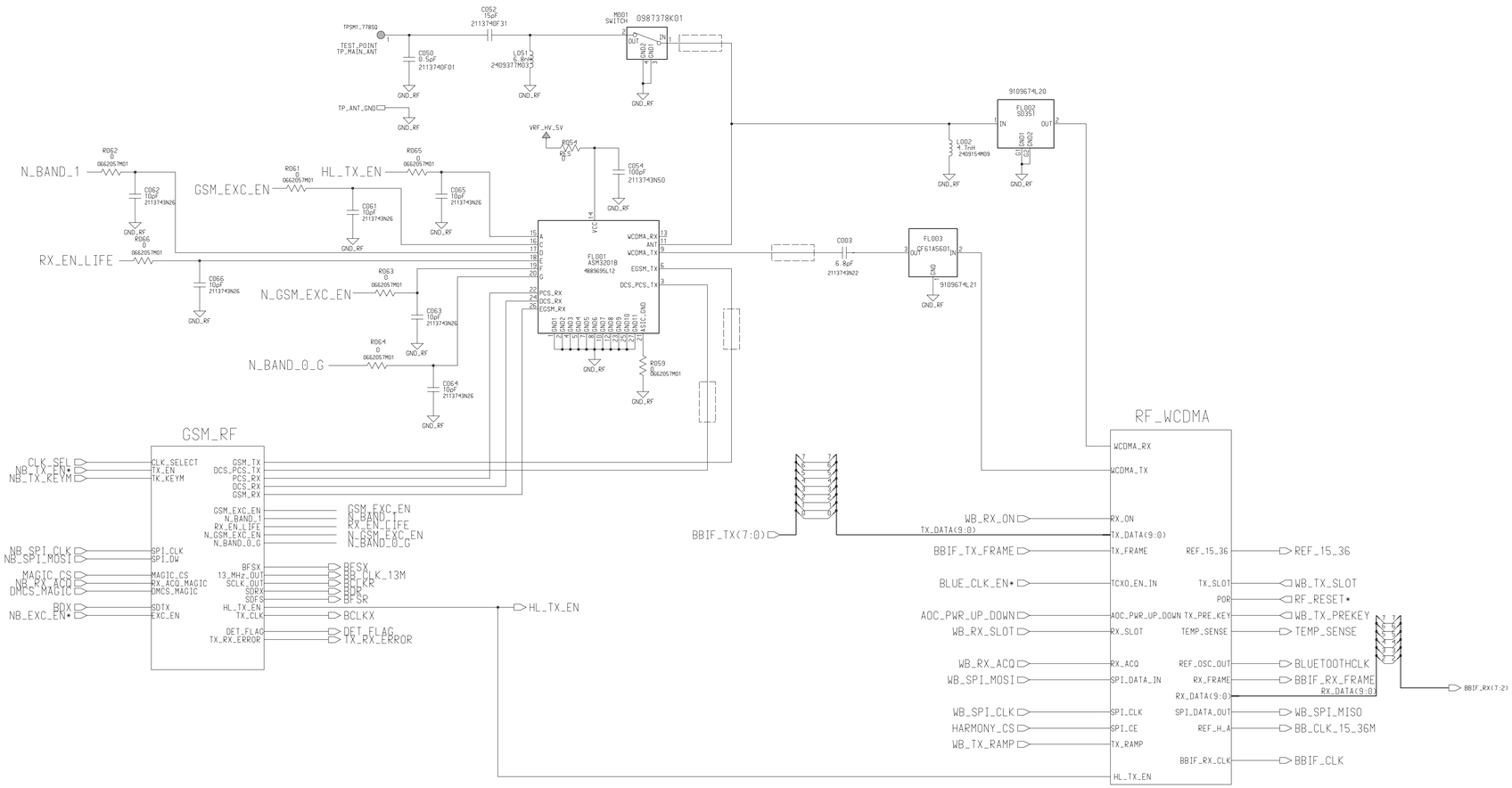
M7900 SHIELD — GND_RF
M7902 SHIELD — GND_RF



Engineer: Dave Suarez	MOTOROLA INC, 600 N US HWY 45 Libertyville, IL		
Drawn by: Dave Suarez			
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MFG CTRL CHK			
QA CHK	REV: P6C	Drawing Number: 8487729N06	Sheet of

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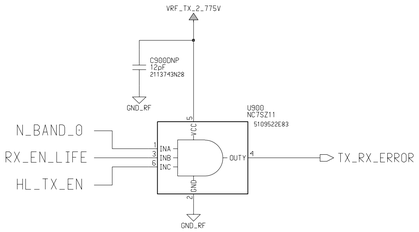
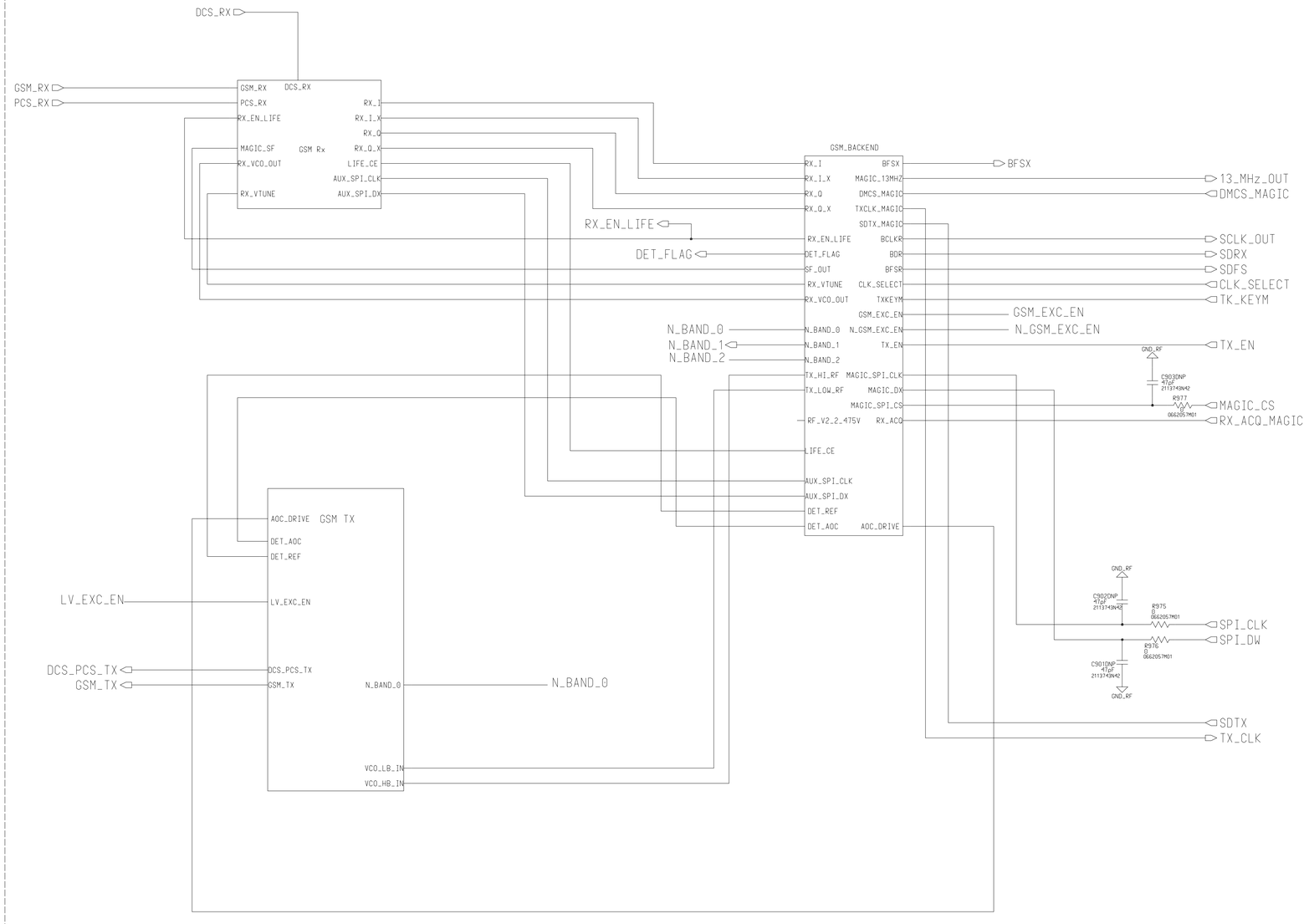
Dave Suarez	July 30, 2003	3:59:05 pm

Band Select Circuits REF # 900-925





Engineer Dave Suarez	COMPANY NAME Address City		
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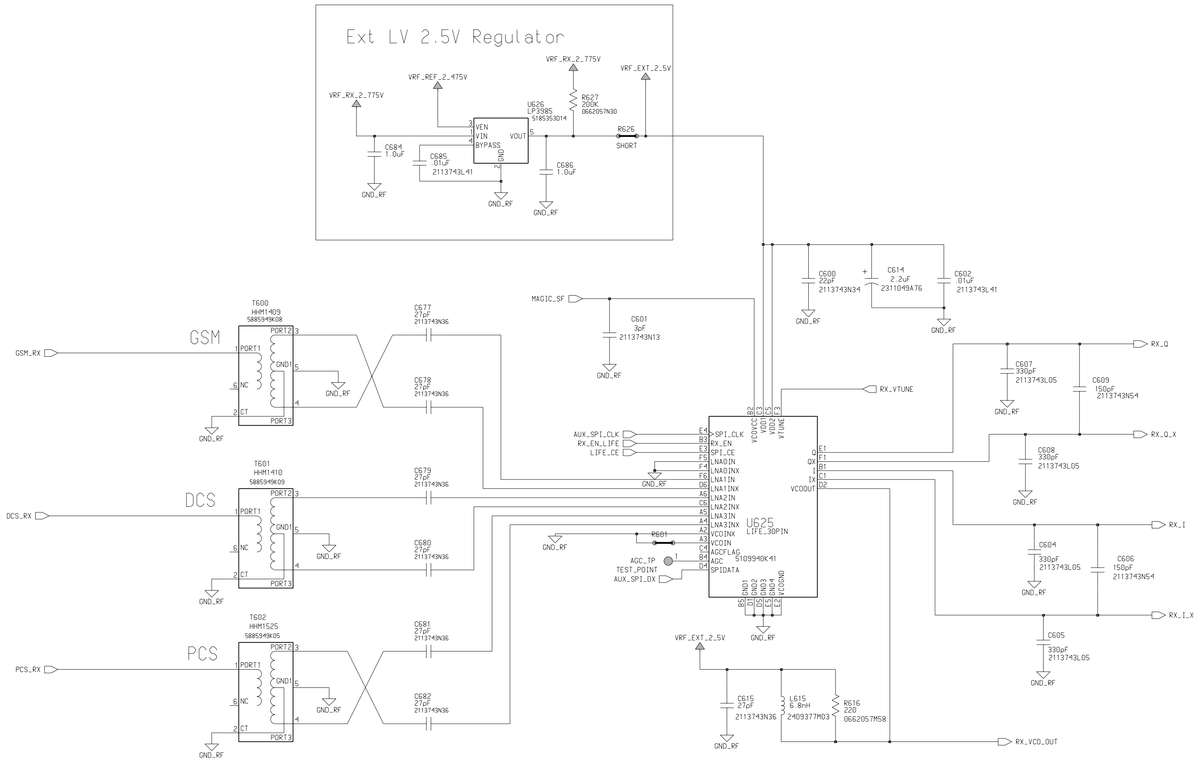

LIFE IC
REF # 600-649

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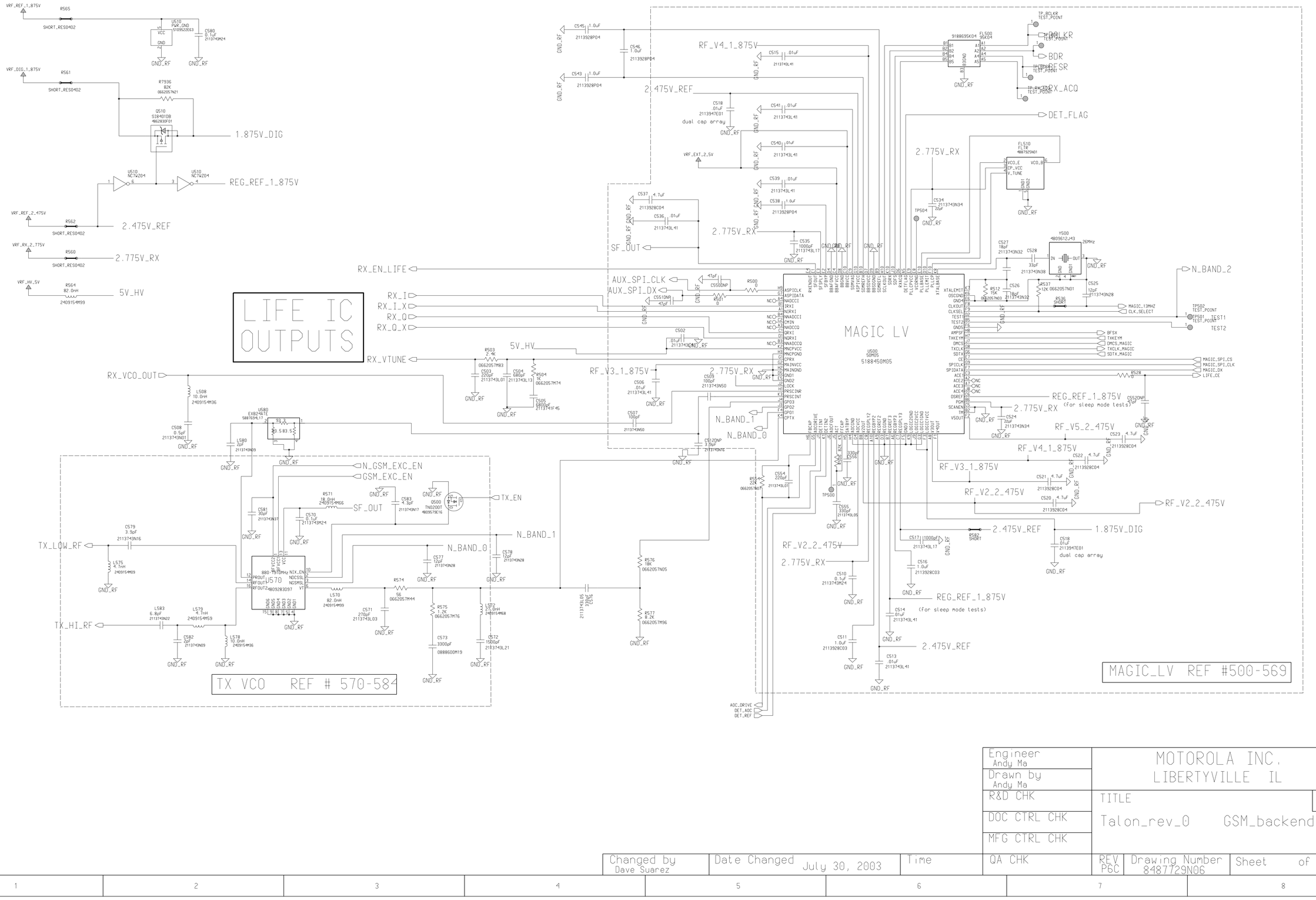

Engineer: Andy Ma	MOTOROLA INC. LIBERTYVILLE IL						
Drawn by: Andy Ma							
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MFG CTRL CHK							
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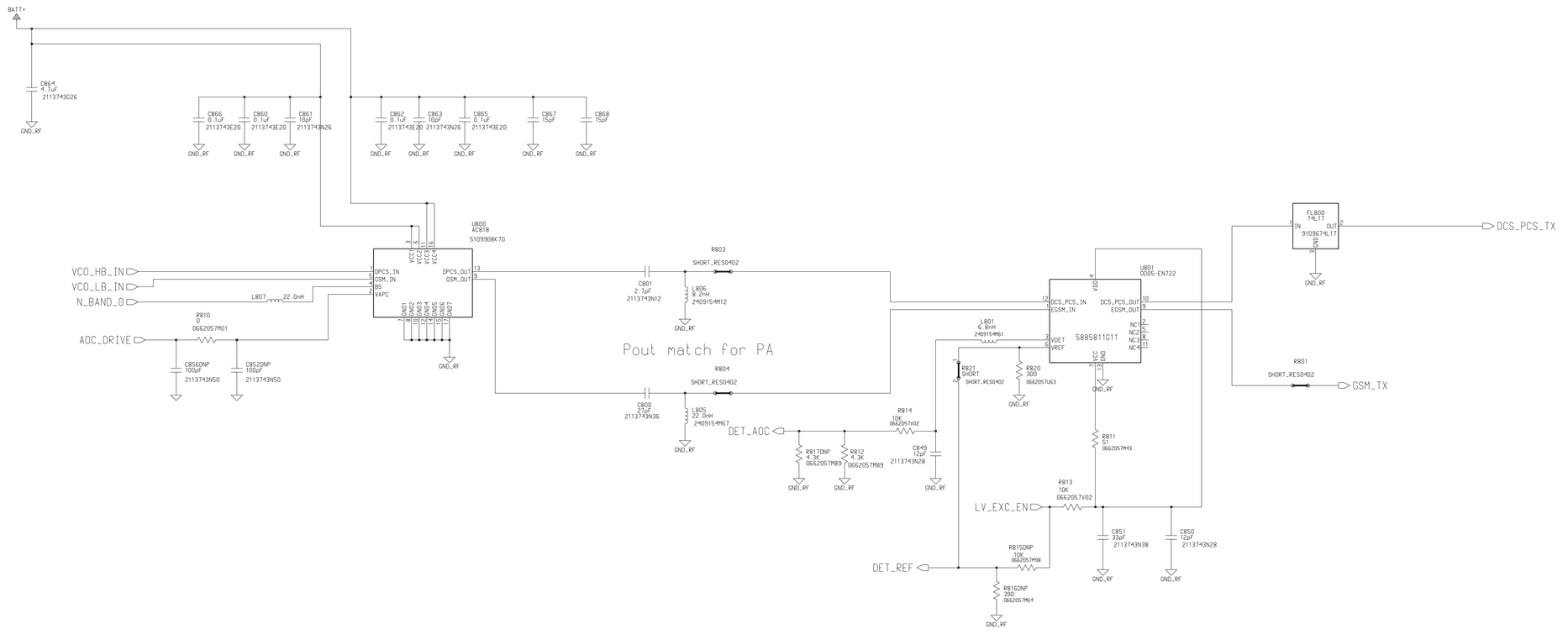
GSM Transmitter



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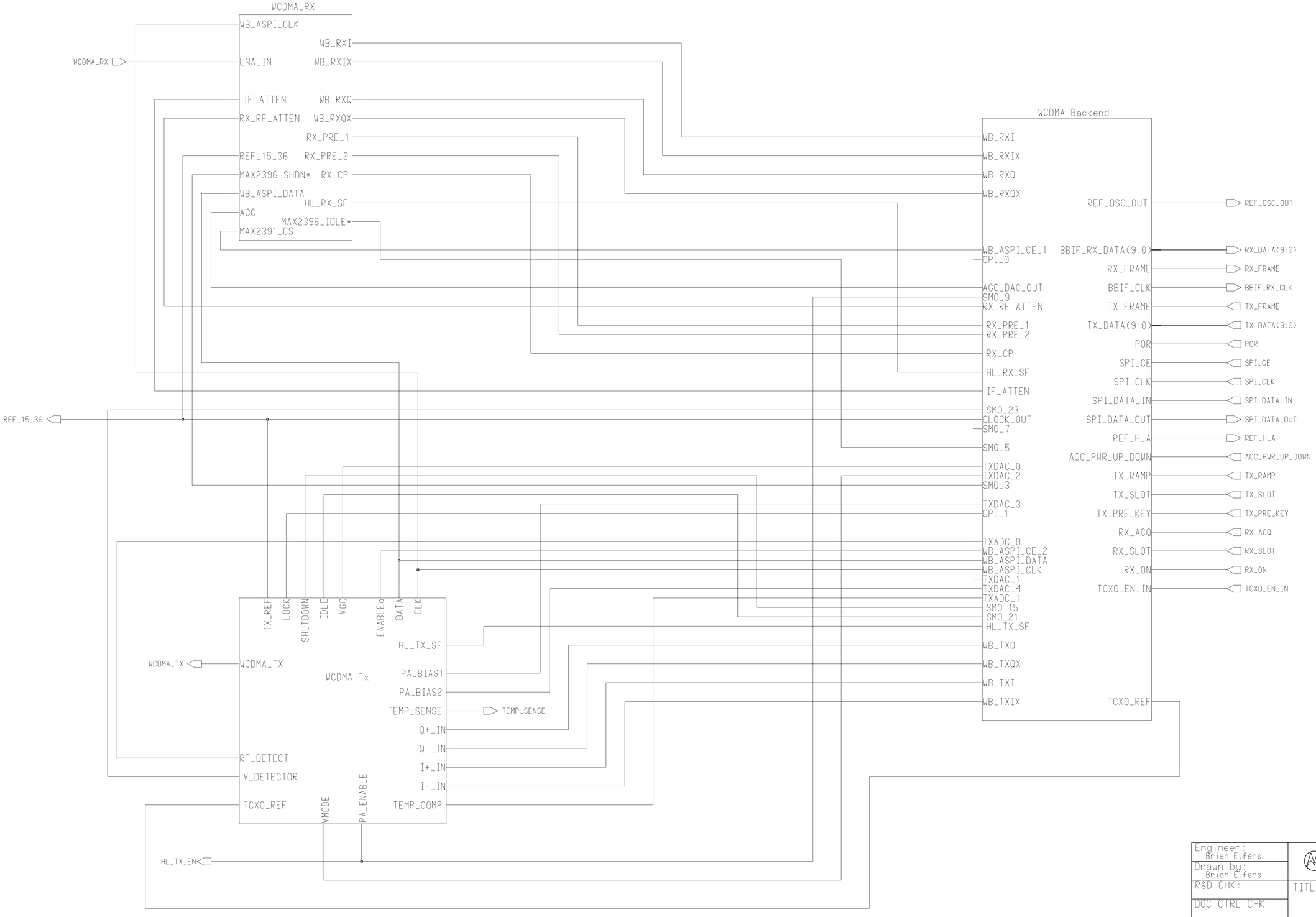

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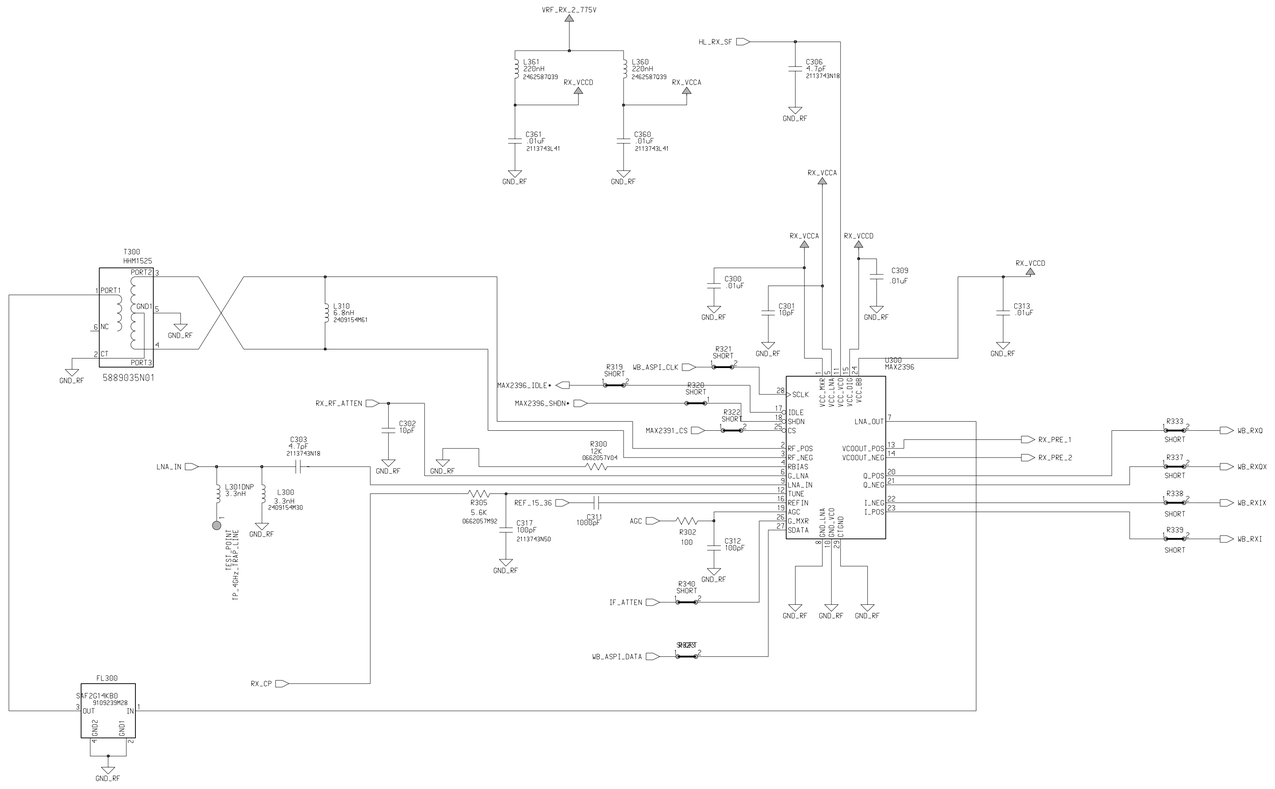
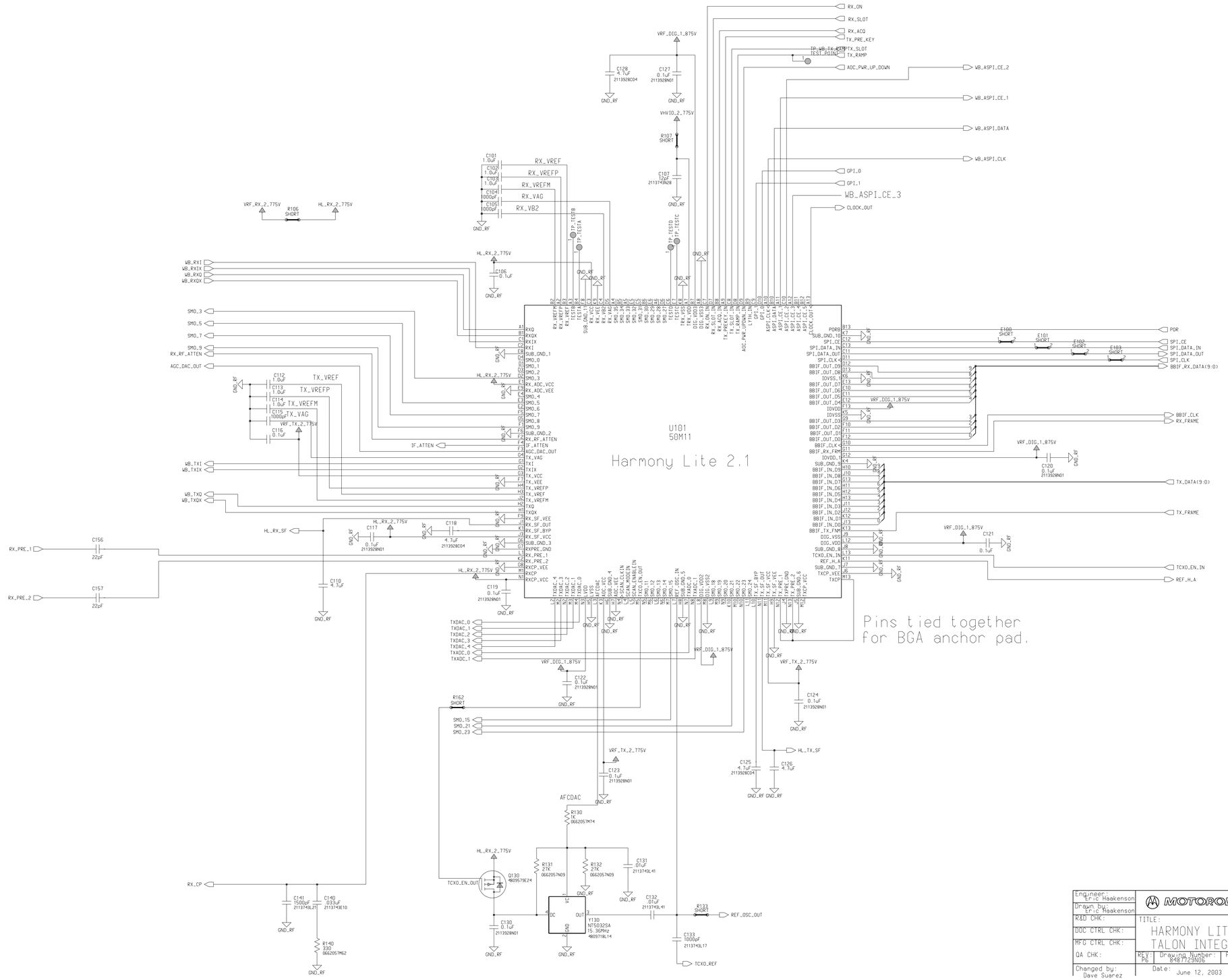
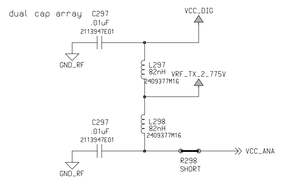
QA CHK:	REV: P3 / Drawing Number: 8487729N03 / Page: / Of:	
Changed by: Dave Suarez	Date: Friday, April 20, 2001	Time: 4:07:28 pm

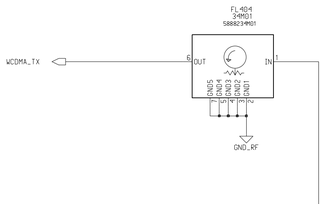


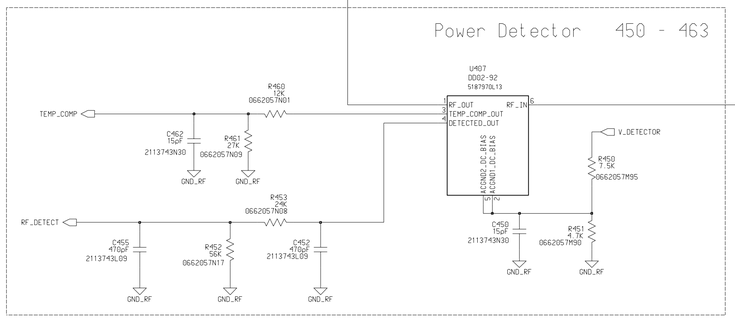
Engineer: Randy Wiessner	MOTOROLA INC.
Drawn by: Randy Wiessner	
R&D CHK:	TITLE: WCDMA_Rx — Size: D
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: P6 — Drawing Number: 8487729N06 — Page: — Of:
Changed by: Dave Suarez	Date: June 12, 2003 — Time: 4:33:16 pm


U101
50M11
Harmony Lite 2.1
Pins tied together
for BGA anchor pad.
RX_ON
RX_SLOT
RX_ACQ
TX_PRE_KEY
TX_SLOT
TX_RAMP
AGC_PWR_UP_DOWN
WB_ASPI_CE_2
WB_ASPI_CE_1
WB_ASPI_DATA
WB_ASPI_CLK
GPI_0
GPI_1
WB_ASPI_CE_3
CLOCK_OUT
POR
SPI_CE
SPI_DATA_IN
SPI_DATA_OUT
SPI_CLK
BBIF_RX_DATA(9:0)
BBIF_CLK
RX_FRAME
TX_DATA(9:0)
TX_FRAME
TCXO_EN_IN
REF_H_A
HL_TX_SF
REF_OSC_OUT
TCXO_REF
RX_CP
TCXO_EN_OUT
VRF_DIG_1_875V
VHVIO_2_775V
VRF_RX_2_775V
HL_RX_2_775V
VRF_TX_2_775V
RX_VREF
RX_VREFP
RX_VREFM
RX_VAG
RX_VB2
TX_VREF
TX_VREFP
TX_VREFM
TX_VAG
AFCDAC
TXDAC_0
TXDAC_1
TXDAC_2
TXDAC_3
TXDAC_4
TXADC_0
TXADC_1
WB_RXI
WB_RXIX
WB_RXQ
WB_RXQX
WB_TXI
WB_TXIX
WB_TXQ
WB_TXQX
SMO_3
SMO_5
SMO_7
SMO_9
SMO_15
SMO_21
SMO_23
RX_RF_ATTEN
IF_ATTEN
AGC_DAC_OUT
RX_SF_VEE
RX_SF_OUT
RX_SF_BYP
RX_SF_VCC
HL_RX_SF
RX_PRE_1
RX_PRE_2
TP_TESTB
TP_TESTA
TP_TESTD
TP_TESTC
C101 1.0uF
C102 1.0uF
C103 1.0uF
C104 1000pF
C105 1000pF
C106 0.1uF
C107 10uF 2113743N28
C110 4.7uF
C112 1.0uF
C113 1.0uF
C114 1.0uF
C115 1000pF
C116 0.1uF
C117 0.1uF 2113928N01
C118 4.7uF 2113928C04
C119 0.1uF 2113928N01
C120 0.1uF 2113928N01
C121 0.1uF
C122 0.1uF 2113928N01
C123 0.1uF 2113928N01
C124 0.1uF 2113928N01
C125 4.7uF 2113928C04
C126 4.7uF
C127 0.1uF 2113928N01
C128 4.7uF 2113928C04
C130 0.1uF 2113928N01
C131 .01uF 2113743L41
C132 .01uF 2113743L41
C133 1000pF 2113743L17
C140 .033uF 2113743E10
C141 1500pF 2113743L21
C156 22pF
C157 22pF
R106 SHORT
R107 SHORT
R130 1K 0662057K14
R131 27K 0662057N09
R132 27K 0662057N09
R133 SHORT
R140 330 0662057M62
R162 SHORT
Q130 4809579E24
Y130 NT50325A 15.36MHz 4809718L14
E100 SHORT
E101 SHORT
E102 SHORT
E103 SHORT
Engineer: Eric Haakenson
Drawn by: Eric Haakenson
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
QA CHK:
Changed by: Dave Suarez
MOTOROLA INC.
TITLE: HARMONY LITE TALON INTEGRATED
Size:
Drawing Number: 84871ZSN05
Rev: P6
Page:
Of:
Date: June 12, 2003
Time:

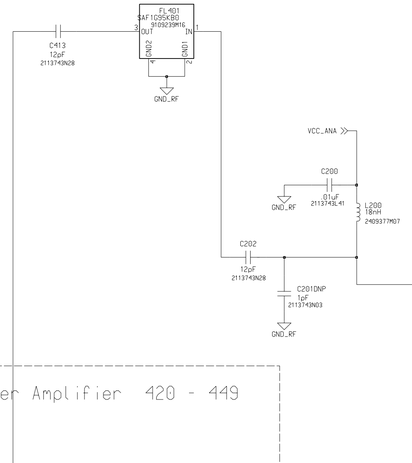


WCDMA Transmitter (TALON)

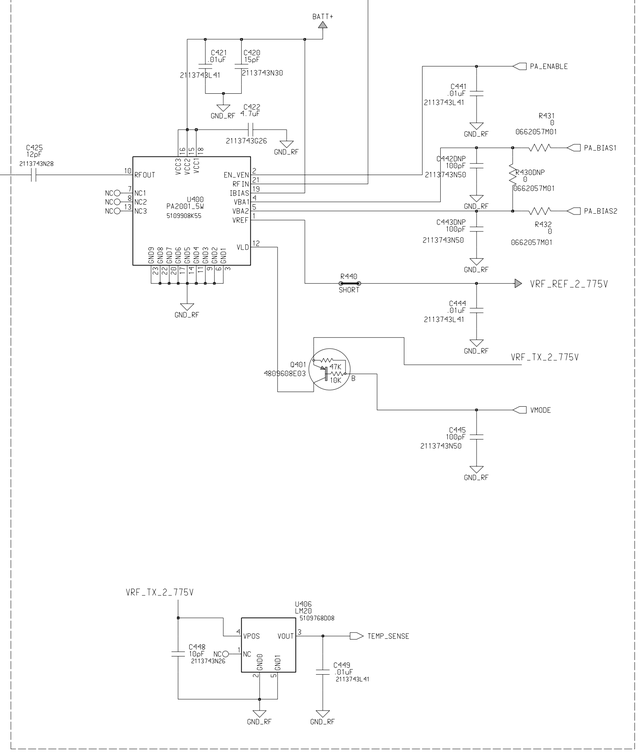




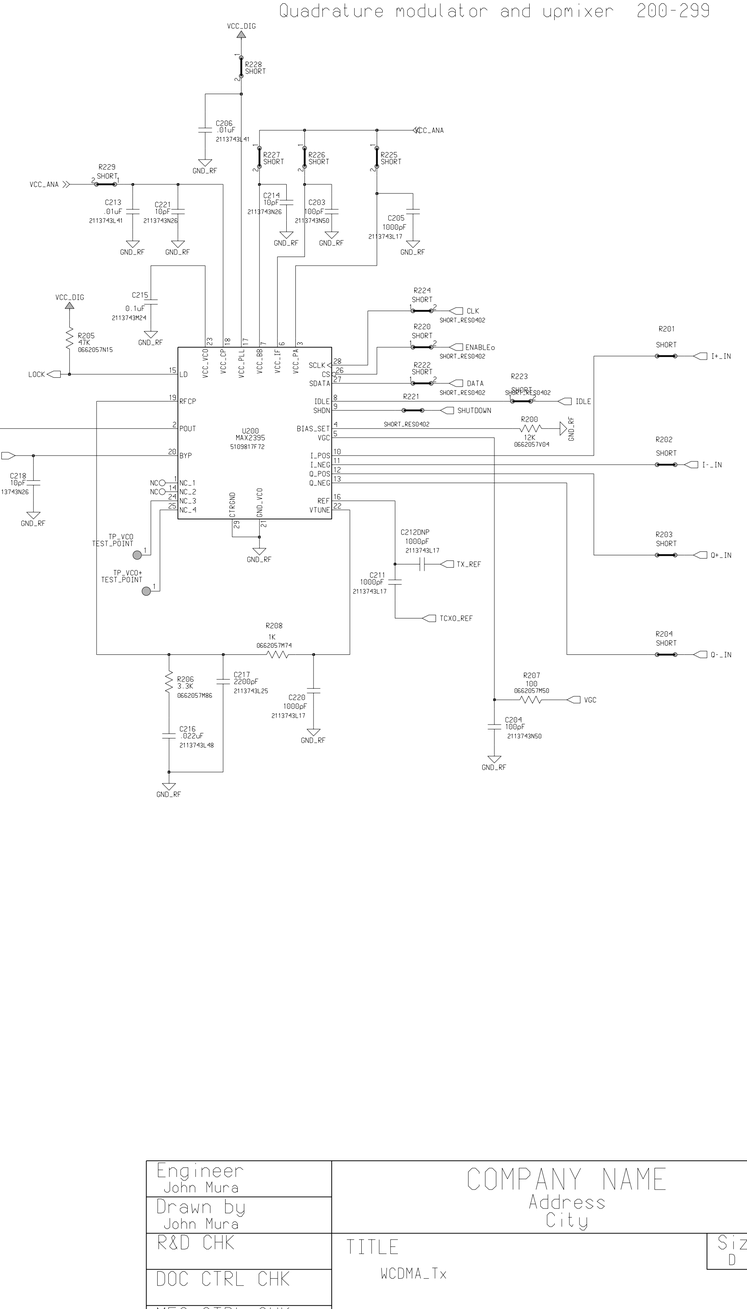
Interstage filter 1920 - 1980



Power Amplifier 420 - 449



Quadrature modulator and upmixer 200-299



Changed by Dave Suarez	Date Changed June 12, 2003	Time 4:39:58 pm	QA CHK	REV P6	Drawing Number 8487729N06	Sheet 1 of 1	

Engineer John Mura	COMPANY NAME Address City
Drawn by John Mura	
R&D CHK	TITLE WCDMA_Tx
DOC CTRL CHK	Size D
MFG CTRL CHK	

Engineer: John S. Kerr
Drawn by: Todd Roesler
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
QA CHK:
Changed by: Ed Naddeo
MOTOROLA INC.
TITLE: Talon Integrated Baseband Top Level
Size: 11x17
REV: | Drawing Number: | Page: | Of:
Date: Monday, March 4, 2002
Time: 10:39:56 am

Misc Connectors

Display Connector USIM
Keypad Connector IrDA
Headset Jack Vibrator
Fun Lights

ALRT+
ALRT-
HS_MAKE_DETECT
HS_MIC
HS_SPKR_L
HS_SPKR_R
ON_OFF_END*
ELEN1
V_VIB
EAR_SPKR-
EAR_SPKR+

FUNLITE_GRN
FUNLITE_RED
FUNLITE_BLU
IRDA_SD
IRDA_RX
IRDA_TX
USIM_CLK
USIM_RST
USIM_IO
USIM_PD*
LCD(15:8)
LCD_CLK
LCD_HSYNC
LCD_VSYNC
CLI_SPI_CLK
CLI_SPI_DATA
CLI_CS
DISPLAY_ON
FRNT_LIGHT_CTRL
KEY[0:12]

CORE LOGIC BLOCK

POG
Memories
Video
AGPS
Embedded SD

RF_RESET*
BCLKR
BFSR
BDR
BCLKX
BFSX
BDX
DMCS_MAGIC
BB_CLK_13M
NB_CLKSEL
NB_EXC_EN*
NB_RX_ACQ
NB_TX_EN*
NB_SPI_CLK
NB_SPI_MOSI
MAGIC_CS
TX_RX_ERROR
DET_FLAG
BBIF_RX_FRAME
BBIF_RX[7:2]
BBIF_TX[7:0]
BBIF_TX_FRAME
BBIF_CLK
BB_CLK_15_36M
WB_PA_ENABLE
WB_RX_SLOT
WB_TX_SLOT
WB_TX_PREKEY
WB_RX_ACQ
WB_RX_ON
AOC_PWR_UP
HL_TX_EN

PCAP_CLK_IN
VID_RTS*
LOGIC_SENSE
VID_CTS*
SWB+_EN
HKSW
MUTE*
DSEL2
DSEL1
DSEL0
OPT1
OPT2
DATALOG*
BLUETOOTH_WAKE*
BLUETOOTH_INT*
BLUE_TX
BLUE_CTS*
BLUE_RTS*
BLUE_RX
WB_SPI_CLK
WB_SPI_MOSI
WB_SPI_MISO
HARMONY_CS
CLK_32_768K_BUFF
ASAP_FS
ASAP_CLK
ASAP_RX
ASAP_TX
STEREO_FS
STEREO_CLK
STEREO_TX
VSIMC_EN
MUXCTL
BATT_IO
RXD.VMIN
TXD.VPOUT
RTS*.XRXD
USB_TXEN*
USB_VMOUT
USB_VPIN
USB_DETECT
BB_SPI_CLK
BB_SPI_MISO
BB_SPI_MOSI
PCAP_CS
PCAP_INT
PCAP_RESET*
USER_OFF
POWER_FAIL
PCAP_MCU_RESET*
WATCHDOG
CLK_32_768K
NB_STANDBY
VID_GPSb_SEL
MIDRATE_1
MIDRATE_2
NB_TX_KEYM
BATT_FDBK_SW
BATT_DETB
REF_15_36

CE Bus Connector

VID_RTS*
LOGIC_SENSE
VID_CTS*
SWB+_EN
HKSW
MUTE*
DSEL2
DSEL1
DSEL0
OPT1
OPT2
DATALOG*
BATT_FDBK
D+
D-
AUDIO_IN
AUDIO_OUT

Bluetooth

BLUETOOTH_WAKE*
BLUETOOTH_INT*
BLUE_TX
BLUE_CTS*
BLUE_RTS*
BLUE_RX
BLUE_CLK_EN*
BLUETOOTHCLK
ASAP_FS
CLK_32_768K_BUFF
ASAP_CLK
ASAP_RX
ASAP_TX

PCAP (Power/Audio)

ASAP_FS
ASAP_CLK
ASAP_RX
ASAP_TX
STEREO_FS
STEREO_CLK
STEREO_TX
VSIMC_EN
MUXCTL
BATT_IO
RXD.VMIN
TXD.VPOUT
RTS*.XRXD
USB_TXEN*
USB_VMOUT
USB_VPIN
USB_DETECT
BB_SPI_CLK
BB_SPI_MISO
BB_SPI_MOSI
PCAP_CS
PCAP_INT
PCAP_RESET*
USER_OFF
POWER_FAIL
PCAP_MCU_RESET*
WATCHDOG
CLK_32_768K
NB_STANDBY
VID_GPSb_SEL
MIDRATE_1
MIDRATE_2
NB_TX_KEYM
BATT_FDBK_SW
BATT_DETB
AUDIO_OUT
AUDIO_IN
D-
D+
BATT_FDBK
CLK_32_768K_BUFF
PCAP_CLK_IN
ALRT+
ALRT-
HS_MAKE_DETECT
HS_MIC
HS_SPKR_L
HS_SPKR_R
TEMP_SENSE
ON_OFF_END*
ELEN1
V_VIB
EAR_SPKR
EAR_SPKR+

EAR_SPKR+
EAR_SPKR-
V_VIB
ELEN1
ON_OFF_END*
HS_SPKR_R
HS_SPKR_L
HS_MIC
HS_MAKE_DETECT
ALRT-
ALRT+

PCAP SYMBOL

Stereo Headset Speakers(4300-4399)

Melody Ringer/Loudspeaker(4200-4299)

Earpiece/Handset Speaker(4000-4099)

Headset Mic and Detection (4300-4399)

Internal Microphone (4100-4199)

Overvoltage Protection

Battery Charge Circuit

Digital Audio Ports

Enumeration Fix

U3000

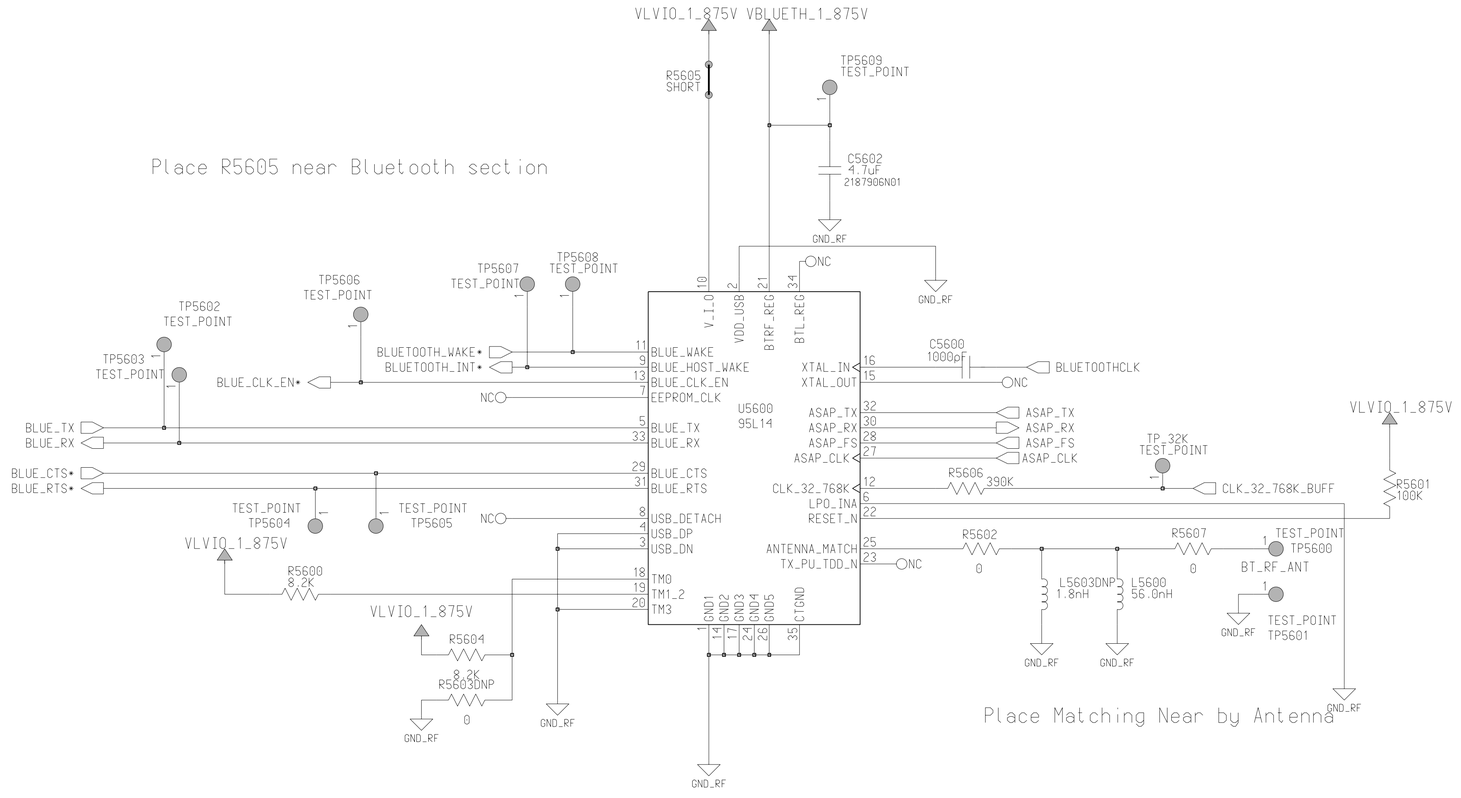
Plot Scale = 0.8

Engineer: Bok Koh & Chuck Farago	MOTOROLA INC.
Drawn by: John Kerr, Bok K. & Chuck F.	
R&D CHK:	TITLE: Talon Integrated Power and Audio
DOC CTRL CHK:	Size:
MFG CTRL CHK:	REV: / Drawing Number: / Page: / Of:
QA CHK:	
Changed by: Amanda H. & David D.	Date: 5/3/02 / Time: 1:36:56 pm

MOTOROLA CONFIDENTIAL PROPRIETARY

Date : July 23, 2001

Place R5605 near Bluetooth section



Place Matching Near by Antenna

Engineer: Dave Stubbs	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: TALON Integrated Bluetooth; Size:
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: Drawing Number: Page: Of:
Changed by: Dave Suarez	Date: February 24, 2003 Time:

MOTOROLA CONFIDENTIAL PROPRIETARY

Vibrator

M5700 MOTOR
V_VIB
C5700 33pF
GND_RF

HEADSET JACK

PLUG TIP
PLUG RING
PLUG SLEEVE
PLUG SLEEVE
PLUG OUTER RING

J4300
R4012 1MEG
VR4300 15KV
C4300 10pF
C4303DNP 33pF
R4010 470K
R4011 470K
Q4300
Q4301
FL4300 FLTR
R5202 SHORT
HS_DETECT
HS_R
HS_L
HS_MIC
HS_SPKR_R
HS_SPKR_L
HS_MAKE_DETECT

Earpiece Speaker

TEST_POINT J4001
TEST_POINT J4000
L4006 27.0nH
L4007 27.0nH
FL4000 FLTR
R4008 22
R4009 22
EAR_SPKR-
EAR_SPKR+

Side Keys

S1 SWITCH VOL DOWN
S2 SWITCH VA/VR
S3 SWITCH VOL UP
KEY[9]
KEY[5]
KEY[8]
KEY[6]

Alert Speaker

J5501 ALRT-
J5500 ALRT+

Keypad Connector

J5100 28 NC
J5100 26 NC
J5100 24 NC
32 J5100
31 J5100
30 J5100
J5100 29
J5100 27
J5100 25
J5100 23
12 J5100 J5100 1
13 J5100 J5100 2
14 J5100 J5100 3
15 J5100 J5100 4
16 J5100 J5100 5
17 J5100 J5100 6
18 J5100 J5100 7
19 J5100 J5100 8
20 J5100 J5100 9
21 J5100 J5100 10
22 J5100 J5100 11

C5112 33pF
C5111 33pF
C5106 33pF
C5103 33pF
C5109 33pF
C5104 33pF
C5105 33pF
C5114 33pF
C5113 33pF
C5108 33pF
C5115 33pF
C5107 33pF
C5110 33pF

EL_LED_5V
ELEN1
ELEN1_C
FUNLITE_RED
FUNLITE_GRN
FUNLITE_BLU
220V
EL_VOUT

EL LED Control
ELEN1_C
FUNLITE_RED
FUNLITE_GRN
FUNLITE_BLU
EL_VOUT

R5100 0
R5101DNP 0
ON_OFF_END*

KEY[0] 0
KEY[1] 1
KEY[2] 2
KEY[3] 3
KEY[4] 4
KEY[5] 5
KEY[6] 6
KEY[7] 7
KEY[8] 8
KEY[9] 9
KEY[10] 10
KEY[11] 11
KEY[12] 12
KEY[0:12]

M5200
M5201
Display Bezel U-clips

Sanyo Display Connector

J5200 0987817K05

LCD(7) LCD(6) LCD(5) LCD(4) LCD(3) LCD(2) LCD(1) LCD(0)
LCD(15) LCD(14) LCD(13) LCD(12) LCD(11) LCD(10) LCD(9) LCD(8)
LCD(15:8)
LCD_OUT(7:0)

65K_LOGIC
LCD_IN(15:8)
LCD_CLK
LCD_OUT(7:0)
SCLK
DISPLAY_ON

AGND GND_RF
DGND GND_RF
ON/OFF LED
V_LED
V_CC
CS
SCLK
SDATA
V_DD
NC
RESET
MCLK
HSYNC
VSYNC
FRNT_LIGHT_CTRL
B+
33pF C5204
C5205 33pF
C5208 33pF
C5209 33pF
DISPLAY_CS
DISPLAY_SPI_CLK
DISPLAY_SPI_DATA
VHVIO_2_775V
C5201 SHORT
DISPLAY_ON
C5203 33pF
LCD_HSYNC
LCD_VSYNC

IrDA

VHVIO_2_775V
R6100 100K
C6105 0.1uF
U6100 HSDL3202 5162852A33
C6101 10uF
C6102DNP 33pF
C6103DNP 33pF
IRDA_SD
IRDA_TX
IRDA_RX
IRDA_TX
IRDA_RX

SIM Card Board Connector

VSIMC
C5503 10pF
R5502 0
R5503 100
C5502DNP 10pF
C5505 10pF
VR5100 6.8V
VSIM
R5501 5.6K
R5504 0
C5501DNP 10pF
USIM_PD*
USIM_IO
USIM_RST
USIM_CLK
J5100 33
J5100 34
J5100 35
J5100 36
J5100 37
38 J5100
39 J5100
40 J5100

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: TALON INTEGRATED Misc Connectors
DOC CTRL CHK:	Size: 11x21
MFG CTRL CHK:	
QA CHK:	REV: 1 / Drawing Number: / Page: 1 / Of: 1
Changed by: Ed Naddeo	Date: Monday, April 23, 2001 / Time: 11:27:59 am

MOTOROLA CONFIDENTIAL PROPRIETARY

Accessory Connector
CE Connector (0987636K05)

J5000

1	GND_RF
2	BATT_FDBK
3	EXT_B+
4	D+ / TXD / TDO
5	D- / RXD / TDI
6	USB_PWR / IGN / SEND_END / RTS / RESET_IN
7	SWB+
8	HKSW / FM_DATA / CTS / DE_B
9	MUTE* / FS / DCD
10	DSEL2 / SCK / RI / TCK
11	DSEL1 / FM_CLOCK / SRDA / DTR / TMS
12	DSEL0 / FM_EN / STDA / DSR / TRST_B
13	OPTION1
14	OPTION2
15	AUDIO_OUT / 12V Flash / 8V JTAG
16	AUDIO_IN
17	GND_RF
18	GND_RF
19	GND_RF
20	GND_RF

Q5001
17F58
VIN 1
VOUT 6
ENABLE 3
NC 4
GND2 5
GND1 2
C5000 0.1uF
R5000 100K
R5001 47K
SWB+_EN
B+
C5005 1.0uF
RAW_EXT_B+
C5007 0.1uF
VR5005 16V 4813830C29
USB_PWR
RAW_BATT_FDBK
D+
D-
U5001 CSPEMI-307
ESD1 ESD3 FLTR1 FLTR2 FLTR3 FLTR4 ESD2 ESD4 GND1 GND2 GND3
D-
MUTE*
D+
BATT_FDBK
D5000
RAW_HKSW
RAW_MUTE*
RAW_DSEL2
RAW_DSEL1
RAW_DSEL0
RAW_OPT1
RAW_OPT2
U5000 CSPEMI-306
FLTR1 FLTR2 FLTR3 FLTR4 FLTR5 FLTR6 GND1 GND2 GND3
OPT2
OPT1
DSEL0
DSEL1
DSEL2
VS5001 16V 4813830C29
C5002 33pF
AUDIO_OUT
VS5002 6.8V 4809788E06
C5002 33pF
AUDIO_IN
VHVIO_2_775V
C5004 0.1uF
VA_2_775V
R5052 270K 0662057N33
R5050 47K 0662057N15
LOGIC_SENSE
C5050 0.1uF 2113743M24
VHVIO_2_775V
U5011 NC7SB3157 VCC GND A B0 B1 S
VID_RTS*
R5010DNP 0
VHVIO_2_775V
U5010 NC7SB3157 VCC GND A B0 B1 S
VID_CTS*
HKSW
DATALOG*

B0 - Normally Closed
B1 - Normally Open
S - Select
A - Common

Engineer: Jennifer Seymour	MOTOROLA INC.
Drawn by:	
R&D CHK:	TITLE: TALON Integrated CE Accessory Connector
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: / Drawing Number: / Page: / Of:
Changed by: Ed Naddeo	Date: 4/3/02 / Time:

128Mb Whitecliff

PCAP_RESET• → PCAP_RESET•

FLASH_ECB•
FLASH_LBA•
FLASH_CLK
FLASH_CS•
FLASH_OE•
FLASH_WE•
DATA[31:0]
ADDR[24:0]

4Mx16 SDRAM

SDRAM_DQMH
SDRAM_DQML
DATA[31:0]
ADDR[24:0]
SDRAM_MA[11:10]
SDRAM_CS•
SDRAM_RAS•
SDRAM_CAS•
SDRAM_CLK
SDRAM_CKE
SDRAM_WE•

POG and Memories should be placed together

POG Hiearachy Block
4 Sheets
MCU and IPCM Peripheral Interface
Memory & Test Interface
DSP Interface
Power

FLASH_ECB•	FLASH_ECB•
FLASH_LBA•	FLASH_LBA•
FLASH_CLK	FLASH_CLK
FLASH_CS•	FLASH_CS•
FLASH_OE•	FLASH_OE•
FLASH_WE•	FLASH_WE•
SDRAM_DQMH	SDRAM_DQMH
SDRAM_DQML	SDRAM_DQML
DATA[31:0]	DATA[31:0]
ADDR[24:0]	ADDR[24:0]
SDRAM_MA[11:10]	SDRAM_MA[11:10]
SDRAM_CS•	SDRAM_CS•
SDRAM_RAS•	SDRAM_RAS•
SDRAM_CAS•	SDRAM_CAS•
SDRAM_CLK	SDRAM_CLK
SDRAM_CKE	SDRAM_CKE
SDRAM_WE•	SDRAM_WE•
BB_SPI_MISO	BB_SPI_MISO
BB_SPI_CLK	BB_SPI_CLK
BB_SPI_MOSI	BB_SPI_MOSI
PCAP_CS	PCAP_CS
RF_RESET•	RF_RESET•
BCLKR	BCLKR
BFSR	BFSR
BDR	BDR
BCLKX	BCLKX
BFSX	BFSX
BDX	BDX
DMCS_MAGIC	DMCS_MAGIC
BB_CLK_13M	BB_CLK_13M
NB_STANDBY	NB_STANDBY
NB_CLKSEL	NB_CLKSEL
NB_EXC_EN•	NB_EXC_EN•
NB_RX_ACQ	NB_RX_ACQ
NB_TX_EN•	NB_TX_EN•
NB_TX_KEYM	NB_TX_KEYM
NB_SPI_CLK	NB_SPI_CLK
NB_SPI_MOSI	NB_SPI_MOSI
MAGIC_CS	MAGIC_CS
TX_RX_ERROR	TX_RX_ERROR
AOC_PWR_UP	AOC_PWR_UP
DET_FLAG	DET_FLAG
BB_CLK_15_36M	BB_CLK_15_36M
WB_RX_ACQ	WB_RX_ACQ
WB_RX_ON	WB_RX_ON
WB_RX_SLOT	WB_RX_SLOT
WB_TX_PREKEY	WB_TX_PREKEY
WB_TX_SLOT	WB_TX_SLOT
WB_PA_ENABLE	WB_PA_ENABLE
BBIF_RX_FRAME	BBIF_RX_FRAME
BBIF_RX[7:2]	BBIF_RX[7:2]
BBIF_TX[7:0]	BBIF_TX[7:0]
BBIF_TX_FRAME	BBIF_TX_FRAME
BBIF_CLK	BBIF_CLK
WB_SPI_CLK	WB_SPI_CLK
WB_SPI_MOSI	WB_SPI_MOSI
WB_SPI_MISO	WB_SPI_MISO
HARMONY_CS	HARMONY_CS
USIM_IO	USIM_IO
USIM_CLK	USIM_CLK
USIM_RST	USIM_RST
VSIMC_EN	VSIMC_EN
USIM_PD•	USIM_PD•
IRDA_SD	IRDA_SD
IRDA_TX	IRDA_TX
IRDA_RX	IRDA_RX
FUNLITE_GRN	FUNLITE_GRN
FUNLITE_RED	FUNLITE_RED
FUNLITE_BLU	FUNLITE_BLU

MUXCTL	MUXCTL
DATALOG•	DATALOG• →
LOGIC_SENSE	LOGIC_SENSE
SWB+_EN	SWB+_EN
USB_DETECT	USB_DETECT
USB_TXEN•	USB_TXEN•
USB_VMOUT	USB_VMOUT
USB_VPIN	USB_VPIN
TXD.VPOUT	TXD.VPOUT
RXD.VMIN	RXD.VMIN
RTS•.XRXD	RTS•.XRXD
DSEL0	DSEL0
DSEL1	DSEL1
DSEL2	DSEL2
HKSW	HKSW
MUTE•	MUTE•
OPT1	OPT1
OPT2	OPT2
CLK_32_768K	CLK_32_768K
WATCHDOG	WATCHDOG
PCAP_INT	PCAP_INT
PCAP_MCU_RESET•	PCAP_MCU_RESET•
POWER_FAIL	POWER_FAIL
USER_OFF	USER_OFF
BLUE_TX	BLUE_TX
BLUE_RX	BLUE_RX
BLUE_RTS•	BLUE_RTS•
BLUE_CTS•	BLUE_CTS•
BLUETOOTH_WAKE•	BLUETOOTH_WAKE•
BLUETOOTH_INT•	BLUETOOTH_INT•
DISPLAY_SPI_CLK	DISPLAY_SPI_CLK
DISPLAY_CS	DISPLAY_CS
DISPLAY_SPI_DATA	DISPLAY_SPI_DATA
DISPLAY_ON	DISPLAY_ON
FRNT_LIGHT_CTRL	FRNT_LIGHT_CTRL
LCD(15:8)	LCD(15:8)
LCD_CLK	LCD_CLK
LCD_HSYNC	LCD_HSYNC
LCD_VSYNC	LCD_VSYNC
KEY[0:12]	KEY[0:12]
PCAP_CLK_IN	PCAP_CLK_IN
ASAP_CLK	ASAP_CLK
ASAP_FS	ASAP_FS
ASAP_TX	ASAP_TX
ASAP_RX	ASAP_RX
STEREO_CLK	STEREO_CLK
STEREO_FS	STEREO_FS
STEREO_TX	STEREO_TX
MIDRATE_1	MIDRATE_1
MIDRATE_2	MIDRATE_2
BATT_IO	BATT_IO
BATT_FDBK_SW	BATT_FDBK_SW
BATT_DETB	BATT_DETB
HL_TX_EN	HL_TX_EN

VID_GPSb_SEL → VID_GPSb_SEL
VID_RTS• → VID_RTS•
VID_CTS• → VID_CTS•

VIDEO

DATALOG•	
VID_RTS•	
VID_CTS•	
VID_RESET•	
VID_GPSb_SEL	
VID_GPS_TX	
VID_GPS_RX	
VID_CLK	
GPS_TX	
GPS_RX	
VID_CLK	

GPS

CLK_32_768K_BUFF	CLK_32_768K_BUFF
GPS_TX	GPS_TX
GPS_RX	GPS_RX
GPS_BOOT_SEL	GPS_BOOT_SEL
GPS_EIT	GPS_EIT
GPS_RESET•	GPS_RESET•
VID_GPS_ON_B	VID_GPS_ON_B
REF_15_36	REF_15_36

Embedded SD

MMC_CLK	MMC_CLK
MMC_CMD	MMC_CMD
MMC_DAT	MMC_DAT

Engineer:	Ed Naddeo
Drawn by:	Ed Naddeo
R&D CHK:	
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	
Changed by:	wlen01

MOTOROLA INC.

TITLE: Talon Integrated Core Logic

Size: 11x21

REV: 1.0 | Drawing Number: 8488888x88 | Page: 1 | Of: 1

Date: Friday, March 1, 2002

Time: 1:16:44 pm

MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A

POG_HVIO
POG_LVIO
C1003 0.1uF
C1007 0.1uF
C1011 0.1uF
C1004 0.1uF
C1019
C1036 0.1uF
C1038 0.1uF
GND_RF

MUXCTL
R1032 0
BATT_IO
VMAIN_1_55V
U1020 NC7SB3157
VCC
GND
B0
B1
S
NC
GND_RF

BLUE_CTS*
BLUE_RTS*
BLUE_RX
BLUE_TX
POG_LVIO
USB_TXEN*
USB_VMOUT
USB_VPIN
USB_VPOUT
POG_HVIO
GPT1
GPT2
DSEL2
MUTE*
DSEL0
DSEL1
HKSW
RTS*_XRXD
RXD_VMIN
TXD_VPOUT
BATT_IO
POG_HVIO
GPS_EIT
GPS_RESET*
VID_RESET*
GPS_BOOT_SEL
VID_CTS*
VID_RTS*
VID_GPS_RX
VID_GPS_TX

T12 CTS3_B
W14 RTS3_B
V13 RXD3
U12 TXD3
Y13 NVCC_12_UART3
U13 USB_TXEN_B
V14 USB_VMOUT
W15 USB_VPIN
Y14 NVCC_36_USB
W11 NVCC_37_UART1_BATIO
Y12 GPIO24
R11 GPIO25
W12 R1_B
T11 DCD1_B
V12 DSR1_B
U11 DTR1_B
V11 CTS1_B
R10 RTS1_B
T10 RXD1
U10 TXD1
P10 MUXCTL
V10 BATT_LINE
A10 NVCC_38_UART2
F9 R2_B
D11 DCD2_B
E11 DSR2_B
E10 DTR2_B
C11 CTS2_B
B11 RTS2_B
E9 RXD2
D10 TXD2

U1000
MCU_IPCM_IO

IRDA_TX
IRDA_RX
POG_HVIO
DISPLAY_SPI_DATA
FRNT_LIGHT_CTRL
DISPLAY_SPI_CLK
BB_SPI_MOSI
BB_SPI_MISO
BB_SPI_CLK
DISPLAY_CS
FUNLITE_RED
PCAP_CS
POG_HVIO
MMC_DAT
FUNLITE_GRN
MMC_CMD
MMC_CLK
VMAIN_1_55V
USER_OFF
WATCHDOG
VID_CLK
TP1000 TEST_POINT
PCAP_MCU_RESET*
POWER_FAIL
PCAP_CLK_IN
POG_CKIL
NVCC_43
POG_LVIO
STEREO_TX
BLUETOOTH_WAKE*
STEREO_CLK
STEREO_FS
MIDRATE_2
BLUETOOTH_INT*

R1043 10K
R1040DNP 0
R1050 0
R1018 0

B14 IRDA_TX1
D13 IRDA_RX1
A15 NVCC_40_GQSPI_IRDA
E12 GQSPI2_DO
B13 GQSPI2_DI
C13 GQSPI2_CK
F13 GQSPI1_DO
F12 GQSPI1_DI
A14 GQSPI1_CK
D12 GQSPI_CS_0
G11 GQSPI_CS_1
F11 GQSPI_CS_2
L1 NVCC_44_MMC
L5 MMC_DAT
L3 MMC_CMD_OD_EN
L2 MMC_CMD
L4 MMC_CLK
G15 NVCC_10_CLKS_RSTS
B20 USER_OFF
G14 WDOG_RST
C18 STO
E16 RESET_IN
D17 POWER_FAIL
C20 CKO2
E18 CKO1
C19 CKIL
W1 NVCC_43_VSAP
W2 V_STD
V3 V_SRD
Y2 V_SCK
U4 V_SC2
T4 V_SC1
W3 V_SC0

POG

MCU & IPCM Peripherals

G1 NVCC_32_LCD
D1 NVCC_31_LCD
H6 LCD_LOAD_HSYNC
G3 LCD_FRAME_VSYNC
G4 LCD_CLK
H5 LCD_AC_LOE
F2 LCD11
F3 LCD10
G5 LCD9
F4 LCD8
E1 LCD7
E2 LCD6
F5 LCD5
E3 LCD4
J5 LCD3
J6 LCD2
H4 LCD1
G2 LCD0
A2 NVCC_30_KEY
C3 KEY_ROW7
F6 KEY_ROW6
D3 KEY_ROW5
C1 KEY_ROW4
B1 KEY_ROW3
C2 KEY_ROW2
D2 KEY_ROW1
E4 KEY_ROW0
B3 KEY_COL3
D4 KEY_COL2
B2 KEY_COL1
E5 KEY_COL0

POG_HVIO
LCD_HSYNC
LCD_VSYNC
LCD_CLK
NC
NVCC_30
POG_LVIO
LCD[15:8]
KEY[0:12]

C12 SVEN0_0
E13 SIMPD0_0
H3 RSTO_0
J3 DATA0_TX_0
J4 DATA0_RX_0
H2 CLK0_0
H1 NVCC_33_SIM0
A12 NVCC_49_SVEN
B12 SVEN0_1
C14 SIMPD0_1
K3 RSTO_1
K5 DATA0_TX_1
K2 DATA0_RX_1
K4 CLK0_1
J1 NVCC_26_SIM1
Y6 GPIO11
U6 GPIO10
V7 GPIO9
U7 GPIO8
T7 GPIO7
R7 GPIO6
Y7 GPIO5
W8 GPIO4
V8 GPIO3
U8 GPIO2
T8 GPIO1
R8 GPIO0
W7 NVCC_41_MCUGPIO

VSIMC_EN
USIM_RST
USIM_IO
USIM_CLK
VSIM
NC
BATT_DETB
BATT_FDBK_SW
DATALOG*
POG_HVIO
SWB+_EN
MIDRATE_1
DISPLAY_ON
IRDA_SD
LOGIC_SENSE
PCAP_INT
TX_RX_ERROR
FUNLITE_BLU
HL_TX_EN
POG_HVIO

VHVIO_2_775V
R1012DNP 100K
R1019DNP 0
U1019 TC7S32F
USB_DETECT
MUXCTL
VHVIO_2_775V
U1019 PWR_GND
GND_RF

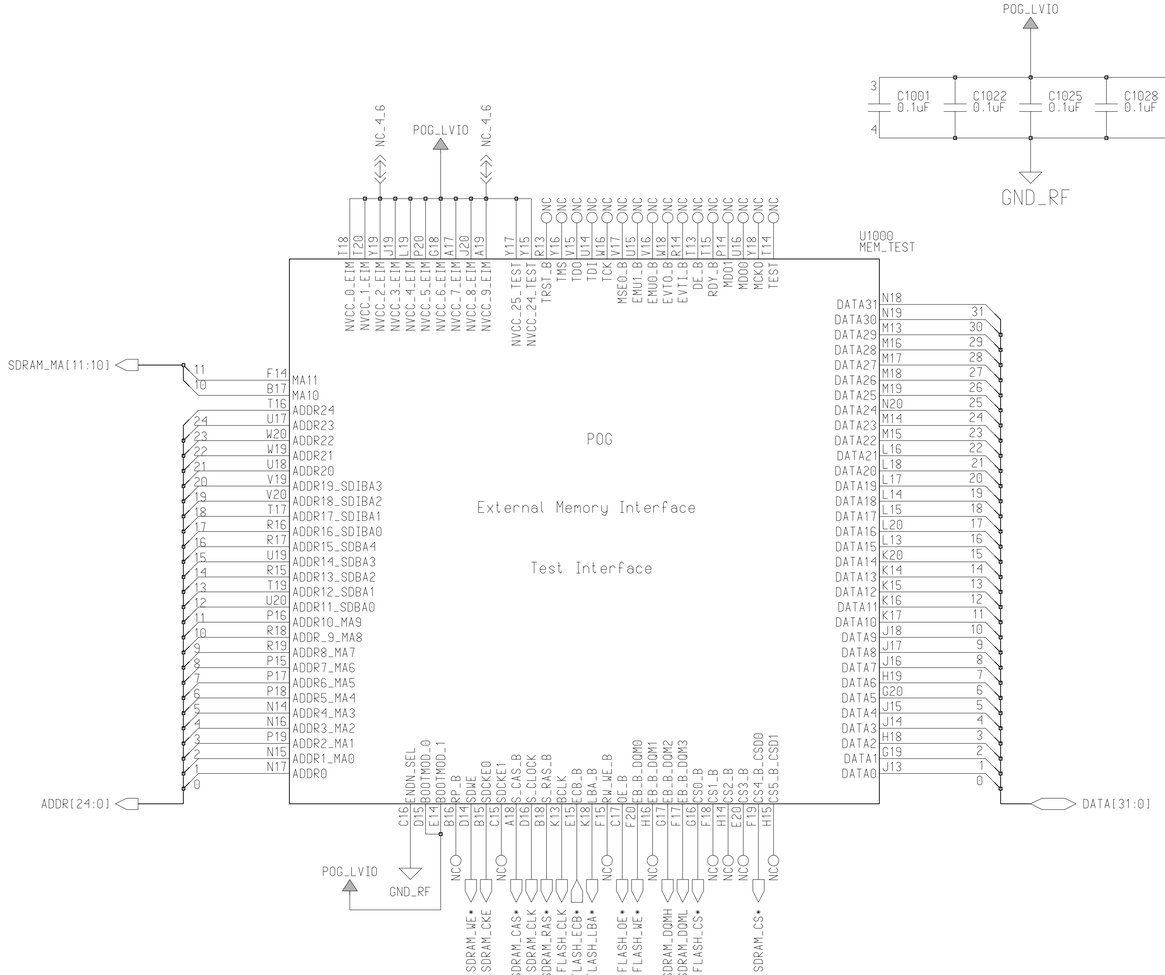
CLK_32_768K
VMAIN_1_55V
U1018DNP NC7SP125
OE
VCC
A
Y
GND
NC
C1029DNP 0.1uF

VSIM
U1046 PWR_GND
C1046 0.1uF
U1046 NC7WZ17
R1046DNP 0
USIM_PD*
C1047 0.1uF
R1047 0
C1045 0.1uF

100K R1041
VID_GPS_ON_B
VID_GPSb_SEL
R1042 100K

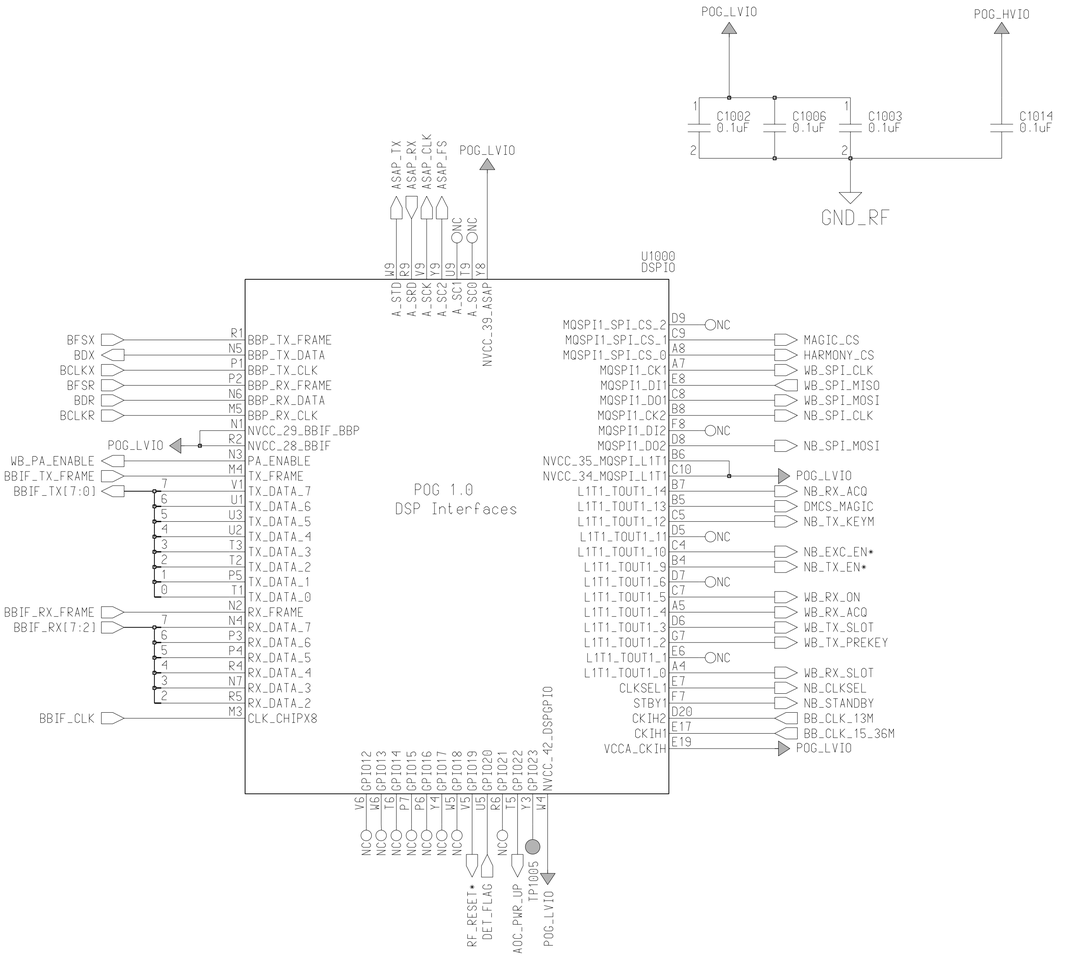
MOTOROLA CONFIDENTIAL PROPRIETARY

4 1 3 A



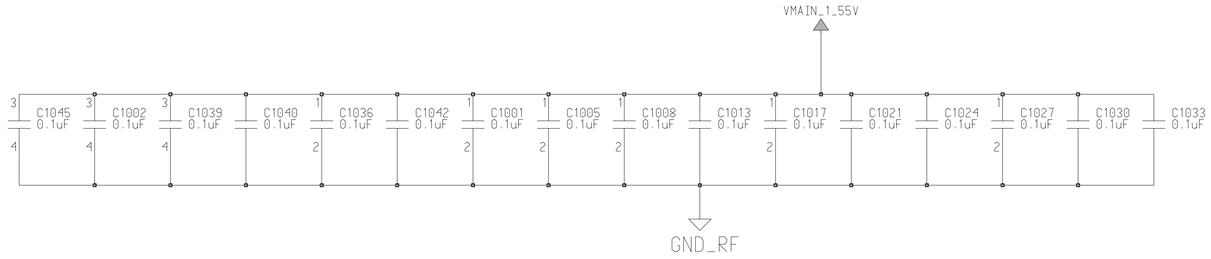
Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated POG Memory and Test Interface
DOC CTRL CHK:	Size: 11x17
MFG CTRL CHK:	
QA CHK:	REV: 1.0 · Drawing Number: 8488888x88 · Page: 3 · Of: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002 · Time: 6:15:09 pm

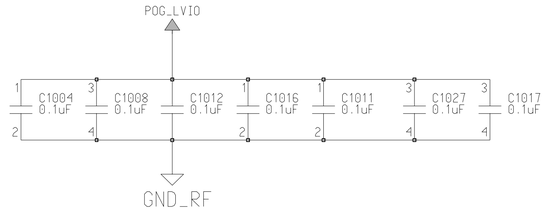
4 1 3 A

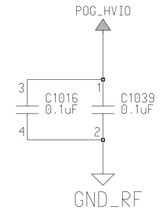


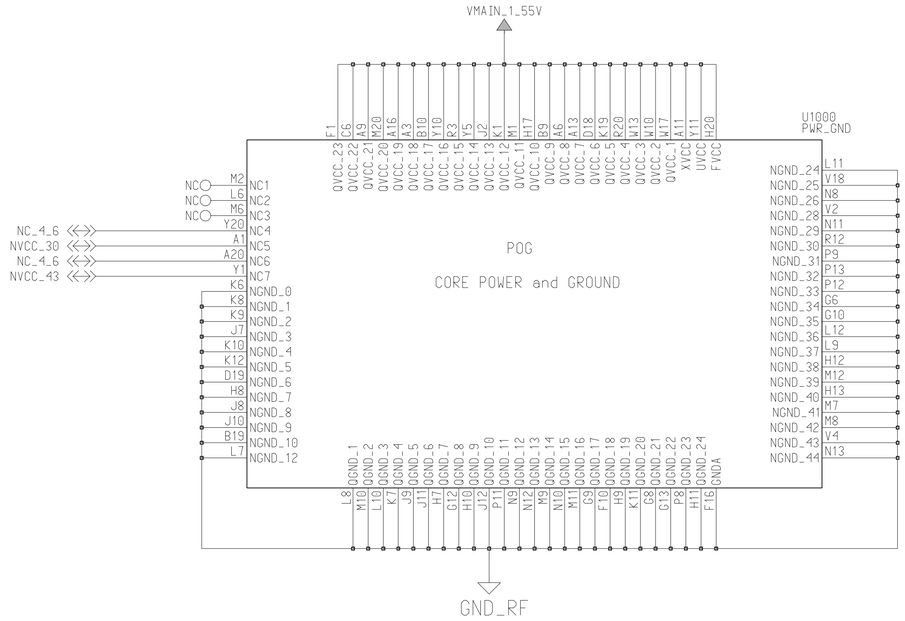
Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated POG DSP Interface — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 1.0 — Drawing Number: 8488888x88 — Page: 4 — Of: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002 — Time: 6:16:44 pm

4 1 3 A









Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated POG Power — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 1 — Drawing Number: 84888888x88 — Page: 1 — OF: 4
Changed by: wlen01	Date: Tuesday, February 26, 2002 — Time: 2:56:17 pm

MOTOROLA INTERNAL USE ONLY

4 1 3 A

VMEM_1_875V
V_FLASH1
R1300
SHORT
V_FLASH2
R1302
SHORT
VLVIO_1_875V
V_FLASH1_IO
R1303
SHORT
V_FLASH2_IO
R1301
SHORT

V_FLASH2
C1301 0.1uF
C1306 0.1uF
GND_RF

V_FLASH1
C1304 0.1uF
C1308 0.1uF
GND_RF

VLVIO_1_875V
TP1301 TEST_POINT 1
R1305 3.3K
TP1300 TEST_POINT 1
FLASH_12V
C1307 0.1uF
C1309 0.1uF
GND_RF

V_FLASH2_IO
C1302 0.1uF
C1310 0.1uF
GND_RF

V_FLASH1_IO
C1300 0.1uF
C1305 0.1uF
GND_RF

DATA[31:0]
ADDR[24:0]

U1300 28F640W18
U1310 28F640W18

V_FLASH1
V_FLASH1_IO
V_FLASH2
V_FLASH2_IO

GND_RF

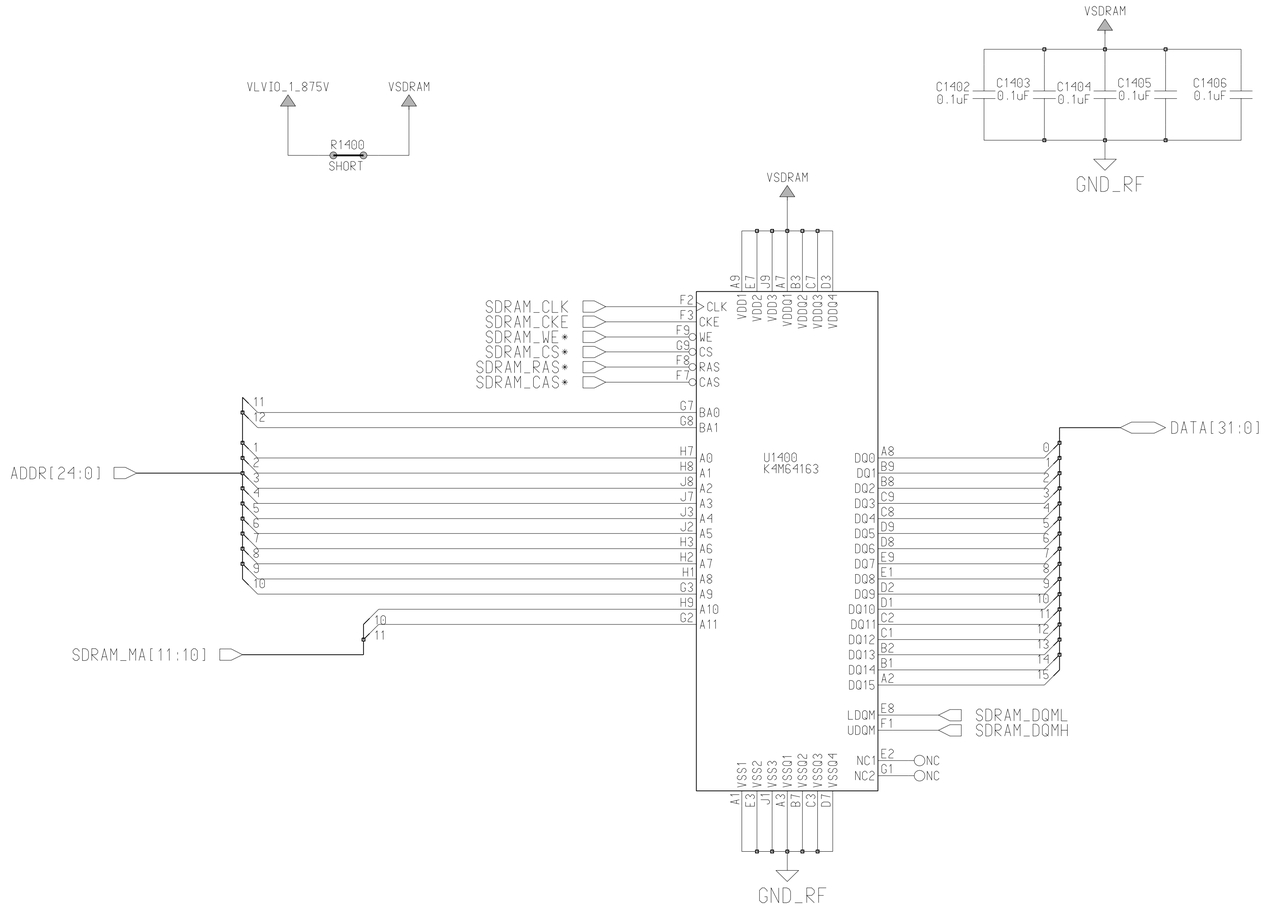
FLASH_CLK
FLASH_CS*
FLASH_OE*
FLASH_WE*
FLASH_LBA*
PCAP_RESET*
FLASH_ECB*

FLASH_CS*
FLASH_OE*
FLASH_LBA*
FLASH_CLK
FLASH_WE*
PCAP_RESET*
FLASH_ECB*

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated Flash Memory
DOC CTRL CHK:	Size: 11x21
MFG CTRL CHK:	
QA CHK:	REV: 0.1 / Drawing Number: / Page: 1 / Of: 1
Changed by: Chris Pipe	Date: Monday, May 6, 2002 / Time: 9:32:29 am

4 1 3 A

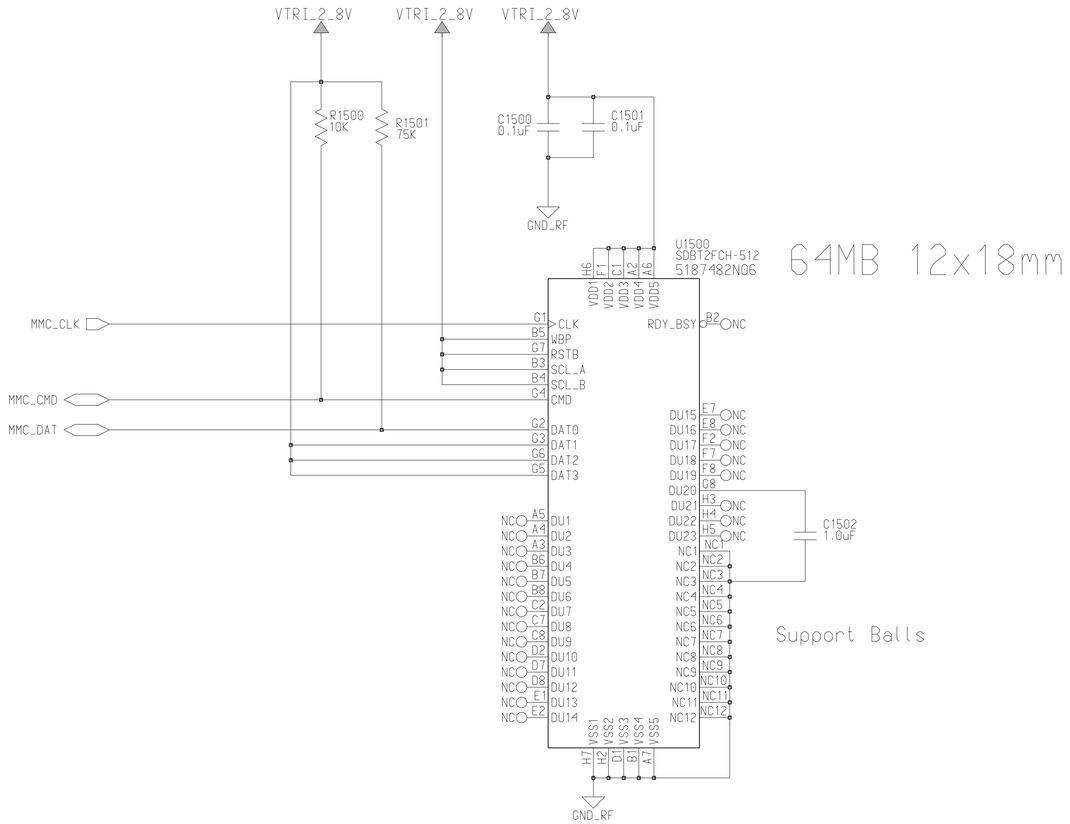
Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated 4Mx16 SDRAM — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 1.0 — Drawing Number: 84888888x88 — Page: 1 — Of: 1
Changed by: wlen01	Date: Friday, March 1, 2002 — Time: 3:37:06 pm



MOTOROLA CONFIDENTIAL PROPRIETARY

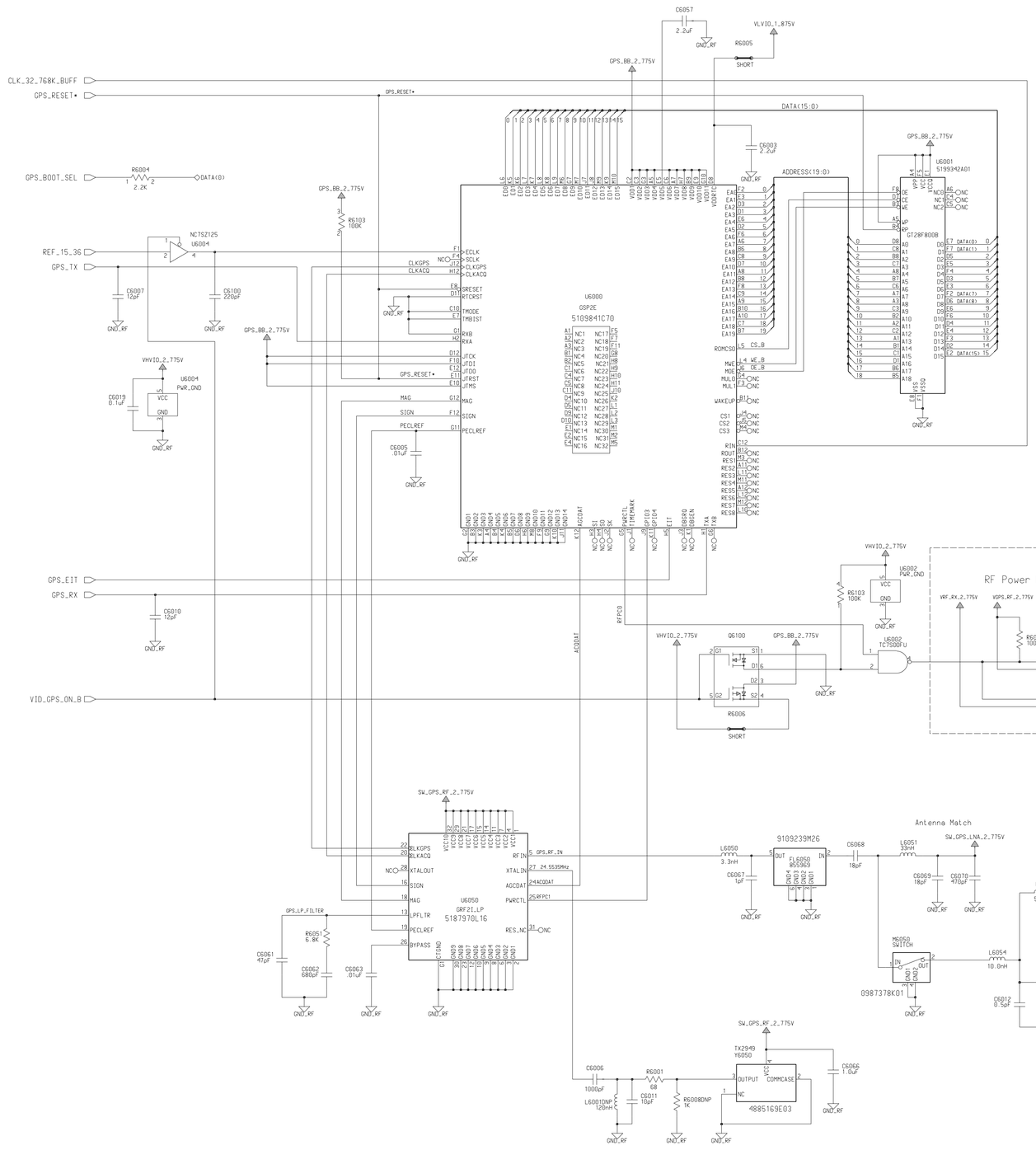
4 1 3 A

Engineer: Ed Naddeo	MOTOROLA INC.
Drawn by: Ed Naddeo	
R&D CHK:	TITLE: Talon Integrated Embedded SD Flash — Size: 11x17
DOC CTRL CHK:	
MFG CTRL CHK:	
QA CHK:	REV: 1.0 — Drawing Number: 848888888x88 — Page: 1 — Of: 1
Changed by: Chris Pipe	Date: Friday, May 3, 2002 — Time: 1:25:03 pm



MOTOROLA CONFIDENTIAL PROPRIETARY

Engineer: J. Abe Keane	MOTOROLA INC.
Drawn by: J. Abe Keane	
R&D CHK:	TITLE: TALON Integrated GPS Block SiRFStarIIe/LP Schematic
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: 1 | Drawing Number: | Page: 1 | OF: 1
Changed by: J. Abe Keane	Date: Monday, September 11, 2001 | Time: 10:21:35 am



MOTOROLA CONFIDENTIAL PROPRIETARY

Oscillator and Memory Device Removed

FALCON
MC30200
U7500
5189251L03

L7500 is place holder for inductor

Place VR parts as close as to J7900 and before any vias

Sensor Connector
Molex 54722-0308

as close as to Falcon

as close as to J7900 pin 1

as close as to J7900 pin 40

Engineer: Jennifer Seymour	MOTOROLA INC.
Drawn by: Jennifer Seymour	
R&D CHK:	TITLE: TALON Integrated Falcon Camera
DOC CTRL CHK:	Size:
MFG CTRL CHK:	
QA CHK:	REV: | Drawing Number: | Page: 1 | OF: 1
Changed by: Jennifer Seymour	Date: Friday, November 9, 2001 | Time: 10:21:35 am

Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the A835 UMTS/GSM handset.

Table 11. Electrical Parts List

Reference Number	Part Number	Description
C003	2113743N22	CAP, 6.8pF
C050	2409377M11	IDCTR, 39nH
C052	2409377M02	IDCTR, 3.9nH
C054DNP	2113743N50	CAP, 100pF
C061	2113743N26	CAP, 10pF
C062	2113743N37	CAP, 30pF
C063	2113743N26	CAP, 10pF
C064	2113743N26	CAP, 10pF
C065	2113743N26	CAP, 10pF
C066	2113743N26	CAP, 10pF
C101	2113928P04	CAP, 1.0uF
C102	2113928P04	CAP, 1.0uF
C103	2113928P04	CAP, 1.0uF
C104	2113743L17	CAP, 1000pF
C105	2113743L17	CAP, 1000pF
C106	2113928N01	CAP, 0.1uF
C107	2113743N28	CAP, 12pF
C1029DNP	2113743M24	CAP, 0.1uF
C110	2113928C04	CAP, 4.7uF
C112	2113928P04	CAP, 1.0uF
C113	2113928P04	CAP, 1.0uF
C114	2113928P04	CAP, 1.0uF
C115	2113743L17	CAP, 1000pF
C116	2113928N01	CAP, 0.1uF
C117	2113928N01	CAP, 0.1uF
C118	2113928C04	CAP, 4.7uF
C119	2113928N01	CAP, 0.1uF
C120	2113928N01	CAP, 0.1uF
C121	2113928N01	CAP, 0.1uF
C122	2113928N01	CAP, 0.1uF
C123	2113928N01	CAP, 0.1uF
C124	2113928N01	CAP, 0.1uF
C125	2113928C04	CAP, 4.7uF
C126	2113928C04	CAP, 4.7uF
C127	2113928N01	CAP, 0.1uF
C128	2113928C04	CAP, 4.7uF
C130	2113928N01	CAP, 0.1uF
C131	2113743L41	CAP, .01uF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C132	2113743L41	CAP, .01uF
C133	2113743L17	CAP, 1000pF
C140	2113743E10	CAP, .033uF
C141	2113743L21	CAP, 1500pF
C156	2113743N34	CAP, 22pF
C157	2113743N34	CAP, 22pF
C200	2113743L41	CAP, .01uF
C201	2113743N09	CAP, 2pF
C202	2113743N28	CAP, 12pF
C203	2113743N50	CAP, 100pF
C204	2113743N50	CAP, 100pF
C205	2113743L17	CAP, 1000pF
C206	2113743L41	CAP, .01uF
C211	2113743L17	CAP, 1000pF
C213	2113743L41	CAP, .01uF
C214	2113743N26	CAP, 10pF
C215	2113743M24	CAP, 0.1uF
C216	2113743L48	CAP, .022uF
C217	2113743L25	CAP, 2200pF
C218	2113743N26	CAP, 10pF
C212DNP	2113743L17	CAP, 1000pF
C220	2113743L17	CAP, 1000pF
C221	2113743N26	CAP, 10pF
C297	2113947E01	CAP, .01uF
C300	2113743L41	CAP, .01uF
C301	2113743N26	CAP, 10pF
C302	2113743N26	CAP, 10pF
C303	2113743N26	CAP, 10pF
C306	2113743N18	CAP, 4.7pF
C309	2113743L41	CAP, .01uF
C311	2113743L17	CAP, 1000pF
C312	2113743N50	CAP, 100pF
C313	2113743L41	CAP, .01uF
C317	2113743N50	CAP, 100pF
C360	2113743L41	CAP, .01uF
C361	2113743L41	CAP, .01uF
C3960DNP	2113743L35	CAP, 5600pF
C413	2113743N28	CAP, 12pF
C4105DNP	2113743N38	CAP, 33pF
C420	2113743N30	CAP, 15pF
C421	2113743L41	CAP, .01uF
C422	2113743G26	CAP, 4.7uF
C425	2113743N28	CAP, 12pF
C4202DNP	2113743L13	CAP, 680pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C4303DNP	2113743N38	CAP, 33pF
C4307DNP	2113743N38	CAP, 33pF
C4352DNP	2113743N38	CAP, 33pF
C4389DNP	2113928P04	CAP, 1.0uF
C441	2113743L41	CAP, .01uF
C444	2113743L41	CAP, .01uF
C445	2113743N50	CAP, 100pF
C448	2113743N26	CAP, 10pF
C449	2113743L41	CAP, .01uF
C4402DNP	2113743N26	CAP, 10pF
C442DNP	2113743N50	CAP, 100pF
C443DNP	2113743N50	CAP, 100pF
C450	2113743N30	CAP, 15pF
C452	2113743N30	CAP, 15pF
C455	2113743L09	CAP, 470pF
C462	2113743N30	CAP, 15pF
C502	2113743N14	CAP, 3.3pF
C503	2113743L01	CAP, 220pF
C504	2113743L13	CAP, 680pF
C505	2113741F45	CAP, 6800pF
C506	2113743L41	CAP, .01uF
C507	2113743N50	CAP, 100pF
C509	2113743N50	CAP, 100pF
C508DNP	2113743N01	CAP, 0.5pF
C510	2113743M24	CAP, 0.1uF
C511	2113928C03	CAP, 1.0uF
C513	2113743L41	CAP, .01uF
C514	2113743L41	CAP, .01uF
C515	2113743L41	CAP, .01uF
C516	2113928C03	CAP, 1.0uF
C517	2113743L17	CAP, 1000pF
C518	2113947E01	CAP, .01uF
C512DNP	2113743N16	CAP, 3.9pF
C520	2113928C04	CAP, 4.7uF
C521	2113928C04	CAP, 4.7uF
C522	2113928C04	CAP, 4.7uF
C523	2113928C04	CAP, 4.7uF
C524	2113743N34	CAP, 22pF
C525	2113743N28	CAP, 12pF
C526	2113743N32	CAP, 18pF
C527	2113743N32	CAP, 18pF
C528	2113743N37	CAP, 30pF
C534	2113743N34	CAP, 22pF
C535	2113743L17	CAP, 1000pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C536	2113743L41	CAP, .01uF
C537	2113928C04	CAP, 4.7uF
C538	2113928P04	CAP, 1.0uF
C539	2113743L41	CAP, .01uF
C5300DNP	2113743F18	CAP, 2.2uF
C5301DNP	2113928E03	CAP, 2.2uF
C5302DNP	2113743F18	CAP, 2.2uF
C540	2113743L41	CAP, .01uF
C541	2113743L41	CAP, .01uF
C543	2113928P04	CAP, 1.0uF
C545	2113928P04	CAP, 1.0uF
C546	2113928P04	CAP, 1.0uF
C554	2113743L01	CAP, 220pF
C555	2113743L05	CAP, 330pF
C556	2113743L05	CAP, 330pF
C5501DNP	2113743N26	CAP, 10pF
C5502DNP	2113743N26	CAP, 10pF
C550DNP	2113743N42	CAP, 47pF
C551DNP	2113743N42	CAP, 47pF
C552DNP	2113743N42	CAP, 47pF
C570	2113743M24	CAP, 0.1uF
C571	2113743N50	CAP, 100pF
C572	2113743L19	CAP, 1200pF
C573	0888600M19	CAP, 3300pF
C576	2113743L05	CAP, 330pF
C577	2113743N28	CAP, 12pF
C578	2113743N28	CAP, 12pF
C579	2113743N37	CAP, 30pF
C580	2113743M24	CAP, 0.1uF
C581	2113743N37	CAP, 30pF
C582	2113743N09	CAP, 2pF
C583	2113743N17	CAP, 4.3pF
C600	2113743N34	CAP, 22pF
C601	2113743N13	CAP, 3pF
C602	2113743L41	CAP, .01uF
C604	2113743L05	CAP, 330pF
C605	2113743L05	CAP, 330pF
C606	2113743N54	CAP, 150pF
C607	2113743L05	CAP, 330pF
C608	2113743L05	CAP, 330pF
C609	2113743N54	CAP, 150pF
C6017DNP	2113743N09	CAP, 2pF
C614	2311049A76	CAPP, 2.2uF
C615	2113743N36	CAP, 27pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C6102DNP	2113743N38	CAP, 33pF
C6103DNP	2113743N38	CAP, 33pF
C677	2113743N36	CAP, 27pF
C678	2113743N36	CAP, 27pF
C679	2113743N36	CAP, 27pF
C680	2113743N36	CAP, 27pF
C681	2113743N36	CAP, 27pF
C682	2113743N36	CAP, 27pF
C684	2113928C03	CAP, 1.0uF
C685	2113743L41	CAP, .01uF
C686	2113928C03	CAP, 1.0uF
C800	0662057M01	RES, 0
C801	2113743N28	CAP, 12pF
C807	2113743N37	CAP, 30pF
C849	2113743N28	CAP, 12pF
C850	2113743N28	CAP, 12pF
C851	2113743N38	CAP, 33pF
C852	2113743N32	CAP, 18pF
C860	2113743E20	CAP, 0.1uF
C861	2113743N26	CAP, 10pF
C862	2113743E20	CAP, 0.1uF
C863	2113743N26	CAP, 10pF
C864	2113743G26	CAP, 4.7uF
C865	2113743E20	CAP, 0.1uF
C866	2113743E20	CAP, 0.1uF
C867	2113743N30	CAP, 15pF
C868	2113743N30	CAP, 15pF
C1001	2113947H01	CAP, 0.1uF
C1002	2113947H01	CAP, 0.1uF
C1003	2113947H01	CAP, 0.1uF
C1004	2113947H01	CAP, 0.1uF
C1005	2113947H01	CAP, 0.1uF
C1006	2113743M24	CAP, 0.1uF
C1007	2113743M24	CAP, 0.1uF
C1008	2113947H01	CAP, 0.1uF
C1011	2113947H01	CAP, 0.1uF
C1012	2113743M24	CAP, 0.1uF
C1013	2113743M24	CAP, 0.1uF
C1014	2113743M24	CAP, 0.1uF
C1016	2113947H01	CAP, 0.1uF
C1017	2113947H01	CAP, 0.1uF
C1019	2113743M24	CAP, 0.1uF
C1021	2113743M24	CAP, 0.1uF
C1022	2113743M24	CAP, 0.1uF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C1024	2113743M24	CAP, 0.1uF
C1025	2113743M24	CAP, 0.1uF
C1027	2113947H01	CAP, 0.1uF
C1028	2113743M24	CAP, 0.1uF
C1030	2113743M24	CAP, 0.1uF
C1033	2113743M24	CAP, 0.1uF
C1036	2113947H01	CAP, 0.1uF
C1038	2113743M24	CAP, 0.1uF
C1039	2113947H01	CAP, 0.1uF
C1040	2113743M24	CAP, 0.1uF
C1042	2113743M24	CAP, 0.1uF
C1045	2113947H01	CAP, 0.1uF
C1046	2113743M24	CAP, 0.1uF
C1047	2113743M24	CAP, 0.1uF
C1091	2113928P04	CAP, 1.0uF
C1300	2113743M24	CAP, 0.1uF
C1301	2113743M24	CAP, 0.1uF
C1302	2113743M24	CAP, 0.1uF
C1304	2113743M24	CAP, 0.1uF
C1305	2113743M24	CAP, 0.1uF
C1306	2113743M24	CAP, 0.1uF
C1307	2113743M24	CAP, 0.1uF
C1308	2113743M24	CAP, 0.1uF
C1309	2113743M24	CAP, 0.1uF
C1310	2113743M24	CAP, 0.1uF
C1402	2113743M24	CAP, 0.1uF
C1403	2113743M24	CAP, 0.1uF
C1404	2113743M24	CAP, 0.1uF
C1405	2113743M24	CAP, 0.1uF
C1406	2113743M24	CAP, 0.1uF
C1500	2113743M24	CAP, 0.1uF
C1501	2113743M24	CAP, 0.1uF
C1502	2187893N01	CAP, 1.0uF
C3000	2113928C12	CAP, 10uF
C3001	2113928C12	CAP, 10uF
C3100	2113928C12	CAP, 10uF
C3101	2113928C12	CAP, 10uF
C3150	2113928C04	CAP, 4.7uF
C3200	2113928C12	CAP, 10uF
C3201	2113928C12	CAP, 10uF
C3204	2113743L41	CAP, .01uF
C3205	2113928C04	CAP, 4.7uF
C3207	2113928C12	CAP, 10uF
C3208	2113743N42	CAP, 47pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C3210	2113928C12	CAP, 10uF
C3212	2113928R03	CAP, 0.47uF
C3250	2113928C04	CAP, 4.7uF
C3300	2113928C04	CAP, 4.7uF
C3350	2113928C12	CAP, 10uF
C3400	2113928C12	CAP, 10uF
C3401	2113928C12	CAP, 10uF
C3402	2113743M24	CAP, 0.1uF
C3450	2113928C04	CAP, 4.7uF
C3500	2113928C12	CAP, 10uF
C3501	2113928C12	CAP, 10uF
C3550	2113928C04	CAP, 4.7uF
C3560	2113928C12	CAP, 10uF
C3561	2113928C12	CAP, 10uF
C3562	2113743M24	CAP, 0.1uF
C3600	2113928C04	CAP, 4.7uF
C3601	2113743M24	CAP, 0.1uF
C3650	2113928C04	CAP, 4.7uF
C3651	2113743M24	CAP, 0.1uF
C3652	2113947B05	CAP, 33pF
C3660	2113743M24	CAP, 0.1uF
C3661	2113743M24	CAP, 0.1uF
C3670	2113743M24	CAP, 0.1uF
C3673	2113743L41	CAP, .01uF
C3701	2113928C12	CAP, 10uF
C3702	2113928N01	CAP, 0.1uF
C3703	2113928C12	CAP, 10uF
C3704	2113743N26	CAP, 10pF
C3801	2113928C04	CAP, 4.7uF
C3850	2113928C04	CAP, 4.7uF
C3851	2113928C04	CAP, 4.7uF
C3950	2113928C04	CAP, 4.7uF
C3962	2113743M24	CAP, 0.1uF
C3980	2113928C03	CAP, 1.0uF
C3983	2113743N30	CAP, 15pF
C3984	2113743N30	CAP, 15pF
C4000	2113743M24	CAP, 0.1uF
C4002	2113743L21	CAP, 1500pF
C4003	2113743N38	CAP, 33pF
C4007	2113743N38	CAP, 33pF
C4009	2113947B05	CAP, 33pF
C4100	2113928P04	CAP, 1.0uF
C4102	2113928P04	CAP, 1.0uF
C4160	2113743N38	CAP, 33pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C4161	2113743N26	CAP, 10pF
C4198	2113743M24	CAP, 0.1uF
C4199	2113947H01	CAP, 0.1uF
C4200	2187893N01	CAP, 1.0uF
C4203	2113743N38	CAP, 33pF
C4204	2113743N38	CAP, 33pF
C4207	2113743N38	CAP, 33pF
C4208	2113947B05	CAP, 33pF
C4209	2113743N38	CAP, 33pF
C4210	2113928C04	CAP, 4.7uF
C4300	2113743N26	CAP, 10pF
C4304	2113947E01	CAP, .01uF
C4306	2311049A89	CAPP, 22uF
C4355	2113947B05	CAP, 33pF
C4356	2311049A89	CAPP, 22uF
C4390	2113743M24	CAP, 0.1uF
C4392	2113743N40	CAP, 39pF
C4393	2113743N40	CAP, 39pF
C4395	2113743M24	CAP, 0.1uF
C4400	2113928P04	CAP, 1.0uF
C4401	2113743M24	CAP, 0.1uF
C4500	2113743M24	CAP, 0.1uF
C4501	2113743N38	CAP, 33pF
C4502	2113928C04	CAP, 4.7uF
C4550	2113743L25	CAP, 2200pF
C4551	2113743L41	CAP, .01uF
C5000	2113743M24	CAP, 0.1uF
C5002	2113947B05	CAP, 33pF
C5004	2113743M24	CAP, 0.1uF
C5005	2113928P04	CAP, 1.0uF
C5007	2113743M24	CAP, 0.1uF
C5050	2113743M24	CAP, 0.1uF
C5051	2113928P04	CAP, 1.0uF
C5103	2113743N38	CAP, 33pF
C5104	2113743N38	CAP, 33pF
C5105	2113743N38	CAP, 33pF
C5106	2113743N38	CAP, 33pF
C5107	2113743N38	CAP, 33pF
C5108	2113743N38	CAP, 33pF
C5109	2113743N38	CAP, 33pF
C5110	2113743N38	CAP, 33pF
C5111	2113743N38	CAP, 33pF
C5112	2113743N38	CAP, 33pF
C5113	2113743N38	CAP, 33pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C5114	2113743N38	CAP, 33pF
C5115	2113743N38	CAP, 33pF
C5116	2113743L35	CAP, 5600pF
C5117	2113743L35	CAP, 5600pF
C5203	2113743N38	CAP, 33pF
C5204	2113743N38	CAP, 33pF
C5205	2113743N38	CAP, 33pF
C5208	2113743N38	CAP, 33pF
C5209	2113743N38	CAP, 33pF
C5250	2113743M24	CAP, 0.1uF
C5253	2113743M24	CAP, 0.1uF
C5255	2113743M24	CAP, 0.1uF
C5256	2113743M24	CAP, 0.1uF
C5303	2113928P04	CAP, 1.0uF
C5310	2113743N46	CAP, 68pF
C5311	2113743L25	CAP, 2200pF
C5401	2113743L41	CAP, .01uF
C5402	2113743M24	CAP, 0.1uF
C5405	2113743L41	CAP, .01uF
C5410	2113928C12	CAP, 10uF
C5412	2113928C12	CAP, 10uF
C5503	2113743N26	CAP, 10pF
C5505	2113743N26	CAP, 10pF
C5600	2113743L17	CAP, 1000pF
C5602	2187906N01	CAP, 4.7uF
C5700	2113743N38	CAP, 33pF
C6000	2113743M24	CAP, 0.1uF
C6001	2113743M24	CAP, 0.1uF
C6002	2113743M24	CAP, 0.1uF
C6003	2113743F18	CAP, 2.2uF
C6004	2113743M24	CAP, 0.1uF
C6005	2113743L41	CAP, .01uF
C6006	2113743L17	CAP, 1000pF
C6007	2113743N28	CAP, 12pF
C6008	2113743M24	CAP, 0.1uF
C6009	2113743M24	CAP, 0.1uF
C6010	2113743N28	CAP, 12pF
C6011	2113743N26	CAP, 10pF
C6012	2113743N01	CAP, 0.5pF
C6013	2113743N11	CAP, 2.4pF
C6014	2113743M24	CAP, 0.1uF
C6015	2113743M24	CAP, 0.1uF
C6019	2113928N01	CAP, 0.1uF
C6050	2113743L09	CAP, 470pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C6051	2113743M24	CAP, 0.1uF
C6054	2113743L09	CAP, 470pF
C6055	2113743L09	CAP, 470pF
C6056	2113743L09	CAP, 470pF
C6057	2113743F18	CAP, 2.2uF
C6061	2113743N42	CAP, 47pF
C6062	2113743L13	CAP, 680pF
C6063	2113743L41	CAP, .01uF
C6066	2113928P04	CAP, 1.0uF
C6067	2113743N03	CAP, 1pF
C6068	2113743N32	CAP, 18pF
C6069	2113743N32	CAP, 18pF
C6070	2113743L09	CAP, 470pF
C6073	2113743N52	CAP, 120pF
C6074	2113743N32	CAP, 18pF
C6075	2113743L09	CAP, 470pF
C6076	2113743L09	CAP, 470pF
C6100	2113743L01	CAP, 220pF
C6101	2113928C12	CAP, 10uF
C6105	2113743M24	CAP, 0.1uF
C7501	2113928N01	CAP, 0.1uF
C7502	2113928N01	CAP, 0.1uF
C7503	2113928N01	CAP, 0.1uF
C7504	2113947H01	CAP, 0.1uF
C7506	2113928N01	CAP, 0.1uF
C7507	2113928N01	CAP, 0.1uF
C7508	2113928N01	CAP, 0.1uF
C7509	2113928N01	CAP, 0.1uF
C7510	2113928N01	CAP, 0.1uF
C7511	2113928N01	CAP, 0.1uF
C7512	2113928N01	CAP, 0.1uF
C7513DNP	2113928N01	CAP, 0.1uF
C7900	2113928C12	CAP, 10uF
C7914	2113928N01	CAP, 0.1uF
C7915	2113928N01	CAP, 0.1uF
C7917	2113743N30	CAP, 15pF
C7918	2113743N30	CAP, 15pF
C7919	2113743N30	CAP, 15pF
C7922	2113743N42	CAP, 47pF
C7923	2113743N42	CAP, 47pF
C7925	2113743N40	CAP, 39pF
C7926	2113743N40	CAP, 39pF
C7927	2113743N30	CAP, 15pF
C7928	2113743N36	CAP, 27pF

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C7932	2113928C03	CAP, 1.0uF
C7933	2113743M24	CAP, 0.1uF
C7934	2113928C12	CAP, 10uF
C7935	2113928E03	CAP, 2.2uF
C7938	2113743N30	CAP, 15pF
C7939	2187893N01	CAP, 1.0uF
C900DNP	2113743N28	CAP, 12pF
C901DNP	2113743N42	CAP, 47pF
C902DNP	2113743N42	CAP, 47pF
C903DNP	2113743N42	CAP, 47pF
CR3000	4809924D18	RB520S-30
CR3100	4809653F02	MBRM120T3
CR3960	4809653F02	MBRM120T3
CR3961	4809653F02	MBRM120T3
CR5401	4809948D42	RB751V40
CR7500	4809606E08	RB715F
D5000	4809948D42	RB751V40
D852DNP	4809496B11	QSMG-H799
E100	SHORT_RES0402	SHORT
E101	SHORT_RES0402	SHORT
E102	SHORT_RES0402	SHORT
E103	SHORT_RES0402	SHORT
E901	SHORT_RES0402	SHORT
FL001	4889695L12	ASM3201B
FL002	9109674L20	S0351
FL003	9109674L21	CF61A5601
FL300	9109239M28	SAF2G14KB0
FL401	9109239M16	SAF1G95KB0
FL404	5888234M01	34M01
FL500	9188695K04	95K04
FL510	4889767N01	FLTR
FL800	9109674L17	74L17
FL4000	4889526L03	FLTR
FL4300	4889526L04	FLTR
FL6050	9109239M26	855969
FL6051	9185223E01	DFM2R1575
J4100	5085600J02	SPKR
J4300	0904136G01	CONN_J
J5000	0987636K05	CONN_J
J5100	0987817K05	CONN_J
J5200	0987817K05	CONN_J
J5400	3989331K01	CONN_J
J5500	3909301S02	CONTACT
J5501	3909301S02	CONTACT

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
J7900	0987817K05	CONN_J
L002	2409154M09	IDCTR, 4.7nH
L051DNP	2409377M03	IDCTR, 6.8nH
L062	2409154M66	IDCTR, 18.0nH
L064	2409154M66	IDCTR, 18.0nH
L200	2409377M07	IDCTR, 18nH
L297	2409377M16	IDCTR, 82nH
L298	2409377M16	IDCTR, 82nH
L300	2409154M59	IDCTR, 4.7nH
L301DNP	2409154M30	IDCTR, 3.3nH
L310	2409154M61	IDCTR, 6.8nH
L360	2462587Q39	IDCTR, 220nH
L361	2462587Q39	IDCTR, 220nH
L564	2409154M66	IDCTR, 18.0nH
L570	2409154M99	IDCTR, 82.0nH
L572	2409154M68	IDCTR, 27.0nH
L578	2409154M59	IDCTR, 4.7nH
L579	2409154M59	IDCTR, 4.7nH
L580	2113743N09	CAP, 2pF
L583	2113743N22	CAP, 6.8pF
L615	2409377M03	IDCTR, 6.8nH
L801	2409154M61	IDCTR, 6.8nH
L805	2409154M67	IDCTR, 22.0nH
L806	2409154M12	IDCTR, 8.2nH
L3000	2588866L14	IDCTR, 47uH
L3100	2487659M11	IDCTR, 47uH
L3206	2588866L05	IDCTR, 2.2uH
L4006	2409154M18	IDCTR, 27.0nH
L4007	2409154M18	IDCTR, 27.0nH
L4399	2409646M13	IDCTR, 39nH
L4400	2409646M13	IDCTR, 39nH
L508DNP	2409154M36	IDCTR, 10.0nH
L5310	2589326L02	IDCTR, 0.68mH
L5600	2409154M22	IDCTR, 56.0nH
L5603	2113743N03	CAP, 1pF
L575DNP	2409154M09	IDCTR, 4.7nH
L6002	2113743N09	CAP, 2pF
L6001DNP	2488289M26	IDCTR, 120nH
L6050	2409154M07	IDCTR, 3.3nH
L6051	2409646M87	IDCTR, 33nH
L6052	2409154M10	IDCTR, 5.6nH
L6054	2409154M13	IDCTR, 10.0nH
L7500	0660076S01	RES, 0
L7501	2409154M48	IDCTR, 100nH

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
L7920	2409154M18	IDCTR, 27.0nH
M001	0987378K01	SWITCH
M002	3989868N01	CONTACT
M003	3989868N01	CONTACT
M5200	3988904N01	CONTACT
M5201	3988904N01	CONTACT
M5400	0985888K01	SOCKET
M5700	5962882K02	MOTOR
M6050	0987378K01	SWITCH
M7900	0989668N01	SHIELD
M7902	0989668N01	SHIELD
Q130	4809579E24	2SJ347
Q3700DNP	4809579E42	FDG6304P
Q3701DNP	4809607E02	2SA1774
Q401	4809608E03	DTA114YE
Q500	4809579E65	TN0200T
Q510	4862830F01	SI8401DB
Q901	4809579E58	FDG6332C
Q902	4809579E48	FDC6306P
Q906	4809939C34	EMB10
Q3301	4809579E35	FDG6301N
Q3302	4809579E35	FDG6301N
Q3310	4862830F01	SI8401DB
Q3403	4809607E04	2SB1132
Q3502	4809607E04	2SB1132
Q3610	4809607E04	2SB1132
Q3960	4862830F01	SI8401DB
Q3961	4809807C42	SI8405DB
Q3963	4862830F01	SI8401DB
Q3966	4862830F01	SI8401DB
Q3967	4809939C39	EMD9
Q4300	4809940E03	DTC114TE
Q4301	4809579E24	2SJ347
Q5001	5109817F58	17F58
Q5310	4809579E64	FDG6316P
Q5400	4862830F01	SI8401DB
Q5401	4809579E58	FDG6332C
Q6001	4809579E50	SI1905
Q6100	4809579E58	FDG6332C
R054	2409154M66	IDCTR, 18.0nH
R059	0662057M01	RES, 0
R061	0662057M01	RES, 0
R063	0662057M01	RES, 0
R065	0662057M01	RES, 0

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R066	0662057M01	RES, 0
R106	SHORT_RES0402	SHORT
R107	SHORT_RES0402	SHORT
R1019DNP	0662057M01	RES, 0
R1040DNP	0662057M01	RES, 0
R1046DNP	0662057M01	RES, 0
R130	0662057M74	RES, 1K
R131	0662057N09	RES, 27K
R132	0662057N09	RES, 27K
R133	SHORT_RES0402	SHORT
R140	0662057M62	RES, 330
R162	SHORT_RES0402	SHORT
R200	0662057V04	RES, 12K
R201	SHORT_RES0402	SHORT
R202	SHORT_RES0402	SHORT
R203	SHORT_RES0402	SHORT
R204	SHORT_RES0402	SHORT
R205	0662057N15	RES, 47K
R206	0662057M86	RES, 3.3K
R207	0662057M50	RES, 100
R208	0662057M74	RES, 1K
R220	SHORT_RES0402	SHORT
R221	SHORT_RES0402	SHORT
R222	SHORT_RES0402	SHORT
R223	SHORT_RES0402	SHORT
R224	SHORT_RES0402	SHORT
R225	SHORT_RES0402	SHORT
R226	SHORT_RES0402	SHORT
R227	SHORT_RES0402	SHORT
R228	SHORT_RES0402	SHORT
R229	SHORT_RES0402	SHORT
R298	SHORT_RES0402	SHORT
R300	0662057V04	RES, 12K
R302	0662057M50	RES, 100
R305	0662057M92	RES, 5.6K
R319	SHORT_RES0402	SHORT
R320	SHORT_RES0402	SHORT
R321	SHORT_RES0402	SHORT
R322	SHORT_RES0402	SHORT
R323	SHORT_RES0402	SHORT
R3205DNP	0662057M01	RES, 0
R333	SHORT_RES0402	SHORT
R337	SHORT_RES0402	SHORT
R338	SHORT_RES0402	SHORT

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R339	SHORT_RES0402	SHORT
R340	SHORT_RES0402	SHORT
R431	0662057M01	RES, 0
R432	0662057M01	RES, 0
R440	SHORT_RES0402	SHORT
R450	0662057M95	RES, 7.5K
R451	0662057M90	RES, 4.7K
R452	0662057N17	RES, 56K
R453	0662057N08	RES, 24K
R460	0662057N01	RES, 12K
R461	0662057N09	RES, 27K
R500	0662057M01	RES, 0
R501	0662057M01	RES, 0
R503	0662057M83	RES, 2.4K
R504	0662057M74	RES, 1K
R506	0662057N21	RES, 82K
R512	0662057N03	RES, 15K
R528	0662057M01	RES, 0
R536	SHORT_RES0402	SHORT
R537	0662057N01	RES, 12K
R554	0662057N07	RES, 22K
R556	0662057N23	RES, 100K
R560	SHORT_RES0402	SHORT
R561	SHORT_RES0402	SHORT
R562	SHORT_RES0402	SHORT
R565	SHORT_RES0402	SHORT
R571	2409154M66	IDCTR, 18.0nH
R574	0662057M76	RES, 1.2K
R575	0662057M74	RES, 1K
R576	0662057N09	RES, 27K
R577	0662057M95	RES, 7.5K
R582	SHORT_RES0402	SHORT
R601	SHORT_RES0402	SHORT
R616	0662057M58	RES, 220
R626	SHORT_RES0402	SHORT
R627	0662057N30	RES, 200K
R801	SHORT_RES0402	SHORT
R803	SHORT_RES0402	SHORT
R804	SHORT_RES0402	SHORT
R810	0662057M66	RES, 470
R811	0662057M43	RES, 51
R812	0662057M89	RES, 4.3K
R813	0662057V02	RES, 10K
R814	0662057V02	RES, 10K

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R820	0662057U63	RES, 300
R821	SHORT_RES0402	SHORT
R901	0662057M98	RES, 10K
R902	0662057M98	RES, 10K
R903	0662057N15	RES, 47K
R904	0662057M98	RES, 10K
R912	0662057N15	RES, 47K
R975	0662057M01	RES, 0
R976	0662057M01	RES, 0
R977	0662057M01	RES, 0
R1010	SHORT_RES0402	SHORT
R1011	SHORT_RES0402	SHORT
R1012	0662057N23	RES, 100K
R1018	0662057M01	RES, 0
R1032	0662057M01	RES, 0
R1041	0662057N23	RES, 100K
R1042	0662057N23	RES, 100K
R1043	0662057M98	RES, 10K
R1047	0662057M01	RES, 0
R1050	0662057M01	RES, 0
R1300	SHORT_RES0402	SHORT
R1301	SHORT_RES0402	SHORT
R1302	SHORT_RES0402	SHORT
R1303	SHORT_RES0402	SHORT
R1305	0662057M86	RES, 3.3K
R1400	SHORT_RES0402	SHORT
R1500	0662057M98	RES, 10K
R1501	0662057N20	RES, 75K
R3000	0687874L02	RES, 0.1
R3001	SHORT_RES0402	SHORT
R3103	SHORT_RES0402	SHORT
R3153	SHORT_RES0402	SHORT
R3203	SHORT_RES0402	SHORT
R3204	SHORT_RES0402	SHORT
R3208	SHORT_RES0402	SHORT
R3210	0662057V40	RES, 240K
R3211	0662057V31	RES, 140K
R3212	0662057M50	RES, 100
R3251	SHORT_RES0402	SHORT
R3301	SHORT_RES0402	SHORT
R3310	SHORT_RES0402	SHORT
R3350	SHORT_RES0402	SHORT
R3402	SHORT_RES0402	SHORT
R3403	0687874L02	RES, 0.1

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R3404	SHORT_RES0402	SHORT
R3451	SHORT_RES0402	SHORT
R3503	SHORT_RES0402	SHORT
R3504	0687874L02	RES, 0.1
R3553	SHORT_RES0402	SHORT
R3554	0662057M50	RES, 100
R3560	SHORT_RES0402	SHORT
R3561	0687874L02	RES, 0.1
R3601	SHORT_RES0402	SHORT
R3650	0662057M78	RES, 1.5K
R3651	0662057M36	RES, 27
R3652	0662057M36	RES, 27
R3653	SHORT_RES0402	SHORT
R3654	0662057M98	RES, 10K
R3660	0662057N23	RES, 100K
R3661	0662057N21	RES, 82K
R3662DNP	0662057M01	RES, 0
R3670	0662057N23	RES, 100K
R3673	0662057N23	RES, 100K
R3672DNP	0662057M01	RES, 0
R3701	SHORT_RES0402	SHORT
R3702	0662057V02	RES, 10K
R3703	0662057U98	RES, 7.5K
R3704	0662057M01	RES, 0
R3705DNP	0662057M01	RES, 0
R3706DNP	0662057M01	RES, 0
R3707DNP	0662057M98	RES, 10K
R3708DNP	0662057M98	RES, 10K
R3801	SHORT_RES0402	SHORT
R3850	SHORT_RES0402	SHORT
R3851	SHORT_RES0402	SHORT
R3950	0662057M74	RES, 1K
R3951	SHORT_RES0402	SHORT
R3960	SHORT_RES0402	SHORT
R3961	0687874L01	RES, 0.24
R3962	0662057M92	RES, 5.6K
R3963	0662057N30	RES, 200K
R3964	SHORT_RES0402	SHORT
R3965	SHORT_RES0402	SHORT
R3966	0662057M98	RES, 10K
R3967	0662057M98	RES, 10K
R3968	0662057N30	RES, 200K
R3970	SHORT_RES0402	SHORT
R4008	0662057M34	RES, 22

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R4009	0662057M34	RES, 22
R4010	0662057N39	RES, 470K
R4011	0662057N39	RES, 470K
R4012	0662057N47	RES, 1MEG
R4103	0662057M90	RES, 4.7K
R4104	0662057M68	RES, 560
R4200	0662057N03	RES, 15K
R4201	0662057N07	RES, 22K
R430DNP	0662057M01	RES, 0
R4392	0662057M68	RES, 560
R4393	0609591M37	RESNET, 10K
R4396	0662057M90	RES, 4.7K
R4397	0662057N39	RES, 470K
R4398	0662057N15	RES, 47K
R4400	0662057M50	RES, 100
R4401	0662057M74	RES, 1K
R4550	0662057N06	RES, 20K
R5000	0662057N23	RES, 100K
R5001	0662057N15	RES, 47K
R5010DNP	0662057M01	RES, 0
R5050	0662057N15	RES, 47K
R5052	0662057N33	RES, 270K
R5053	0662057M86	RES, 3.3K
R5100	0662057M01	RES, 0
R5101DNP	0662057M01	RES, 0
R5201	SHORT_RES0402	SHORT
R5202	SHORT_RES0402	SHORT
R5291	SHORT_RES0402	SHORT
R5293	0662057M98	RES, 10K
R5294	0662057N23	RES, 100K
R5300	SHORT_RES0402	SHORT
R5302	0662057M01	RES, 0
R5306	SHORT_RES0402	SHORT
R5307	0662057N21	RES, 82K
R5301DNP	0662057M01	RES, 0
R5305DNP	0662057M01	RES, 0
R5310	0662057N23	RES, 100K
R5312	0662057N23	RES, 100K
R5315DNP	0662057M01	RES, 0
R5317DNP	0662057N23	RES, 100K
R5401	0662057M90	RES, 4.7K
R5402	0662057M50	RES, 100
R5403	0662057N13	RES, 39K
R5404	0662057M98	RES, 10K

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R5405	0662057N39	RES, 470K
R5406DNP	0662057M01	RES, 0
R5480	0662057M98	RES, 10K
R5481	0662057V11	RES, 22K
R5482	0662057V43	RES, 330K
R5501	0662057M92	RES, 5.6K
R5502	0662057M01	RES, 0
R5503	0662057M50	RES, 100
R5504	0662057M01	RES, 0
R5600	0662057M96	RES, 8.2K
R5601	0662057N23	RES, 100K
R5602	0662057M01	RES, 0
R5604	0662057M96	RES, 8.2K
R5605	SHORT_RES0402	SHORT
R5606	0662057N37	RES, 390K
R5607	2409154M10	IDCTR, 5.6nH
R5603DNP	0662057M01	RES, 0
R6001	0662057M46	RES, 68
R6002	0609591M49	RESNET, 100K
R6003	0609591M49	RESNET, 100K
R6004	0662057M82	RES, 2.2K
R6005	SHORT_RES0402	SHORT
R6006	SHORT_RES0402	SHORT
R6007	0662057N23	RES, 100K
R6008DNP	0662057M74	RES, 1K
R6012	0662057N23	RES, 100K
R6051	0662057M94	RES, 6.8K
R6100	0662057N23	RES, 100K
R6103	0609591M49	RESNET, 100K
R7508	0662057M98	RES, 10K
R7501DNP	0662057M01	RES, 0
R7509DNP	0662057M01	RES, 0
R7510	0662057M01	RES, 0
R7513	0662057M01	RES, 0
R7511DNP	0662057M01	RES, 0
R7576	SHORT_RES0402	SHORT
R7901	0662057M98	RES, 10K
R7902	0609591M25	RESNET, 1K
R7904	0662057M38	RES, 33
R7910	0662057M98	RES, 10K
R7932	0662057M74	RES, 1K
R7933	0662057M74	RES, 1K
R7936	0662057N21	RES, 82K
R7940	0662057M46	RES, 68

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R7941	0662057M46	RES, 68
R7942	0662057M46	RES, 68
R7943	0662057M46	RES, 68
R7944	0662057M46	RES, 68
R7945	0662057M46	RES, 68
R7946	0662057M46	RES, 68
R7947	0662057M46	RES, 68
R7948	0662057M46	RES, 68
R815DNP	0662057M98	RES, 10K
R816DNP	0662057M64	RES, 390
R817DNP	0662057M89	RES, 4.3K
S1	4087635K01	SWITCH
S2	4087635K01	SWITCH
S3	4087635K01	SWITCH
SH01	2688097N01	SHIELD
SH02	2688098N03	SHIELD
SH03	2688099N01	SHIELD
SH04	2688100N01	SHIELD
SH05	2688101N01	SHIELD
SH06	2688102N01	SHIELD
SH07	2688103N01	SHIELD
SH08	2688104N02	SHIELD
SH09	2688105N01	SHIELD
SH10	2688106N01	SHIELD
SH11	2688107N03	SHIELD
SH12	2688108N03	SHIELD
SH13	2688109N03	SHIELD
SH14	2688110N03	SHIELD
SH15	2688111N01	SHIELD
SH16	2688096N01	SHIELD
SH5200	PT26LVLA01	SHIELD
SH5201	PT26LVLA01	SHIELD
SH5202	PT26LVLA01	SHIELD
T300	5889035N01	HHM1525
T600	5885949K08	HHM1409
T601	5885949K09	HHM1410
T602	5885949K05	HHM1525
TP1000	TPSM1_016	TEST_POINT
TP1005	TPSM1_016	TEST_POINT
TP_4GHz_TRAP_L	TPSM0_65SQ	TEST_POINT
U101	5188450M11	50M11
U1000	5199149J02	DSPIO
U1019	5109522E14	TC7S32F
U1018DNP	5109522E90	NC7SP125

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
U200	5109817F72	MAX2395
U300	5109817F73	MAX2396
U400	5109908K55	PA2001_5W
U406	5109768D08	LM20
U407	5187970L13	DD02-92
U500	5188450M05	50M05
U510	5109522E63	NC7WZ04
U1020	5109522E82	NC7SB3157
U1046	5109522E84	NC7WZ17
U1300	5199146J01	28F640W18
U1310	5199146J01	28F640W18
U1400	5109509A55	K4M64163
U1500	5187482N06	SDBT2FCH-512
U3000	5188450M06	50M06
U3200	5109512F48	LP2985
U3206	5187970L31	LTC3406
U3210	5113837M37	NL17SZ04
U3650	5164751E01	MC74VHC1GT50
U3651	5109522E90	NC7SP125
U3660	5186311J23	NC7SZ126
U3670	5186311J23	NC7SZ126
U3700	5109512F46	ILC7081
U3960	5109512F51	NCP304
U5000	4889526L01	CSPEMI-306
U5001	4889526L02	CSPEMI-307
U5010	5109522E82	NC7SB3157
U5011	5109522E82	NC7SB3157
U5210	5113837A30	NLSF1174
U5211	5113837A30	NLSF1174
U5220	5113837M32	NL27WZ00
U5240	5113837M31	NL17SZ74
U5300DNP	5185353D23	LM2665
U5301DNP	5113837M35	TC7W32FK
U5302DNP	5109522E14	TC7S32F
U570	4809283D97	83D97
U580	5885924L15	RAC10-1A-E
U625	5109940K41	LIFE_30PIN
U626	5185353D14	LP3985
U800	5109908K74	08K74
U801	5885811G11	DD05-EN722
U900	5109522E83	NC7SZ11
U5310	5186569G04	D371A
U5600	4889695L14	95L14
U6000	5109841C70	GSP2E

Table 11. Electrical Parts List - cont'd

Reference Number	Part Number	Description
U6001	5199342A01	GT28F800B
U6002	5109522E17	TC7S00FU
U6004	5109522E53	NC7SZ125
U6050	5187970L16	GRF2I_LP
U6051	5105739X12	BGA428
U6100	5162852A33	HSDL3202
U7500	5189251L03	MC30200
U7510	5162852A58	NLAS44599
U7511	5162852A58	NLAS44599
U7513DNP	5109522E35	TC7S86FU
U7540	5164751E01	MC74VHC1GT50
VR4300	4809948D44	CSPESD304
VR5005	4813830C29	MMSZ5246B
VR5100	4813830M74	MMBZ6V8ALT1
VR5101	4888938N01	TPS852
VR7505	4809948D44	CSPESD304
VR7507	4809948D44	CSPESD304
VR7508	4809948D44	CSPESD304
VR7509	4809948D44	CSPESD304
VR7510	4809948D44	CSPESD304
VS4200	4809788E06	UDZTE-176.8B
VS4201	4809788E06	UDZTE-176.8B
VS5001	4813830C29	MMSZ5246B
VS5002	4809788E06	UDZTE-176.8B
VS5402	4809788E06	UDZTE-176.8B
VS5405	4809788E08	UDZS8_2B
VS5400DNP	4809788E06	UDZTE-176.8B
VS5401DNP	4809788E06	UDZTE-176.8B
Y130	4809718L14	NT5032SA
Y500	4809612J43	XTAL
Y3982	4809995L13	CC5V
Y6050	4885169E03	TX2949