MOTOROLA

Personal Communications Sector

GSM Service Support Level 3 Authorized

A008 / A6188 +

GSM Service Support

Training - Documentation - Engineering

Level 3
Circuit Description
03 / 03 / 01
V1.1

A6188 Level 3 Product Guide

RF: Receive

1) The RF Signal from the base station is received through the Antenna A1 and is fed to RF Switch U101, This connects RF to the Aux RF port or the antenna, and isolates TX from RX. The switch is controlled primarily by the following signals **SW_RF:** This is a 50Ω load signal from **Pin 2** of the Accessory Socket J600, when an external device is attached. RX / TX isolation is achieved using the negatively biased signals from Q101 and Q102. These devices use the signals **MIX_275** (**RX_EN + RF_V2** through Q340) and **PAC_275** (**TX_EN + RF_V2** through Q321 and Q320) to produce the Transmit and Receive switching signals. The negative bias is produced using **-5V** through Q104, Q105, these 2 transistors are used to provide the RF Switch with the correct switching voltages (for RX Mode 0 – 2.7V, for TX Mode –5V to 2.7V) and Q106 is used to change the output path between Antenna and Buttplug. The control signals from Q101 and Q102 are then fed to **Pins 2** and **9** of the RF switch. These 3 signals, supported by the voltages **GSM_LNA275** (**MIX_275 + GSM_SEL**) and **DCS_LNAS275** (**DCS_SEL and MIX_275**) both through Q342 select whether the signal is Transmitted or Received.

2) Provided **MIX_275** is high, then the received signal will be passed to the band pass filter FL460, for GSM 900 and to FL450 for GSM 1800. The filters will then pass the frequency range (GSM 1800 or GSM900), and remove any existing harmonics or other unwanted frequencies.

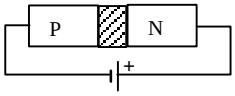
3) The signal will be fed into the appropriate Low noise Amplifier Circuit, Q461 for GSM 900 and Q451 for DCS. This part of the circuit is critical in the achievement of a very low signal to noise ratio, therefore as can be seen around the actual amplifiers, a large amount of external frequency matching and noise reduction circuitry is involved. The LNA's are supported by **MIX_275** and are biased on or off by **GSM_LNA275** for Q461and **DCS_LNAS275** for Q451.

4) The appropriate signal is then fed onto FL470 (For GSM 900 or FL465 (For GSM 1800) where any harmonics created during amplification are removed.

5) The amplified signal is now injected to the base of the dual transistor mixer Q1254. Both mixers are supported by **MIX_275** (Q340).The tuned emitter biasing voltage is provided by **GSM_LNA275** (Q342) and **DCS_LNA275** (Q342)

6) The RX VCO Varactor CR250. Is the active component used within the RX VCO, basically a Varactor diode works in the following way:
When a reverse voltage is applid to a PN junction , the holes in the p-region are attracted to the anode terminal and electrons in the n-region are attracted to the cathode terminal creating a region where there is little current.This region ,the depletion region, is essentially devoid of carriers and behaves as the dielectric of a capacitor.
The depletion region increases as reverse voltage across it increases; and since capacitance varies inversely as dielectic thickness, the junction capacitance will

decrease as the voltage across the PN junction increases. So by varying the reverse voltage across a PN junction the junction capacitance can be varied .This is shown in the typical varactor voltage-capacitance curve below. **Fig 6.1.** This variable



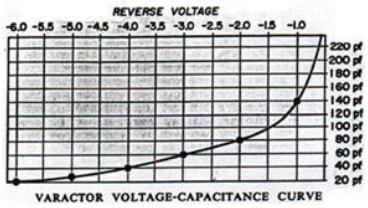


Fig 6.1

capacitence can then be used along with the inductive strip (PCB Tracks lying very close) to provide a LC tuning resonant circuit.
The tuning voltage for the varactor is provided by **CP_RX** (MAGIC U913 **Pin A1**). The VCO amplification is made up of 3 transistor stages Q253, Q255 and Q262, these are supported by the voltage **RVCO_250** (**SF_OUT** through Q344). The collector output from Q255 provides the Phase locked loop feedback to the MAGIC IC **Pin A3,** to ensure the RX VCO frequency changes in line with the Received signal to give the correct IF.

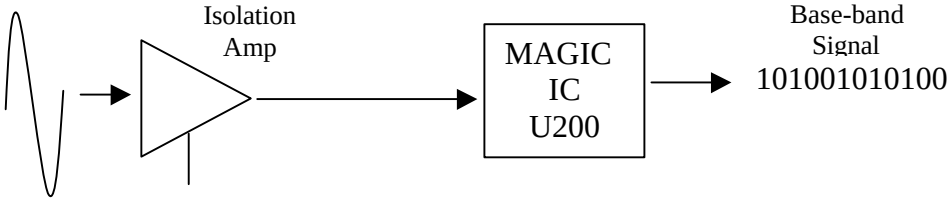
7) Within the mixer, the received frequency and the RX VCO frequencies are mixed sum and difference signals are created, it will be the difference signal of 400Mhz that will be created.

8) The – IF, is now fed to the SAW FL457 filter (Surface Acoustic Wave), this filter is the same as was used in previous 400MHz products. The purpose of the SAW filter is to provide comprehensive removal of harmonics created during the mixing process. The reason the IF was changed from 215Mhz to 400Mhz was for the following reason:

Description	IF	Channel	Received Frequency	RX VCO Frequency	Difference
EGSM L Channel	400Mhz	975	925.2Mhz	1325.2Mhz	154.6Mhz
DCS H Channel	400Mhz	885	1879.8Mhz	1479.8Mhz	
EGSM L Channel	215Mhz	975	925.2Mhz	1140.2Mhz	524.6Mhz
DCS L Channel	215Mhz	810	1879.8Mhz	1664.8Mhz	

The above table demonstrates that if 215Mhz were used instead of 400Mhz, the RX VCO would be required to operate over an extra 370Mhz. With this need eliminated, the part count and therefore the cost are reduced.

9) The 400Mhz IF signal is then passed to the Isolation Amplifier Q490
The purpose of an Isolation Amp is to couple an analogue signal to adjoining parts of a circuit with 2 different grounds. Also to protect the base band signals produced in MAGIC from any stray RF. The Isolation Amp is supported by **SW_VCC** (MAGIC U200 **Pin C7**)



10) The signal is then passed to the MAGIC IC U200 **PRE IN Pin A7**

11) The signal is demodulated internally using an external Varactor diode RX Local Oscillator set up CR259, which is driven by **LO2 CP Pin A9** of MAGIC U200.

12) Where in earlier products, we used to have **RX RXQ, and I** these signals are now only used in digital form within the MAGIC and cannot be measured without technical set up. The demodulated signal is now converted internally to digital form to be passed along an RX SPI bus to the Whitecap.

13) The **RX SPI** signal is made up of **BDR** (Base band Data Receive), **BFSR** (Base band Frame Synch Receive) and **BCLKR** (Base band Clock Receive, fed from MAGIC **Pins G8, G9 and F7** respectively.

14) The Whitecap U800 receives these signals on **Pins A3, D4 and B4,** within the Whitecap the signal is digitally processed. Baud rate reduced, Error correction bits removed, etc…

15) The digital signal is now being fed down the **DIG_AUD** SPI bus to the GCAP II U900, internally to the GCAP, the digital signal is converted to analogue and distributed to the correct outputs

16) For Earpiece, from GCAP II **Pins H6 and H7** to Speaker Pads J9833 **Pins 1 and 2**

17) The Alert is generated within the Dragon ball IC U2000, and not GCAP II given the appropriate data from the incoming signal, SMS, call etc… an interrupt from the alert is fed back to the GCAP, via the signal **SPEAK_TP915**. This signal is supported by the signal **PDA_VCC** (**ALRT_VCC** (Q938 on AL) to **SECOND_VCC** (PDA) and then to **PDA_VCC** through Q9800.

18) For the headset only the **SPKR-** signal is used GCAP II **Pin H6** and feeds the Headset Connector J650, **Pin 3**.

RF: Transmit

1) There are 2 Mic inputs, firstly from the Xcvr mic J910 **Pin 2**, where the analogue input is fed to the GCAP II U900 **Pin J2**

2) Secondly the analogue voice can be fed from the Aux Mic attached to the headset and will be routed from **connection 1** of the Headset Jack J504, through to GCAP II, **Pin H3**. The Aux mic input is amplified through U980 which is supported by **BOOM_PWR** (**BOOM_EN**-Whitecap +**V2**)

3) Within the GCAP II the analogue audio will be converted to digital and clocked out onto the **DIG_AUD** SPI bus to the Whitecap U800.

4) It is within the Whitecap that all information about the transmission burst is formulated i.e. The timing of the burst / The channel to transmit on / The error correction protocol / In which frame the information will be carried to the base station, etc, etc…

5) All this information is then added to the digitised audio and is transferred to the MAGIC U200 along the TX SPI bus. The bus is made up of **BCLKX** (Base band Clock Transmit) **Pin B3** and **BDX** (Base band Data Transmit) **Pin B6**. The timing for

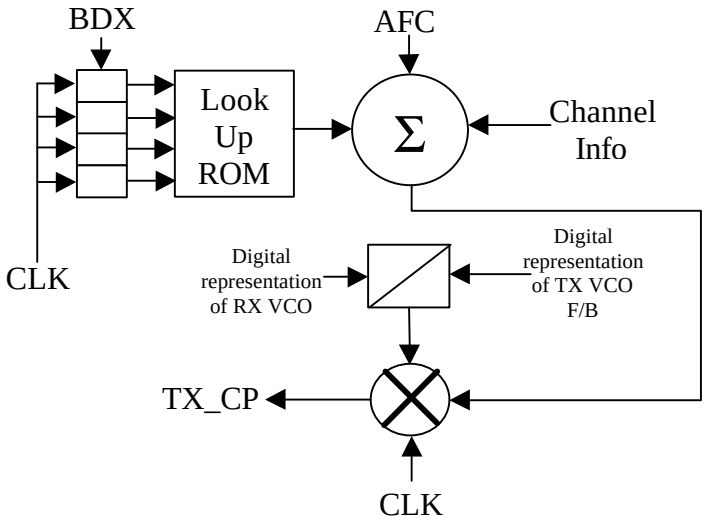
this data is already decided for the transmission burst, and therefore a frame synch is not required.

6) The SPI bus signals enters into the MAGIC at **Pin G7** (**BCLKX**) and **Pin J2** (**BDX**)

7) The operation of the MAGIC is very complex and with respect to the transmit path, integrates the functions of the Modem and its function of GMSK (Gaussian Minimum Shift Keying) and also the functions of the TIC (Translational Integrated Circuit).

8) A very basic block view of how the transmit path works within the MAGIC is demonstrated in: Fig 8.1

Internal MAGIC Operation **Fig 8.1**



9) The data is transmitted from Whitecap to MAGIC on TX SPI bus **BDX**, within the MAGIC each bit of data is clocked into a register. The clocked bit and the 3 preceding bits on the register are then clocked into the look up ROM, which looks at the digital word and from that information downloads the appropriate GSMK digital representation. Channel information and AFC information from MAGIC SPI is then added to this new digital word, this word is then representative of the TX IF frequency of GIFSYN products. As in the case of the TIC, the TX frequency feedback and the RX VCO frequency are mixed to give a difference signal, this is digitally phase compared with the 'modulation' from the look up ROM. The difference creates a DC error voltage **TX_CP** that forms part of the TX Phase locked loop.

10) The error correction voltage **CP_TX** is then fed from **Pin B1** of MAGIC to **Pin 8** of the TX VCO IC U250, adjoining this line is the loop filter (See Loop Filter document on the GSM Service Support Website).

11) The Loop filter comprises mainly of U200 / Q201 / Q202 and C205 and it's main function is to 'smooth' out any overshoots when the channel is changed, see Fig 11.1. If this overshoot were fed to the TX VCO the resulting burst would not meet the world standards for GSM with respect to bandwidth, see Fig 11.2.

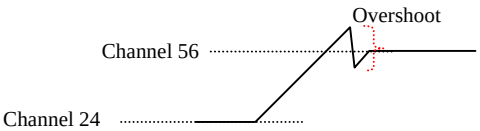


Fig 11.1

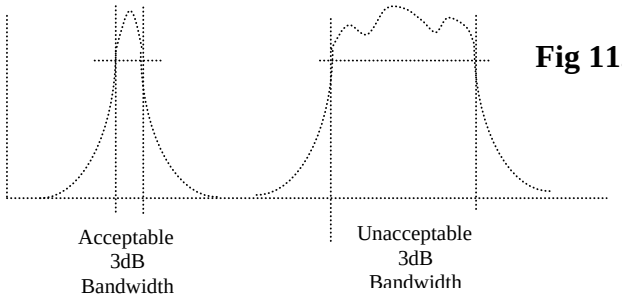


Fig 11.2

12) The Loop filter basically acts then as a huge capacitor and resistor to give a long CR time for smoothing. It uses a small capacitor and the very high input impedance buffer Op-Amp. During the **TX_EN** (Whitecap) period when the transmitter is preparing to operate the capacitor charges, then on receipt of **DM_CS** (Whitecap) when the Transmitter actually fires; the capacitor discharges through the Op-Amp giving a smooth tuning voltage, carrying modulation to the TX VCO. The support voltage for the Loop filter is **V1_FILT** (**V1** + **MAGIC Pin C2**).

13) The TX VCO IC now creates our required output frequency with the support signals **D_TX_VCO** (**DCS_SEL** (MAGIC **Pin C4**) +**TVCO_250** (Q343) through Q333) and **G_TX_VCO** (**GSM_SEL** (U201) +**TVCO_250** (Q343) through Q333), to enable either GSM or DCS frequency production and the IC Power is supported by **SF_OUT** (MAGIC).

14) The output signal is now split with a sample sent back to MAGIC to control the TX Phase locked loop

15) The remaining signal is then fed out through a pre amplifier Q455, which is supported via **PAC_275**

16) To prevent the output frequency from the TX VCO before stabilisation has occurred, being amplified and transmitted, there are Isolation Diodes CR300 (DCS) and CR301 (GSM) placed. This is biased 'on' by the exciter voltage from the PAC IC U350 (Power Amplifier Control IC); **Pin 7** this allows the TX output frequency through to the Exciter stages Q300 and Q400 respectively and at same time gives more or less drive to the exciter stage via Q301 (supported by **G_TX_VCO** and **D_TX_VCO**) The exciter stages are supported by **PA B+ (B+ and PAC_275** through Q330.

17) The signal is then fed to a two separate uni-stage, narrow bandwidth Integrated PA's made up from Q300 (DCS) and Q400 (GSM), these are driven by the exciter voltage from the PAC IC, and supported by **PA_B+.** Name changes to **DCS_PA_B+** for U400. The PA is negatively biased using **–5V_SW** and for GSM using the transistor network Q303, Q304 and Q301, for DCS using Q302, Q303 and Q301.

18) PA matching is achieved using the MCIC Filter FL300 and the signal **GSM_PINDIODE** (**-5V** and **DCS_SEL** through Q322). The signal switches in or out tuning stubs within the MCIC to provide correct matching. The MCIC filter also samples off part of the transmitted power to feed back to the PAC IC U340

19) The signal now goes through FL1000, FL1000 is a low pass filter, filtering 2nd and 3rd harmonics of GSM and DCS frequencies.

20) The amplified signal is then fed through to the RF switch U101, which again is controlled as was discussed in **Receive**, then passed to the Antenna A1/ Accessory Socket Switch J600

RF: Power Control Operation

1) The PAC IC U350 (Power Amplifier Control Integrated Circuit) controls the power control of the transmitter. Below is a list of the main signals associated with the PAC IC and their purposes.

2) The RF detector (**RF_IN Pin 2**) provides a DC level proportional to the peak RF voltage out of the power amplifier, this is taken via an inductive strip from the output of the PA Q370.

3) **DET_SW Pin 11**. This pin controls the variable gain stage connected between the RF detector and the integrator. The gain of the variable stage will be unity when **DET_SW** is low and will be 3 when **DET_SW** is high (floating).

4) **TX_KEY Pin 10**. This signal is used to 'pre-charge' the Exciter and P.A. and occurs 20µS before the start of the transmit pulse.

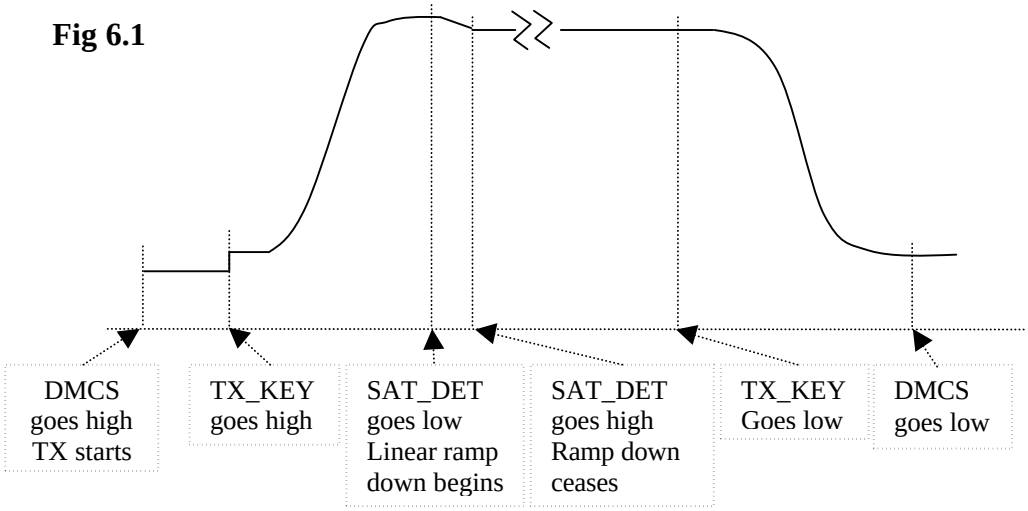
5) **EXC Pin 7**.This output drives the power control port of the exciter. An increase of this voltage will cause the exciter to increase its output power.

6) **SAT_DET Pin 12**. If the feedback signal from the RF detector lags too far behind the AOC signal then this output will go low, indicating that the loop in at or near saturation. This signals the DSP to reduce the **AOC_DRIVE** signal until **SAT_DET** rises. See **Fig 6.1**

7) **AOC_DRIVE Pin 8**. The voltage on this pin will determine the output power of the transmitter. Under normal conditions the control loop will adjust the voltage on EXC so that the power level presented to the RF detector results in equality of the voltage present at INT and AOC. The input level will be between 0 and 2.5V.

8) **ACT Pin 9**. This pin will hold a high voltage when no RF is present. Once the RF level increases enough to cause the detector to rise a few millivolts then this output will go low. In the GSM radio a resistor is routed between this point and the AOC input to cause the radio to ramp up the power until the detector goes active.

Fig 6.1



Logic: Power Up sequence

1) The power up sequence is very similar to Kramer with the 2 sources of power being the battery which is a slim version of the Zap battery (SNN5713A), or using an External B+ source. The unit will not operate without the battery.

2) The battery component consists of 4 output leads: serial data, ground, power supply (+) and temperature sensor.

- **BATT_SER_DATA**: J613. It connects to Whitecap Pin H5 to be used to communicate both ways with the internal EEprom on the battery. This is used to determine if the battery is authentic and what the battery charging profile is to be used. (Sometimes known as **OWDAT**)
- **Ground**: J612. It connects to be used as the reference ground
- **BATT +**: J611. It provides the main PCB with source voltage. The voltage range of A008 battery is from 1.4 VDC (after discharging) to 5.1 VDC (after charging).
- **BATT_THERM**: J610. Is used to determine the temperature of the battery. The temperature of the battery determines the end of the battery charging cycle. In order to protect the charging circuit, this line will be measured constantly during the charging period by GCAP II (U900 **Pin B3**)

  THERM: This is used to ensure that a battery is present when the phone is powered up, therefore ensuring the SIM card cannot be removed whilst the unit is powered up.

  (Q628 is used to reduce standby current)

  The A008 will use two types of charging batteries– Ni-MH battery and Li-ION battery. The unit derives its power from the battery in the following way, **BATT +** is

controlled through Battery FET Q942 by GCAP II Output **Pin F10** and is output as **B+**

2) Once **B+** is available the unit carries out the following checks:

- The battery temperature is monitored to establish whether rapid charge is required, (J610 **BATT_THERM_AD** to GCAP II **Pin B3**)
  -40 deg C – 2.75V 25 deg C – 1.39V 40 deg C – 0.96V
- Charger sensed (J600 **Pin 5** **MANTEST_AD** to GCAP II **Pin A1**) This is achieved using different sense resistors within the accessory.
  For DHFA Charger - 2.75V For Fast Charger – 2.13V
- Senses battery voltage (GCAP II **Pin F7** – **BATT+**)
- Senses input B+ level GCAP II **Pin E10** – **B+**)
  If **EXT B+** is available the current will be passed through protection diode CR940 and output as **B+** to provide power to the PCB.

3) The GCAP II is programmed to Boost mode (5.6V) by **PGM0** **Pin G7** and **PGM1** **Pin G8** both being tied to Ground. Once **B+** is applied to GCAP II **Pin K5**, all the appropriate voltages to supply the circuit are provided. These are:

- **V1** – Programmed to 5.0V. **V1** is at 2.775V at immediate power on, but is 'boosted' to 5.0V through the switch mode power supply L901 / CR901 and C934. See **Fig 6.1** for basic operation.

- **V1** supplies the DSC bus drivers, negative voltage regulators and MAGIC. **V1** is created from GCAP II **Pin A6** and can be measured on C906.

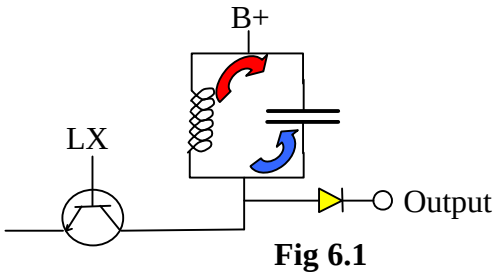


Fig 6.1

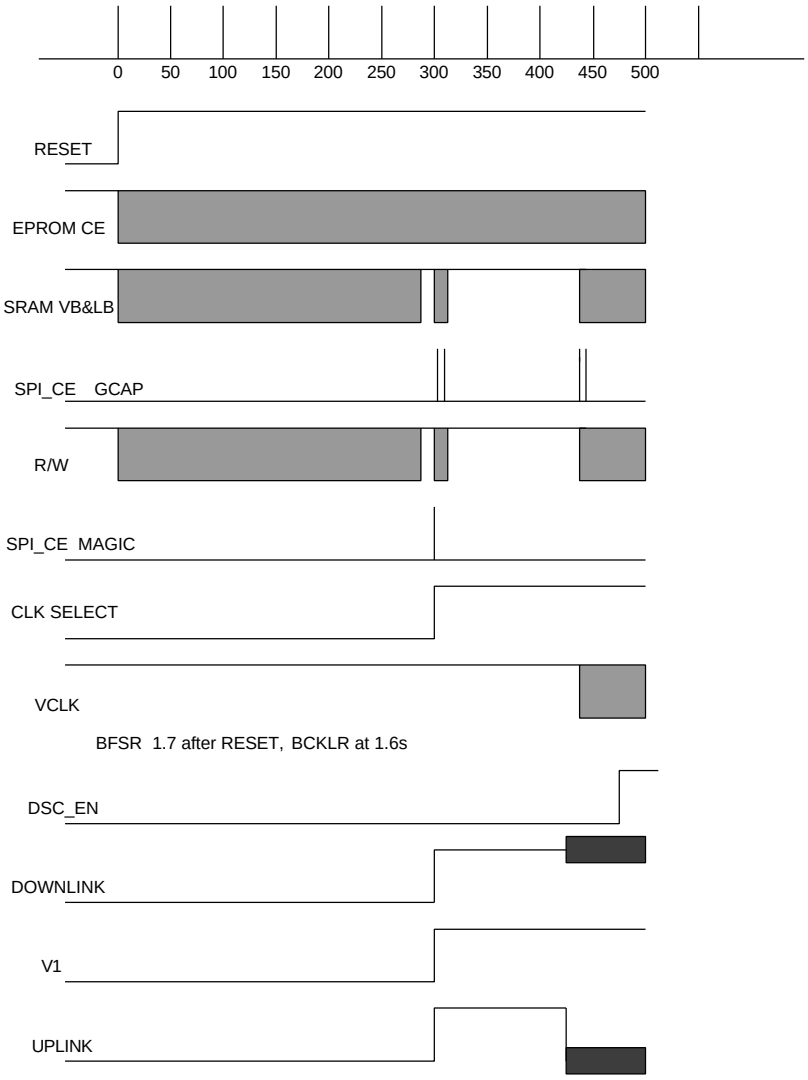
The basic circuit operation for the Boost circuit is as follows the **LX** signal (GCAP II **Pin B10**) allows a path for **B+** to charge the capacitor, when the switch is on, the capacitor then discharges through the inductor (switch off), setting up an electric field. The field then collapses setting up a back EMF to charge the capacitor, and so on and so on. The back EMF created by the inductor is greater than **B+** with the +ve half of the cycle passing through the diode to charge a capacitor from where the **V_BOOST** voltage is taken. The frequency of the switching signal **LX** decides the duty cycle of the output wave and therefore the resultant voltage. **V_BOOST** is fed back into the GCAP.
On initial power up the **LX** signal is not always immediately correct in frequency, therefore the duty cycle of the **B+** signal is incorrect which can lead to the switch mode power supply creating huge current problems. To prevent this Q9808 is placed with Q902 as a protection circuit.

As excess current is drawn through **B+** towards L901 through Q9808 source, **Pin 4**. Q902 base will go low forcing its collector high. This high on **Pin 3** Gate of Q9808 will switch off Q9808, therefore preventing **B+** to the power supply, until **LX** is stable.

- **V2** – Programmed to 2.775V, available whenever the radio is on and supplies most of the logic side of the board. **V2** is supplied out of GCAP II **Pin J2** and can be measured on either C923 or C924.
- **V3** – Programmed to 2.003V to support the Whitecap, but does support the normal 2.75V logic output from the Whitecap, it originates from GCAP II **Pin B5** and can be measured on C926 or C927.
- **VSIM1** – Used to support either 3V or 5V SIM cards. Will dynamically be set to 3V upon power up, but if the card cannot be read then the SIM card is powered down and an attempt to read the card at 5V is tried. **VSIM1** can be measured on C928 and is distributed from GCAP II **Pin C6** (For further information, see SIM Card Operation).
- **VREF** – Programmed as **V2** i.e. 2.775 and provides a reference voltage for the MAGIC IC, distributed from GCAP II **Pin G9** and can be measured on C939.
- **-5V –** Used to drive TX Biasing, produced from **LS_V1** and **–5V_EN** through U901
- **SR_VCC** – **Power Cut Circuit -** Used to buffer the SRAM U702 voltage with a built in soft reset within the unit's software. The reason for this is to protect the user from any accidental loss of power up to 0.5 seconds i.e. If the unit is knocked, causing a slight battery contact bounce, the **SR_VCC** will, to the user, keep the unit running normally, whilst internally the unit resets itself. During this loss of power the unit takes it's power from a the **RTC BATT. SR_VCC** is created from a buffered **V2** using R9922
- **V1_SW –** See **Deep Sleep Mode**

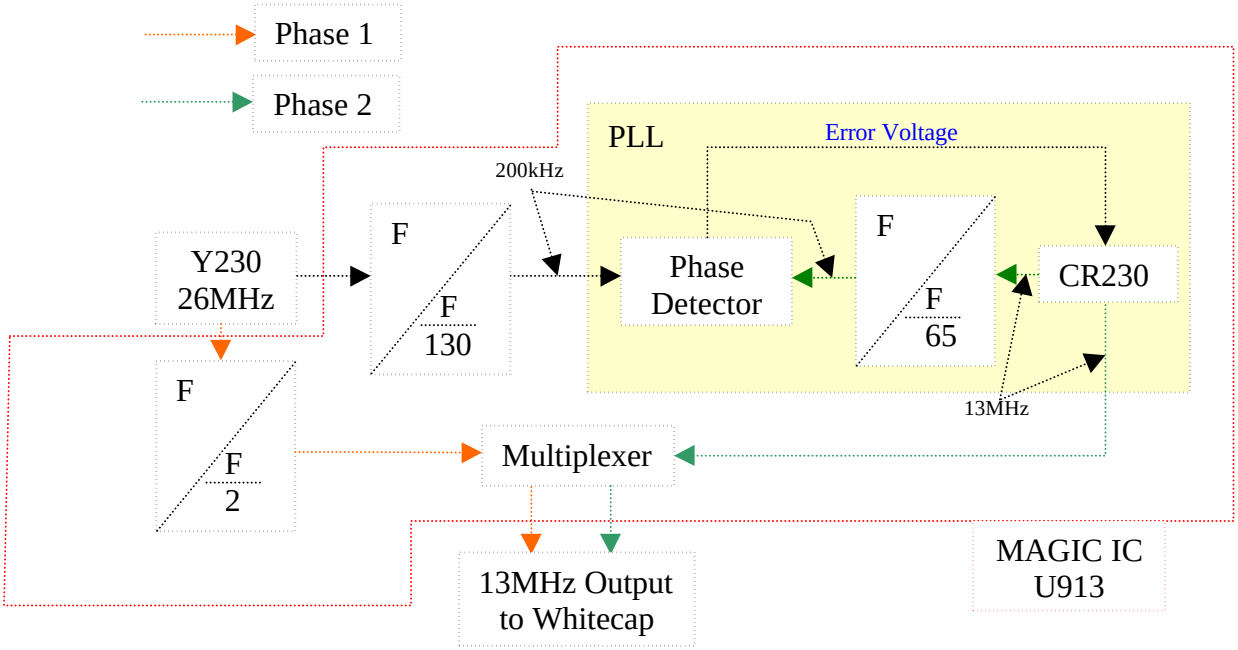
4) Once the power source has been selected to power the phone on the **PWR_SW** must be toggled low. This can be done by pressing the Power Key to create **PWR_SW**, which is supported by **ON+** (GCAP II **Pin C8**), or inserting an external power source into the Accessory Connector J600. Either way will drive **Pin G5 ON2+** low

5) The unit will then follow on as in the sequence below:



6) **13 MHz clock**. On Power Up there are 2 different reference clocks produced. Initially, as soon as power is applied to the MAGIC IC the crystal, Y200, supported by the **CRYSTAL_BASE** (MAGIC **Pin E1**) will emit a 26MHz signal to the MAGIC IC, which will internally be divided by 2 to give our external 13MHz clock. This is then fed out of the MAGIC on **Pin J6** (**CLK_OUT**) and distributed to Whitecap **Pin H10** (**CLKIN**), then from Whitecap to GCAP II **Pin F5** as **GCAP_CLK**. At the same time the 13MHz Varactor Diode CR248 is producing an output. This output is controlled in the following way: The 26MHz from Y230 is divided down to 200 kHz and fed to a phase comparator within the MAGIC. The 13MHz from CR230 is also divided down and fed in to the phase comparator, the difference in phase produces an error voltage that is fed onto the cathode of the Varactor CR230. Which regulates the output to a stable 13MHz clock. Once the software is running and the logic side of the board has successfully powered up, the **CLK_SELECT** signal from Whitecap **Pin 1** is fed to MAGIC **Pin G6**. This in turn

then switches the Multiplexer from the output of Y200 to the CR230 output. A high will switch to 13MHz.



Logic: SIM Card Interface

1) Once powered up, the SIM card is interrogated. The SIM interface is part of the Whitecap U800 and it supports both 'synchronous' (Prepay card) and asynchronous, serial data transmission, though the A008 is programmed only for asynchronous. **VSIM1** (**SIM_VCC**) is originally programmed to 3V but if the card is 5V then the SIM card will be powered down and **VSIM1** will be reprogrammed to 5V The Whitecap interprets that the card is 5V if after programming with 3V, it cannot read any data from the card. The signal levels for in and out of the SIM are now required to be level shifted within GCAP II U900 to 3V these signals are:

- **Reset** (Whitecap Pin E9 – **RST0**) in to GCAP II **Pin E9** – **LS1_IN_TG1A**. This signal is then level shifted to the required voltage and fed out to SIM Contacts J900 **Pin 4** from **Pin J7** - **LS1_OUT_TG1A**.
- **Clock**: This is a 3.25MHz signal from Whitecap – **CLK0 Pin E7** to GCAP II **Pin G6** – **LS2_IN**. This signal is then level shifted to the required voltage and fed out to SIM Contacts J900 **Pin 6** from **Pin F6** – **LS2_OUT**.
- **SIM I/O** – Data transmission to and from SIM card; for TX, from SIM card contact **SIM I/O Pin 5** through to GCAP II **Pin J8 SIM I/O**. Through level shifter to desired voltage and out through **Pin K10** (**LS3_TX_PA_B+**) to Whitecap **Pin F3 DAT0_TX**. For RX data from Whitecap **Pin B5 DATA0_RX** to GCAP II, **Pin H8** – **LS3_RX** where the signal is level shifted to desired voltage and outputted on Pin J8 **SIM I/O** to SIM contacts **Pin 5 SIM I/O**.
- **SIM_PD** – This signal is provided by the signal **THERM** (Batt Contact J610), or by **BATT+**. If there are no batteries present then the unit will display 'Insert Battery'. If batteries are present but the SIM card is either not inserted or faulty '! NO SIM CARD ' will be displayed. The reason behind this is to prevent the extra cost of a

mechanical SIM presence detect switch and to prevent the SIM card being removed whilst connected to Aux Power.

NB With no SIM card, Antenna Off can be selected and the unit can be used directly as an organiser without the use of the transceiver.

Logic: Charger Circuit

1) The charging operation is as follows:
2) After a charger has been detected **MAN_TEST_AD**, the Whitecap U700 will communicate with the device via **DSC_EN**.
3) **EXT B+** is fed in from Accessory Connector J600 **Pin 14** to the source of Q901, controlled by U9819,(these components are placed purely for high voltage protection), this voltage will then be passed back to the source of Q932, where the line **MOBPORTB** detects the presence of **EXT B+.** The current is sensed through R932 Current Sense Resistor, the voltage drop over it is sent to GCAP II **Pin D9 I_SENSE**, this is used to evaluate the charging current.
4) The charging current is then passed through CR932 to charge **BATT +**. The charge current is restricted by the signal **CHRGC** – GCAP II **Pin E8**, this opens the gate of Q635. **CHRGC** is programmed during charger phasing.
5) **CHRG_EN** Whitecap **Pin 1**, biases Q634 On or Off

Logic: Deep Sleep Mode

1) Deep sleep mode is there to provide a facility to save battery life by intermittently shutting off part of the PCB. This is achieved in the following way. The signal **STDBY** is generated from Whitecap **Pin F1**, and from here the signal is then passed onto Q960 and Q921. This has the effect respectively of:
2) Grounding **VREF** which makes MAGIC inoperable
3) Grounding **V2** This switches off MAGIC, and inhibits the Transmit path through **RF_V2**
4) Also the signal is passed through a standby delay using the logic gate U9820 and diode CR701 these provide a short delay between the de-activation of **V2** and **VREF** and the activation of **LS_V1**. Which will support the Down-link lines during sleep mode.
5) The shutdown is only for a fraction of a second and during that time the GCAP Clock supports the logic side of the unit. The GCAP clock is generated by Y900, which generates a 32.768MHz clock. This clock is output from Whitecap **Pin C7** and fed directly to Whitecap **Pin P4**. The clock is always monitored by Whitecap and should it fail, the unit will no longer go into deep sleep mode.

Logic: Keypad Operation

1) The keypad works as a matrix supported by V2. The signals inform the Whitecap upon a key press by dropping the signal 'low'. There are only 6 'hard' keys, these are:

PAGE UP – **KBR0**
PAGE DOWN – **KBR1**
HOME – **KBC0**
POWER – **PWR_SW**
VA – **KBC3**
JOG DIAL – **KBR2 / KBR3** for clockwise operation
KBC1 / GND for counter clockwise operation
KBR3 / KBR2 for push.

The jog dial can be used for most scrolling operations within the touch screen menu
HS_INT is used to detect the Flip being opened

PDA

Next to being a telephone the A6188 is a touch screen personal organiser. It incorporates many functions these being:

- Address book
- Recent call Log
- WAP Browser
- Voice recorder
- Calculator
- Currency Converter
- Measurement converter
- Instant Messaging
- Transfer Application
- Messaging Center
- Diary
- Memo pad
- Chinese / English Dictionary
- Games are available
- KJAVA
- Full Email functions
- Truesync PC ⟷ A6188 Data

Dragon Ball IC U2000

1) Dragon Ball is the processor that operates the running system of the display. The MC68EZ328 features a more flexible LCD controller with streamlined list of peripherals placed in a smaller package. This processor mainly targeted for portable consumer products, which require less peripheral and a more flexible LCD controller. By providing 3V, fully static operation in an efficient 100 TQFP package.

2) Static 68EC000 Core Processor

- 32-Bit internal address bus
- 24-Bit external address bus capable of addressing maximum 4 x 16MB blocks with chip selects 16-Bit on-chip data bus for MC68000 bus operations
- Static design allows processor clock to be stopped to provide power savings
- External M68000 Bus interface with selectable bus sizing for 8-bit and 16-bit data ports

3) System Integration Module (SIM28-EZ)

Related to External Array Logic, such as:

- System configuration, programmable address mapping
- Interface to SRAM, EPROM, FLASH memory
- 8 programmable chip selects with wait state generation logic
- 4 programmable interrupt I/O and with keyboard interrupt capability
- 5 general purpose, programmable edge/level/polarity interrupt IRQ
- Other programmable I/O, multiplexed with peripheral functions up to 47 parallel I/O
- Low-Power mode control

4) DRAM Controller

- Support 8 bit / 16 bit port DRAM
- Programmable refresh rate
- Support up to 2 banks of DRAM/EDO DRAM
- Programmable column address size

5) UART

- Support IrDA physical layer protocol up to 115.2kbps
- 8 Bytes FIFO on TX and 12 Bytes FIFO on RX

6) Serial Peripheral Interface Port

- 16 bit programmable SPI to support external peripherals
- Master mode support

7) 16-Bit General Purpose Counter / Timer

- Automatic interrupt generation
- 60-ns resolution at 16.58-MHz system clock
- Timer input/output pin

8) Real Time Clock / Sampling Timer

- Separate power supply for the RTC
- One programmable alarm
- Capable to count up to 512 days
- Sampling Timer with selectable frequency (4Hz, 8Hz, 16Hz, 32Hz, 64Hz, 256Hz, 512Hz, 1kHz). Generate interrupt for digitizer sampling, or keyboard debouncing.

9) LCD Controller

- Software programmable screen size (up to 640*512) to support single (Non-Split) monochrome/ colour STN panels
- Capable of direct driving popular LCD drivers/modules from Motorola, Sharp, Hitachi, Toshiba etc.

- Support up to 4 grey levels out of 16 palettes.
- Utilise system memory as display memory
- LCD contrast control using 8-bit PWM

10) Pulse Width Modulation (PWM) Module

- 8 bit resolution
- 5 Byte FIFO provide more flexibility on performance
- Sound and melody generation

11) Build-in Emulation Function

- Dedicated memory space for Emulator Debug Monitor with Chip Select

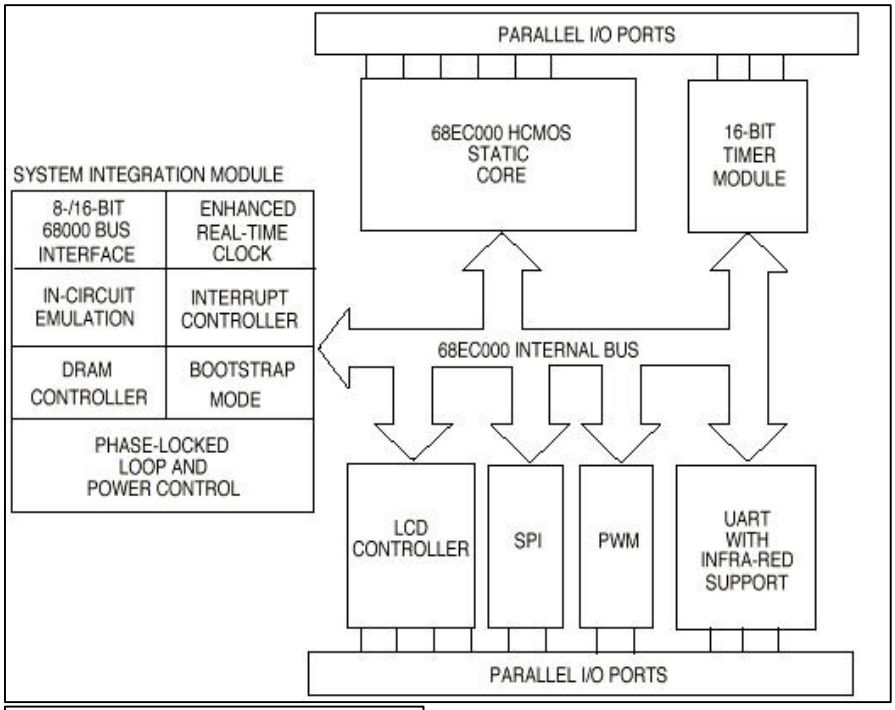
12) Boot Strap Mode Function

- Allow User to initialise system and download program/data to system memory through UART
- Accept execution command to run program stored in system memory

13) Power Management

- Fully static HCMOS technology
- Programmable clock synthesiser using 32.768 kHz/38.4 kHz crystal for full frequency control
- Low power stop capabilities
- Modules can be individually shut-down

- Operation from DC To 16.58 MHz (processor clock)
- Operating Voltage of 2.7V-3.3V
- 144 Pin Ball Grid Array (PBGA) packages



Dragon Ball Block Diagram

The touch screen is controlled in the following way See **Fig 1.**

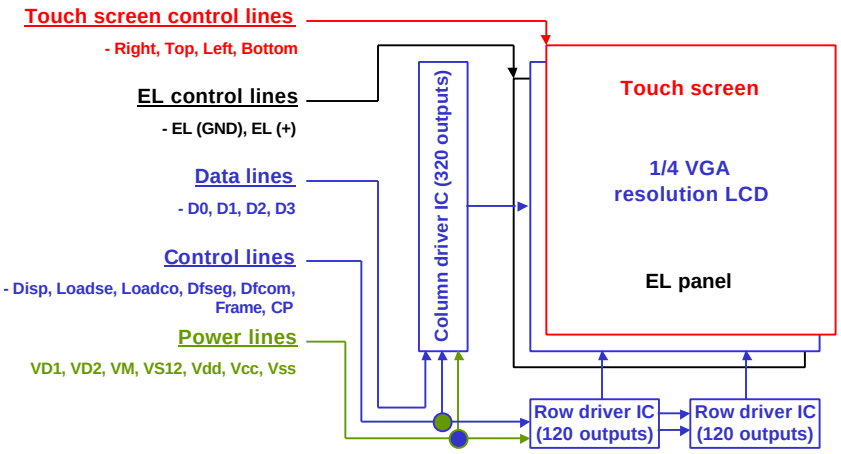


Fig.1 LCD module electrical block diagram

Each row and column, is in effect a long imaginary resistor with a +ve voltage at one end and a –ve or Grounded voltage level at the other. We can imagine that if these resistors could be overlapped then we can create a comprehensive resistor matrix. It is this matrix that provides us with the information of where the pen is placed on the touch screen. See **Fig 2** (Example values only)

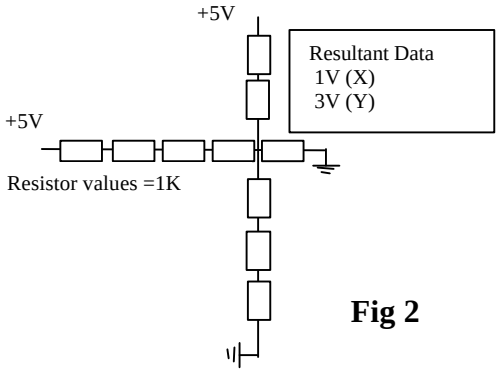


Fig 2

1) The row drivers / Control Lines **LOADCO** and **LOADCE** are originated from Dragon Ball **LLP** **Pin K8** (latches line of data J9805 where the signal becomes **LOAD_IN** before splitting to produce the 2 signals going to J9805 Pins **11** and **12**
DFSEG is originated from Dragon Ball **LACD** **PIN L7** (used to toggle the crystal polarisation) to J9805 where the signal becomes **DF_IN** changing again to **DFSEG** on J9805 **Pin 13**
LCDOFF* From Dragon Ball **Pin M2** (switches LCD On or Off – **NOT USED**)
FRAME – Used to indicate start of new frame
CP is originated from Dragon Ball **LCLK** **PIN M7** (synchronises display data) to J9805 **Pin 10**, where the signal becomes **CP**

2) Power Lines these consist of the following: These are all created in the LCD Module
VD1 – 3.3V to supply logic circuit of LCD Driver
VD2 – 3.0V to segment driver
VM – 1.5V to for comparator of segment driver
Vdd - +ve LCD Drive Voltage
Vcc – Internal Logic voltage of Com Driver IC
Vss – -ve LCD Driver Voltage

3) Contrast control is again controlled from within the LCD module using a resistive potential divider with the average room temperature contrast voltage being 12.5V.

4) The Data bus is a 4-line bus that is used to transfer pixel information to the LCD. They are **D0– D3**. These lines connect between Dragon Ball U2000 **Pins J10, M9, L9 & K9** and J9805 **Pins 6,7,8,9** respectively.

5) The EL panel within the LCD requires a LCD AC voltage to correctly orientate the liquid crystal. This is provide using a DC- AC Converter U9824. The DC to AC converter samples the DC input before separating it into small elements that will make up a sinusoidal waveform, this waveform is then stepped up to the appropriate voltage using a transformer (L9800). The input is controlled by the signal backlight and supported by **PDA_VCC** the resultant output will be a 100V amplitude sine wave, **EL+** see **Fig 3**

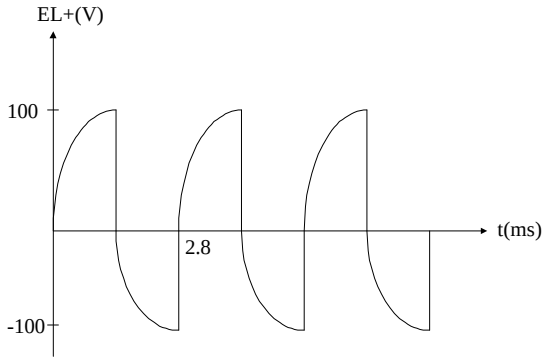
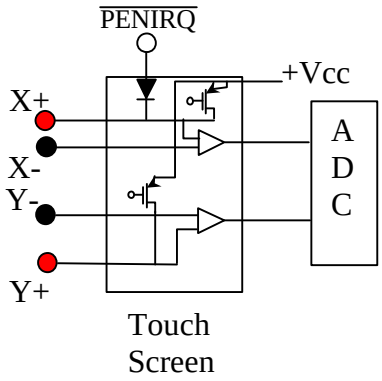


Fig 3 EL+ Driving Signal

6) This signal **EL+** is then fed to J9805 **Pin 23**

7) When the screen is touched as was discussed earlier the voltage matrix will be converted to a 12-bit word (Interrupt Request).



8) The analogue signal is fed from the LCD PCB as **RIGHT / TOP / LEFT / BOTTOM** on J9805 **Pins 1,2, 3 & 4** respectively and is fed to the ADC converter on **Pins 2, 3,4& 5.** This data is then relayed to and from Dragon Ball on **SPM_TXD** and **SPM_RXD.** The ADC is supported by **PDA_VCC.**

Logic: Communication

1) There are several ways by which the A008 can transmit and receive data; these are as follows.
   - Communication between the Whitecap and the Dragon ball, is carried on 6 lines, these are **U_CTS / U_RTX / URXD / UTXD / WD_INT* & DW_INT***.
   - When W/CAP need to send data to Dragon ball, it will send an interrupt signal to Dragon ball through **WD_INT*.** Dragon ball will response by clear **U_CTS**, then data will be send to Dragon ball over the UART port. If Dragon ball need to send data to W/CAP, it will send an interrupt to W/CAP through **DW_INT*.** The communication is the same.

2) Communication between Whitecap and GCAP uses the following lines of communication **– DR2 / DX2 / MQSPI_CLK2 / MQSPI – CS0**
   - Where **DR2** is data transfer from GCAP to Whitecap
   - Where **DX2** is data transfer from Whitecap to GCAP
   - **MQSPI_CLK2** is the data transfer clock
   - **MQSPI_CS0** is the select line for **DR2 / DX2**

3) For programming i.e. flashing the phone, we use the flow matrix consisting of U9821 / U9822 and U2601. Basic function being.
   - U9822 and U9821 are inverter and non inverting devices respectively
   - **PB2** (Whitecap **Pin L2**) is sent to the input of U9822 and also output as **A** to U9821is used to decide whether information is sent from External Connector to Whitecap or to Dragon Ball
   - The signals **CTS2*** and **RTS2*** (Dragon Ball **Pins F4 and F3**) control data flow and data can either be sent from either processor to External connector on the

UPLINK / GCAP UPLINK lines or for example Flash Information can be programmed into either Processor using **DOWNLINK / GCAP_DOWNLINK**.

4) IrDA – The IrDA transceiver module is U9812. The IrDA data takes the form of an SIP (Serial Infrared Pulse) with **SD_IrDA** being an active high signal that turns the LED on. The received signal **IrDA RXD** is always a pulsed, active low 2.4µs pulse, and a low will light the LED. The data for TX is sent to **IRDA_TXD** U9812 **Pin 7** from Dragon Ball as **TXD2** **Pin E4**. For **IRDA_RXD**, information received is passed from U9812 to Dragon Ball as **RXD2** **Pin E3**