A1200 Bolck Diagram Signal Description

1	ACC_ID	U901	U900	ACCesory IDendification from EMU IC to Pcap AD converter input
2	ALERTM_PAD	U900	Alert contact pad	ALERT Out Negatve (Minus) from Alert amplifier to Alert speaker pad
3	ALERTP_PAD	U900	Alert contact pad	ALERT Out Positive (Plus)from Alert amplifier to Alert speaker pad
4	ANT_DETB	J100	U800	Antenna Detect low active indication for an extern connected antenna
5	AP_CLK_RQST	U2000	U911	Application Processor to PCAP Sleep ReQueST
6	AP_CORE	U900	U2000	Aplication Processor CORE 1,2V supply
7	AP_IO_REG	U900	Q990,U300,U800...	generic 2,775V supply Voltage for the Base Band section
8	AP_PCAP_INT	U900	U2000	PCAP to Application Processor control SPI Bus - INTerupt
9	AP_READY	U2000	U800	APplication Processor Handskake signal to Baseband Processor
10	AP_SAP_CLK	U900	U2000	PCAP to Application Processor Serial Audio Peripherie SPI Data Bus - CLocK
11	AP_SAP_FS	U900	U2000	PCAP to Application Processor Serial Audio Peripherie SPI Data Bus - Frame Sync
12	AP_SAP_TX	U2000	U900	Application Processor to PCAP Serial Audio Peripherie SPI Data Bus - Transmit (X) Data
13	AP_SLEEP_RQST	U911	U900	inverted AP_CLK_RQST
14	AP_SPI_CLK	U2000	U900	Application Processor to PCAP control SPI Bus - CLocK
15	AP_SPI_CS	U2000	U900	Application Processor to PCAP control SPI Bus - Chip Select
16	AP_SPI_MISO	U900	U2000	PCAP to Application Processor control SPI Bus - Master Input - Slave Output
17	AP_SPI_MOSI	U2000	U900	Application Processor to PCAP control SPI Bus - Master Output - Slave Input
18	AP_WDOG	U2000	U900	Application Processor to PCAP WatchDOG - forces system to power down in fail mode
19	AUD_REG	U900	U900	AUDio 2,775V support voltage for U900 internal functions
20	AUDIO_IN	U901	U900	External AUDIO INput from J904 via EMU IC interface
21	AUDIO_REG	U900	U500	2,775V AUDio REGulator output to FM Chipset
22	BATTFET	U901	Q902	Enables / Disables Battery BATT + FET- Switch to support B+ as Main source for the device with Battery power
23	BATTI	R910	U900	AD converter input to PCap to mesure the votage drop over R910 as Current flow indicator of charge mode
24	BATTP	M901	R921, U900	BATTery (Plus) output/input to Battery switch Q902 and U900 AD converter input
25	BATTP	M901	U900	AD converter input to PCap to mesure the Battery voltage level
26	BB_IO_REG	U900	U800, U804, U809...	Generic BaseBand REGulator output 2,775V to supply different BaseBand chipsets
27	BB_SAP_CLK	U900	U300, U800, U2000	Base Band Serial Audio Port CLocK to Clock Audio Data Flow (Audio SPI Bus)
28	BB_SAP_FS	U900	U300, U800, U2000	Base Band Serial Audio Port Frame Synchronisation to syncronize the Audio Frames (Audio SPI Bus)
29	BB_SAP_RX	U300, U900, U2000	U800	Base Band Serial Audio Port Receive signal to U800 (Audio SPI Bus)
30	BB_SAP_TX	U800	U300, U900, U2000	Base Band Serial Audio Port Transmitt signal to U900 and U300.... (Audio SPI Bus)
31	BB_SLEEP_RQST	U803	U900	SLEEP ReQeST from Base Band Processor on 2,775 V Level, to request Sleep mode Operation from PCAP
32	BB_SLEEP_RQST_1_5V	U800	U803	SLEEP ReQeST from Base Band Processor on 1,5 V Level, to request Sleep mode Operation from PCAP and BB 26MHz Clock circuit
33	BB_SPI_CLK	U800	U900	BaseBand SPI Bus CLocK to Clock Data Flow (Neptune /PCAP Control Communication)
34	BB_SPI_MISO	U900	U800	BaseBand SPI Bus Master (U800) Input, Slave (U900) Output (Neptune /PCAP Control Communication)
35	BB_SPI_MOSI	U800	U900	BaseBand SPI Bus Master (U800) Output, Slave (U900) Input (Neptune /PCAP Control Communication)
36	BB_WDOG	U800	U2000	WatchDOG- active low signal to U2000 to drive power down of the unit
37	BLK_PWM	U2000	U404	BacKLight PoWer enable signal
38	BLUE_HOST_WAKEB	U300	U2000	Communication WAKEup signal from U300 to U2000
39	BLUE_WAKEB	U2000	U300	Communication WAKEup signal from U2000 to U300
40	BLUE1_CATHODE	U401	J402	BLUE LED1 CATHODE connection from U401 Funlight Driver

41	BLUE2_CATHODE	U401	J402	BLUE LED2 CATHODE connection from U401 Funlight Driver
42	BP_FET	U901	Q903	OverVoltage control interface output to Enable / Disable BATT+ Switch to support B+ as Main source for the device with external power
43	BP_FLASH_MODE_EN	U2000	U800	ENables BaseBand Processor FLASH MODE
44	BP_OPT1	U800	U809	if line is shorted with BP_OPT2, Neptune is forced into Flash Mode operation
45	BP_OPT2	U809	U800	if line is shorted with BP_OPT1, Neptune is forced into Flash Mode operation
46	BP_READY	U800	U2000	Baseband Processor Handskake signal Application Processor
47	BP_RESETB	U2000	U801 / U800	active low (B) system RESET from Application Processor to Baseband Processor Neptune
48	BPLUS	U900	U900, U150,....	Main Source for the Phone supporting U900 power supply and power support for U150, U404, Q801 and Q990
49	BT_ANTENNA	BT Antenna Pad	FL301	BlueTooth ANTENNA input
50	BT_CTS	U300	U2000	BlueTooth Clear To Send Data indication to Application Processor (InterChip Communication)
51	BT_NRESET	U2000	U301	BlueTooth Active Low (N) RESET to BT Chipset
52	BT_RF_REG	Q901	U300	2,775 Volt regulator output from PCap (via Q901 pass device) to support the BT Chipset U300
53	BT_RTS	U2000	U300	BlueTooth Request To Send Indication from Application Proccesor
54	BT_RXD	U300	U2000	Receive (X) Data Communication from BlueTooth chipset
55	BT_TXD	U2000	U300	Transmitt (X) Data Communication to BlueTooth chipset
56	BUL_VCC_BATT	AP_IO_REG	U2000	2,775V Power supply to BUL verde
57	BUL_VCC_BB	AP_IO_REG	U2000	2,775V Power supply to BUL verde
58	BUL_VCC_IO	AP_IO_REG	U2000	2,775V Power supply to BUL verde
59	BUL_VCC_LCD	VBUCK	U2000	1,875V Power supply to BUL verde
60	BUL_VCC_MEM	VBUCK	U2000	1,875V Power supply to BUL verde
61	BURSTCLK	U800	U805	BURST CLocK to clock U805 to syncronize the loading of addresses and delivery of burst read data
62	CAM_CLK_IN	U1301	J403	CAMera CLlocK INput, operation clock for camera circuit
63	CAM_CLK_OUT	J403	U405	Pixel CLocK from CAMera OUTput to U405 AND Gate
64	CAM_DATA(0 - 7)	J403	U2000	CAMera Data Bus to Graphic Interface of U2000
65	CAM_EN	U2000	J403	CAMera ENable from U2000 to power on the Camera
66	CAM_HSYNC	J403	U2000	CAMera Horizontal SYNChronization
67	CAM_PCLK_GATE	U405	U2000	Pixel CLocK from U405 GATE output to Application Processor if CAM_HSYNC and CAM_CLK_OUT available and syncronized
68	CAM_VSYNC	J403	U2000	CAMera Vertical SYNChronization
69	CELL_RX_50	U150	U100	850 MHZ (PCS) RX Antenna signal on 50 OHm level
70	CHARGER_INPUT	R967	Q905	CHARGER transistor INPUT, source is VBUS from the Mini USB connector
71	CLK 13MHZ_1_8V	U800	U900	13 MHz Core CLocK to Pcap on a 1,8V level
72	CLK_32KHZ	U900	U500, U2006	32KHZ CLocK output to U500 and U2006 (Level Shifter)
73	CLK_32KHZ_1_5V	U2006	U2000, U300,U800	32Khz CLocK 1,5V level shifted to support the Aplication Processor, Bluetooth and Neptune
74	CLKR	U150	U800	Voice Band Data Bus CLocK Receive signal from U150 to U800
75	CNTRL1	U100	U150	CoNTRoL signal to PA to select the Antenna Switch (see Martix on Block Diagram
76	CNTRL2	U100	U150	CoNTRoL signal to PA to select the Antenna Switch (see Martix on Block Diagram
77	CNTRL3	U100	U150	CoNTRoL signal to PA to select the Antenna Switch (see Martix on Block Diagram
78	CS0B	U800	U805	Chip Select 0 - active low output is used as external Flash Memory chip select
79	CS1B	U800	U805	Chip Select 1 - active low output is used as external Flash Memory chip select
80	DCS_RX_50	U150	U100	1800 MHZ (PCS) RX Antenna signal on 50 OHm level
81	DM_TXD	J904, U901	U901, J904	bidirectional Data Minus USB input (USB-) also used as Audio output from hedsets or other audio devices

82	DP_RXD	J904, U901	U901, J904	bidirectional Data Positive USB input (USB+) also used as Audio input /output to/ from hedsets or other audio devices
83	DQM0	U2000	U2001	used to select the SDRAM Data input Masks Data (0-7)
84	DQM1	U2000	U2001	used to select the SDRAM Data input Masks Data (8-15)
85	DRI	U150	U800	Voice Band Data Bus Data Receive Input signal from U150 to U800
86	EB0_B	U800	U805	Used as write Enable to partition of SRAM
87	EB1_B	U800	U805	Used as write Enable to partition of SRAM
88	ECBB	U800	U805	End Off Curret Burst-active low(B)- to indicate to FLASH the end of current burst sequence.
89	EMU_INT	U901	U2000	INTerupt signal to Application Processor fromEnhanced Mini USB Chip
90	EMU_PWR_ON	U901	U900	External (EMU) PoWeR indication to PCAP
91	EMU_USB_SE0	U2000	U901	USB (Minus) OUT data to EMU IC
92	EMU_USB_TX_ENB	U2000	U901	USB Transmit (X) ENable- active low (B) - signals to EMU IC when to transmit data on USB bus
93	EMU_USB_VMIN_RXD	U901	U2000	USB (Minus) IN data communication to Application Processor fomEMU IC
94	EMU_USB_VPIN	U901	U2000	USB (Positive) IN data communication to Application Processor fomEMU IC
95	EMU_USB_VPOUT_TXD	U2000	U901	USB (Positive) OUT data to EMU IC
96	EMU_USB_XRXD	U901	U2000	CMOS logic value of value received from USB wires
97	ENR	U150	U800	ENable Receive signal from U150 to U800
98	FLIP_INT	U2005	U2000	FLIP open/ close INTerupt signal to Application Processor
99	FM_ANT_IN	J902	U500	FM Radio ANTennea INput to FM chipset
100	FM_INT	U500	U2000	INTerupt signal to Application Processor fromFM Chip
101	FM_VCCA	AUD_REG	U500	VCC Power supply toFM Chip
102	FM_VCCD	AP_IO_REG	U500	VCC Power supply toFM Chip
103	FSR	U150	U800	Voice Band Data Bus Frame Syncronisation Receive signal from U150 to U800
104	GND	PCB	PCB	GrouND connection
105	GREEN1_CATHODE	U401	J402	GREEN LED1 CATHODE connection from U401 Funlight Driver
106	GREEN2_CATHODE	U401	J402	GREEN LED2 CATHODE connection from U401 Funlight Driver
107	GSM_RX_50	U150	U100	900 MHZ (PCS) RX Antenna signal on50 OHm level
108	HAND_SPKRM	U900	FL902, J402	Audio amplifier output (Minus) to Flip connector to support the EarpeaceSPeaKeR through FL1200
109	HAND_SPKRP	U900	FL902, J402	Audio amplifier output (Plus) to Flip connector to support the EarpeaceSPeaKeR through FL1200
110	HB_TX_OUT	U100	U150	TX High frequency Band OUTput to PA
111	HJACK_DET	J902	U900	DETect signal of the insertion of a Headset into theHeadset JACK
112	HJACK_MIC	J902	U900	Headset JACK MICrophone signal line
113	HJACK_SPKR_L	U900	FL901	Headset JACK SPeaKeR Left channel audio signal
114	HJACK_SPKR_R	U900	FL901	Headset JACK SPeaKeR Right channel audio signal
115	HS_SPKR_L	U900	FL901	HeadSet SPeaKeR Left channel audio signal
116	HS_SPKR_R	U900	FL901	HeadSet SPeaKeR Right channel audio signal
117	I2C_ADDRESS	AP_IO_REG	U901	Floated I2C ADDRESS input line of U901
118	I2C_RESET	U2000	J403	Inter IC_Bus RESET signal
119	I2C_SCL	U2000	J403, U901,U401...	Inter IC_Bus Serial CLocK signal
120	I2C_SDA	U2000	J403, U901,U401...	Inter IC_Bus Serial DATA signal
121	INT_MICP	L909	U900	analog INTernal MICrophone Positive signal as input to microphone amplifier
122	ISENSE	R901	U901	Charge Current (I) SENSE to U901

123	ISENSE	U150	U800	used as PA detect signal to Neptune
124	KBC0-1	U2000	Keypad	Keypad (Board) Colum Strobe
125	KBR0-7	Keypad	U2000	Keypad (Board) Row Sense
126	LB_TX_OUT	U100	U150	TX Low frequency Band OUTput to PA
127	LBAB	U800	U805	Load Burst Address active low- causing that U805 is loading a new starting burst address
128	LCD_CM	U2000	J400	used to control the Color Mode of the LCD display - when it is high, it displays in 8-color (not in A1200), in low, it displays in 262k colors
129	LCD_HSYNC	U2000	J400	LCD Horizontal SYNCronisation
130	LCD_ID0	J400	U2000	Indicades in combination with LCD_ID1 the Display vendor ID (logic low means TMD vendor, logic high means TOPPOLY vendor)
131	LCD_MCLK	U2000	J400	Pixel CLOCK to Display -syncronized with V/ HSYNC
132	LCD_OE	U2000	J400	indicates Output Enable to the display - means a logig high will let data pass into the display
133	LCD_SD	U2000	J400	used to Shut Down the LCD display when phone is in sleep mode
134	LCD_VSYNC	U2000	J400	LCD Vertical SYNCronisation
135	LCDID1	J400	U2000	Indicades in combination with LCD_ID0 the Display vendor ID (in A1200 design it is always logic low)
136	LCELL_BYP	U800,C805-C808	C805-C808, U800	Lithium CELL BYPass Capacitor voltage
137	LCELL_BYP	U900	C962, C963	RTC Battery (Lithium CELL) BYPass Capacitor input/ output
138	LDD1-LDD17	U2000	J400	LCD Display Data line 1-17
139	LED-	U404	J400	negative (-)connection of the LED Backlight Constand Current Power supply
140	LED+	D101	J400	positive (+)connection of the LED Backlight Constand Current Power supply
141	LICELL	U900,BT900	BT900, U900	RTC Battery (Lithium CELL) used to support the RTC interface and the Memory Hold circuit
142	MCLK	U800	U100	Digital Modulation SPI BusCLocK
143	MDI	U800	U100	Digital Modulation SPI BusData Input line
144	MIC_BIAS1	U900	Int Mic Audio Line	BIAS Voltage output to support the internal MIC Audio line
145	MIC_BIAS2	U900	Mic Audio Line	BIAS Voltage output to support the Headset Jack MIC Audio line
146	MMC_CLK	U2000	M2001	Multi Media Card CLocK
147	MMC_CMD	U2000	M2001	Multi Media Card CoMmanD line
148	MMC_D0 - MMC_D3	M2001, U2000	U2000, M2001	bidirectional Multi Media Card Data lines
149	MMEDIA_13MHz	U2000	U900	13 MHZ Master CLocK to Pcap from the Aplication (MEDIA) Processor in Airplane mode
150	MS	U800	U100	Digital Modulation SPI Bus ReSet
151	NCS0	U2000	U2001	FLASH Chip Enable active low selects the Flash memory
152	NEP_AVDD	U900	U800	1,875V supply to support Neptune
153	NEP_ICL_SE0	U800	U2000	NEPtune Bulverde USBinter IC controL Bus - negative USB wire (USB-) to Application Processor
154	NEP_ICL_TXENB	U800	U2000	NEPtune Bulverde USBinter IC controL Bus Transmit (X) ENable - active low (B)
155	NEP_ICL_VMIN	U2000	U800	NEPtune Bulverde USBinter IC controL Bus - negative USB wire (USB-) to BaseBand Processor
156	NEP_ICL_VPIN	U2000	U800	NEPtune Bulverde USBinter IC controL Bus - positive USB wire (USB+) to BaseBand Processor
157	NEP_ICL_VPOUT	U800	U2000	NEPtune Bulverde USBinter IC controL Bus - positive USB wire (USB+) to Application Processor
158	NEP_ICL_XRXD	U2000	U800	CMOS logic value of value received from USB wires
159	NEP_QVDD	U900	U800	1,875V supply to support Neptune
160	NEP_RESET_INB	U801	U800	System RESET to NEPtune Input - active low (B)
161	NOE	U2000	U2001	active low (N) Flash Output Enable - used to enable the output drivers of the selected die
162	NRESET_OUT	U2000	U2001	active low (N) Flash RESET - resets internal operations
163	NSDCAS	U2000	U2001	used to define, at the positive rising edge of the clock, the command to be executed by the SDRAM_LDQM & SDRAM_UDQM

164	NSDCS0	U2000	U2001	active low (N) SDRAM CS for the 32MB part
165	NSDCS3	U2000	U2001	active low (N) SDRAM CS for the 16MB part
166	NSDRAS	U2000	U2001	used to define, at the positive rising edge of the clock, the command to be executed by the SDRAM_LDQM & SDRAM_UDQM
167	NWE	U2000	U2001	active low (N) Flash Write Enable - selects the associated memory die for write operation
168	OEB	U800	U805	Output Enable-active low (B)- is indicating that the bus access is a read and enables slave devicesto drive the bus with read data.
169	OSCM	U804	U100	26 MHz BaseBand OSCillator Clock Enable signal
170	OSCO_F	U100	U800	OSCillator Output Frequency (26MHz Clock) to Neptune
171	OWB	M901	U800	One Wire Bus signal line from Battery EEProm to Neptune. Used to download Battery Recharge information to Neptune
172	PCAP_BP	Q990	U900	Battery (Plus) input to PCAP - enabled by AP_IO_REG
173	PCAP_CS	U800	U900	BaseBand SPI Bus Chip Select from U800 to PCAP (Neptune /Atlas Control Communication)
174	PCAP_INT	U900	U800	INTerupt from PCAP to U800 indicate the end of conversation on Communication Bus
175	PCAP_MCU_RESETB	U900	U901, U2000	System RESET from PCAP
176	PCS_RX_50	U150	U100	1900 MHZ (PCS) RX Antenna signal on50 OHm level
177	PCUTS_VCC	U900	Q907	Power CUTS VCC supply to avoid power lost at Memory IC´s during mechanical shocks to the device (Source of VCC_STACKED_MEM)
178	POWER_FAIL	U900	U910	Batterie POWER_FAIL detect to Application Processor
179	POWER_FAIL_N	U910	U200	invertet (N) Batterie POWER_FAIL detect to Application Processor
180	PRIME_DIG	U900	U100	VCC from AP_IO_REG source to support the U100 Tranceiver IC
181	PWR_SW	M903	U900	PoWeR ON/Off SWitch signal to PCAP
182	Q904_5_EN	Q901	Q904, Q905	Charge transistor control -current flow control
183	R_WB	U800	U805	Read Write, active low in Write. Indicates the bus acces type.
184	RAMP	U800	U50	Bias control signal to U150 TX Power Amplifier (RAMP up Power)
185	RED1_CATHODE	U401	J402	RED LED1 CATHODE connection from U401 Funlight Driver
186	RED2_CATHODE	U401	J402	RED LED2 CATHODE connection from U401 Funlight Driver
187	REF_REG	U900	U800	REFerence REGulator Supply only for internal Pcap use 1,575V and Neptune
188	RESET_OUT	U800	U805	RESET from Neptune for U805
189	RESETB	U900	U801	active low (B) system RESET for U901 and Neptune
190	RF_CLK	U800	U100	SPI CLocK output to U100(RF Interface)
191	RF_CS	U800	U100	SPI Chip Select output to U100 (RF Interface)
192	RF_DATA	U800	U100	SPI Serial DATA to U100 (RF Interface)
193	RF_REG	U900	U100	2,775 Supply for Synthesyzer, super filterREGulators , RF and analog functions
194	RFIO	FL301	U300	Bluetooth RF Antenna In /Output
195	RX_ANT_EN	U800	U100	Receive ENable indication to U100
196	SDCKE	U2000	U2001	Enables/ activates the SDRAM ClocK when logig high level, thereby initiateseither the Power Down mode, Suspend mode or the Self Refresh mode
197	SDCLK0	U2000	U2001	CLocK for the Flash part of the stacked memory chip
198	SDCLK2	U2000	U2001	CLocK for the lower SDRAM partition
199	SDCLK3	U2000	U2001	CLocK for the upper SDRAM partition
200	**Signal**	**From**	**To**	**Description**
201	SIM_CLK	U800	M800	output CLocK from Sim Card Interface to SIM Card
202	SIM_DIO	U800/M800	M800/U800	Data In and Output from and to SIM Card / Interface
203	SIM_PD	U900	U800	SIM Presence Detect signals the insertion or removel of Phone Battrey to Neptune organated by BATT_DETB output from PCAP
204	SIM_REG	U900	U800/ J1403	SIM Card support voltage VCC 1.8 or 3V from Atlas

205	SIM_RST	U900	M800	active low ReSeT signal from SIM interface
206	SOL	U901	Q925	Sign Of Live enable output to support a live indication if charger is connected (Display on)
207	ST_REF	U900	HJACK_DET	Bias Voltage to HJACK_DET
208	SYS_RESTART	U2000	U900	SYStem RESTART control signal to PCAP2 from Bulverde - Active 100ms pulse
209	THERM	M901	U900	Analog Referece voltage Biased by THERM_BIAS to Indicate the Battery Temperature to Pcap Charger Interface.
210	THERMBIAS	U900	M901	Analog Bias Votage to Thermistor line from Battery
211	TSX1	U900	VR400	Touch Screen X axis Signal1 to PCAP Touch screen interface
212	TSX2	U900	VR400	Touch Screen X axis Signal2 to PCAP Touch screen interface
213	TSY1	VR400	U900	Touch Screen Y axis Signal1 to PCAP Touch screen interface
214	TSY2	VR400	U900	Touch Screen Y axis Signal2 to PCAP Touch screen interface
215	TX_EN	U100	U150	TX ENable is enabling the TX signal path in U150
216	TX_START	U800	U100, U900	Transmit Enable (START) indication to U100 Frontend , VCO´s and PCAP Regulators
217	UID	J904	VR902-U901	USB Device IDentification - a pull down resistor in the connected USB device is used as identification
218	USB_PWR	J904	CR906, R967	Power source from USB Charger input
219	USB_READY	U2000	U901	USB Enable (READY) to U901 to start USB communication
220	V_BUCK	U900	J400, J403, U2000..	1,875 V Buck Mode supply Voltage for the Base Band section
221	VBOOST	U900	U800, U900, J402	5,6 Volt regulator output of PCAP to support PCAP internal Interface, U2000, J402
222	VBOOST_EMU	VBOOST	U901	Power source (VBOOST) from PCAP to Enhanced Mini USB IC
223	VBOOST_FLIP	VBOOST	J902	5,6 V Power source (VBOOST) to Flip Connector
224	VBUS	R967	U901	External Power sense input to U901
225	VCC_NEP_MEM	VBUCK	U805	see VBUCK description
226	VCC_PLL	U900	U2000	1,275V VCC Power supply for the Aplication Processor
227	VCC_SRAM	U900	U2000	1,275V VCC Power supply for the Aplication Processor
228	VCC_STACKED_MEM	Q907	U2001	1,8V VCC Power supply for theU2001 STACKED MEMory IC
229	VCC_TRANSFLASH	U900	M2001	2,8V VCC Power supply for theTRANSFLASH Card Reader
230	VCO_REF	U900	U100	2,775V Voltage Controled Ocillator REGulator supply for U100
231	VDDA	U900	U800	2,775V supply to support Neptune
232	VHOLD_EXT_EN	U900	Q907	ENable signal to Q907
233	VIB_REG	U900	Vibrator Motor	VIBrator REGulator OUTput to vibrator motor contacts
234	VSIM	U900	U800, M800	1,8V/ 3V Supply for NeptuneSIM interface and Sim Card
235	VSIM_EN	U800	U900	ENable signal from Neptune to Seaweed for theSIM VCC regulator