Service Manual

Level 3

Draft 1.0

MOTOROLA™

DIGITAL WIRELESS TELEPHONE

Model A1000

UMTS 2100MHz/PCS 1900MHz/DCS 1800MHz/GSM 900MHz

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3G Flash Procedures

Introduction

This document is intended to describe the flashing (firmware upgrade) procedures for 3G terminals. The 3G terminal described in this document will be limited to the A1000.

Firmware upgrades need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the firmware upgrade application database is up-to-date.

Firmware upgrades allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific circumstances, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the 3G terminal.

Power Hardware

1. Fully Charged battery (SNN5697)

2. Full-rate Charger (SPN5049)

Interface Options

1. USB Data Kit (S8951)
   USB Cable (SKN6311A)
   Data Software CD

Software Requirements

The RSD (Remote Software Download) General Release is used to allow functions such as firmware upgrade, Phone Swap, and Multi-refurbish. Contact your local Motorola service representative to receive download information for the RSD and related support files. Also insure that the RSD database has the latest update.

Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1-1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a nonfunctional (Bricked) 3G terminal.

The A1000 contains Flash EPROMs for the Application Processor (AP) and Baseband Processor (BP). The firmware upgrade software will contain AP and BP firmware integrated as a One File Flash (1FF) solution.

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery
2. Full-Rate Charger w/battery (recommended)

If the user decides on using the battery only solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the flash process. This action may cause unrecoverable failures to the 3G terminal.

RSD Firmware Upgrade Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal.

1. Launch the RSD General application
2. Connect the unit as illustrated in figure 1-1.
3. Power up the 3G terminal
4. If the 3G terminal doesn't power up, refer to the Force Flash section.
5. Once the phone is fully powered up, the Radio Information Panel will be updated.
7. In the Utilities Panel, select Firmware Upgrade.
8. In the Main information Panel, select desired restore and logging options
9. In the Main information Panel, click on the Start button to begin Firmware upgrade.

NOTE: DO NOT interrupt any hardware connections during the flash process. Connection interruptions may cause the flashing process to fail and render the 3G terminal non-operational.

10. When the process is complete, the Main Information Panel will indicate whether the process was successful. At this time you may safely disconnect the 3G terminal.
11. Power up the 3G terminal to insure that the flash procedure was successful.

Figure 1-1. RSD Hardware Configuration

Figure 1-2. RSD General Release GUI

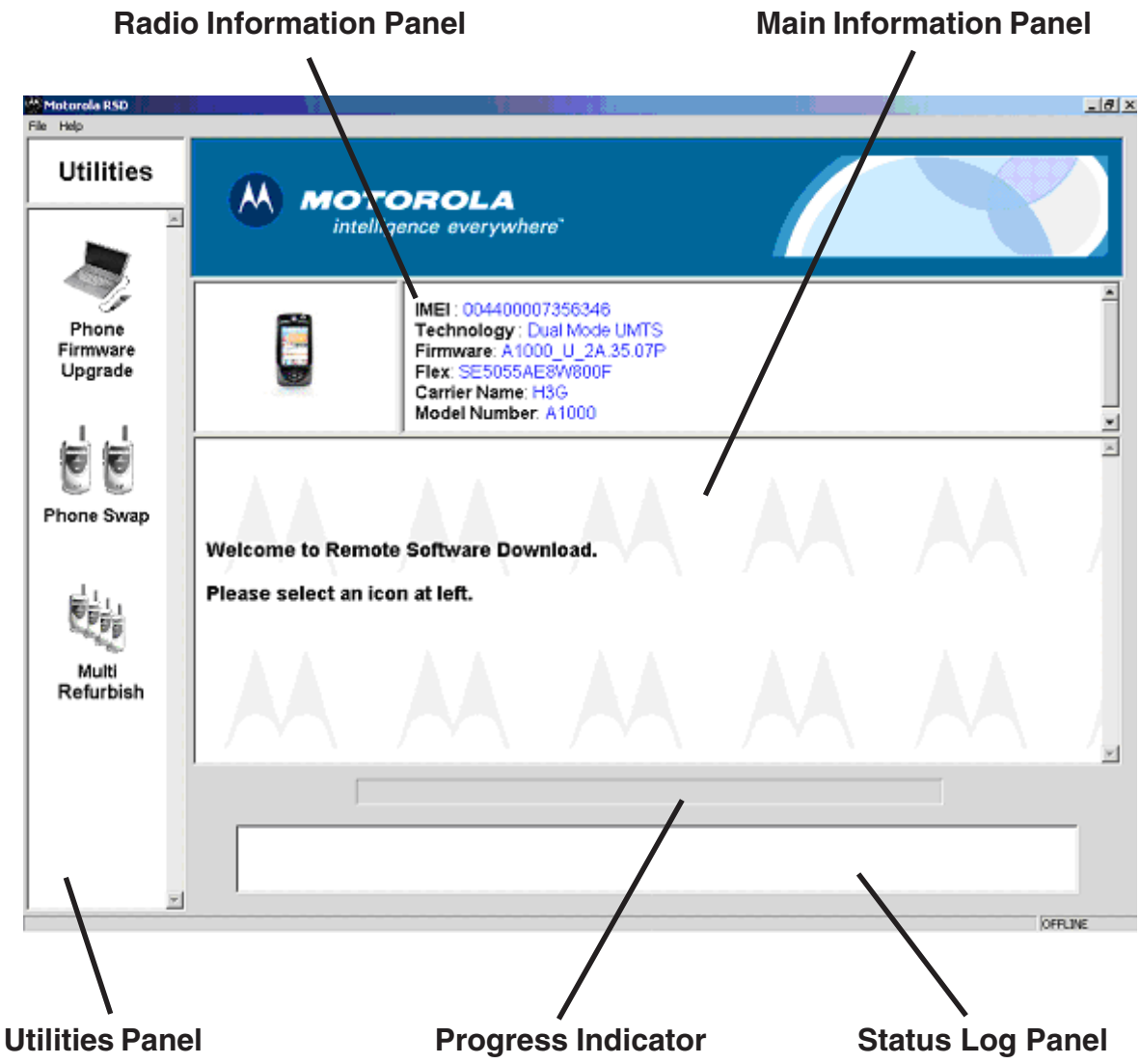
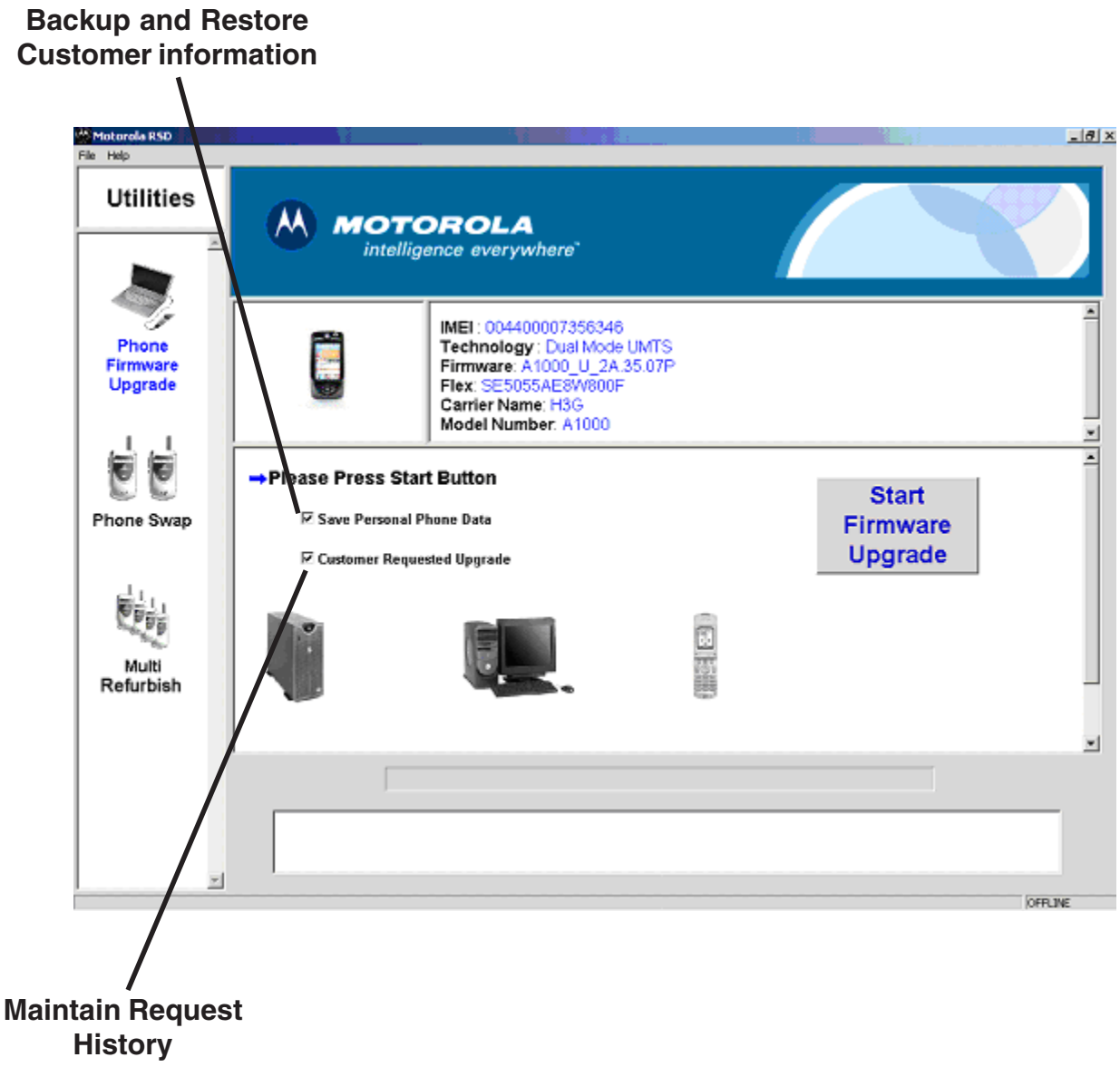


Figure 1-3. Firmware Upgrade



Force Flash Procedures

The procedures described in this section apply only to situations where the 3G terminal will not initiate it's normal power up sequence, but may recover functionality by a repeat flash procedure.

There are two possible alternatives to place the 3G terminal in force flash mode.

Key Hold Solution

Hardware: Refer to Figure 1 (USB solution)

Step 1. Remove the battery from the 3G terminal

Step 2. Prior to connecting the USB cable, press and hold both gaming keys from the 3G terminal

Step 3. Attach the USB cable

Step 4. Verify that the RSD application detects the 3G terminal, if it's not detected, press and hold the gaming keys once again.

Force Flash USB Cable Solution

Hardware: Refer to Figure 1-1 (USB solution), except, replace USB cable (SKN6311A) with force flash cable (SKN6168A)

Step 1. Connect the force flash cable in the same manner described in Figure 1-1.

Step 2. The 3G terminal will automatically be placed in force flash mode. There's no need to press the power key. The RSD application will now detect the 3G terminal

Manual Test Procedures

Introduction

The phone allows computer controlled testing of various test parameters.

This chapter includes the computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

Non-Signaling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signaling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The phasing parameters are stored in an EPROM in the transceiver board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted (phased) with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5697[1] or equivalent)
- Full-Rate Power Supply (SPN5049A[1])
- Battery Eliminator (5-00-3V-10000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

RF Interface

- RF Adapter (2-00-4E-10000[2])
- SMA/N type Adapter (0-00-00-40042)
- SMA Cable 0.5m (0-00-00-40047[2])
- USIM (0-00-00-40810[2])

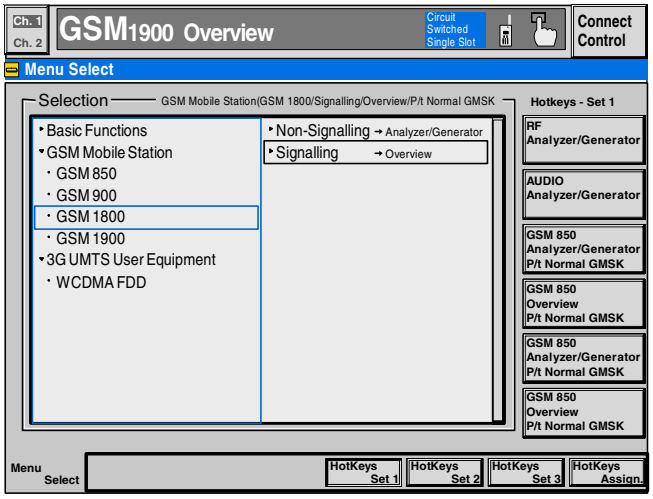
[2]Contact AMS Software and Elektronik GmbH for ordering

Call Origination

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

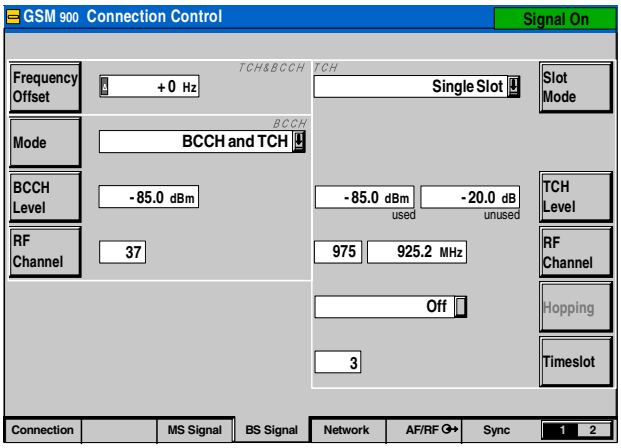
1. Install the test USIM in phone.
2. Connect hardware as illustrated in figure 2-5.

Figure 2-1. GSM Signaling Setup



3. Setup up the test box for GSM, DCS, or PCS Signaling
4. Set Broadcast Channel (BCH) to 120 (GSM), 700 (DCS), or 661 (PCS)
5. Set Broadcast channel level to -85dBm
6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS/PCS)
7. Set Traffic channel level to -85dBm
8. Wait until the phone indicates a receive signal

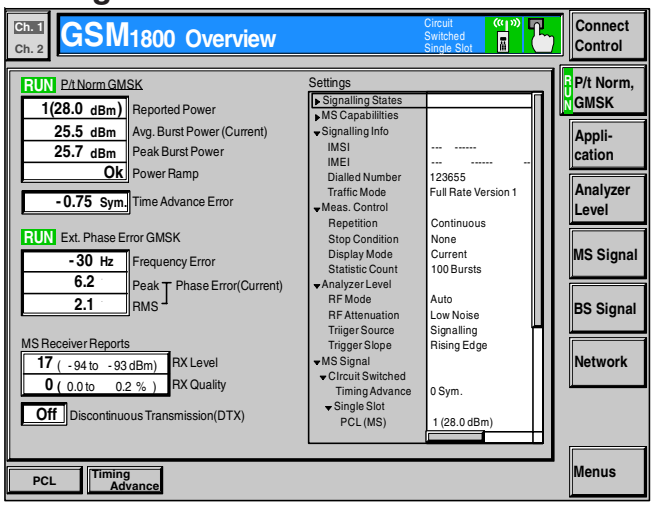
Figure 2-2. GSM Connection Control



9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 2-3. GSM Call Connected



Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-1. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	27	31	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 2-2. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

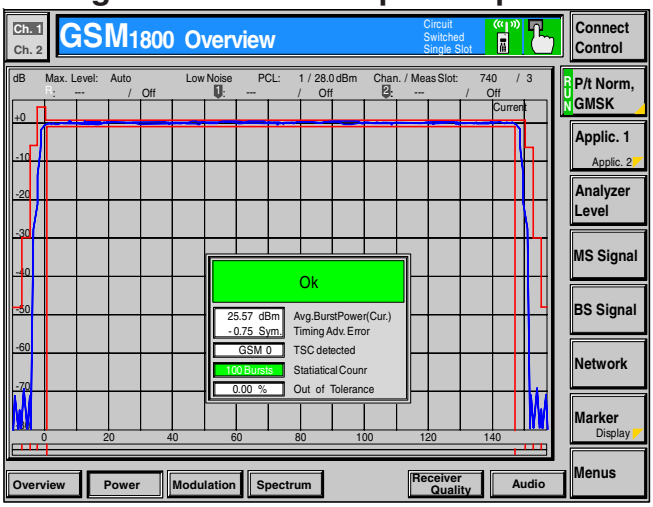
[1]Power Level = 15
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 2-3. PCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	-5	5	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 15
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Figure 2-4. Burst Output Shape



Burst Output Shape should fall within the standard limits of the Power Ramp.

BER measurements is only required if RX Quality reads a value of 4 or greater.

It is recommended that handover procedures be performed as shown in the following table.

Table 2-4. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

Figure 2-5. A1000 Manual Test Hardware Configuration

WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 2-5.

Software Requirements

None.

Call Origination (WCDMA)

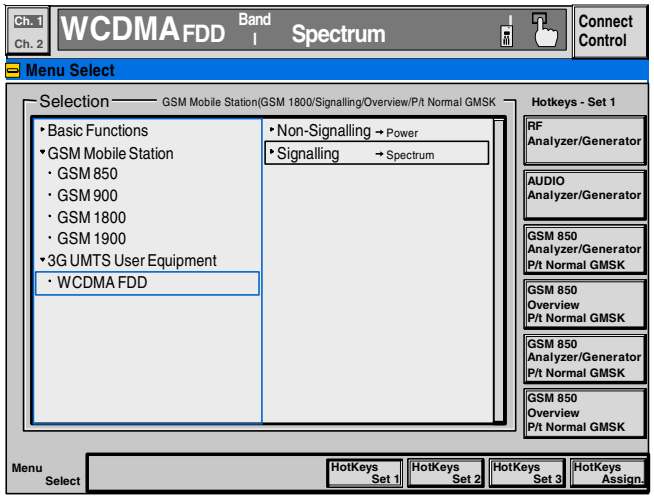
Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signaling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

Figure 2-6. WCDMA Signalling Setup

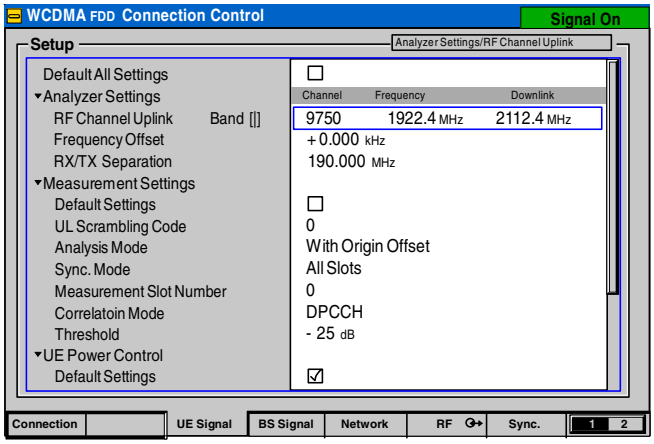


3. Setup up the test box for WCDMA FDD Signaling

4. Set UE Signal, RF Channel Uplink to 9400

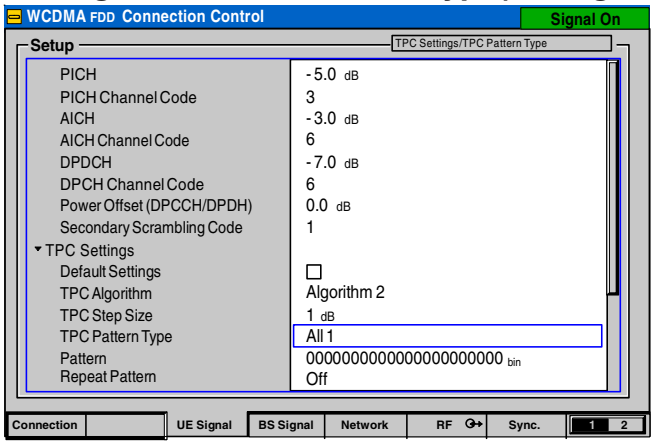
5. Set UE Signal, RF Channel Downlink to 9800

Figure 2-7. Channel Uplink(UE Signal)



6. Set TPC Pattern Type to All 1

Figure 2-8. TPC Pattern Type(UE Signal)

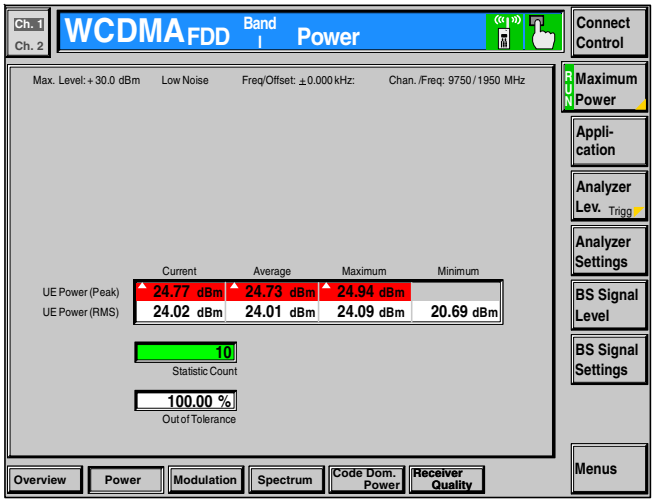


7. Wait until the phone indicates a signal

8. Dial a number from the phone and press the send button.

9. The phone is now connected.

Figure 2-9. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 2-5. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 2-10. WCDMA Modulation

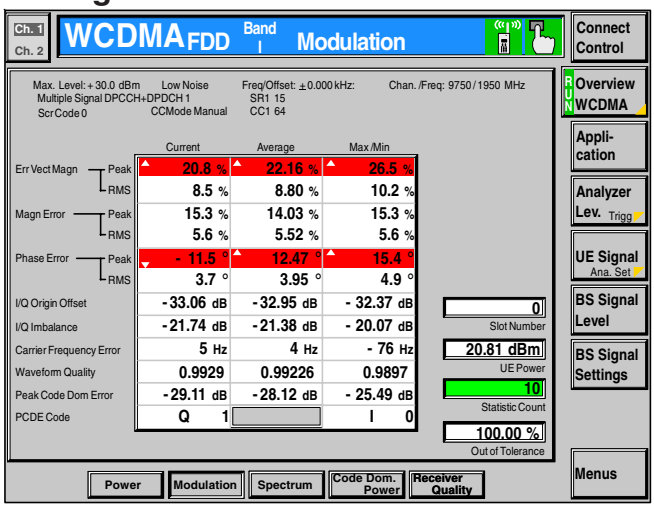
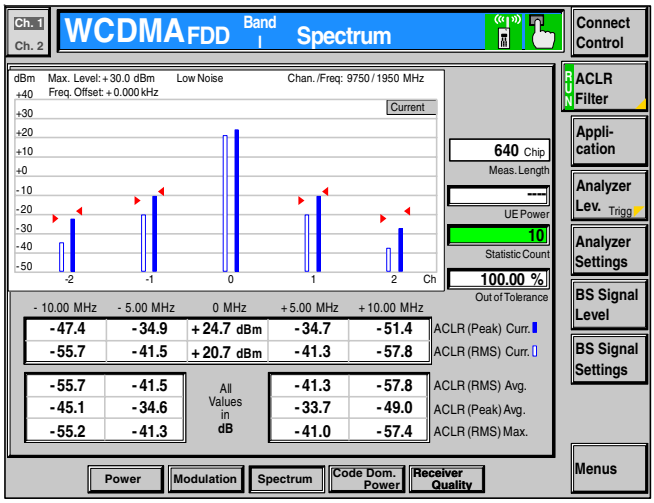


Figure 2-11. ACLR Screen

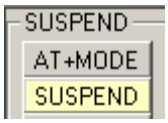


Non-Signaling Test Procedures (GSM/DCS/PCS)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands are sent using a computer.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)



Click SUSPEND (USB Only)

Hardware Requirements

Control Interface Options

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

[1]Contact your local Motorola dealer for ordering

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

Verify TX Power Output (GSM/DCS/PCS)

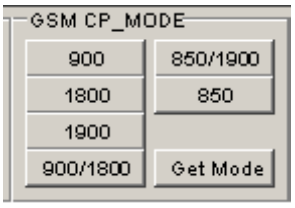
Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-6. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28.2	30	dBm
PCS TX Power Out	28.2	30	dBm

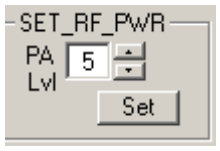
[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

Click on 900/1800 (GSM/DCS) or 1900 (PCS)

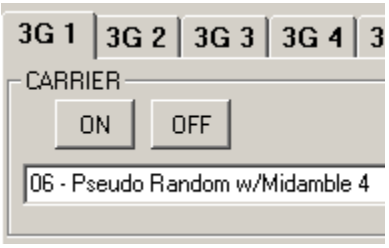


Enter 38 (GSM), 700 (DCS), or 661 (PCS) and then click Set

Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



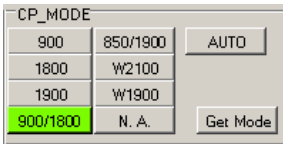
NOTE: Set Training Sequence to 4 on the test equipment.

GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

Broadcast Channel (BCH): 38
Broadcast Channel (BCH) Level: -105 dBm

Click on 850/1900 (GSM/DCS) or 1800 (DCS)



Enter Channel 38
Click INIT

Click Execute

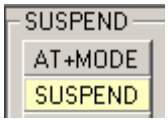
Verify return data is approximately -105 dBm

Non-signaling Test Procedures (WCDMA)

To perform non-signaling test procedures, the user is required to be familiarized with sending test commands to the phone under test.

In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)



Hardware Requirements

Refer to page 2-2 for a list of Hardware. Refer to Figure 2-5 for a configuration illustration.

Software Requirements

Radio Comm (latest release)

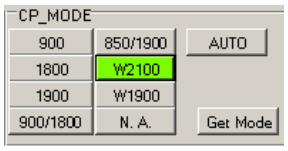
Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 2-7. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	19.5	22	dBm

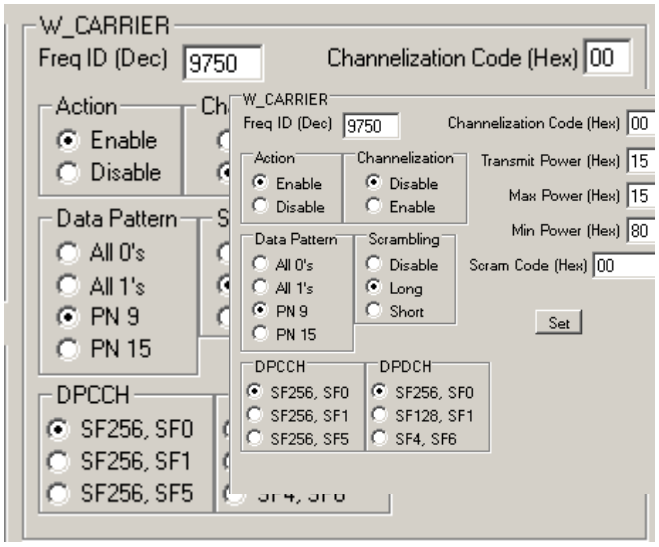
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)

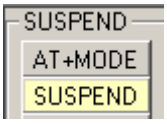


Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

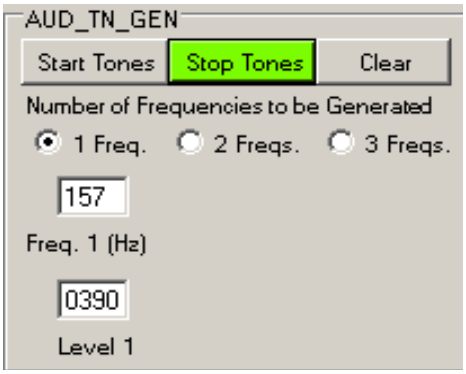
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Click AT+MODE then SUSPEND (Serial Only)
Click SUSPEND (USB Only)

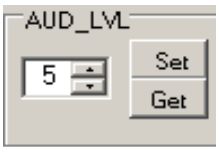


MFT Vibrator Test

Set AUD_TN_GEN as illustrated and click Start Tones

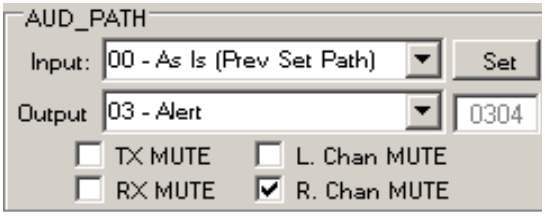


Set as illustrated
Click Set



Switch to GSM mode (located under Main>MA) Temporary until 3G section is updated.

Set AUD_PATH as ilustrated and Click Set



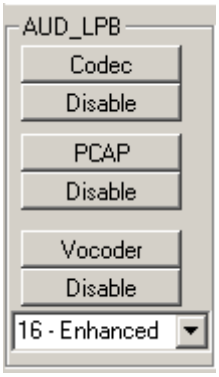
Verification

Verify that vibrate function is functioning

Handset Mic/Speaker test

Set as illustrated.
Click Set

Select Enhanced Full Rate and click Vocoder



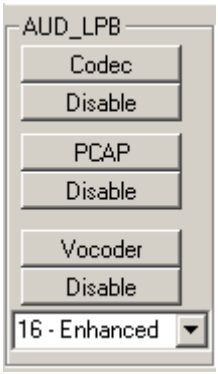
Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

Mono Headset Mic/Speaker test

Set as illustrated
Click Set

Select Enhanced Full Rate and click Vocoder

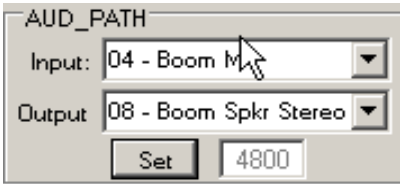


Verification

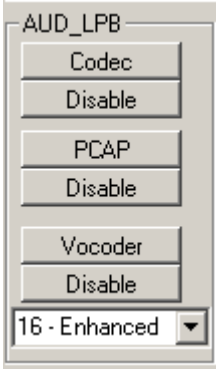
Speak into the headset mic and listen for undistorted speech in the headset speaker.

Stereo Headset Mic/Speaker test

Set as illustrated
Click Set



Select Enhanced Full Rate and click Vocoder

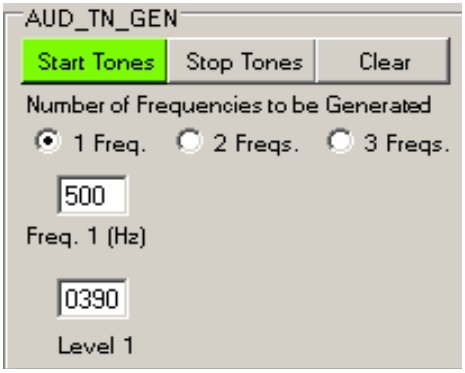


Verification

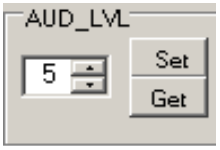
Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

Set AUD_TN_GEN as illustrated and click Start Tones

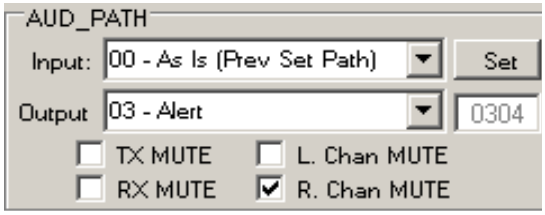


Set as illustrated
Click Set



Switch to GSM mode (located under Main>MA) Temporary until 3G section is updated.

Set AUD_PATH as ilustrated and Click Set



Verification

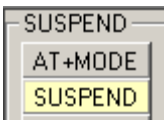
Listen for undistorted audio on the Left Channel. To verify Right Channel, de-select “R. Chan MUTE” and select “L. Chan MUTE.”

Software Version Check

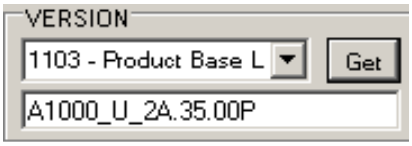
Use the following procedures to retrieve software information. Software information can also be retrieved from the phone's customer User Interface. Refer to the phone's user manual for details.

In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands

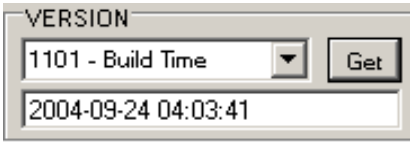
Click AT+MODE (Serial Only)



Select Product Base Label and click "Get" to retrieve software version



Select Build Time and click "Get" to retrieve Build Date

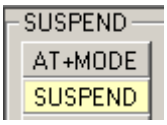


LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

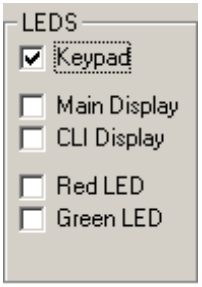
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Click AT+MODE (Serial Only)



Keypad Backlight

Select Keypad to enable. Deselect Keypad to disable.

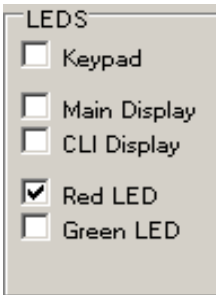


Verification

Verify that all keypad backlight LEDs activate.

Status LEDs

Select Red LED to enable. Deselect Red LED to disable.



Verification

Verify that the red status LED is active. To verify Green LED, de-select "Red LED" and select "Green LED."

Theory of Operation

A1000 Overview

Motorola A1000 is the most powerful among all convergent companion devices because it combines leading-edge technologies(AGPS for location-based services, Bluetooth for wireless connectivity, and dual-mode tri-brand support for global roaming), an advanced multimedia experience(2-way video call, video streaming and playback, MP3 and gaming, large and vibrant TFT touch screen display), and fast and easy access to information (true Internet browsing with broadband download speeds, advanced PIM functionality with multimedia messaging, multi-call functionality, external memory storage).

As a 3G product, the A1000 complies with all key specifications as defined by the 3GPP. Key product features are:

- UMTS: WCDMA 2100, GSM 900/1800 and 1900 MHz Tri-band technology
- GPRS High speed packet data (64kbps UL, 384 kbps DL)
- Display: 240x320, 262K TFT
- 1.2 mega-pixel integrated camera with 4x digital zoom and Video Graphics Array (VGA) for video recording and image capturing
- 2 Way video conferencing (Point to Point Video)
- Multimedia: Streaming, Capture & Playback (MP3, MPEG4)
- Opera™ 7.0 Full HTML Browser with Small Screen Rendering
- Picsel™ Document Viewer (Word, Excel, PowerPoint, PDF, Unzip)
- Messaging: SMS, MMS, E-mail (IMAP4, POP3)
- PIM application (calendar, contacts, notes)
- SyncML (OTA) and Desktop PC Synchronization
- Certicom MovianVPN™ Virtual Private Network Support (user installable)
- Integrated USB, Bluetooth® & A-GPS support for Location Services
- 24MB of User Memory /Supports Removable Memory (Triflash-R)
- Internal antenna

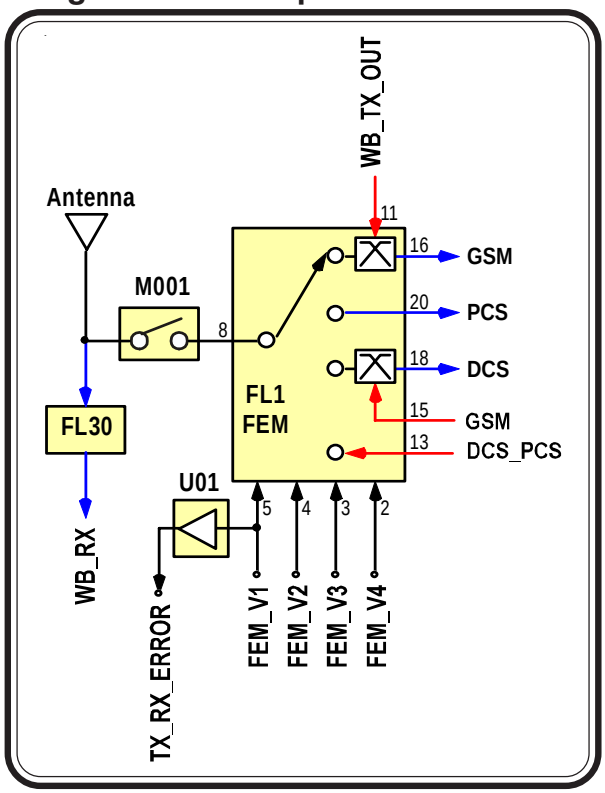
Figure 3-1. A1000 Transceiver

- Dual audio speakers
- Symbian™ 7.0 Operating System
- J2ME™ (MIDP 2.0 + APIs)
- Companion products (Stereo headsets, Bluetooth® headset, desktop charger, Bluetooth® car kits, etc.

Front End Module

GSM receive signals from the antenna are fed into the FEM (Front End Module) through an antenna matching network and RF connector (M001). The WCDMA receive signal is directly tapped into the antenna matching network. This WCDMA receive configuration allows the mobile transceiver to receive WCDMA and GSM signals simultaneously, facilitating the ability to handover from a GSM network to UMTS network and vise-versa.

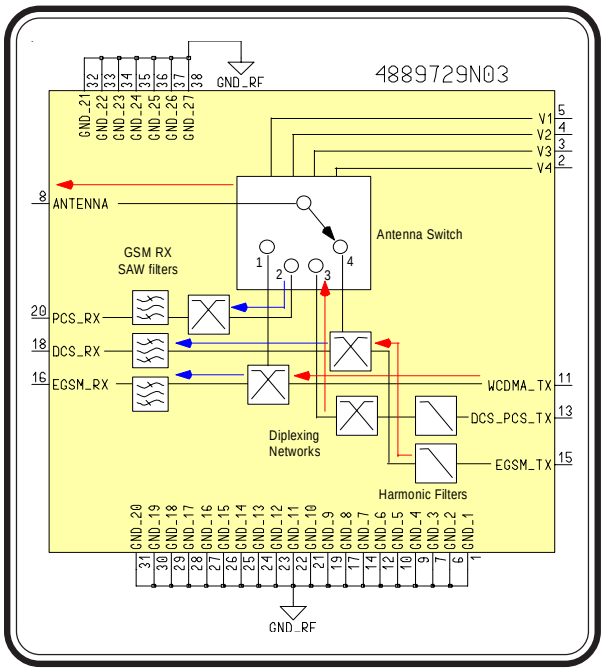
Figure 3-2. RF Top



WCDMA and GSM (all bands) transmit signals are passed through the FEM and fed into the antenna for transmission. If M001 is used, all WCDMA and GSM signals are fed into M001. Also, the internal antenna path will be in an open state when M001 is used.

The FEM integrates a 4-position GaAs antenna switch, diplexers, transmit harmonic filters, SAW filters and matching components on a multilayer low-temperature cofired ceramic (LTCC) module. The module provides band selection and filtering between the EGSM, DCS, PCS, and WCDMA (UMTS) receive and transmit bands in the A1000.

Figure 3-3. FEM Module (FL1)



There is a network on each port of the antenna switch that serves several functions. The primary function is to make each switch path behave as an open circuit to incoming signals in the WCDMA receive band (2110 – 2170 MHz). Signals in the WCDMA Rx band are thereby reflected back to the WCDMA receiver. Received signals in the EGSM, DCS or PCS bands are allowed to pass through the switch and undergo some pre-filtering, then pass through SAW filters before leaving the module.

Signals from the WCDMA transmitter are diplexed with EGSM Rx, sharing switch position 1. Similarly, signals from the EGSM transmitter are diplexed with DCS Rx, sharing switch position 4. Switch position 3 is used solely by the DCS/PCS transmitter, and switch position 2 is used only by PCS Rx.

Band Selection in the Front End Module follows the Truth Table shown in table 3-1.

Table 3-1. FEM Truth Table

Band Selected	V1	V2	V3	V4
WCDMA Rx	x	x	x	x
WCDMA Tx, EGSM Rx	1	0	0	0
PCS Rx	0	1	0	0
DCS/PCS Tx	0	0	1	0
EGSM Tx, DCS Rx	0	0	0	1

WCDMA Rx is available in any switch position.
Logic “1” is defined as 2.5 volts minimum.
Logic “0” is defined as 0 volts.

After the FEM, the EGSM or DCS receive signal is fed into one of the two transformers for differential conversion. For PCS, the receive signal leaving the FEM is fed into a high rejection band pass filter (FL005), which allows PCS RX and WCDMA TX/RX signals to pass. The PCS RX and WCDMA RX signal is then fed into an adjustable gain LNA (U001).

U001 operates in two gain modes selectable by MBC_EN2. The nominal gain expected while in high gain mode is ~16dB. During high input signal levels of ~–40dBm or stronger, the LNA will be in low gain mode. Currently, signal levels below ~–55dBm would trigger the high gain mode.

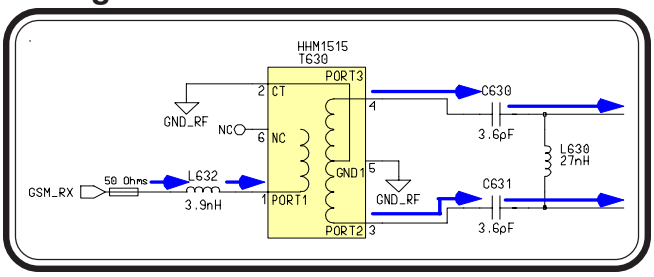
FL004 is a digital filter which is used to pass PCS receive signals to a transformer, for differential conversion, located in the GSM circuit. WCDMA receive signal is passed to the WCDMA circuit.

RF GSM Receiver

BALUN

From the FEM, the GSM singled-end, unbalanced received signals are fed into the Algae MB IC. Since the Algae MB IC expects a balanced differential receive input signal, the EGSM, PCS, and DCS signals must first pass through a differential conversion. Balun transformers provide the conversions from an unbalanced to a balanced line condition.

Figure 3-4. Balun Transformer



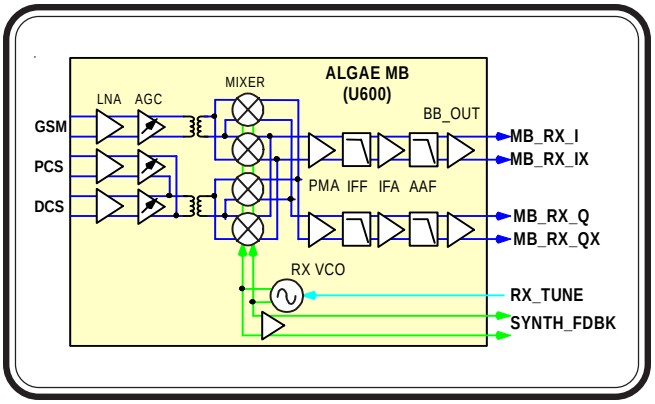
Each GSM band will contain a Balun transformer for differential conversions. The expected insertion loss for the Balun transformer is approximately 0.6 dBm.

ALGAE MB IC (U600)

Three LNAs are used for each receiver frequency band. Two hi-band LNAs are used for DCS and PCS frequencies and one low-band LNA is used for EGSM. Both hi-band LNAs are grouped together to share the same impedance matching transformer at the output. The low-band EGSM LNAs uses a separate impedance matching transformer at the the output.

Automatic gain control is provided by an AGC current steering differential pair. This current steering stage diverts current from the LNA load to supply in order to reduce the gain. The current steering differential pair alone would not have the desired transfer function, therefore an AGC linearizer is needed to provide a response that is linear in dB/V.

Figure 3-5. ALGAE MB (Receiver)



The LNAs drive AGC current steering stages that feed integrated transformer matching networks. The transformer drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q.

The downmixer converts the RF signal to baseband so that the signal can pass through a low-pass antialiasing filter and be converted to a digital format.

The output of the mixer connects directly to the post-mixer amplifier. Large integrated capacitors are used to provide a low-frequency, low-pass corner at the output of the mixer. The signal then passes through baseband amplification and anti-aliasing filtering. The output of ALGAE MB will be balanced RXI and RXQ signal. It will have a 100kHz Very Low Intermediate Frequency (VLIF) signal that will be sent to the Harmony for Analog to digital conversion.

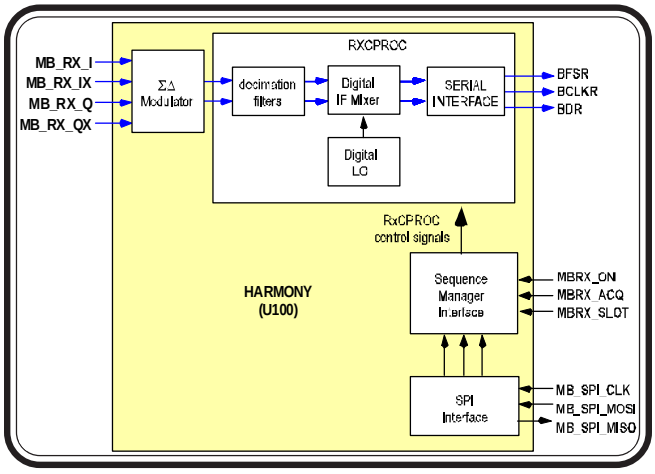
The LO signal is provided by a fully integrated VCO that drives either a divide-by-two or divide-by-four quadrature generator. In addition, a divide-by-3or5 circuit is used to feed back the LO signal to the synthesizer. The divide-by-3or5 circuit drives a differential output stage that provides the appropriate power level

to the synthesizer. This output stage is shared with the TX path and provides the synthesizer feedback signal in both transmit and receive.

HARMONY GSM_RX (U100)

The RXI and RXQ VLIF signal entering the Harmony is sent to the Sigma-Delta modulator which transforms the slow moving analog signal into a high speed digital output. The Sigma-Delta modulator is set as an Analog-to-Digital Converter (ADC). The output of the Sigma-Delta modulator is then fed into the Receive Coprocessor (RxCPROC).

Figure 3-6. Harmony (GSM RX)



The RxCPROC includes the digital signal processing hardware required for the receive transceiver (Rx) after the initial conversion done by the sigma-delta modulator. It's configured to be used in the very low intermediate frequency mode (VLIF). The RxCPROC supports the GSM and EDGE standards.

The RxCPROC is represented by blocks listed as "decimation filters", "digital IF mixer", "digital LO" and "serial interface". The RxCPROC decimates and filters the I and Q quadrature input signals and converts them to baseband. Processed signals are sent serially to the Base Band Port (BBP) to be further handled by the DSP and VIAC.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data to the BBP module in the POG. SDFS is a framing signal which marks the beginning of an I,Q transfer. SDRX is the serial data. The clock used for the serial transfer is SCLK.

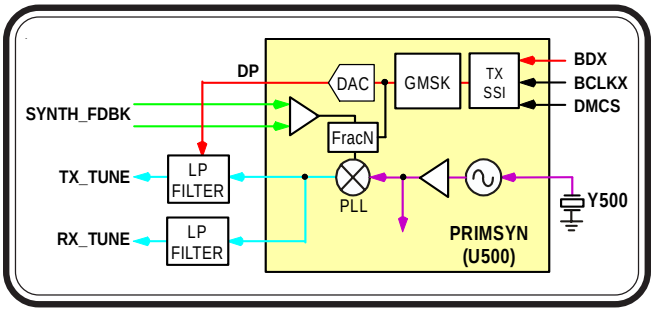
The RxCPROC is controlled via the SEQUENCE MANGER or SPI. Each control line of the Seq. Manager can be overridden by a corresponding line from the SPI (MB_SPI_CLK, MB_SPI_MOSI). Layer One timer signals (MB_RX_ON, MBRX_ACQ, MBRX_SLOT) from POG control the start of major sequences of events.

RF GSM Transmitter

PRIMSYN GSM_TX (U500)

The PRIMSYN receives SSI TX data at *DMCS* (digital input to start Tx modulation), *TXCLK* (clock for serial transfer) and *SDTX* (serial Tx data) from POG. This data pattern input to a fractional N synthesizer with a 24-bit resolution. For EGSM the synthesizer output is 880 – 915MHz, DCS is 1710 – 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

Figure 3-7. PRIMSYN (GSM TX)

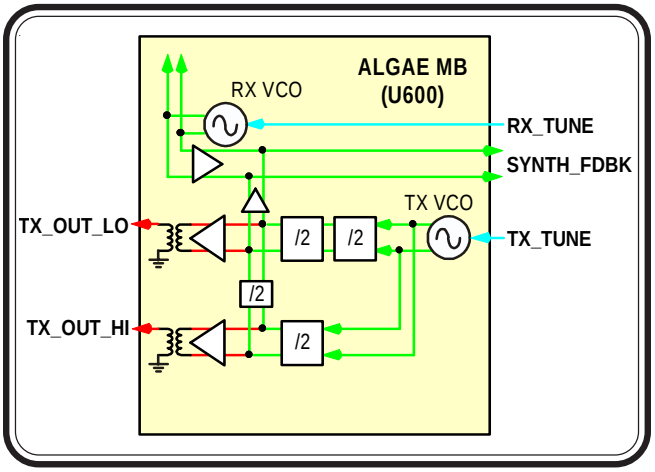


ALGAE MB IC (U600)

TRANSMIT SECTION

An integrated VCO is used for the transmit path. A single VCO is used for transmit. A low noise floor divide-by-2 stage drives the high band output. The low band output is driven by a divide-by-4 stage.

Figure 3-8. ALGAE MB (Transceiver)



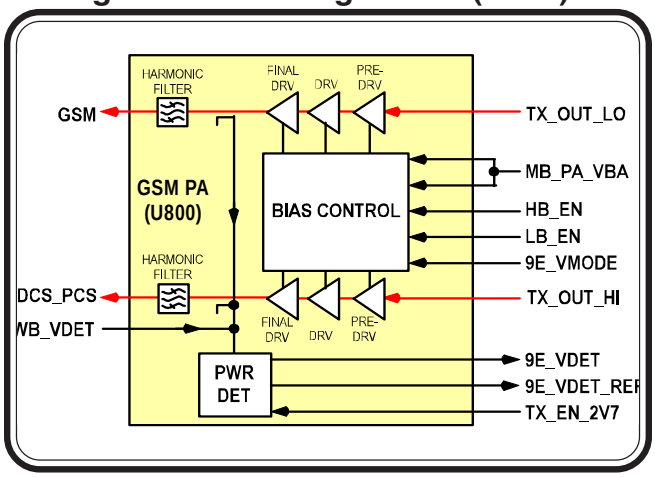
Two transmit output stages are provided. Both stages have integrated output matches in order to reduce the required number of discrete components. The integrated matches are implemented as differential to single-ended transformers.

The transmit signal is fed back to the synthesizer through a differential output stage that is shared with the receiver.

GSM PA (U800)

The TX VCO output signal from the ALGAE MB is injected in the Durango 9E3G via the TX_OUT_LO (Low Band) and TX_OUT_HI (Hi Band). Durango

Figure 3-9. Durango 9E3G (U800)



9E3G is a quad band PA Module for GSM applications in 3G phones. The module uses a dual amplifier lineup which operates in the three separate EGSM, DCS1800, and PCS1900 bands. It is compatible with GSM/GPRS operating modes. The integrated module incorporates coupler/detector for power control, Low pass filtering for harmonic rejection, and is internally input and output matched to 50 ohms.

This Transmit module is to be used as the final amplification stages in the A1000 for the EGSM (900 MHz), DCS (1800 MHz) and PCS (1900 MHz).

The nominal expected maximum gain is ~30dB.

The *VDET* (output) is the RF feedback along the DC reference *V_REF_DET* (output) are used in backend PA Control (PAC) processing by the HARMONY.

VBA_1 and VBA_2 are inputs from HARMONY that controls the PA output level. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases.

The power detector is internal to the PA and is shared among all GSM bands as well as WCDMA. WB_VDET connects WCDMA TX to the power detector

HB_EN enables the high band (DCS/PCS) amplifier lineup. LB_EN enables the low band (EGSM) amplifier lineup. TX_EN_2V7 enables the detector.

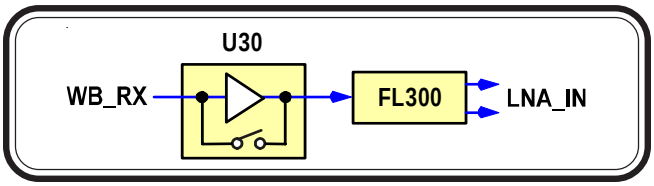
9E_VMODE sets the operating mode of the PA. GMSK and EDGE modes are supported, but only GMSK mode is used in this design. 9E_VMODE is set high during GMSK TX mode. 9E-VMODE is set low when the transmitter is in standby mode. This line is also enabled in WCDMA mode to allow proper WCDMA power detection.

RF WCDMA Receiver

MC13820 (U30)

The first IC in the WCDMA Rx line up is U30 (MC13820), which is a Low Noise Amplifier. The RX frequency will be amplified and passed on to OneLife WB through FL300. The LNA is controlled by Harmony (U100) through two enable lines. MBC_EN1 enables gain for the LNA while MBC_EN2 enables the IC. Both lines can be probed at testpoints located near Harmony (TP120 and TP121). U30 operates from the PCAP supply voltage *VRF_RX_2_775*

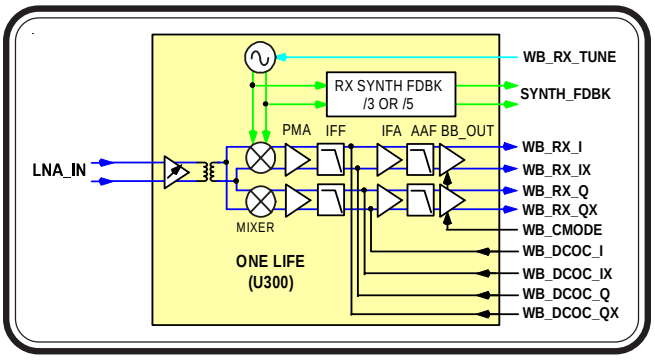
Figure 3-10. WCDMA LNA



ONELife (U300)

ONELife is a full custom mixed signal BiCMOS IC with the SiGe option with electroplated copper inductors. This IC is a fully differential direct-conversion front-end IC and is comprised of a multiband RF section and a single path baseband section. The RF section is comprised of three Low Noise Amplifiers, two sets of quadrature mixers and an integrated 4GHz VCO with a divided prescaler output. Only one LNA is used in this design to cover the WCDMA/UMTS band (2110-1710). The LNA has two gain states; a high gain state and a bypass state with no reverse isolation. The LNA drives the quadrature mixers, via an integrated transformer matching network, that convert the RF signal to baseband, quadrature I and Q. The LO signal is provided by fully integrated VCOs that drives a divide-by-two quadrature generator. In addition, a divide-by-three/five circuit is used to feed back the LO signal to the synthesizer via an open collector output stage.

Figure 3-11. ONELife (U300)



The baseband section is comprised of two separate I and Q paths each containing a PMA, an anti-aliasing filter made up of an IFA with an active pole and DCOC, two bi-quad sections, and an output buffer. The baseband signal path has six poles of baseband filtering distributed between mixer pole, the active IFA pole, and the two bi-quad blocks. The PMA has pseudo-continuous gain capability and is part of the AGC system along with the LNAs. The PMA AGC is controlled through five dedicated IC pins. At the output of the PMA stage, a baseband detector circuit provides broadband, strong signal information to the baseband part. DC Offset correction is provided through external differential pins to provide offset corrections to the internal IFA stage. The output buffer receives an input voltage via feedback from the Harmony WB_CMODE line so that OneLifeWB's output signal drives the A/D with the correct common mode voltage.

Control and programming are done through a SPI interface from Harmony. Two supplies are required to power the IC, VRF_DIG_1.875V for SPI lines and VRF_2.775V for RF portions.

Harmony WCDMA_RX (U100)

The RX I an Q baseband signals are fed into the Sigma-Delta modulator of the Harmony. The Sigma-Delta modulator is an A/D converter that converts the I and Q baseband inputs to noise shaped 6-bit digital outputs. These outputs are then next decimated by a ratio of 3 using 3-stage cascaded comb type filters to a sampling rate of 15.36 MHz.

DC offset correction is performed next immediately to minimize the amount of delay in this mixed mode control loop to achieve rapid DC acquisition during *normal mode warmup sequences*. The DC offset correction unit has feedback to the OneLife-WB IC to be able to correct for DC offsets at the inputs to IF amplifier stage.

The matched selectivity filter is designed such that it provides the desired selectivity to meet adjacent channel and blocker specifications in the 2100 and 1800 MHz frequency bands.

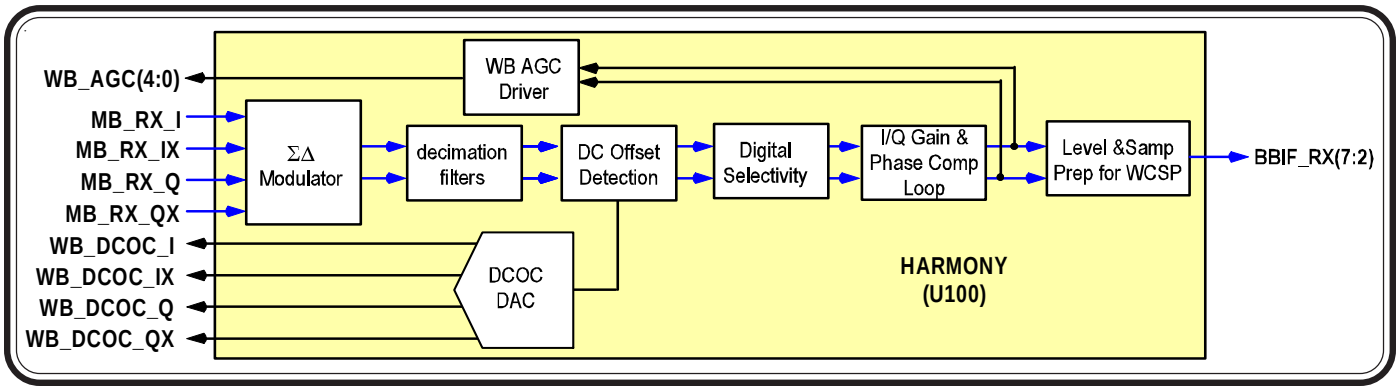
I/Q gain and phase imbalance equalization units located next in the lineup is used to correct for I/Q mismatches due to both the base station transmitter as well as the mobile device.

Next, the outputs of the I/Q gain equalization unit feed into the RF/IF AGC as well as the digital gain compensation control units. These outputs from the I/Q gain equalizer are used by the AGC unit for on-channel power detection. In addition, the AGC unit also receives off-channel power indication from a 2-bit SOS detector data bus from OneLife-WB IC. The on-channel and off-channel power levels are used by the RF/IF AGC unit to control internal and external LNA step attenuator stages as well as the variable gain PMA stage in OneLife-WB IC.

Two bit control lines are used to control each of the external LNA step attenuator stages. Alternately, a 1-bit control line is employed to control the internal LNA in the OneLife IC. In addition, a 5-bit parallel digital bus is employed to control the PMA variable gain control stage in OneLife-WB IC. The AGC unit also supplies the detected RSSI level to the external host device (e.g. POG IC) based upon the current RF, IF, and digital baseband gain control settings as well as the on-channel RSSI detected.

Following the I/Q gain equalization stage, a digital gain compensation unit is located next. The purpose of this gain compensation unit is to provide a 6-bit gain compensated output signal to the WCSP unit given that the input signal's dynamic range is 13 bits. The 15.36 MHz rate I and Q outputs are then interleaved in the BBIF (baseband interface) unit to generate the output I/Q data at a 30.72 MHz rate on a single 6-bit data bus to the external host device.

Figure 3-12. Harmony WCDMA RX (U300)



RF WCDMA Transmitter

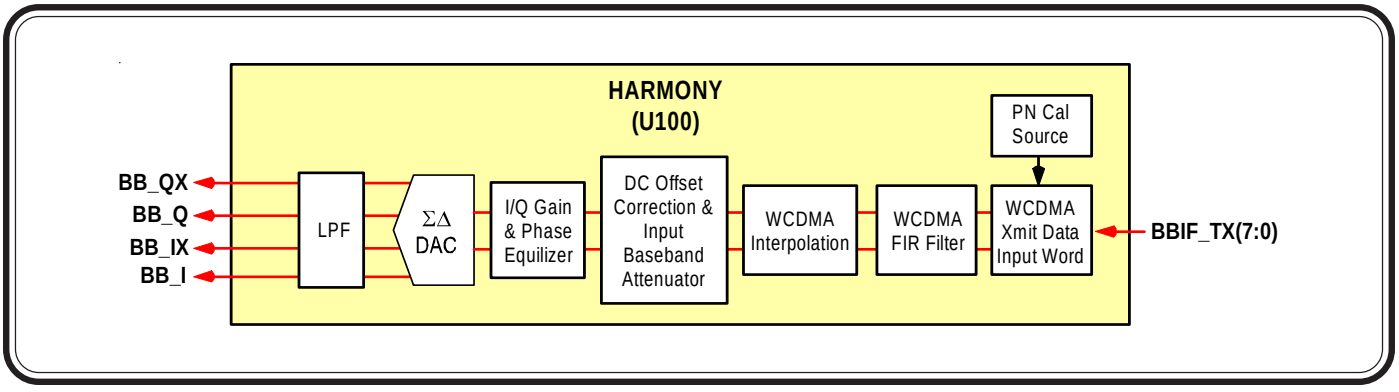
Harmony WCDMA TX (U100)

The Harmony provides pulse shaping and modulation of the 8-bit interleaved TX data coming from the POG. RF carrier suppression and baseband DC offset, I/Q gain and phase equilization will be then be performed. Finally, the I/Q signal is passed through a DAC and fed into the Rattler IC.

An 8-bit parallel interleaved data interface (BBIF_TX) is used to load the I and Q chip data from POG into the WCDMA signal path. Alternately, a PN calibration signal may also be loaded into this signal path for correction of baseband DC offsets and I/Q imbalances during transmitter warmup sequences. The parallel I and Q data from POG is first pulse shaped at a 7.68 MHz sampling rate using 31-tap SRRC FIR filters for the I and Q channels. These filters' outputs are then interpolated to a 30.72 MHz sampling rate using two stages of halfband interpolation filters.

The 12-bit outputs from the baseband pulse shaping and modulation system are fed into this DC and I/Q correction system. The specified 12 bit inputs first pass through the DC offset, I/Q phase and gain equalization blocks. The output samples from the gain equalizer are then fed into the sigma delta DACs at a higher sampling rate to minimize anti-aliasing filtering requirements. Following the DACs, there is an analog gain stage with 5 attenuation settings available for the baseband gain control system. Following this stage, a 2-pole passive filter and a 4th order Butterworth filter is employed in the quadrature signal path to eliminate the shaped noise from the sigma delta D/A's. The outputs of these reconstruction filters feed into the RF modulator IC (Rattler).

Figure 3-13. Harmony WCDMA TX (U300)



MC13786 (U200)

The MC13786 is an integrated I/Q modulator, IF and RF variable gain amplifier, UHF frequency synthesizer with a fully integrated VCO, image-reject upconverter mixer, and linear PA driver.

The synthesizer or phase locked loop (PLL) consists of a buffer amplifier, multi-modulus prescaler (divide by 4, 5, 6, and 7), a sixbit programmable post divider, reference divider, phase detector, and charge pump. The PLL uses a reference frequency of 15.36 MHz. One frequency synthesizer/VCO provides both the main and offset LO functions. The VCO operates over a frequency range of 2114 MHz to 2263 MHz and is fully integrated.

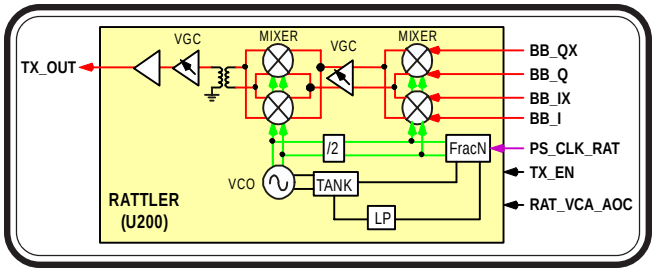
The I/Q Modulator consists of a quadrature generator and two Gilbert Cell active mixers. Using the offset LO and quadrature generator, the active mixers modulate the differential baseband I/Q signals onto a TXIF signal. Depending on the channel selection, the TXIF frequency will range from 274 MHz to 283 MHz.

From the active mixers, the TXIF signal is fed into a IF Variable Gain Amplified (IF VGA). The IF VGA has 70 dB of total typical gain control range and is controlled by the VGC line. The output of the VGA shall have a single pole bandpass tank circuit to provide attenuation to far-out noise.

The upconverter has an image-reject configuration so that the unwanted sideband is rejected to decrease the linearity requirements of the VGA stage. An input polyphase filter shall provide the necessary phase shift for the IR mixer. The TXIF signal is upconverted to a TX carrier frequency ranging from 1920MHz to 1980MHz. An on-chip copper balun shall provide the differential to single ended conversion necessary for the following stages.

The VGA provides a reduction in gain and current to optimize the TX lineup for lower output power levels. The PA driver amplifies the signal to provide sufficient drive for the radio power amplifier.

Figure 3-14. Rattler (U200)

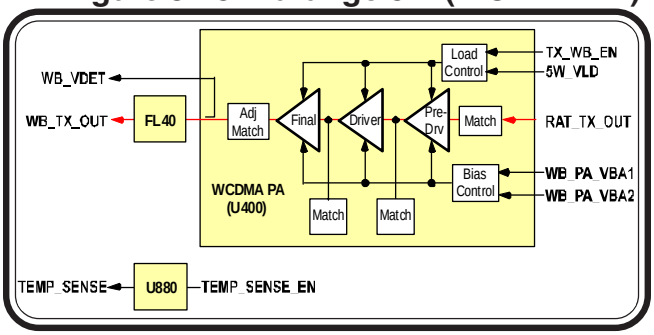


WCDMA PA (U400)

Durango5W is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 – 1980MHz. The nominal expected maximum gain is ~30dB.

A Motorola proprietary high power / low power efficiency enhancement load switch (5W_VLD) is included in the output match. VLD adjusts the output load for optimum efficiency from low power to high power out.

Figure 3-15. Durango 5W (WCDMA PA)



In conjunction with VLD, bias control (WB_PA_VBA1/WB_PA_VBA2) is performed between high and low power ranges.

The amplified WCDMA carrier is fed into a RF coupler device which has an integrated RF detector. An RF detect will pass through the Durango 9E3G (GSM PA) before being fed to the Harmony for power detection.

U880 is used to measure temperature. Its linear output is a voltage signal that corresponds to its physical device temperature. TEMP_SENSE is measured by PCAP and the MCU (POG) retreives the temperature readings every 5 seconds and passes it to the DSP (POG) so that the temperature compensation tables are updated.

The isolator provides a stable 50 ohm PA load. It also protects the PA from interfering with other frequency bands. Finally, it guards against IM products being produced by the transmitter and affecting receiver circuits.

RF Interface

Harmony

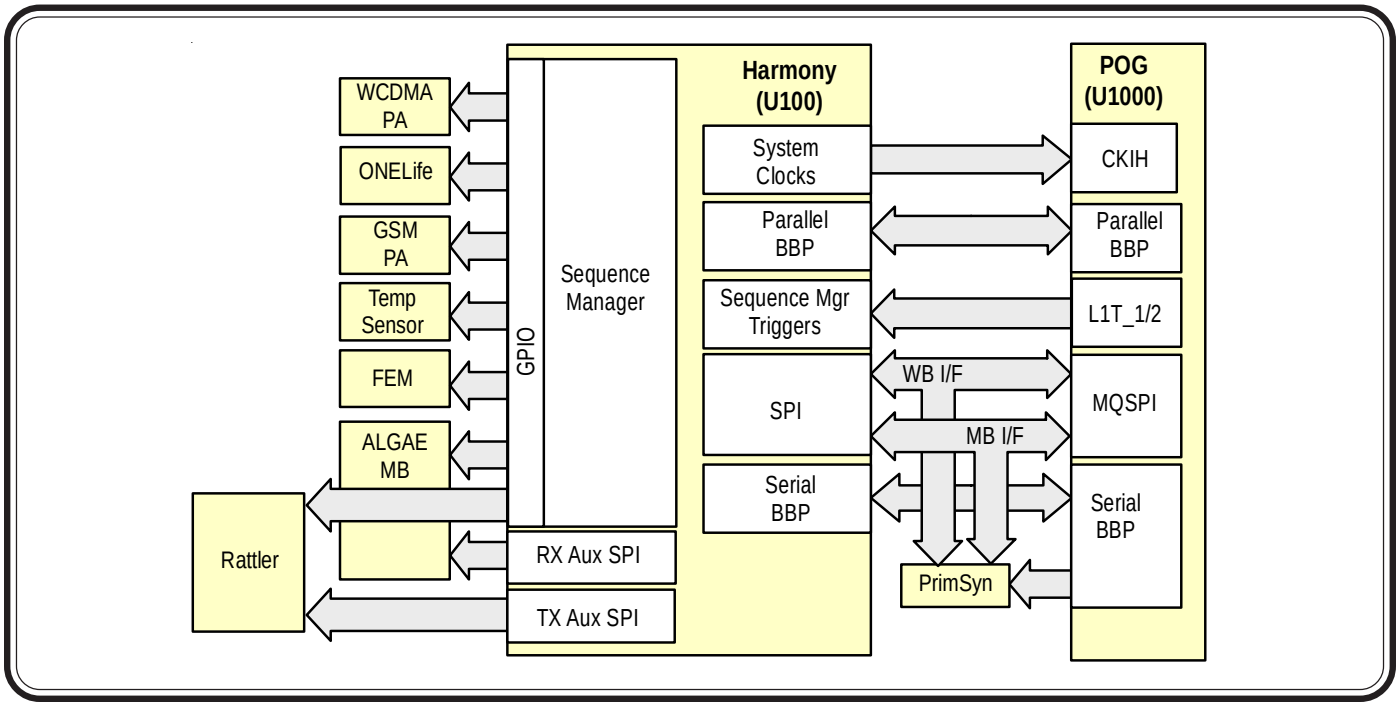
The Harmony IC is a mixed-signal transceiver backend IC intended to support GSM, EDGE and WCDMA services. It includes 2 receive paths: a medium-band path and a wideband path. The medium-band path is intended for GSM and EDGE and is configured to support VLIF receiver architecture. The wideband path is intended for WCDMA and is designed to operate in a direct conversion receiver architecture. Both of these receive signal paths are optimized for non-compressed mode. The transmitter path is designed to operate in a direct-launch transmitter architecture. The IC also includes dual clock synthesizers, as well as general support circuit such as sequence manager and SPI.

The Harmony IC and Base-Band (POG) IC interface consists of two independent sets of SPI lines (WB I/F, MB I/F); 2 chip-enable inputs, 2 clock inputs, 2 data inputs, and 2 data outputs. Harmony interfaces to the Base-band IC as a slave IC, however, it is also a master to two auxiliary ICs (Algae MB and Rattler) using two independent sets of SPI lines (TX AUX, RX AUX). The two auxiliary ICs are programmed by the Base-Band via Harmony.

In order to decrease the overall area required for controlling the sequences, a sequential access strategy was developed. The sequence manager would consist of controllers that would access an SRAM device sequentially. These controllers run of a set of programs that are pre loaded in to an SRAM memory device. In order to eliminate the need for a stack and interrupts each controller is dedicated to a single task. In the sequence manager there exists a controller per task, where the number of maximum tasks would be equivalent to the number of input TIMER lines.

A serial bus consisting of SDFS and SDRX will transmit the GSM RXI and RXQ data in 2's complement format to the Serial BBP module. The RXI and RXQ data will then be handled by the DSP integrated in the

Figure 3-16. RF Interface Block Diagram



POG. The Serial BBP module for TX is not used in this design.

The WCDMA path receive path has a parallel BBP interface to send data to the Base Band processor. The interface is programmed to run at 15.36mhz. An 8-bit parallel interleaved data interface (Parallel BBP) is used to load the TX I and Q chip data from the external host processor (POG) IC into the WCDMA signal path of Harmony.

Baseband Electrical (Digital)

OMAP 1510 (U2000)

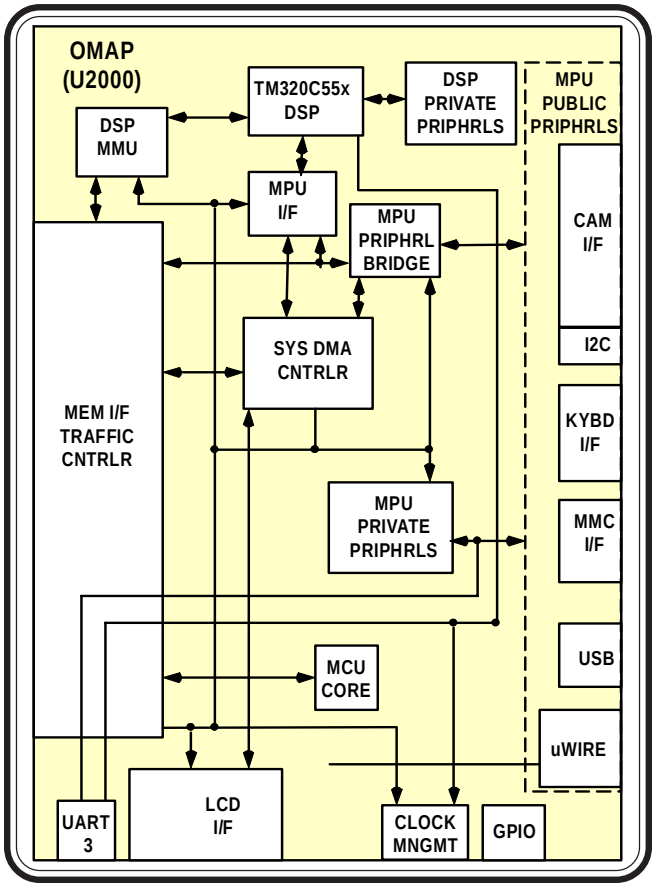
The OMAP1510 processor features first generation Texas Instruments Incorporated OMAP™ architecture with the OMAP3.1 gigacell as its core building block.

The OMAP1510 processor is designed to support Symbian OS. The OMAP1510 performs all personal communication system (PCS) tasks such as call manager, email/fax reader/composer, Internet access, personal digital assistant (PDA), and personal information management (PIM) tasks.

The OMAP1510 processor is targeted for the following applications:

- Wireless video and image processing (MPEG4, JPEG, Windows Media Video [WMV])
- Wireless advanced speech applications (text to speech, speech recognition)
- Wireless audio processing (MPEG-1 Audio Layer3 [MP3], AMR, WMA, AAC, and other GSM speech codecs)
- Graphics and video acceleration
- Web generalized access
- Wireless data processing (fax, encryption/ decryption, signature verification, and watermarking)
- Bluetooth interface and applications
- USB host and function support
- MMC, SD, and MS card interface applications and support

Figure 3-17.OMAP Block Diagram



The OMAP1510 device includes the MPU subsystem, the DSP subsystem, a memory interface traffic controller, general-purpose peripherals, dedicated multimedia application (MMA) peripherals, and multiple interfaces. The MPU is the master of the platform, and it has access to the entire 16M bytes of memory space and to the 128K bytes of I/O space of the DSP subsystem. Additionally, the MPU and DSP share access to the internal SRAM and external memory interfaces.

POG (U1000)

POG is the baseband processor IC of the 3G chipset solution. POG is crafted to provide a high performance embedded solution at low power for 3G mobile devices. POG is a TriCore processor IC integrating a powerful DSP core, a 32bit MCU RISC core with unified cache and a custom 32bit RISC engine for data movement across the processing domains.

The DSP core is a high performance StarCore with four parallel ALUs, the SC140, with a novel Variable Length Execution Set (VLES) architecture which maximizes the execution of multiple instructions in a single clock cycle. The SC140 is assisted by 3G specific hardware accelerators and timers to optimize performance and power. As part of the 3G support, the Wideband CDMA Signal Processor (WCSP) module implements modem functions required by the CDMA subscriber unit in accordance with the 3GPP specifications.

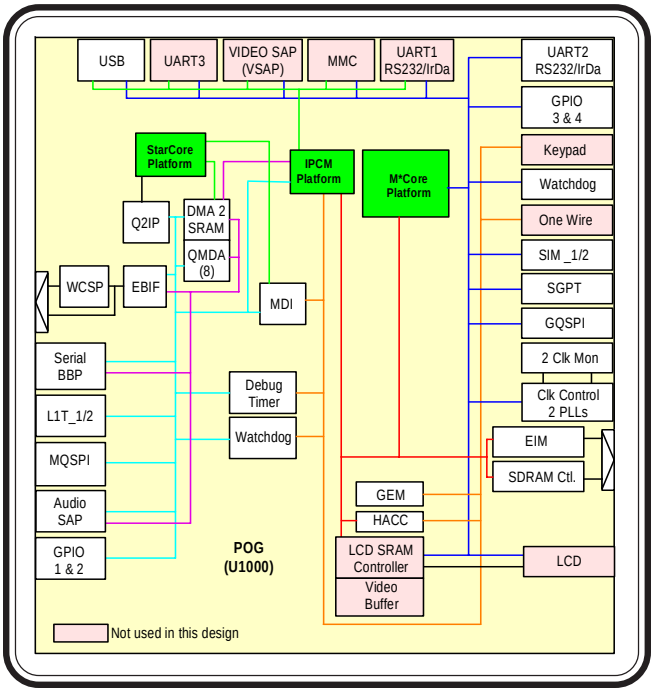
The 32bit MCU RISC core is the M*Core M341 designed for high performance and low power embedded systems. The M341 embodies an 16K unified cache, integer multiplier and MMU in support of virtual memory management OSes.

Data communication across the cores is handled by a flexible 32bit RISC machine, the Inter Processor Communication Module (IPCM). The IPCM supports flexible data flow between the MCU, DSP and the multimedia peripherals.

Due to the dual processor architecture design of A1000, some of the POG modules are not used. Functions of these unused modules are controlled by the OMAP application processor. The primary functions of POG will include,

- Colorado RF interface
- PCAP Audio interface
- SIM interface
- GPS GAM interface

Figure 3-18. POG Block Diagram



Display Interface

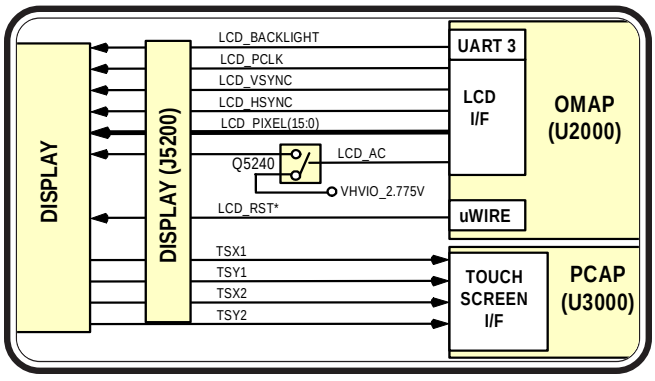
The OMAP uses a dedicated LCD DMA channel for the LCD display. The LCD controller is configured to interface with an active color panel showing 16-bit color, providing up to 65536 colors. A 16-wire interface is used to pass the pixels to the panel, with 1 pixel per clock.

In active color mode the LCD line clock pin functions as a horizontal synchronization (HSYNC) signal and the frame clock pin functions as a vertical synchronization (VSYNC) signal.

Here is the line descriptions of the LCD controller.

- LCD_PIXEL(15:0) are I/O pins used to transfer sixteen data values at a time to the LCD Display
- LCD_PCLK clock the pixel data into the line register
- LCD_HSYNC is the horizontal synchonization signal
- LCD_VSYNC is the vertical synchronization signal
- LCD_AC is an poutput enable to signal when data is latched from the data pins using a clock signal

Figure 3-19. Display Interface



The touchscreen itself consists of two parallel resistive plates, called the X and Y plates, separated by short distance. Contact initiated by a user using a stylus or finger creates a series of resistances.

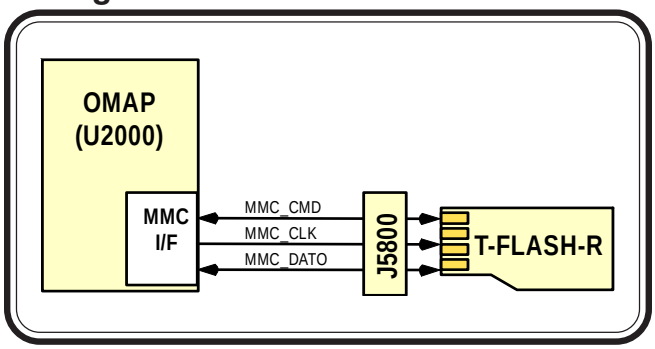
The touch screen interface consists of a digital state machine, a voltage reference, and an analog switch matrix which is connected to the four wire resistive touch screen inputs (TSX1, TSX2, TSY1, TSY2) and the internal 10 bit ADC. The state machine controls the sequencing of the switch matrix to cycle through the three types of measurement modes (position, pressure, plate resistance) and the low power standby interrupt mode. The separate internal voltage reference, TS_REF, is disabled in standby and off modes.

MMC/SD Flash Interface

The MMC/SD host controller provides an interface between the OMAP and Triflash-R memory card.

The MMC/SD host controller handles MMC/SD protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for syntactical correctness.

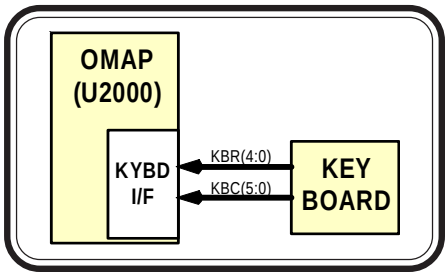
Figure 3-20. MMC Interface



Keypad Interface

The keyboard interrupt to the OMAP is an AND of the eight row lines filtering during one 32-kHz clock period (CLK_32KHZ). As soon as any key of the keyboard matrix is pressed, the corresponding row and column lines are shorted together and a low level is driven on the corresponding row line, generating a keyboard interrupt.

Figure 3-21. Keyboard Interface



There are 14 keys total: 4 side, 4 directional, 1 select, 2 gaming, 3 other. All keys in the matrix are on either the upper or lower flex, as opposed to the transceiver board. The slide switch is mounted directly to the transceiver. The two slide switch functions, power and device lock, are not part of the keypad matrix.

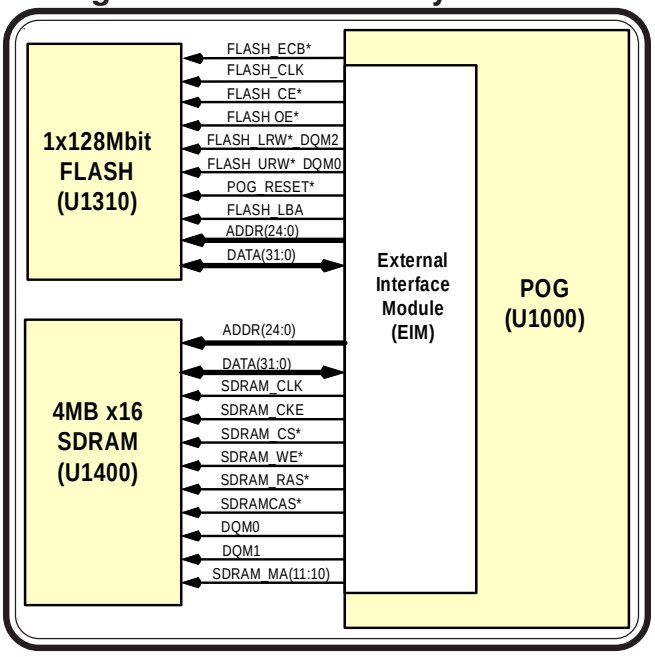
The entire keypad backlight, except for the end key, is powered by VBOOST and controlled by PCAP2's BL_SINK pin. The single red LED on the end key is powered by VHVIO and controlled by PCAP2's BL2_SINK. The red/green servicelight is controlled by the dedicated LEDR/LEDG PCAP2 pins

POG Memory

The POG flash memory uses a 128 (128 Mbit) 1.8 Volt wireless memory which delivers high density flash memory in a single package. Individually erasable memory blocks are optimally sized for code and data storage. Four 16-Kword blocks and seven 64-Kword blocks are located in the parameter partition. The rest of the flash memory is divided into fifteen partitions of eight 64-Kword main blocks. By dividing the flash memory into partitions, program or erase can take place simultaneously during read operations. The device is available in a 56-ball vfBGA* package with 0.75 mm ball pitch.

The POG SDRAM device is a JEDEC standard SDRAM with 1.8V core supply, 1.8V I/O supply, four banks, and density of 4Mb x 16 (64 Mb). It is low power with special function support including partial array self refresh and temperature compensated refresh. It has a max frequency of 104MHz with CAS latency of three.

Figure 3-22. POG Memory

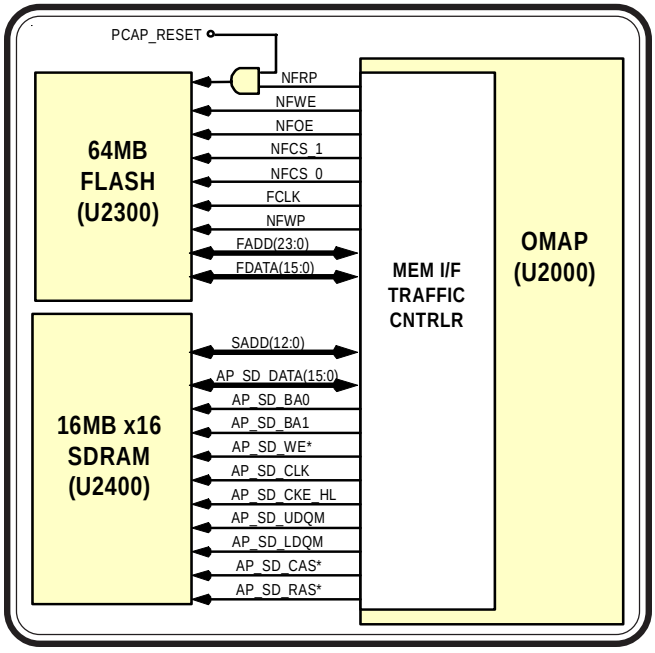


OMAP Memory

OMAP interfaces to a 512-Mbit (2x256Mbit) 1.8 Volt wireless Synchronous Flash memory Stacked-CSP which delivers high density flash memory in a single package. The device is in an 88-ball (80 active balls) matrix Stacked Chip-Scale Package with 0.8 mm ball pitch.

The SDRAM for OMAP is a JEDEC standard 2.5V core supply, 1.8V/2.5V IO supply, 16 Mb x 16 (256 Mb) low power synchronous Mobile DRAM. It is a 4-bank device with Partial Array Self Refresh and Temperature Compensated Self Refresh function. This is a 133 MHz part with a RAS and CAS of 2,3.

Figure 3-23. OMAP Memory



Power Supply Architecture

Voltage regulation is provided by the PCAP IC. Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are illustrated below.

Table 3-1. Power Distribution 1

Physical name	Logical name(s)	Voltage	Supplies
SW1	VMEM_1.875V	1.875	AP/BP Flash cores, AP flash I/O
	VGPS_1.875V		GPS Baseband
SW2	VOMAP_1.6V	1.725	OMAP Core
SW3	VBOOST_5.5V	5.5	V10, Keypad backlights
V1	VCAM_1.875V	1.875	Camera processors
V2	VA_2.775V	2.775	Audio
V3	VRF_DIG_1.875V	1.875	Harmony
V4	VLVIO_1.875V	1.875	Low voltage I/O
V5	Not used	2.775	PCAP internal components
V6	VRF_TX_2.775V	2.775	Harmony, Rattler, RF TX
V7	VCAMIO_2.775V	2.775	Camera I/O

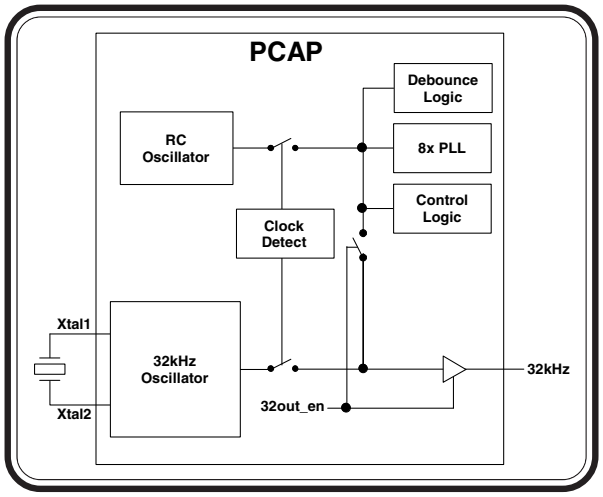
Table 3-2. Power Distribution 2

Physical name	Logical name(s)	Voltage	Supplies
V8	VBLUETH_1.875V	1.875	Bluetooth
V9	VRF_REF_2.475V	2.775	RF Reference
V10	VRF_HV_5V	5	RF HV
VAUX1	VHVIO_2.775V	2.775	Display, high voltage I/O, Harmony
	VGPS_2.775V		GPS RF
VAUX2	VRF_RX_2.775V	2.775	Harmony, Algae, RF RX
VAUX3	VTRI_2.8V	2.8	Transflash
VAUX4	VHOST_3V	3	OMAP-Bluetooth USB
U3206	VMAIN_1.55V	1.55	POG Core
U7700	VCAM_MAIN	2.5/2.85	Camera sensors

Clock Generation

PCAP can generate a 32kHz clock either from an internal RC Oscillator or an external crystal. The internal RC oscillator doesn't provide the stability that the Rainbow requires for optimal performance, therefore, an external 32.768kHz crystal is used.

Figure 3-24. RTC Clock



The PGM2 pin of PCAP is tied to LCELL_BYP, to prevent the internal RC oscillator from being routed to the 32kHz pin under any circumstances. The 32kHz oscillator will run at all times. It is powered by LCELL, a coincell battery that is also used to maintain the real time clock. The phone will only power up when the 32kHz becomes stable.

Audio Circuits

PCAP (U3000)

The PCAP2 IC is an ASIC intended for use in Colorado platform mobile phones. It integrates several functional modules:

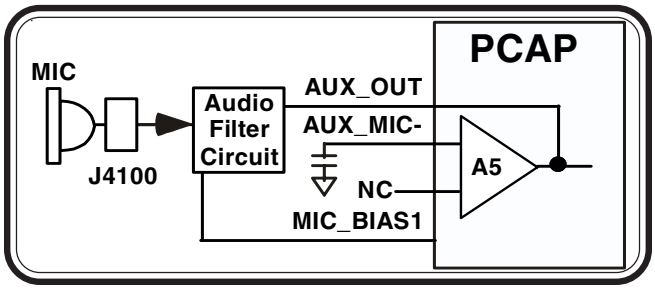
- Voltage regulators of both linear and switching types designed for use in the Colorado power scheme
- Audio codecs and amplifiers
- RS-232 and USB transceivers
- LED controllers for the service light and display/keypad backlights
- Digital interfaces for two controlling processors.

TX Audio

The A1000 supports three microphone input paths identified as Internal Microphone (AUX_MIC-), Headset Microphone (MICIN-), and External Microphone (EXT_MIC). These three inputs are single-ended with respect to VAG. The proper Microphone path is selected by the MUX controller and path gain is programmable at the PGA.

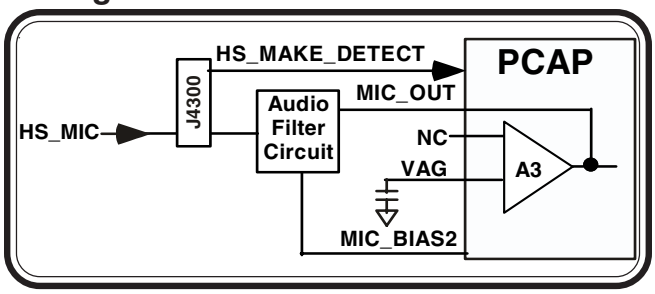
The Internal Microphone is a single ended through - hole part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 and R4101 to AUX_MIC- pin on PCAP, which is the input to the A5 amplifier. The microphone path is tapped off by R4102 to connect the AUX_OUT pin of PCAP, which is the output of the A5 amplifier.

Figure 3-25. Internal Mic Path



The headset microphone path is biased through R4396, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by using R4399 as a pull-up resistor and detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

Figure 3-26. Headset Mic Path



The External Microphone input is connected to the accessory connector for the mobile phone. The path is routed through C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage.

RX Audio

The mobile phone supports four audio output paths. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. These outputs connect to the SPKR+/- amplifier (Handset Earpiece Speaker), the ALERT+/- amplifier (Handset Loudspeaker/Alert Speaker), the EXTOUT amplifier (Accessory connector output), and the ARight/ALeft Out amplifier (Headset Speaker). The single ended Alert mode amplifier (A2) is not used in this design. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins Speaker- and Speaker+, they are routed through R34003 and R34002 respectively, and then connected to the transducer. Off the Speaker-path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to Speaker- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

Figure 3-28. Handset Speaker Path

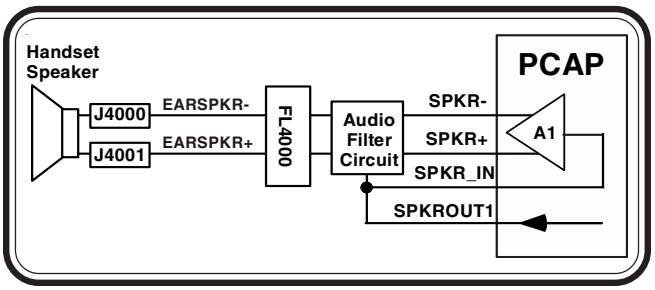
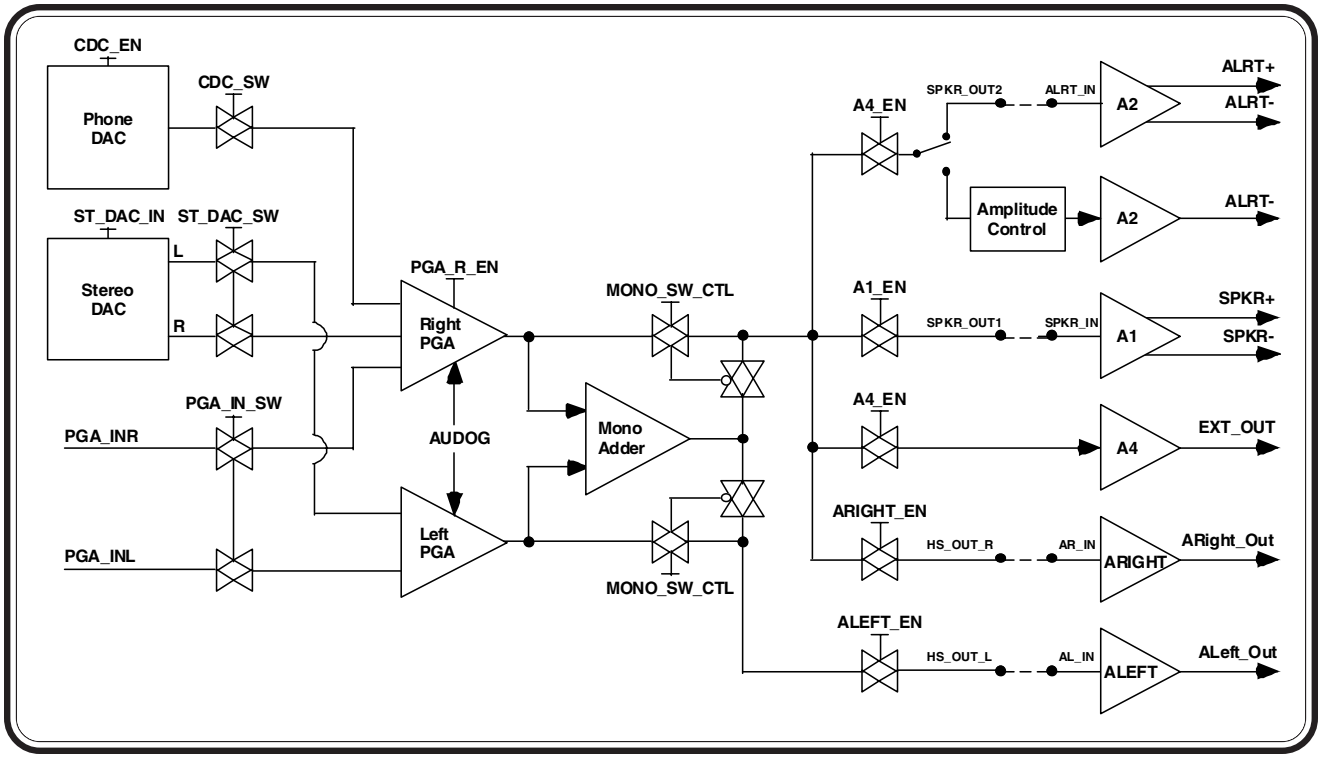
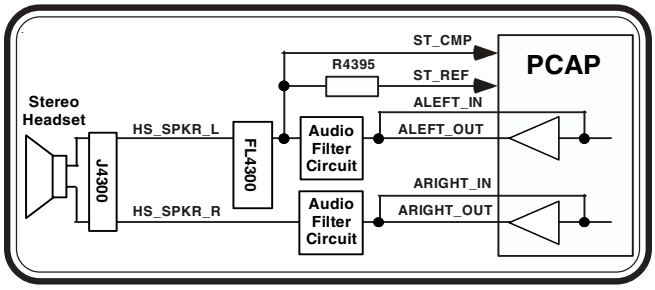


Figure 3-27. RX Audio Block



The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

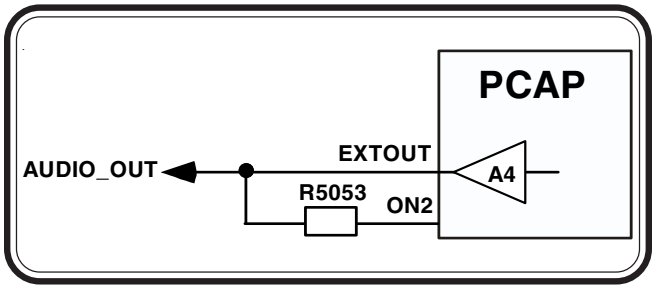
Figure 3-29. Headset Speaker Path



The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R34304 and C4306, R34303 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ARight_Out path, AL_IN is tapped off through C4354 for the inverting input of the audio amp ALEFT.

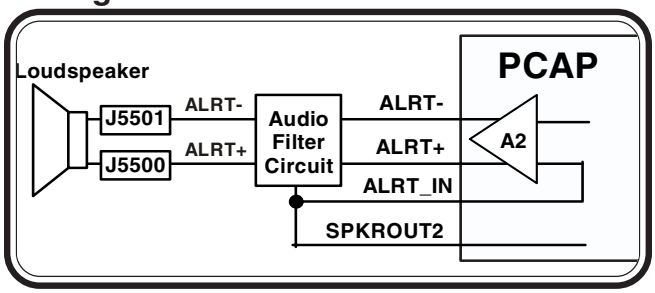
The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT ON/OFF), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

Figure 3-30. External Speaker Path



The Alert Transducer is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

Figure 3-31. Alert Path



Battery Interface

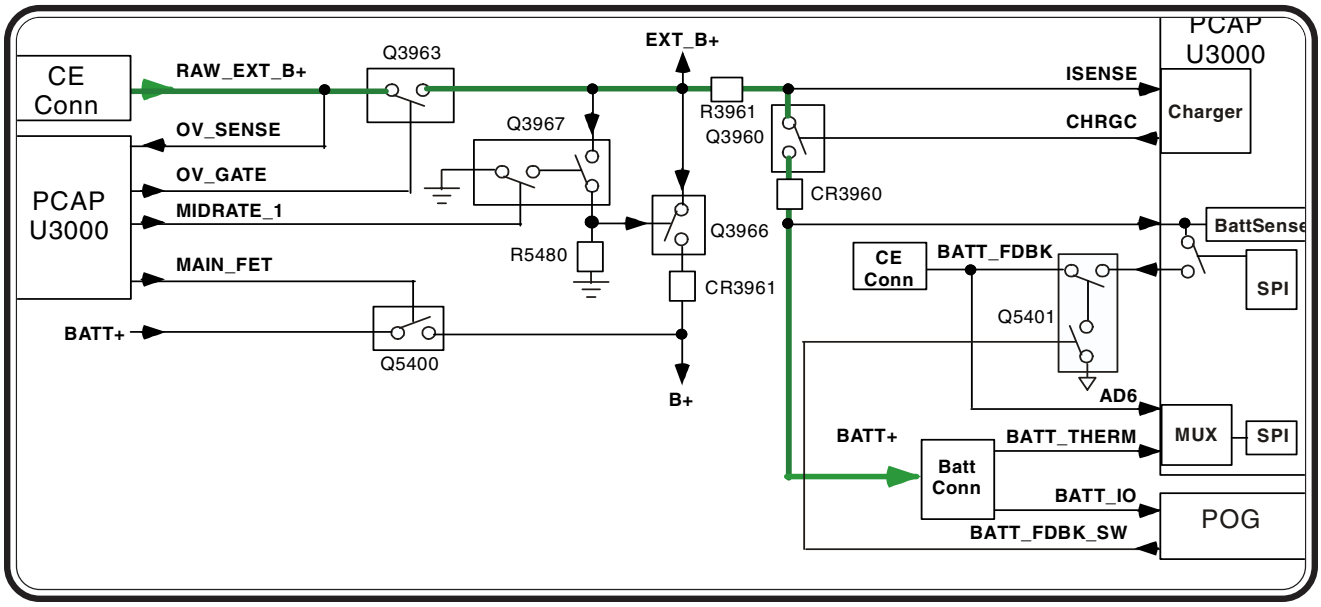
Batteries interface to the main transceiver board via a 4-pin connector (J5400). Motorola approved removable Lithium Ion and Lithium Polymer batteries are supported. Upon power-up, the MCU (through it's integrated One-Wire Interface Module) will interrogate the EPROM located inside the battery package to determine battery characteristics that impact radio and charging operations. Battery validity will also be verified. A thermistor element in the battery package provides temperature feedback.

During normal phone operation, without a charger attached, Q5400 is turned ON so that current can be supplied from the battery to the B+ power node on the transceiver board. When the phone is 'ON', the PCAP IC (U3000) will enable its internal regulators so that transceiver circuitry can be enabled. When the phone is 'OFF', the PCAP IC disables its regulators to disable most active circuitry. In the OFF state, only minimal circuitry will be connected to B+ to minimize 'OFF' state leakage current.

Lithium Ion/Polymer charging is internally supported in the phone. Full rate charging is supported when a valid full rate charger is detected on the accessory interface (J5000). During full rate charging, Q3966 is turned ON so that current can be supplied from the external source to B+. Q5400 will be turned OFF to disconnect the Battery from B+. Based on battery voltage and radio status, charging current will be set by controlling the voltage at the gate of Q3960. A sense resistor (R3961) provides current sense feedback to the charger circuit. Battery charging will be disabled if an invalid battery is detected, if the radio is transmitting, if temperature is too high or too low, or if the battery voltage is too high.

Reduced rate charging is supported when a compatible lower capacity charger is detected on the accessory interface (J5000). Operation with a reduced rate charger will not allow dead battery or 'no battery' operation.

Figure 3-32. Battery Interface Block

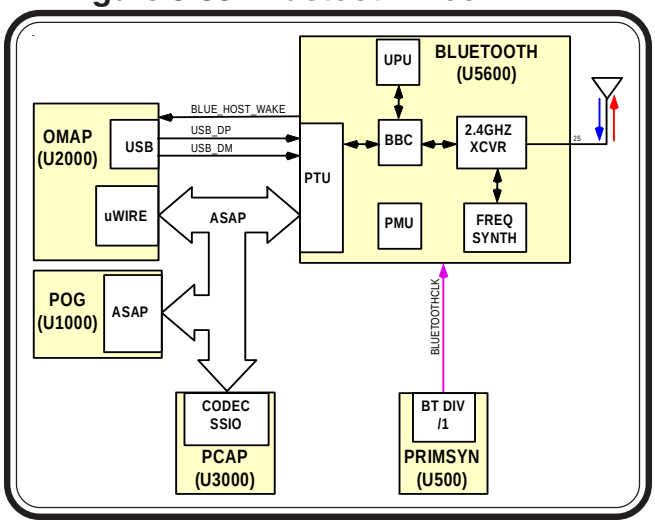


Bluetooth

The Broadcomm 2033 Single Chip Bluetooth solution is being used with the A1000. The BMC2033 is a Bluetooth 1.1 compliant stand alone baseband processor with an integrated 2.4GHz transceiver. The baseband section controls all bluetooth functionality from the physical layers to the HCI layer. The radio section includes PLL, VCO, LNA, PA, upconverter, downconverter, modulator, demodulator, and channel select filtering.

The fractional- N synthesizer can support multiple reference frequencies, including 13MHz and 15.36MHz. The BCM2033 USB module interfaces the OMAP. The ASAP interface communicates between OMAP, POG, PCAP, and BCM2033.

Figure 3-33. Bluetooth Block



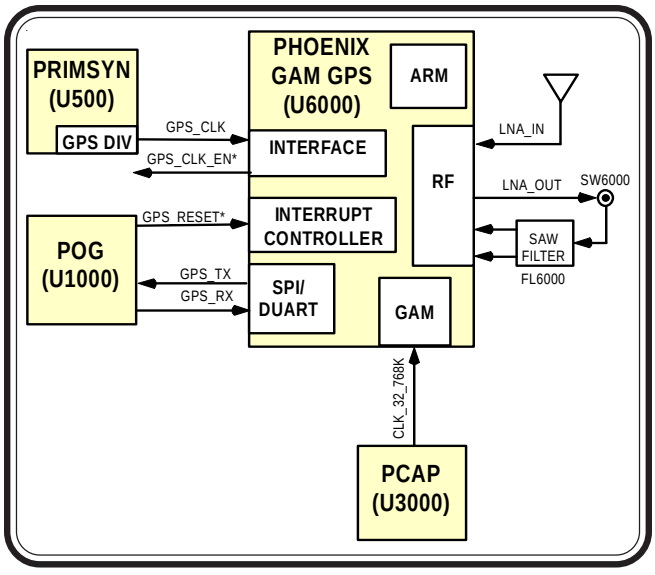
AGPS

The GPS section is based on the Motorola MG4100 single chip GPS receiver 2M SRAM IC (Phoenix) along with One-Track firmware.

The main blocks of the MG4100 IC consist of the GPS Acquisition Module (GAM), a low IF front-end, an ARM7TDMI microprocessor module, a Boot ROM synthesized in gates, and several processor peripherals.

When Phoenix is configured to OneTrack mode, it will search, acquire, and track satellite signals; decode data without host intervention; calculate position, velocity, and time at a 1Hz rate and perform background data decode. It supports both Oneshot and autonmous (stand alone GPS receiver). In reacquisition mode if more than four satellites with signal strength of more than -140dBm are visible, Phoenix will decode satellite data and autonomously compute a position fix without any assistance. The Tim-To-First-Fix will be greatly reduced comparing to Oneshot.

Figure 3-34. Bluetooth Block



The GPS external RF connector (SW6000) allows users to attach a pro install car kit or external GPS attenae. It provides power supply through the signal pin at 2.775V and 15mA current max.

The control signals for the Phoenix IC will be transported via the POG (U1000) 2-wire DUART interface (GPS_TX,GPS_RX).

A 26 MHz clock coming from the PrimSyn is used as a dedicated accurate input clock to acquire GPS fix at weak signal environment and faster TTFF. This clock is powered off when GAM does not require the clock. A RTC clock is used for low power operation.

GPS_CLK_EN signal is used to turn off external reference clock when Phoenix IC switches to CPU and low power mode. Conversely, the clock will be turned on when the software switches to full power mode.

Camera

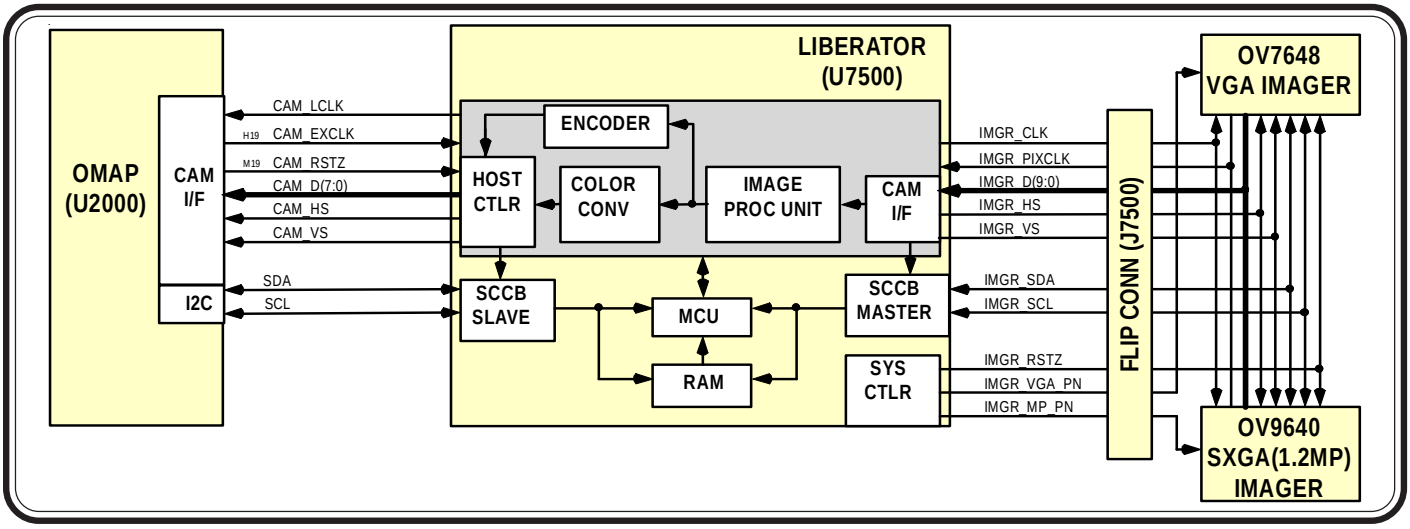
The Imager Module includes two image sensor ICs with the lenses which comprise the optical element and the mechanical mount for the lenses, a flexible interconnection cable, and any required passive components for the image sensors, serial EEPROM and connector.

One image sensor is used for point-to-point video calling and supports an imager format of VGA (640 x 480 pixels). The second image sensor is used for video and photo capture and supports an imager format of 1.2 Mega pixel (1280 x 960). The image sensor produces color image data in the Bayer RGB (Red, Green, Blue) format. The lens system will be a two-element, fixed focal length design. The finished module will have bad pixel data for the both imagers stored in the EEPROM. Imager selection is processed through the system controller module of the Liberator IC.

The Liberator IC is a low-power image processor and encoder, capable of supporting imager sensors of up to 2.0 Mega pixel resolution. The Liberator interfaces directly with the imager and with the OMAP processor and does not require an external memory. The IC is equipped with master/slave 2-wire bidirectional serial bus interfaces and an embedded 8-bit microcontroller. An internal linear 1.8V fixed value regulator is also included in the IC.

The chip is housed in a 49-pin 0.8mm pitch BGA package.

Figure 3-35. Bluetooth Block



Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Electrical Parts List

The following table lists the electrical parts list for the A1000 UMTS/GSM handset.

Table 4-1. Electrical Parts List - Axxx - C20x

Reference Number	Part Number	Description
ANT01	3989625N02	CONTACT
ANT02	3989625N02	CONTACT
ANT03DNP	3989625N02	CONTACT
ANT04DNP	3989625N02	CONTACT
ANT06DNP	3989625N02	CONTACT
ANT5600	3989625N02	CONTACT
ANT5601	3989625N02	CONTACT
ANT6000	3989625N02	CONTACT
ANT6001	3989625N02	CONTACT
C2	0662057M01	RES, 0
C3	2488090Y25	IDCTR, 100nH
C4	2488090Y25	IDCTR, 100nH
C5	2113743N38	CAP, 33pF
C6	2113743N38	CAP, 33pF
C7	2113743N38	CAP, 33pF
C8	2113743N38	CAP, 33pF
C01	2113743M24	CAP, 0.1uF
C10	2186463Z07	CAP, 0.3pF
C100	2113928C04	CAP, 4.7uF
C101	2113928C04	CAP, 4.7uF
C102	2113743N38	CAP, 33pF
C103	2187893N01	CAP, 1.0uF
C104	2187893N01	CAP, 1.0uF
C105	2187893N01	CAP, 1.0uF
C106	2187893N01	CAP, 1.0uF
C107	2187893N01	CAP, 1.0uF
C110	2113743L21	CAP, 1500pF
C111	2113743L41	CAP, .01uF
C112	2113743L21	CAP, 1500pF
C113	2113743L41	CAP, .01uF
C1303DNP	2113743M24	CAP, 0.1uF
C1304DNP	2113743M24	CAP, 0.1uF
C1305DNP	2113743M24	CAP, 0.1uF
C1307DNP	2113743M24	CAP, 0.1uF
C1308DNP	2113743M24	CAP, 0.1uF
C1313DNP	2113743M24	CAP, 0.1uF
C1403DNP	2113743M24	CAP, 0.1uF
C201DNP	2113743N26	CAP, 10pF

Table 4-2. Electrical Parts List - C21x - C50x

Reference Number	Part Number	Description
C213DNP	2113743N26	CAP, 10pF
C30	2113743N38	CAP, 33pF
C31	2188884Y01	CAP, 0.7pF
C33	2113743N26	CAP, 10pF
C35	2113743N03	CAP, 1pF
C37	2113743L41	CAP, .01uF
C200	2187906N01	CAP, 4.7uF
C230	2113743L41	CAP, .01uF
C231	2113743L41	CAP, .01uF
C300	2113928C04	CAP, 4.7uF
C301	2113743N26	CAP, 10pF
C302	2113743N26	CAP, 10pF
C303	2113743N26	CAP, 10pF
C304	2113743L41	CAP, .01uF
C305	2113743L41	CAP, .01uF
C306	2113743N26	CAP, 10pF
C307	2113928C04	CAP, 4.7uF
C308	2113743L17	CAP, 1000pF
C309	2113743L17	CAP, 1000pF
C3007DNP	2113743M24	CAP, 0.1uF
C3008DNP	2113743M24	CAP, 0.1uF
C310	2113743N38	CAP, 33pF
C311	2113743N38	CAP, 33pF
C312	2113743N01	CAP, 0.5pF
C313	2113743M24	CAP, 0.1uF
C3651DNP	2113743N30	CAP, 15pF
C3652DNP	2113743N30	CAP, 15pF
C400	2113928C04	CAP, 4.7uF
C401	2113946D02	CAP, 1.0uF
C402	2113946D02	CAP, 1.0uF
C403	2113743N26	CAP, 10pF
C404	2113743N26	CAP, 10pF
C405	2113743N40	CAP, 39pF
C406	2113743N40	CAP, 39pF
C407	2113946D02	CAP, 1.0uF
C408	2113743N07	CAP, 1.5pF
C4003DNP	2113743N38	CAP, 33pF
C4004DNP	2113743N38	CAP, 33pF
C4307DNP	2113743N38	CAP, 33pF
C4352DNP	2113743N38	CAP, 33pF
C4389DNP	2113928P04	CAP, 1.0uF
C4402DNP	2113743N38	CAP, 33pF
C500	2113743N34	CAP, 22pF
C501	2113743L41	CAP, .01uF

Table 4-3. Electrical Parts List - C50x - C61x

Reference Number	Part Number	Description
C502	2113743L41	CAP, .01uF
C503	2113743L41	CAP, .01uF
C504	2113946D02	CAP, 1.0uF
C505	2113946D02	CAP, 1.0uF
C506	2113743N38	CAP, 33pF
C507	2113743N44	CAP, 56pF
C508	2113743N44	CAP, 56pF
C509	2113946D02	CAP, 1.0uF
C510	2113743N26	CAP, 10pF
C511	2113743N38	CAP, 33pF
C5100DNP	2113928N01	CAP, 0.1uF
C5250DNP	2113743L25	CAP, 2200pF
C5251DNP	2113743L25	CAP, 2200pF
C5252DNP	2113743N38	CAP, 33pF
C5253DNP	2113743N38	CAP, 33pF
C530	2113743N44	CAP, 56pF
C531	2113743N44	CAP, 56pF
C532	2113743N42	CAP, 47pF
C533	2113743N50	CAP, 100pF
C534	2113743L33	CAP, 4700pF
C535	2113743L01	CAP, 220pF
C560	2113743N44	CAP, 56pF
C561	2113743N44	CAP, 56pF
C562	2113743L25	CAP, 2200pF
C563	2109622N09	CAP, 3300pF
C564	2113741A53	CAP, .022uF
C565	2113743L09	CAP, 470pF
C567	2113743L13	CAP, 680pF
C568	2113741A45	CAP, .01uF
C569	2113743N52	CAP, 120pF
C570	2113743N26	CAP, 10pF
C571	2113743L01	CAP, 220pF
C600	2113743L41	CAP, .01uF
C601	2113743N26	CAP, 10pF
C602	2113743L41	CAP, .01uF
C603	2113743N38	CAP, 33pF
C604	2113743L01	CAP, 220pF
C605	2113743N26	CAP, 10pF
C606	2113743L41	CAP, .01uF
C607	2113743N38	CAP, 33pF
C608	2113928C04	CAP, 4.7uF
C609	2113928C04	CAP, 4.7uF
C610	2113743N17	CAP, 4.3pF
C611	2113743N17	CAP, 4.3pF

Table 4-4. Electrical Parts List - C61x - C10xx

Reference Number	Part Number	Description
C613	2113743N26	CAP, 10pF
C614	2113743N38	CAP, 33pF
C615	2113743N38	CAP, 33pF
C616	2113743N38	CAP, 33pF
C617	2113928C12	CAP, 10uF
C620	2113743N26	CAP, 10pF
C621	2113743N26	CAP, 10pF
C622	2113743N09	CAP, 2pF
C630	2113743N15	CAP, 3.6pF
C631	2113743N15	CAP, 3.6pF
C800	2113740F41	CAP, 39pF
C801	2113928C04	CAP, 4.7uF
C802	2187906N01	CAP, 4.7uF
C803	2113743E20	CAP, 0.1uF
C805	2113743E20	CAP, 0.1uF
C806	2113743E20	CAP, 0.1uF
C807	2113743N26	CAP, 10pF
C810	2113743N40	CAP, 39pF
C811	2113743N40	CAP, 39pF
C821	2113743N03	CAP, 1pF
C830	2113743N02	CAP, 0.75pF
C831	2113743N16	CAP, 3.9pF
C832	2113743N22	CAP, 6.8pF
C833	2113743N10	CAP, 2.2pF
C840	2113743N26	CAP, 10pF
C880	2113743L41	CAP, .01uF
C881	2113743L41	CAP, .01uF
C1000	2113743M24	CAP, 0.1uF
C1001	2113743M24	CAP, 0.1uF
C1002	2113743M24	CAP, 0.1uF
C1003	2113743M24	CAP, 0.1uF
C1004	2113743M24	CAP, 0.1uF
C1005	2113743M24	CAP, 0.1uF
C1006	2113743M24	CAP, 0.1uF
C1007	2113743M24	CAP, 0.1uF
C1008	2113743M24	CAP, 0.1uF
C1009	2113743M24	CAP, 0.1uF
C1010	2113743M24	CAP, 0.1uF
C1011	2113743M24	CAP, 0.1uF
C1012	2113743M24	CAP, 0.1uF
C1013	2113743M24	CAP, 0.1uF
C1014	2113743M24	CAP, 0.1uF
C1015	2113743M24	CAP, 0.1uF
C1016	2113743M24	CAP, 0.1uF

Table 4-5. Electrical Parts List - C10xx - C20xx

Reference Number	Part Number	Description
C1017	2113743M24	CAP, 0.1uF
C1018	2113743M24	CAP, 0.1uF
C1019	2113743M24	CAP, 0.1uF
C1020	2113743M24	CAP, 0.1uF
C1021	2113743M24	CAP, 0.1uF
C1022	2113743M24	CAP, 0.1uF
C1023	2113743M24	CAP, 0.1uF
C1024	2113743M24	CAP, 0.1uF
C1025	2113743M24	CAP, 0.1uF
C1026	2113743M24	CAP, 0.1uF
C1027	2113743M24	CAP, 0.1uF
C1028	2113743M24	CAP, 0.1uF
C1029	2113743M24	CAP, 0.1uF
C1030	2113743M24	CAP, 0.1uF
C1100	2113743N38	CAP, 33pF
C1110	2113743M24	CAP, 0.1uF
C1120	2113743M24	CAP, 0.1uF
C1122	2113743L41	CAP, .01uF
C1140	2113743M24	CAP, 0.1uF
C1300	2113743M24	CAP, 0.1uF
C1302	2113743M24	CAP, 0.1uF
C1306	2113743M24	CAP, 0.1uF
C1309	2113743M24	CAP, 0.1uF
C1310	2113743M24	CAP, 0.1uF
C1312	2113743M24	CAP, 0.1uF
C1400	2113743M24	CAP, 0.1uF
C1401	2113743M24	CAP, 0.1uF
C1402	2113743M24	CAP, 0.1uF
C1404	2113743M24	CAP, 0.1uF
C1405	2113743M24	CAP, 0.1uF
C1406	2113743M24	CAP, 0.1uF
C1407	2113743M24	CAP, 0.1uF
C2001	2113743N30	CAP, 15pF
C2002	2113743N30	CAP, 15pF
C2003	2113928N01	CAP, 0.1uF
C2004	2113928N01	CAP, 0.1uF
C2005	2113928N01	CAP, 0.1uF
C2006	2113928N01	CAP, 0.1uF
C2007	2187906N01	CAP, 4.7uF
C2008	2113928N01	CAP, 0.1uF
C2009	2113928N01	CAP, 0.1uF
C2010	2113928N01	CAP, 0.1uF
C2011	2113928N01	CAP, 0.1uF
C2012	2113928N01	CAP, 0.1uF

Table 4-6. Electrical Parts List - C20xx - C30xx

Reference Number	Part Number	Description
C2013	2113928N01	CAP, 0.1uF
C2014	2113928N01	CAP, 0.1uF
C2015	2113928N01	CAP, 0.1uF
C2016	2113928N01	CAP, 0.1uF
C2017	2113928N01	CAP, 0.1uF
C2018	2113928N01	CAP, 0.1uF
C2019	2113928N01	CAP, 0.1uF
C2020	2113743M24	CAP, 0.1uF
C2021	2113928N01	CAP, 0.1uF
C2022	2113928N01	CAP, 0.1uF
C2023	2113743N34	CAP, 22pF
C2024	2113743N34	CAP, 22pF
C2025	2113928N01	CAP, 0.1uF
C2026	2113743M24	CAP, 0.1uF
C2027	2113928C12	CAP, 10uF
C2028	2113928N01	CAP, 0.1uF
C2030	2113928N01	CAP, 0.1uF
C2031	2113743N38	CAP, 33pF
C2032	2113928N01	CAP, 0.1uF
C2033	2113928N01	CAP, 0.1uF
C2034	2113928N01	CAP, 0.1uF
C2035	2113743M24	CAP, 0.1uF
C2046	2113743N34	CAP, 22pF
C2068	2113928N01	CAP, 0.1uF
C2069	2113928N01	CAP, 0.1uF
C2070	2113928N01	CAP, 0.1uF
C2090	2113928N01	CAP, 0.1uF
C2094	2113928N01	CAP, 0.1uF
C2097	2113928N01	CAP, 0.1uF
C2098	2113928N01	CAP, 0.1uF
C2099	2113928C12	CAP, 10uF
C2302	2113928N01	CAP, 0.1uF
C2303	2113928N01	CAP, 0.1uF
C2306	2113928N01	CAP, 0.1uF
C2350	2113928N01	CAP, 0.1uF
C2351	2113928N01	CAP, 0.1uF
C3000	2187906N01	CAP, 4.7uF
C3001	2113928C12	CAP, 10uF
C3003	2113928N01	CAP, 0.1uF
C3005	2113743M24	CAP, 0.1uF
C3006	2187906N01	CAP, 4.7uF
C3020	2187906N01	CAP, 4.7uF
C3021	2113928C12	CAP, 10uF
C3022	2113928N01	CAP, 0.1uF

Table 4-7. Electrical Parts List - C30xx - C39xx

Reference Number	Part Number	Description
C3023	2113928C12	CAP, 10uF
C3024	2187906N01	CAP, 4.7uF
C3025	2113743M24	CAP, 0.1uF
C3026	2113946D02	CAP, 1.0uF
C3027	2187906N01	CAP, 4.7uF
C3028	2113743N38	CAP, 33pF
C3050	2113946D02	CAP, 1.0uF
C3060	2113946D02	CAP, 1.0uF
C3100	2113928C12	CAP, 10uF
C3101	2113928C12	CAP, 10uF
C3102	2113928N01	CAP, 0.1uF
C3105	2113743M24	CAP, 0.1uF
C3106	2187906N01	CAP, 4.7uF
C3150	2113946D02	CAP, 1.0uF
C3205	2187906N01	CAP, 4.7uF
C3206	2113928N01	CAP, 0.1uF
C3207	2113928C12	CAP, 10uF
C3208	2113928N01	CAP, 0.1uF
C3209	2113946D02	CAP, 1.0uF
C3210	2113743N34	CAP, 22pF
C3211	2113743N50	CAP, 100pF
C3250	2113946D02	CAP, 1.0uF
C3300	2113928C03	CAP, 1.0uF
C3350	2113946D02	CAP, 1.0uF
C3400	2113928C12	CAP, 10uF
C3403	2113928N01	CAP, 0.1uF
C3450	2113946D02	CAP, 1.0uF
C3550	2113928E03	CAP, 2.2uF
C3560	2113928C12	CAP, 10uF
C3600	2113928E03	CAP, 2.2uF
C3654	2113946D02	CAP, 1.0uF
C3655	2113743N38	CAP, 33pF
C3656	2113743N38	CAP, 33pF
C3700	2113928C12	CAP, 10uF
C3801	2113946D02	CAP, 1.0uF
C3850	2113946D02	CAP, 1.0uF
C3851	2113946D02	CAP, 1.0uF
C3950	2113946D02	CAP, 1.0uF
C3951	2187906N01	CAP, 4.7uF
C3960	2113928C12	CAP, 10uF
C3962	2113743M24	CAP, 0.1uF
C3975	2113946D02	CAP, 1.0uF
C3983	2113743N30	CAP, 15pF
C3984	2113743N30	CAP, 15pF

Table 4-8. Electrical Parts List - C41xx - C49xx

Reference Number	Part Number	Description
C4100	2113743E07	CAP, .022uF
C4102	2113928P04	CAP, 1.0uF
C4103	2113743N38	CAP, 33pF
C4104	2113743N26	CAP, 10pF
C4200	2187906N01	CAP, 4.7uF
C4203	2113743N38	CAP, 33pF
C4204	2113743N38	CAP, 33pF
C4208	2113743N38	CAP, 33pF
C4211	2113743N38	CAP, 33pF
C4212	2113928N01	CAP, 0.1uF
C4213	2113928N01	CAP, 0.1uF
C4215	2113743N38	CAP, 33pF
C4217	2113743N38	CAP, 33pF
C4218	2113743N38	CAP, 33pF
C4219	2113928N01	CAP, 0.1uF
C4300	2113743N38	CAP, 33pF
C4301	2113743N38	CAP, 33pF
C4302	2113743N38	CAP, 33pF
C4306	2113928Z11	CAP, 22uF
C4356	2113928Z11	CAP, 22uF
C4392	2113743N40	CAP, 39pF
C4393	2113743N40	CAP, 39pF
C4450	2113946D02	CAP, 1.0uF
C4502	2187906N01	CAP, 4.7uF
C4550	2113743L33	CAP, 4700pF
C4551	2113928N01	CAP, 0.1uF
C4900	2113928N01	CAP, 0.1uF
C4901	2113928N01	CAP, 0.1uF
C4910	2113928N01	CAP, 0.1uF
C4911	2113743L41	CAP, .01uF
C4912	2113743L41	CAP, .01uF
C4913	2113928N01	CAP, 0.1uF
C4914	2113743M24	CAP, 0.1uF
C4916	2113743N38	CAP, 33pF
C4917	2113743N38	CAP, 33pF
C4918	2113743N38	CAP, 33pF
C4920	2113928N01	CAP, 0.1uF
C4921	2113743N38	CAP, 33pF
C4922	2113743N38	CAP, 33pF
C4923	2113743N28	CAP, 12pF
C4930	2113743L21	CAP, 1500pF
C4931	2113928N01	CAP, 0.1uF
C4933	2113743N38	CAP, 33pF
C4934	2113743N28	CAP, 12pF

Table 4-9. Electrical Parts List - C49xx - C54xx

Reference Number	Part Number	Description
C4935	2113743N38	CAP, 33pF
C4936	2113743N28	CAP, 12pF
C4940	2113743L13	CAP, 680pF
C4941	2113928N01	CAP, 0.1uF
C4943	2113743N38	CAP, 33pF
C4944	2113743N38	CAP, 33pF
C4945	2113743N38	CAP, 33pF
C4950	2113743L41	CAP, .01uF
C4955	2113743L41	CAP, .01uF
C4960	2113928N01	CAP, 0.1uF
C4961	2113928N01	CAP, 0.1uF
C4962	2113743N38	CAP, 33pF
C4963	2113743N38	CAP, 33pF
C5000	2113743M24	CAP, 0.1uF
C5001	2113928N01	CAP, 0.1uF
C5002	2113743N38	CAP, 33pF
C5003	2113743N38	CAP, 33pF
C5004	2113743N38	CAP, 33pF
C5005	2113743N38	CAP, 33pF
C5006	2113743N38	CAP, 33pF
C5053	2113928A01	CAP, 1.0uF
C5101	2113743N38	CAP, 33pF
C5102	2113743N38	CAP, 33pF
C5103	2113928N01	CAP, 0.1uF
C5104	2113743N38	CAP, 33pF
C5105	2113928N01	CAP, 0.1uF
C5106	2113743N38	CAP, 33pF
C5107	2113928N01	CAP, 0.1uF
C5108	2113743N38	CAP, 33pF
C5109	2113928N01	CAP, 0.1uF
C5110	2113928N01	CAP, 0.1uF
C5111	2113928N01	CAP, 0.1uF
C5112	2113743L41	CAP, .01uF
C5221	2113928P04	CAP, 1.0uF
C5222	2113928P04	CAP, 1.0uF
C5224	2188468Y01	CAP, 1uF
C5225	2113945B02	CAP, .01uF
C5226	2113944A31	CAP, 33pF
C5240	2113743L50	CAP, .033uF
C5241	2113928P04	CAP, 1.0uF
C5400	2187906N01	CAP, 4.7uF
C5401	2113928N01	CAP, 0.1uF
C5402	2187906N01	CAP, 4.7uF
C5403	2113743N38	CAP, 33pF

Table 4-10. Electrical Parts List - C54xx - C75xx

Reference Number	Part Number	Description
C5404	2113928N01	CAP, 0.1uF
C5405	2113928N01	CAP, 0.1uF
C5406	2113743N38	CAP, 33pF
C5500	2113928N01	CAP, 0.1uF
C5501	2113743N38	CAP, 33pF
C5502	2113743N38	CAP, 33pF
C5503	2113743N38	CAP, 33pF
C5504	2113743N38	CAP, 33pF
C5505	2113743N38	CAP, 33pF
C5506	2113928N01	CAP, 0.1uF
C5507	2113928N01	CAP, 0.1uF
C5602	2113928N01	CAP, 0.1uF
C5603	2113928N01	CAP, 0.1uF
C5800	2113743M24	CAP, 0.1uF
C5801	2113743M24	CAP, 0.1uF
C5805DNP	2113743N38	CAP, 33pF
C6000	2113928N01	CAP, 0.1uF
C6001	2113743N28	CAP, 12pF
C6002	2113743L11	CAP, 560pF
C6003	2113743L25	CAP, 2200pF
C6004	2113743N28	CAP, 12pF
C6005	2113743N28	CAP, 12pF
C6006	2113743N32	CAP, 18pF
C6007	2113743N28	CAP, 12pF
C6008	2113743Q03	CAP, 1pF
C6009	2113743L41	CAP, .01uF
C6010	2113928N01	CAP, 0.1uF
C6012	2113928N01	CAP, 0.1uF
C6013	2113743L41	CAP, .01uF
C6014	2113928N01	CAP, 0.1uF
C6015	2113743L17	CAP, 1000pF
C6016	2113743L17	CAP, 1000pF
C6017	2113928N01	CAP, 0.1uF
C6018	2113743L41	CAP, .01uF
C6011DNP	2113928N01	CAP, 0.1uF
C6019DNP	2113928N01	CAP, 0.1uF
C6020	2113743N28	CAP, 12pF
C6021DNP	2113928N01	CAP, 0.1uF
C6030	2113743M24	CAP, 0.1uF
C7500	2113946D02	CAP, 1.0uF
C7501	2113946D02	CAP, 1.0uF
C7502	2113928N01	CAP, 0.1uF
C7503	2113928N01	CAP, 0.1uF
C7504	2113928N01	CAP, 0.1uF

Table 4-11. Electrical Parts List - C75xx - E20x

Reference Number	Part Number	Description
C7505	2113928N01	CAP, 0.1uF
C7507	2113928N01	CAP, 0.1uF
C7508	2113928N01	CAP, 0.1uF
C7701	2113928C12	CAP, 10uF
C7702	2113743N38	CAP, 33pF
C7703	2113928C12	CAP, 10uF
C7704	2113928N01	CAP, 0.1uF
C21058	2113928N01	CAP, 0.1uF
C21059	2113928N01	CAP, 0.1uF
C21060	2113928N01	CAP, 0.1uF
C21061	2113928N01	CAP, 0.1uF
C21062	2113928N01	CAP, 0.1uF
C21063	2113743L41	CAP, .01uF
C7506DNP	2113743N38	CAP, 33pF
C808DNP	2113743N26	CAP, 10pF
C820DNP	2113743N10	CAP, 2.2pF
C835DNP	2113743N14	CAP, 3.3pF
CR3000	4809924D18	RB520S-30
CR3020	4809924D18	RB520S-30
CR5240	4809924D18	RB520S-30
CR5401	4809948D42	RB751V40
D622	4809948D37	BA892
D2300	4809924D18	RB520S-30
D3100	4809924D18	RB520S-30
D3963	4809653F07	MBRM120ET3
D3964	4809653F07	MBRM120ET3
D3961DNP	4809924D24	IR1H40CSP
D3962DNP	4809924D24	IR1H40CSP
E1	SHORT_BAR0_61	SHORTING_BAR
E2	SHORT_BAR0_61	SHORTING_BAR
E3	SHORT_BAR0_61	SHORTING_BAR
E4	SHORT_BAR0_61	SHORTING_BAR
E5	SHORT_BAR0_61	SHORTING_BAR
E30	0662057M01	RES, 0
E100	SHORT_RES0402	SHORT
E101	SHORT_RES0402	SHORT
E102	SHORT_RES0402	SHORT
E103	0662057M01	RES, 0
E104	0662057M01	RES, 0
E105	0662057M01	RES, 0
E106	0662057M01	RES, 0
E201	SHORT_RES0402	SHORT
E203	SHORT_RES0201	SHORT
E204	SHORT_RES0201	SHORT

Table 4-12. Electrical Parts List - E20x - E60xx

Reference Number	Part Number	Description
E205	SHORT_RES0201	SHORT
E206	SHORT_RES0402	SHORT
E207	SHORT_RES0402	SHORT
E208	SHORT_RES0402	SHORT
E209	SHORT_RES0402	SHORT
E210	SHORT_RES0402	SHORT
E211	SHORT_RES0402	SHORT
E213	SHORT_RES0402	SHORT
E300	0662057M01	RES, 0
E301	0662057M01	RES, 0
E302	SHORT_RES0402	SHORT
E403	SHORT_RES0201	SHORT
E404	SHORT_RES0201	SHORT
E502	0662057M01	RES, 0
E801	SHORT_RES0402	SHORT
E2021	SHORT_RES0402	SHORT
E3960	SHORT_RES0402	SHORT
E4210	SHORT_RES0201	SHORT
E5200	SHORT_RES0201	SHORT
E5201	SHORT_RES0201	SHORT
E5202	SHORT_RES0201	SHORT
E5203	SHORT_RES0201	SHORT
E5204	SHORT_RES0201	SHORT
E5205	SHORT_RES0201	SHORT
E5206	SHORT_RES0201	SHORT
E5207	SHORT_RES0201	SHORT
E5208	SHORT_RES0201	SHORT
E5209	SHORT_RES0201	SHORT
E5210	SHORT_RES0201	SHORT
E5211	SHORT_RES0201	SHORT
E5212	SHORT_RES0201	SHORT
E5213	SHORT_RES0201	SHORT
E5214	SHORT_RES0201	SHORT
E5215	SHORT_RES0201	SHORT
E5217	SHORT_RES0201	SHORT
E5601	0662057M01	RES, 0
E5603	0662057M01	RES, 0
E5607	0662057M01	RES, 0
E5609	SHORT_RES0402	SHORT
E5610	SHORT_RES0402	SHORT
E5611	SHORT_RES0402	SHORT
E5613	SHORT_RES0402	SHORT
E6001	2488090Y19	IDCTR, 33nH
E6002	2488090Y19	IDCTR, 33nH

Table 4-13. Electrical Parts List - F1 - L42xx

Reference Number	Part Number	Description
F1	FIDUCIAL_CE	CE_FIDUCIAL
F2	FIDUCIAL_CE	CE_FIDUCIAL
F3	FIDUCIAL_CE	CE_FIDUCIAL
F4	FIDUCIAL_CE	CE_FIDUCIAL
FL1	4889729N03	FEM3203_ES6D
FL30	9109674L20	S0351
FL40	9109674L21	CF61A5601
FL80	9109674L17	74L17
FL100	9188695K05	CSPRC032AG
FL300	9109239M38	SAFSD2G14
FL4000	4889526L15	CSPEMI201AG
FL4300	4889526L14	CSPEMI202AG
FL6000	9180310L36	SAW_1575_42MHZ
FL6001	9189312N01	B9000
J4100	5085600J01	SPKR
J4200	3989946N01	CONN_P
J4210	3989946N01	CONN_P
J4300	0989675N03	CONN_J
J5000	0987636K08	CONN_J
J5100	0987817K02	CONN_J
J5101	0989921N01	CONN_J
J5200	0988866N01	CONN_J
J5400	3986666K01	CONTACT
J5500	3989654N02	CONTACT
J5800	3989655N02	CONTACT
J7500	0988866N01	CONN_J
L6	2487319K01	IDCTR, 1.0nH
L1DNP	2404574Z09	IDCTR, 100nH
L30	2488090Y09	IDCTR, 4.7nH
L31	2488090Y09	IDCTR, 4.7nH
L32	2488090Y01	IDCTR, 1nH
L34	2488090Y06	IDCTR, 2.7nH
L230	2488090Y24	IDCTR, 82nH
L231	2488090Y24	IDCTR, 82nH
L310	2488090Y06	IDCTR, 2.7nH
L312	2488090Y06	IDCTR, 2.7nH
L409	2488090Y11	IDCTR, 6.8nH
L3000	2485063F04	IDCTR, 10uH
L3020	2485063F04	IDCTR, 10uH
L3100	2487356Y01	IDCTR, 10uH
L3206	2485063F04	IDCTR, 10uH
L408DNP	2488090Y04	IDCTR, 1.8nH
L4210DNP	2488090Y20	IDCTR, 39nH
L4211DNP	2488090Y15	IDCTR, 15nH

Table 4-14. Electrical Parts List - L42xx - R10xx

Reference Number	Part Number	Description
L4212DNP	2488090Y15	IDCTR, 15nH
L5600DNP	2409154M08	IDCTR, 3.9nH
L5601DNP	2409154M08	IDCTR, 3.9nH
L604	2488090Y25	IDCTR, 100nH
L610	2488090Y08	IDCTR, 3.9nH
L612	2488090Y07	IDCTR, 3.3nH
L620	2488090Y13	IDCTR, 10nH
L630	2488090Y18	IDCTR, 27nH
L632	2488090Y08	IDCTR, 3.9nH
L820	2488090Y05	IDCTR, 2.2nH
L831	2488090Y12	IDCTR, 8.2nH
L834	2488090Y05	IDCTR, 2.2nH
L4399	2409646M13	IDCTR, 39nH
L4400	2409154M71	IDCTR, 47.0nH
L4401	2409154M71	IDCTR, 47.0nH
L5221	2587957N04	IDCTR, 22uH
L6000	2488090Y17	IDCTR, 22nH
L6001	2488090Y19	IDCTR, 33nH
L6002	2488090Y07	IDCTR, 3.3nH
L6003	2488090Y19	IDCTR, 33nH
L7500	2462587Q46	IDCTR, 820nH
L7501DNP	2488090Y20	IDCTR, 39nH
M001	0987378K01	SWITCH
M5400	0990107N01	CONN_J
Q1001	4809579E02	2SK1830
Q2021DNP	4809579E02	2SK1830
Q3000	4809807C42	SI8405DB
Q3001	4809807C42	SI8405DB
Q3403	4804616R01	MBT35200MT1
Q3560	4804616R01	MBT35200MT1
Q3703	4804616R01	MBT35200MT1
Q3960	4862830F01	SI8401DB
Q3961	4862830F01	SI8401DB
Q3963	4809807C42	SI8405DB
Q3964	4862830F01	SI8401DB
Q3981	4862830F01	SI8401DB
Q5240	4809579E58	FDG6332C
Q5403DNP	4809579E58	FDG6332C
R1	2113743N62	CAP, 6pF
R01DNP	0662057M01	RES, 0
R1004DNP	0662057N23	RES, 100K
R1005DNP	0662057N23	RES, 100K
R1020DNP	0662057M76	RES, 1.2K
R1021DNP	0662057M76	RES, 1.2K

Table 4-15. Electrical Parts List - R10xx - R5xx

Reference Number	Part Number	Description
R1022DNP	0662057M76	RES, 1.2K
R1030DNP	0662057M76	RES, 1.2K
R1031DNP	0662057M76	RES, 1.2K
R1064DNP	0662057M01	RES, 0
R111	0662057M78	RES, 1.5K
R113	0662057M78	RES, 1.5K
R1105DNP	0662057M01	RES, 0
R1120DNP	0662057M98	RES, 10K
R1150DNP	0662057M98	RES, 10K
R130	0662057M01	RES, 0
R131DNP	0662057M01	RES, 0
R200	0662057M40	RES, 39
R201	2488090Y07	IDCTR, 3.3nH
R2021DNP	0662057N23	RES, 100K
R202DNP	0662057M01	RES, 0
R203DNP	0662057M01	RES, 0
R213	0662057M01	RES, 0
R212DNP	0662057M01	RES, 0
R214DNP	0662057M01	RES, 0
R2300DNP	0662057M01	RES, 0
R32	0662057M86	RES, 3.3K
R33	0662057M81	RES, 2K
R3205DNP	0662057M01	RES, 0
R405	0662057M70	RES, 680
R406	0662057M70	RES, 680
R501	0662057M01	RES, 0
R509	0662057M50	RES, 100
R510	2113743N38	CAP, 33pF
R511	0662057M01	RES, 0
R513	0662057M01	RES, 0
R530	0662057M64	RES, 390
R531	0662057M70	RES, 680
R532	0662057M78	RES, 1.5K
R533	0662057M74	RES, 1K
R560	0662057M64	RES, 390
R561	0662057N09	RES, 27K
R562	0662057M78	RES, 1.5K
R563	0662057M56	RES, 180
R564	0662057M62	RES, 330
R565	0662057M62	RES, 330
R566	0662057M68	RES, 560
R567	0662057M82	RES, 2.2K
R568	0662057M88	RES, 3.9K
R570	0662057M01	RES, 0

Table 4-16. Electrical Parts List - R6xx - R20xx

Reference Number	Part Number	Description
R622	0662057M98	RES, 10K
R801	0662057M01	RES, 0
R810	0662057M51	RES, 110
R811	0662057M51	RES, 110
R880	0662057M66	RES, 470
R1000	0662057M01	RES, 0
R1001	0662057M01	RES, 0
R1003	0662057M01	RES, 0
R1023	0662057M76	RES, 1.2K
R1040	0662057M01	RES, 0
R1041	0662057M01	RES, 0
R1042	0662057M01	RES, 0
R1051	0662057M01	RES, 0
R1058	0662057M01	RES, 0
R1101	0662057M01	RES, 0
R1102	0662057M01	RES, 0
R1103	0662057M01	RES, 0
R1122	0662057M98	RES, 10K
R1123	0662057N23	RES, 100K
R1124	0662057N23	RES, 100K
R1127	0662057N30	RES, 200K
R1128	0662057N23	RES, 100K
R1129	0662057N23	RES, 100K
R1130	0662057M98	RES, 10K
R1300	0662057M01	RES, 0
R1302	0662057M01	RES, 0
R1303	0662057M01	RES, 0
R1400	0662057M01	RES, 0
R1402	0662057M01	RES, 0
R2002	0662057M98	RES, 10K
R2003	0662057M98	RES, 10K
R2006	0662057M98	RES, 10K
R2007	0662057M01	RES, 0
R2010	0662057M01	RES, 0
R2011	0662057M01	RES, 0
R2012	0662057M01	RES, 0
R2013	0662057M01	RES, 0
R2020	0662057M01	RES, 0
R2022	0662057M01	RES, 0
R2026	0609591M37	RESNET, 10K
R2030	0662057M98	RES, 10K
R2040	0662057N23	RES, 100K
R2041	0662057M35	RES, 24
R2042	0662057M35	RES, 24

Table 4-17. Electrical Parts List - R20xx - R37xx

Reference Number	Part Number	Description
R2043	0662057N03	RES, 15K
R2044	0662057N03	RES, 15K
R2045	0662057N23	RES, 100K
R2046	0662057V24	RES, 75K
R2047	0662057V35	RES, 200K
R2055	0662057M98	RES, 10K
R2059	0662057M82	RES, 2.2K
R2097	0662057M26	RES, 10
R2301	0662057M98	RES, 10K
R2302	0662057M98	RES, 10K
R2303	0662057M98	RES, 10K
R2304	0662057M98	RES, 10K
R2310	0662057M01	RES, 0
R2311	0662057M01	RES, 0
R2402	0662057N23	RES, 100K
R2403	0662057V35	RES, 200K
R2410	0662057M01	RES, 0
R2411	0662057M01	RES, 0
R2430	0662057V35	RES, 200K
R2431	0662057V35	RES, 200K
R3001	0662057M01	RES, 0
R3002	0662057M01	RES, 0
R3003	SHORT_RES0201	SHORT
R3028	0662057U85	RES, 2.2K
R3029	0662057V13	RES, 27K
R3050	0662057M01	RES, 0
R3060	0662057M01	RES, 0
R3101	0662057M01	RES, 0
R3150	0662057M01	RES, 0
R3151	0662057M01	RES, 0
R3206	0662057M01	RES, 0
R3210	0662057V34	RES, 180K
R3211	0662057V25	RES, 82K
R3250DNP	0662057M01	RES, 0
R3350	0662057M01	RES, 0
R3400	0662057M01	RES, 0
R3550	0662057M01	RES, 0
R3560	0662057M01	RES, 0
R3650	0662057M78	RES, 1.5K
R3651	0662057M34	RES, 22
R3652	0662057M34	RES, 22
R3653	SHORT_RES0201	SHORT
R3654	SHORT_RES0201	SHORT
R3700	0662057M01	RES, 0

Table 4-18. Electrical Parts List - R38xx - R50xx

Reference Number	Part Number	Description
R3800	SHORT_RES0201	SHORT
R3850	0662057M01	RES, 0
R3851	0662057M01	RES, 0
R3950	0662057M01	RES, 0
R3960	0687874L01	RES, 0.24
R3961	0688044N02	RES, 20m
R3962	0662057M92	RES, 5.6K
R3963	0662057N30	RES, 200K
R3965	SHORT_RES0201	SHORT
R3990	0662057N23	RES, 100K
R3995	0662057V35	RES, 200K
R3997	0662057N23	RES, 100K
R3998DNP	0662057V35	RES, 200K
R4000	0662057M22	RES, 6.8
R4001	0662057M22	RES, 6.8
R4211	0662057N23	RES, 100K
R4212	0662057N23	RES, 100K
R4213	0662057N30	RES, 200K
R4214	0662057M01	RES, 0
R4305	0662057N07	RES, 22K
R4450	0662057M50	RES, 100
R4550	0662057M92	RES, 5.6K
R4900	0662057M74	RES, 1K
R4901	0662057N15	RES, 47K
R4902	0662057N33	RES, 270K
R4910	0662057M98	RES, 10K
R4911	0662057M98	RES, 10K
R4912	0662057N39	RES, 470K
R4913	0662057N15	RES, 47K
R4915	0662057N15	RES, 47K
R4916	0662057M90	RES, 4.7K
R4920	0662057M90	RES, 4.7K
R4950	0662057V43	RES, 330K
R4951	0662057V11	RES, 22K
R4952	0662057V02	RES, 10K
R4955	0662057V02	RES, 10K
R4956	0662057V17	RES, 39K
R5000	0662057N23	RES, 100K
R5001	0662057N15	RES, 47K
R5005	0662057N34	RES, 300K
R5006	0609591M49	RESNET, 100K
R5004DNP	0662057N23	RES, 100K
R5007DNP	0662057N23	RES, 100K
R500DNP	0662057M01	RES, 0

Table 4-19. Electrical Parts List - R50xx - R75xx

Reference Number	Part Number	Description
R5010	0662057M01	RES, 0
R5053	0662057M86	RES, 3.3K
R508DNP	0662057M01	RES, 0
R5100	0662057M98	RES, 10K
R5101	0662057M98	RES, 10K
R5102	0662057M98	RES, 10K
R5103	0662057M98	RES, 10K
R5104	0662057M98	RES, 10K
R5105	0662057M98	RES, 10K
R5106	0662057N34	RES, 300K
R5107	0662057M50	RES, 100
R512DNP	0662057M01	RES, 0
R514DNP	0662057M01	RES, 0
R5223	0662057M90	RES, 4.7K
R5225	0662057M26	RES, 10
R5241	0662057N20	RES, 75K
R5242	0662057N23	RES, 100K
R5243	0662057M98	RES, 10K
R5244	0662057M98	RES, 10K
R5304	0662057M14	RES, 3.3
R5401	0662057M90	RES, 4.7K
R5402	0662057M50	RES, 100
R5403	0662057M01	RES, 0
R5404DNP	0662057N30	RES, 200K
R5405DNP	0662057N30	RES, 200K
R5500	0662057M01	RES, 0
R5501	0662057M01	RES, 0
R5502	0662057M01	RES, 0
R5503	0662057M92	RES, 5.6K
R5600	2113743L17	CAP, 1000pF
R5601	0609591M37	RESNET, 10K
R5602	2409377M03	IDCTR, 6.8nH
R5604	0662057M78	RES, 1.5K
R5605	0662057N23	RES, 100K
R5608	0662057M98	RES, 10K
R5800	0662057M98	RES, 10K
R5801	0662057N20	RES, 75K
R5802	0662057M01	RES, 0
R6000	0662057U85	RES, 2.2K
R6001	0662057N23	RES, 100K
R6005	2113743N11	CAP, 2.4pF
R6006	0662057M01	RES, 0
R7501	0662057N23	RES, 100K
R7502	0662057M01	RES, 0

Table 4-20. Electrical Parts List - R75xx - U11xx

Reference Number	Part Number	Description
R7503	0662057M01	RES, 0
R7505	0662057M82	RES, 2.2K
R7506	0662057M82	RES, 2.2K
R7508	0662057N17	RES, 56K
R7509	0662057M98	RES, 10K
R7510	0662057M98	RES, 10K
R7511	0662057M82	RES, 2.2K
R7512	0662057M82	RES, 2.2K
R7513	0662057M01	RES, 0
R7514	0662057M01	RES, 0
R7520	0662057N27	RES, 150K
R7700	0662057M01	RES, 0
R7701	0662057V08	RES, 16K
R7702	0662057V07	RES, 15K
R7703	0662057V24	RES, 75K
R29524	0662057M01	RES, 0
R800DNP	0662057M01	RES, 0
R802DNP	0662057M01	RES, 0
S5100	4089775N02	SWITCH
SH1DNP	2688646Y01	SHIELD
SH30	2690077N02	SHIELD
SH200	2690076N01	SHIELD
SH300	2690075N01	SHIELD
SH400	2690074N01	SHIELD
SH3000	2690073N01	SHIELD
SH7500	2687327Y02	SHIELD
SW6000	0987378K01	SWITCH
T610	5885949K06	HHM1526
T620	5885949K06	HHM1526
T630	5885949K04	HHM1515
U01	5113837M44	NL17SZ16
U30	5109944C61	MC13820
U100	5188450M23	50M23
U200	5188450M21	50M21
U300	5109923D59	MC13778
U400	5189552N01	MMM5092
U500	5188450M26	PC13780
U600	5109923D61	23D61
U800	5188220Y02	20Y02
U880	5109768D08	LM20
U1000	5199154K04	DSPIO
U1110	5109522E53	NC7SZ125
U1120	5114000M64	MC74VHC1G09
U1140	5164751E01	MC74VHC1GT50

Table 4-21. Electrical Parts List - U11xx - VS50xx

Reference Number	Part Number	Description
U1150	5109522E82	NC7SB3157
U1160	5109522E60	TC7SZ08FU
U1161	5113837M40	NL17SZ00
U1162	5113837M42	NL17SZ32
U1310	5103670B05	28F128L18
U1400	5109509A66	MT48H4M16LF
U2000	5189251L05	OMAP1510
U2020	5109522E60	TC7SZ08FU
U2021	5109522E60	TC7SZ08FU
U2030	5109522E53	NC7SZ125
U2040	5109522E25	TC7SH02FU
U2070	5109522E16	TC7W74FU
U2100	5109522E82	NC7SB3157
U2300	5199174J01	PF48F4400
U2400	5109509A68	HYE25L256160AF
U3000	5185941F02	TWL93010DGZGR
U3021	5188221Y01	LP3983
U3206	5188128Y01	TPS62021
U4210	5109731C42	TPA2010D1
U4211	5109522E60	TC7SZ08FU
U5000	5109817F58	17F58
U5001	4889526L13	CSPEMI307AG
U5002	5109522E82	NC7SB3157
U5003	4889526L12	CSPEMI306AG
U5004	5109522E82	NC7SB3157
U5005	5109522E82	NC7SB3157
U5220	5187970L55	LT3465
U5500	4809948D49	CSPESD304G
U5600	4889695L14	95L14
U5602	5109522E53	NC7SZ125
U6000	5109841C71	GPS
U6030	5109522E53	NC7SZ125
U7500	5188536Y01	OV610
U7700	5109512F46	ILC7081
U9532	2113743M24	CAP, 0.1uF
U9560	2113928C12	CAP, 10uF
U9567	0662057M01	RES, 0
U9568	0662057M01	RES, 0
U9717	5109522E82	NC7SB3157
VS4200	4809788E06	UDZTE-176.8B
VS4201	4809788E06	UDZTE-176.8B
VS4210DNP	4809948D49	CSPESD304G
VS4300	4809948D49	CSPESD304G
VS5000	4809788E17	EDZ68B

Table 4-22. Electrical Parts List - VS50xx - Y39xx

Reference Number	Part Number	Description
VS5001	4813830C29	MMSZ5246B
VS5002	4809788E17	EDZ68B
VS5003	4809788E17	EDZ68B
VS5004	4813830C29	MMSZ5246B
VS5105	4809948D49	CSPESD304G
VS5110	4809948D49	CSPESD304G
VS5111	4809948D49	CSPESD304G
VS5112	4809948D49	CSPESD304G
VS5120	4809948D49	CSPESD304G
VS5121	4809948D49	CSPESD304G
VS5122	4809948D49	CSPESD304G
VS5200	4809948D49	CSPESD304G
VS5201	4809948D49	CSPESD304G
VS5203	4809948D49	CSPESD304G
VS5204	4809948D49	CSPESD304G
VS5205	4809948D49	CSPESD304G
VS5206	4809948D49	CSPESD304G
VS5207	4809948D49	CSPESD304G
VS5403	4809948D49	CSPESD304G
VS5402DNP	4809788E17	EDZ68B
VS5800	4809948D49	CSPESD304G
VS7501	4809948D49	CSPESD304G
VS7502	4809948D49	CSPESD304G
VS7503	4809948D49	CSPESD304G
VS7504	4809948D49	CSPESD304G
VS7505	4809948D49	CSPESD304G
VS7506	4809948D49	CSPESD304G
Y500	4809718L20	TCO-5871
Y2000	4809612J45	CX-91F
Y3982	4809995L13	CC5V